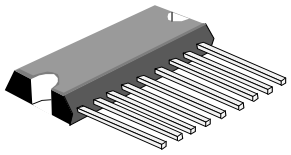
2 x 6 WATT STEREO POWER AMPLIFIER

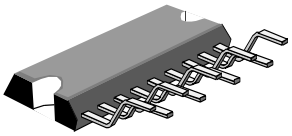
KKA1519

The KKA1519B, KKA1519B1, KKA1519B1Q is an integrated class-B dual output amplifier in a 9-lead single in-line (SIL) plastic medium power package. The device is primarily developed for car radio applications.

ORDERING INFORMATION



KKA1519B1 → SOT131-2



KKA1519B1Q → SOT157-2

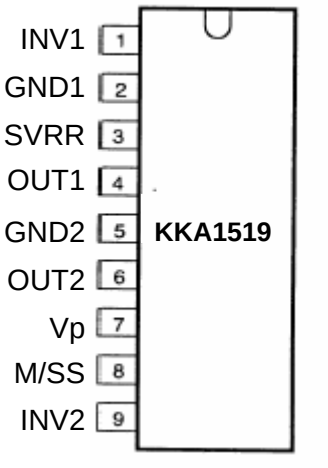
T_A = -55° to 125° C for all packages

Features

Requires very few external components
High output power
Fixed gain
Good ripple rejection
Mute/stand-by switch
Load dump protection
Thermally protected
Thermally protected
Reverse polarity safe
Compatible with TDA1517 (except gain)
No switch-on/switch-off plop
Protected against electrostatic discharge
Capability to handle high energy on outputs (Vp = 0 V)

PINNING

1	INV1	non-inverting input 1
2	GND1	ground (signal)
3	SVRR	supply voltage ripple rejection
4	OUT1	output 1
5	GND2	ground (substrate)
6	OUT2	output 2
7	Vp	supply voltage
8	M/SS	mute/stand-by switch
9	INV2	non-inverting input 2



QUICK REFERENE DATA

parameter	conditions	symbol	min.	typ.	max.	unit
Supply voltage range						
operating		V_p	6,0	14,4	18,0	V
non-operating		V_p	-	-	30	V
load dump protected		V_p	-	-	45	V
Repetitive peak output current		I_{ORM}	-	-	2,5	A
Total quiescent current		I_{tot}		40	80	mA
Stand-by current		I_{sb}		0,1	100	mA
Switch-on current		I_{sw}			40	mA
Input impedance		$/Z_1/$	50			kΩ
Output power	THD= 0,5%;4 Ω			5		W
	THD=10%;4 Ω			6		W
Channel separation		α	40			dB
Noise output voltage		$V_{no(rms)}$			150	μV
Supply voltage ripple rejection	f=100Hz	SVRR	40			dB
	f=1kHz to 10 kHz	SVRR	48			dB
Crystal temperature		Tc			150	^{0}C

DC CHARACTERISTICS (note 1) Vp = 14,4 V; Tamb = 25 ^{o}C; unless otherwise specified

parameter	conditions	symbol	min.	Typ.	max.	unit
Supply						
Supply voltage range	note 2	Vp	6,0	14,4	18,0	V
Quiescent current		IP	-	40	80	mA
DC output voltage	note 3	V_O	-	6,95	-	V
Mute/stand-by switch						
Switch-on voltage level	see Fig.3	VON	8,5	-	-	V
Mute condition		Vmute	3,3	-	6,4	V
Output signal in mute position	V_I = 1 V (max.); f = 20 Hz to 15 kHz	V_O	-	-	20	mV
Stand-by condition		Vsb	0	-	2 100	V
DC current in stand-by condition		Isb	-	-	40	μA
Switch-on current		Isw	-	12		μA

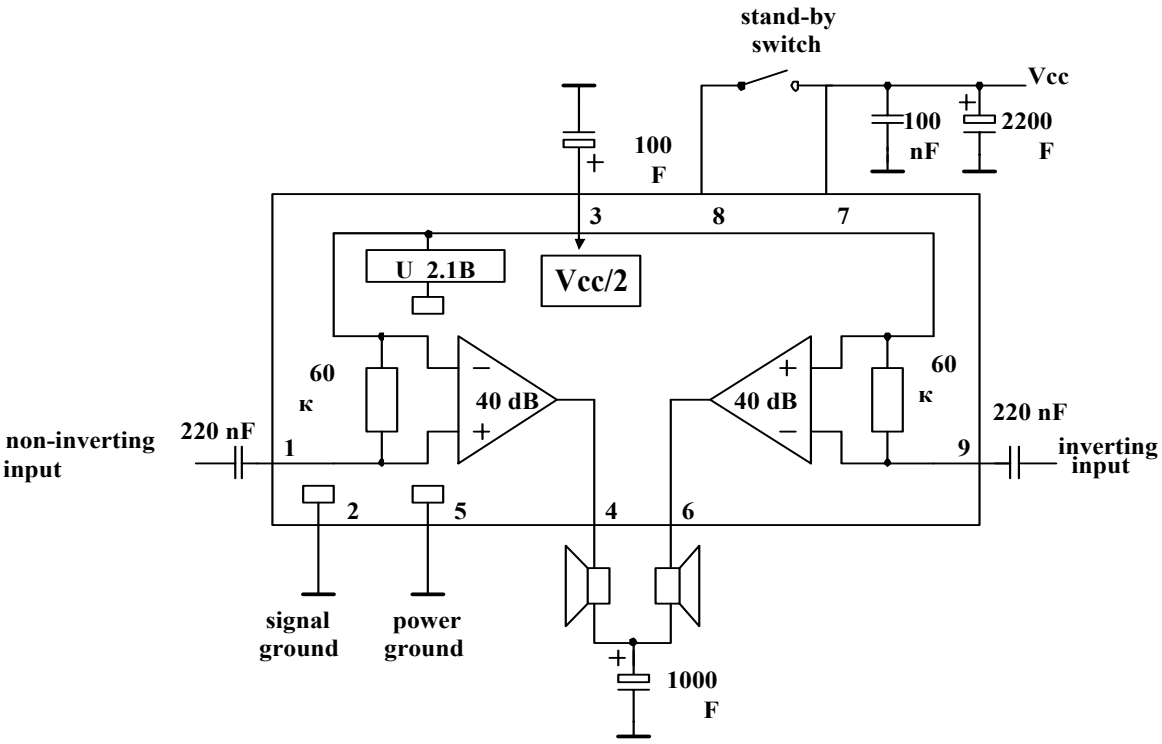
AC CHARACTERISTICS (note 1)

Vp=14,4V; R_L=4Ω; f=1kHz; Tamb=25°C unless otherwise specified

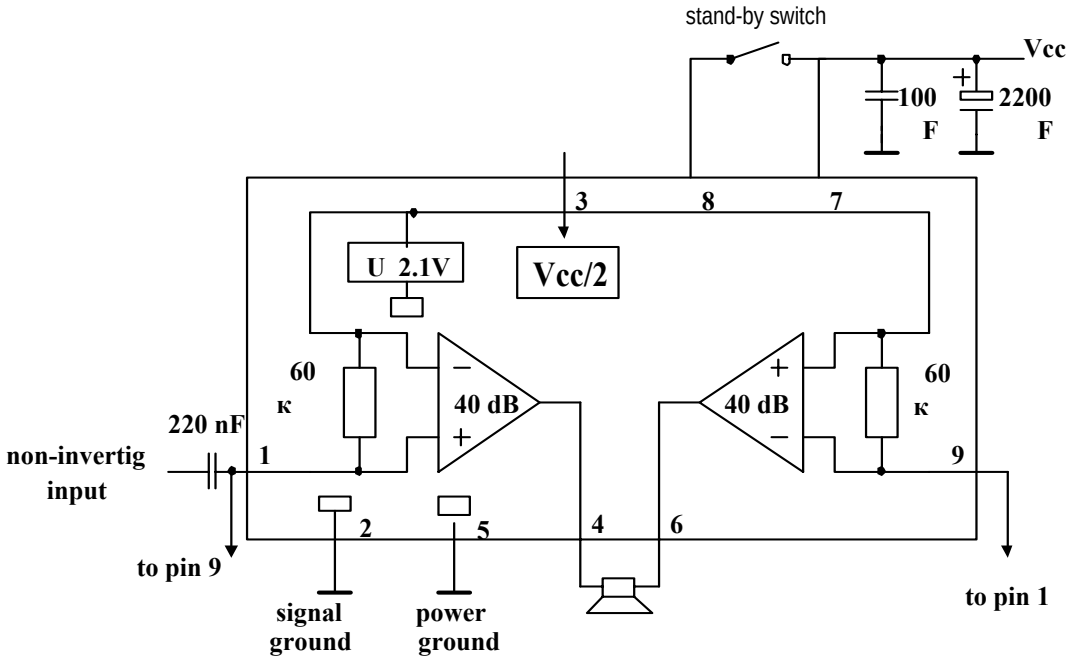
parameter	conditions	symbol	min.	typ.	max.	unit
Output power	note 4;					
	THD = 0,5%	P_O	4	5	-	W
	THD = 10%	P_O	5,5	6,0	-	W
Total harmonic distortion	P_O=1W	THD	-	0,1	-	%
Low frequency roll-off	note 5;					
	-3 dB	f_L	-	45	-	Hz
High frequency roll-off	-1 dB	f_H	20	-	-	kHz
Closed loop voltage gain		G_V	39	40	41	dB
Supply voltage ripple rejection						
	note 6					
ON						
ON	f= 100 Hz	SVRR	40	-	-	dB
	f= 10 Hz to 10 kHz	SVRR	48	-	-	dB
mute		SVRR	48	-	-	dB
stand-by		SVRR	80	-	-	dB
Input impedance		lZil	50	60	75	kΩ
Noise output voltage	note 7;					
ON	R_S=0Ω	Vno(rms)	-	150	-	mV
ON	R_S= 10 kΩ	Vno(rms)	-	250	500	mV
mute	note 8	Vno(rms)	-	120	-	mV
Channel separation	R_S= 10 kΩ	a	40	-	-	dB
Channel balance		lDGvl	-	0,1	1	dB

Notes to the characteristics

1. All characteristics are measured using the circuit shown in Fig. 4.
2. The circuit is DC adjusted at Vp= 6V to 18V and AC operating at Vp= 8,5V to 18 V.
3. At 18 V < Vp< 30 V the DC output voltage **<** Vp/2.
4. Output power is measured directly at the output pins of the IC.
5. Frequency response externally fixed.
6. Ripple rejection measured at the output with a source impedance of 0 ^ (maximum ripple amplitude of 2 V) and a frequency between 100 Hz and 10 kHz.
7. Noise voltage measured in a bandwidth of 20 Hz to 20 kHz.
8. Noise output voltage independent of R^ (V j = 0 V).



Stereo application circuit diagram



BTL application circuit diagram

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit ≥-55°C	Guaranteed Limit 25°C	Guaranteed Limit ≤125 °C	Unit
V_{IH}	Minimum High-Level Input Voltage	V_{OUT}=0.5 V or V_{CC} - 0.5 V	5.0	3.5	3.5	3.5	V
		V_{OUT}=1.0 V or V_{CC} - 1.0 V	10	7	7	7	
		V_{OUT}=1.5 V or V_{CC} - 1.5 V	15	11	11	11	
V_{IL}	Maximum Low - Level Input Voltage	V_{OUT}=0.5 V or V_{CC} - 0.5 V	5.0	1.5	1.5	1.5	V
		V_{OUT}=1.0 V or V_{CC} - 1.0 V	10	3	3	3	
		V_{OUT}=1.5 V or V_{CC} - 1.5 V	15	4	4	4	
V_{OH}	Minimum High-Level Output Voltage	V_{IN}=GND or V_{CC}	5.0	4.95	4.95	4.95	V
			10	9.95	9.95	9.95	
			15	14.95	14.95	14.95	
		V_{IL}=1.5V, V_{IH}=3.5V, I_O=-1μA	5.0	4.5	4.5	4.5	
		V_{IL}=3.0V, V_{IH}=7.0V, I_O=-1μA	10	9.0	9.0	9.0	
		V_{IL}=4.0V, V_{IH}=11V, I_O=-1μA	15	13.5	13.5	13.5	
V_{OL}	Maximum Low-Level Output Voltage	V_{IN}=GND or V_{CC}	5.0	0.05	0.05	0.05	V
			10	0.05	0.05	0.05	
			15	0.05	0.05	0.05	
		V_{IL}=1.5V, V_{IH}=3.5V, I_O=1μA	5.0	0.5	0.5	0.5	
		V_{IL}=3.0V, V_{IH}=7.0V, I_O=1μA	10	1.0	1.0	1.0	
		V_{IL}=4.0V, V_{IH}=11V, I_O=1μA	15	1.5	1.5	1.5	
I_{IN}	Maximum Input Leakage Current	V_{IN}= GND or V_{CC}	18	±0.1	±0.1	±1.0	μA
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_{IN}= GND or V_{CC}	5.0	1	1	30	μA
			10	2	2	60	
			15	4	4	120	
			20	20	20	600	
I_{OL}	Minimum Output Low (Sink) Current	V_{IN}= GND or V_{CC}					mA
		U_{OL}=0.4 V	5.0	0.64	0.51	0.36	
		U_{OL}=0.5 V	10	1.6	1.3	0.9	
		U_{OL}=1.5 V	15	4.2	3.4	2.4	
I_{OH}	Minimum Output High (Source) Current	V_{IN}= GND or V_{CC}					mA
		U_{OH}=2.5 V	5.0	-2.0	-1.6	-1.15	
		U_{OH}=4.6 V	5.0	-0.64	-0.51	-0.36	
		U_{OH}=9.5 V	10	-1.6	-1.3	-0.9	
		U_{OH}=13.5 V	15	-4.2	-3.4	-2.4	

AC ELECTRICAL CHARACTERISTICS (C_L=50pF, R_L=200 kΩ, Input t_r=t_f=20 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit ≥-55°C	Guaranteed Limit 25°C	Guaranteed Limit ≤125°C	Unit
f_{max}	Maximum Clock Frequency (Figure 1)	5.0 10 15	3.5 8 12	3.5 8 12	3.0 6 10	MHz
t_{PLH}, t_{PHL}	Maximum Propagation Delay, Clock to Q or $\overline{Q}$ (Figure 1)	5.0 10 15	300 130 90	300 130 90	450 200 150	ns
t_{PLH}	Maximum Propagation Delay, Set to Q or Reset to Q ($\overline{F}$igure 2)	5.0 10 15	300 130 90	300 130 90	450 200 150	ns
t_{PHL}	Maximum Propagation Delay, Set to $\overline{Q}$ or Reset to Q (Figure 2)	5.0 10 15	400 170 120	400 170 120	600 250 150	ns
t_{TLH}, t_{THL}	Maximum Output Transition Time, Any Output (Figure 1)	5.0 10 15	200 100 80	200 100 80	250 150 100	ns
C_{IN}	Maximum Input Capacitance	5.0		7.5		pF

TIMING REQUIREMENTS(C_L=50pF, R_L=200 kΩ, Input t_r=t_f=20 ns)

Symbol	Parameter	V_{CC} V	Guaranteed Limit ≥-55°C	Guaranteed Limit 25°C	Guaranteed Limit ≤125°C	Unit
t_w	Minimum Pulse Width, Clock (Figure 1)	5.0 10 15	140 60 40	140 60 40	200 80 50	ns
t_w	Minimum Pulse Width, Set or Reset (Figure 2)	5.0 10 15	180 80 50	180 80 50	250 120 80	ns
t_{su}	Minimum Setup Time, Data to Clock (Figure 3)	5.0 10 15	40 20 15	40 20 15	40 20 15	ns
t_h	Minimum Hold Time, Clock to Data (Figure 3)	5.0 10 15	5 5 5	5 5 5	8 5 5	ns
t_r, t_f	Maximum Input Rise or Fall Time, Clock (Figure 1)	5.0 10 15	500 30 6	500 30 6	500 30 6	μs

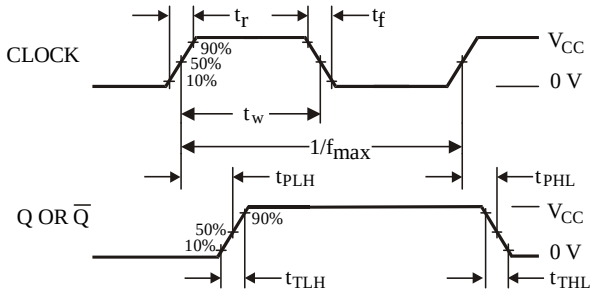


Figure 1. Switching Waveforms

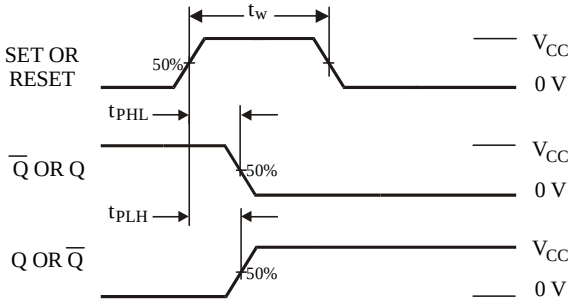


Figure 2. Switching Waveforms

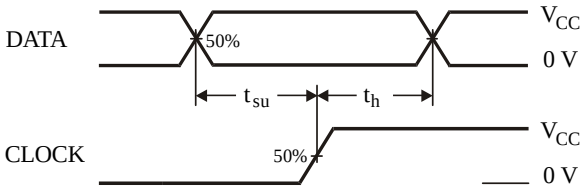
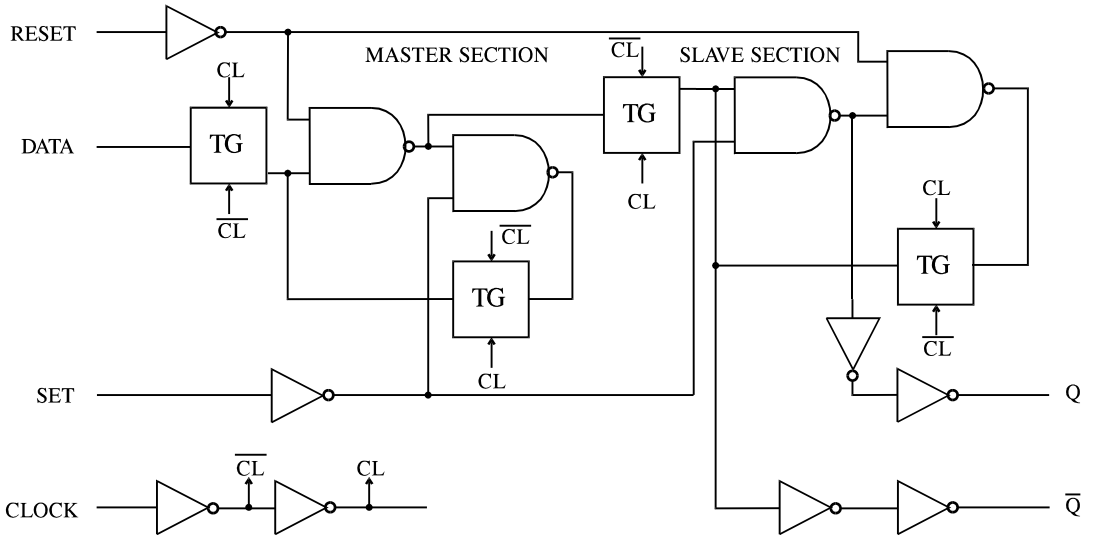
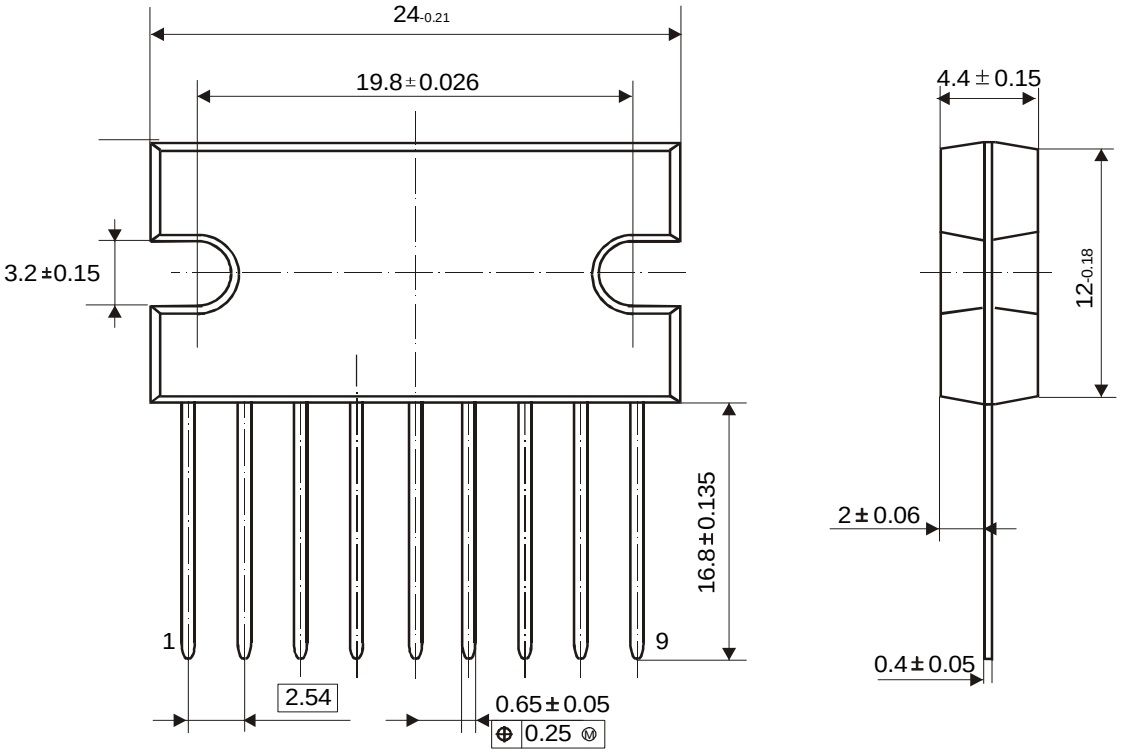


Figure 3. Switching Waveforms

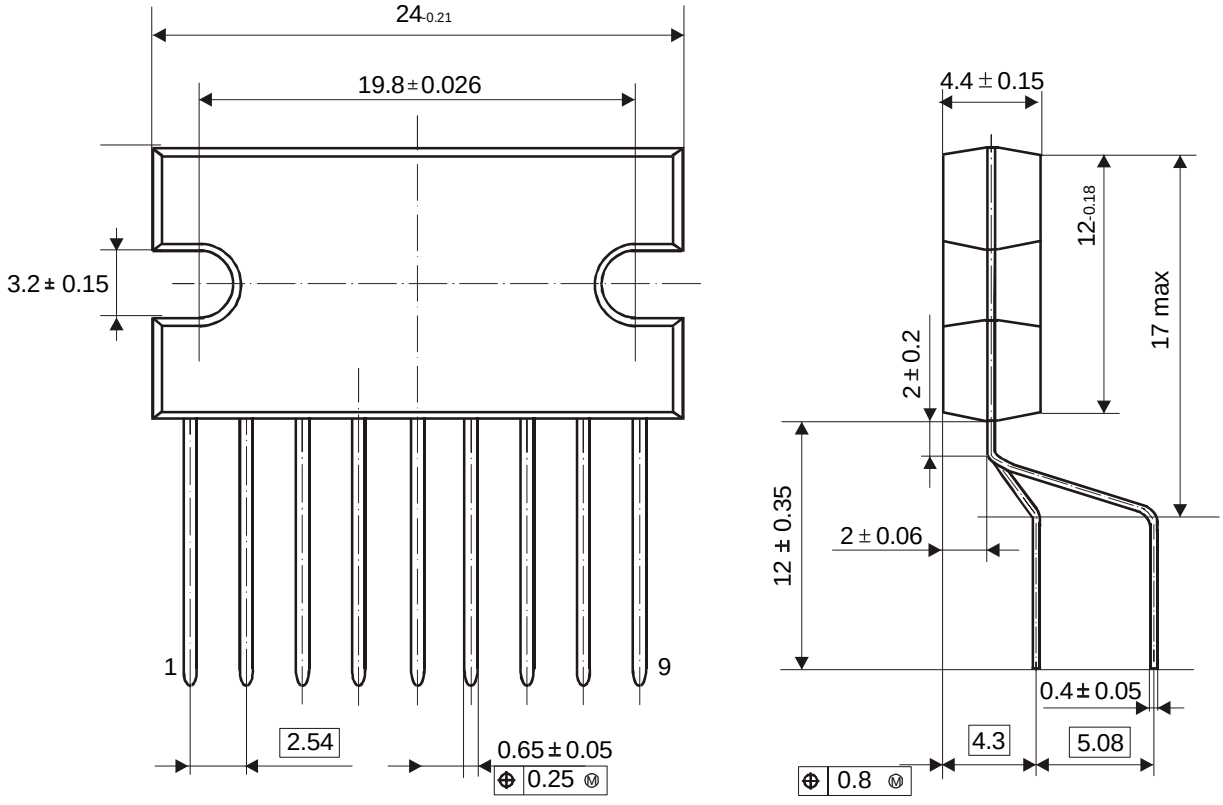
EXPANDED LOGIC DIAGRAM
(1/2 of the Device)



- **9-Pin Plastic Power Single-in-Line (SIL-9MPF, SOT 131-2)**



- **9-Pin Plastic Power DIL-Bent-SIL (SIL-9P, SOT 157-2)**



- **9-Pin Plastic Power Single-in-Line (SIL-9MPF, SOT 110-1)**