

**KKA6083**

**PWM Power Control with Interference Suppression**

**Description**

KKA6083 is a PWM IC in bipolar technology for the control of an N-channel power MOSFET used as a high side switch. The IC is ideal for the use in the brightness control (dimming) of lamps e.g., in dashboard applications.

**Features**

- Pulse width modulation up to 2 kHz clock frequency
- Protection against short circuit, load dump over-voltage and reverse  $V_S$
- Duty cycle 15 to 100% continuously
- Reduced internal pulse slope of lamp's voltage
- High side switch
- Interference and damage protection according to VDE 0839 and ISO/TR 7637/1.
- Charge pump noise suppressed
- Ground wire breakage protection
- Low interference voltage

Case: DIP 8

**Block Diagram**

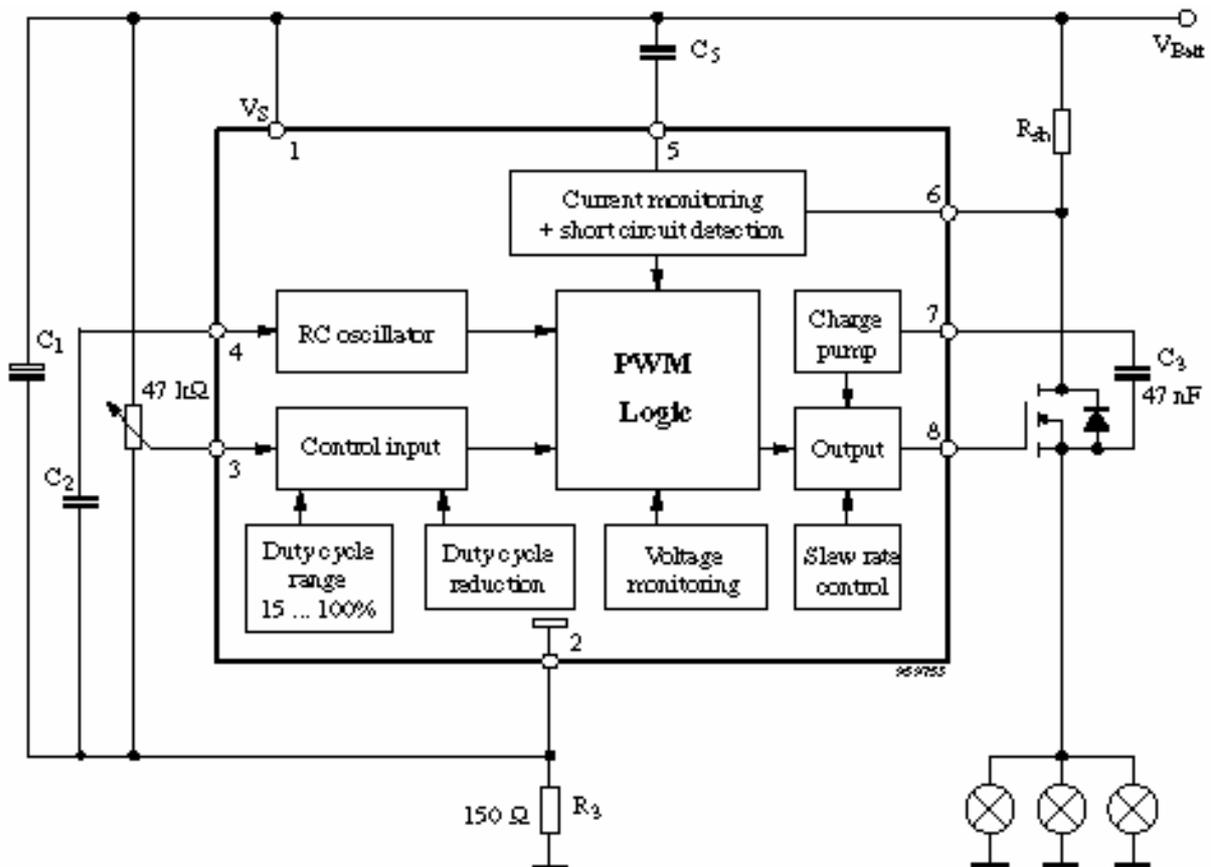
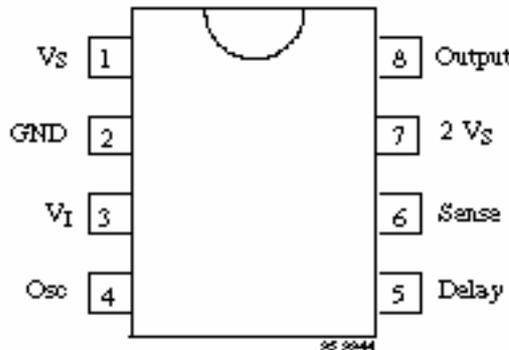


Figure 1. Block diagram with external circuit

## Pin Description



Pin	Symbol	Function
1	V <sub>S</sub>	Supply voltage V <sub>S</sub>
2	GND	IC ground
3	V <sub>T</sub>	Control input (duty cycle)
4	Osc	Oscillator
5	Delay	Short circuit protection delay
6	Sense	Current sensing
7	2 V <sub>S</sub>	Voltage doubler
8	Output	Output

## Functional Description

### Supply Voltage, V<sub>S</sub> or V<sub>Batt</sub>, Pin 1

### GND Pin 2

### Control Input, Pin 3

The pulse width is controlled by means of an external potentiometer (47 kΩ). The characteristic (angle of rotation/duty cycle) is linear. The duty cycle can be varied from 15 to 100%. It can be reduced by increasing the supply voltage as from V<sub>Batt</sub> > 13 V. This produces a power reduction in the FET and increases the life time of lamps. It is possible to further restrict the duty cycle with the resistors R<sub>1</sub> and R<sub>2</sub>.

Pin 3 is protected against short-circuit to V<sub>Batt</sub> and ground GND (V<sub>Batt</sub> ≤ 16.5 V).

### Oscillator, Pin 4

The oscillator determines the frequency of the output voltage. This is defined by an external capacitor, C<sub>2</sub>. It is charged with a constant current, I<sub>1</sub> until the upper switching threshold is reached. A second current source is then activated which taps a double current, 2 I<sub>1</sub>, from the charging current. The capacitor, C<sub>2</sub> is thus discharged by the current, I<sub>1</sub> until the lower switching threshold is reached. The second source is then switched off again and the procedure starts once more.

Example for oscillator frequency calculation:

$$V_{T100} = V_0 \cdot \alpha_1 = (V_{Zener} - I_0 \cdot R_s) \cdot \alpha_1$$

$$V_{T<100} = V_0 \cdot \alpha_2 = (V_{Zener} - I_0 \cdot R_s) \cdot \alpha_2$$

$$V_{II} = V_0 \cdot \alpha_3 = (V_{Zener} - I_0 \cdot R_s) \cdot \alpha_3$$

whereas

V<sub>T100</sub> - High switching threshold (100% duty cycle)

V<sub>T<100</sub> - High switching threshold (< 100% duty cycle)

V<sub>II</sub> - Low switching threshold

α<sub>1</sub>, α<sub>2</sub> and α<sub>3</sub> are fixed constant.

The above mentioned threshold voltages are calculated for the following values given in the data sheet.

$$V_{Batt} = 12 \text{ V}, I_0 = 4 \text{ mA}, R_s = 150 \Omega,$$

$$\alpha_1 = 0.7, \alpha_2 = 0.67 \text{ and } \alpha_3 = 0.28.$$

$$V_{T100} = (12 \text{ V} - 4 \text{ mA} \cdot 150 \Omega) \cdot 0.7 \approx 8 \text{ V}$$

$$V_{T<100} = 11.4 \text{ V} \cdot 0.67 = 7.6 \text{ V}$$

$$V_{II} = 11.4 \text{ V} \cdot 0.28 = 3.2 \text{ V}$$

For a duty cycle of 100%, an oscillator frequency, f, is as follows:

$$f = \frac{I_{oss}}{2 \cdot (V_{T100} - V_{II}) \cdot C_2}, \text{ whereas } C_2 = 68 \text{ nF} \text{ and } I_{oss} = 45 \mu\text{A}$$

Therefore:

$$f = \frac{45 \mu\text{A}}{2 \cdot (8 \text{ V} - 3.2 \text{ V}) \cdot 68 \text{ nF}} = 69 \text{ Hz}$$

For a duty cycle of less than 100%, the oscillator frequency, f, is as follows:

$$f = \frac{I_{oss}}{2 \cdot (V_{T<100} - V_{II}) \cdot C_2 + 2 \cdot V_{Zener} \cdot C_4}$$

whereas C<sub>4</sub> = 0.1 = 45 μA and C<sub>2</sub> = 68 nF

$$\frac{45 \mu\text{A}}{2 \cdot (7.6 \text{ V} - 3.2 \text{ V}) \cdot 68 \text{ nF}} = 75$$

But when C<sub>4</sub> = 1.8 nF then

$$f = \frac{45 \mu\text{A}}{2 \times (7.6 \text{ V} - 3.2 \text{ V}) \times 68 \text{ nF} + 2 \times 12 \text{ V} \times 1.8 \text{ nF}} = 70 \text{ Hz}$$

By selecting different values of C<sub>2</sub> and C<sub>4</sub>, it is possible to have a range of oscillator frequency, f, from 10 to 2000 Hz as shown in the data sheet.

## Output Slope Control

The slope of the lamp voltage is internally limited to reduce radio interference, by limitation of the open loop voltage gain of the PWM comparator.

This means the voltage rise on the lamp is proportional to the oscillator voltage increase at the switch over time multiplied with the corresponding amplification.

$$dV_g/dt = \alpha_4 \cdot dV_d/dt = 2 \cdot \alpha_4 \cdot f \cdot (V_{TX} - V_{TL}) \cdot (V_{Batt} - I_S \cdot R_3)$$

when  
 $f = 75 \text{ Hz}$ ,  $V_{TX} = V_T < 100$  and  $\alpha_4 = 63$  ( $(63 \cdot R)/R$ )  
 we obtain  
 $dV_g/dt = 2 \cdot 63 \cdot 75 \cdot (0.67 - 0.28) \cdot (12 - 4 \text{ mA} \cdot 150) = 42 \text{ V/ms}$

With an external capacitor,  $C_4$ , the slope can be further reduced as follows:

$$dV_g/dt = I / (C_4 + C_2/\alpha_4)$$

when  
 $I = 45 \text{ } \mu\text{A}$ ,  $C_4 = 1.8 \text{ nF}$ ,  $C_2 = 68 \text{ nF}$  and  $\alpha_4 = 63$   
 then  $dV_g/dt = 45 \text{ } \mu\text{A} / (1.8 \text{ nF} + 68 \text{ nF}/63) = 15.6 \text{ V/ms}$

To damp oscillation tendencies, a resistance of 100  $\Omega$  in series with capacitance,  $C_4$ , is recommended.

## Interference Suppression

"on board" radio reception according to VDE 0879 part 3/4.81

Test conditions:

Application circuit according to figure 2.

Load: nine 4 W lamps in parallel.

Duty cycle = 18%  
 $V_{Batt} = 12 \text{ V}$   
 $f_{Qec} = 100 \text{ Hz}$

## Overvoltage Detection

Stage 1:

If overvoltages  $V_{Batt} > 20 \text{ V}$  (typ) occur, the external transistor is switched off and on at  $V_{Batt} < 18.5 \text{ V}$  (hysteresis).

Stage 2:

If  $V_{Batt} > 28.5 \text{ V}$  (typ), the voltage limitation of the IC is reduced from 26 V to 20 V. The gate of the external transistor remains at the potential of the IC ground, thus producing voltage sharing between FET and lamps in the event of overvoltage pulses occurring (e.g. load dump). The short-circuit protection is not in operation. At  $V_{Batt}$  approx.  $< 23 \text{ V}$ , the overvoltage detection stage 2 is switched off.

$$V_{Lamp} = V_{Batt} - V_S - V_{GS}$$

$V_S$  = Supply voltage of the IC at overvoltage detection stage 2  
 $V_{GS}$  = Gate - source voltage of the FET

## Short-Circuit Protection and Current Sensing, Pins 5 and 6

1. Short-Circuit Detection and Time Delay,  $t_d$

The lamp current is monitored by means of an external shunt resistor. If the lamp current exceeds the threshold for the short-circuit detection circuit ( $V_{T2} \approx 90 \text{ mV}$ ), the duty cycle is switched over to 100% and the capacitor  $C_5$  is charged by a current source of  $10 \text{ } \mu\text{A}$  ( $I_{dis} - I_h$ ). The external FET is switched off after the cut-off threshold ( $V_{TL}$ ) is reached. Renewed switching on of the FET is possible only after a power-on reset. The current source,  $I_{dis}$ , ensures that the capacitor  $C_5$  is not charged by parasitic currents.

Time delay,  $t_d$  is as follows:

$$t_d = C_5 \times V_{TL} / (I_{dis} - I_h)$$

With  $C_5 = 100 \text{ nF}$  and  $V_{TL} = 10.4 \text{ V}$ ,  $I_{dis} = 13 \text{ } \mu\text{A}$ ,  $I_h = 3 \text{ } \mu\text{A}$ , we have

$$t_d = 100 \text{ nF} \cdot 10.4 \text{ V} / (13 \text{ } \mu\text{A} - 3 \text{ } \mu\text{A}) = 104 \text{ ms}$$

2. Current limitation:

The lamp current is limited by a control amplifier to protect the external power transistor. The voltage drop across an external shunt resistor acts as the measured variable. Current limitation takes place for a voltage drop of  $V_{T1} \approx 100 \text{ mV}$ . Owing to the difference  $V_{T1} - V_{T2} \approx 10 \text{ mV}$ , it is ensured that current limitation

occurs only when the short-circuit detection circuit has responded.

After a power-on reset, the output is inactive for half an oscillator cycle. During this time the supply voltage capacitor can be charged so that current limitation is guaranteed in the event of a short-circuit when the IC is switched on for the first time.

### Charge Pump and Output, Pins 7 and 8

Output, Pin 8, is suitable for controlling a power MOSFET. During the active integration phase, the supply current of the operational amplifier is mainly supplied by the capacitor  $C_3$  (bootstrapping). In addition, a trickle charge is generated by an integrated oscillator

( $f_1 \approx 400$  kHz) and a voltage doubler circuit. This permits a gate voltage supply at a duty cycle of 100%.

#### Undervoltage Detection

In the event of voltages of approximately  $V_{Batt} < 5.0$  V, the external FET is switched off and the latch for short-circuit detection is reset.

A hysteresis ensures that the FET is switched on again at approximately  $V_{Batt} > 5.4$  V.

#### Ground-Wire Breakage

To protect the FET in the case of ground-wire breakage, a 820 k $\Omega$  resistor between gate and source it is recommended to provide proper switch-off conditions.

## Absolute Maximum Ratings

Parameters	Symbol	Value	Unit
Supply voltage	$V_S$	25	V
Junction temperature	$T_j$	150	$^{\circ}\text{C}$
Ambient temperature range	$T_{amb}$	-40 to +110	$^{\circ}\text{C}$
Storage temperature range	$T_{str}$	-55 to +125	$^{\circ}\text{C}$

## Thermal Resistance

Parameters	Symbol	Value	Unit
Junction ambient	$R_{thJA}$	120	K/W

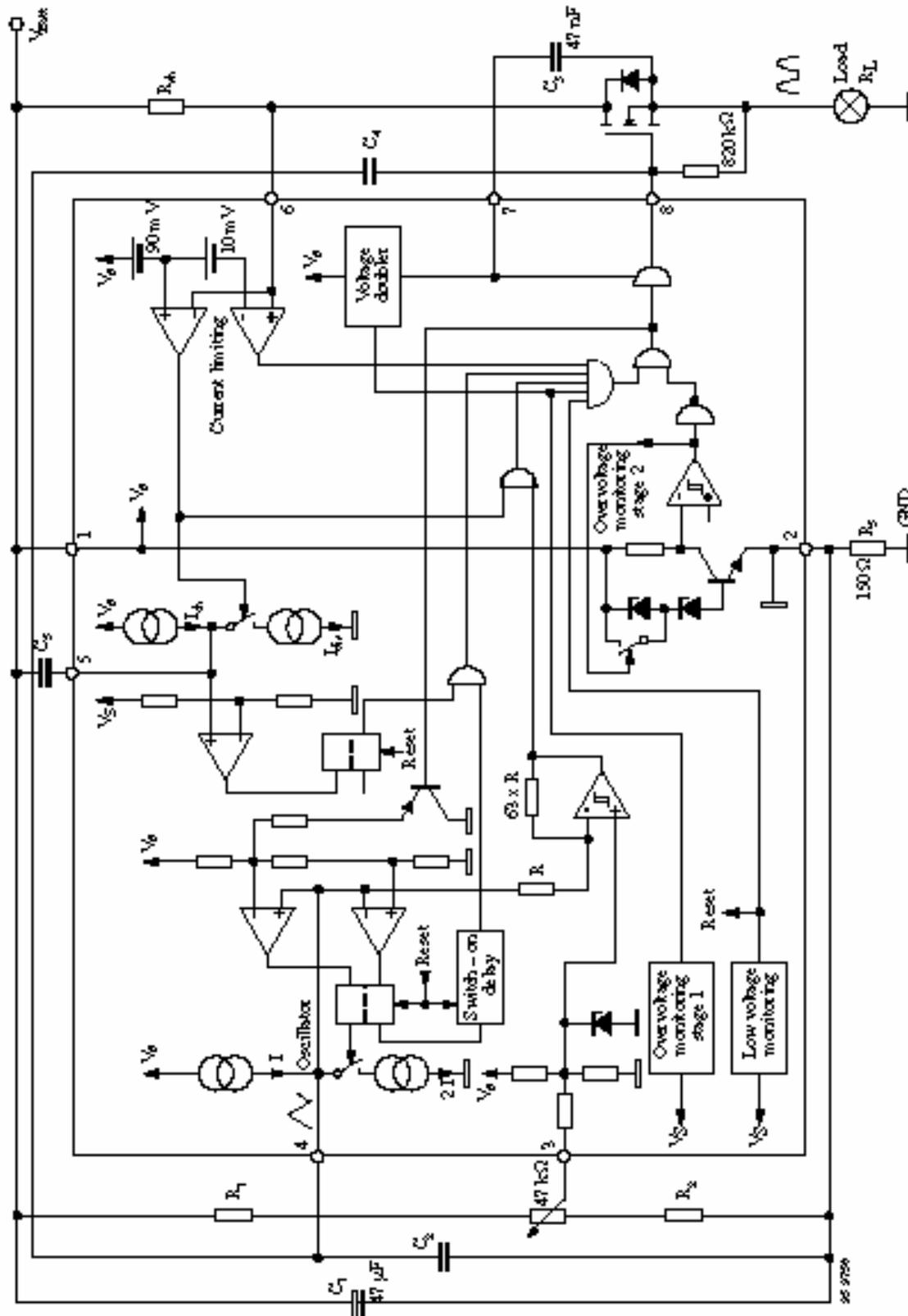
## Electrical Characteristics

$T_{amb} = -40$  to  $+110^{\circ}\text{C}$ ,  $V_{Batt} = 9$  to  $16.5$  V, (Basic function is guaranteed between  $6.0$  V to  $9.0$  V) reference point GND, unless otherwise specified (see figure 1).

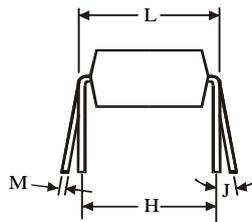
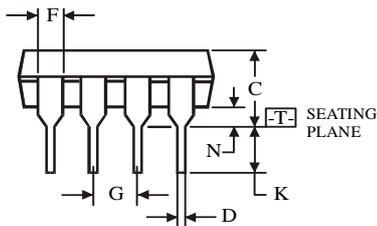
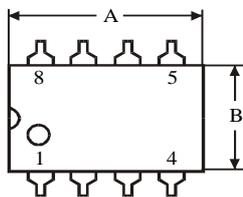
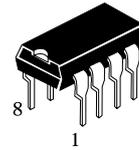
Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Current consumption	Pin 1	$I_S$			7.9	mA
Supply voltage	Oversvoltage detection, stage 1	$V_{Batt}$			25	V
Stabilized voltage	$I_S = 10$ mA Pin 1	$V_Z$	24.5		27.0	V
Battery undervoltage detection	- on	$V_{Batt}$	4.4	5.0	5.6	V
	- off		4.8	5.4	6.0	

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit	
Oscillator f = 10 to 2000 Hz Pin 4							
Threshold cycle	Upper	$V_{\theta}$ High, $\alpha_1$ , $\frac{V_{T100}}{V_S}$	$\alpha_1$	0.68	0.7	0.72	
	Lower	$V_{\theta}$ Low, $\alpha_2$ , $\frac{V_{T<100}}{V_S}$	$\alpha_2$	0.65	0.67	0.69	
		$\alpha_3$ , $\frac{V_{TH}}{V_S}$	$\alpha_3$	0.26	0.28	0.3	
Oscillator current	$V_{Bat} = 12\text{ V}$	$\pm I_{osc}$	34	45	54	$\mu\text{A}$	
Frequency	$C_4$ open, $C_2 = 68\text{ nF}$ , duty cycle = 50%	$\Delta f$	56	75	90	Hz	
Battery overvoltage detection Pin 8							
Stage 1:	Gate output: - switched off - switched on	$V_{Bat}$	18.3 16.7	20.0 18.5	21.7 20.3	V	
Stage 2: Detection stage 2	- on - off	$V_{Bat}$	25.5 19.5	28.5 23.0	32.5 26.5	V	
Stabilized voltage	$I_S = 30\text{ mA}$ Pin 1	$V_Z$	18.5	20.0	21.5	V	
Gate output Pin 8							
Voltage	Low level	$V_{\theta}$	0.35	0.70	0.95	V	
	$V_{Bat} = 16.5\text{ V}$ , $T_{amb} = 110^\circ\text{C}$ , $R_{\theta} = 150\ \Omega$				15		
	High level, duty cycle 100%	$V_{\theta}$		$V_1$			
Current	$V_{\theta} = \text{Low level}$	$I_{\theta}$	1.0			mA	
	$V_{\theta} = \text{High level}$ , $I_T >  I_{\theta} $		-1.0				
Duty cycle	Min: $C_2 = 68\text{ nF}$	$\psi/T$	15	18	21	%	
	Max: $V_{Bat} \leq 12.4\text{ V}$		100				
	$V_{Bat} = 16.5\text{ V}$ , $C_2 = 68\text{ nF}$ Pin 8		65	73	81		
Short-circuit protection Pin 6							
Short-circuit current regulation	$V_{T1} = V_S - V_{\theta}$	$V_{T1}$	85	100	120	mV	
Short-circuit detection	$V_{T2} = V_S - V_{\theta}$	$V_{T2}$	75	90	105	mV	
		$V_{T1} - V_{T2}$	3	10	30		
Short circuit recognition, $V_{Bat} = 12\text{ V}$ Pin 5							
Switched off threshold	$V_{TL} = V_S - V_S$	$V_{TL}$	10.2	10.4	10.6	V	
Charge current		$I_{ch}$		13		$\mu\text{A}$	
Discharge current		$I_{dis}$		3		$\mu\text{A}$	
Capacitance current	$I_S = I_{ch} - I_{dis}$	$I_S$	5	10	15	mA	
Voltage doubler Pin 7							
Voltage	Duty cycle 100%	$V_1$	$2 V_S$				
Oscillator frequency		$f_7$	280	400	520	kHz	
Internal voltage limitation	$I_T = 5\text{ mA}$ or whichever is lower	$V_1$	26	27.5	30.0	V	
			$V_{S+14}$	$V_{S+15}$	$V_{S+16}$		
Edge steepness	$dv_{\theta}/dt = \alpha_4 dv_{\theta}/dt$ $dV_{\theta}/dt_{max}$	$\alpha_4$	53	63	72	V/ms	
					130		

**Application**



**N SUFFIX PLASTIC DIP  
(MS - 001BA)**



$\oplus 0.25 (0.010) \text{ (M) T}$

Symbol	Dimension, mm	
	MIN	MAX
A	8.51	10.16
B	6.1	7.11
C		5.33
D	0.36	0.56
F	1.14	1.78
G	2.54	
H	7.62	
J	0°	10°
K	2.92	3.81
L	7.62	8.26
M	0.2	0.36
N	0.38	

**NOTES:**

- Dimensions "A", "B" do not include mold flash or protrusions.  
Maximum mold flash or protrusions 0.25 mm (0.010) per side.