



**1M x 32 SRAM MODULE**

**SYS321000ZK/LK - 012/015/020/025**

Issue 1.5 : December 1998

**Description**

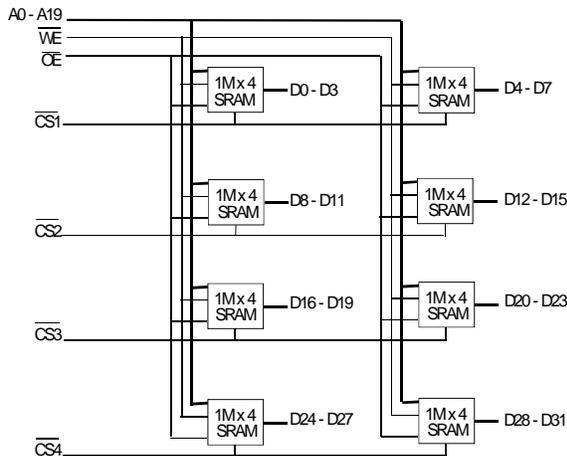
The SYS321000ZK/LK is a industry standard plastic 32Mbit Static RAM Module housed in a 72 pin plastic SIMM & ZIP package organised as 1M x 32. The module utilises fast SRAMs housed in SOJ packages, and uses double sided surface mount techniques to achieve a very high density module.

The module has four Chip Selects, which allow reading and writing to individual bytes or words. The pins PD0-3, are used to identify module memory density in applications where alternative modules can be interchanged.

**Features**

- Access Times of 12/15/20/25 ns.
- 72 Pin ZIP, SIMM package
- 5 Volt Supply  $\pm 10\%$ .
- Low Power Dissipation:  
Average (min cycle) 7.48 W (Max).  
Standby -L Version (CMOS) 22 mW (Max).
- Completely Static Operation.
- On-board Supply Decoupling Capacitors.
- Equivalent to EDI part EDI8F321024C, IDT part IDT7MP4120, and Cypress part CYM1851.

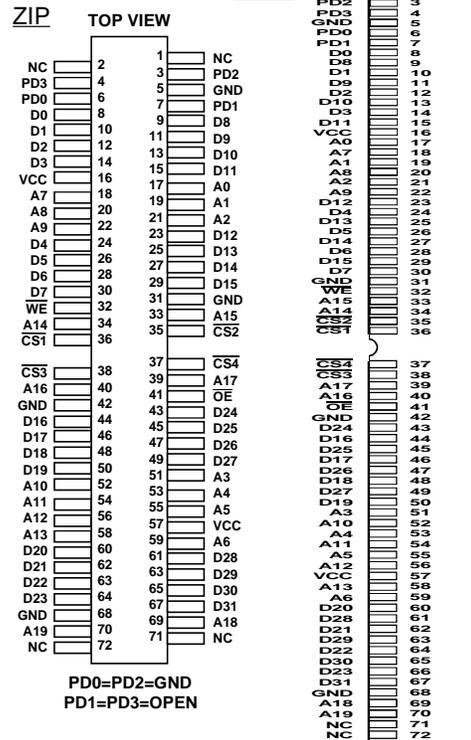
**Block Diagram**



**Pin Functions**

Address Inputs	<b>A0 - A19</b>
Data Input/Output	<b>D0 - D31</b>
Chip Select	<b>CS1-4</b>
Presence Detect	<b>PD0-3</b>
Write Enable	<b>WE</b>
Output Enable	<b>OE</b>
No Connect	<b>NC</b>
Power (+5V)	<b>V<sub>cc</sub></b>
Ground	<b>GND</b>

**Pin Definition**



**Package Details**

Plastic 72 Pin SIMM  
Plastic 72 Pin ZIP

**DC OPERATING CONDITIONS**

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**Absolute Maximum Ratings** <sup>(1)</sup>

Parameter	Symbol	Min	Typ	Max	Unit
Voltage on any pin relative to $V_{SS}$	$V_T^{(2)}$	-0.3	-	7.0	V
Power Dissipation	$P_T$	-	-	8.0	W
Storage Temperature	$T_{STG}$	-55	-	125	°C

Notes : (1) Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

(2)  $V_T$  can be -2.0V pulse of less than 10ns.

**Recommended Operating Conditions**

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	$V_{CC}$	4.5	5.0	5.5	V
Input High Voltage	$V_{IH}$	2.2	-	$V_{CC}+0.3$	V
Input Low Voltage	$V_{IL}$	-0.3	-	0.8	V
Operating Temperature	(Commercial) $T_A$	0	-	70	°C
	(Industrial) $T_{AI}$	-40	-	85	°C

**DC Electrical Characteristics** ( $V_{CC}=5V\pm 10\%$ )  $T_A$  0 to 70 °C

Parameter	Symbol	Test Condition	Min	Typ	max	Unit
I/P Leakage Current Address, $\overline{OE}$ , $\overline{WE}$	$I_{LI}$	$0V \leq V_{IN} \leq V_{CC}$	-16	-	16	$\mu A$
Output Leakage Current Worst Case	$I_{LO}$	$\overline{CS} = V_{IH}, V_{IO} = GND \text{ to } V_{CC}$	-16	-	16	$\mu A$
Average Supply Current	$I_{CC1}$	Min. Cycle, $\overline{CS} = V_{IL}, V_{IL} \leq V_{IN} \leq V_{IH}$	-	-	1360	mA
Standby Supply Current	TTL $I_{SB1}$	$\overline{CS} = V_{IH}$	-	-	480	mA
	CMOS $I_{SB2}$	$\overline{CS} \geq V_{CC}-0.2V, 0.2 \leq V_{IN} \leq V_{CC}-0.2V$	-	-	80	mA
Output Voltage	$V_{OL}$	$I_{OL} = 8.0mA$	-	-	0.4	V
	$V_{OH}$	$I_{OH} = -4.0mA$	2.4	-	-	V

Typical values are at  $V_{CC}=5.0V, T_A=25^\circ C$  and specified loading.  $\overline{CS}$  above refers to  $\overline{CS1-4}$ .

**Capacitance** ( $V_{CC}=5V\pm 10\%, T_A=25^\circ C$ )

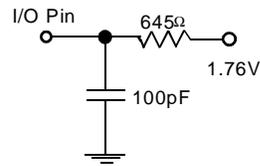
Note: Capacitance calculated, not measured.

Parameter	Symbol	Test Condition	max	Unit
Input Capacitance (Address, $\overline{OE}$ , $\overline{WE}$ )	$C_{IN1}$	$V_{IN} = 0V$	64	pF
I/P Capacitance (other)	$C_{IN2}$	$V_{IN} = 0V$	10	pF
I/O Capacitance	$C_{IO}$	$V_{IO} = 0V$	80	pF

**AC Test Conditions****Output Load**

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- \* Input pulse levels: 0V to 3.0V
- \* Input rise and fall times: 3ns
- \* Input and Output timing reference levels: 1.5V
- \* Output load: see diagram
- \*  $V_{CC} = 5V \pm 10\%$

**Operation Truth Table**

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	DATA PINS	SUPPLY CURRENT	MODE
H	X	X	High Impedance	$I_{SB1}, I_{SB2}, I_{SB3}$	Standby
L	L	H	Data Out	$I_{CC1}$	Read
L	H	L	Data In	$I_{CC1}$	Write
L	L	L	Data In	$I_{CC1}$	Write
L	H	H	High-Impedance	$I_{SB1}, I_{SB2}, I_{SB3}$	High-Z

Notes : H =  $V_{IH}$  : L =  $V_{IL}$  : X =  $V_{IH}$  or  $V_{IL}$

**AC OPERATING CONDITIONS****Read Cycle**

Parameter	Symbol	-12		-15		-20		-25		Unit
		min	max	min	max	min	max	min	max	
Read Cycle Time	$t_{RC}$	12	-	15	-	20	-	25	-	ns
Address Access Time	$t_{AA}$	-	12	-	15	-	20	-	25	ns
Chip Select Access Time	$t_{ACS}$	-	12	-	15	-	20	-	25	ns
Output Enable to Output Valid	$t_{OE}$	-	6	-	7	-	10	-	12	ns
Output Hold from Address Change	$t_{OH}$	3	-	3	-	4	-	5	-	ns
Chip Selection to Output in Low Z	$t_{CLZ}$	3	-	3	-	3	-	3	-	ns
Output Enable to Output in Low Z	$t_{OLZ}$	0	-	0	-	0	-	0	-	ns
Chip Deselection to O/P in High Z	$t_{CHZ}$	0	7	0	7	0	8	0	10	ns
Output Disable to Output in High Z	$t_{OHZ}$	0	7	0	7	0	8	0	10	ns

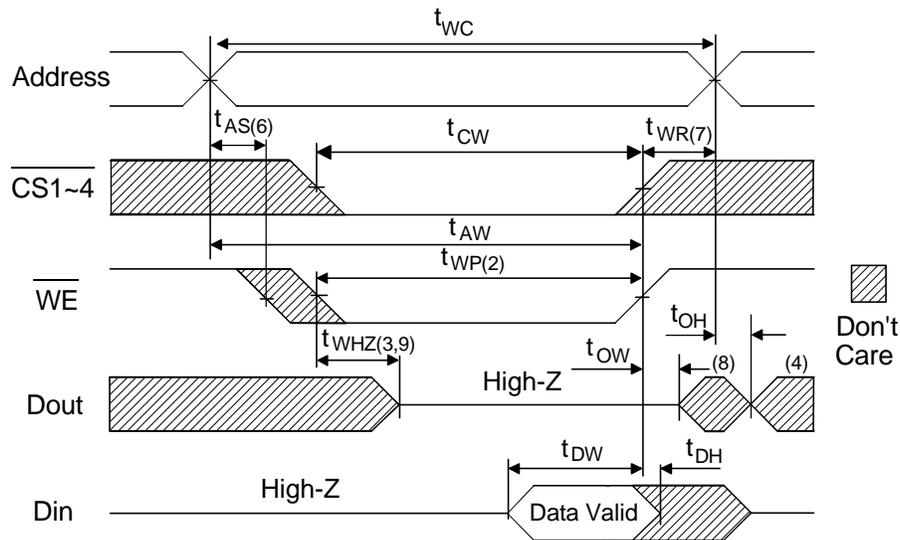
**Write Cycle**

Parameter	Symbol	-12		-15		-20		-25		Unit
		min	max	min	max	min	max	min	max	
Write Cycle Time	$t_{WC}$	12	-	15	-	20	-	25	-	ns
Chip Selection to End of Write	$t_{CW}$	8	-	12	-	15	-	15	-	ns
Address Valid to End of Write	$t_{AW}$	8	-	12	-	15	-	15	-	ns
Address Setup Time	$t_{AS}$	0	-	0	-	0	-	0	-	ns
Write Pulse Width	$t_{WP}$	15	-	15	-	15	-	15	-	ns
Write Recovery Time	$t_{WR}$	0	-	0	-	0	-	0	-	ns
Write to Output in High Z	$t_{WHZ}$	0	6	0	7	0	8	0	10	ns
Data to Write Time Overlap	$t_{DW}$	6	-	8	-	10	-	12	-	ns
Data Hold from Write Time	$t_{DH}$	0	-	0	-	0	-	0	-	ns
Output active from End of Write	$t_{OW}$	0	-	0	-	0	-	0	-	ns



**Write Cycle No.2 Timing Waveform (1,5)**

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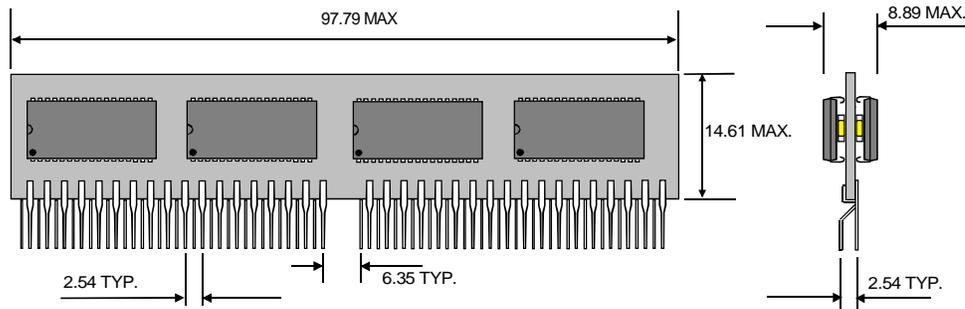
**AC Write Characteristics Notes**

- (1) All write cycle timing is referenced from the last valid address to the first transition address.
- (2) All writes occur during the overlap of CS1~4 and WE low.
- (3) If  $\overline{OE}$ ,  $\overline{CS1\sim4}$ , and  $\overline{WE}$  are in the Read mode during this period, the I/O pins are low impedance state. Inputs of opposite phase to the output must not be applied because bus contention can occur.
- (4) Dout is the Read data of the new address.
- (5)  $\overline{OE}$  is continuously low.
- (6) Address is valid prior to or coincident with  $\overline{CS1\sim4}$  and  $\overline{WE}$  low, too avoid inadvertant writes.
- (7)  $\overline{CS1\sim4}$  or  $\overline{WE}$  must be high during address transitions.
- (8) When  $\overline{CS1\sim4}$  are low : I/O pins are in the output state. Input signals of opposite phase leading to the output should not be applied.
- (9) Defined as the time at which the outputs achieve open circuit conditions and are not referenced to output voltage levels. These parameters are sampled and not 100% tested.

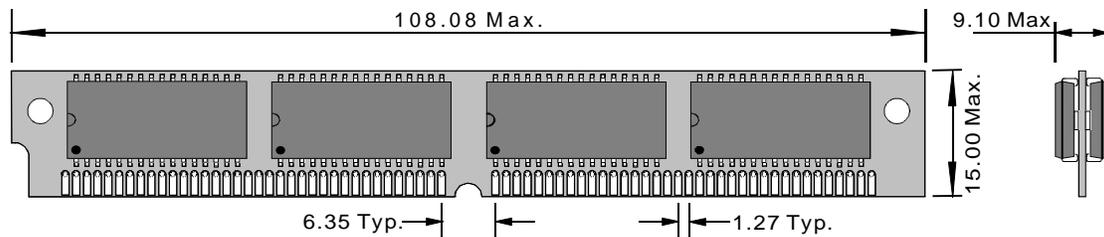
**Package Information**      Dimensions in mm(inches)

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**Plastic 72 Pin ZIP**

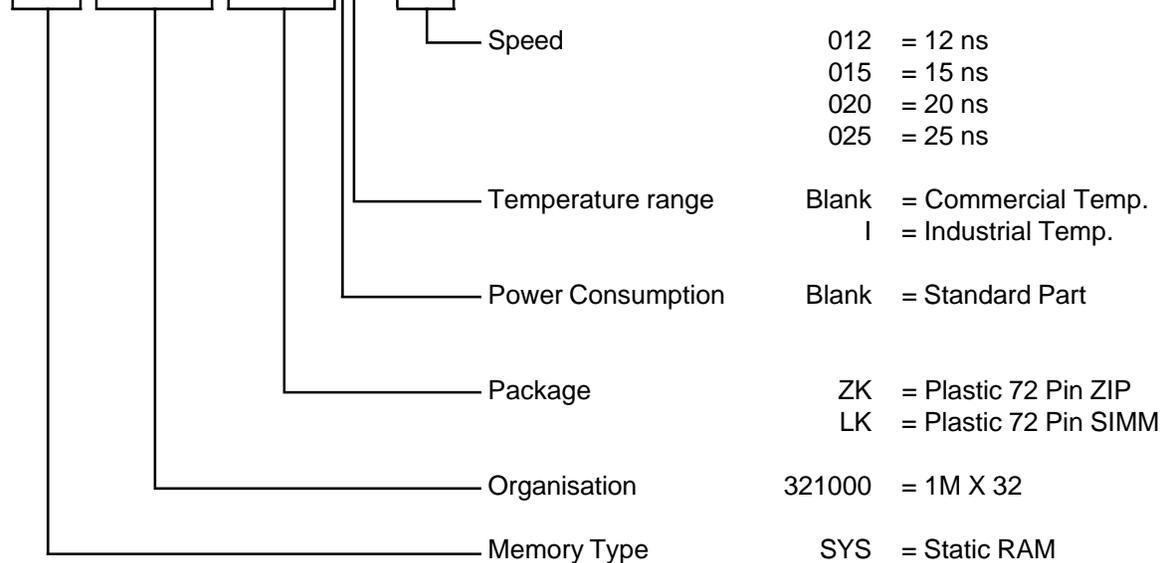


**Plastic 72 Pin SIMM**



**Ordering Information**

**SYS 321000 ZK/LK I - 015**



**Note :**

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