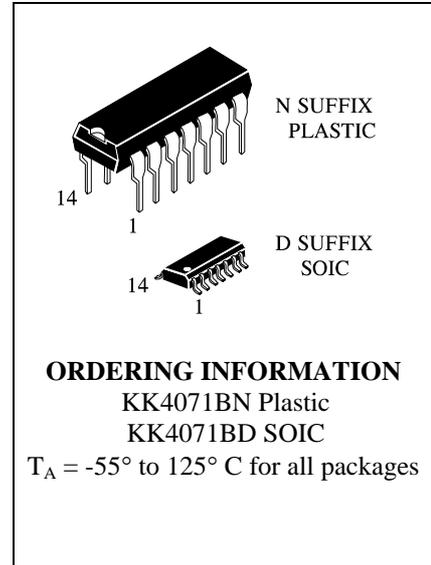**KK4071B**

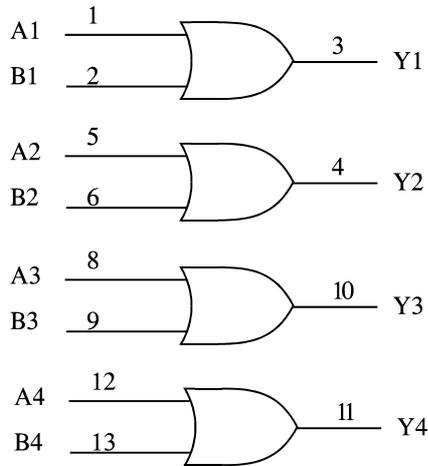# Quad 2-Input OR Gate
High-Voltage Silicon-Gate CMOS

The KK4071B OR gates provide the system designer wich direct emplementation of the positive-logic OR function.

- Operating Voltage Range: 3.0 to 18 V
- Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (over full package temperature range):
  - 1.0 V min @ 5.0 V supply
  - 2.0 V min @ 10.0 V supply
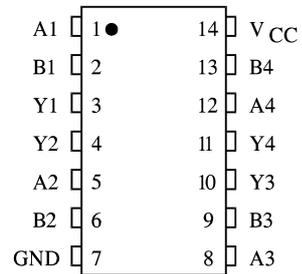 - 2.5 V min @ 15.0 V supply

N SUFFIX
PLASTIC

14

1

D SUFFIX
SOIC

14

1

ORDERING INFORMATION
KK4071BN Plastic
KK4071BD SOIC
T_A = -55° to 125° C for all packages

LOGIC DIAGRAM

A1 1
B1 2
3 Y1

A2 5
B2 6
4 Y2

A3 8
B3 9
10 Y3

A4 12
B4 13
11 Y4

PIN 14 = V_{CC}
PIN 7 = GND

PIN ASSIGNMENT

A1	1●	14	V_{CC}
B1	2	13	B4
Y1	3	12	A4
Y2	4	11	Y4
A2	5	10	Y3
B2	6	9	B3
GND	7	8	A3

FUNCTION TABLE

Inputs		Output
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	H

MAXIMUM RATINGS[*]

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +20	V
V_{IN}	DC Input Voltage (Referenced to GND)	-0.5 to V_{CC} +0.5	V
V_{OUT}	DC Output Voltage (Referenced to GND)	-0.5 to V_{CC} +0.5	V
I_{IN}	DC Input Current, per Pin	±10	mA
P_D	Power Dissipation in Still Air, Plastic DIP+ SOIC Package+	750 500	mW
P_D	Power Dissipation per Output Transistor	100	mW
Tstg	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package)	260	°C

[*]Maximum Ratings are those values beyond which damage to the device may occur.
Functional operation should be restricted to the Recommended Operating Conditions.
+Derating - Plastic DIP: - 10 mW/°C from 65° to 125°C
          SOIC Package: : - 7 mW/°C from 65° to 125°C

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	DC Supply Voltage (Referenced to GND)	3.0	18	V
V_{IN}, V_{OUT}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V_{CC}	V
T_A	Operating Temperature, All Package Types	-55	+125	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND≤(V_{IN} or V_{OUT})≤V_{CC}.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V_{CC} V	Guaranteed Limit			Unit
				$\geq$-55°C	25°C	$\leq$125 °C	
V_{IH}	Minimum High-Level Input Voltage	$V_{OUT}=V_{CC}$ - 0.5V $V_{OUT}=V_{CC}$ - 1.0V $V_{OUT}=V_{CC}$ - 1.5V	5.0 10 15	3.5 7 11	3.5 7 11	3.5 7 11	V
V_{IL}	Maximum Low - Level Input Voltage	$V_{OUT}=0.5$ V or V_{CC} - 0.5 V $V_{OUT}=1$ V or V_{CC} - 1 V $V_{OUT}=1.5$ V or V_{CC} - 1.5 V	5.0 10 15	1.5 3 4	1.5 3 4	1.5 3 4	V
V_{OH}	Minimum High-Level Output Voltage	V_{IN}=GND or V_{CC}	5.0 10 15	4.95 9.95 14.95	4.95 9.95 14.95	4.95 9.95 14.95	V
V_{OL}	Maximum Low-Level Output Voltage	V_{IN}=GND	5.0 10 15	0.05 0.05 0.05	0.05 0.05 0.05	0.05 0.05 0.05	V
I_{IN}	Maximum Input Leakage Current	V_{IN}= GND or V_{CC}	18	±0.1	±0.1	±1.0	µA
I_{CC}	Maximum Quiescent Supply Current (per Package)	V_{IN}= GND or V_{CC}	5.0 10 15 20	0.25 0.5 1.0 5.0	0.25 0.5 1.0 5.0	7.5 15 30 150	µA
I_{OL}	Minimum Output Low (Sink) Current	V_{IN}= GND or V_{CC} U_{OL}=0.4 V U_{OL}=0.5 V U_{OL}=1.5 V	5.0 10 15	0.64 1.6 4.2	0.51 1.3 3.4	0.36 0.9 2.4	mA
I_{OH}	Minimum Output High (Source) Current	V_{IN}= GND or V_{CC} U_{OH}=2.5 V U_{OH}=4.6 V U_{OH}=9.5 V U_{OH}=13.5 V	5.0 5.0 10 15	-2.0 -0.64 -1.6 -4.2	-1.6 -0.51 -1.3 -3.4	-1.15 -0.36 -0.9 -2.4	mA

AC ELECTRICAL CHARACTERISTICS (C$_L$=50pF, R$_L$=200kΩ, Input t$_r$=t$_f$=20 ns)

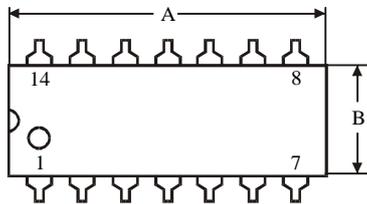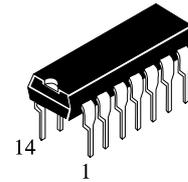| Symbol	Parameter	V$_{CC}$ V	Guaranteed Limit			Unit
			≥-55°C	25°C	≤125°C	
t$_{PLH}$, t$_{PHL}$	Maximum Propagation Delay, Input A or B to Output Y (Figure 1)	5.0 10 15	250 120 90	250 120 90	500 240 180	ns
t$_{TLH}$, t$_{THL}$	Maximum Output Transition Time, Any Output (Figure 1)	5.0 10 15	200 100 80	200 100 80	400 200 160	ns
C$_{IN}$	Maximum Input Capacitance	-		7.5		pF
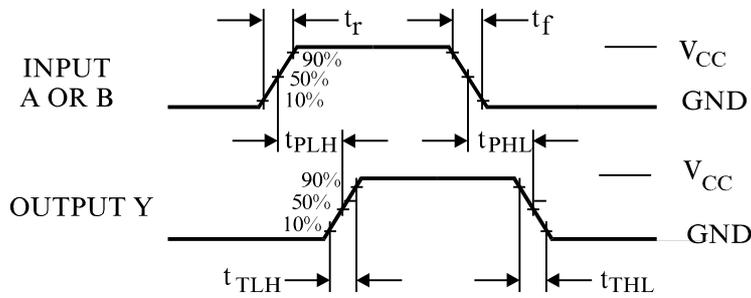
Figure 1. Switching Waveforms

EXPANDED LOGIC DIAGRAM
(1/4 of the Device)
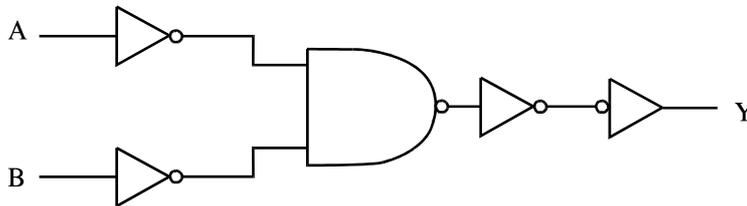
N SUFFIX PLASTIC DIP
(MS - 001AA)

	Dimension, mm	
Symbol	**MIN**	**MAX**
A	18.67	19.69
B	6.1	7.11
C		5.33
D	0.36	0.56
F	1.14	1.78
G	2.54	
H	7.62	
J	0°	10°
K	2.92	3.81
L	7.62	8.26
M	0.2	0.36
N	0.38	
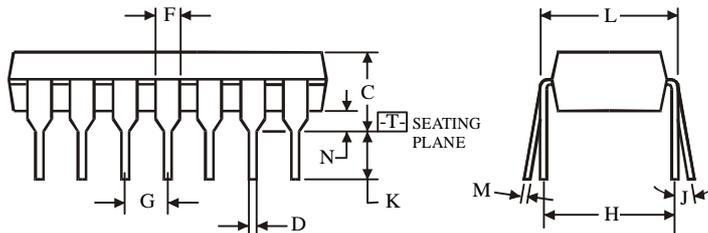
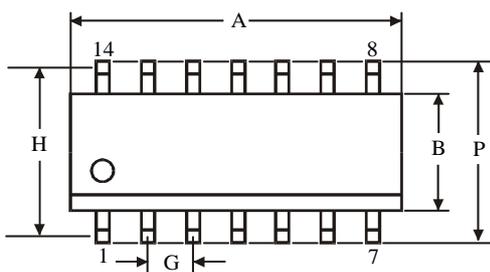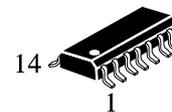⊕ 0.25 (0.010) Ⓜ | T

NOTES:

1. Dimensions "A", "B" do not include mold flash or protrusions.

   Maximum mold flash or protrusions 0.25 mm (0.010) per side.

D SUFFIX SOIC
(MS - 012AB)

	Dimension, mm	
Symbol	**MIN**	**MAX**
A	8.55	8.75
B	3.8	4
C	1.35	1.75
D	0.33	0.51
F	0.4	1.27
G	1.27	
H	5.27	
J	0°	8°
K	0.1	0.25
M	0.19	0.25
P	5.8	6.2
R	0.25	0.5
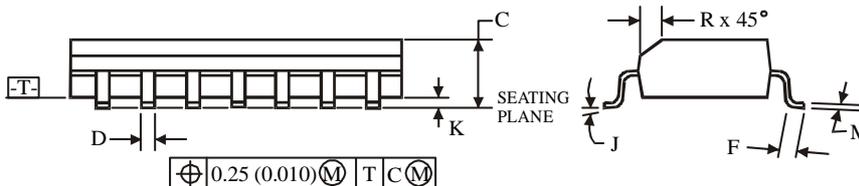
⊕ 0.25 (0.010) Ⓜ | T | C Ⓜ

NOTES:

1. Dimensions A and B do not include mold flash or protrusion.

2. Maximum mold flash or protrusion 0.15 mm (0.006) per side
   for A; for B – 0.25 mm (0.010) per side.