## 1. Generel Description

The CSC1004 is a timing controller IC to control AV type TFT LCD modules,which built in horizontal frequency driver and phase comparator circuit for PLLcircuit.
Also this IC can support external clock mode that it doesn't need PLL circuit.
This IC generates all kind of control timing signals to the LCD source drivers and gate drivers.
This IC provides 16:9 aspect ratio TFT LCD modules and it also provides different display mode.

## 2. Features

-Support multiple resolution mode
-Support Standard NTSC/PAL video system
-Line Inversion Driving method
-Provide timing scan for Left/Right and Up/Down shift control
-Support 3 shift clock
-Provide multi display mode (960*234,1200*234,1440*234 mode, 1920*234 mode)
-Support composite sync input mode and separate sync input mode
-Support external clock input mode (960*234,1200*234,1440*234,1920*234 mode)
-64 pin QFP (0.5mm pitch)
-Dual power supplies: +5.0v/+3.3v
-0.35u CMOS process,3.3V for core and 3.3V/5V for IO PAD

## 3. Pin assignment

| pin No. | pin | I/O | Remark | pin No. | pin | I/O | Remark |
|---|---|---|---|---|---|---|---|
| 1 | ivsync | I | schimtt | 33 | ires1 | I | pull_down |
| 2 | iviy | I | schimtt | 34 | iz_sel | I | Pull_down |
| 3 | ifrst | I | schimtt | 35 | itst1 | I | AC/DC test |
| 4 | icsy | I | schimtt | 36 | ooe3 | O | 3mA |
| 5 | icomps | I | pull_up | 37 | ooe2 | O | 3mA |
| 6 | iclkc | I | pull_up | 38 | ooe1 | O | 3mA |
| 7 | iomclk | I/O | Bi dir.(3mA) | 39 | VSS | | |
| 8 | opsi | O | 3mA | 40 | ostv2 | O | 3_state(1mA) |
| 9 | opsc | O | 3mA | 41 | ostv1 | O | 3_state(1mA) |
| 10 | opols | O | 3mA | 42 | ocpv | O | 3mA |
| 11 | opolc | O | 3mA | 43 | HVDD | | 5.0V/3.3V |
| 12 | oblk | O | 3mA | 44 | iosci | I | xin (25Mhz) |
| 13 | onpo | O | 3mA | 45 | oosco | O | xout(25Mhz) |
| 14 | iohsy | I/O | Bi dir.(3mA) | 46 | VSS | | |
| 15 | iovsy | I/O | Bi dir(3mA). | 47 | opda | O | 3_state(3mA) |
| 16 | HVDD | | 5.0V/3.3V | 48 | osrst | O | 1mA |
| 17 | imode1 | I | pull_down | 49 | ocph1 | O | 6mA |
| 18 | imode2 | I | pull_down | 50 | ocph2 | O | 6mA |
| 19 | imode3 | I | pull_down | 51 | ocph3 | O | 6mA |
| 20 | ivpos1 | I | pull_up | 52 | osth1 | O | 3_state(3mA) |
| 21 | ivpos2 | I | pull_up | 53 | osth2 | O | 3_state(3mA) |
| 22 | VSS | | | 54 | oq2h | O | 3mA |
| 23 | ihpos1 | I | pull_up | 55 | LVDD | | 3.3V |
| 24 | ihpos2 | I | pull_up | 56 | ooeh | O | 3mA |
| 25 | iarea_sel | I | pull_up | 57 | ocpo | O | 3mA |
| 26 | iimode | I | pull_up | 58 | VSS | | |
| 27 | icpo_sel | I | pull_up | 59 | icpi | I | |
| 28 | icph_sel | I | pull_up | 60 | iq2h_sel | I | pull_up |
| 29 | iodd_sel | I | pull_up | 61 | ioeh_sel | I | pull_up |
| 30 | LVDD | | 3.3V | 62 | ilnr | I | pull_up |
| 31 | ires3 | I | pull_down | 63 | iund | I | pull_up |
| 32 | ires2 | I | pull_down | 64 | innp | I | pull_up |

## 4. Pin Description

| No. | Symbol | I/O | Description | Remark |
|---|---|---|---|---|
| 1 | ivsync | I | vertical sync signal in composite sync mode (low active) | |
| 2 | iviy | I | vertical sync signal in separate sync mode(low active) | |
| 3 | ifrst | I | reset pin in ASIC<br>1) ifrst = "H" : Normal state<br>2) ifrst = "L" : Reset state | |
| 4 | icsy | I | select composite signal/horizontal signal<br>1) icomps = "H" : icsy is composite sync signal (high active)<br>2) icomps = "L" : icsy is horizontal sync signal(low active) | |
| 5 | icomps | I | select composite sync mode/separate sync mode<br>1) icomps = "H" : composite sync mode<br>2) icomps = "L" : separate sync mode | Note1) |
| 6 | iclkc | I | select PLL mode/external clock mode<br>1) iclkc = "H" : PLL mode<br>2) iclkc = "L" : external clock mode | Note1) |
| 7 | iomclk | I/O | input clock signal (external clock mode)<br>1) iclkc = "H" : This signal will be ground<br>2) iclkc = "L" : This signal will be external input ternimal | |
| 8 | opsl | O | control decorder chip pin | |
| 9 | opsc | O | control DC-DC chip pin | |
| 10 | opols | O | polarity alternating signal for video | |
| 11 | opolc | O | polarity alternating signal for Vcom | |
| 12 | oblk | O | blanking control pin<br>1) oblk ="H" : blanking display (black)<br>2) oblk ="L" : normal display | |
| 13 | onpo | O | auto detect pin for NTSC/PAL<br>1) onpo ="H" : NTSC<br>2) onpo ='L" : PAL | Note2) |
| 14 | iohsy | I/O | input/output horizontal sync. signal (low active)<br>1) iclkc = "H" : This signal outputs horizontal sync. signal<br>2) iclkc = "L" : This signal will be external horizontal sync. Input. | |
| 15 | iovsy | I/O | input/output vertical sync. signal (low active)<br>1) iclkc = "H" : This signal outputs vertical sync. signal<br>2) iclkc = "L" : This signal will be external vertical sync. Input. | |
| 16 | HVDD | - | high voltage power (5.0 V or 3.3V) | Note3) |
| 17<br>18<br>19 | imode1<br>imode2<br>imode3 | I<br>I<br>I | select display mode (1920,1440, 1200, 960 mode only) | Note4) |

| imode1 | imode2 | imode3 | Description |
|---|---|---|---|
| L | L | L | Full mode |
| H | L | L | Normal center mode |
| L | H | L | Normal wide mode |
| H | H | L | Zoom1 mode |
| L | L | H | Zoom2 mode |
| H | L | H | Normal left mode |
| L | H | H | Normal right mode |
| H | H | H | Zoom3 mode |

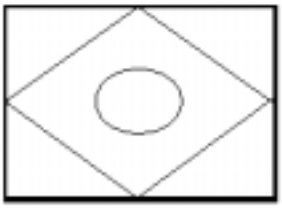
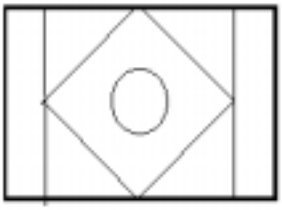
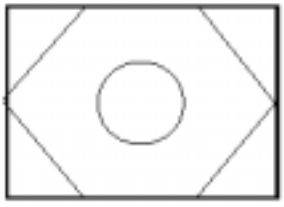
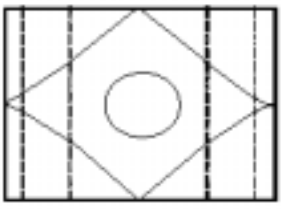
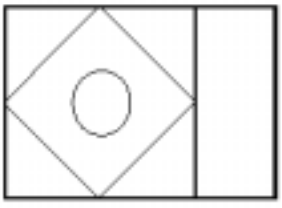
<table>
<tr><th>No.</th><th>Symbol</th><th>I/O</th><th>Description</th><th>Remark</th></tr>
<tr><td>20<br>21</td><td>ivpos1<br>ivpos2</td><td>I<br>I</td><td>select vertical start line
<table>
<tr><th>ivpos2</th><th>ivpos1</th><th>NTSC</th><th>PAL</th></tr>
<tr><td>L</td><td>L</td><td>20</td><td>26</td></tr>
<tr><td>L</td><td>H</td><td>21</td><td>28</td></tr>
<tr><td>H</td><td>L</td><td>22</td><td>30</td></tr>
<tr><td>H</td><td>H</td><td>23</td><td>31</td></tr>
</table></td><td>Note1)</td></tr>
<tr><td>22</td><td>VSS</td><td>-</td><td>Ground</td><td></td></tr>
<tr><td>23<br>24</td><td>ihpos1<br>ihpos2</td><td>I<br>I</td><td>select horizontal start point (iclkc ="L" only, ext clock mode)
<table>
<tr><th>ivpos2</th><th>ivpos1</th><th>1440</th><th>1200</th><th>960</th><th>1920</th></tr>
<tr><td>L</td><td>L</td><td>100</td><td>85</td><td>67</td><td>134</td></tr>
<tr><td>L</td><td>H</td><td>101</td><td>86</td><td>68</td><td>135</td></tr>
<tr><td>H</td><td>L</td><td>102</td><td>87</td><td>69</td><td>136</td></tr>
<tr><td>H</td><td>H</td><td>103</td><td>88</td><td>70</td><td>137</td></tr>
</table></td><td>Note1)<br>Note5)</td></tr>
<tr><td>25</td><td>iarea_sel</td><td>I</td><td>select display range<br>1) iarea_sel = "H" : The display range is 50.01us (NTSC)<br>2) iarea_sel = "L" : The display range is 48.00us (NTSC)</td><td>Note1)</td></tr>
<tr><td>26</td><td>iimode</td><td>I</td><td>select simultaneous mode/sequential mode<br>1) iimode ="H" : simultaneous mode (stripe arrangement)<br>2) iimode ="L" : sequential mode (delta arrangement)</td><td>Note1)</td></tr>
<tr><td>27</td><td>icpo_sel</td><td>I</td><td>select horizontal position adjust (iclkc = "H" only)<br>1) icpo_sel = "H" : hor. Position adjustment is normal<br>2) icpo_sel = "L" : hor.position adjustment is more wide</td><td>Note1)</td></tr>
<tr><td>28</td><td>icph_sel</td><td>I</td><td>select ocph1,2,3 phase (delta arrangement module only)<br>1) icph_sel = "H" : PVI's arrangement<br>2) icph_sel = "L" : another company's arrangement</td><td>Note1)<br>Note6)</td></tr>
<tr><td>29</td><td>iodd_sel</td><td>I</td><td>select falling edge of iovsy's position (NTSC, composite sync only<br>1) iodd_sel = "H" : iovsy's phase difference is 1.5H (even field)<br>2) iodd_sel = "L" : iovsy's phase difference is 0.5H (even field)</td><td>Note1)</td></tr>
<tr><td>30</td><td>LVDD</td><td>-</td><td>low voltage power (3.3V only)</td><td></td></tr>
<tr><td>31<br>32<br>33</td><td>ires3<br>ires2<br>ires1</td><td>I<br>I<br>I</td><td>select resolution mode
<table>
<tr><th>ires1</th><th>ires2</th><th>ires3</th><th>resolution mode</th></tr>
<tr><td>L</td><td>L</td><td>L</td><td>1200 * 234</td></tr>
<tr><td>H</td><td>L</td><td>L</td><td>-</td></tr>
<tr><td>L</td><td>H</td><td>L</td><td>1920 * 234</td></tr>
<tr><td>H</td><td>H</td><td>L</td><td>240 * 234</td></tr>
<tr><td>L</td><td>L</td><td>H</td><td>480 * 234</td></tr>
<tr><td>H</td><td>L</td><td>H</td><td>960 * 234 (S)</td></tr>
<tr><td>L</td><td>H</td><td>H</td><td>960 * 234 (D)</td></tr>
<tr><td>H</td><td>H</td><td>H</td><td>1440 * 234</td></tr>
</table></td><td>Note4)</td></tr>
<tr><td>34</td><td>iz_sel</td><td>I</td><td>select falling edge of iovsy's position (PAL mode only)<br>1) iz_sel = "H" : iovsy's phase difference is 0.5H (even field)<br>2) iz_sel = "L" : iovsy's phase difference is 1.5H (even field)</td><td>Note4)</td></tr>
</table>

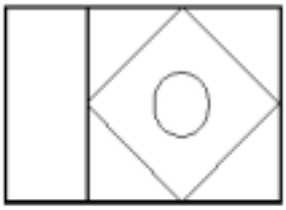
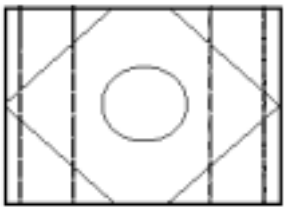
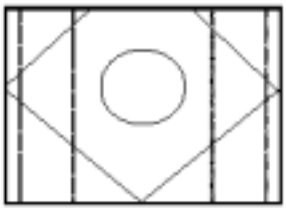
| No. | Symbol | I/O | Description | Remark |
|---|---|---|---|---|
| 35 | itst1 | I | select AC/DC test<br>1) itst1 = "H" : AC/DC test mode<br>2) itst1 = "L" : normal mode | |
| 36<br>37<br>38 | ooe3<br>ooe2<br>ooe1 | O<br>O<br>O | output enable control signal for gate driver<br>ooe1,2,3 ="H" : gate output => Vee<br>1) ooe1 controls 1 4 7 10 --- 238 lines<br>2) ooe2 controls 2 5 8 11 --- 239 lines<br>3) ooe3 controls 3 6 9 12 --- 240 lines | note7) |
| 39 | VSS | - | Ground | |
| 40 | ostv2 | O | gate driver start pulse<br>1) iund = "H" : ostv2 is in high impedance state<br>2) iund = "L" : ostv2 is output pin of start pulse | note7) |
| 41 | ostv1 | O | gate driver start pulse<br>1) iund = "H" : ostv1 is output pin of start pulse<br>2) iund = "L" : ostv1 is in high impedance state | note7) |
| 42 | ocpv | O | gate driver shift clock | |
| 43 | HVDD | - | high voltage power (5.0 V or 3.3V) | Note3) |
| 44 | iosci | I | input for clock oscillator circuit | |
| 45 | oosco | O | output for clock oscillator circuit | |
| 46 | VSS | - | Ground | |
| 47 | opda | O | output for phase comparative signal for PLL circuit | |
| 48 | osrst | O | reset source driver IC (active high) | |
| 49 | ocph1 | O | source driver shift clock #1 | |
| 50 | ocph2 | O | source driver shift clock #2<br>1) iimode = "H" : ochp2 is always high signal (stripe arrangement)<br>2) iimode = "L" : ocph2 is shift clock (delta arrangement) | |
| 51 | ocph3 | O | source driver shift clock #3<br>1) iimode = "H" : ochp3 is always low signal (stripe arrangement)<br>2) iimode = "L" : ocph3 is shift clock (delta arrangement) | |
| 52 | osth1 | O | source driver start pulse<br>1) ilnr = "H" : osth1 is output pin of start pulse<br>2) ilnr = "L" : osth1 is in high impedance state | Note8) |
| 53 | osth2 | O | source driver start pulse<br>1) ilnr = "H" : osth2 is in high impedance state<br>2) ilnr = "L" : osth2 is output pin of start pulse | Note8) |
| 54 | oq2h | O | pin of RGB output data order on no rotation mode<br>1) iimode ="H" : no use (low)<br>2) iimode ="L" : use (delta arrangement) | |
| 55 | LVDD | - | low voltage power (3.3V only) | |
| 56 | ooeh | O | output enable control signal for source driver<br>1) ioeh_sel = "H" : ooeh is active low<br>2) ioeh_sel = "L" : ooeh is active high | |
| 57 | ocpo | O | output for horizontal position adjustment | |
| 58 | VSS | - | Ground | |
| 59 | icpi | I | input for horizontal position adjustment | |

| No. | Symbol | I/O | Description | Remark |
|---|---|---|---|---|
| 60 | iq2h_sel | I | select oe's control in zoom mode<br>1) iq2h_sel = "H" : 3 oe (oe1,oe2,oe3) control<br>2) iq2h_sel = "L" : 1 oe control | Note1)<br>note6) |
| 61 | ioeh_sel | I | select perioty of ooeh<br>1) ioeh_sel = "H" : ooeh is active low<br>2) ioeh_sel = "L" : ooeh is active high | Note1) |
| 62 | ilnr | I | select left/right direction<br>1) ilnr = "H" : normal scan<br>2) ilnr = "L" : reverse scan | Note1)<br>Note8) |
| 63 | iund | I | select up/down direction<br>1) iund = "H" : normal scan<br>2) iund = "L" : reverse scan | Note1)<br>Note7) |
| 64 | innp | I | select NTSC/PAL<br>1) ilnr = "H" : normal scan<br>2) ilnr = "L" : reverse scan | Note1) |

Note1) Those pins are Normally pull-up
Note2) If use auto detection, this pin must connect innp
Note3) If you want to use 5V's I/O signal, It must connect 5V's Voltage,
otherwise, if you want to use 3.3V's I/O signal, it must connect 3.3V's voltage
Note4) Those pins are Normally pull-down
Note5) This count means No.of input clock from the falling edge of iohsy
Note6) If you use another company's TFT LCD module, please contact PVI.
Note7) iund controls up/down direction
1) iund = "H" : ostv1 → G1(ooe1) → G2(ooe2) → G3(ooe3) → G4(ooe1) → G5(ooe1) → — → G238(ooe1) → G239(ooe2) → G240(ooe3) → ostv2
2) iund = "L" : ostv1 ← G1(ooe1) ← G2(ooe2) ← G3(ooe3) ← G4(ooe1) ← G5(ooe1) ← — ← G238(ooe1) ← G239(ooe2) ← G240(ooe3) ← ostv2
Note8) ilnr controls left/right direction
1) ilnr = "H" : osth1 → ----- → osth2
2) ilnr = "L" : osth1 ← ----- ← osth2

## 5. Display mode (1200, 1440, 1920, 960 mode only)

| Display mode | Display characteristics (4:3 aspect-ratio input) | imd 1 | imd 2 | imd 3 | Note |
|---|---|---|---|---|---|
| Full |  | Lo | Lo | Lo | Input video signals are displayed in full screen (To display 4:3 signal on 16:9 screen) |
| Normal Center |  | Hi | Lo | Lo | Input video signals are displayed in the center screen (4:3 aspect ratio) |
| Zoom 1 |  | Hi | Hi | Lo | Input video signal of central 176 lines are displayed in full screen (Vertically extention) |
| Wide |  | Lo | Hi | Lo | Input video signals are displayed in full screen (Horizontal modification) |
| Normal Left |  | Hi | Lo | Hi | Input video signals are displayed in the left screen (4:3 aspect ratio) |

| Display mode | Display characteristics (4:3 aspect ratio input) | ind 1 | ind 2 | ind 3 | Note |
|---|---|---|---|---|---|
| Normal Right |  | Lo | Hi | Hi | Input video signals are displayed in the right screen (4:3 aspect ratio) |
| Zoom 2 |  | Lo | Lo | Hi | Input video signal of central 204 lines are displayed in full screen (Vertically extention and horizon. Modified) |
| Zoom 3 |  | Hi | Hi | Hi | Same as Zoom 2 mode. Vertically offset centered |

## 6. Electrical Characteristics

### 6.1 Absolute Maximum Ratings

| Parameter | Symbol | Ratings | Units |
|---|---|---|---|
| Power supply voltage | HVDD | -0.3 to 7.0 | V |
| | LVDD | -0.3 to 4.0 | V |
| Input voltage | $V_{IN}$ | -0.3 to HVDD+0.5 | V |
| Output voltage | $V_{OUT}$ | -0.3 to HVDD+0.5 | V |
| Storage temperature | Tstg | -65 to 150 | ℃ |

### 6.2 Recommened Operating Conditions

| Parameter | Symbol | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| Power supply voltage | HVDD 1 | 4.5 | 5.0 | 5.5 | V |
| | HVDD 2 | 3.0 | 3.3 | 3.6 | V |
| | LVDD | 3.0 | 3.3 | 3.6 | 0 |
| Input voltage | $V_{IN}$ | VSS | 0 | HVDD | 0 |
| Operating temperature | Topr | -40 | - | 85 | ℃ |

### 6.3 General DC characteristics

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units | Remark |
|---|---|---|---|---|---|---|---|
| Input low current | $I_{IL}$ | $V_I$ = 0 V | -1 | - | 1 | uA | |
| Input high current | $I_{IH}$ | $V_I$ = HVDD | -1 | - | 1 | uA | |
| Tristate leakage current | $I_{OZ}$ | | -10 | - | 10 | uA | |
| Logic input low voltage | $V_{IL}$ | HVDD=MIN | - | - | 1.0 | V | |
| Schmitt input low voltage | $V_{ISL}$ | HVDD=MIN | 0.8 | - | 3.1 | V | |
| Logic input high voltage | $V_{IH}$ | HVDD=MAX | 3.5 | - | - | V | |
| Schmitt input high voltage | $V_{ISH}$ | HVDD=MAX | 2.0 | - | 4.0 | V | |
| Output low voltage | $V_{OL}$ | HVDD=MIN | HVDD-0.4 | - | - | V | |
| Output High voltage | $V_{OH}$ | HVDD=MIN | - | - | VDD+0.4 | V | |
| Input pullup/down resista | $R_I$ | $V_L$ = 0V or $V_H$ = HVDD | - | 60 | - | • | |

### 6.4 Current consumption

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Units | Remark |
|---|---|---|---|---|---|---|---|
| Current consumption | $I_{IH}$ | HVDD=3.3V | - | 8.5 | 15 | mA | |

## 7. Timing conditions

7-1) 1200 * 234 mode (6.5")

a. Input signal characteristics

| Paramet | Symbo | Min. | Typ. | Max. | Unit | Remar |
|---|---|---|---|---|---|---|
| iosci | $t_{OSC}$ | 81 | 83 | 85 | ns | |
| icsy | $T_H$ | 61. | 63. | 65. | us | |
| icsy pulse | $t_{CSYN}$ | 4 | 4.7 | 5.4 | us | |
| icsy rising | $T_{cr}$ | - | - | 700 | ns | |
| icsy falling | $T_{cf}$ | - | - | 300 | ns | |
| ivsync pulse | $t_{VSY}$ | 1 | 3 | 5 | $t_H$ | |
| ivsync rising | $T_{vr}$ | - | - | 700 | ns | |
| ivsync falling | $T_{vf}$ | - | - | 1.5 | us | |
| Horizontal lines per | | 256 | 262. | 268 | line | Note |

Note1 : Please don't use odd horizontal lines to drive LCD panel for both simult

b. Output signal characteristics

| Paramet | Symbo | Min. | Typ. | Max. | Unit | Remar |
|---|---|---|---|---|---|---|
| rising | $t_r$ | - | - | 10 | ns | |
| falling | $t_f$ | - | - | 10 | ns | |
| clock pulse | $t_{CPH}$ | - | 1.5 | - | $t_{OSC}$ | |
| clock pulse | $t_{OWH}$ | 30 | 33(67 | 70 | % | |
| osth setup | $t_{SUH}$ | - | $t_{CPH}$/2 | - | ns | |
| osth pulse | $t_{STH}$ | - | 1 | - | $t_{CPH}$ | |
| iohsy pulse | $t_{HSY}$ | - | 4.6 | - | us | |
| ooeh pulse | $t_{OEH}$ | - | 2.8 | - | us | |
| sample & hold disable | $t_{DIS1}$ | - | 5.5 | - | us | |
| ope1(2)(3) pulse | $t_{OEV}$ | - | 16 | - | us | |
| ocpv pulse | $t_{CPV}$ | - | $t_H$/2 | - | us | |
| ocpo - ooeh time | $t_1$ | - | 7.4 | - | us | |
| ocpv - opda time | $t_2$ | - | 6.1 | - | us | |
| ope1 - opda time | $t_3$ | - | 14.2 | - | us | |
| ocpo - opda time | $t_4$ | - | 7.7 | - | us | |
| iohsy - opsi time | $t_5$ | - | 4.8 | - | us | |
| opsi pulse | $t_{SPW}$ | - | 4.6 | - | us | |
| ostv1(2) setup | $t_{SUV}$ | - | $t_H$/2 | - | us | |
| ostv1(2) pulse | $t_{STV}$ | - | 1 | - | $t_H$ | |
| iovsy - ostv1(2) time | $t_{VS1(2)}$ | - | 18(27 | - | $t_H$ | Note1 |

Note1) Values in brackets correspond to

7-2) 1440 * 234 mode (6.2",7", 8.4")

a. Input signal characteristics

| Parameter | Symbol | Min. | Typ. | Max. | Units | Remark |
|---|---|---|---|---|---|---|
| iosci perioc | $t_{OSC}$ | 64.5 | 69.5 | 74.5 | ns | |
| icsy period | $T_H$ | 61.5 | 63.5 | 65.5 | us | |
| icsy pulse width | $t_{CSYN}$ | 4 | 4.7 | 5.4 | us | |
| icsy rising time | $T_{cr}$ | - | - | 700 | ns | |
| icsy falling time | $T_{cf}$ | - | - | 300 | ns | |
| ivsync pulse width | $t_{VSY}$ | 1 | 3 | 5 | $t_H$ | |
| ivsync rising time | $T_{vr}$ | - | - | 700 | ns | |
| ivsync falling time | $T_{vf}$ | - | - | 1.5 | us | |
| Horizontal lines per field | | 256 | 262.5 | 268 | line | Note1 |

Note1 : Please don't use odd horizontal lines to drive LCD panel for both odd and even field simultaneously

b. Output signal characteristics

| Parameter | Symbol | Min. | Typ. | Max. | Units | Remark |
|---|---|---|---|---|---|---|
| rising time | $t_r$ | - | - | 10 | ns | |
| falling time | $t_f$ | - | - | 10 | ns | |
| clock pulse width | $t_{CPH}$ | - | 1.5 | - | $t_{OSC}$ | |
| clock pulse duty | $t_{CWH}$ | 30 | 33(67) | 70 | % | |
| osth setup time | $t_{SUH}$ | - | $t_{CPH}/2$ | - | ns | |
| osth pulse width | $t_{STH}$ | - | 1 | - | $t_{CPH}$ | |
| iohsy pulse width | $t_{HSY}$ | - | 4.65 | - | us | |
| ooeh pulse width | $t_{OEH}$ | - | 3.46 | - | us | |
| sample & hold disable time | $t_{DIS1}$ | - | 5.52 | - | us | |
| ooe1(2)(3) pulse width | $t_{OEV}$ | - | 16 | - | us | |
| ocpv pulse width | $t_{CPV}$ | - | $t_H/2$ | - | us | |
| ocpo - ooeh time diff. | $t_1$ | - | -2.8 | - | us | |
| ocpv - opda time diff. | $t_2$ | - | 8.56 | - | us | |
| ooe1 - opda time diff. | $t_3$ | - | 16.64 | - | us | |
| ocpo - opda time diff. | $t_4$ | - | -1.8 | - | us | |
| iohsy - opsi time diff. | $t_5$ | - | 4.8 | - | us | |
| opsi pulse width | $t_{PSIW}$ | - | 4.48 | - | us | |
| ostv1(2) setup time | $t_{SUV}$ | - | $t_H/2$ | - | us | |
| ostv1(2) pulse width | $t_{STV}$ | - | 1 | - | $t_H$ | |
| iovsy - ostv1(2) time diff. | $t_{VS1(2)}$ | - | 18(27) | - | $t_H$ | Note1) |

Note1) Values in brackets correspond to PAL mode

7-3) 960 * 234 mode (Stripe mode, 3.6",4.5", 5", 6.4")

a. Input signal characteristics

| Parameter | Symbol | Min. | Typ. | Max. | Units | Remark |
|---|---|---|---|---|---|---|
| iosci perio | $t_{OSC}$ | 100.2 | 104.2 | 108.2 | ns | |
| icsy period | $T_H$ | 61.5 | 63.5 | 65.5 | us | |
| icsy pulse width | $t_{CSYN}$ | 4 | 4.7 | 5.4 | us | |
| icsy rising time | $T_{cr}$ | - | - | 700 | ns | |
| icsy falling tim | $T_{cf}$ | - | - | 300 | ns | |
| ivsync pulse width | $t_{VSY}$ | 1 | 3 | 5 | $t_H$ | |
| ivsync rising time | $T_{vr}$ | - | - | 700 | ns | |
| ivsync falling time | $T_{vf}$ | - | - | 1.5 | us | |
| Horizontal lines per field | | 256 | 262.5 | 268 | line | Note1 |

Note1 : Please don't use odd horizontal lines to drive LCD panel for both odd and even field simultaneously

b. Output signal characteristics

| Parameter | Symbol | Min. | Typ. | Max. | Units | Remark |
|---|---|---|---|---|---|---|
| rising time | $t_r$ | - | - | 10 | ns | |
| falling time | $t_f$ | - | - | 10 | ns | |
| clock pulse width | $t_{CPH}$ | - | 1.5 | - | $t_{OSC}$ | |
| clock pulse duty | $t_{CWH}$ | 30 | 33(67) | 70 | % | |
| osth setup tim | $t_{SUH}$ | - | $t_{CPH}/2$ | - | ns | |
| osth pulse width | $t_{STH}$ | - | 1 | - | $t_{CPH}$ | |
| iohsy pulse width | $t_{HSY}$ | - | 4.76 | - | us | |
| ooeh pulse width | $t_{OEH}$ | - | 3.52 | - | us | |
| sample & hold disable tin | $t_{DIS1}$ | - | 5.82 | - | us | |
| ooe1(2)(3) pulse width | $t_{OEV}$ | - | 17.2 | - | us | |
| ocpv pulse width | $t_{CPV}$ | - | $t_W/2$ | - | us | |
| ocpo - ooeh time diff. | $t_1$ | - | 4.4 | - | us | |
| ocpv - opda time diff. | $t_2$ | - | 8.56 | - | us | |
| ooe1 - opda time diff. | $t_3$ | - | 16.6 | - | us | |
| ocpo - opda time diff. | $t_4$ | - | 5.5 | - | us | |
| iohsy - opsi time diff. | $t_5$ | - | 4.88 | - | us | |
| opsi pulse width | $t_{PSW}$ | - | 4.8 | - | us | |
| ostv1(2) setup time | $t_{SUV}$ | - | $t_W/2$ | - | us | |
| ostv1(2) pulse width | $t_{STV}$ | - | 1 | - | $t_H$ | |
| iovsy - ostv1(2) time diff. | $t_{VS1(2)}$ | - | 18(27) | - | $t_H$ | Note1) |

Note1) Values in brackets correspond to PAL mode

7-4) 480 * 234 mode (2.5", 3.5")

a. Input signal characteristics

| Parameter | Symbol | Min. | Typ. | Max. | Units | Remark |
|---|---|---|---|---|---|---|
| dsciperiod | $t_{DSC}$ | 100.2 | 104.2 | 109.2 | ns | |
| hsy period | $T_H$ | 61.5 | 63.5 | 65.5 | us | |
| hsy pulse width | $t_{HSYW}$ | 4 | 4.7 | 5.4 | us | |
| hsy rising time | $T_{HR}$ | - | - | 700 | ns | |
| hsy falling time | $T_{HF}$ | - | - | 300 | ns | |
| vsync pulse width | $t_{VST}$ | 1 | 3 | 5 | $t_H$ | |
| vsync rising time | $T_{VR}$ | - | - | 700 | ns | |
| vsync falling time | $T_{VF}$ | - | - | 1.5 | us | |
| Horizontal lines per field | | 256 | 262.5 | 268 | line | Note1 |

Note1 : Please don't use odd horizontal lines to drive LCD panel for both odd and even field simultaneously

b. Output signal characteristics

| Parameter | Symbol | Min. | Typ. | Max. | Units | Remark |
|---|---|---|---|---|---|---|
| rising time | $t_r$ | - | - | 10 | ns | |
| falling time | $t_f$ | - | - | 10 | ns | |
| clock pulse width | $t_{CPW}$ | - | 3 | - | $t_{DSC}$ | |
| clock pulse duty | $t_{CWH}$ | 30 | 33 | 40 | % | |
| osth setup time | $t_{STH}$ | - | $t_{CPW}/2$ | - | ns | |
| osth pulse width | $t_{STH}$ | - | 1 | - | $t_{CPH}$ | |
| ohsy pulse width | $t_{HSY}$ | - | 4.76 | - | us | |
| ooeh pulse width | $t_{OEH}$ | - | 3.52 | - | us | |
| sample & hold disable time | $t_{SHD}$ | - | 5.82 | - | us | |
| ooe1(2)(3) pulse width | $t_{OEV}$ | - | 17.2 | - | us | |
| ocpv pulse width | $t_{CPV}$ | - | $t_H/2$ | - | us | |
| ocpo - ooeh time diff. | $t_A$ | - | 4.4 | - | us | |
| ocpv - opda time diff. | $t_B$ | - | 8.56 | - | us | |
| ooe1 - opda time diff. | $t_B$ | - | 16.6 | - | us | |
| ocpo - opda time diff. | $t_A$ | - | 5.5 | - | us | |
| ohsy - opsi time diff. | $t_B$ | - | 4.88 | - | us | |
| opsi pulse width | $t_{PSW}$ | - | 4.8 | - | us | |
| ostv1(2) setup time | $t_{STV}$ | - | $t_H/2$ | - | us | |
| ostv1(2) pulse width | $t_{STV}$ | - | 1 | - | $t_H$ | |
| ovsy - ostv1(2) time diff. | $t_{VS1(2)}$ | - | 18(27) | - | $t_H$ | Note1) |

Note1) Values in brackets correspond to PAL mode

7-5) 1920 * 234 mode (9")

| Parameter | Symbol | Min. | Typ. | Max. | Units | Remark |
|---|---|---|---|---|---|---|
| iosci perio( | $t_{OSC}$ | 50.1 | 52.1 | 54.1 | ns | |
| icsy period | $T_H$ | 61.5 | 63.5 | 65.5 | us | |
| icsy pulse width | $t_{CSYN}$ | 4 | 4.7 | 5.4 | us | |
| icsy rising time | $T_{cr}$ | - | - | 700 | ns | |
| icsy falling tim» | $T_{cf}$ | - | - | 300 | ns | |
| ivsync pulse width | $t_{VSY}$ | 1 | 3 | 5 | $t_H$ | |
| ivsync rising time | $T_{vr}$ | - | - | 700 | ns | |
| ivsync falling time | $T_{vf}$ | - | - | 1.5 | us | |
| Horizontal lines per field | | 256 | 262.5 | 268 | line | Note1 |

Note1 : Please don't use odd horizontal lines to drive LCD panel for both odd and even field simultaneously

b. Output signal characteristics

| Parameter | Symbol | Min. | Typ. | Max. | Units | Remark |
|---|---|---|---|---|---|---|
| rising time | $t_r$ | - | - | 10 | ns | |
| falling time | $t_f$ | - | - | 10 | ns | |
| clock pulse width | $t_{CPH}$ | - | 1.5 | - | $t_{OSC}$ | |
| clock pulse duty | $t_{DWH}$ | 30 | 33(67) | 70 | % | |
| osth setup tim» | $t_{SUH}$ | - | $t_{CPH}$/2 | - | ns | |
| osth pulse width | $t_{STH}$ | - | 1 | - | $t_{CPH}$ | |
| iohsy pulse width | $t_{HSY}$ | - | 4.6 | - | us | |
| ooeh pulse width | $t_{OEH}$ | - | 3.6 | - | us | |
| sample & hold disable tirr | $t_{DIS1}$ | - | 5.26 | - | us | |
| ooe1(2)(3) pulse width | $t_{OEV}$ | - | 16 | - | us | |
| ocpv pulse width | $t_{CPV}$ | - | $t_H$/2 | - | us | |
| ocpo - ooeh time diff. | $t_1$ | - | 4.08 | - | us | |
| ocpv - opda time diff. | $t_2$ | - | 8.72 | - | us | |
| ooe1 - opda time diff. | $t_3$ | - | 16.8 | - | us | |
| ocpo - opda time diff. | $t_4$ | - | 5 | - | us | |
| iohsy - opsi time diff. | $t_5$ | - | 3.3 | - | us | |
| opsi pulse width | $t_{PSW}$ | - | 4.64 | - | us | |
| ostv1(2) setup time | $t_{SUV}$ | - | $t_H$/2 | - | us | |
| ostv1(2) pulse width | $t_{STV}$ | - | 1 | - | $t_H$ | |
| iovsy - ostv1(2) time diff. | $t_{VS1(2)}$ | - | 18(27) | - | $t_H$ | Note1) |

Note1) Values in brackets correspond to PAL mode

7-6) 960 * 234 mode (Delta mode, 3.5")

a. Input signal characteristics

| Parameter | Symbol | Min. | Typ. | Max. | Units | Remark |
|---|---|---|---|---|---|---|
| ibsciperiod | $t_{BSC}$ | 50.1 | 52.1 | 54.1 | ns | |
| icsy period | $T_H$ | 61.5 | 63.5 | 65.5 | us | |
| icsy pulse width | $t_{CSYH}$ | 4 | 4.7 | 5.4 | us | |
| icsy rising time | $T_{CR}$ | - | - | 700 | ns | |
| icsy falling time | $T_{CF}$ | - | - | 300 | ns | |
| ivsync pulse width | $t_{VSY}$ | 1 | 3 | 5 | $t_H$ | |
| ivsync rising time | $T_{VR}$ | - | - | 700 | ns | |
| ivsync falling time | $T_{VF}$ | - | - | 1.5 | us | |
| Horizontal lines per field | | 256 | 262.5 | 268 | line | Note1 |

Note1 : Please don't use odd horizontal lines to drive LCD panel for both odd and even field simultaneously

b. Output signal characteristics

| Parameter | Symbol | Min. | Typ. | Max. | Units | Remark |
|---|---|---|---|---|---|---|
| rising time | $t_r$ | - | - | 10 | ns | |
| falling time | $t_f$ | - | - | 10 | ns | |
| clock pulse width | $t_{CPH}$ | - | 3 | - | $t_{BSC}$ | |
| clock pulse duty | $t_{CWH}$ | 30 | 33(67) | 70 | % | |
| osth setup time | $t_{SUH}$ | - | $t_{CPH}/2$ | - | ns | |
| osth pulse width | $t_{STH}$ | - | 1 | - | $t_{CPH}$ | |
| iohsy pulse width | $t_{HSY}$ | - | 4.6 | - | us | |
| ooeh pulse width | $t_{OEH}$ | - | 3.6 | - | us | |
| sample & hold disable time | $t_{DIS1}$ | - | 5.26 | - | us | |
| ooe1(2)(3) pulse width | $t_{OEV}$ | - | 16 | - | us | |
| ocpv pulse width | $t_{CPV}$ | - | $t_H/2$ | - | us | |
| ocpo - ooeh time diff. | $t_1$ | - | 4.08 | - | us | |
| ocpv - opda time diff. | $t_2$ | - | 8.72 | - | us | |
| ooe1 - opda time diff. | $t_3$ | - | 16.8 | - | us | |
| ocpo - opda time diff. | $t_4$ | - | 5 | - | us | |
| iohsy - opsi time diff. | $t_5$ | - | 3.3 | - | us | |
| opsi pulse width | $t_{PSW}$ | - | 4.64 | - | us | |
| ostv1(2) setup time | $t_{STV}$ | - | $t_H/2$ | - | us | |
| ostv1(2) pulse width | $t_{STV}$ | - | 1 | - | $t_H$ | |
| iovsy - ostv1(2) time diff. | $t_{VS1(2)}$ | - | 18(27) | - | $t_H$ | Note1) |

Note1) Values in brackets correspond to PAL mode

## 8. Display Position

### 8-1. Horizontal position

| Items | Symbol | Conditions | NTSC | PAL | unit | Remark |
|---|---|---|---|---|---|---|
| Horizontal Start Position | HPOS | - | 11.78 | 11.89 | us | *) |
| Horizontal display Area | HDIS | - | 50.01 | 50.36 | us | **) |

*) Sampling start based on the csy's rising edge

**) Horizontal display position is changed by delay

### 8-2. Vertical position

| Items | Symbol | Conditions | | Display mode: Full Normal | Wide | Zoom1 | Zoom2 | Zoom3 | unit | Remark |
|---|---|---|---|---|---|---|---|---|---|---|
| Vertical Start Position | VPOS | NTSC | Odd | 25 | 25 | 55 | 41 | 56 | Line | *) |
| | | | Even | 288 | 288 | 318 | 304 | 318 | | |
| | | PAL | Odd | 31 | 31 | 65 | 51 | 68 | Line | |
| | | | Even | 343 | 343 | 377 | 363 | 380 | | |
| Vertical displa | VDIS | NTSC | | 234 | 234 | 176 | 204 | 204 | Line | |
| Position | | PAL | | 273 | 273 | 199 | 234 | 234 | Line | |

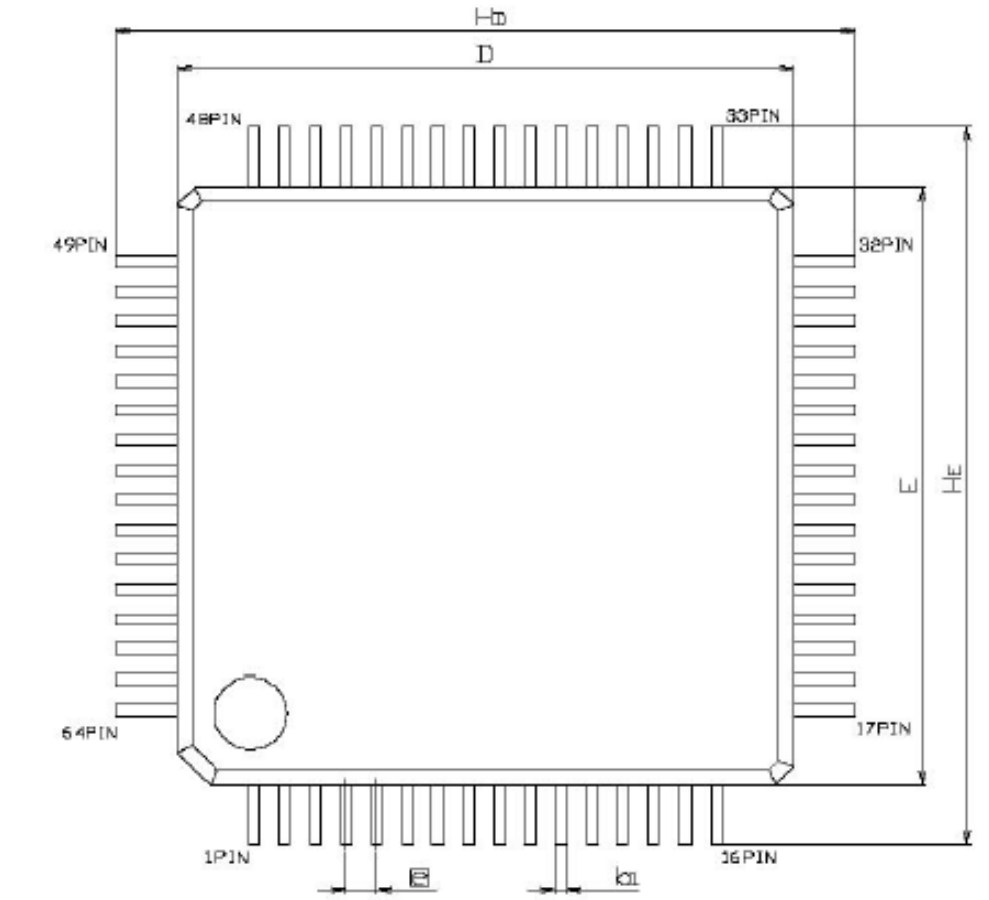
*) Sampling start line number base on Line no

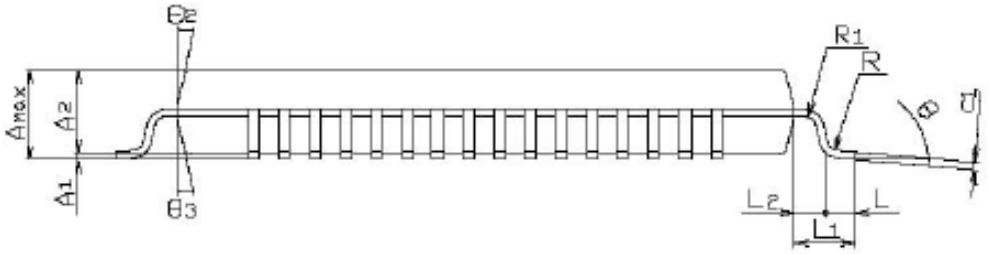
## 9. Reliability test items

| No. | Test items | Conditions | Remark |
|---|---|---|---|
| 1 | High temperature storage | Ta = 150< 240h | |
| 2 | Low temperature storage | Ta = -60< 240h | |
| 3 | High temperature operation | Ta = 85< 240h | |
| 4 | Low temperature operation | Ta = -40< 240h | |
| 5 | High temperature and High huminity | Ta = 80< , 95%RH 240h | operation |
| 6 | Heat shock | -30< , < , < 200cycle<br>30min, 5mun, 30min | non- operation |
| 7 | Electrostatic discharge | < 200V, 200pF(0? )<br>once for each terminal | non- operation |

Note : Ta = Ambient temperature

## 10. Package information




| | Symbol | Dimension in Millimeters | | |
|---|---|---|---|---|
| | | Min | Nom | Max |
| * | F | 9.9 | 10 | 10.1 |
| * | D | 9.9 | 10 | 10.1 |
| | Amax | | | 1.7 |
| | A1 | | 0.1 | |
| | A2 | 1.3 | 1.4 | 1.5 |
| | e | | 0.5 | |
| * | b1 | 0.13 | 0.18 | 0.28 |
| * | c1 | 0.1 | 0.125 | 0.175 |
| | θ | 0° | | 10° |
| | L | 0.3 | 0.5 | 0.7 |
| | L1 | | 1 | |
| | L2 | | 0.5 | |
| | HE | 11.6 | 12 | 12.4 |
| | HD | 11.6 | 12 | 12.4 |
| | θ2 | | 12° | |
| | θ3 | | 12° | |
| | R | | 0.2 | |
| | R1 | | 0.2 | |

*E,D Excluding the tie bar cutting stub

b1 Lead width of basemetal.

c1 Lead thickness of basemetal.

A. The timing Diagram

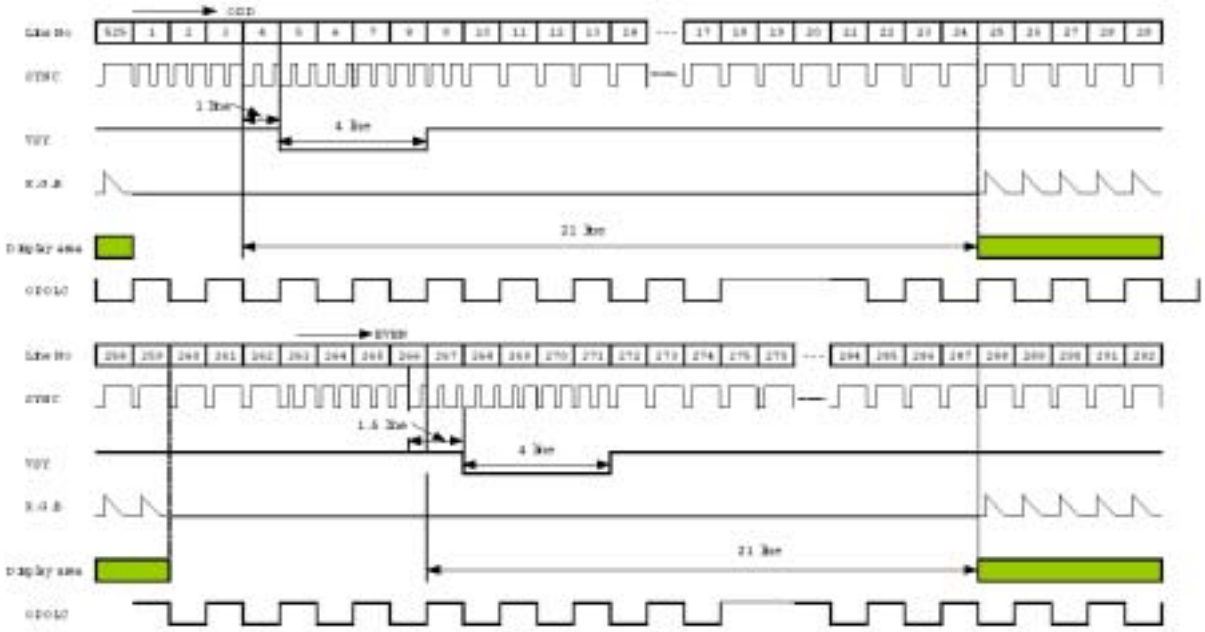


Fig.1. NTSC Vertical (odd_sel= "High")

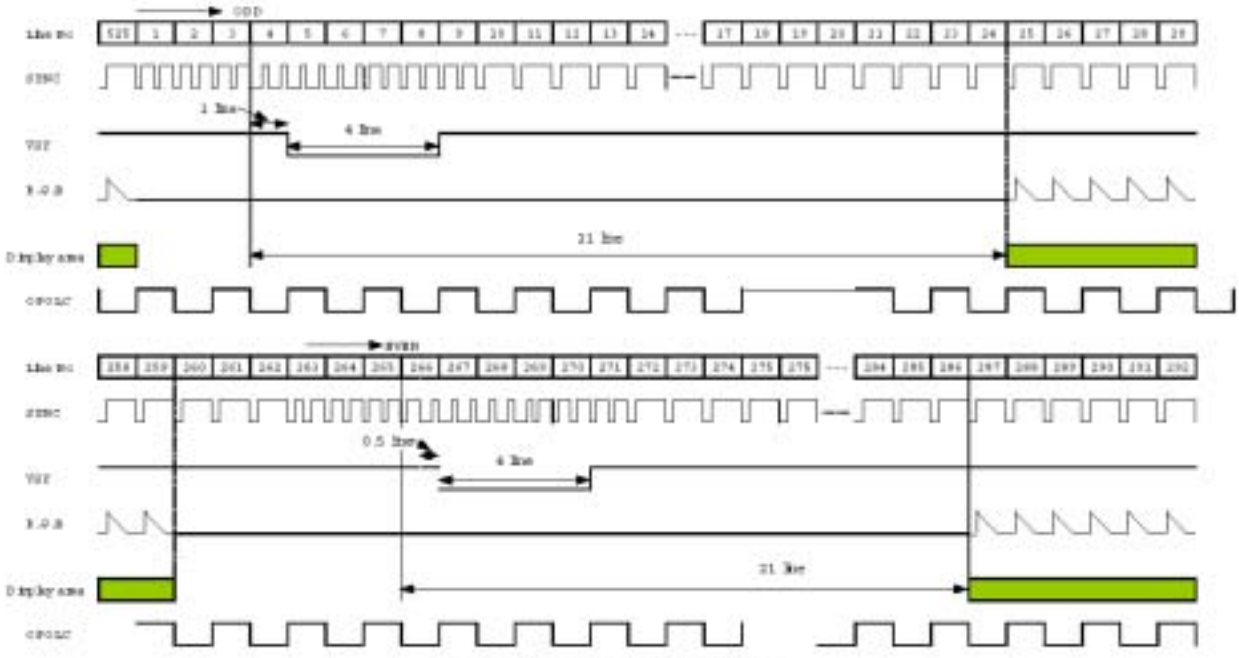


Fig.2. NTSC Vertical (odd sel= "Low")

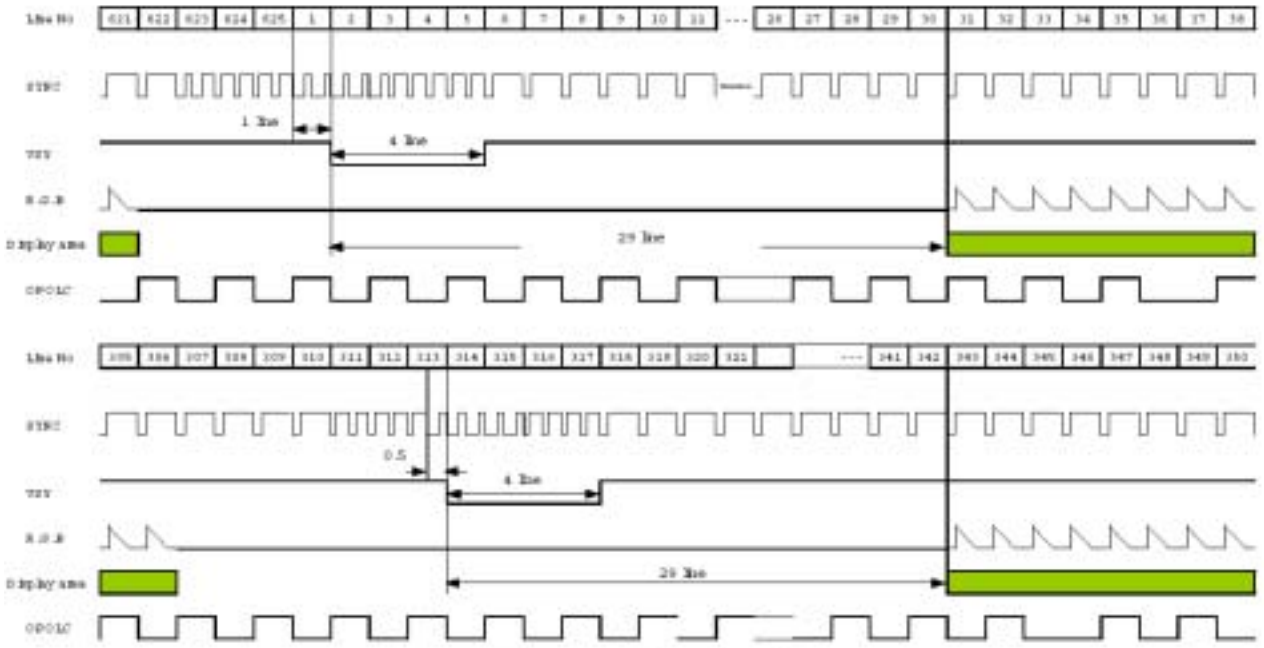


Fig.3. PAL Vertical (R_sel= "H")

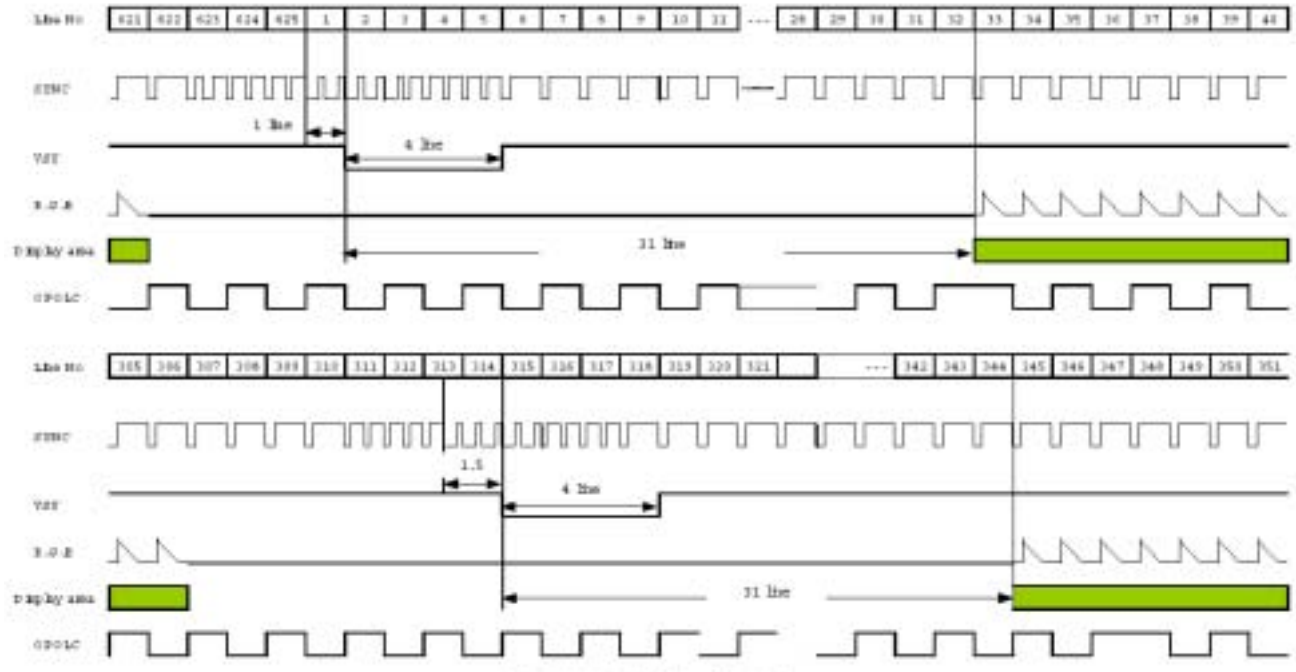
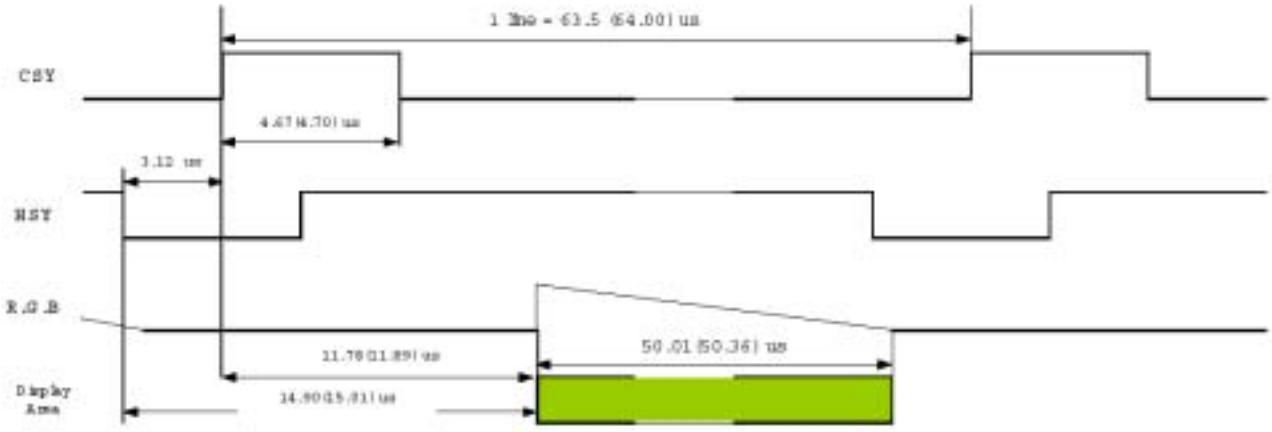


Fig.4. PAL Vertical (R_sel= "L")




*) Values in brackets correspond to PAL mode
**) fH = 15.734 (15.625) kHz
***) Horizontal display position is changed by delay time (control cpi, cpo)

Fig.5. Horizontal (NTSC/PAL)

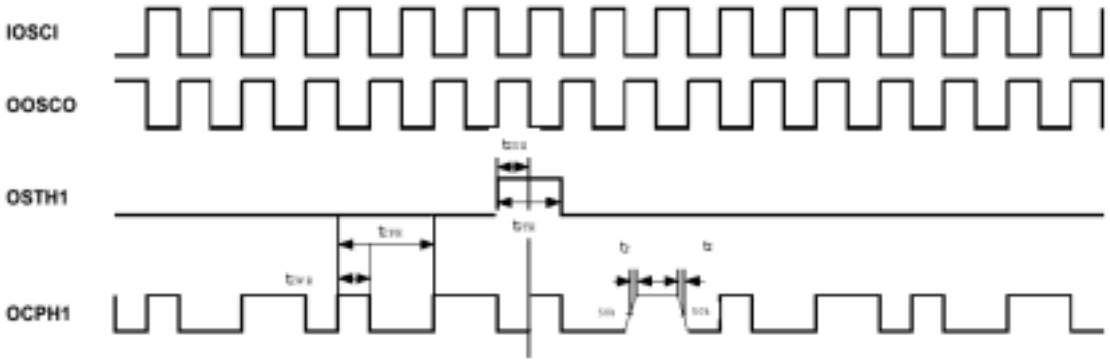



FIG.6 Sampling clock timing (1920,1440,1200,960*234m ode)

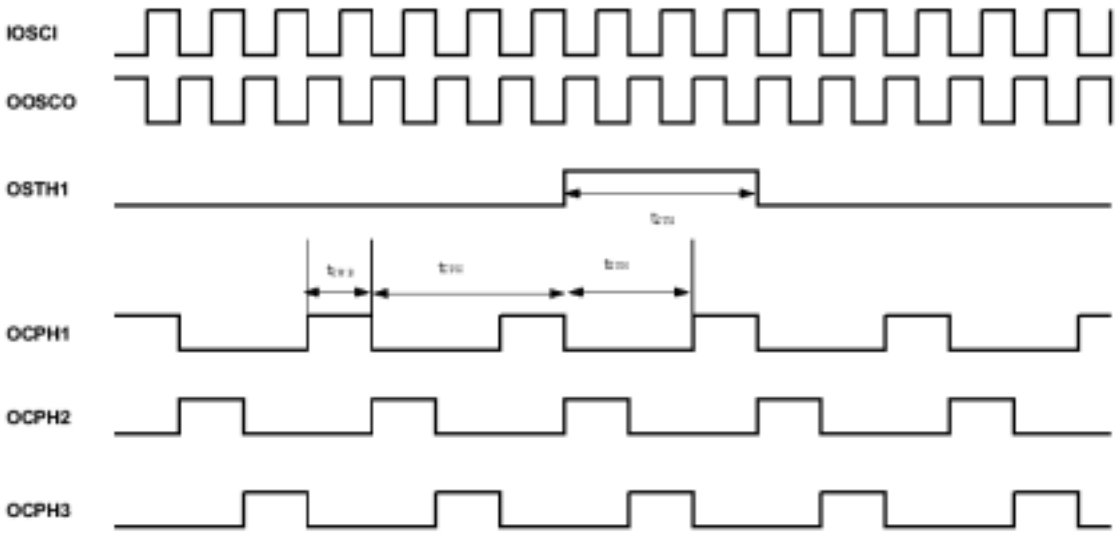



FIG .7 Sampling clock timing(960,480*234mode(Delta mode))

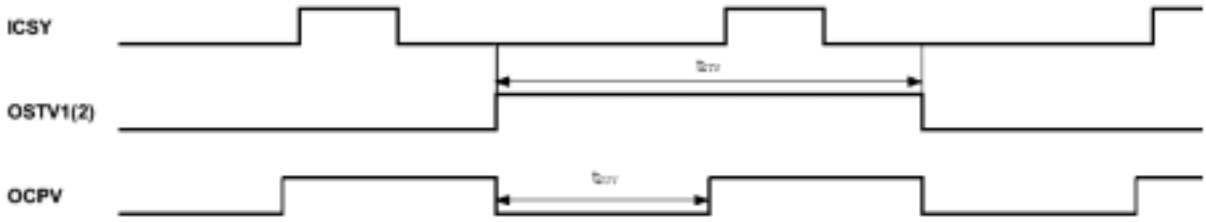



FIG .8 Vertical shift clock timing

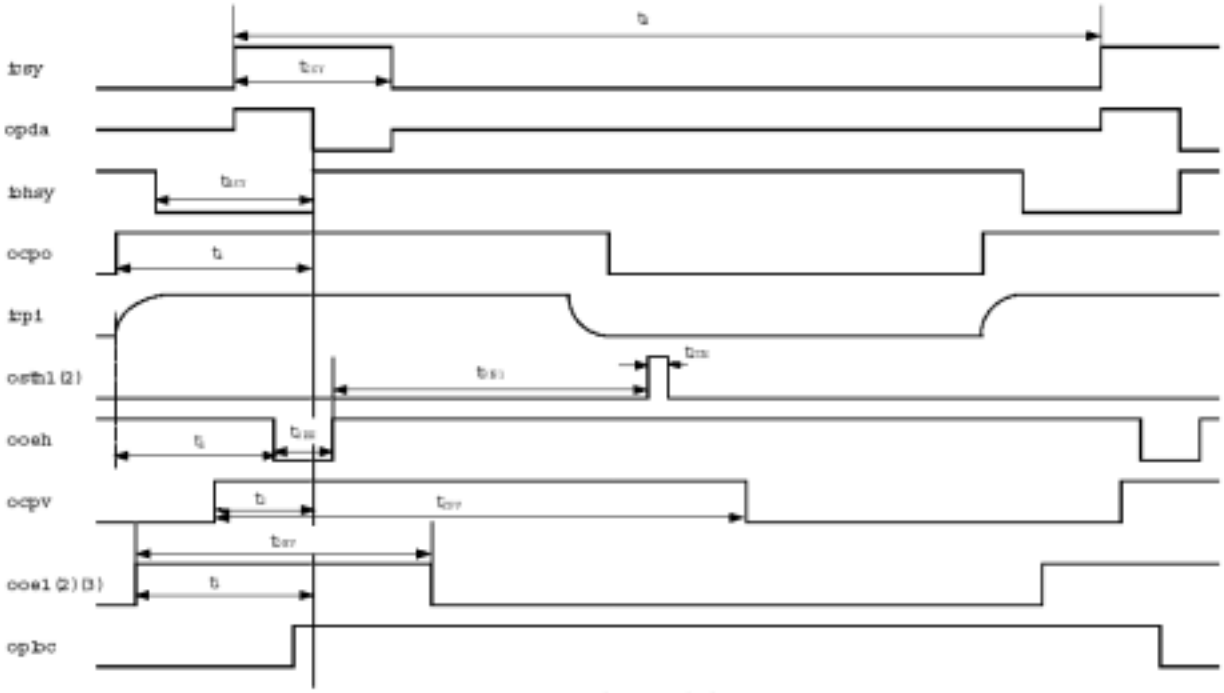



FIG .9 HorizontalTiming

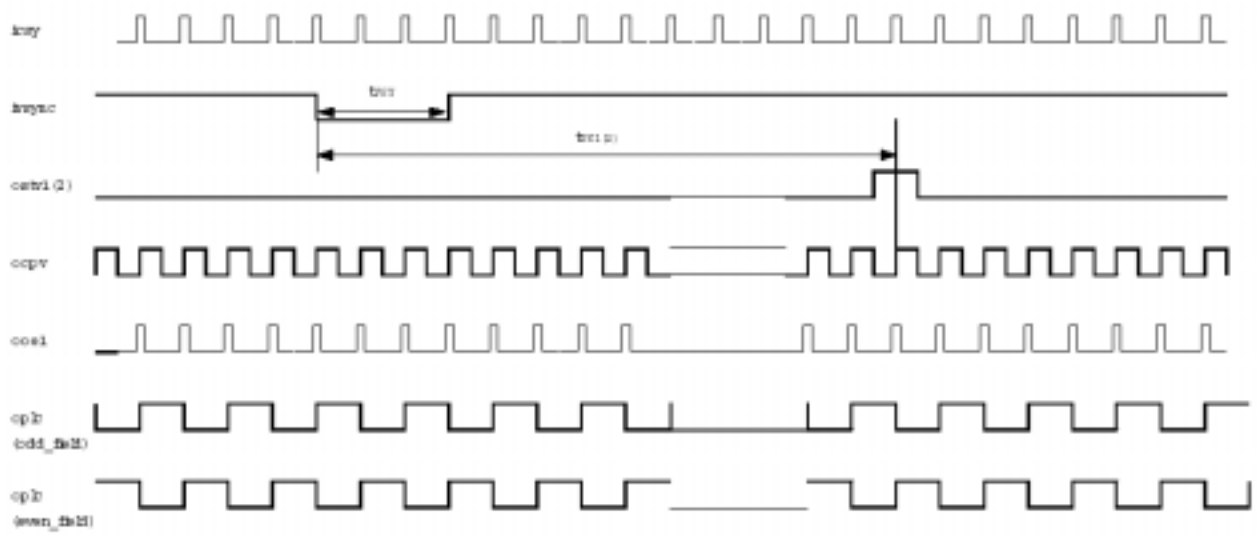
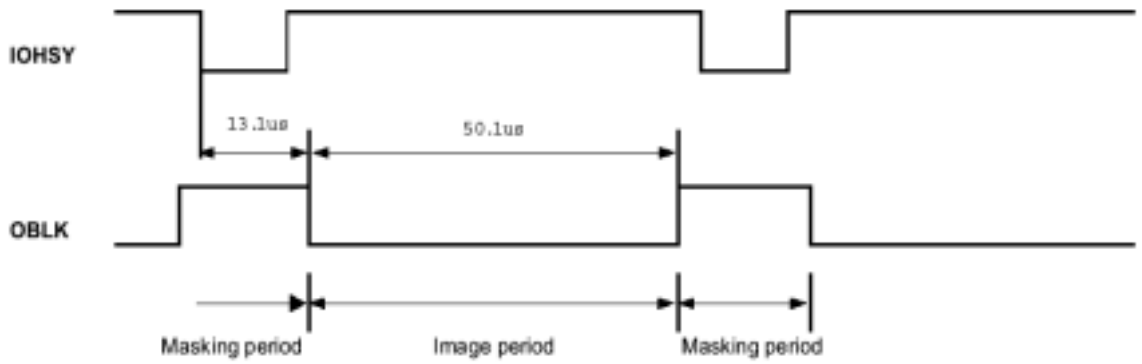



FIG .10 VerticalTiming




* Display range can adjust by H-position

FIG.11 Input/output signal waveforms(Normal center, Normal left, Normal right mode)

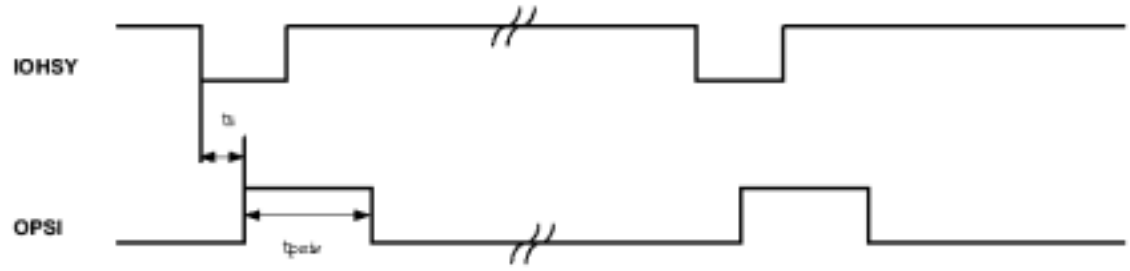
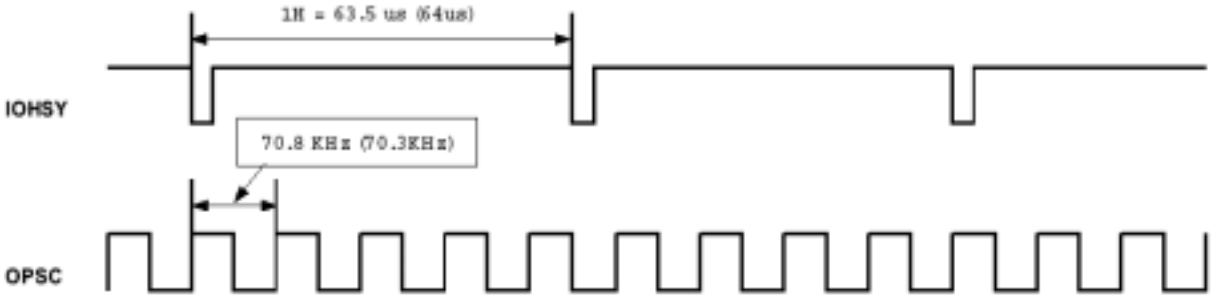



FIG.12 OPSI timing




Note1) Values in brackets correspond to PAL mode

FIG.13 OPSC dimming timing