



SPP8803

P-Channel Enhancement Mode MOSFET

DESCRIPTION

The SPP8803 is the Dual P-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology.

This high density process is especially tailored to minimize on-state resistance.

These devices are particularly suited for low voltage application , notebook computer power management and other battery powered circuits where high-side switching .

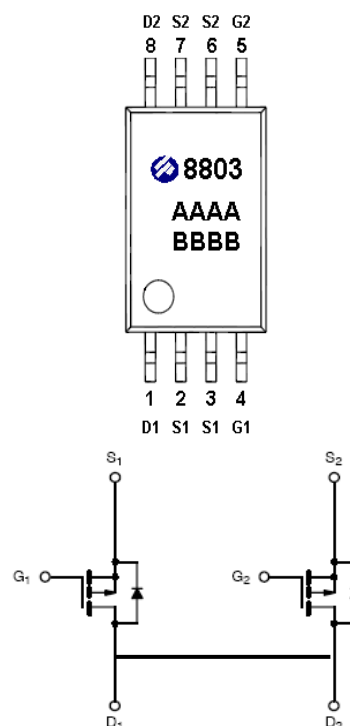
FEATURES

- ◆ -20V/-7.0A, $R_{DS(ON)}=20m\Omega@V_{GS}=-4.5V$
- ◆ -20V/-6.0 A, $R_{DS(ON)}=25m\Omega@V_{GS}=-2.5V$
- ◆ -20V/-5.0 A, $R_{DS(ON)}=35m\Omega@V_{GS}=-1.8V$
- ◆ Super high density cell design for extremely low $R_{DS(ON)}$
- ◆ Exceptional on-resistance and maximum DC current capability
- ◆ TSSOP-8P package design

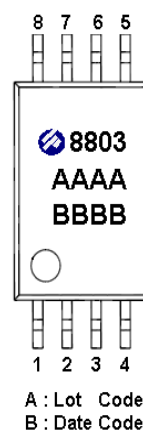
APPLICATIONS

- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- DSC
- LCD Display inverter

PIN CONFIGURATION(TSSOP – 8P)



PART MARKING





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PIN DESCRIPTION

Pin	Symbol	Description
1	D1	Drain
2	S1	Source
3	S1	Source
4	G1	Gate
5	G2	Gate
6	S2	Source
7	S2	Source
8	D2	Drain

ORDERING INFORMATION

Part Number	Package	Part Marking
SPP8803TS8RGB	TSSOP- 8P	8803

※ SPP8803TS8RGB : 13" Tape Reel ; Pb – Free; Halogen -Free

ABSOLUTE MAXIMUM RATINGS

(TA=25°C Unless otherwise noted)

Parameter	Symbol	Typical	Unit
Drain-Source Voltage	V _{DSS}	-20	V
Gate –Source Voltage	V _{GSS}	±12	V
Continuous Drain Current(T _J =150°C)	I _D	-7.0	A
		-5.8	
Pulsed Drain Current	I _{DM}	-30	A
Continuous Source Current(Diode Conduction)	I _S	-2.3	A
Power Dissipation	P _D	1.5	W
		0.9	
Operating Junction Temperature	T _J	-55/150	°C
Storage Temperature Range	T _{STG}	-55/150	°C
Thermal Resistance-Junction to Ambient	R _{θJA}	80	°C/W



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ELECTRICAL CHARACTERISTICS

(T_A=25°C Unless otherwise noted)

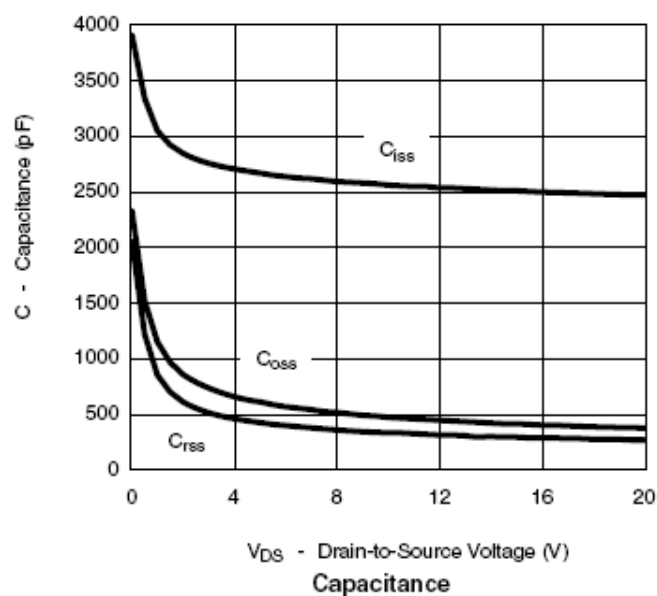
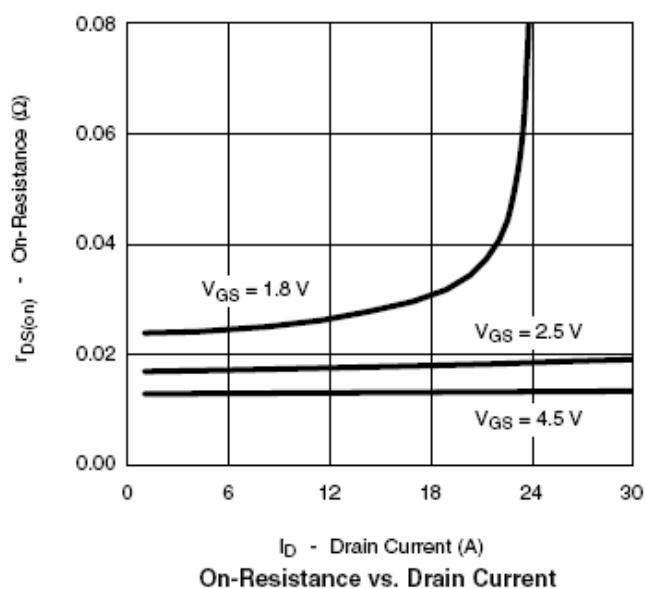
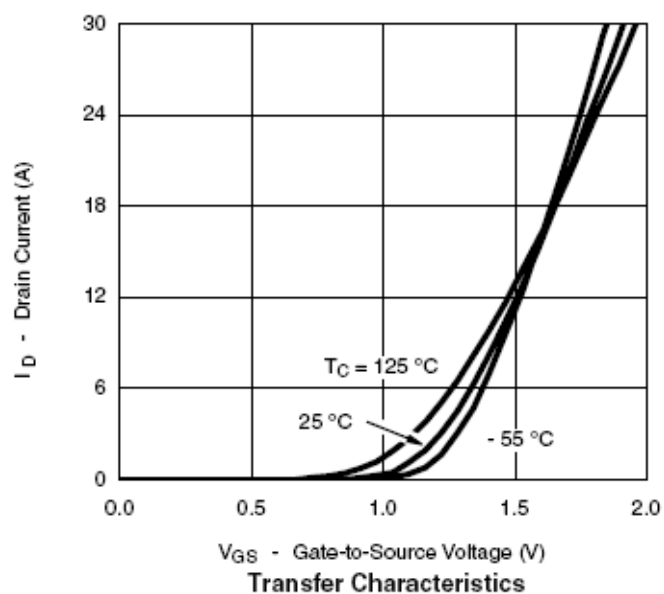
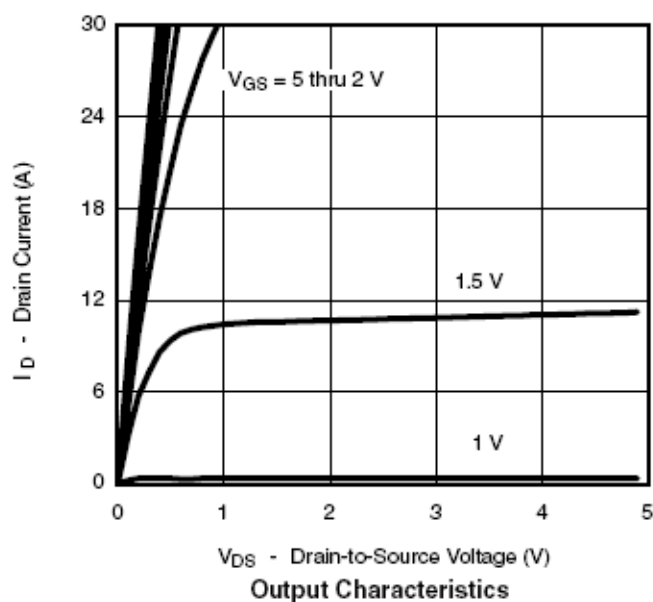
Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} =0V, I _D =-250uA	-20			V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =-250uA	-0.35		-0.9	
Gate Leakage Current	I _{GSS}	V _{DS} =0V, V _{GS} =±12V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =-16V, V _{GS} =0V			-1	uA
		V _{DS} =-20V, V _{GS} =0V T _J =55°C			-10	
On-State Drain Current	I _{D(on)}	V _{DS} ≤ -5V, V _{GS} =-4.5V	-20			A
Drain-Source On-Resistance	R _{DS(on)}	V _{GS} =- 4.5V, I _D =-7.0A		0.016	0.020	Ω
		V _{GS} =- 2.5V, I _D =-6.0A		0.020	0.025	
		V _{GS} =- 1.8V, I _D =-5.0A		0.028	0.035	
Forward Transconductance	g _{fs}	V _{DS} =-5.0V, I _D =-10.0A		36		S
Diode Forward Voltage	V _{SD}	I _S =-2.5A, V _{GS} =0V		-0.8	-1.2	V
Dynamic						
Total Gate Charge	Q _g	V _{DS} =-10V, V _{GS} =-5.0V I _D =-10.0A		30	45	nC
Gate-Source Charge	Q _{gs}			4.5		
Gate-Drain Charge	Q _{gd}			8.0		
Input Capacitance	C _{iss}	V _{DS} =-10V, V _{GS} =0V f=1MHz		2670		pF
Output Capacitance	C _{oss}			520		
Reverse Transfer Capacitance	C _{rss}			480		
Turn-On Time	t _{d(on)}	V _{DD} =-10V, R _L =15Ω I _D =-1.0A, V _{GEN} =-4.5V R _G =6Ω		25	40	ns
	t _r			45	70	
Turn-Off Time	t _{d(off)}			145	240	
	t _f			70	115	



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TYPICAL CHARACTERISTICS

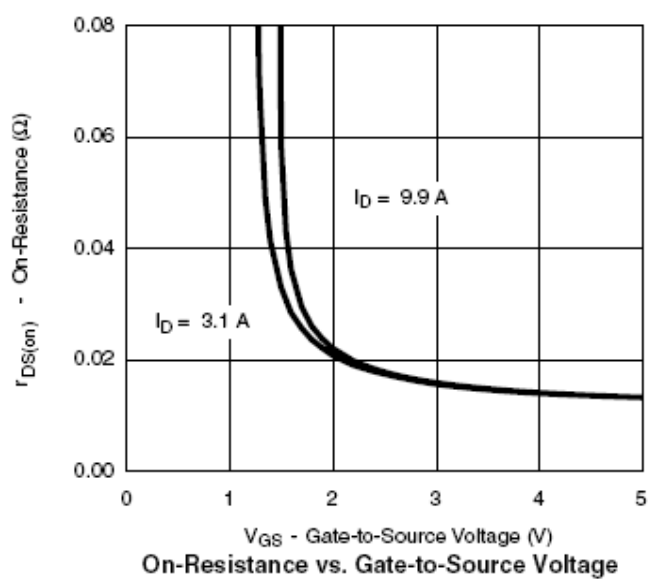
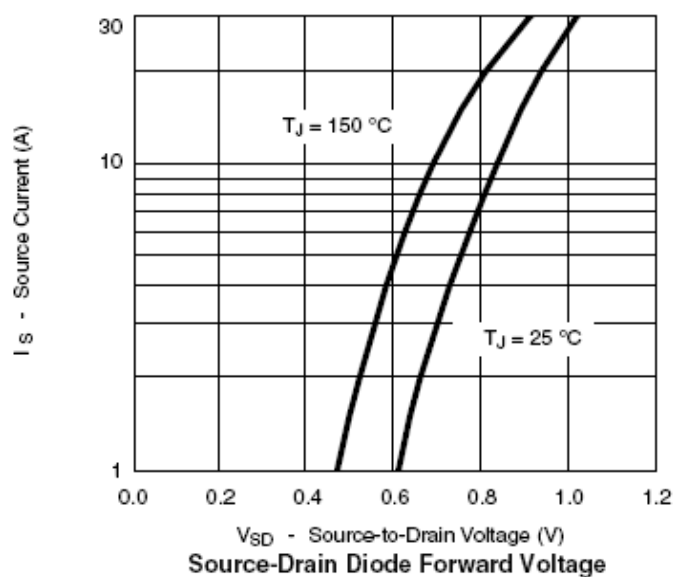
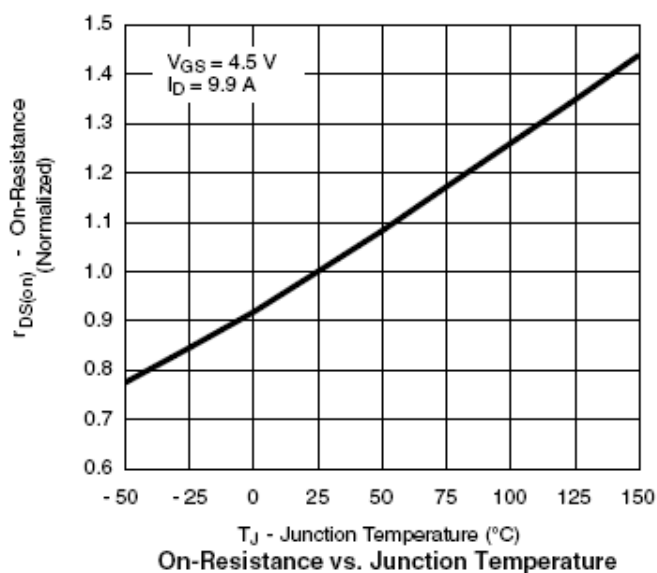
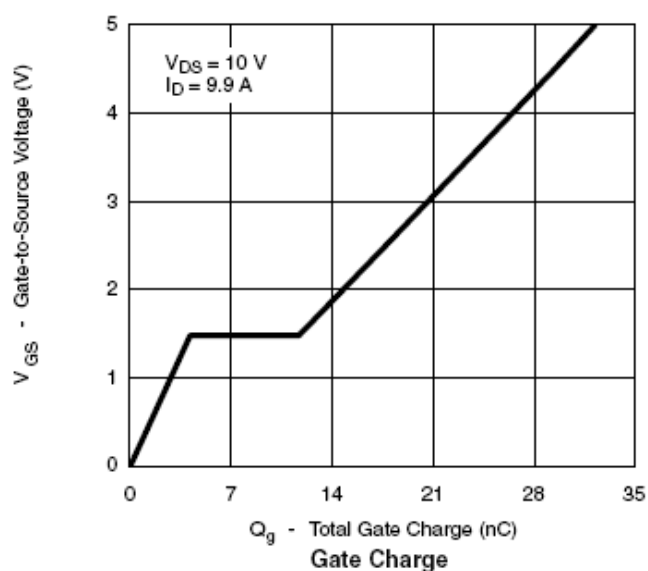




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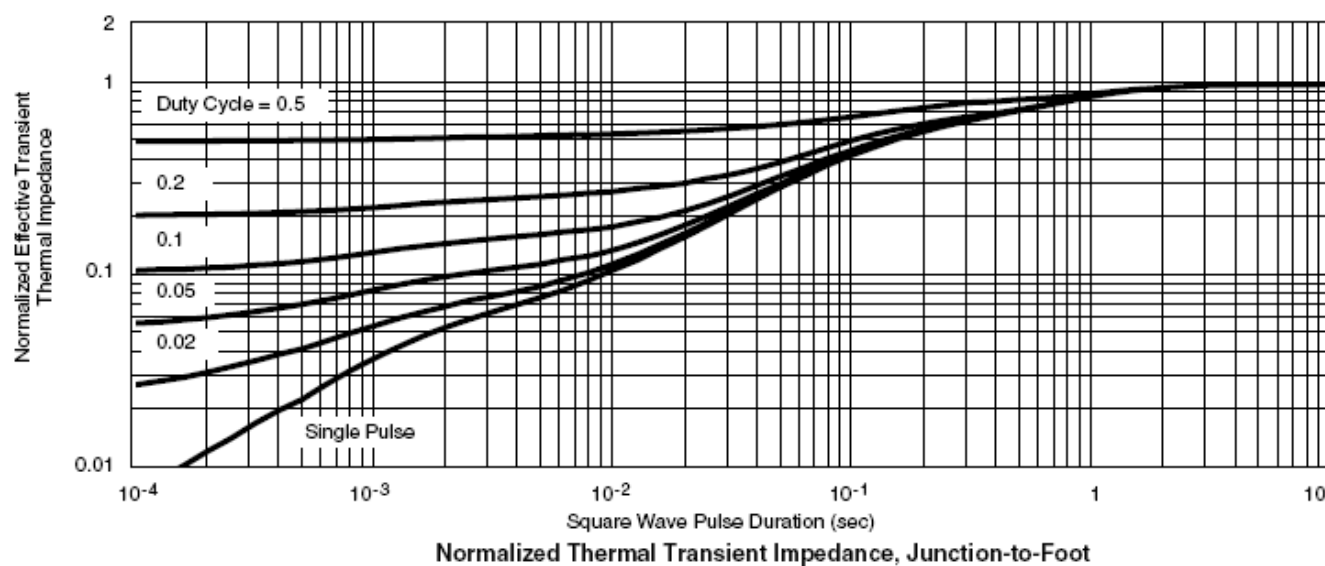
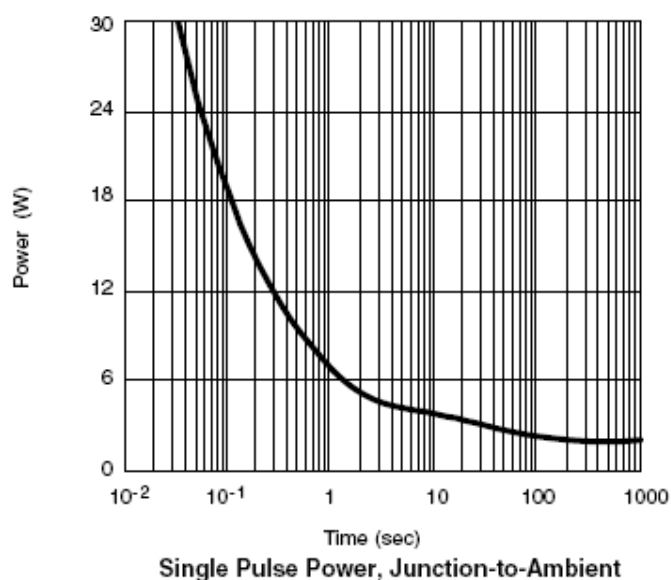
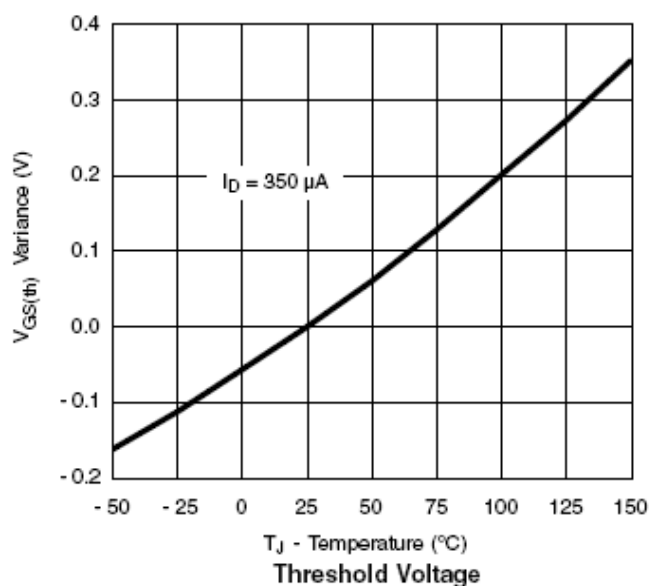




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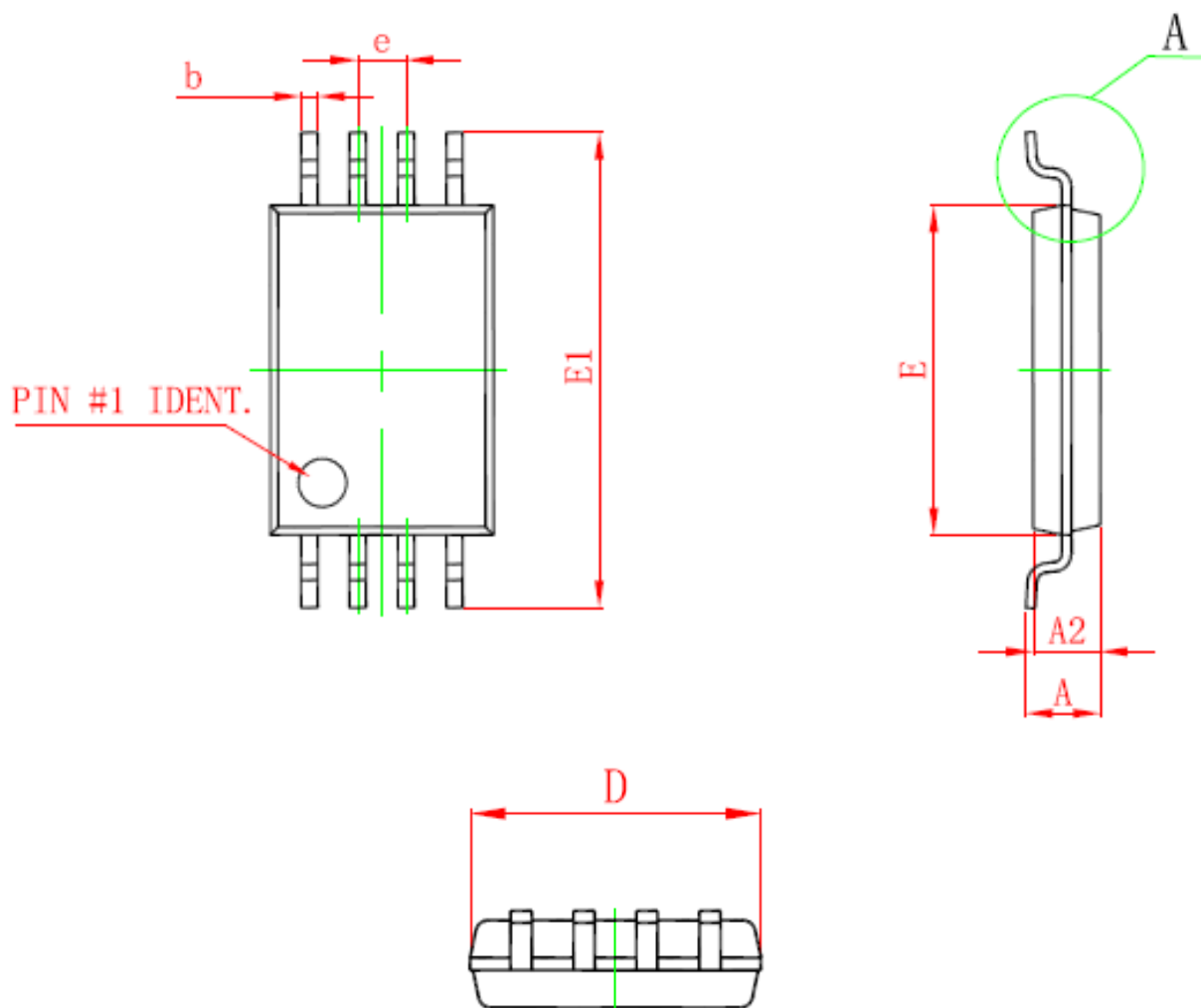




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TSSOP- 8P PACKAGE OUTLINE



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
D	2.900	3.100	0.114	0.122
E	4.300	4.500	0.169	0.177
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
E1	6.250	6.550	0.246	0.258
A		1.100		0.043
A2	0.800	1.000	0.031	0.039
A1	0.020	0.150	0.001	0.006
e	0.65 (BSC)		0.026 (BSC)	
L	0.500	0.700	0.020	0.028
H	0.25 (TYP)		0.01 (TYP)	
θ	1°	7°	1°	7°



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