



Preliminary data

**SPI47N10L**  
**SPP47N10L,SPB47N10L**

## SIPMOS® Power-Transistor

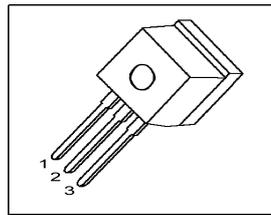
### Feature

- N-Channel
- Enhancement mode
- Logic Level
- 175°C operating temperature
- Avalanche rated
- dv/dt rated

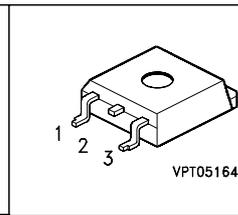
### Product Summary

$V_{DS}$	100	V
$R_{DS(on)}$	26	m $\Omega$
$I_D$	47	A

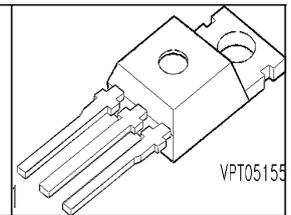
P-TO262-3-1



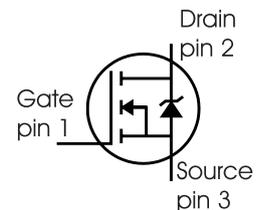
P-TO263-3-2



P-TO220-3-1



Type	Package	Ordering Code	Marking
SPP47N10L	P-TO220-3-1	Q67040-S4177	47N10L
SPB47N10L	P-TO263-3-2	Q67040-S4176	47N10L
SPI47N10L	P-TO262-3-1	tbd	47N10L


**Maximum Ratings**, at  $T_j = 25\text{ }^\circ\text{C}$ , unless otherwise specified

Parameter	Symbol	Value	Unit
Continuous drain current	$I_D$		A
$T_C=25\text{ }^\circ\text{C}$		47	
$T_C=100\text{ }^\circ\text{C}$		33	
Pulsed drain current	$I_D$ puls	188	
$T_C=25\text{ }^\circ\text{C}$			
Avalanche energy, single pulse	$E_{AS}$	400	mJ
$I_D=47\text{ A}$ , $V_{DD}=25\text{ V}$ , $R_{GS}=25\text{ }\Omega$			
Avalanche energy, periodic limited by $T_{jmax}$	$E_{AR}$	17.5	
Reverse diode dv/dt	dv/dt	6	kV/ $\mu\text{s}$
$I_S=47\text{ A}$ , $V_{DS}=0\text{ V}$ , $di/dt=200\text{ A}/\mu\text{s}$			
Gate source voltage	$V_{GS}$	$\pm 20$	V
Power dissipation	$P_{tot}$	175	W
$T_C=25\text{ }^\circ\text{C}$			
Operating and storage temperature	$T_j$ , $T_{stg}$	-55... +175	$^\circ\text{C}$
IEC climatic category; DIN IEC 68-1		55/175/56	



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SPP47N10L, SPB47N10L**Thermal Characteristics**

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
<b>Characteristics</b>					
Thermal resistance, junction - case	$R_{thJC}$	-	-	0.85	K/W
Thermal resistance, junction - ambient, leaded	$R_{thJA}$	-	-	62	
SMD version, device on PCB:	$R_{thJA}$				
@ min. footprint		-	-	62	
@ 6 cm <sup>2</sup> cooling area <sup>1)</sup>		-	-	40	

**Electrical Characteristics**, at  $T_j = 25^\circ\text{C}$ , unless otherwise specified

Parameter	Symbol	Values			Unit
		min.	typ.	max.	
<b>Static Characteristics</b>					
Drain-source breakdown voltage $V_{GS}=0V, I_D=2mA$	$V_{(BR)DSS}$	100	-	-	V
Gate threshold voltage, $V_{GS} = V_{DS}$ $I_D = 2 mA$	$V_{GS(th)}$	1.2	1.6	2	
Zero gate voltage drain current $V_{DS}=100V, V_{GS}=0V, T_j=25^\circ\text{C}$ $V_{DS}=100V, V_{GS}=0V, T_j=150^\circ\text{C}$	$I_{DSS}$	-	0.1	1	$\mu\text{A}$
Gate-source leakage current $V_{GS}=20V, V_{DS}=0V$	$I_{GSS}$	-	10	100	
Drain-source on-state resistance $V_{GS}=4.5V, I_D=33A$	$R_{DS(on)}$	-	25	40	m $\Omega$
Drain-source on-state resistance $V_{GS}=10V, I_D=33A$	$R_{DS(on)}$	-	18	26	

<sup>1</sup>Device on 40mm\*40mm\*1.5mm epoxy PCB FR4 with 6cm<sup>2</sup> (one layer, 70  $\mu\text{m}$  thick) copper area for drain connection. PCB is vertical without blown air.



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SPI47N10L  
SPP47N10L, SPB47N10LElectrical Characteristics, at  $T_j = 25^\circ\text{C}$ , unless otherwise specified

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

## Dynamic Characteristics

Transconductance	$g_{fs}$	$V_{DS} \geq 2 \cdot I_D \cdot R_{DS(on)max}$ , $I_D = 33\text{A}$	18	36	-	S
Input capacitance	$C_{iss}$	$V_{GS} = 0\text{V}$ , $V_{DS} = 25\text{V}$ , $f = 1\text{MHz}$	-	2000	2500	pF
Output capacitance	$C_{oss}$		-	375	470	
Reverse transfer capacitance	$C_{rss}$		-	210	265	
Turn-on delay time	$t_{d(on)}$	$V_{DD} = 50\text{V}$ , $V_{GS} = 4.5\text{V}$ , $I_D = 47\text{A}$ , $R_G = 2\Omega$	-	50	75	ns
Rise time	$t_r$		-	100	150	
Turn-off delay time	$t_{d(off)}$		-	50	75	
Fall time	$t_f$		-	70	105	

## Gate Charge Characteristics

Gate to source charge	$Q_{gs}$	$V_{DD} = 80\text{V}$ , $I_D = 47\text{A}$	-	8	12	nC
Gate to drain charge	$Q_{gd}$		-	16	24	
Gate charge total	$Q_g$	$V_{DD} = 80\text{V}$ , $I_D = 47\text{A}$ , $V_{GS} = 0$ to $10\text{V}$	-	90	135	
Gate plateau voltage	$V_{(plateau)}$	$V_{DD} = 80\text{V}$ , $I_D = 47\text{A}$	-	3.38	-	V

## Reverse Diode

Inverse diode continuous forward current	$I_S$	$T_C = 25^\circ\text{C}$	-	-	47	A
Inverse diode direct current, pulsed	$I_{SM}$		-	-	188	
Inverse diode forward voltage	$V_{SD}$	$V_{GS} = 0\text{V}$ , $I_F = 94\text{A}$	-	1.1	1.5	V
Reverse recovery time	$t_{rr}$	$V_R = 50\text{V}$ , $f = 5$ , $di_F/dt = 100\text{A}/\mu\text{s}$	-	80	120	ns
Reverse recovery charge	$Q_{rr}$		-	340	510	

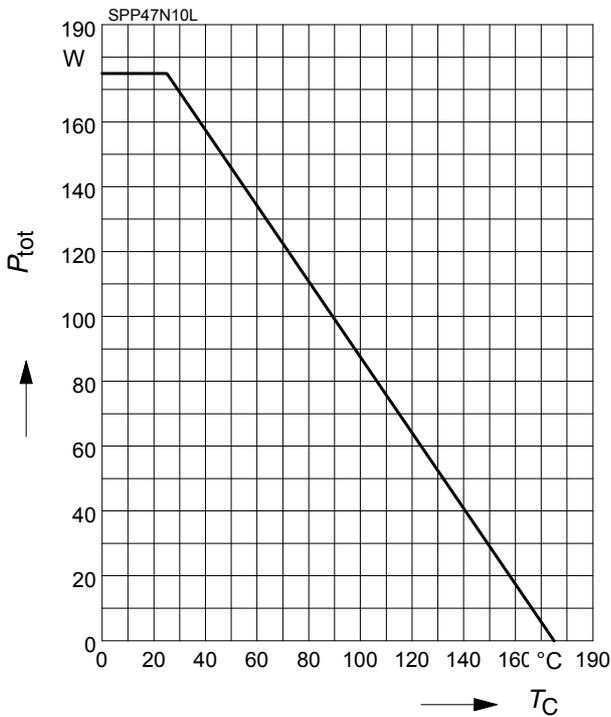


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1 Power dissipation

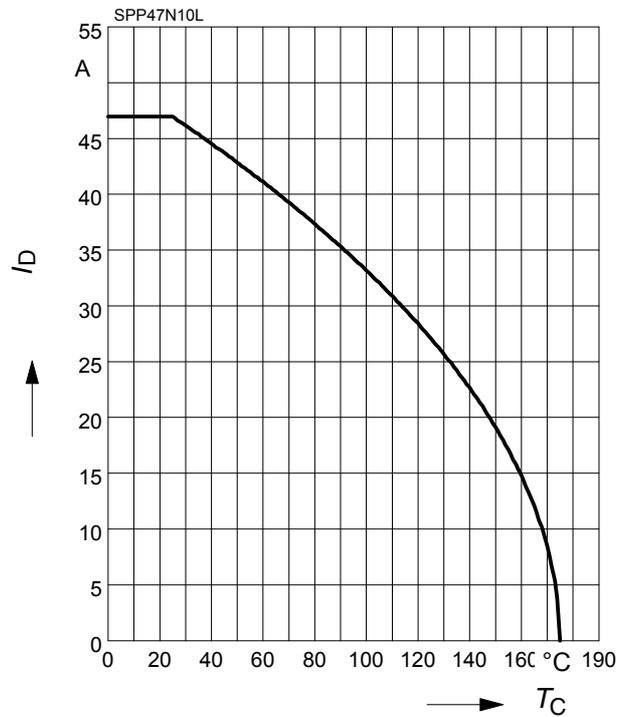
$P_{tot} = f(T_C)$



2 Drain current

$I_D = f(T_C)$

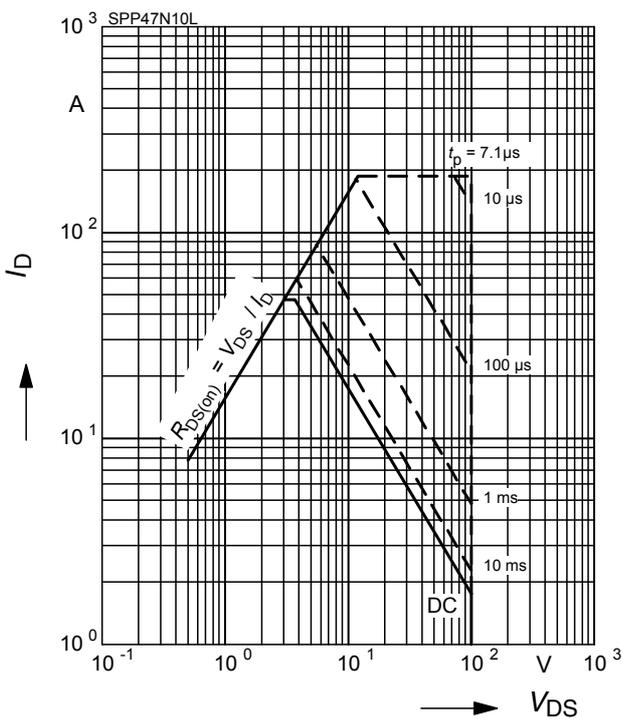
parameter:  $V_{GS} \geq 10\text{ V}$



3 Safe operating area

$I_D = f(V_{DS})$

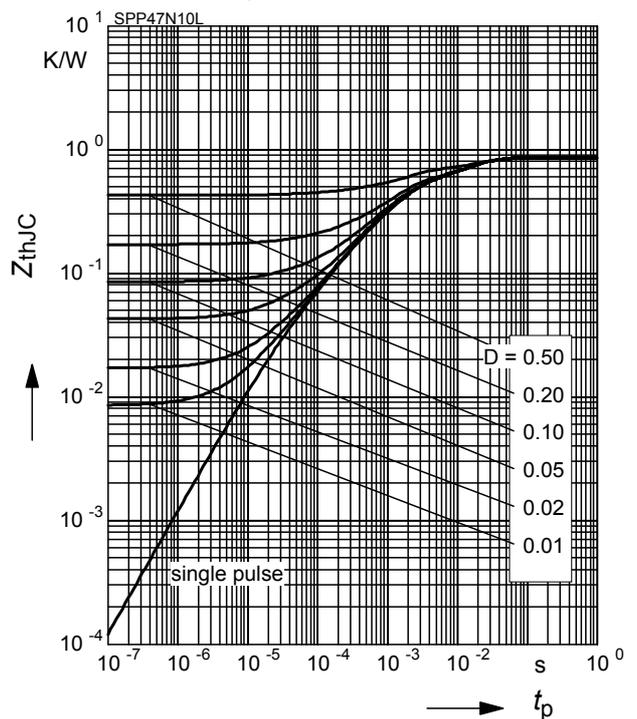
parameter:  $D = 0, T_C = 25\text{ °C}$



4 Transient thermal impedance

$Z_{thJC} = f(t_p)$

parameter:  $D = t_p/T$

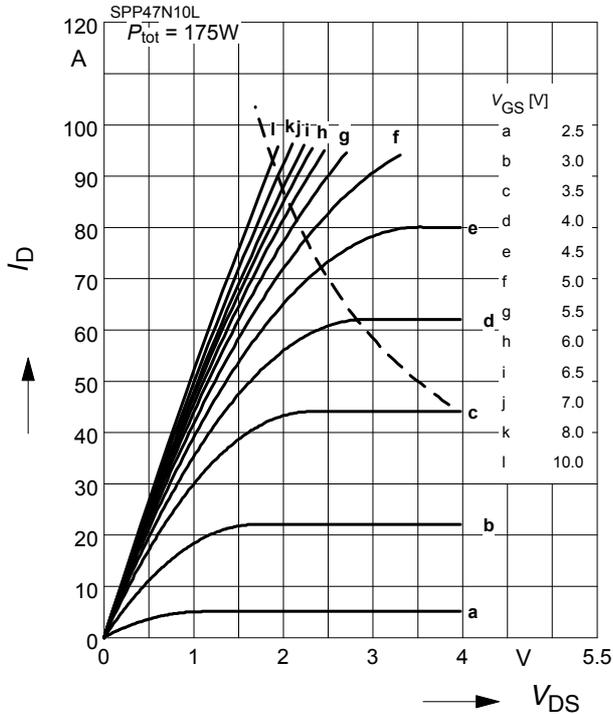




**5 Typ. output characteristic**

$I_D = f(V_{DS}); T_j = 25^\circ\text{C}$

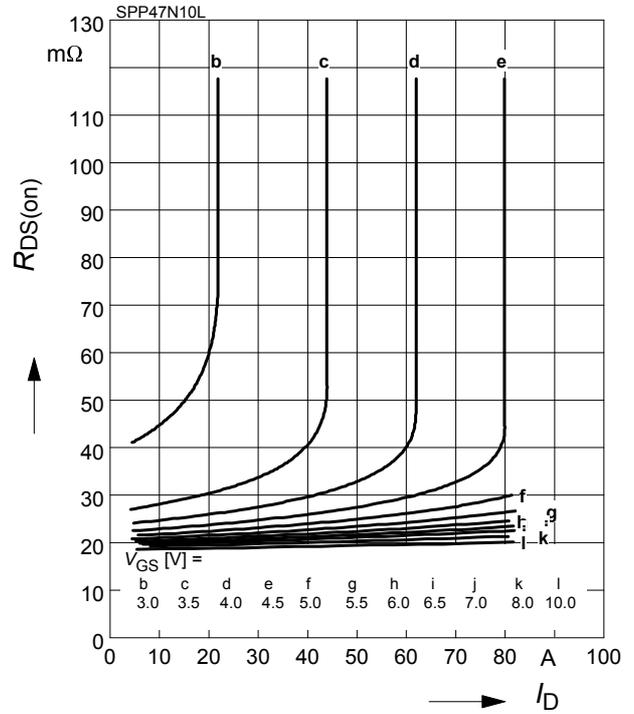
parameter:  $t_p = 80 \mu\text{s}$



**6 Typ. drain-source on resistance**

$R_{DS(on)} = f(I_D)$

parameter:  $V_{GS}$

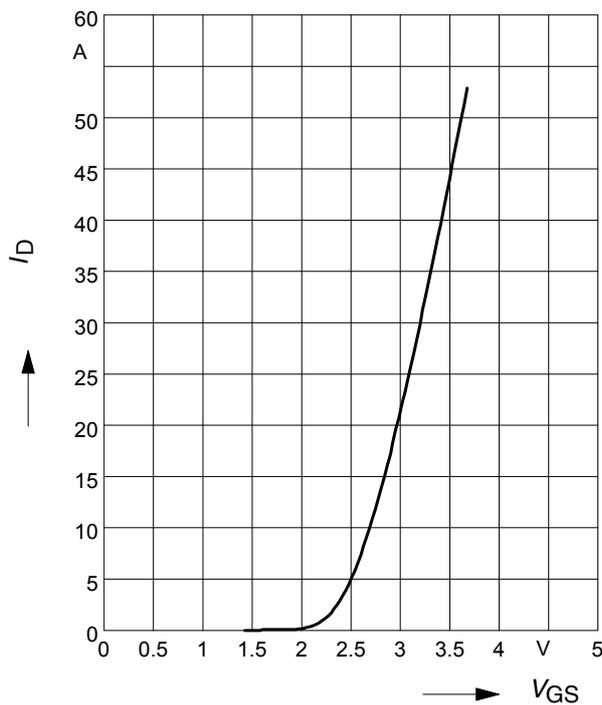


**7 Typ. transfer characteristics**

$I_D = f(V_{GS}); V_{DS} \geq 2 \times I_D \times R_{DS(on)max}$

parameter:  $t_p = 80 \mu\text{s}$

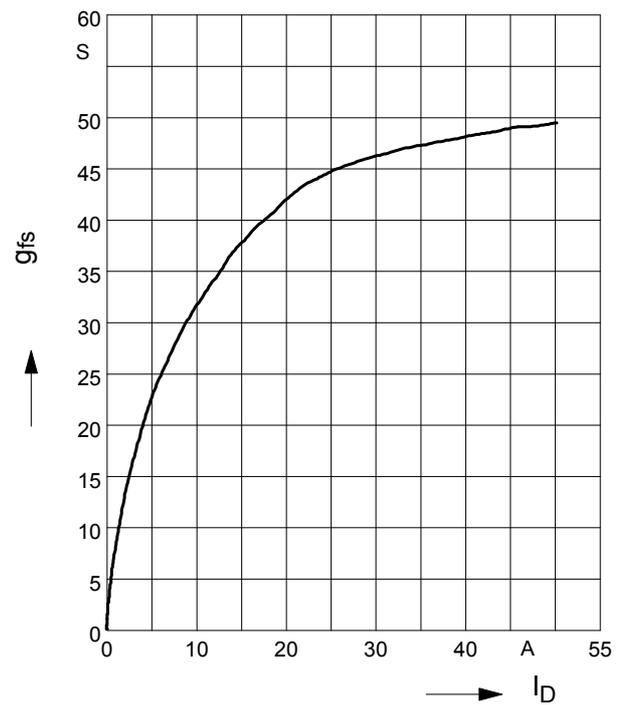
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**8 Typ. forward transconductance**

$g_{fs} = f(I_D); T_j = 25^\circ\text{C}$

parameter:  $g_{fs}$

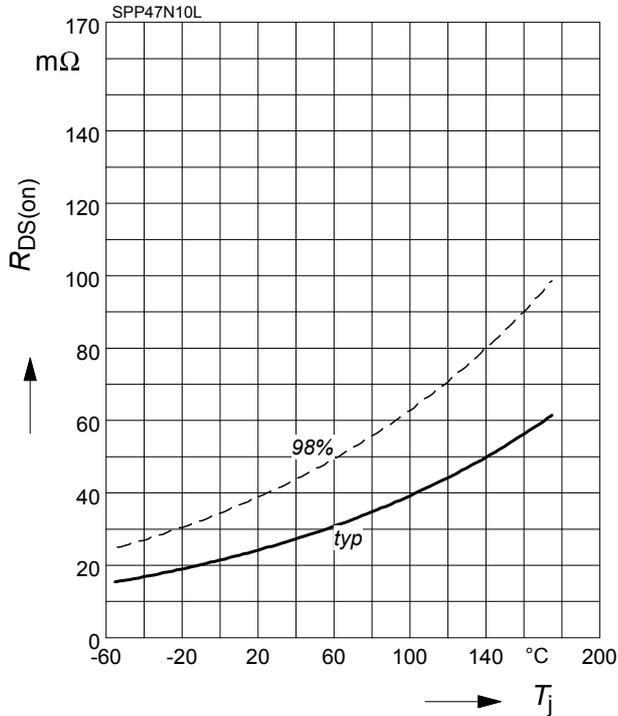




**9 Drain-source on-state resistance**

$R_{DS(on)} = f(T_j)$

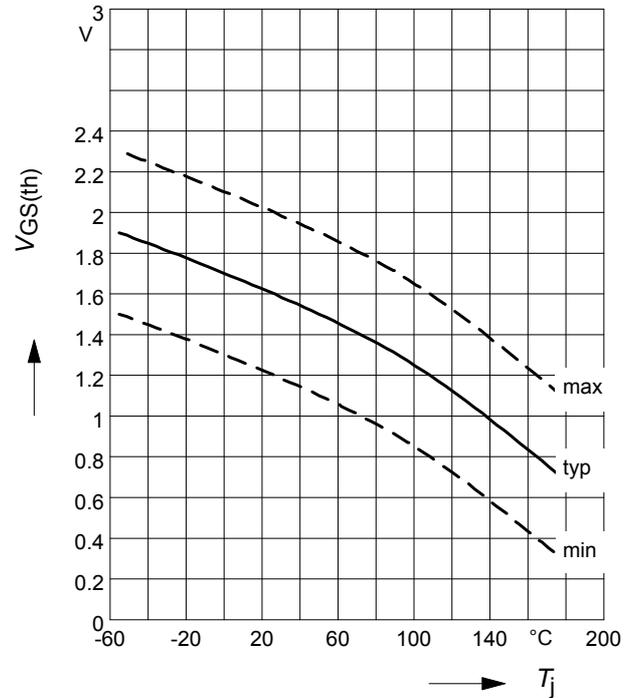
parameter :  $I_D = 33\text{ A}$ ,  $V_{GS} = 4.5\text{ V}$



**10 Gate threshold voltage**

$V_{GS(th)} = f(T_j)$

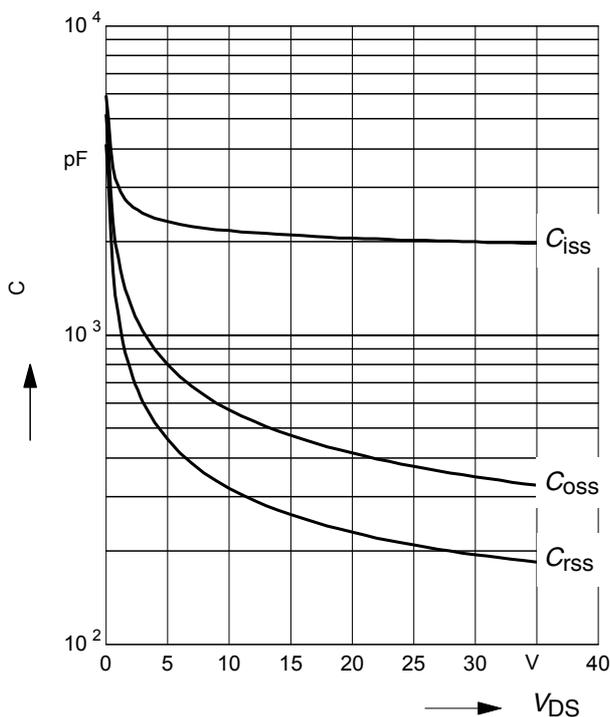
parameter:  $V_{GS} = V_{DS}$ ,  $I_D = 2\text{ mA}$



**11 Typ. capacitances**

$C = f(V_{DS})$

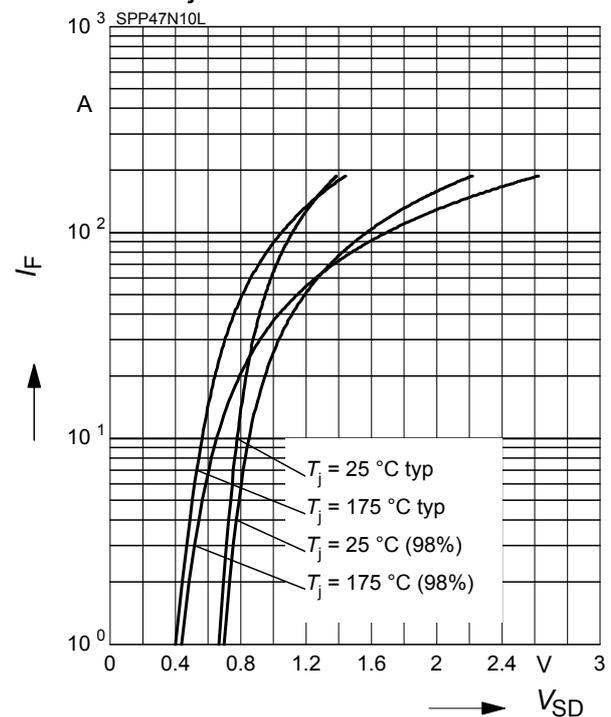
parameter:  $V_{GS}=0\text{V}$ ,  $f=1\text{ MHz}$



**12 Forward character. of reverse diode**

$I_F = f(V_{SD})$

parameter:  $T_j$ ,  $t_p = 80\text{ }\mu\text{s}$

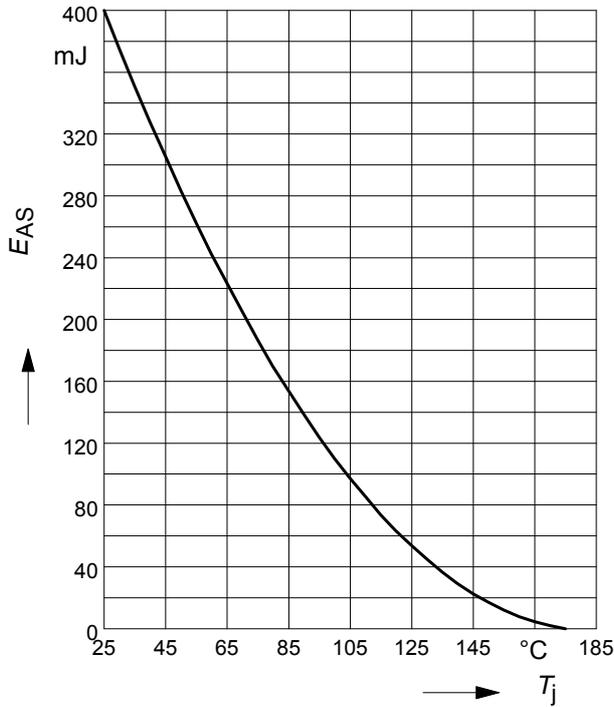




**13 Typ. avalanche energy**

$$E_{AS} = f(T_j)$$

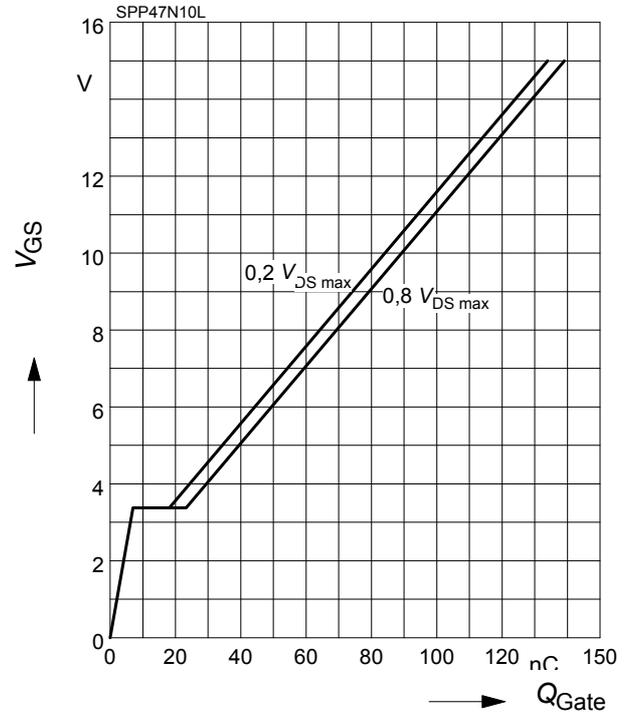
par.:  $I_D = 47\text{ A}$  ,  $V_{DD} = 25\text{ V}$  ,  $R_{GS} = 25\ \Omega$



**14 Typ. gate charge**

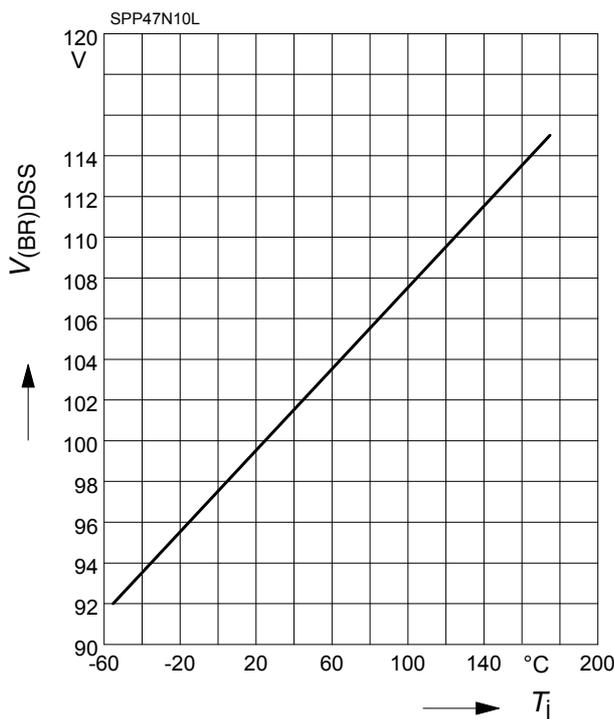
$$V_{GS} = f(Q_{Gate})$$

parameter:  $I_D = 47\text{ A}$  pulsed



**15 Drain-source breakdown voltage**

$$V_{(BR)DSS} = f(T_j)$$





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SPP47N10L, SPB47N10L

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**Published by**  
**Infineon Technologies AG,**  
**Bereichs Kommunikation**  
**St.-Martin-Strasse 53,**  
**D-81541 München**  
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### **Further information**

Please notice that the part number is BSPP47N10L, BSPB47N10L and BSPI47N10L, for simplicity the device is referred to by the term SPP47N10L, SPB47N10L and SPI47N10L throughout this documentation