SSD1770

Advance Information

LCD Segment / Common COLOR Driver with Controller
CMOS

1   General Description

SSD1770 is a single-chip CMOS color STN LCD driver with controller for dot-matrix graphic liquid crystal display system. SSD1770 consists of 393 high voltage driving output pins for driving maximum 104 RGB Segments, 80 Commons and 1 icon-driving Common.

SSD1770 consists of 312 (104 RGB) x 81 x 4 bits Graphic Display Data RAM (GDDRAM). Data/Commands are sent from common MCU through 8-bit 6800-series / 8080-series compatible Parallel Interface or 3-wires / 4-wires Serial Peripheral Interface by pins selection.

SSD1770 embeds DC-DC Converter, On-Chip Oscillator and Bias Divider so as to reduce the number of external components. With the advanced design, low power consumption, stable LCD operating voltage and flexible die package layout, SSD1770 is suitable for any portable battery-driven applications requiring long operation period with compact size.

2   FEATURES

- Power Supply: V_{DD} = 2.4 V – 3.6V
  - V_{DDIO} = 2.4 V – 3.6V
  - V_{CI} = 2.4 V – 3.6V
- LCD Driving Output Voltage: 12.5V
- Low Current Sleep Mode
- Maximum display size: 104 RGB columns by 80 rows with one Icon line
- Color display support: 256 colors or 4096 colors graphical display
- 256-colors Position Control and simultaneous RGB display control
- 8-bit 6800-series / 8080-series Parallel Interface, 3-wires / 4-wires Serial Peripheral Interface
- On-Chip 312 (104 RGB) X (81) x 4 = 101088 bits Graphic Display Data RAM
- Programmable partial display function
- Column Re-mapping and RAM Page scan direction control
- Software selection on Center Screen Scrolling, Top Screen Scrolling, Bottom Screen Scrolling and Whole Screen Scrolling
- On-Chip Voltage Generator or External LCD Driving Power Supply Selectable
- 3X/ 4X / 5X / 6X On-Chip DC-DC Converter with internal flying capacitor
- 64 Levels Internal Contrast Control
- Programmable LCD Driving Voltage Temperature Compensation Coefficients
- On-Chip Bias Divider with internal flying capacitor (expect V_{OUT})
- Programmable drive duty ratio: 1 /8 to 1 /81
- On-Chip Oscillator
- 2-D Graphic Acceleration Engine
- Non-Volatile Memory (OTP) for calibration

3   ORDERING INFORMATION

Ordering Part Number	SEG	COM	Display Colors	Package Form	Reference
SSD1770Z	104	81	4096 or 256 colors	Gold Bump Die	Figure 2 on page 4

Table 1 – Ordering Information

4 BLOCK DIAGRAM

Figure 1 – SSD1770 Block Diagram

5   DIE PAD FLOOR PLAN

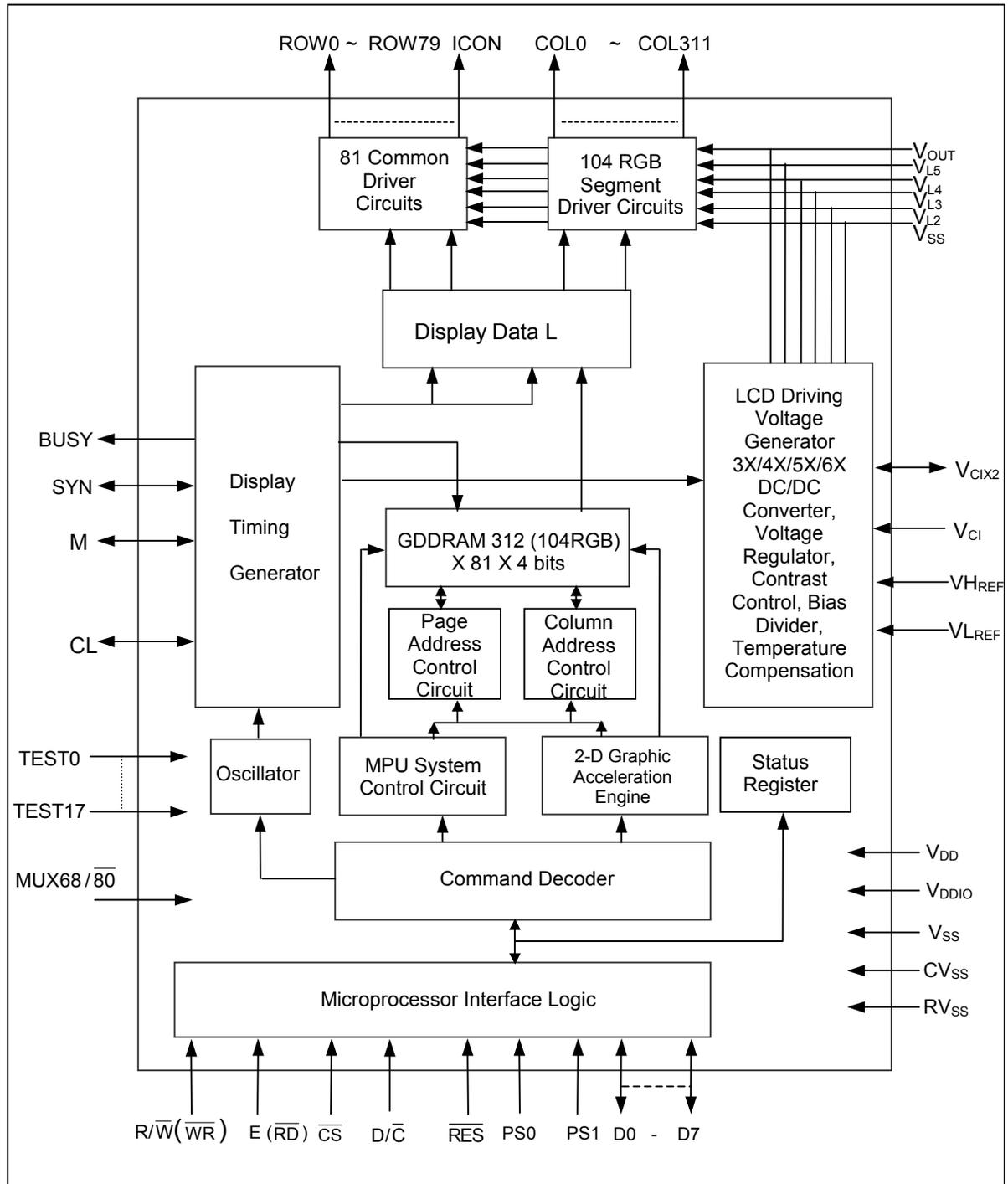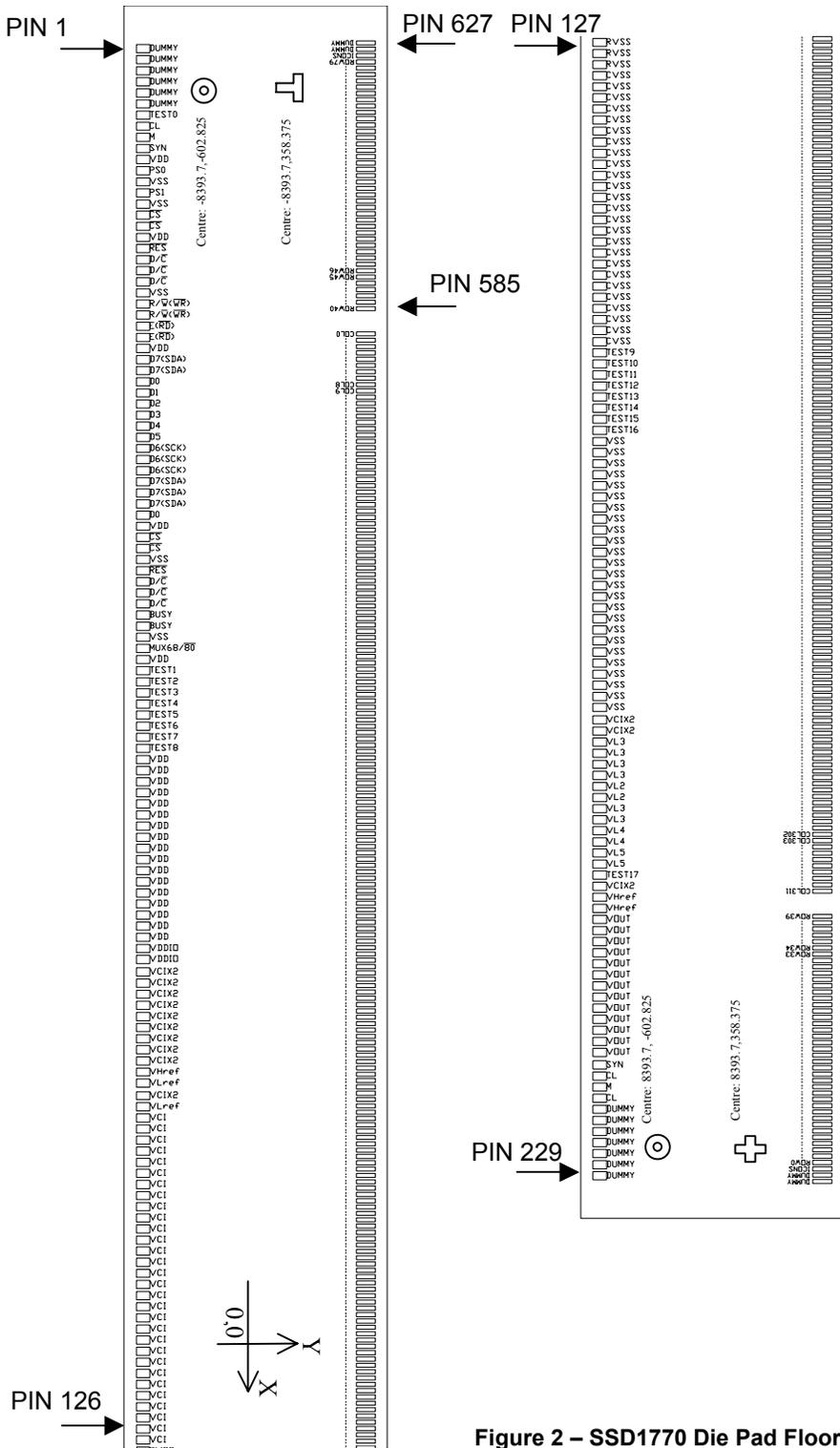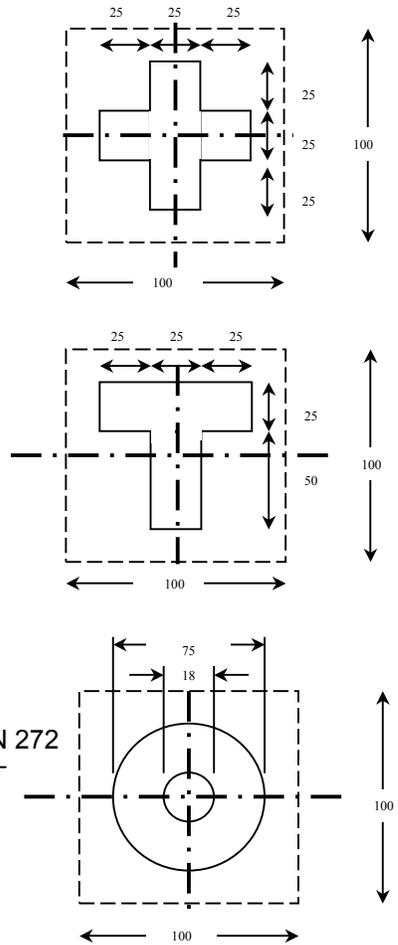**Figure 2 – SSD1770 Die Pad Floor Plan**

Note:
1. Diagram showing the die face up.
2. Coordinates are reference to center of the chip.
3. Unit of coordinates and Size of all alignment marks are in um.
4. All alignment keys do not contain gold bump.

Die size: 17.74 mm x 1.88 mm
Die Thickness: 457 ± 25µm
Bump Height: typical 15µm
Bump co-planarity <3µm (within die)

Table 2 – SSD1770 Series Bump Die Pad Coordinates (Bump center)

Pad #	Signal	X-pos	Y-pos	Pad #	Signal	X-pos	Y-pos	Pad #	Signal	X-pos	Y-pos
1	DUMMY	-8706.0	-769.7	51	$D/\overline{C}$	-4896.0	-769.7	101	V_{CI}	-1066.6	-769.7
2	DUMMY	-8629.8	-769.7	52	BUSY	-4819.8	-769.7	102	V_{CI}	-990.4	-769.7
3	DUMMY	-8553.6	-769.7	53	BUSY	-4743.6	-769.7	103	V_{CI}	-914.2	-769.7
4	DUMMY	-8477.4	-769.7	54	V_{SS}	-4667.4	-769.7	104	V_{CI}	-838.0	-769.7
5	DUMMY	-8401.2	-769.7	55	$MUX68/\overline{80}$	-4591.2	-769.7	105	V_{CI}	-761.8	-769.7
6	DUMMY	-8325.0	-769.7	56	V_{DD}	-4515.0	-769.7	106	V_{CI}	-685.6	-769.7
7	TEST0	-8248.8	-769.7	57	TEST1	-4438.8	-769.7	107	V_{CI}	-609.4	-769.7
8	CL	-8172.6	-769.7	58	TEST2	-4362.6	-769.7	108	V_{CI}	-533.2	-769.7
9	M	-8096.4	-769.7	59	TEST3	-4286.4	-769.7	109	V_{CI}	-457.0	-769.7
10	SYN	-8020.2	-769.7	60	TEST4	-4210.2	-769.7	110	V_{CI}	-380.8	-769.7
11	V_{DD}	-7944.0	-769.7	61	TEST5	-4134.0	-769.7	111	V_{CI}	-304.6	-769.7
12	PS0	-7867.8	-769.7	62	TEST6	-4057.8	-769.7	112	V_{CI}	-228.4	-769.7
13	V_{SS}	-7791.6	-769.7	63	TEST7	-3981.6	-769.7	113	V_{CI}	-152.2	-769.7
14	PS1	-7715.4	-769.7	64	TEST8	-3905.4	-769.7	114	V_{CI}	-76.0	-769.7
15	V_{SS}	-7639.2	-769.7	65	V_{DD}	-3829.2	-769.7	115	V_{CI}	0.2	-769.7
16	$\overline{CS}$	-7563.0	-769.7	66	V_{DD}	-3753.0	-769.7	116	V_{CI}	76.4	-769.7
17	$\overline{CS}$	-7486.8	-769.7	67	V_{DD}	-3676.8	-769.7	117	V_{CI}	152.6	-769.7
18	V_{DD}	-7410.6	-769.7	68	V_{DD}	-3600.6	-769.7	118	V_{CI}	228.8	-769.7
19	$\overline{RES}$	-7334.4	-769.7	69	V_{DD}	-3524.4	-769.7	119	V_{CI}	305.0	-769.7
20	$D/\overline{C}$	-7258.2	-769.7	70	V_{DD}	-3448.2	-769.7	120	V_{CI}	381.2	-769.7
21	$D/\overline{C}$	-7182.0	-769.7	71	V_{DD}	-3372.0	-769.7	121	V_{CI}	457.4	-769.7
22	$D/\overline{C}$	-7105.8	-769.7	72	V_{DD}	-3295.8	-769.7	122	V_{CI}	533.6	-769.7
23	V_{SS}	-7029.6	-769.7	73	V_{DD}	-3219.6	-769.7	123	V_{CI}	609.8	-769.7
24	$R/\overline{W}\ (\overline{WR})$	-6953.4	-769.7	74	V_{DD}	-3143.4	-769.7	124	V_{CI}	686.0	-769.7
25	$R/\overline{W}\ (\overline{WR})$	-6877.2	-769.7	75	V_{DD}	-3067.2	-769.7	125	V_{CI}	762.2	-769.7
26	$E(\overline{RD})$	-6801.0	-769.7	76	V_{DD}	-2991.0	-769.7	126	V_{CI}	838.4	-769.7
27	$E(\overline{RD})$	-6724.8	-769.7	77	V_{DD}	-2914.8	-769.7	127	RV_{SS}	914.6	-769.7
28	V_{DD}	-6648.6	-769.7	78	V_{DD}	-2838.6	-769.7	128	RV_{SS}	990.8	-769.7
29	D7 (SDA)	-6572.4	-769.7	79	V_{DD}	-2762.4	-769.7	129	RV_{SS}	1067.0	-769.7
30	D7 (SDA)	-6496.2	-769.7	80	V_{DD}	-2686.2	-769.7	130	CV_{SS}	1143.2	-769.7
31	D0	-6420.0	-769.7	81	V_{DD}	-2610.0	-769.7	131	CV_{SS}	1219.4	-769.7
32	D1	-6343.8	-769.7	82	V_{DDIO}	-2533.8	-769.7	132	CV_{SS}	1295.6	-769.7
33	D2	-6267.6	-769.7	83	V_{DDIO}	-2457.6	-769.7	133	CV_{SS}	1371.8	-769.7
34	D3	-6191.4	-769.7	84	V_{CIX2}	-2371.7	-769.7	134	CV_{SS}	1448.0	-769.7
35	D4	-6115.2	-769.7	85	V_{CIX2}	-2295.5	-769.7	135	CV_{SS}	1524.2	-769.7
36	D5	-6039.0	-769.7	86	V_{CIX2}	-2219.3	-769.7	136	CV_{SS}	1600.4	-769.7
37	D6 (SCK)	-5962.8	-769.7	87	V_{CIX2}	-2143.1	-769.7	137	CV_{SS}	1676.6	-769.7
38	D6 (SCK)	-5886.6	-769.7	88	V_{CIX2}	-2066.9	-769.7	138	CV_{SS}	1752.8	-769.7
39	D6 (SCK)	-5810.4	-769.7	89	V_{CIX2}	-1990.7	-769.7	139	CV_{SS}	1829.0	-769.7
40	D7 (SDA)	-5734.2	-769.7	90	V_{CIX2}	-1914.5	-769.7	140	CV_{SS}	1905.2	-769.7
41	D7 (SDA)	-5658.0	-769.7	91	V_{CIX2}	-1838.3	-769.7	141	CV_{SS}	1981.4	-769.7
42	D7 (SDA)	-5581.8	-769.7	92	V_{CIX2}	-1762.1	-769.7	142	CV_{SS}	2057.6	-769.7
43	D0	-5505.6	-769.7	93	VH_{REF}	-1685.9	-769.7	143	CV_{SS}	2133.8	-769.7
44	V_{DD}	-5429.4	-769.7	94	VL_{REF}	-1609.7	-769.7	144	CV_{SS}	2210.0	-769.7
45	$\overline{CS}$	-5353.2	-769.7	95	V_{CIX2}	-1523.8	-769.7	145	CV_{SS}	2286.2	-769.7
46	$\overline{CS}$	-5277.0	-769.7	96	VL_{REF}	-1447.6	-769.7	146	CV_{SS}	2362.4	-769.7
47	V_{SS}	-5200.8	-769.7	97	V_{CI}	-1371.4	-769.7	147	CV_{SS}	2438.6	-769.7
48	$\overline{RES}$	-5124.6	-769.7	98	V_{CI}	-1295.2	-769.7	148	CV_{SS}	2514.8	-769.7
49	$D/\overline{C}$	-5048.4	-769.7	99	V_{CI}	-1219.0	-769.7	149	CV_{SS}	2591.0	-769.7
50	$D/\overline{C}$	-4972.2	-769.7	100	V_{CI}	-1142.8	-769.7	150	CV_{SS}	2667.2	-769.7

Pad #	Signal	X-pos	Y-pos	Pad #	Signal	X-pos	Y-pos
151	CV_{SS}	2743.4	-769.7	201	V_{L5}	6563.1	-769.7
152	CV_{SS}	2819.6	-769.7	202	TEST17	6639.3	-769.7
153	CV_{SS}	2895.8	-769.7	203	V_{CIX2}	6715.5	-769.7
154	CV_{SS}	2972.0	-769.7	204	VH_{REF}	6791.7	-769.7
155	TEST9	3048.2	-769.7	205	VH_{REF}	6867.9	-769.7
156	TEST10	3124.4	-769.7	206	V_{OUT}	6944.1	-769.7
157	TEST11	3200.6	-769.7	207	V_{OUT}	7020.3	-769.7
158	TEST12	3276.8	-769.7	208	V_{OUT}	7096.5	-769.7
159	TEST13	3353.0	-769.7	209	V_{OUT}	7172.7	-769.7
160	TEST14	3429.2	-769.7	210	V_{OUT}	7248.9	-769.7
161	TEST15	3505.4	-769.7	211	V_{OUT}	7325.1	-769.7
162	TEST16	3581.6	-769.7	212	V_{OUT}	7401.3	-769.7
163	V_{SS}	3657.8	-769.7	213	V_{OUT}	7477.5	-769.7
164	V_{SS}	3734.0	-769.7	214	V_{OUT}	7553.7	-769.7
165	V_{SS}	3810.2	-769.7	215	V_{OUT}	7629.9	-769.7
166	V_{SS}	3886.4	-769.7	216	V_{OUT}	7706.1	-769.7
167	V_{SS}	3962.6	-769.7	217	V_{OUT}	7782.3	-769.7
168	V_{SS}	4038.8	-769.7	218	V_{OUT}	7858.5	-769.7
169	V_{SS}	4115.0	-769.7	219	SYN	7944.4	-769.7
170	V_{SS}	4191.2	-769.7	220	CL	8020.6	-769.7
171	V_{SS}	4267.4	-769.7	221	M	8096.8	-769.7
172	V_{SS}	4343.6	-769.7	222	CL	8173.0	-769.7
173	V_{SS}	4419.8	-769.7	223	DUMMY	8249.2	-769.7
174	V_{SS}	4496.0	-769.7	224	DUMMY	8325.4	-769.7
175	V_{SS}	4572.2	-769.7	225	DUMMY	8401.6	-769.7
176	V_{SS}	4648.4	-769.7	226	DUMMY	8477.8	-769.7
177	V_{SS}	4724.6	-769.7	227	DUMMY	8554.0	-769.7
178	V_{SS}	4800.8	-769.7	228	DUMMY	8630.2	-769.7
179	V_{SS}	4877.0	-769.7	229	DUMMY	8706.4	-769.7
180	V_{SS}	4953.2	-769.7				
181	V_{SS}	5029.4	-769.7				
182	V_{SS}	5105.6	-769.7				
183	V_{SS}	5181.8	-769.7				
184	V_{SS}	5258.0	-769.7				
185	V_{SS}	5334.2	-769.7				
186	V_{SS}	5410.4	-769.7				
187	V_{SS}	5486.6	-769.7				
188	V_{CIX2}	5572.5	-769.7				
189	V_{CIX2}	5648.7	-769.7				
190	V_{L3}	5724.9	-769.7				
191	V_{L3}	5801.1	-769.7				
192	V_{L3}	5877.3	-769.7				
193	V_{L3}	5953.5	-769.7				
194	V_{L2}	6029.7	-769.7				
195	V_{L2}	6105.9	-769.7				
196	V_{L3}	6182.1	-769.7				
197	V_{L3}	6258.3	-769.7				
198	V_{L4}	6334.5	-769.7				
199	V_{L4}	6410.7	-769.7				
200	V_{L5}	6486.9	-769.7				

Pad #	Pad Name	Signal (MUX68/$\overline{80}$ =V_{DD}) – 68mux	Signal (MUX68/$\overline{80}$ =V_{SS})–80 mux	X-pos	Y-pos
230	DUMMY	DUMMY	DUMMY	8745.1	754.3
231	DUMMY	DUMMY	DUMMY	8701.7	754.3
232	ICONS	ICONS	ICONS	8658.3	754.3
233	ROW0	COM0	COM0	8614.9	754.3
234	ROW1	COM1	COM1	8571.5	754.3
235	ROW2	COM2	COM2	8528.1	754.3
236	ROW3	COM3	COM3	8484.7	754.3
237	ROW4	COM4	COM4	8441.3	754.3
238	ROW5	COM5	COM5	8397.9	754.3
239	ROW6	COM6	COM6	8354.5	754.3
240	ROW7	COM7	COM7	8311.1	754.3
241	ROW8	COM8	COM8	8267.7	754.3
242	ROW9	COM9	COM9	8224.3	754.3
243	ROW10	COM10	COM10	8180.9	754.3
244	ROW11	COM11	COM11	8137.5	754.3
245	ROW12	COM12	COM12	8094.1	754.3
246	ROW13	COM13	COM13	8050.7	754.3
247	ROW14	COM14	COM14	8007.3	754.3
248	ROW15	COM15	COM15	7963.9	754.3
249	ROW16	COM16	COM16	7920.5	754.3
250	ROW17	COM17	COM17	7877.1	754.3
251	ROW18	COM18	COM18	7833.7	754.3
252	ROW19	COM19	COM19	7790.3	754.3
253	ROW20	COM20	COM20	7746.9	754.3
254	ROW21	COM21	COM21	7703.5	754.3
255	ROW22	COM22	COM22	7660.1	754.3
256	ROW23	COM23	COM23	7616.7	754.3
257	ROW24	COM24	COM24	7573.3	754.3
258	ROW25	COM25	COM25	7529.9	754.3
259	ROW26	COM26	COM26	7486.5	754.3
260	ROW27	COM27	COM27	7443.1	754.3
261	ROW28	COM28	COM28	7399.7	754.3
262	ROW29	COM29	COM29	7356.3	754.3
263	ROW30	COM30	COM30	7312.9	754.3
264	ROW31	COM31	COM31	7269.5	754.3
265	ROW32	COM32	COM32	7226.1	754.3
266	ROW33	COM33	COM33	7182.7	754.3
267	ROW34	Non select signal	COM34	7139.3	754.3
268	ROW35	Non select signal	COM35	7095.9	754.3
269	ROW36	Non select signal	COM36	7052.5	754.3
270	ROW37	Non select signal	COM37	7009.1	754.3
271	ROW38	Non select signal	COM38	6965.7	754.3
272	ROW39	Non select signal	COM39	6922.3	754.3

Pad #	Pad Name	Signal	Color	X-pos	Y-pos
273	COL311	SEG103	B	6748.7	754.3
274	COL310	SEG103	G	6705.3	754.3
275	COL309	SEG103	R	6661.9	754.3
276	COL308	SEG102	B	6618.5	754.3
277	COL307	SEG102	G	6575.1	754.3
278	COL306	SEG102	R	6531.7	754.3
279	COL305	SEG101	B	6488.3	754.3
280	COL304	SEG101	G	6444.9	754.3
281	COL303	SEG101	R	6401.5	754.3
282	COL302	SEG100	B	6358.1	754.3
283	COL301	SEG100	G	6314.7	754.3
284	COL300	SEG100	R	6271.3	754.3
285	COL299	SEG99	B	6227.9	754.3
286	COL298	SEG99	G	6184.5	754.3
287	COL297	SEG99	R	6141.1	754.3
288	COL296	SEG98	B	6097.7	754.3
289	COL295	SEG98	G	6054.3	754.3
290	COL294	SEG98	R	6010.9	754.3
291	COL293	SEG97	B	5967.5	754.3
292	COL292	SEG97	G	5924.1	754.3
293	COL291	SEG97	R	5880.7	754.3
294	COL290	SEG96	B	5837.3	754.3
295	COL289	SEG96	G	5793.9	754.3
296	COL288	SEG96	R	5750.5	754.3
297	COL287	SEG95	B	5707.1	754.3
298	COL286	SEG95	G	5663.7	754.3
299	COL285	SEG95	R	5620.3	754.3
300	COL284	SEG94	B	5576.9	754.3
301	COL283	SEG94	G	5533.5	754.3
302	COL282	SEG94	R	5490.1	754.3
303	COL281	SEG93	B	5446.7	754.3
304	COL280	SEG93	G	5403.3	754.3
305	COL279	SEG93	R	5359.9	754.3
306	COL278	SEG92	B	5316.5	754.3
307	COL277	SEG92	G	5273.1	754.3
308	COL276	SEG92	R	5229.7	754.3
309	COL275	SEG91	B	5186.3	754.3
310	COL274	SEG91	G	5142.9	754.3
311	COL273	SEG91	R	5099.5	754.3
312	COL272	SEG90	B	5056.1	754.3
313	COL271	SEG90	G	5012.7	754.3
314	COL270	SEG90	R	4969.3	754.3
315	COL269	SEG89	B	4925.9	754.3
316	COL268	SEG89	G	4882.5	754.3
317	COL267	SEG89	R	4839.1	754.3
318	COL266	SEG88	B	4795.7	754.3
319	COL265	SEG88	G	4752.3	754.3
320	COL264	SEG88	R	4708.9	754.3

Pad #	Pad Name	Signal	Color	X-pos	Y-pos	Pad #	Pad Name	Signal	Color	X-pos	Y-pos
321	COL263	SEG87	B	4665.5	754.3	369	COL215	SEG71	B	2582.3	754.3
322	COL262		G	4622.1	754.3	370	COL214		G	2538.9	754.3
323	COL261		R	4578.7	754.3	371	COL213		R	2495.5	754.3
324	COL260	SEG86	B	4535.3	754.3	372	COL212	SEG70	B	2452.1	754.3
325	COL259		G	4491.9	754.3	373	COL211		G	2408.7	754.3
326	COL258		R	4448.5	754.3	374	COL210		R	2365.3	754.3
327	COL257	SEG85	B	4405.1	754.3	375	COL209	SEG69	B	2321.9	754.3
328	COL256		G	4361.7	754.3	376	COL208		G	2278.5	754.3
329	COL255		R	4318.3	754.3	377	COL207		R	2235.1	754.3
330	COL254	SEG84	B	4274.9	754.3	378	COL206	SEG68	B	2191.7	754.3
331	COL253		G	4231.5	754.3	379	COL205		G	2148.3	754.3
332	COL252		R	4188.1	754.3	380	COL204		R	2104.9	754.3
333	COL251	SEG83	B	4144.7	754.3	381	COL203	SEG67	B	2061.5	754.3
334	COL250		G	4101.3	754.3	382	COL202		G	2018.1	754.3
335	COL249		R	4057.9	754.3	383	COL201		R	1974.7	754.3
336	COL248	SEG82	B	4014.5	754.3	384	COL200	SEG66	B	1931.3	754.3
337	COL247		G	3971.1	754.3	385	COL199		G	1887.9	754.3
338	COL246		R	3927.7	754.3	386	COL198		R	1844.5	754.3
339	COL245	SEG81	B	3884.3	754.3	387	COL197	SEG65	B	1801.1	754.3
340	COL244		G	3840.9	754.3	388	COL196		G	1757.7	754.3
341	COL243		R	3797.5	754.3	389	COL195		R	1714.3	754.3
342	COL242	SEG80	B	3754.1	754.3	390	COL194	SEG64	B	1670.9	754.3
343	COL241		G	3710.7	754.3	391	COL193		G	1627.5	754.3
344	COL240		R	3667.3	754.3	392	COL192		R	1584.1	754.3
345	COL239	SEG79	B	3623.9	754.3	393	COL191	SEG63	B	1540.7	754.3
346	COL238		G	3580.5	754.3	394	COL190		G	1497.3	754.3
347	COL237		R	3537.1	754.3	395	COL189		R	1453.9	754.3
348	COL236	SEG78	B	3493.7	754.3	396	COL188	SEG62	B	1410.5	754.3
349	COL235		G	3450.3	754.3	397	COL187		G	1367.1	754.3
350	COL234		R	3406.9	754.3	398	COL186		R	1323.7	754.3
351	COL233	SEG77	B	3363.5	754.3	399	COL185	SEG61	B	1280.3	754.3
352	COL232		G	3320.1	754.3	400	COL184		G	1236.9	754.3
353	COL231		R	3276.7	754.3	401	COL183		R	1193.5	754.3
354	COL230	SEG76	B	3233.3	754.3	402	COL182	SEG60	B	1150.1	754.3
355	COL229		G	3189.9	754.3	403	COL181		G	1106.7	754.3
356	COL228		R	3146.5	754.3	404	COL180		R	1063.3	754.3
357	COL227	SEG75	B	3103.1	754.3	405	COL179	SEG59	B	1019.9	754.3
358	COL226		G	3059.7	754.3	406	COL178		G	976.5	754.3
359	COL225		R	3016.3	754.3	407	COL177		R	933.1	754.3
360	COL224	SEG74	B	2972.9	754.3	408	COL176	SEG58	B	889.7	754.3
361	COL223		G	2929.5	754.3	409	COL175		G	846.3	754.3
362	COL222		R	2886.1	754.3	410	COL174		R	802.9	754.3
363	COL221	SEG73	B	2842.7	754.3	411	COL173	SEG57	B	759.5	754.3
364	COL220		G	2799.3	754.3	412	COL172		G	716.1	754.3
365	COL219		R	2755.9	754.3	413	COL171		R	672.7	754.3
366	COL218	SEG72	B	2712.5	754.3	414	COL170	SEG56	B	629.3	754.3
367	COL217		G	2669.1	754.3	415	COL169		G	585.9	754.3
368	COL216		R	2625.7	754.3	416	COL168		R	542.5	754.3

Pad #	Pad Name	Signal	Color	X-pos	Y-pos	Pad #	Pad Name	Signal	Color	X-pos	Y-pos
417	COL167		B	499.1	754.3	465	COL119		B	-1584.1	754.3
418	COL166	SEG55	G	455.7	754.3	466	COL118	SEG39	G	-1627.5	754.3
419	COL165		R	412.3	754.3	467	COL117		R	-1670.9	754.3
420	COL164		B	368.9	754.3	468	COL116		B	-1714.3	754.3
421	COL163	SEG54	G	325.5	754.3	469	COL115	SEG38	G	-1757.7	754.3
422	COL162		R	282.1	754.3	470	COL114		R	-1801.1	754.3
423	COL161		B	238.7	754.3	471	COL113		B	-1844.5	754.3
424	COL160	SEG53	G	195.3	754.3	472	COL112	SEG37	G	-1887.9	754.3
425	COL159		R	151.9	754.3	473	COL111		R	-1931.3	754.3
426	COL158		B	108.5	754.3	474	COL110		B	-1974.7	754.3
427	COL157	SEG52	G	65.1	754.3	475	COL109	SEG36	G	-2018.1	754.3
428	COL156		R	21.7	754.3	476	COL108		R	-2061.5	754.3
429	COL155		B	-21.7	754.3	477	COL107		B	-2104.9	754.3
430	COL154	SEG51	G	-65.1	754.3	478	COL106	SEG35	G	-2148.3	754.3
431	COL153		R	-108.5	754.3	479	COL105		R	-2191.7	754.3
432	COL152		B	-151.9	754.3	480	COL104		B	-2235.1	754.3
433	COL151	SEG50	G	-195.3	754.3	481	COL103	SEG34	G	-2278.5	754.3
434	COL150		R	-238.7	754.3	482	COL102		R	-2321.9	754.3
435	COL149		B	-282.1	754.3	483	COL101		B	-2365.3	754.3
436	COL148	SEG49	G	-325.5	754.3	484	COL100	SEG33	G	-2408.7	754.3
437	COL147		R	-368.9	754.3	485	COL99		R	-2452.1	754.3
438	COL146		B	-412.3	754.3	486	COL98		B	-2495.5	754.3
439	COL145	SEG48	G	-455.7	754.3	487	COL97	SEG32	G	-2538.9	754.3
440	COL144		R	-499.1	754.3	488	COL96		R	-2582.3	754.3
441	COL143		B	-542.5	754.3	489	COL95		B	-2625.7	754.3
442	COL142	SEG47	G	-585.9	754.3	490	COL94	SEG31	G	-2669.1	754.3
443	COL141		R	-629.3	754.3	491	COL93		R	-2712.5	754.3
444	COL140		B	-672.7	754.3	492	COL92		B	-2755.9	754.3
445	COL139	SEG46	G	-716.1	754.3	493	COL91	SEG30	G	-2799.3	754.3
446	COL138		R	-759.5	754.3	494	COL90		R	-2842.7	754.3
447	COL137		B	-802.9	754.3	495	COL89		B	-2886.1	754.3
448	COL136	SEG45	G	-846.3	754.3	496	COL88	SEG29	G	-2929.5	754.3
449	COL135		R	-889.7	754.3	497	COL87		R	-2972.9	754.3
450	COL134		B	-933.1	754.3	498	COL86		B	-3016.3	754.3
451	COL133	SEG44	G	-976.5	754.3	499	COL85	SEG28	G	-3059.7	754.3
452	COL132		R	-1019.9	754.3	500	COL84		R	-3103.1	754.3
453	COL131		B	-1063.3	754.3	501	COL83		B	-3146.5	754.3
454	COL130	SEG43	G	-1106.7	754.3	502	COL82	SEG27	G	-3189.9	754.3
455	COL129		R	-1150.1	754.3	503	COL81		R	-3233.3	754.3
456	COL128		B	-1193.5	754.3	504	COL80		B	-3276.7	754.3
457	COL127	SEG42	G	-1236.9	754.3	505	COL79	SEG26	G	-3320.1	754.3
458	COL126		R	-1280.3	754.3	506	COL78		R	-3363.5	754.3
459	COL125		B	-1323.7	754.3	507	COL77		B	-3406.9	754.3
460	COL124	SEG41	G	-1367.1	754.3	508	COL76	SEG25	G	-3450.3	754.3
461	COL123		R	-1410.5	754.3	509	COL75		R	-3493.7	754.3
462	COL122		B	-1453.9	754.3	510	COL74		B	-3537.1	754.3
463	COL121	SEG40	G	-1497.3	754.3	511	COL73	SEG24	G	-3580.5	754.3
464	COL120		R	-1540.7	754.3	512	COL72		R	-3623.9	754.3

Pad #	Pad Name	Signal	Color	X-pos	Y-pos	Pad #	Pad Name	Signal	Color	X-pos	Y-pos
513	COL71		B	-3667.3	754.3	561	COL23		B	-5750.5	754.3
514	COL70	SEG23	G	-3710.7	754.3	562	COL22	SEG7	G	-5793.9	754.3
515	COL69		R	-3754.1	754.3	563	COL21		R	-5837.3	754.3
516	COL68		B	-3797.5	754.3	564	COL20		B	-5880.7	754.3
517	COL67	SEG22	G	-3840.9	754.3	565	COL19	SEG6	G	-5924.1	754.3
518	COL66		R	-3884.3	754.3	566	COL18		R	-5967.5	754.3
519	COL65		B	-3927.7	754.3	567	COL17		B	-6010.9	754.3
520	COL64	SEG21	G	-3971.1	754.3	568	COL16	SEG5	G	-6054.3	754.3
521	COL63		R	-4014.5	754.3	569	COL15		R	-6097.7	754.3
522	COL62		B	-4057.9	754.3	570	COL14		B	-6141.1	754.3
523	COL61	SEG20	G	-4101.3	754.3	571	COL13	SEG4	G	-6184.5	754.3
524	COL60		R	-4144.7	754.3	572	COL12		R	-6227.9	754.3
525	COL59		B	-4188.1	754.3	573	COL11		B	-6271.3	754.3
526	COL58	SEG19	G	-4231.5	754.3	574	COL10	SEG3	G	-6314.7	754.3
527	COL57		R	-4274.9	754.3	575	COL9		R	-6358.1	754.3
528	COL56		B	-4318.3	754.3	576	COL8		B	-6401.5	754.3
529	COL55	SEG18	G	-4361.7	754.3	577	COL7	SEG2	G	-6444.9	754.3
530	COL54		R	-4405.1	754.3	578	COL6		R	-6488.3	754.3
531	COL53		B	-4448.5	754.3	579	COL5		B	-6531.7	754.3
532	COL52	SEG17	G	-4491.9	754.3	580	COL4	SEG1	G	-6575.1	754.3
533	COL51		R	-4535.3	754.3	581	COL3		R	-6618.5	754.3
534	COL50		B	-4578.7	754.3	582	COL2		B	-6661.9	754.3
535	COL49	SEG16	G	-4622.1	754.3	583	COL1	SEG0	G	-6705.3	754.3
536	COL48		R	-4665.5	754.3	584	COL0		R	-6748.7	754.3
537	COL47		B	-4708.9	754.3						
538	COL46	SEG15	G	-4752.3	754.3						
539	COL45		R	-4795.7	754.3						
540	COL44		B	-4839.1	754.3						
541	COL43	SEG14	G	-4882.5	754.3						
542	COL42		R	-4925.9	754.3						
543	COL41		B	-4969.3	754.3						
544	COL40	SEG13	G	-5012.7	754.3						
545	COL39		R	-5056.1	754.3						
546	COL38		B	-5099.5	754.3						
547	COL37	SEG12	G	-5142.9	754.3						
548	COL36		R	-5186.3	754.3						
549	COL35		B	-5229.7	754.3						
550	COL34	SEG11	G	-5273.1	754.3						
551	COL33		R	-5316.5	754.3						
552	COL32		B	-5359.9	754.3						
553	COL31	SEG10	G	-5403.3	754.3						
554	COL30		R	-5446.7	754.3						
555	COL29		B	-5490.1	754.3						
556	COL28	SEG9	G	-5533.5	754.3						
557	COL27		R	-5576.9	754.3						
558	COL26		B	-5620.3	754.3						
559	COL25	SEG8	G	-5663.7	754.3						
560	COL24		R	-5707.1	754.3						

Pad #	Pad Name	Signal ($MUX68/\overline{80}$ = V_{DD}) - 68mux	Signal ($MUX68/\overline{80}$ = V_{SS}) – 80mux	X-pos	Y-pos
585	ROW40	Non Select Signal	COM40	-6922.3	754.3
586	ROW41	Non Select Signal	COM41	-6965.7	754.3
587	ROW42	Non Select Signal	COM42	-7009.1	754.3
588	ROW43	Non Select Signal	COM43	-7052.5	754.3
589	ROW44	Non Select Signal	COM44	-7095.9	754.3
590	ROW45	Non Select Signal	COM45	-7139.3	754.3
591	ROW46	COM34	COM46	-7182.7	754.3
592	ROW47	COM35	COM47	-7226.1	754.3
593	ROW48	COM36	COM48	-7269.5	754.3
594	ROW49	COM37	COM49	-7312.9	754.3
595	ROW50	COM38	COM50	-7356.3	754.3
596	ROW51	COM39	COM51	-7399.7	754.3
597	ROW52	COM40	COM52	-7443.1	754.3
598	ROW53	COM41	COM53	-7486.5	754.3
599	ROW54	COM42	COM54	-7529.9	754.3
600	ROW55	COM43	COM55	-7573.3	754.3
601	ROW56	COM44	COM56	-7616.7	754.3
602	ROW57	COM45	COM57	-7660.1	754.3
603	ROW58	COM46	COM58	-7703.5	754.3
604	ROW59	COM47	COM59	-7746.9	754.3
605	ROW60	COM48	COM60	-7790.3	754.3
606	ROW61	COM49	COM61	-7833.7	754.3
607	ROW62	COM50	COM62	-7877.1	754.3
608	ROW63	COM51	COM63	-7920.5	754.3
609	ROW64	COM52	COM64	-7963.9	754.3
610	ROW65	COM53	COM65	-8007.3	754.3
611	ROW66	COM54	COM66	-8050.7	754.3
612	ROW67	COM55	COM67	-8094.1	754.3
613	ROW68	COM56	COM68	-8137.5	754.3
614	ROW69	COM57	COM69	-8180.9	754.3
615	ROW70	COM58	COM70	-8224.3	754.3
616	ROW71	COM59	COM71	-8267.7	754.3
617	ROW72	COM60	COM72	-8311.1	754.3
618	ROW73	COM61	COM73	-8354.5	754.3
619	ROW74	COM62	COM74	-8397.9	754.3
620	ROW75	COM63	COM75	-8441.3	754.3
621	ROW76	COM64	COM76	-8484.7	754.3
622	ROW77	COM65	COM77	-8528.1	754.3
623	ROW78	COM66	COM78	-8571.5	754.3
624	ROW79	COM67	COM79	-8614.9	754.3
625	ICONS	ICONS	ICONS	-8658.3	754.3
626	DUMMY			-8701.7	754.3
627	DUMMY			-8745.1	754.3

Bump Size

PAD#	X [um]	Y [um]	Pad pitch [um]
Pad 1-229	56	92	76.2
Pad 230 - 627	28	130	43.4
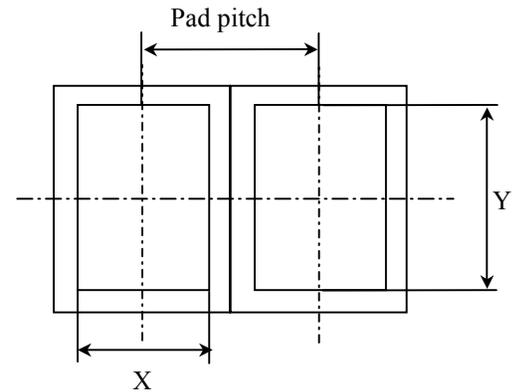
6   PIN DESCRIPTION

6.1 $\overline{CS}$

This pin is the chip selection input. The chip is enabled for MCU communication only when $\overline{CS}$ is pulled low.

6.2 $\overline{RES}$

This pin is the reset signal input. Initialization of the chip is started once the reset pin is pulled low. The minimum pulse width for reset sequence is 10us.

6.3   D/$\overline{C}$

This pin is Data/Command control pin. When the pin is pulled high, the input at D_7-D_0 is treated as display data. When the pin is pulled low, the input at D_7-D_0 will be transferred to the command register.

6.4   R/$\overline{W}$ ($\overline{WR}$)

This pin is MCU interface input. When 6800 interface mode is selected, this pin will be used as Read/Write (R/$\overline{W}$) selection input. Read mode will be carried out when this pin is pulled high and write mode when this pin is pulled low.
When 8080 interface mode is selected, this pin is the Write ($\overline{WR}$) control signal input. Data write operation is initiated when this pin is pulled low and the chip is selected.

6.5   E($\overline{RD}$)

This pin is MCU interface input. When 6800 interface mode is selected, this pin will be used as the Enable (E) signal. Read/ write operation is initiated when this pin is pulled high and the chip is selected.
When 8080 interface mode is selected, this pin is the Read ($\overline{RD}$) control signal input. Data read operation is initiated when this pin is pulled low and the chip is selected.

6.6   PS0 – PS1

These pins are the bus interface mode selection input. Different bus interface can be selected changing the setting of these pins.

PS1	PS0	MPU Interface
L	H	8-bit 8080 parallel interface
H	H	8-bit 6800 parallel interface
H	L	3-lines serial peripheral interface (SPI) – 9 bits SPI
L	L	4-lines serial peripheral interface (SPI)

Note1: For serial applications, D_0 – D_5, R/$\overline{W}$ ($\overline{WR}$), E($\overline{RD}$) are recommended to connect V_{DD}.
Note2: Read back operation is only available in parallel mode

6.7   MUX68/$\overline{80}$

This pin is used to select the Mux ratio of the LCD driver. When MUX68/($\overline{80}$) is equal to V_{DD}, COM0 ~COM33 are mapped to ROW0~ROW33 and COM46~COM79 are mapped to ROW34~ROW67 of the memory. When MUX68/($\overline{80}$) is equal to V_{SS}, COM0~COM79 are mapped to ROW0~ROW79.

6.8 D_7-D_0

These pins are the 8-bit bi-directional data bus in parallel interface mode. D_7 is the MSB while D_0 is the LSB. When serial mode selected, D_7 is the serial data input SDA and D_6 is the serial clock input SCK.

6.9 VL$_{REF}$

This pin is the ground of operation amplifier V$_{L4}$ and V$_{L5}$. In normal power mode, it must connect to V$_{SS}$. In low power mode, it must connect to V$_{CI}$ and V$_{L4}$ must greater than 4V. Please refer to Figure 5 on page 20 for the detail.

6.10 VH$_{REF}$

This pin is the power supply pin of the operation amplifier V$_{L3}$. It must connect to V$_{OUT}$.

6.11 V$_{CIX2}$

This pin is internal reference pin. It must connect to V$_{CI}$.

6.12 V$_{DD}$

This pin is the system power supply pin of the logic block.

6.13 V$_{DDIO}$

This pin is the system power supply pin of I/O buffer. Please refer to Figure 24 on page 59 for connection example.

6.14 V$_{CI}$

This pin is the reference voltage input for internal DC-DC converter. The DC-DC converter output is equals to the multiple factor (3X, 4X, 5X or 6X) times V$_{CI}$ with respect to V$_{SS}$. The maximum output voltage will limit the max. V$_{OUT}$ characteristic.

Note: Voltage at this input pin must be larger than or equal to V$_{DD}$. ($V_{CI} \geq V_{DD}$)

6.15 V$_{SS}$

This pin is the ground of logic.

6.16 RV$_{SS}$

This pin is the ground of Vref.

6.17 CV$_{SS}$

This pin is the ground of analog.

6.18 V$_{OUT}$

This is the most positive voltage supply pin of the chip. It can be supplied externally or generated by the internal DC-DC converter. If the internal DC-DC converter generates the voltage level at V$_{OUT}$, the voltage level is used for internal referencing only. The voltage level at V$_{OUT}$ pin is not used for driving external circuitry.

6.19 V_{L5}, V_{L4}, V_{L3} and V_{L2}

LCD driving voltages. They can be supplied externally or generated by the internal bias divider. They have the following relationship:

$$V_{OUT} > V_{L5} > V_{L4} > V_{L3} > V_{L2} > V_{SS}$$

Table 3 – $V_{OUT} > V_{L5} > V_{L4} > V_{L3} > V_{L2} > V_{SS}$ Relationship

	1 : a bias
V_{L5}	(a-1)/a * V_{OUT}
V_{L4}	(a-2)/a * V_{OUT}
V_{L3}	2/a * V_{OUT}
V_{L2}	1/a * V_{OUT}

6.20 ROW0 – ROW79

These pins provide the driving signals, COMMON, to the LCD panel.

6.21 COL0 – COL311

These pins provide the LCD driving signals, SEGMENT, to the LCD panel. The Red, Green, Blue colors signal are sent out from the SEGMENT output at the same time. The output voltage level of these pins is V_{DD} during sleep mode or standby mode.

6.22 ICON

This pin provides the driving signals, COMMON icon line.

6.23 CL

This pin is the system clock I/O. This pin is the external clock input for the device, which is enabled by using extended command. It should be left open under normal operation. The internal oscillator will be used after power on reset.

6.24 M

This pin is used for cascade purpose only. It should be left open under normal operation.

6.25 SYN

This pin is used for cascade purpose only. It should be left open under normal operation.

6.26 BUSY

This pin will be high during RAM buffer read/write operation and during graphic commands executing. System programmer should read this pin (low is ready, high is busy) before sending next RAM buffer related command (e.g. RAM write – 5CH; RAM read – 5DH OR any graphic commands)

6.27 TEST0~TEST17

These pins are used for internal only and should be left open, any connection is not allowed.

6.28 Dummy

There is a floating dummy pad without any internal circuitry connection.

7 FUNCTIONAL BLOCK DESCRIPTIONS

7.1 Microprocessor Interface Logic

The Microprocessor Interface unit consists of three functional blocks for driving the 6800-series parallel interface, 8080-series parallel interface, 3-lines serial peripheral interface and 4-lines serial peripheral interface. The selection of different interface is done by PS0 to PS1 pins. Please refer to the pin descriptions on page 12.

   a) MPU Parallel 6800-series Interface

      The parallel Interface consists of 8 bi-directional data pins ($D_7 - D_0$), R/$\overline{W}$, D/$\overline{C}$, E, $\overline{CS}$. R/$\overline{W}$ ($\overline{WR}$) input high indicates a read operation from the Graphical Display Data RAM (GDDRAM) or the status register. R/$\overline{W}$ input low indicates a write operation to Display Data RAM or Internal Command Registers depending on the status of D/$\overline{C}$ input. The E input serves as data latch signal (clock) when high provided that $\overline{CS}$ is low. Please refer to Figure 19 to Figure 20 on page 54 to 55 for Parallel Interface Timing Diagram of 6800-series microprocessors. In order to match the operating frequency of the GDDRAM with that of the MCU, some pipeline processing is internally performed which requires the insertion of a dummy read before the first actual display data read. This is shown in the following diagram.
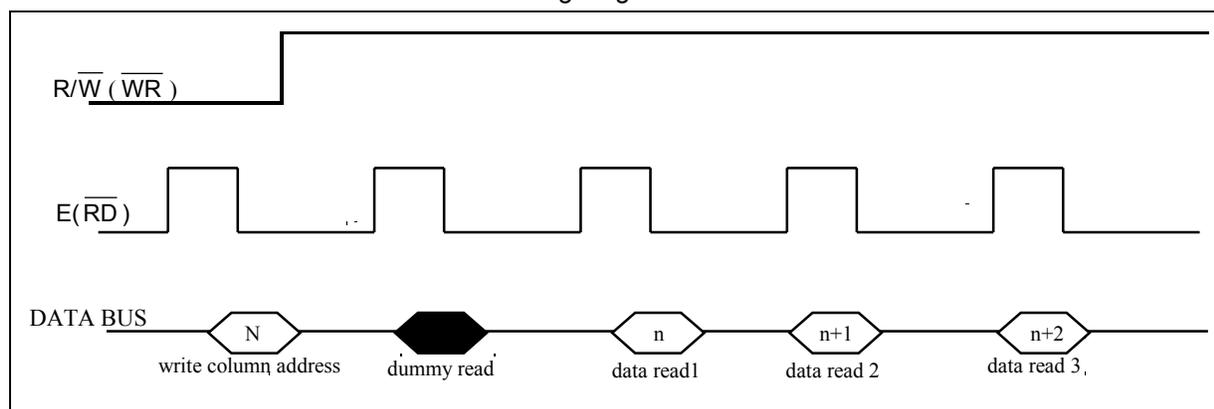
Figure 3 – Display Data

   b) MPU Parallel 8080-series Interface

      The parallel interface consists of 8 bi-directional data pins $D_7 - D_0$, $\overline{RD}$, $\overline{WR}$, D/$\overline{C}$, $\overline{CS}$. $\overline{RD}$ input serves as data read latch signal (clock) when low provided that $\overline{CS}$ is low. Whether reading the display data from GDDRAM or reading the status from the status register is controlled by D/$\overline{C}$. $\overline{WR}$ input serves as data write latch signal (clock) when low provided that $\overline{CS}$ is low. Whether writing the display data to the GDDRAM or writing the command to the command register is controlled by D/$\overline{C}$. A dummy read is also required before the first actual display data read for 8080-series interface.

   c) MPU 4-lines Serial Peripheral Interface

      The 4-lines serial peripheral Interface consists of serial clock SCK, serial data SDA, D/$\overline{C}$, $\overline{CS}$. SDA is shifted into 8-bit shift register on every rising edge of SCK in the order of data bit 7, data bit 6 …… data bit 0. D/$\overline{C}$ is sampled on every eighth clock to determine whether the data byte in the shift register is written to the Display Data RAM or command register at the same clock. Please refer to Figure 21 on page 56 for serial interface timing.

d) MPU 3-lines Serial Peripheral Interface

The operation is similar to 4-lines serial peripheral interface while D/$\overline{C}$ is not used. There are altogether 9-bits will be shifted into the shift register on every ninth clock in sequence: D/$\overline{C}$ bit, D_7 to D_0 bit. The D/$\overline{C}$ bit (first bit of the sequential data) will determine the following data byte in the shift register is written to the Display Data RAM (D/$\overline{C}$ bit = 1) or the command register (D/$\overline{C}$ bit = 0).

	6800 – series Parallel Interface	8080 – series Parallel Interface	3-lines or 4-lines Serial peripheral Interface
Data Read	8-bits	8-bits	No
Data Write	8-bits	8-bits	8-bits
Command Read	Status only	Status only	No
Command Write	Yes	Yes	Yes

Table 4 – Data bus selection modes

7.2 Reset Circuit

This block is integrated into the Microprocessor Interface Logic which includes Power On Reset circuitry and the hardware reset pin, $\overline{RES}$. Both of these having the same reset function. Once the $\overline{RES}$ pin receives a negative reset pulse, all internal circuitry will start to initialize. The minimum pulse width for completing the reset sequence is 10us. The status of the chip after reset is given by:

When $\overline{RES}$ input is low, the chip is initialized to the following:

1.	Display ON/OFF:	Display is OFF
2.	Normal/Inverse Display:	Normal Display
3.	COM Scan Direction:	COM0 -> COM67/COM79
4.	Internal Oscillator:	Disable
5.	Reference Voltage Generation Circuit:	Disable
6.	Voltage regulator and Voltage Follower:	Disable
7.	Booster level:	6X
8.	Bias ratio:	1/7(68 Mux) / 1/8 (80 Mux)
9.	Multiplex ratio:	68 / 80 Mux
10.	Contrast level:	32
11.	Internal regulator gain:	2.84
12.	Average temperature gradient:	-0.2%/^{o}C
13.	Partial display mode:	Disable
	Start COM address:	0
	End COM address:	0
14.	Area Scroll set	
	Top block address:	0
	Bottom block address:	0
	Number of specified block:	0
	Area scroll mode:	Whole screen scroll mode
15.	Scroll start set	
	Start block address:	0
16.	Data Scan Direction	
	Normal/inverse display of page address:	Normal
	Normal/inverse display of column address:	Normal
	Address-scan direction:	Column direction
	RGB arrangement:	RGB
	Gray-scale setup:	8 gray-scale
17.	Start Page Address set:	0
18.	End Page Address set:	0
19.	Start Column address set:	0
20.	End Column address set:	0
21.	Select PWM/FRC	2-bit PWM + 2 bit FRC mode

7.3 Command Decoder

This module determines whether the input data is interpreted as data or command. Data is directed to this module based upon the input of the D/$\overline{C}$ pin. If D/$\overline{C}$ pin is high, data is written to Graphic Display data RAM (GDDRAM). If it is low, the input at $D_7 - D_0$ is interpreted as a Command and it will be decoded. The decoded command will be written to the corresponding command register.

7.4 Graphic Display Data RAM (GDDRAM)

The GDDRAM is a bit mapped static RAM holding the bit pattern to be displayed. The size of the RAM is 312 (104 RGB) x 81 x 4 = 101088 bits. Figure 4 on page 19 is a description of the GDDRAM address map. For mechanical flexibility, re-mapping on both Segment and Common outputs can be selected by software. Please refer to the command "Data Output/Scan direction" in Table 5 on page 22 for detail description.

Four pages of display data form a RAM address block and stored in the GDDRAM. Each block will form the fundamental units of scrolling addresses. Various types of area scrolling can be performed by software program according to the command "Set area Scroll" and "Set Scroll Start" in Table 11 on page 36.

In order to ease the access of the red, green and blue color data; the 8-bits color data (Red: 3 bits, Green: 3 bits, Blue: 2 bits) is converted to 4-bits data (P10, P11, P12, P13). The 4-bits data are stored into the GDDRAM such that the data are located in the appropriate RAM locations according to the gray scale settings. Please refer to the description section of the command "Set Data Output/Scan Direction" on page 22.

each cell contains 4-bits data

COMMON OUTPUT

BLOCK	PAGE		COMMON OUTPUT
	0		COM0
	1		COM1
	2		COM2
0	3		COM3
	4		COM4
	5		COM5
	6		COM6
1	7		COM7
	8		COM8
	9		COM9
	10		COM10
2	11		COM11
⋮	⋮		⋮
	64		COM64
	65		COM65
	66		COM66
16	67		COM67
	68		COM68
	69		COM69
	70		COM70
17	71		COM71
	72		COM72
	73		COM73
	74		COM74
18	75		COM75
	76		COM76
	77		COM77
	78		COM78
19	79		COM79
20	ICON		ICON

DATA

SEGMENT: SEG0, SEG1, SEG2, ..., SEG101, SEG102, SEG103

COLUMN: COL0, COL1, COL2, COL3, COL4, COL5, COL6, COL7, COL8, ..., COL303, COL304, COL305, COL306, COL307, COL308, COL309, COL310, COL311

Mapping depends on COM Output scan direction setting

Notes: Page and SEGMENT data scan direction depend on Data Output Scan Direction Setting.

Data Output Scan Directin setting cannot affect the Block scan direction.

Figure 4 – Display Data RAM Map

7.5 LCD Driving Voltage Generator and Regulator

This module generates the LCD voltage needed for display output. It takes a single supply input and generates necessary bias voltages. It consists of:

1. 3X, 4X, 5X and 6X DC-DC voltage converter
2. Bias Divider - If the output op-amp buffer option in Set Power Control Register command is enabled, this circuit block will divide the regulator output (V_{OUT}) to give the LCD driving levels ($V_{L2} - V_{L5}$).
    The divider does not require external capacitors to reduce the external hardware and pin counts, power configuration of op-amp is shown on below figure.
3. Contrast Control – Software control of 64 voltage levels of LCD voltage.
4. Bias Ratio Selection circuitry – Software control of 1/4 to 1/8 bias ratio to match the characteristic of LCD panel.
5. Self adjust temperature compensation circuitry – Provide 4 different compensation grade selections to satisfy the various liquid crystal temperature grades. The grading can be selected by software control. Defaulted temperature coefficient (TC) value is –0.2%/°C.
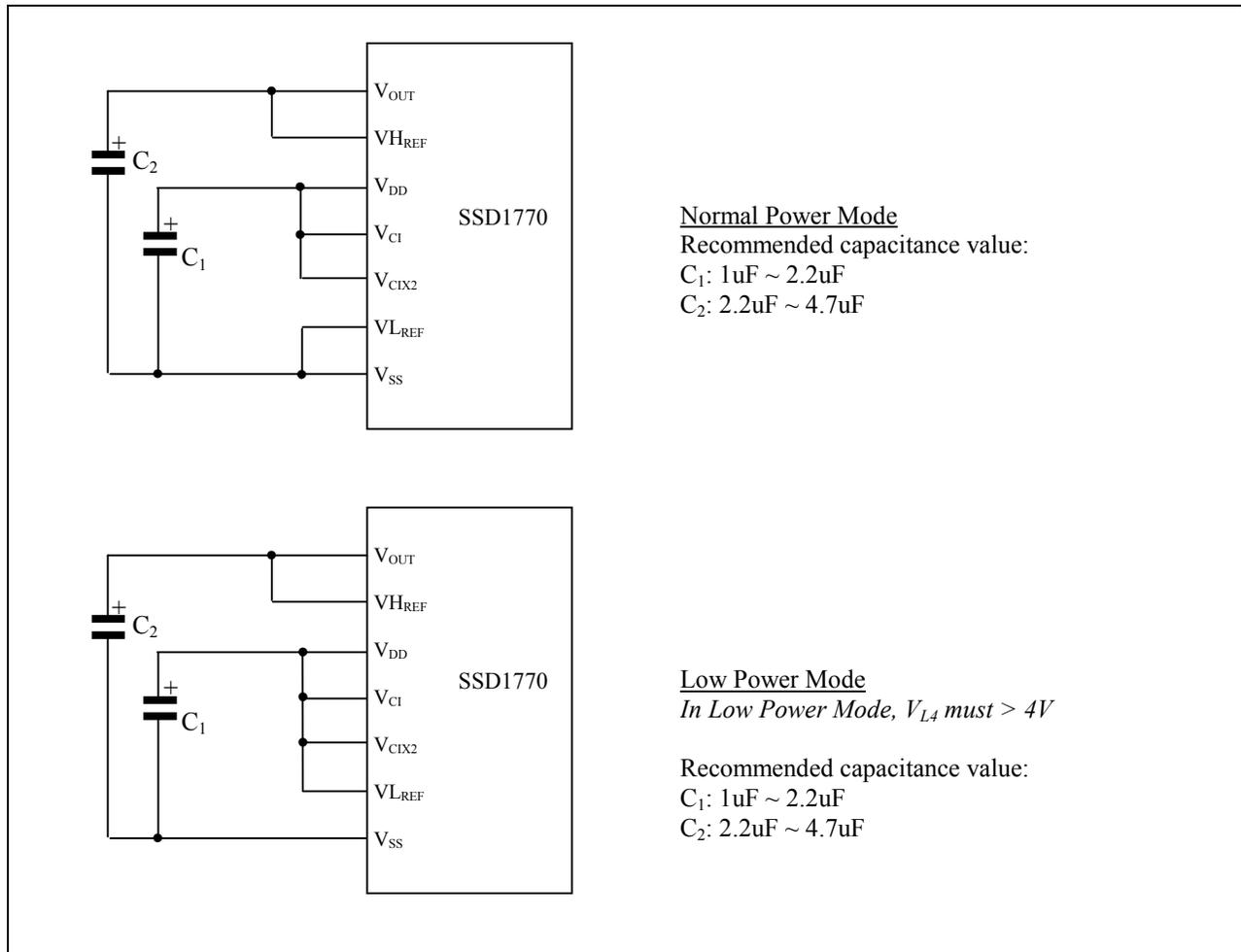
Figure 5 – SSD1770 Hardware Configurations

7.6 Oscillator Circuit

This module is an On-Chip low power RC oscillator circuitry (Figure 6). The oscillator generates the clock for the DC-DC voltage converter. This clock is also used in the Display Timing Generator.
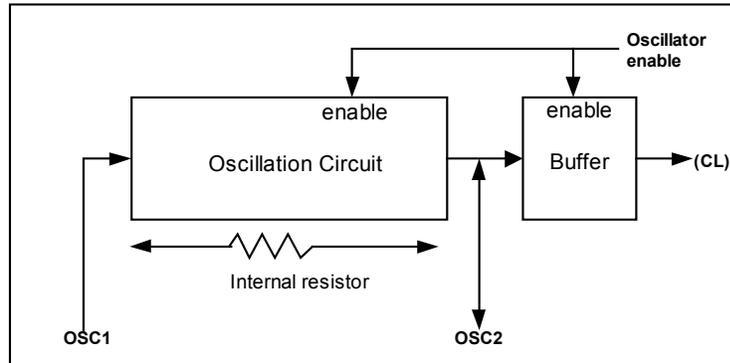
Figure 6 – Oscillator structural block diagram

7.7 Display Data Latch

This block is a series of latches carrying the display signal information. These latches hold the data, which will be fed to the HV Buffer Cell and Level Selector to output the required voltage level.

7.8 HV Buffer Cell (Level Shifter)

This block is embedded in the Segment/Common Driver Circuits. HV Buffer Cell works as a level shifter, which translates the low voltage output signal to the required driving voltage. The output is shifted out with reference to the internal FRM clock, which comes from the Display Timing Generator. The voltage levels are given by the level selector, which is synchronized with the internal M signal.

7.9 Level Selector

This block is embedded in the Segment/Common Driver circuits. Level Selector is a control of the display synchronization. Display voltage levels can be separated into two sets and used with different cycles. Synchronization is important since it selects the required LCD voltage level to the HV Buffer Cell, which in turn outputs the COM or SEG LCD waveform.

8 COMMAND TABLE

Table 5 – COMMAND TABLE (D/$\overline{C}$ = 0, R/$\overline{W}$ ($\overline{WR}$) = 0, E=1($\overline{RD}$ = 1) unless specific setting is stated)

Bit Pattern	Command	Description
(D/$\overline{C}$ = 0) 00010101 (D/$\overline{C}$ = 1) $X_7X_6X_5X_4X_3X_2X_1X_0$ (D/$\overline{C}$ = 1) $Y_7Y_6Y_5Y_4Y_3Y_2Y_1Y_0$	Set Column Address	Set the start column address by $X_7X_6X_5X_4X_3X_2X_1X_0$ Set the end column address by $Y_7Y_6Y_5Y_4Y_3Y_2Y_1Y_0$. Column address = 00000000b (POR) In 8-levels gray scale mode, column address is in a range of 0~103. In 16-level gray scale mode, column address is in a range of 0~51.
(D/$\overline{C}$ = 0) 01110101 (D/$\overline{C}$ = 1) $X_7X_6X_5X_4X_3X_2X_1X_0$ (D/$\overline{C}$ = 1) $Y_7Y_6Y_5Y_4Y_3Y_2Y_1Y_0$	Set Page Address	Set the start page address by $X_7X_6X_5X_4X_3X_2X_1X_0$ Set the end page address by $Y_7Y_6Y_5Y_4Y_3Y_2Y_1Y_0$. Page address = 00000000b (POR)
(D/$\overline{C}$ = 0) 10111011 (D/$\overline{C}$ = 1) *****$X_2X_1X_0$	Set COM Output Scan Direction	MUX68/$\overline{80}$ = V_{SS} X_2 X_1 X_0 ROW0..ROW33 ROW34..ROW39 ROW40..ROW45 ROW46..ROW79 0 0 0 COM0->COM33 COM34->COM39 COM40->COM45 COM46->COM79 (POR) 0 0 1 COM0->COM33 COM34->COM39 COM79<-COM64 COM63<-COM40 0 1 0 COM39<-COM6 COM5<-COM0 COM40->COM45 COM46->COM79 0 1 1 COM39<-COM6 COM5<-COM0 COM79<-COM64 COM63<-COM40 MUX68/$\overline{80}$ = V_{DD} X_2 X_1 X_0 ROW0..ROW33 ROW34..ROW39 ROW40..ROW45 ROW46..ROW79 0 0 0 COM0->COM33 NON SELECT OUTPUT COM34->COM67 (POR) 0 0 1 COM0->COM33 NON SELECT OUTPUT COM67<-COM34 0 1 0 COM33<-COM0 NON SELECT OUTPUT COM34->COM67 0 1 1 COM33<-COM0 NON SELECT OUTPUT COM67<-COM34
(D/$\overline{C}$ = 0) 10111100 (D/$\overline{C}$ = 1) *****P12 P11 P10 (D/$\overline{C}$ = 1) *****P22 P21 P20 (D/$\overline{C}$ = 1) *****P32 P31 P30	Set Data Output Scan Direction	a) Normal or Reverse page/column/scan directions P10 = 0: set page address to normal display (POR) P10 = 1: set page address to inverse display P11 = 0: set column address to normal rotation (POR) P11 = 1: set column address to inverse rotation P12 = 0: set scan direction to column scan (POR) P12 = 1: set scan direction to page scan Please refer to the Figure 9 on page 33 for detail description of column/page scan direction modes b) RGB color arrangement P22, P21, P20: The control bits are used for setting the (RGB) color arrangement of segment output, 000 is POR value. Please refer to the Figure 10 on page 34 for detail mapping of the segment output. c) Gray-scale selection P32 P31 P30 Gray-scale modes 0 0 1 8-levels gray scale mode (POR) 0 1 0 16-levels gray scale mode (Type A) Please refer to the Table 12 on page 27 to Table 15 on page 30 for detail description of different gray-scale selection modes.

Remarks: "" denote DON'T CARE bit*

Bit Pattern	Command	Description
$(D/\overline{C} = 0)$ 11001110 $(D/\overline{C} = 1)$ **** $X_{31}X_{21}X_{11}X_{01}$ $(D/\overline{C} = 1)$ **** $X_{32}X_{22}X_{12}X_{02}$: $(D/\overline{C} = 1)$ **** $X_{38}X_{28}X_{18}X_{08}$ $(D/\overline{C} = 1)$ **** $X_{39}X_{29}X_{19}X_{09}$: $(D/\overline{C} = 1)$ **** $X_{316}X_{216}X_{116}X_{016}$ $(D/\overline{C} = 1)$ **** $X_{317}X_{217}X_{117}X_{017}$: $(D/\overline{C} = 1)$ **** $X_{320}X_{220}X_{120}X_{020}$	Set Color Look Up Table	N DB_3 DB_2 DB_1DB_0 color position 1 X_{3N} X_{2N} X_{1N} X_{0N} Intermediate red tone 000 2 X_{3N} X_{2N} X_{1N} X_{0N} Intermediate red tone 001 : : 8 X_{3N} X_{2N} X_{1N} X_{0N} Intermediate red tone 111 9 X_{3N} X_{2N} X_{1N} X_{0N} Intermediate green tone 000 : : 16 X_{3N} X_{2N} X_{1N} X_{0N} Intermediate green tone 111 17 X_{3N} X_{2N} X_{1N} X_{0N} Intermediate blue tone 00 : : 20 X_{3N} X_{2N} X_{1N} X_{0N} Intermediate blue tone 11
$(D/\overline{C} = 0)$ 11001010 $(D/\overline{C} = 1)$ 00000000 $(D/\overline{C} = 1)$ ** $Y_5Y_4Y_3Y_2Y_1Y_0$ $(D/\overline{C} = 1)$ 00000000	Set Display Control	Driver duty selection Select driver duty from 1 / 8 to 1 / 80. As $Y_5Y_4Y_3Y_2Y_1Y_0$ is increased from 000001b to 010011b, the number of display lines, N is increased at the same rating. To specify the $Y_5Y_4Y_3Y_2Y_1Y_0$, $$Y_5 \sim Y_0 = \frac{N}{4} - 1$$
$(D/\overline{C} = 0)$ 10101010 $(D/\overline{C} = 1)$ ** $X_5X_4X_3X_2X_1X_0$ $(D/\overline{C} = 1)$ ** $Y_5Y_4Y_3Y_2Y_1Y_0$ $(D/\overline{C} = 1)$ ** $Z_5Z_4Z_3Z_2Z_1Z_0$ $(D/\overline{C} = 1)$ ****** P41 P40	Set Area Scroll	a) Top Block Address $X_5X_4X_3X_2X_1X_0$ is used to specify the block address (1 block = 4 lines) at the top of the scrolling area. Top block address = 000000b (POR) b) Bottom Block Address $Y_5Y_4Y_3Y_2Y_1Y_0$ is used to specify the block address (1 block = 4 lines) at the bottom of the scrolling area. Bottom block address = 000000b (POR) c) Number of specified Blocks The number of specified blocks = Number of (Top fixed area + Scroll area) blocks −1. If bottom scroll or whole screen scroll mode is chosen, the number of specified blocks is set to $Z_5 \sim Z_0$ Number of specified blocks = 000000b (POR) d) Area Scroll Mode There are four types of area scroll. P41 P40 Types of Area Scroll 0 0 Center Screen Scroll 0 1 Top Screen Scroll 1 0 Bottom Screen Scroll 1 1 Whole Screen Scroll Type of area scroll = Whole Screen Scroll (POR)
$(D/\overline{C} = 0)$ 10101011 $(D/\overline{C} = 1)$ ** $X_5X_4X_3X_2X_1X_0$	Set Scroll Start	$X_5X_4X_3X_2X_1X_0$ specify the start block address (1 block = 4 lines) of area scrolling. Start block address = 000000b (POR)

Remarks: "" denote DON'T CARE bit*

Bit Pattern	Command	Description
$(D/\overline{C} = 0)$ 00100000 $(D/\overline{C} = 1)$ ****$X_3X_2X_1X_0$	Set Power Control Register	X_0=0: turns off the reference voltage generator (POR) X_0=1: turns on the reference voltage generator X_1=0: turns off the internal regulator and voltage follower (POR) X_1=1: turns on the internal regulator and voltage follower Select booster level X_3 X_2 Boost level 0 0 3X 0 1 4X 1 0 5X 1 1 6X (POR)
$(D/\overline{C} = 0)$ 10000001 $(D/\overline{C} = 1)$ ** $X_5X_4X_3X_2X_1X_0$ $(D/\overline{C} = 1)$ ***** $Y_2Y_1Y_0$	Set Contrast Level & Internal Regulator Resistor Ratio	a) Select contrast level from 64 contrast steps Contrast increases as $X_5X_4X_3X_2X_1X_0$ is increased from 000000b to 111111b. $X_5X_4X_3X_2X_1X_0$ = 000000b (POR) b) The internal regulator gain $(1+R_2/R_1)$ V_{OUT} increases as $Y_2Y_1Y_0$ is increased from 000b to 111b. The factor, $1+R_2/R_1$, is given by: $Y_2Y_1Y_0$ = 000: 2.84 (POR) $Y_2Y_1Y_0$ = 001: 3.71 $Y_2Y_1Y_0$ = 010: 4.57 $Y_2Y_1Y_0$ = 011: 5.44 $Y_2Y_1Y_0$ = 100: 6.30 $Y_2Y_1Y_0$ = 101: 7.16 $Y_2Y_1Y_0$ = 110: 8.03 $Y_2Y_1Y_0$ = 111: 8.89
$(D/\overline{C} = 0)$ 1101011X_0	Set Increment / Decrement of the contrast	X_0=0: The contrast set of voltage regulator is incremented by 1 X_0=1: The contrast set of voltage regulator is decremented by 1
$(D/\overline{C} = 0)$ 1010011X_0	Set Normal/Inverse Display	X_0=0: normal display (POR) X_0=1: inverse display
$(D/\overline{C} = 0)$ 10101000 $(D/\overline{C} = 1)$ *$X_6X_5X_4X_3X_2X_1X_0$ $(D/\overline{C} = 1)$ *$Y_6Y_5Y_4Y_3Y_2Y_1Y_0$	Enter partial Display	$X_6X_5X_4X_3X_2X_1X_0$: Start COM Address = 000000b (POR) $Y_6Y_5Y_4Y_3Y_2Y_1Y_0$: End COM Address = 000000b (POR)
$(D/\overline{C} = 0)$ 10101001	Exit partial Display	Exit the "partial display mode" by executing the command 10101001b (POR)
$(D/\overline{C} = 0)$ 1010111X_0	Set Display On/Off	X_0=0: turns off LCD panel (POR) X_0=1: turns on LCD panel
$(D/\overline{C} = 0)$ 1001010X_0	Enter/Exit sleep mode	X_0=0: exit the sleep mode. X_0=1: enter sleep mode. (POR)
$(D/\overline{C} = 0)$ 110100 X_1X_0	Enable/disable internal oscillator	X_1 X_0 Internal oscillator status 0 1 ON 1 0 OFF (POR)
$(D/\overline{C} = 0)$ 10000010 $(D/\overline{C} = 1)$ ****** X_1X_0	Set Temperature compensation coefficient	Average temperature gradients X_1 X_0 Average Temperature Gradient [%/^{o}C] 0 0 -0.10 0 1 -0.15 1 0 -0.20(POR) 1 1 -0.25
$(D/\overline{C} = 0)$ 00100101	NOP	Command result in No Operation The command should be issued after the execution of the Status Read command
$(D/\overline{C} = 0)$ 01011100 $(D/\overline{C} = 1)$ $Y_{71}Y_{61}Y_{51}Y_{41}Y_{31}Y_{21}Y_{11}Y_{01}$	Write display data	Enter the "write display data mode " by executing the command 01011100b. The following byte is used to specify the data byte to be written to the GDDRAM directly. The $D/\overline{C}$ bit should be stated at logic "1" during the display data is written to the GDDRAM.

Remarks: "" denote DON'T CARE bit*

Bit Pattern	Command	Description
$(D/\overline{C} = 0)$ 01011101 $(D/\overline{C} = 1 \ \& \ R/\overline{W} = 1)$ ******** $Y_{71}Y_{61}Y_{51}Y_{41}Y_{31}Y_{21}Y_{11}Y_{01}$	Read display data	Enter the "read display data mode " by executing the command 01011100b. The next byte is a dummy data. The GDDRAM data will be read form the second byte. The GDDRAM column address pointer will be increased by one automatically after each data read (8-levels gray scale mode) OR after each 3-bytes data read. (16-levels gray scale mode).

Graphic command table

Bit Pattern	Command	Description
$(D/\overline{C} = 0)$ 10000011 $(D/\overline{C} = 1)$ $A_7A_6A_5A_4A_3A_2A_1A_0$ $(D/\overline{C} = 1)$ $B_7B_6B_5B_4B_3B_2B_1B_0$ $(D/\overline{C} = 1)C_7C_6C_5C_4C_3C_2C_1C_0$ $(D/\overline{C} = 1)D_7D_6D_5D_4D_3D_2D_1D_0$ $(D/\overline{C} = 1)R_3R_2R_1R_0G_3G_2G_1G_0$ $(D/\overline{C} = 1)$ ****$B_3B_2B_1B_0$	Draw Line	Enter the "Draw line mode" by executing the command 10000011. The following four bytes (A_0 to A_7, B_0 to B_7, C_0 to C_7, D_0 to D_7) are used to specify the start coordinates of X address, start coordinates of Y address, end coordinates or X address and the end coordinates of Y address. The remaining two bytes are used to specify the color. *Remarks: $A \le 103$; $B \le 79$; $C \le 103$; $D \le 79$*
$(D/\overline{C} = 0)$ 10010010 $(D/\overline{C} = 1)$ *******A_0	Fill Enable/Disable	Enter the "Fill Enable/Disable mode" by executing the command 10010010. $A_0=0$: Filled color option is disabled (POR) $A_0=1$: Filled color option is enabled
$(D/\overline{C} = 0)$ 10000100 $(D/\overline{C} = 1)$ $A_7A_6A_5A_4A_3A_2A_1A_0$ $(D/\overline{C} = 1)$ $B_7B_6B_5B_4B_3B_2B_1B_0$ $(D/\overline{C} = 1)$ $C_7C_6C_5C_4C_3C_2C_1C_0$ $(D/\overline{C} = 1)$ $D_7D_6D_5D_4D_3D_2D_1D_0$ $(D/\overline{C} =1)$ $R_3R_2R_1R_0G_3G_2G_1G_0$ $(D/\overline{C} =1)$ ****$B_3B_2B_1B_0$ $(D/\overline{C} =1)$ $R_3R_2R_1R_0G_3G_2G_1G_0$ $(D/\overline{C} =1)$ ****$B_3B_2B_1B_0$	Draw rectangle	Enter the "Draw rectangle mode" by executing the command 10000100. The following four bytes (A_0 to A_7, B_0 to B_7, C_0 to C_7, D_0 to D_7) are used to specify the start coordinates of X address, start coordinates of Y address, end coordinates or X address and the end coordinates of Y address. The next two bytes are used to specify the color. The last two bytes are used to specify the fill color. *Remarks: $A \le C$; $B \le D$; $C \le 103$; $D \le 79$*
$(D/\overline{C} = 0)$ 10001010 $(D/\overline{C} = 1)$ $A_7A_6A_5A_4A_3A_2A_1A_0$ $(D/\overline{C} = 1)$ $B_7B_6B_5B_4B_3B_2B_1B_0$ $(D/\overline{C} = 1)$ $C_7C_6C_5C_4C_3C_2C_1C_0$ $(D/\overline{C} = 1)$ $D_7D_6D_5D_4D_3D_2D_1D_0$ $(D/\overline{C} = 1)$ $E_7E_6E_5E_4E_3E_2E_1E_0$ $(D/\overline{C} = 1)$ $F_7F_6F_5F_4F_3F_2F_1F_0$	Copy	Enter the "Copy mode" by executing the command. The following four bytes (A_0 to A_7, B_0 to B_7, C_0 to C_7, D_0 to D_7) are used to specify the start coordinates of X address, start coordinates of Y address, end coordinates or X address and the end coordinates of Y address. The remaining two bytes (E_0 to E_7, F_0 to F_7) are used to specify the new location of X coordinates and Y coordinates. *Remarks: $A \le C$; $B \le D$; $C \le 103$; $D \le 79$*
$(D/\overline{C} = 0)$ 10001100 $(D/\overline{C} = 1)$ $A_7A_6A_5A_4A_3A_2A_1A_0$ $(D/\overline{C} = 1)$ $B_7B_6B_5B_4B_3B_2B_1B_0$ $(D/\overline{C} = 1)$ $C_7C_6C_5C_4C_3C_2C_1C_0$ $(D/\overline{C} = 1)$ $D_7D_6D_5D_4D_3D_2D_1D_0$	Dim Window	Enter the "Dim Window mode" by executing the command 10001100. The following four bytes (A_0 to A_7, B_0 to B_7, C_0 to C_7, D_0 to D_7) are used to specify the start coordinates of X address, start coordinates of Y address, end coordinates or X address and the end coordinates of Y address. The selected window area will be dimmed by 75% white. *Remarks: $A \le C$; $B \le D$; $C \le 103$; $D \le 79$*
$(D/\overline{C} = 0)$ 10001110 $(D/\overline{C} = 1)$ $A_7A_6A_5A_4A_3A_2A_1A_0$ $(D/\overline{C} = 1)$ $B_7B_6B_5B_4B_3B_2B_1B_0$ $(D/\overline{C} = 1)$ $C_7C_6C_5C_4C_3C_2C_1C_0$ $(D/\overline{C} = 1)$ $D_7D_6D_5D_4D_3D_2D_1D_0$	Clear Window	Enter the "Clear Window mode" by executing the command 10001110. The following four bytes (A_0 to A_7, B_0 to B_7, C_0 to C_7, D_0 to D_7) are used to specify the start coordinates of X address, start coordinates of Y address, end coordinates or X address and the end coordinates of Y address. All GDDRAM content will be set to 0. *Remarks: $A \le C$; $B \le D$; $C \le 103$; $D \le 79$*

- *Remarks: "*" denote DON'T CARE bit*

- After executed the graphic command, waiting time is required for update GDDRAM content. (When V_{DD} = 2.4 ~ 3.6, waiting time = 125 ns/pixel.)

Extended command table

Bit Pattern	Command	Description
$(D/\overline{C} = 0)$ 1111 1011 $(D/\overline{C} = 1)$ ****0$B_2B_1B_0$	Set biasing ratio	Allow user to set bias from 1/4 to 1/8 $B_2B_1B_0$ Bias ratio 0 0 0 1/4 bias 0 0 1 1/5 bias 0 1 0 1/6 bias 0 1 1 1/7 bias (POR, if 68 Mux) 1 0 0 1/8 bias (POR, if 80 Mux) 1 0 1 reserved 1 1 X reserved
$(D/\overline{C} = 0)$ 1111 0010 $(D/\overline{C} = 1)$ 0000 $F_3F_2F_1F_0$ $(D/\overline{C} = 1)$ x00N_4 $N_3N_2N_1N_0$	Set Frame frequency and N-line Inversion	This command uses to change the frame frequency and set the N-line inversion. 68 Mux operation 80 Mux operation $F_3F_2F_1F_0$ $F_3F_2F_1F_0$ 1 1 1 1 : 110 Hz 1 1 1 1 : 93.5 Hz 1 1 1 0 : 102.5 Hz 1 1 1 0 : 87 Hz 1 1 0 1 : 97.5 Hz 1 1 0 1 : 82.5 Hz 1 1 0 0 : 92 Hz 1 1 0 0 : 78 Hz 1 0 1 1 : 88.5 Hz 1 0 1 1 : 75 Hz 1 0 1 0 : 84 Hz 1 0 1 0 : 71.5 Hz 1 0 0 1 : 81 Hz 1 0 0 1 : 69 Hz 1 0 0 0 : 78 Hz (POR) 1 0 0 0 : 66 Hz (POR) 0 1 1 1 : 76 Hz 0 1 1 1 : 64.5 Hz 0 1 1 0 : 73 Hz 0 1 1 0 : 62 Hz 0 1 0 1 : 70.5 Hz 0 1 0 1 : 60 Hz 0 1 0 0 : 68 Hz 0 1 0 0 : 58 Hz 0 0 1 1 : 66 Hz 0 0 1 1 : 56 Hz 0 0 1 0 : 64 Hz 0 0 1 0 : 54.5 Hz 0 0 0 1 : 62 Hz 0 0 0 1 : 53 Hz 0 0 0 0 : 60 Hz 0 0 0 0 : 51 Hz The second byte data sets the n-line inversion register from 2 to 32 lines to reduce display crosstalk. Register values from 00001b to 11111b are mapped to 2 lines to 32 lines respectively. Value 00000b disables the N-line inversion. 00110 is the POR value. To avoid a fix polarity at some lines, it should be noted that the total number of mux (including the icon line) should NOT be a multiple of the lines of inversion (n).
$(D/\overline{C} = 0)$ 1010001X_0	Enable/disable icon	X_0=0: Disable icon row (POR) X_0=1: Enable icon row
$(D/\overline{C} = 0)$ 1111 0111 $(D/\overline{C} = 1)$ 0010 1000 $(D/\overline{C} = 1)$ 0010 11X_1X_0 $(D/\overline{C} = 1)$ **** 0101	Select PWM/FRC	4 bits PWM/FRC or 2 bits PWM + 2 bits FRC selection X_1X_0 0 0 : 4 bits PWM 0 1 : 4 bits FRC 1 0 : 2 bits PWM + 2 bits FRC (POR) 1 1 : Reserved

Remarks: "" denote DON'T CARE bit*

Bit Pattern	Command	Description
($D/\overline{C}$ = 0) 1111 0110 ($D/\overline{C}$ = 1) 0001 $X_3X_2X_1X_0$ ($D/\overline{C}$ = 1) 0000 1010	OTP setting	This command set the offset value of contrast $X_3X_2X_1X_0$ 0000 : original contrast 0001 : original contrast + 2 step 0010 : original contrast + 4 steps 0011 : original contrast + 6 steps 0100 : original contrast + 8 steps 0101 : original contrast + 10 steps 0110 : original contrast + 12 steps 0111 : original contrast + 14 steps 1000 : original contrast - 16 steps 1001 : original contrast - 14 steps 1010 : original contrast - 12 steps 1011 : original contrast - 10 steps 1100 : original contrast - 8 steps 1101 : original contrast - 6 steps 1110 : original contrast - 4 steps 1111 : original contrast - 2 step
($D/\overline{C}$ = 0) 1111 1000	OTP programming	This command start to program LCD driver with OTP offset value. Each bit can be programmed to 1 once. Detail of OTP programming procedure on page 46

Remarks: "" denote DON'T CARE bit*

Table 6 - Read Command Table

Bit Pattern	Command	Description
($D/\overline{C}$ = 0 & $_{R/\overline{W}}$ = 0) 01011101 ($D/\overline{C}$ = 0 & $_{R/\overline{W}}$ = 1) D_7D_6 * $D_4D_3D_2D_1D_0$	Status Register Read	D_7D_6 = 00: Center Screen Scroll Mode D_7D_6 = 01: Top Screen Scroll Mode D_7D_6 = 10: Bottom Screen Scroll Mode D_7D_6 = 11: Whole Screen Scroll Mode D_4 = 0: Scan Direction is column direction D_4 = 1: Scan Direction is page direction D_3 = 0: Display is OFF D_3 = 1: Display is ON D_2 = 0: Sleep Mode is disabled D_2 = 1: Sleep Mode is enabled D_1 = 0: Display is Inverse D_1 = 1: Display is Normal D_0 = 0: Partial display is disabled D_0 = 1: Partial display is enabled

Note: Command patterns other than that given in Command Table are prohibited. Otherwise, unexpected result will occur.

Remarks: "" denote DON'T CARE bit*

8.1 Data Read / Write

To read data from the GDDRAM, 5Dhex command should be executed then input High to R/$\overline{W}$ ($\overline{WR}$) pin and D/$\overline{C}$ pin for 6800-series parallel mode. Low to E($\overline{RD}$) pin and High to D/$\overline{C}$ pin for 8080-series parallel mode. No data read is provided for serial mode. In normal mode, GDDRAM column address pointer will be increased by one automatically after each data read in 8-levels gray scale mode OR after each 3-bytes data read in 16-levels gray scale mode. Also, a dummy read is required before the first data is read. See Figure 3 in Functional Description.

To write data to the GDDRAM, input Low to R/$\overline{W}$ ($\overline{WR}$) pin and High to D/$\overline{C}$ pin for 6800-series parallel mode. For serial interface, it will always be in write mode. GDDRAM column address pointer will be increased by one automatically after each data write in 8-levels gray scale mode OR each 3-bytes data write in 16-levels scale mode. The address will be reset to 0 in next data read/write operation is executed when it is 103.

9 COMMAND DESCRIPTIONS

9.1 Set Column Address

This command specifies the 8-bit column address of the display data RAM. The start and the end column address are specified by this command. The driver supports up to 104 columns. As the addresses are incremented from the start column to the end column in the column direction scan, the page address is automatically incremented by 1. The column address is then returned to the start column. The column address will be increased by each data access after it is preset by the MCU. Start column < End column must be maintained.

	RGB Alignment using 8-levels gray scale mode																								
		Column																							
	P11 = 0	0			1			2			3				101			103							
	P11 = 1	103			102			101			100				1			0							
LCD Read Direction	Color	R	G	B	R	G	B	R	G	B	R	G	B		R	G	B	R	G	B			COMMON OUTPUTS		
	Data	D7	D4	D1	D7	D4	D1	D7	D4	D1	D7	D4	D1		D7	D4	D1	D7	D4	D1					
	Page	D6	D3	D0	D6	D3	D0	D6	D3	D0	D6	D3	D0		D6	D3	D0	D6	D3	D0					
BLOCK	P10 = 0 / P10 = 1	D5	D2		D5	D2		D5	D2		D5	D2			D5	D2		D5	D2						
0	0 / 79																						COM0		
	1 / 78																						COM1		
	2 / 77																						COM2		
	3 / 76																						COM3		
1	4 / 75																						COM4		
	5 / 74																						COM5		
	6 / 73																						COM6		
	7 / 72																						COM7		
:	: / :																						:		
17	68 / 11																						COM68		
	69 / 10																						COM69		
	70 / 9																						COM70		
	71 / 8																						COM71		
18	72 / 7																						COM72		
	73 / 6																						COM73		
	74 / 5																						COM74		
	75 / 4																						COM75		
19	76 / 3																						COM76		
	77 / 2																						COM77		
	78 / 1																						COM78		
	79 / 0																						COM79		
20	ICON / ICON																						ICON		
SEGMENT OUTPUTS		COL0	COL1	COL2	COL3	COL4	COL5	COL6	COL7	COL8	COL9	COL10	COL11	....	COL306	COL307	COL308	COL309	COL310	COL311					

Table 7 - RAM arrangements of 8-levels gray scale mode

RGB Alignment using 16-levels gray scale mode

			Column																			
	P11 = 0		0			0			1			1						51			51	
	Color		R1	G1	B1	R2	G2	B2	R1	G1	B1	R2	G2	B2			R1	G1	B1	R2	G2	B2
LCD Read Direction	Data / Page		D7 D6 D5 D4	D3 D2 D1 D0	D7 D6 D5 D4	D3 D2 D1 D0	D7 D6 D5 D4	D3 D2 D1 D0	D7 D6 D5 D4	D3 D2 D1 D0	D7 D6 D5 D4	D3 D2 D1 D0	D7 D6 D5 D4	D3 D2 D1 D0			D7 D6 D5 D4	D3 D2 D1 D0	D7 D6 D5 D4	D3 D2 D1 D0	D7 D6 D5 D4	D3 D2 D1 D0
	P11 = 1		51			51			50			50						0			0		
	Color		R2	G2	B2	R1	G1	B1	R2	G2	B2	R1	G1	B1			R2	G2	B2	R1	G1	B1
	Data / Page		D3 D2 D1 D0	D7 D6 D5 D4	D3 D2 D1 D0	D7 D6 D5 D4	D3 D2 D1 D0	D7 D6 D5 D4	D3 D2 D1 D0	D7 D6 D5 D4	D3 D2 D1 D0	D7 D6 D5 D4	D3 D2 D1 D0	D7 D6 D5 D4			D3 D2 D1 D0	D7 D6 D5 D4	D3 D2 D1 D0	D7 D6 D5 D4	D3 D2 D1 D0	D7 D6 D5 D4	COMMON OUTPUTS

BLOCK	P10 = 0	P10 = 1																					COMMON OUTPUTS
0	0	79																					COM0
	1	78																					COM1
	2	77																					COM2
	3	76																					COM3
1	4	75																					COM4
	5	74																					COM5
	6	73																					COM6
	7	72																					COM7
⋮	⋮	⋮											⋮										⋮
17	68	11																					COM68
	69	10																					COM69
	70	9																					COM70
	71	8																					COM71
18	72	7																					COM72
	73	6																					COM73
	74	5																					COM74
	75	4																					COM75
19	76	3																					COM76
	77	2																					COM77
	78	1																					COM78
	79	0																					COM79
20	ICON	ICON																					ICON

SEGMENT OUTPUTS: COL0 COL1 COL2 COL3 COL4 COL5 COL6 COL7 COL8 COL9 COL10 COL11 ……….. COL306 COL307 COL308 COL309 COL310 COL311

Table 8 - RAM arrangements of 16-levels gray scale mode

9.2 Set Page Address

This command enters the page address from 0 to 79 to the RAM page register for read/write operations. The driver supports up to 80 lines. All in all, there are 80 pages. As the addresses are incremented from the start page to the end page in the page direction scan, the column address is incremented by 1. The page address is then returned to the start page. Start page < End page must be maintained.

9.3 Set COM Output Scan Direction

This command sets the scan direction of the COM output allowing layout flexibility in LCD module assembly. Please refer to the Table 5 on Page 22 for detail mapping. In addition, the display will have immediate effect once this command is issued. That is, if this command is sent during normal display, the graphic display will have vertical flipping effect.

9.4 Set Data Output Scan Direction

This command sets the DDRAM such that the MPU operates the display data in the internal RAM.

A. Normal or Inverse page/column/scan directions
The Data Scan direction can be set to either normal or inverse display page and column address scan direction. The column and the page direction are illustrated in the Figure 7 on page 32.

$\text{MUX68}/\overline{80} = 0$

P12 = 0: Column Direction

P11=0		0	1	2		101	102	103
P11=1		103	102	101		2	1	0
P10=0	P10=1							
0	79							
1	78							
2	77							
⋮	⋮			⋮		⋮		
77	2							
78	1							
79	0							

P12 = 1: Page Direction

P11=0		0	1	2		101	102	103
P11=1		103	102	101		2	1	0
P10=0	P10=1							
0	79							
1	78							
2	77							
⋮	⋮			⋮		⋮		
77	2							
78	1							
79	0							
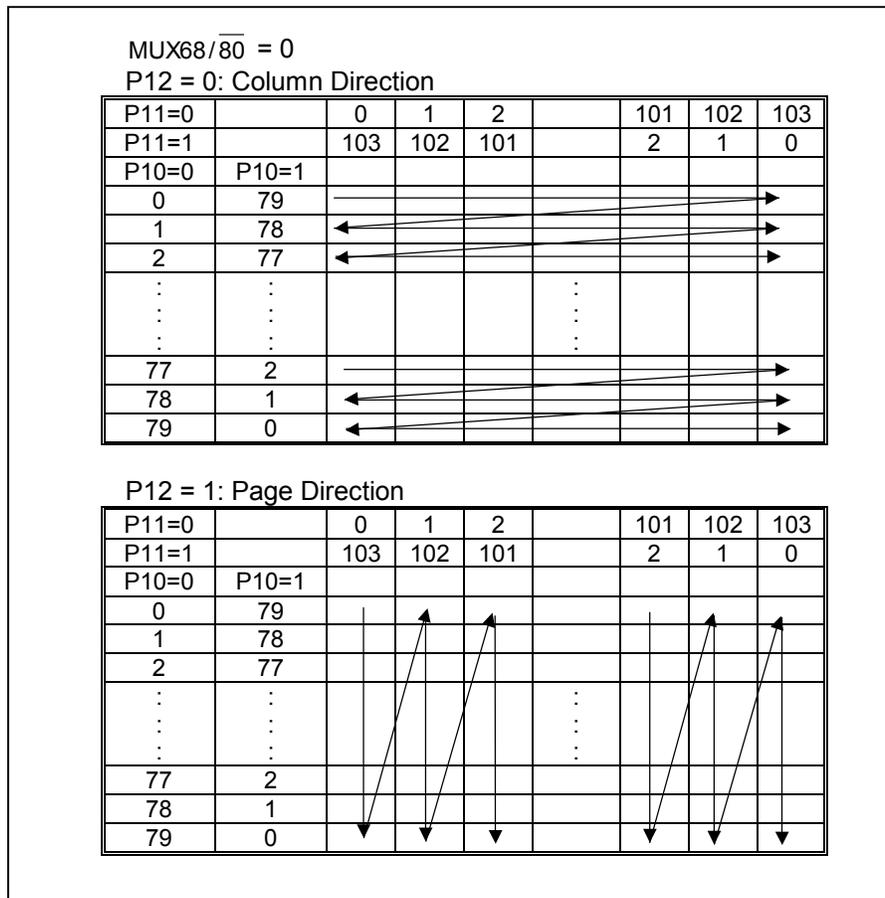
Figure 7 - column and page scan direction of 8-level gray scale mode

MUX68/$\overline{80}$ = 0
P12 = 0: Column Direction

P11=0		0	0	1		50	51	51
P11=1		51	51	50		1	0	0
P10=0	P10=1							
0	79							
1	78							
2	77							
⋮	⋮				⋮			
77	2							
78	1							
79	0							

P12 = 1: Page Direction

P11=0		0	0	1		50	51	51
P11=1		51	51	50		1	0	0
P10=0	P10=1							
0	79							
1	78							
2	77							
⋮	⋮				⋮			
77	2							
78	1							
79	0							
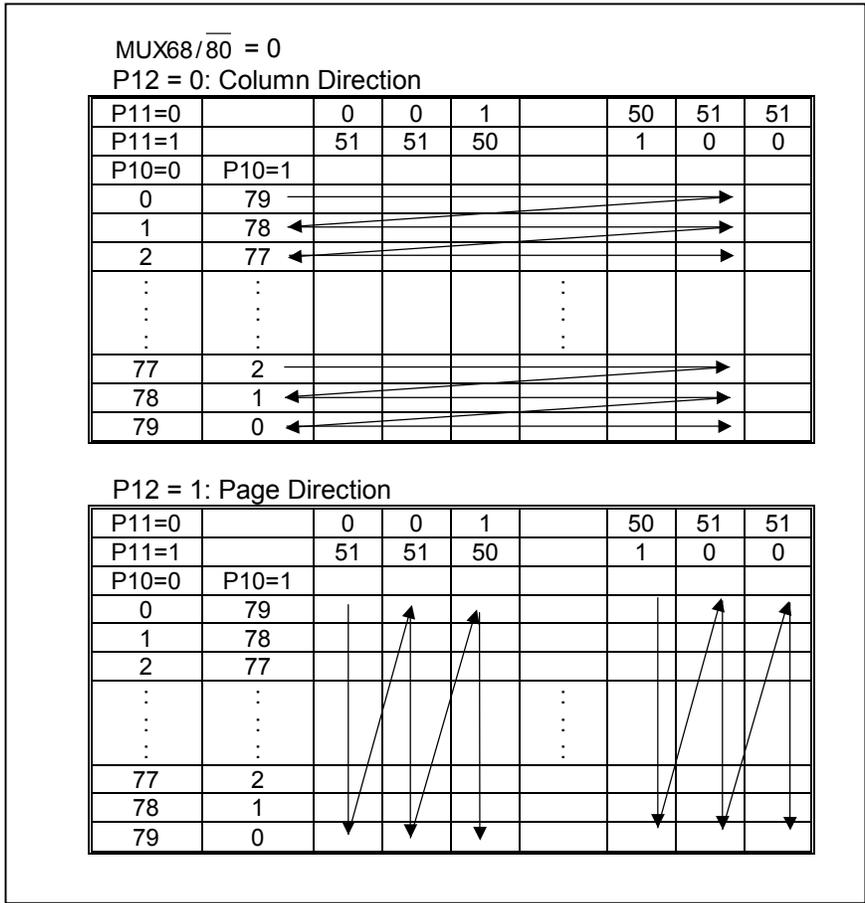
Figure 8 - column and page scan direction of 16-level gray scale mode

P10 = 0　　P10 = 1　　P10 = 0　　P10 = 1
P11 = 0　　P11 = 0　　P11 = 1　　P11 = 1
P12 = 0　　P12 = 0　　P12 = 0　　P12 = 0

P10 = 0　　P10 = 1　　P10 = 0　　P10 = 1
P11 = 0　　P11 = 0　　P11 = 1　　P11 = 1
P12 = 1　　P12 = 1　　P12 = 1　　P12 = 1
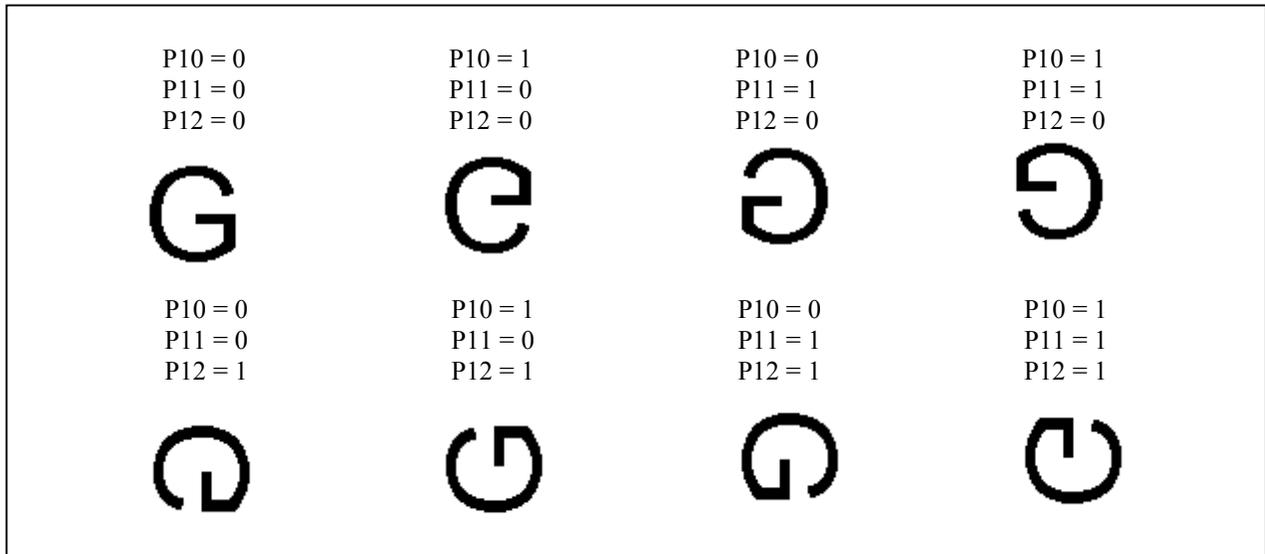
Figure 9 – Example of Normal or Reverse page/column/ scan directions

The parameters following the command set data output scan direction specifies the RGB arrangement and the selection of various gray-scale modes. Please find the information of the RGB arrangement and the gray scale mode in the following section.

B. RGB arrangement mode
The RGB arrangement mode can be selected according to the following table. Three selection bits will give eight combinations of the RGB arrangements. Each combination set will specify the Red, Green and Blue segment output arrangement in odd and even page.

P22, P21, P20	LINE	COL0	COL1	COL2	COL3	COL4	COL5	COL6	COL7	…	COL311
000	Even page	R	G	B	R	G	B	R	G	…	B
	Odd page	R	G	B	R	G	B	R	G	…	B
001	1	B	G	R	B	G	R	B	G	…	R
	2	B	G	R	B	G	R	B	G	…	R
010	1	R	G	B	B	G	R	R	G	…	R
	2	R	G	B	B	G	R	R	G	…	R
011	1	B	G	R	R	G	B	B	G	…	B
	2	B	G	R	R	G	B	B	G	…	B
100	1	R	G	B	R	G	B	R	G	…	B
	2	B	G	R	B	G	R	B	G	…	R
101	1	B	G	R	B	G	R	B	G	…	R
	2	R	G	B	R	G	B	R	G	…	B
110	1	R	G	B	B	G	R	R	G	…	R
	2	B	G	R	R	G	B	B	G	…	B
111	1	B	G	R	R	G	B	B	G	…	B
	2	R	G	B	B	G	R	R	G	…	R

Table 9 - RGB Arrangement modes

C. Gray scale mode
The gray scale mode can be selected according to the following table. Two types of gray scale mode such that the device can display between 256 colors or 4096 colors.

P32	P31	P30	Numbers of Gary-scale
0	0	1	8 gray-scale mode
0	1	0	16 gray-scale mode

Table 10 - Gray scale selection mode

R(D7, D6, D5)	Black (0, 0, 0)	------- (0,0,1)	------- (0,1,0)	------- (0,1,1)	------- (1,0,0)	------- (1,0,1)	------- (1,1,0)	------- (1,1,1)		Red

R(D7, D6, D5) Black (0, 0, 0)   (0,0,1)   (0,1,0)   (0,1,1)   (1,0,0)   (1,0,1)   (1,1,0)   (1,1,1)   Red

G(D4, D3, D2) Black (0, 0, 0)   (0,0,1)   (0,1,0)   (0,1,1)   (1,0,0)   (1,0,1)   (1,1,0)   (1,1,1)   Green

B(D1, D0) Black (0, 0)   (0,1)   (0,1)   (0,1)   (1,0)   (1,0)   (1,0)   (1,1)   Blue

Any one of above   Any one of above

Figure 10 - Examples: 8 gray-scale display arrangement

Description of different gray-scale display
8-gray-scale display:
Figure 7 on page 32 shows the arrangement of the display data. The data D7, D6, D5, D4, D3, D2, D1, D0 (RRRGGGBB) is converted into 4-bits data (RRRRGGGGBBBB). The 4-bits data is then stored into the GDDRAM.

16-gray-scale display:
Figure 8 on page 33 shows the arrangement of the display data. The data D7, D6, D5, D4, D3, D2, D1, D0 is encoded and write into the GDDRAM in three operation cycles.

D7, D6, D5, D4, D3, D2, D1, D0: R1, R1, R1, R1, G1, G1, G1, G1 (1ST write)

D7, D6, D5, D4, D3, D2, D1, D0: B1, B1, B1, B1, R2, R2, R2, R2 (2ND write)

D7, D6, D5, D4, D3, D2, D1, D0: G2, G2, G2, G2, B2, B2, B2, B2 (3RD write)

9.5   Set Color Look Up Table

This command transforms the display data (R: 3 bits, G: 3 bits, B: 2 bits) into 4-bit data. The 4 bit data will then be stored into the GDDRAM by choosing colors to represent red, green and blue from 4096 colors. When the GDDRAM output the data, the red, green and blue data are converted back to 8 bit data (R: 3 bits, G: 3 bits, B: 2 bits). The Color Look-up Table must be set when using 8-levels gray scale mode.

9.6   Set Display Control

This command is used to select the duty ratio of the IC. All available driving duty can be selected using this command. The driving duty can be changed from 1/8 to 1/80 (exclude ICON).

9.7   Set Area Scroll

This command specifies the portion of screen for scrolling. The command sets the starting block address, finishing block address, number of specific blocks and the area scroll mode of the area scrolling. Please be noted that the starting block address should be smaller than the finishing block address.

The block address increment direction is started at 0th block such that the GDDRAM address corresponds to the top of the fixed area. Similarly, the block address decrement direction is started at the 19th block such that the GDDRAM address corresponds to the bottom fixed area. The remaining block address excluding the top and the bottom fixed areas are assigned to the scroll plus the background areas.
The set area scroll function is divided into four parts.

Part I -Specify the top block address of the scroll + the background areas. Specify the 0th block for the top screen scroll or the whole screen scroll. The scroll start block address is also set at this top block address until the scroll start set command is executed.

Part II – Specify the bottom address of the scroll + background areas. Specify the 19th block for the bottom or the whole screen scroll.

Part III – Specify number of scrolled blocks = number of (Top fixed area + scroll area) blocks – 1. When the bottom scroll or whole screen scroll is chosen, the resulted value is identical to the value stated in part II.

Part IV
Specify the area scroll type. Altogether there are four types of area scroll. Please refer to Table 11 for detail.

P41	P40	Types of Area Scroll
0	0	Center Screen Scroll
0	1	Top Screen Scroll
1	0	Bottom Screen Scroll
1	1	Whole Screen Scroll

Table 11 - Area scrolling selection modes
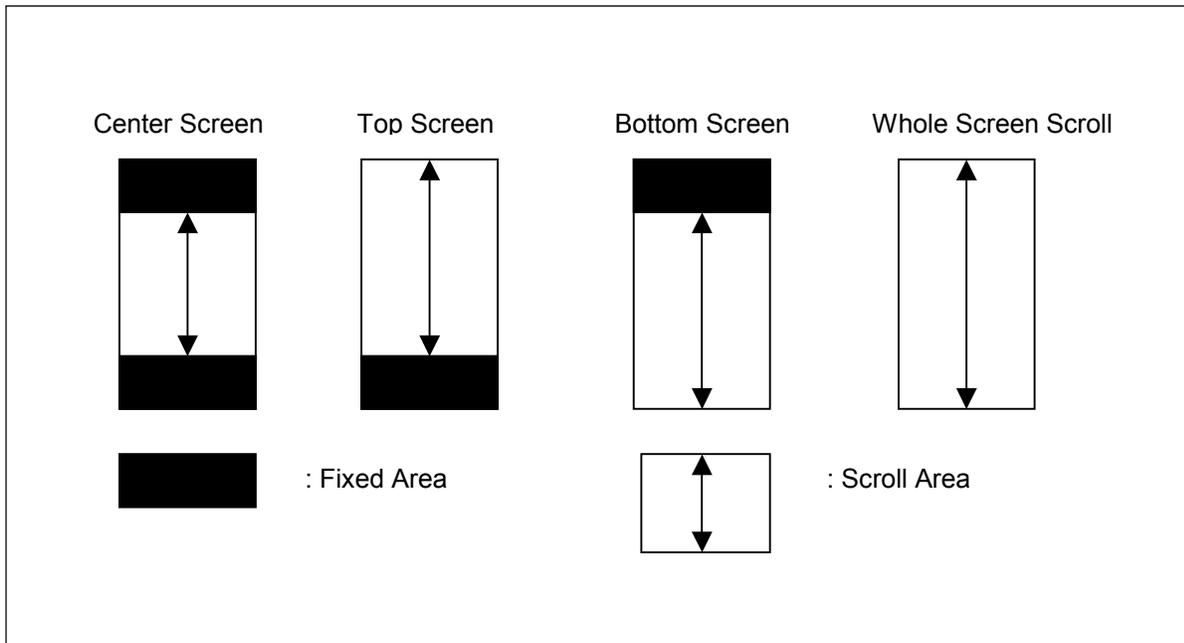
Figure 11 - Area scrolling selection modes

The area scroll function is executed by prompt in the set area scroll command following by changing the start block address by the set scroll start command. Figure 11 illustrates the operation model of the scrolling function.

Example: In the Center screen scroll of 1/64 duty (display range: 64 lines = 16 blocks)

Description	Command	Data
- Set Area Scroll	AAH	
- 8 lines (block 0 & block 1) are specified for the top fixed area		
- The Top Block Address = Number of the top fixed area		
= 8 / 4		02H
- 8 lines (block 18 & block 19) are specified for the bottom fixed area		
- The Specified Bottom Block Address		
= Bottom Block Address + Number of Background area		
= 13 + (16 / 4) = 17 (11Hex)		11H
- 48 lines (block 2 to block 13) are specified the scroll area		
- Number of Specified Block		
= Top fixed area + Scroll Area – 1		
= (8 / 4) + (48 / 4) – 1 = 13 (0DHex)		0DH
- 16 lines (block 14 to block 17) are specified the background area		
- Set area scroll mode – Center screen mode		00H
- Set Scroll start (Scroll range form 02H ~ 11H)	ABH	
		02H
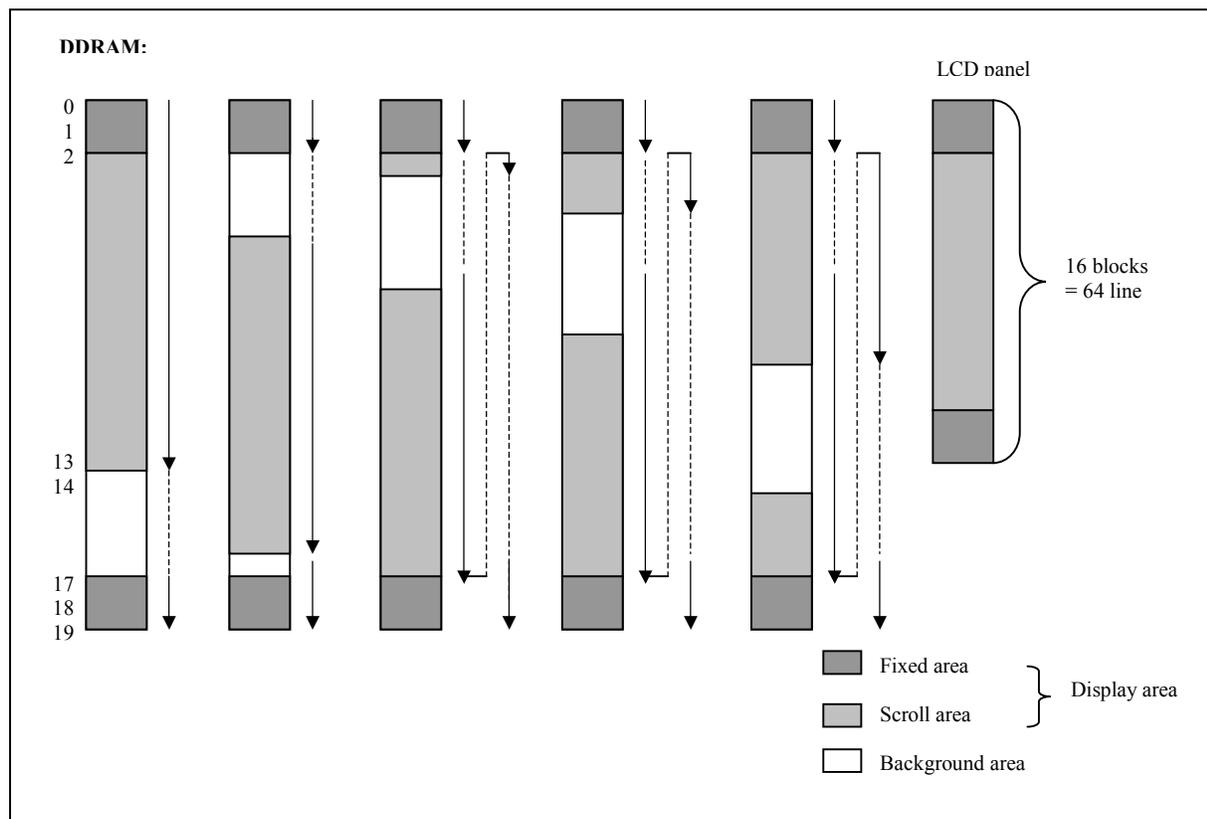
Figure 12 - GDDRAM updates for area scrolling

104 RGB X 80 Line GDDRAM Content

Top Fix Area

Scroll Area

Background Area

Bottom Fix Area

Block

104 RGB X 64 lines Panel

COM0

0
1
2
3
:
:
:
12
13
18
19

Scroll Start = 2

COM63
COM0

0
1
3
4
:
:
:
13
14
18
19

Scroll Start = 3

COM63
COM0

0
1
Scroll Start 4
= 4   5
:
:
14
15
18
19

COM63
COM0

0
1
8
9
:
2
3
18
19

Scroll Start = 8

COM63

Example Program of Specified Center Scroll mode.

Void center_scroll(void)
{
//Set 1/64 Duty
Comm_out (0xCA);
Data_out (0x00);
Data_out (0x0F);
Data_out(0x00);
//Set Area Scroll
Comm_out(0xAA);
Data_out(0x02);   // Top Block Address
Data_out(0x11);   // Specified Bottom Block Address
Data_out(0x0D);   //Number of Specified Block
Data_out(0x00);   //Center Screen Mode
//Set Scroll Start
for (I=0x02; I<=0x11; I++)
* {*
* Comm_out(0xAB); //set scroll start*
* Data_out(I);*
* Delay (200);   //delay 200ms*
* }*
}

Figure 13 – Example of Specified Center Scroll Mode

9.8   Set Scroll Start

This command specifies the starting block address of the area scrolling and then executes the area scroll by changing the start block address dynamically. Start block < End block must be maintained. Please be noted that the set scroll start command should be executed after the set area scroll command.

9.9   Set Power Control Register

This command turns on/off the various power circuits associated with the chip. There are three power sub-circuits (reference voltage generator, internal regulator and voltage follower) could be turned on/off by this command. In addition, the configuration of the internal primary booster (3X/4X/5X/6X) can be selected by this command.

9.10 Set Contrast Level & Internal Regulator Ratio

This command adjusts the contrast of the LCD panel by changing the LCD driving voltage, V_{OUT}, provided by the On-Chip power circuits. V_{OUT} is set with 64 steps (6-bit) in the contrast control register by a set of compound commands. Please refer to the Figure 14 for the contrast control process flow diagram.
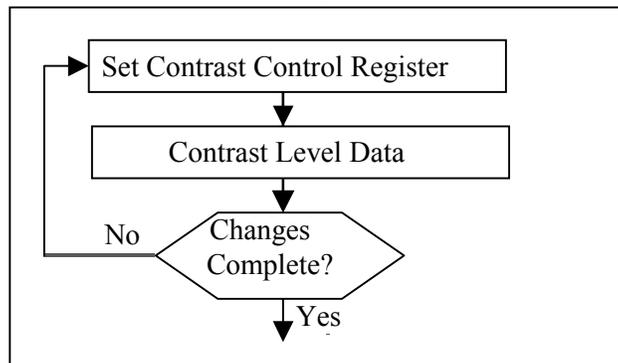
Figure 14 - Contrast Control Flow Set Segment Re-map

This command also sets the feedback gain of the internal regulator. There are altogether 8 internal regulator gains, which are used for the adjustment of V_{OUT} level. This command is to enable any one of the eight internal resistor (IRS) settings for different regulator gains when using internal regulator resistor network. The Contrast Control Voltage Range curves is referred to the following formula:

$$V_{out} = \left(1 + \frac{R_2}{R_1}\right) * V_{con}$$

$$V_{con} = \left(1 - \frac{63 - \alpha}{210}\right) * V_{ref}$$

$$, where\ Vref = 1.7V$$

Remarks: TC = -0.25%/^oC
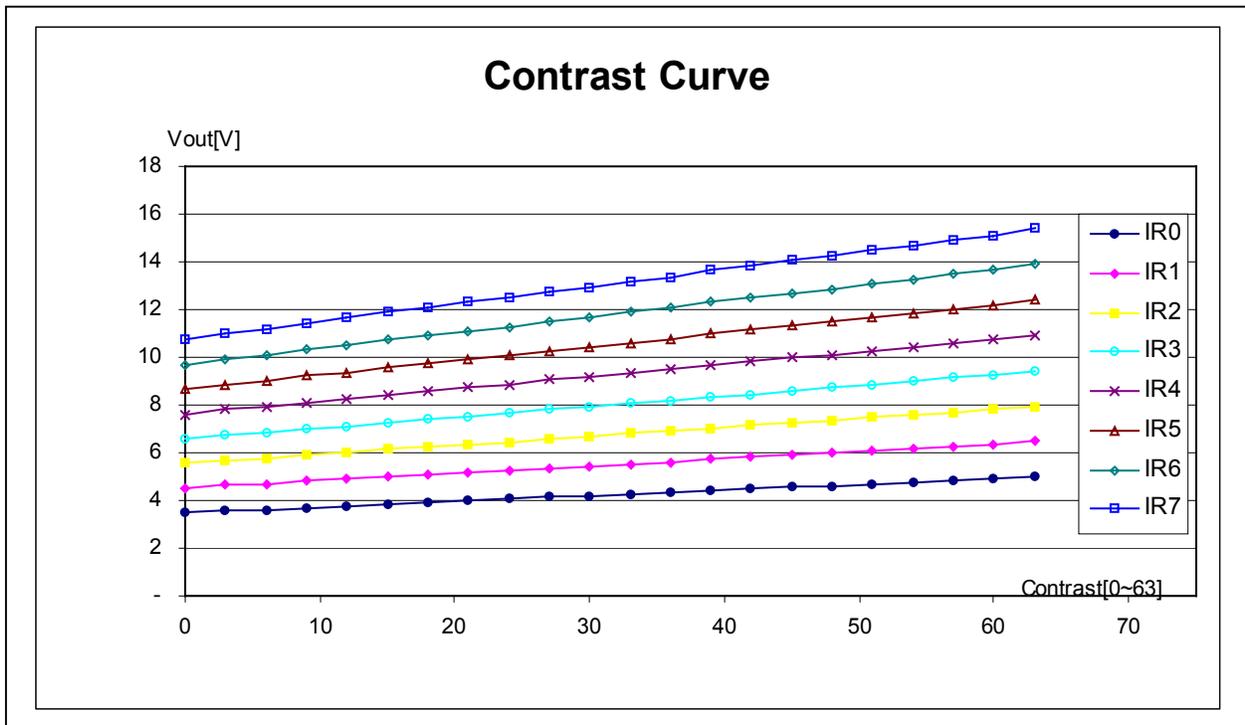
Contrast Curve

Figure 15 - Contrast Control Voltage Range Curve (V$_{DD}$ =2.7V; V$_{CI}$ =3V; Booster level = 6X; TC = -0.25%/^{o}C)

Note: The Maximum operation voltage of V$_{OUT}$ is 12.5V with panel load.

9.11 Set Increment/Decrement of the contrast set

This command can increase the contrast step by +1 and decrease the contrast set by –1. It is the most convenient way to change the contrast of the display by programming.

9.12 Set Normal/Inverse Display

This command turns the display to be either normal or inverse. In normal display mode, a RAM data of 1 indicates an illumination on the corresponding pixel in the normal white panel. In inverse display mode, a RAM data of 0 will turn on the pixel. It should be noted that the icon line is not affected. The icon line is not inversed by this command.

Example:

For a normal White display panel (Set Normal Display: A6Hex):

RAM Content			Color
R	G	B	
F	F	F	White
0	0	0	Black
F	0	0	Red
0	F	0	Green
0	0	F	Blue

For a normal Black display panel (Set Normal Display: A7Hex):

RAM Content			Color
R	G	B	
F	F	F	White
0	0	0	Black
F	0	0	Red
0	F	0	Green
0	0	F	Blue

9.13 Enter Partial Display

This command and the following parameters specify the display area of the partial display mode. The following figure shows the display and non-display area when the partial display mode is executed.
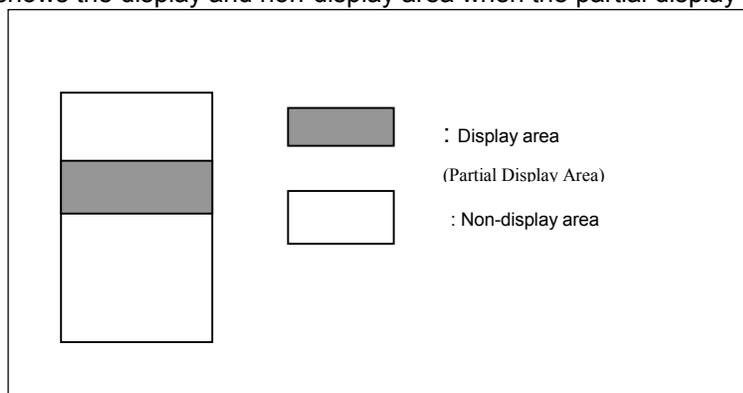
Figure 16 - Partial display mode

9.14 Exit Partial Display

This command exits the partial display mode.

9.15 Set Display On/Off

This command is used to turn the display on or off. When display off is issued with entire display is on, power save mode will be entered.

9.16 Enter/Exit sleep mode

This command enter/exit the sleep mode.

9.17 Enable/Disable the internal oscillator

This command enables or disables the internal oscillator. The internal oscillator is turned off after hardware or software reset.

9.18 Set Temperature compensation coefficient

This command sets the average temperature gradients. Four sets of average temperature gradients can be selected. Please refer to the command table for detail description of the average temperature gradients. The default value of the temperature gradient is $-0.2 \%/^{0}C$

9.19 NOP

A command causing the chip takes No Operation.

9.20 Write display data mode

This command is used to execute the write display data mode. The display data byte is directly written to the GDDRAM. Please be noted that the $D/\overline{C}$ signal should be set to high during the display data is written to the GDDRAM.

9.21 Read display data mode

This command is used to execute the read display data mode. The display data byte is directly red from the GDDRAM. Please be noted that the D/$\overline{C}$ signal should be set to high during the display data is read from to the GDDRAM.

Graphic Command

9.22 Draw Line

Given the starting point (X1, Y1) and the ending point (X2, Y2), a line will be drawn with the color specified.
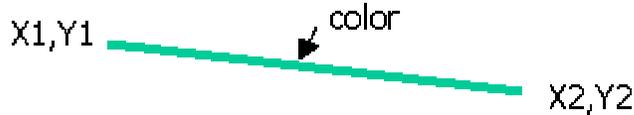
The following example illustrates the line drawing procedure.
1. Enter the "draw line mode" by execute the command 83H
2. Set the starting X-coordinates, X1. E.g., 00H.
3. Set the starting Y-coordinates, Y1. E.g., 00H.
4. Set the finishing X-coordinates, X2. E.g., 01H
5. Set the finishing Y-coordinates, Y2. E.g., 01H
6. Set the color to RGB = (0,1,0) e.g., 0FH following by 00H

Result: A color line will be drawn between coordinates (0,0) and (1,1)

Remarks: X1 $\leq$ 103; X2 $\leq$ 103; Y1 $\leq$ 79; Y2 < 79

9.23 Fill Enable/Disable

This command allows the fill color option to be enabled or disabled. This command is applicable to the Draw Rectangle feature. When the selection bit is "0", the fill color option is disabled. When the selection bit is "1", the fill color option is enabled.

9.24 Draw rectangle

Given the starting point (X1, Y1) and the ending point (X2, Y2), specify the width and height of a rectangle that will be drawn with the color specified. Remarks: If fill color option is disabled, the enclosed area will not be filled.
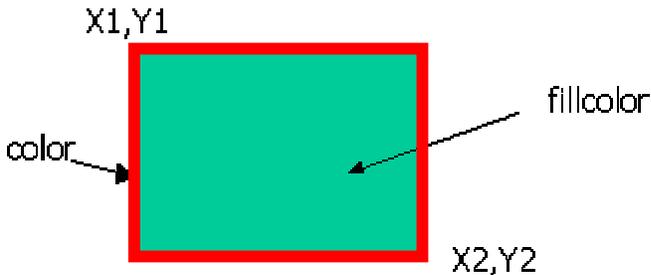
The following example illustrates the rectangle drawing procedure.
1. Enter the "draw rectangle mode" by execute the command 8AH
2. Set the starting X-coordinates, X1. E.g., 00H.
3. Set the starting Y-coordinates, Y1. E.g., 00H.
4. Set the finishing X-coordinates, X2. E.g., 02H
5. Set the finishing Y-coordinates, Y2. E.g., 02H
6. Set the color to RGB = (1,0,0) e.g., F0H following by 00H
7. Set the filled color to RGB = (0,1,0) e.g., 0FH following by 00H

Result: A filled color square will be drawn with the coordinates of the top left hand corner at (0,0) and the coordinates of the bottom right hand corner at (2,2)

Remarks: X1 $\leq$ X2; Y1 $\leq$ Y2; X2 $\leq$ 103; Y2 $\leq$ 79

9.25 Copy

Copy the rectangular region defined by the starting point (X1, Y1) and the ending point (X2, Y2) to location (X3, Y3). There are two possible results with the command copy executed depending on the setting of the start point coordinates and end point coordinates.

The following example illustrates the copy procedure.

X1,Y1

X2,Y2
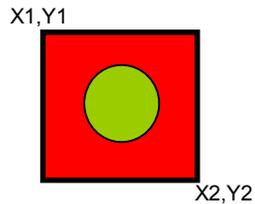
Case 1 – The overlap region will superimpose.
1. Enter the "copy mode" by execute the command 84H
2. Set the starting X-coordinates, X1. E.g., 00H.
3. Set the starting Y-coordinates, Y1. E.g., 00H.
4. Set the finishing X-coordinates, X2. E.g., 02H
5. Set the finishing Y-coordinates, Y2. E.g., 02H
6. Set the New X-coordinates, X3. E.g., 01H
7. Set the New Y-coordinates, Y3. E.g., 01H

X1,Y1

X3,Y3

X2+X3,
Y2+Y3
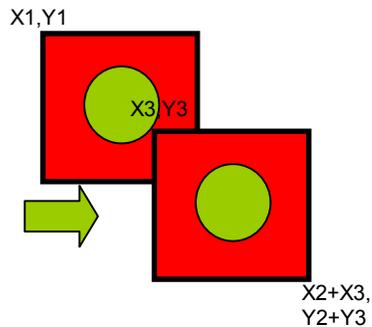
Case 2 – The original GDDRAM content remains unchanged
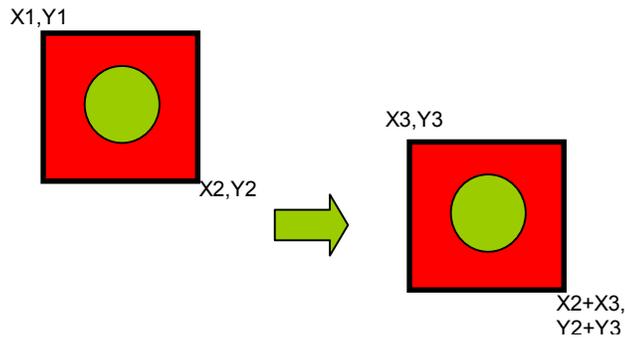
1. Enter the "copy mode" by execute the command 84H
2. Set the starting X-coordinates, X1. E.g., 00H.
3. Set the starting Y-coordinates, Y1. E.g., 00H.
4. Set the finishing X-coordinates, X2. E.g., 01H
5. Set the finishing Y-coordinates, Y2. E.g., 01H
6. Set the New X-coordinates, X3. E.g., 09H
7. Set the New Y-coordinates, Y3. E.g., 09H

Remarks: $X1 \leq X2$; $Y1 \leq Y2$; $X2 \leq 103$; $Y2 \leq 79$

9.26 Dim Window

This command will dim the window area specify by starting point (X1, Y1) and the ending point (X2, Y2). After the execution of this command, the selected window area will be dimmed by 75% white. Additional execution of this command over the same window area will not change the data content.

Remarks: $X1 \leq X2$; $Y1 \leq Y2$; $X2 \leq 103$; $Y2 \leq 79$

9.27 Clear Window

This command sets the window area specify by starting point (X1, Y1) and the ending point (X2, Y2) to clear the window display. The GDDRAM content of the window will be set to zero.

Remarks: $X1 \leq X2$; $Y1 \leq Y2$; $X2 \leq 103$; $Y2 \leq 79$

Extended Command

9.28 Set biasing ratio

This command selects a suitable bias ratio (1/4 to 1/8) required for driving the particular LCD panel in use.

9.29 Set Frame Frequency

This command specifies the frame frequency so as to minimize the flickering due to the ac main frequency. The frequency is set to 78Hz after POR.

9.30 Set N-line inversion

Number of line inversion is set by this command for reducing crosstalk noise. 2 to 32-line inversion operations could be selected. At POR, this operation is set to 0110b (7 lines). It should be noted that the total number of mux (including the icon line) should NOT be a multiple of the inversion number (n). Or else, some lines will not change their polarity during frame change.

9.31 Enable/disable icon

This command enable/disable the Icon display.

9.32 Select PWM/FRC

This command set the Pulse Width Modulation, Frame Rate Control or mix of FWM & FRC.

9.33 OTP setting and programming

OTP (One Time Programming) is a method to adjust V_{OUT}. In order to eliminate the variations of LCD module in terms of contrast level, OTP can be used to fine-tune the contrast of every LCD modules. Each OTP bit can be programmed to '1' once.

OTP setting and programming should include two major steps. Find the OTP offset and OTP programming as following,

Step 1. Find OTP offset

(1) Hardware Reset (sending an active low reset pulse to $\overline{\text{RES}}$ pin)
(2) Send original initialization routines
(3) Set and display any test patterns
(4) Adjust the contrast value (C:0x81, D:0x00~0x3F, D: 0x00 ~ 0x07) until there is the best visual contrast
(5) OTP setting steps = Contrast value of the best visual contrast - Contrast value of original initialization

Example 1:
Contrast value of original initialization = 0x20
Contrast value of the best original initialization = 0x24
OTP offset value = 0x24 - 0x20 = +4
OTP setting command should be (C: 0xF6, D: 0x12, D: 0x0A)

Example 2:
Contrast value of original initialization = 0x20
Contrast value of the best original initialization = 0x1B
OTP setting = 0x1B - 0x20 = -6
OTP setting command should be (C:0xF6, D: 0x1D, D: 0x0A)

Step 2. OTP programming

(6) Hardware Reset (sending an active low reset pulse to $\overline{\text{RES}}$ pin)
(7) Enable Oscillator (C: 0xD1) and Exit Sleep Mode (C: 0x94)
(8) Connect an external V_{OUT} (see diagram below)
(9) Send OTP setting commands that we find in step 1 (C: 0xF6, D: 0x10~0x1F, D: 0x0A)
(10) Send OTP programming command (C: 0xF8)
(11) Wait at least 2 seconds
(12) Hardware Reset
(13) Verify the result by repeating step 1. (2) – (3)
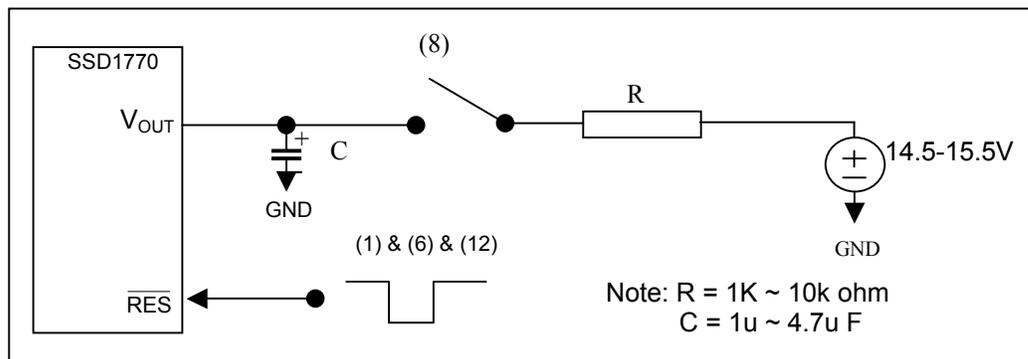
Figure 17 – OTP programming circuitry
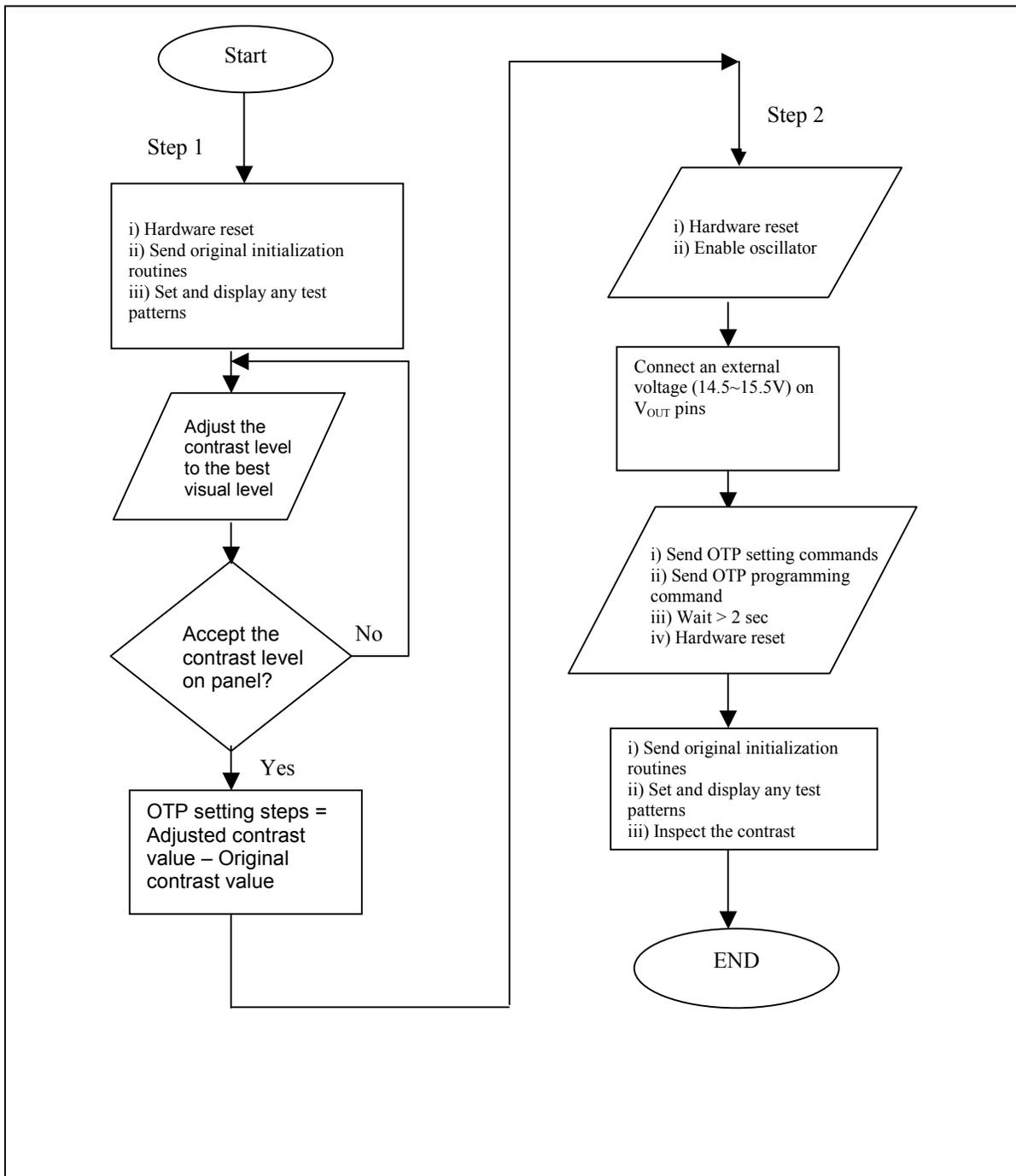
Figure 18 – Flow chart of OTP programming Procedure

OTP Example program

Find the OTP offset:
1. Hardware reset by sending an active low reset pulse to $\overline{RES}$ pin

2. COMMAND(0XD1);   \\Enable oscillator;

    COMMAND(0X94);   \\ exit sleep mode;

3. COMMAND(0X20);   \\ turn on the reference voltage generator, internal regulator and voltage follower; Select booster level.

    DATA(0X0B);

4. COMMAND(0XCA)   \\ Set Duty ratio

    DATA(0X10)   \\ 68Mux ([68 / 4] –1 = 16(decimal) / 10(Hex))

    COMMAND(0XF7)   \\ Set PWM/FRC

    DATA(0X28)   \\ pure PWM

    DATA(0X2C)

    DATA(0X05)

    COMMAND(0XFB)   \\ Set Biasing ratio

    DATA(0X3)   \\ 1/7

5. COMMAND(0X81)   \\Set target gain and contrast.

    DATA(0X14)   \\ contrast = 20

    DATA(0X05)   \\ IR5 => gain = 7.16

6. \\ Set target display contents

    COMMAND(0X15)   \\ set column address

    DATA(0x00)   \\ set start column address at 0

    DATA(0X67)   \\ set end column address at 103

    COMMAND(0X75)   \\ set page address

    DATA(0X00)   \\ set start page address at 0

    DATA(0X43)   \\ set end page address at 67

    COMMAND(0X5C)   \\ write target content to GDDRAM

    DATA(…)

    COMMAND(0xAF)   \\ display on

7. OTP offset calculation… target OTP offset value is +6

OTP programming:
8. Hardware reset by sending an active low reset pulse to $\overline{RES}$ pin

9. COMMAND(0XD1)   \\ Enable Oscillator

10. COMMAND(0x94)   \\ Exit Sleep Mode

11. Connect a external V_{OUT} (14.5V~15.5V)

12. COMMAND(0XF6)   \\ Set OTP offset value to +6 (0011)

    DATA(0X13)   \\ 0001 $X_3X_2X_1X_0$, where $X_3X_2X_1X_0$ is the OTP offset value

    DATA(0x0A)

13. COMMAND(0XF8)   \\ Send the OTP programming command.

14. Wait at least 2 seconds for programming wait time.

Verify the result:

15. After OTP programming, procedure 2 to 5 are repeated for inspection of the contrast on the panel.

Read Status Command

9.34 Status register read

This command will output the status of the device. Before sending the " status register read" command, the command "read display data mode" should be sent to the device. The following parameters can be monitored by the status read register.

1. Various area scroll mode
2. Column scan direction
3. Page scan direction
4. Display ON/OFF
5. Sleep mode ON/OFF
6. Display Normal/Inverse
7. Partial display mode ON/OFF

10 MAXIMUM RATINGS

Table 12 - Maximum Ratings (Voltage Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	-0.3 to +4.0	V
V_{OUT}		-0.3 to 15	V
V_{CI}	Input Voltage	V_{SS} -0.3 to 4.0	V
I	Current Drain Per Pin Excluding V_{DD} and V_{SS}	25	mA
T_A	Operating Temperature	-40 to +85	^{o}C
T_{stg}	Storage Temperature	-65 to +150	^{o}C
Ron	Input Resistance	1000	ohm

Maximum ratings are those values beyond which damages to the device may occur. Functional operation should be restricted to the limits in the Electrical Characteristics tables or Pin Description section

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions to be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{CI} and V_{OUT} be constrained to the range $V_{SS} < V_{DD} \leq V_{CI} < V_{OUT}$. Reliability of operation is enhanced if unused input is connected to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open. This device may be light sensitive. Caution should be taken to avoid exposure of this device to any light source during normal operation. This device is not radiation protected.

11 DC CHARACTERISTICS

Table 13 - DC Characteristics (Unless otherwise specified, Voltage Referenced to V_{SS}, V_{DD} = 2.4 to 3.6V, T_A = -40 to 85°C)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{DD}	System power supply pins of the logic block Range	Recommend Operating Voltage Possible Operating Voltage	2.4	2.7	3.6	V
V_{DDIO}	System power supply pins of the logic block Range	Recommend Operating Voltage Possible Operating Voltage	1.2	-	V_{DD}	V
V_{CI}	Booster Reference Supply Voltage Range	Recommend Operating Voltage Possible Operating Voltage	V_{DD}	-	3.6	V
I_{AC}	Access Mode Supply Current Drain (V_{DD} Pins)	V_{DD} = 2.7V, Voltage Generator On, 5X DC-DC , Write accessing, Tcyc =5MHz, Typ. Osc. Freq., Display On, no panel attached.	-	400	1000	µA
I_{DP2}	Display Mode Supply Current Drain (V_{DD} Pins)	V_{DD} = 2.7V, V_{OUT} = 9.2V, Voltage Generator On, 5X DC-DC Converter Enabled, R/W(WR) Halt, Typ. Osc. Freq., Display On, no panel attached.	-	250	500	µA
I_{SLEEP}	Sleep Mode Supply Current Drain (V_{DD} Pins)	V_{DD} = 2.7V, LCD Driving Waveform Off, Oscillator Off, R/W(WR) halt.	-	2	5	µA
V_{OUT}	LCD Driving Voltage Generator Output (V_{OUT} Pin)	Display On, Voltage Generator Enabled, DC-DC Converter Enabled, Typ. Osc. Freq., Regulator Enabled, Divider Enabled.	5	-	12.5	V
	V_{OUT} Converter Efficiency	6X boost, no panel loading	93	99	-	%
V_{REF}	Internal Reference Voltage (T = 25 °C)	TC0 = -0.10%/°C TC1 = -0.15%/°C TC2 = -0.20%/°C (POR) TC3 = -0.25%/°C	1.62 1.65 1.60 1.65	1.7 1.67 1.65 1.70	1.72 1.75 1.70 1.75	V V V V
	Reference Voltage (T = 25 °C) Reference Voltage (T = -20 °C) Reference Voltage (T = 70 °C)	TC3 = -0.25%/°C TC3 = -0.25%/°C TC3 = -0.25%/°C	1.65 1.83 1.46	1.70 1.89 1.51	1.75 1.95 1.56	V V V
V_{OH1}	Logic High Output Voltage	Iout=-100 A	0.9 * V_{DDIO}	-	V_{DDIO}	V
V_{OL1}	Logic Low Output Voltage	Iout=100 A	0	-	0.1 *V_{DDIO}	V
V_{IH1}	Logic High Input voltage		0.8* V_{DDIO}	-	V_{DDIO}	V
V_{IL1}	Logic Low Input voltage		0	-	0.2* V_{DDIO}	V
I_{OH}	Logic High Output Current Source	V_{OUT} = V_{DD}-0.4V	50	-	-	µA
I_{OL}	Logic Low Output Current Drain	V_{OUT} = 0.4V	-	-	-50	µA
I_{OZ}	Logic Output Tri-state Current Drain Source		-1	-	1	µA
I_{IL}/I_{IH}	Logic Input Current		-1	-	1	µA
C_{IN}	Logic Pins Input Capacitance		-	5	7.5	pF
ΔV_{OUT}	Variation of V_{OUT} Output (V_{DD} is fixed)	Regulator Enabled, Internal Contrast Control Enabled, Set Contrast Control Register = 0	-2	0	2	%

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
TC0	Average Temperature Gradient Flat Temperature Coefficient		0	-0.10	-0.12	%/°C
TC1	Temperature Coefficient 1	Voltage Regulator Enabled	-0.12	-0.15	-0.17	%/°C
TC2	Temperature Coefficient 2 (POR)		-0.17	-0.20	-0.22	%/°C
TC3	Temperature Coefficient 3		-0.22	-0.25	-0.27	%/°C

The formula for the temperature coefficient is:

$$TC(\%) = \frac{V_{ref} \, at 50°C - V_{ref} \, at 0°C}{50°C - 0°C} \, x \, \frac{1}{V_{ref} \, at 25°C} \, x100\%$$

12 AC CHARACTERISTICS

Table 14 - AC Characteristics (Unless otherwise specified, Voltage Referenced to V_{SS}, V_{DD} = 2.7V, T_A = 25°C)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
Fosc	Oscillation Frequency of Display Timing Generator for: 80 MUX Mode or 68 MUX mode	Internal Oscillator Enabled (default), V_{DD} = 2.7V Remark: -0.2%/°C (POR)	465.12	477.36	489.6	kHz
F_{FRM}	Frame Frequency for: 80 MUX Mode	a. 104 RGB x 80 Graphic Display Mode, Display ON, Internal Oscillator Enabled	62.7	66	69.3	Hz
	Frame Frequency for: 68 MUX Mode	b. 104 RGB x 68 Graphic Display Mode, Display ON, Internal Oscillator Disabled, External clock with freq., Fext, feeding to CL pin.	74.1	78	81.9	Hz

Remarks: Fext stands for the frequency value of external clock feeding to the CL pin
Fosc stands for the frequency value of internal oscillator

Table 15 – Parallel Timing Characteristics (T_A = -40 to 85°C, V_{DD} = 2.4V to 3.6V)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time (write cycle)	166.6	-	-	ns
t_{AS}	Address Setup Time	15	-	-	ns
t_{AH}	Address Hold Time	10	-	-	ns
t_{DSW}	Data Setup Time	10	-	-	ns
t_{DHW}	Data Hold Time	20	-	-	ns
t_{ACC}	Data Access Time	15	-	200	ns
t_{OH}	Output Hold time	20	-	60	ns
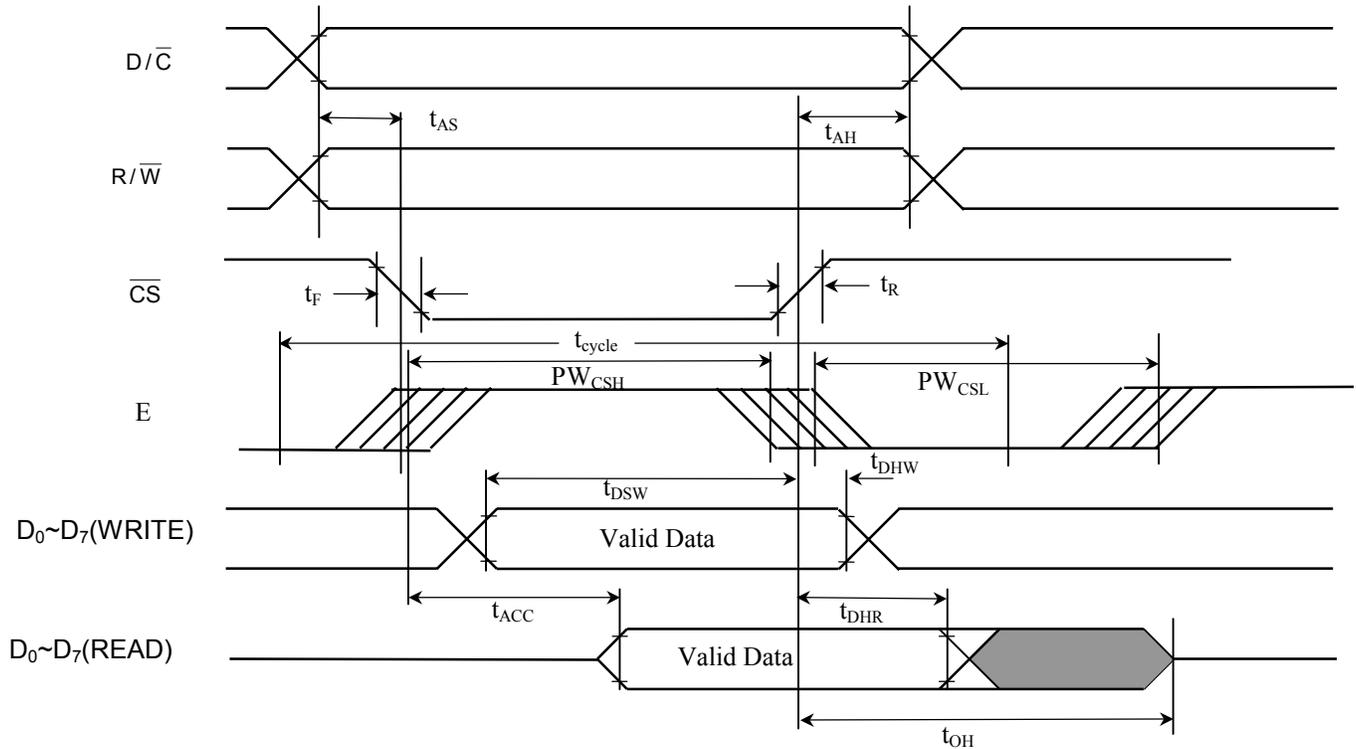
Figure 19 – Parallel 6800-series Interface Timing Characteristics (PS0 = H, PS1 = H)

Table 16 – Parallel Timing Characteristics (T_A = -40 to 85°C, V_{DD} = 2.4V to 3.6V)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time (write cycle)	166.6	-	-	ns
t_{AS}	Address Setup Time	15	-	-	ns
t_{AH}	Address Hold Time	10	-	-	ns
t_{DSW}	Data Setup Time	10	-	-	ns
t_{DHW}	Data Hold Time	20	-	-	ns
t_{ACC}	Data Access Time	15	-	170	ns
t_{OH}	Output Hold time	20	-	60	ns

Write Cycle
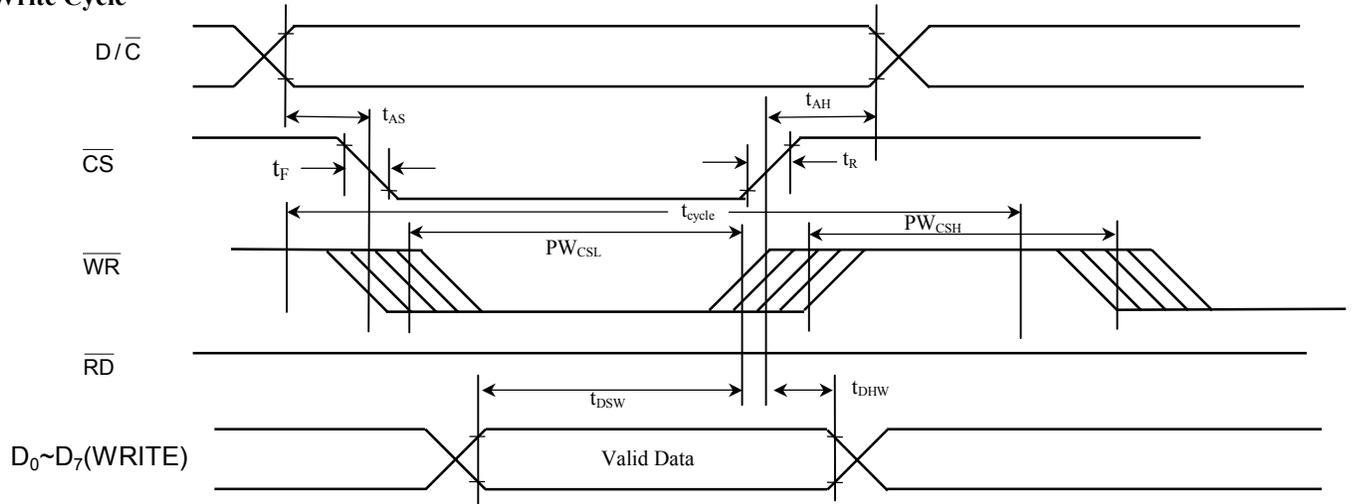
Read Cycle
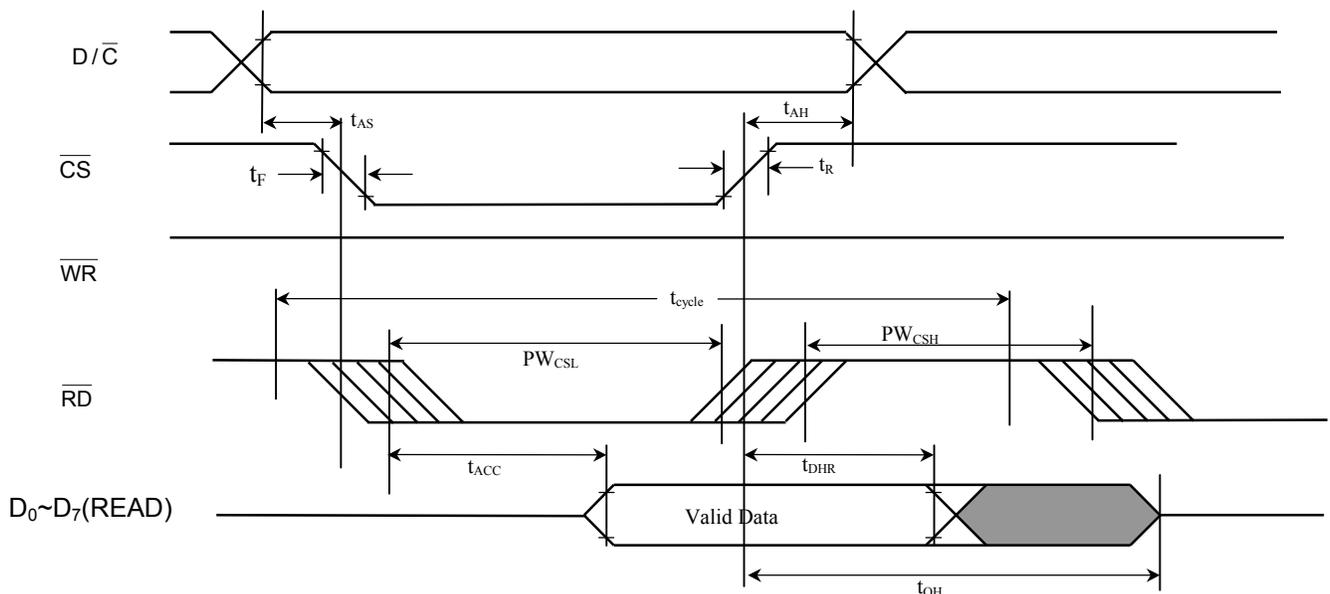
Figure 20 – Parallel 8080-series Interface Timing Characteristics (PS0 = H, PS1 = L)

Table 17 - Serial Timing Characteristics (T_A = -40 to 85°C, V_{DD} = 2.4V to 3.6V)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	66.6	-	-	ns
f_{CLK}	Serial Clock Cycle Time SPI Clock tolerance = +/- 2 ppm	-	-	15	MHz
t_{AS}	Register select Setup Time	90	-	-	ns
t_{AH}	Register select Hold Time	20	-	-	ns
t_{CSS}	Chip Select Setup Time	10	-	-	ns
t_{CSH}	Chip Select Hold Time	30	-	-	ns
t_{DSW}	Write Data Setup Time	10	-	-	ns
t_{OHW}	Write Data Hold Time	10	-	-	ns
t_{CLKL}	Clock Low Time	15	-	-	ns
t_{CLKH}	Clock High Time	15	-	-	ns
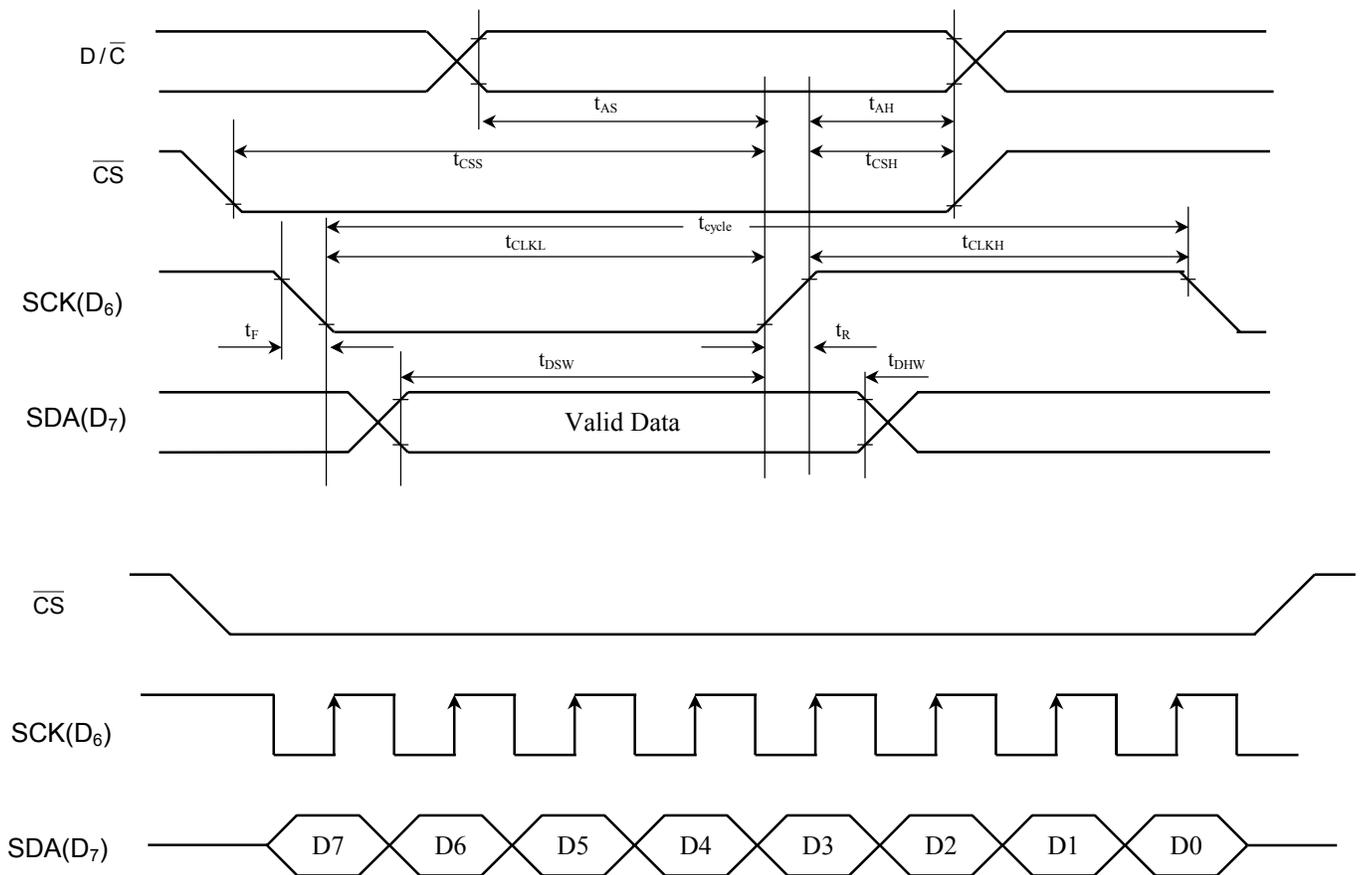
Figure 21 - Serial Timing Characteristics (PS0 = L, PS1 =L)

13 APPLICATION EXAMPLES

,where
V_{DD} & V_{CI} = 2.775V;
V_{DDIO} = 2.775V;
C_1 = 1uF ~2uF;
C_2 = 2.2uF ~ 4.7uF.
Logic pin connections not specified above:
Pins connected to V_{DD}: E; R/$\overline{W}$; D_0~D_5;
Pins connected to V_{SS}: PS0; PS1; RV_{SS}; CV_{SS}; MUX68/($\overline{80}$); VL_{REF};
Pin connected to V_{OUT}: VH_{REF};
Pin connected to V_{CI}: V_{CIX2};
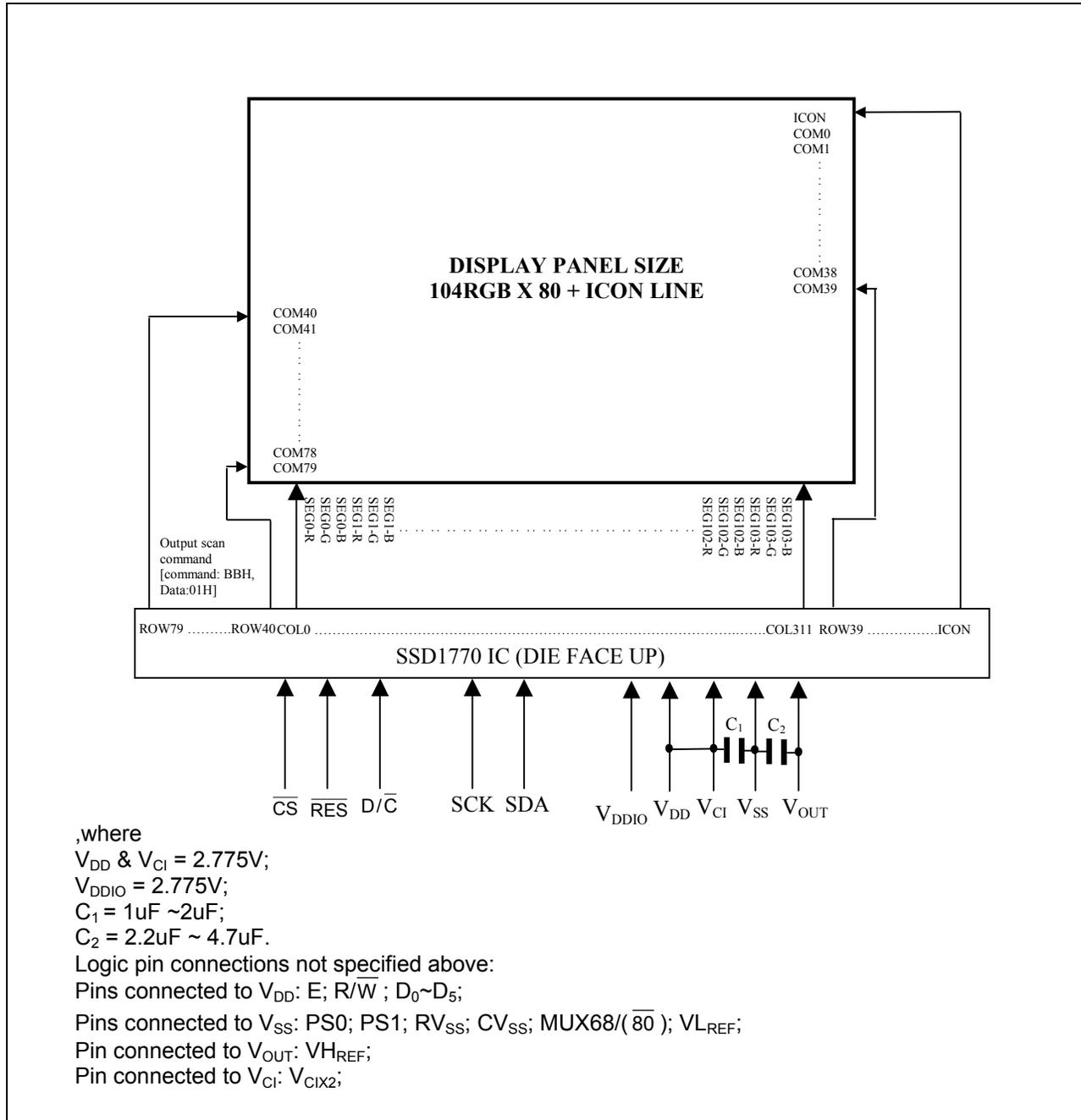
Figure 22 - Application Example I (4-wires SPI mode)

DISPLAY PANEL SIZE
104RGB X 80 + ICON LINE

ICON
COM0
COM1

COM38
COM39

COM40
COM41

COM78
COM79

SEG0-R
SEG0-G
SEG0-B
SEG1-R
SEG1-G
SEG1-B

SEG102-R
SEG102-G
SEG102-B
SEG103-R
SEG103-G
SEG103-B

Output scan
command
[command: BBH,
Data:01H]

ROW79 ....ROW40 COL0 ....COL311 ROW39 ....ICON

SSD1770 IC (DIE FACE UP)

$\overline{CS}$ $\overline{RES}$ D/$\overline{C}$ R/$\overline{W}$ E $D_0 \dots D_7$ V_{DDIO} V_{DD} V_{CI} V_{SS} V_{OUT}

C_1 C_2

,where
V_{DD} & V_{CI} = 2.775V;
V_{DDIO} = 2.775V;
C_1 = 1uF ~ 2.2uF;
C_2 = 2.2uF ~ 4.7uF.
Logic pin connections not specified above:
Pins connected to V_{DD}: PS0; PS1;
Pins connected to V_{SS}: RV_{SS}; CV_{SS}; MUX68/($\overline{80}$); VL_{REF};
Pin connected to V_{OUT}: VH_{REF};
Pin connected to V_{CI}: V_{CIX2};

Figure 23 - Application Example II (6800 PPI mode)
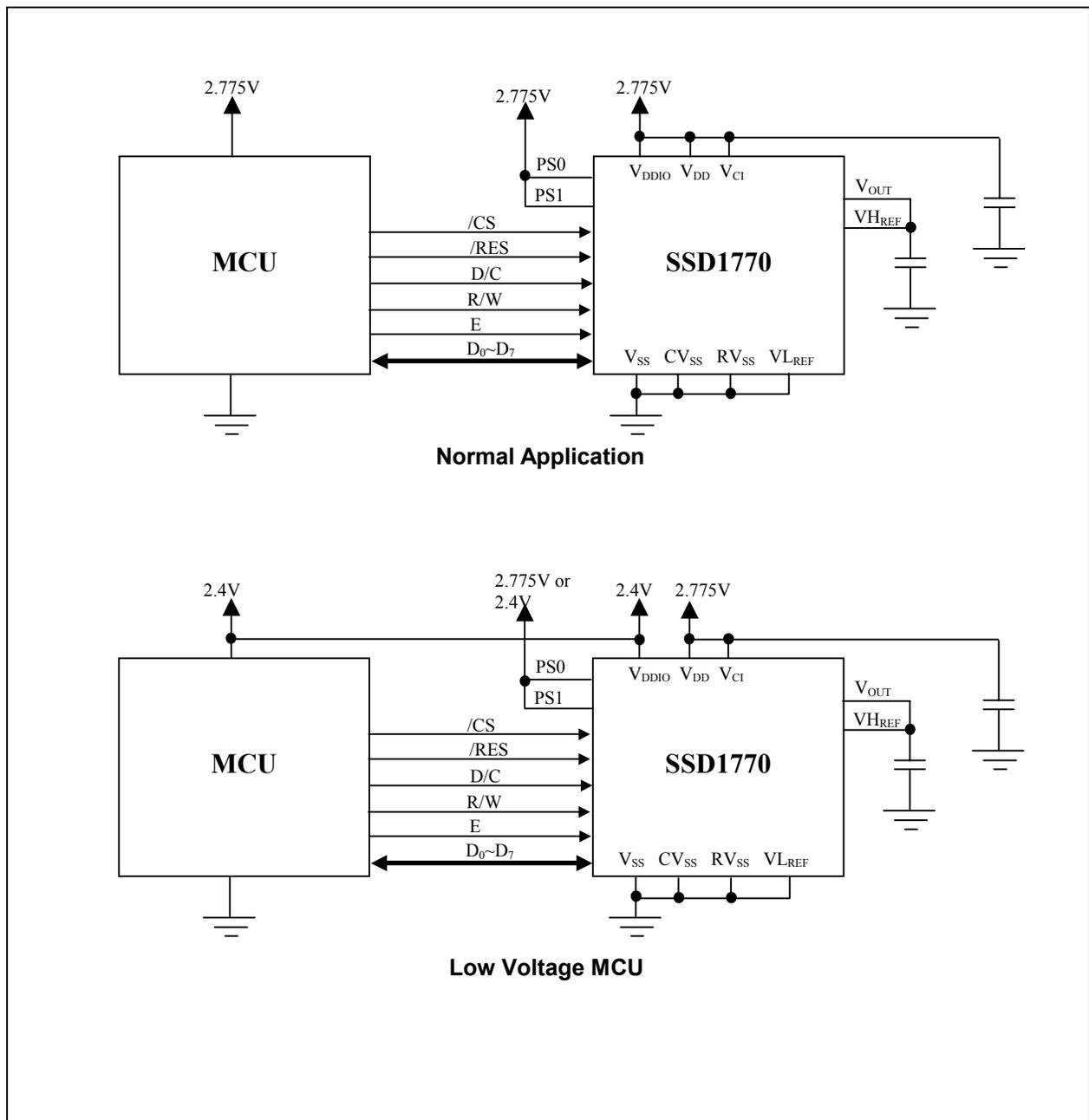
Figure 24 – Applications notes for V_{DD}/V_{DDIO} connection

14 SSD1770Z DIE TRAY DIMENSIONS
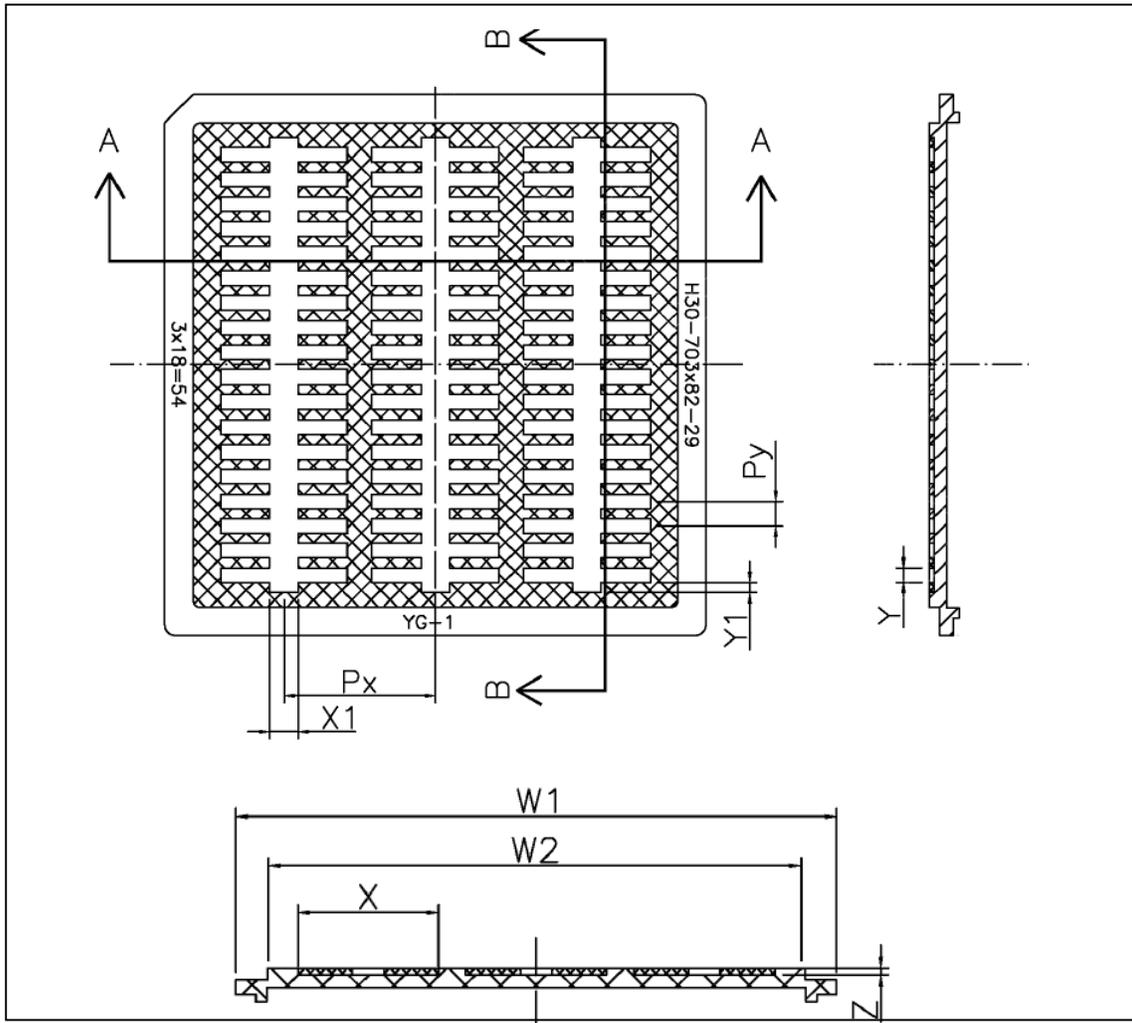
Spec	mm	(mil)
W1	$76.0^{+0.2}_{-0.1}$	(2992)
W2	$68.0^{+0.2}_{-0.1}$	(2677)
X1	4.0 ± 0.1	(158)
Y1	1.40 ± 0.1	(55)
X	17.85 ± 0.1	(703)
Y	2.07 ± 0.1	(82)
Z	0.73 ± 0.1	(29)
N	54	

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