



## STW26NM60N-H

N-channel 600 V, 0.135  $\Omega$ , 20 A TO-247  
MDmesh™ II Power MOSFET

### Features

Type	V <sub>DSS</sub>	R <sub>DS(on)</sub> max	I <sub>D</sub>
STW26NM60N-H	600 V	< 0.165 $\Omega$	20 A

- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance

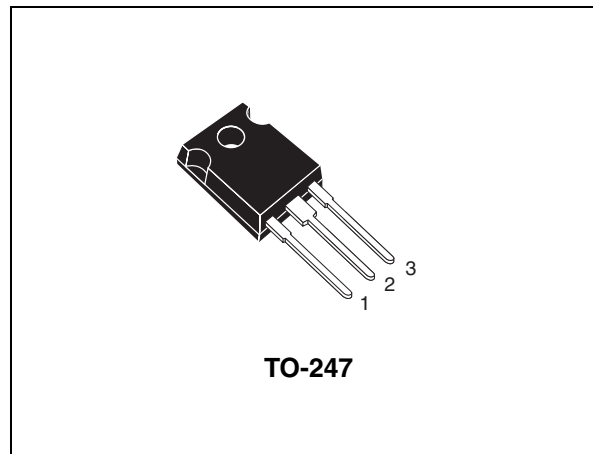
### Application

- Switching applications

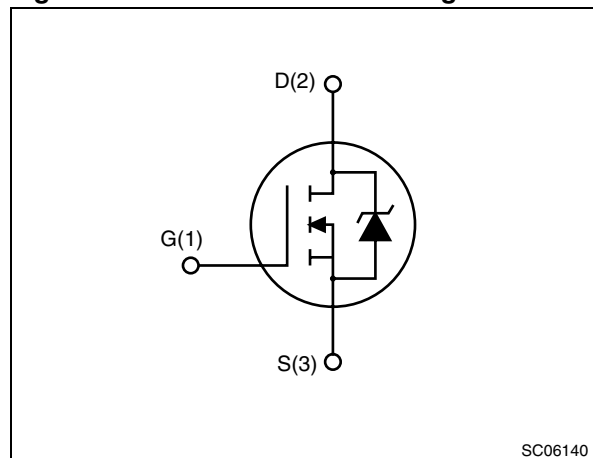
### Description

This series of devices implements second generation MDmesh™ technology. This revolutionary Power MOSFET associates a new vertical structure to the company's strip layout to yield one of the world's lowest on-resistance and gate charge. It is therefore suitable for the most demanding high efficiency converters.

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**Figure 1. Internal schematic diagram**



**Table 1. Device summary**

Order codes	Marking	Package	Packaging
STW26NM60N-H	26NM60N	TO-247	Tube

*Note:* The device meets ECOPACK® standards, an environmentally-friendly grade of products commonly referred to as "halogen-free". See [Section 4: Package mechanical data](#)

# Contents

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage ( $V_{GS} = 0$ )	600	V
$V_{GS}$	Gate-source voltage	$\pm 25$	V
$I_D$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	20	A
$I_D$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	12.6	A
$I_{DM}^{(1)}$	Drain current (pulsed)	80	A
$P_{TOT}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	140	W
	Derating factor	1.12	
$dv/dt^{(2)}$	Peak diode recovery voltage slope	15	V/ns
$T_{stg}$	Storage temperature	-55 to 150	$^\circ\text{C}$
$T_j$	Max. operating junction temperature	150	$^\circ\text{C}$

1. Pulse width limited by safe operating area
2.  $I_{SD} \leq 20\text{ A}$ ,  $di/dt \leq 400\text{ A}/\mu\text{s}$ ,  $V_{DD} \leq 80\% V_{(BR)DSS}$

**Table 3. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	0.89	$^\circ\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-ambient max	50	$^\circ\text{C}/\text{W}$
$T_l$	Maximum lead temperature for soldering purpose	300	$^\circ\text{C}$

**Table 4. Avalanche characteristics**

Symbol	Parameter	Value	Unit
$I_{AS}$	Avalanche current, repetitive or not-repetitive (pulse width limited by $T_j$ max)	8.5	A
$E_{AS}$	Single pulse avalanche energy (starting $T_j=25\text{ }^\circ\text{C}$ , $I_D=I_{AS}$ , $V_{DD}=50\text{ V}$ )	610	mJ

## 2 Electrical characteristics

( $T_{CASE} = 25\text{ °C}$  unless otherwise specified)

**Table 5. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$ , $V_{GS} = 0$	600			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = \text{Max rating}$ $V_{DS} = \text{Max rating}$ , @125 °C			1 10	$\mu\text{A}$ $\mu\text{A}$
$I_{GSS}$	Gate-body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 20\text{ V}$			0.1	$\mu\text{A}$
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$	2	3	4	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{ V}$ , $I_D = 10\text{ A}$		0.135	0.165	$\Omega$

**Table 6. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 50\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0$	-	1800	-	$\mu\text{F}$
$C_{oss}$	Output capacitance			115		
$C_{rss}$	Reverse transfer capacitance			1.1		
$C_{oss\text{ eq.}}^{(1)}$	Equivalent output capacitance	$V_{GS} = 0$ , $V_{DS} = 0\text{ to }480\text{ V}$	-	310	-	$\mu\text{F}$
$Q_g$	Total gate charge	$V_{DD} = 480\text{ V}$ , $I_D = 20\text{ A}$ , $V_{GS} = 10\text{ V}$ , <i>(see Figure 15)</i>	-	60	-	nC
$Q_{gs}$	Gate-source charge			8.5		
$Q_{gd}$	Gate-drain charge			30		
$R_g$	Gate input resistance	f=1 MHz Gate DC Bias=0 Test signal level = 20 mV open drain	-	2.8	-	$\Omega$

1.  $C_{oss\text{ eq.}}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DS}$

**Table 7. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit	
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 300\text{ V}$ , $I_D = 10\text{ A}$ $R_G = 4.7\ \Omega$ , $V_{GS} = 10\text{ V}$ (see Figure 14)		13		ns	
$t_r$	Rise time			25		ns	
$t_{d(off)}$	Turn-off delay time				85	-	ns
$t_f$	Fall time				50		ns

**Table 8. Source drain diode**

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
$I_{SD}$	Source-drain current		-		20	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				80	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 20\text{ A}$ , $V_{GS} = 0$	-		1.5	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 20\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 60\text{ V}$ (see Figure 16)	-	370		ns
$Q_{rr}$	Reverse recovery charge			5.8		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current			31.6		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 20\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 60\text{ V}$ , $T_j = 150\text{ }^\circ\text{C}$ (see Figure 16)	-	450		ns
$Q_{rr}$	Reverse recovery charge			7.5		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current			32.5		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area for TO-247

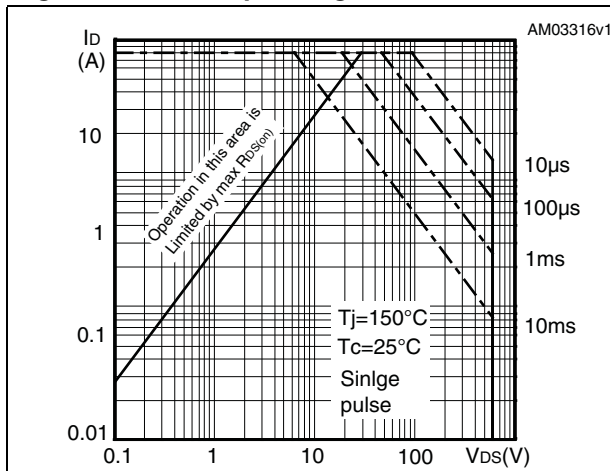


Figure 3. Thermal impedance for TO-247

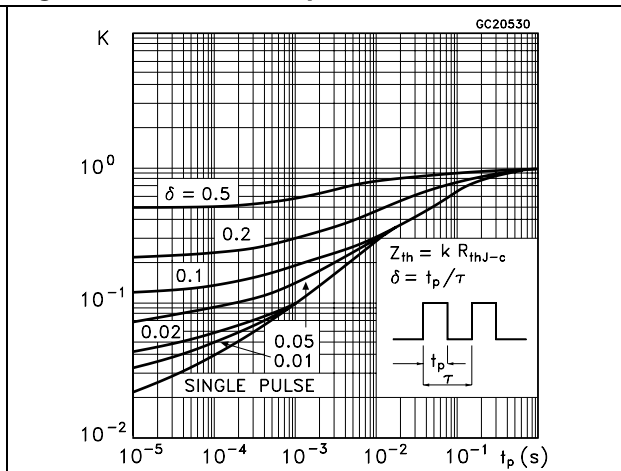


Figure 4. Output characteristics

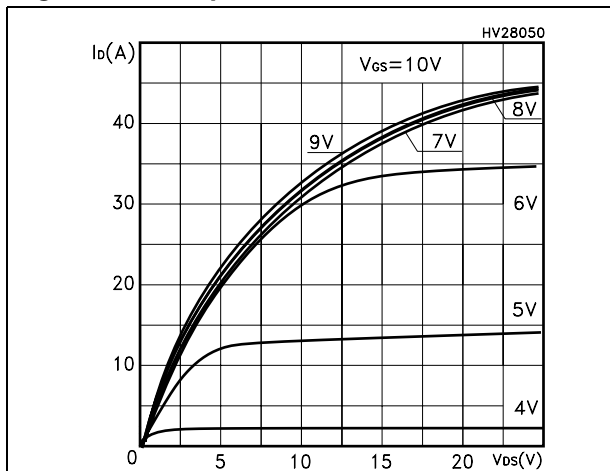


Figure 5. Transfer characteristics

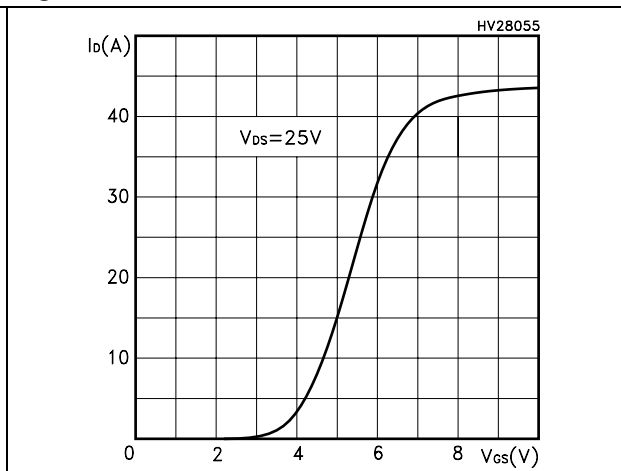


Figure 6. Transconductance

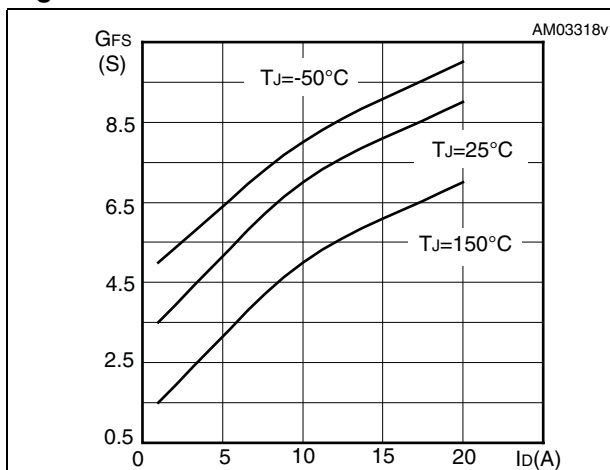
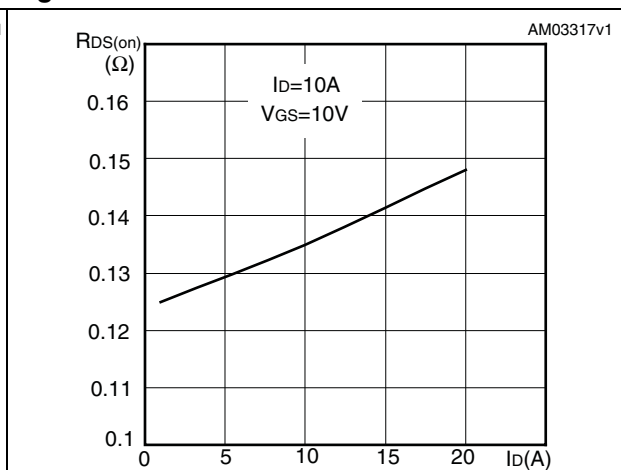


Figure 7. Static drain-source on resistance



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Figure 8. Gate charge vs gate-source voltage Figure 9. Capacitance variations

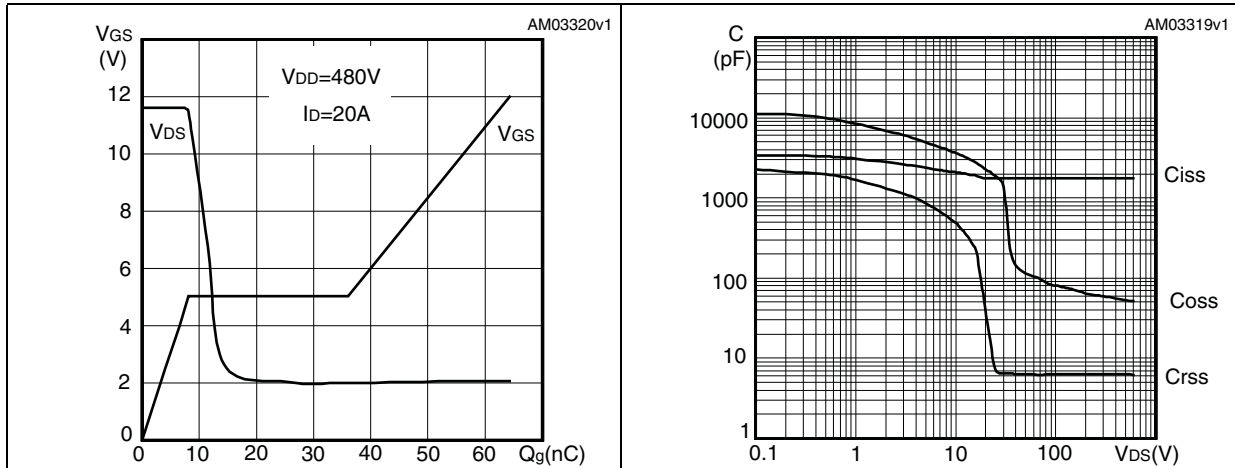


Figure 10. Normalized gate threshold voltage vs temperature Figure 11. Normalized on resistance vs temperature

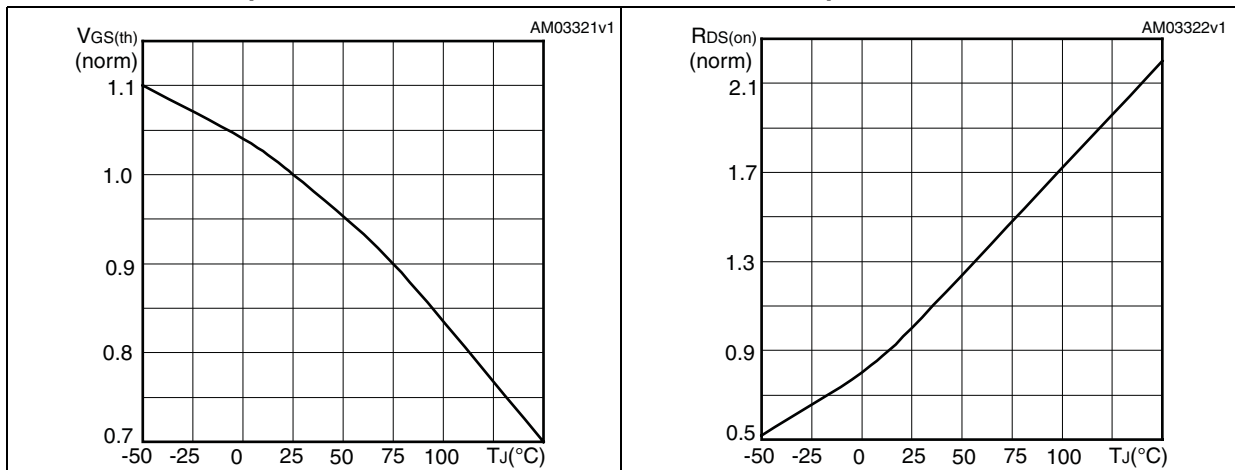
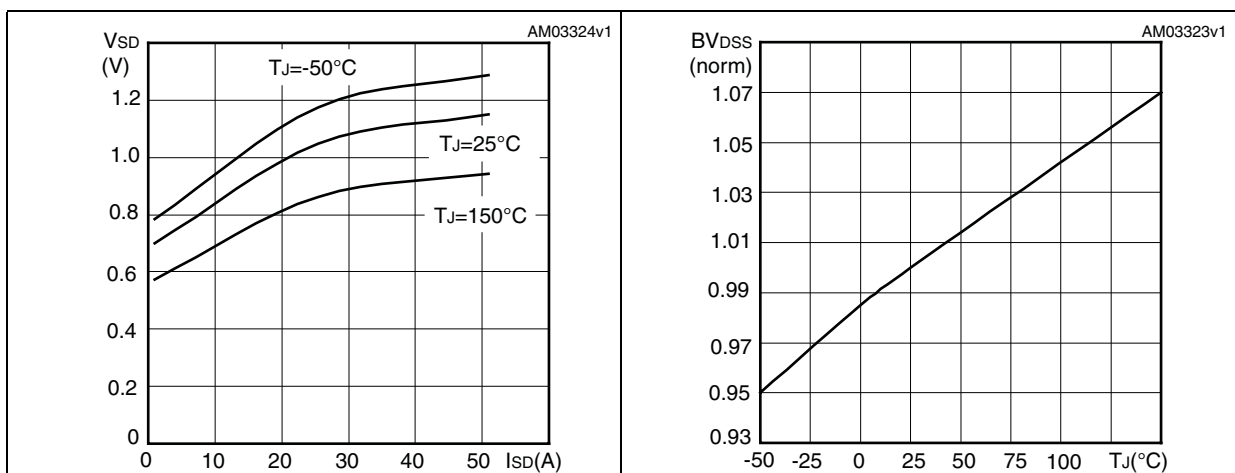
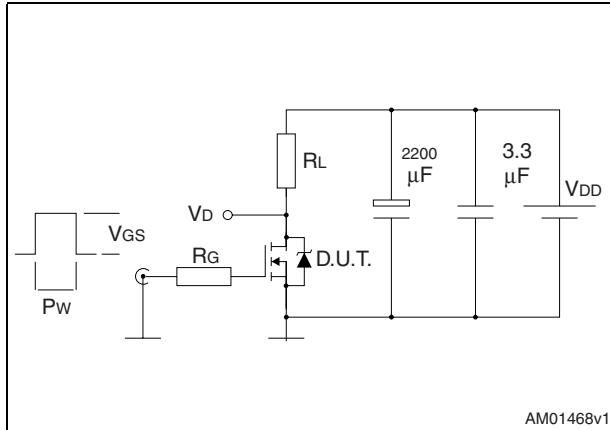


Figure 12. Source-drain diode forward characteristics Figure 13. Normalized BV<sub>DSS</sub> vs temperature



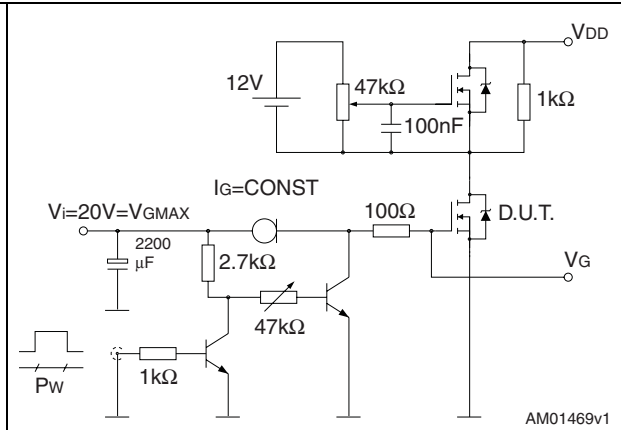
### 3 Test circuits

**Figure 14. Switching times test circuit for resistive load**



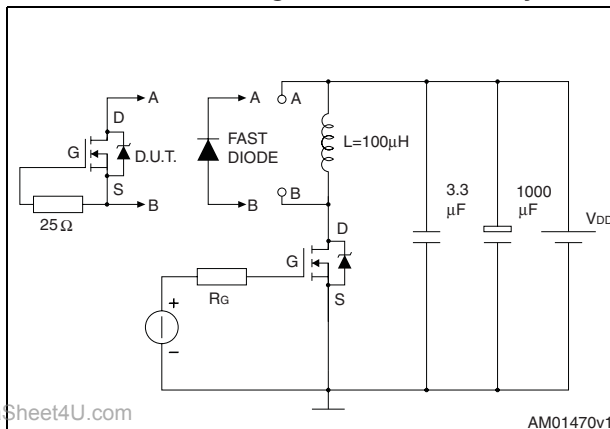
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**Figure 15. Gate charge test circuit**



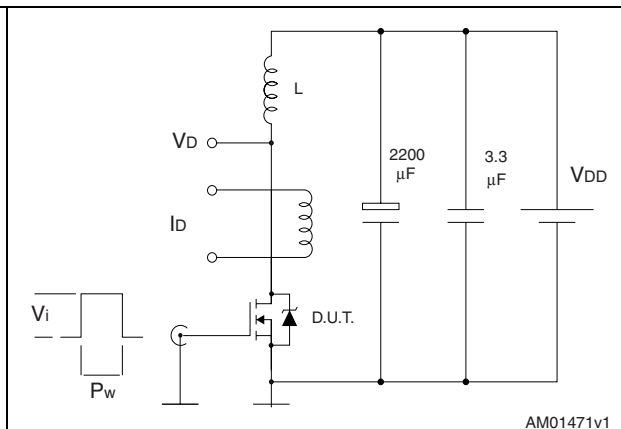
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**Figure 16. Test circuit for inductive load switching and diode recovery times**



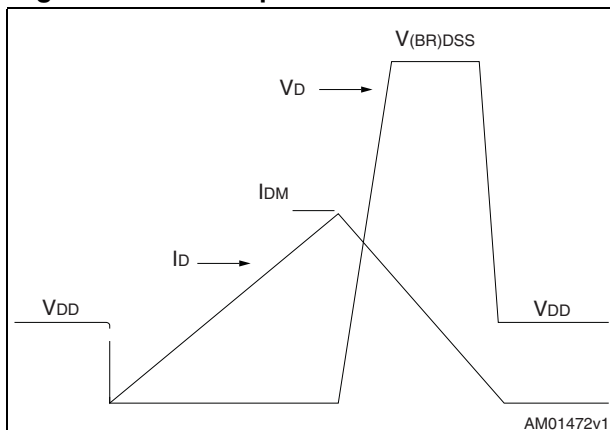
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**Figure 17. Unclamped inductive load test circuit**



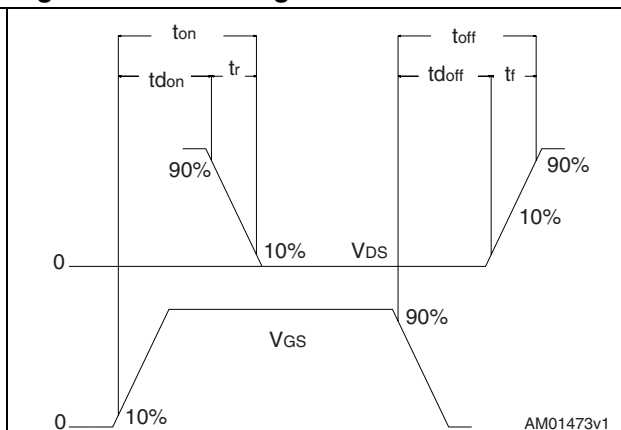
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**Figure 18. Unclamped inductive waveform**



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**Figure 19. Switching time waveform**



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## 4 Package mechanical data

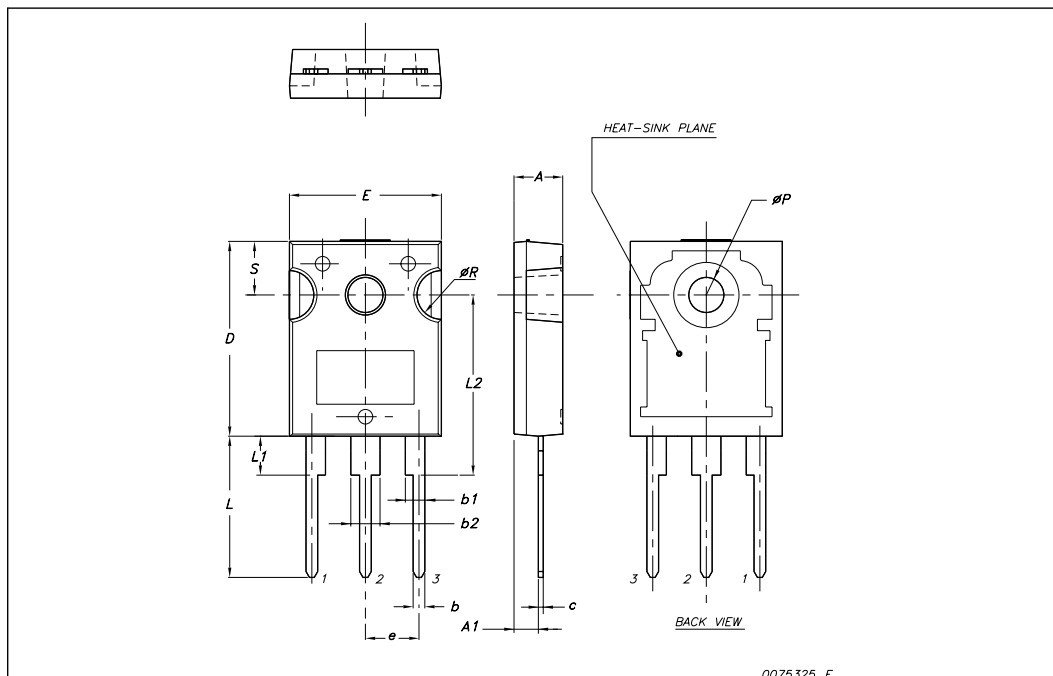
In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

## Package mechanical data

## STW26NM60N-H

## TO-247 Mechanical data

Dim.	mm.		
	Min.	Typ	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e		5.45	
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
øP	3.55		3.65
øR	4.50		5.50
S		5.50	



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## 5 Revision history

**Table 9. Document revision history**

Date	Revision	Changes
06-Oct-2009	1	First release

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