Elektronische Bauelemente

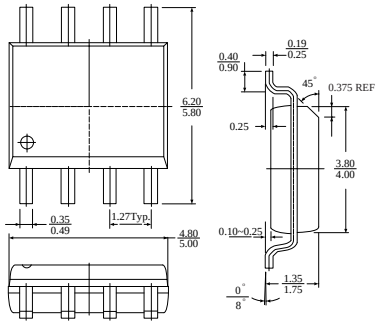
SSG4565

N Channel 7.6A, 40V, $R_{DS(ON)}$ 25mΩ
P Channel 6.5A, 40V, $R_{DS(ON)}$ 33mΩ

Enhancement Mode Power Mos.FET

RoHS Compliant Product

SOP-8



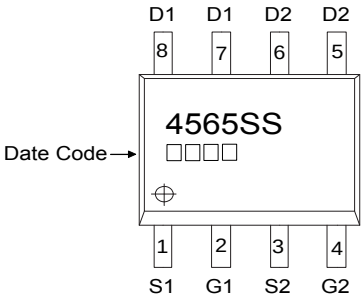
Dimensions in millimeters

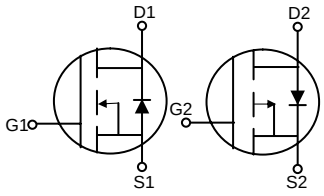
Description

The SSG4565 provide the designer with the best combination of fast switching, ruggedized device design, Ultra low on-resistance and cost-effectiveness.
The SOP-8 package is universally preferred for all commercial industrial surface mount application and suited for low voltage applications such as DC/DC converters.

Features

* Simple Drive Requirement
* Lower On-resistance
* Fast Switching Performance





Absolute Maximum Ratings

Parameter	Symbol	Ratings		Unit
		N-Channel	P-Channel	
Drain-Source Voltage	V_{DS}	40	-40	V
Gate-Source Voltage	V_{GS}	±20	±20	V
Continuous Drain Current [3]	I_D@T_A=25°C	7.6	-6.5	A
Continuous Drain Current [3]	I_D@T_A=70°C	6	-5.2	A
Pulsed Drain Current [1]	I_{DM}	30	-30	A
Total Power Dissipation	P_D@T_A=25°C	2		W
Linear Derating Factor		0.016		W/°C
Operating Junction and Storage Temperature Range	Tj, Tstg	-55~+150		°C

Thermal Data

Parameter	Symbol	Ratings	Unit
Thermal Resistance Junction-ambient [3]	Rthj-a	62.5	°C/W

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Enhancement Mode Power Mos.FET

Electrical Characteristics N-Channel (Tj=25 °C Unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Drain-Source Breakdown Voltage	BV_{DSS}	40	–	–	V	V_{GS}=0V, I_D=250uA
Breakdown Voltage Temp. Coefficient	$\triangle BV_{DS}/\triangle Tj$	–	0.03	–	V/°C	Reference to 25°C, I_D=1mA
Gate Threshold Voltage	$V_{GS(th)}$	1.0	–	3.0	V	V_{DS}=V_{GS}, I_D=250uA
Gate-Source Leakage Current	I_{GSS}	–	–	±100	nA	V_{GS}=±20V
Drain-Source Leakage Current (Tj=25°C)	I_{DSS}	–	–	1	uA	V_{DS}=40V, V_{GS}=0
Drain-Source Leakage Current (Tj=70°C)		–	–	25	uA	V_{DS}=32V, V_{GS}=0
Static Drain-Source On-Resistance[2]	$R_{DS(ON)}$	–	–	25	mΩ	V_{GS}=10V, I_D=7A
		–	–	32		V_{GS}=4.5V, I_D=5A
Total Gate Charge[2]	Qg	–	17	27	nC	I_D=7A V_{DS}=32V V_{GS}=4.5V
Gate-Source Charge	Qgs	–	4	–		
Gate-Drain ("Miller") Charge	Qgd	–	10	–		
Turn-on Delay Time[2]	$Td_{(ON)}$	–	11	–	nS	V_{DD}=20V I_D=1A V_{GS}=10V R_G=3.3Ω R_D=20 Ω
Rise Time	Tr	–	8	–		
Turn-off Delay Time	$Td_{(Off)}$	–	30	–		
Fall Time	T_f	–	11	–		
Input Capacitance	Ciss	–	1400	2400	pF	V_{GS}=0V V_{DS}=25V f=1.0MHz
Output Capacitance	Coss	–	250	–		
Reverse Transfer Capacitance	Crss	–	170	–		
Forward Transconductance	Gfs	–	12	–	S	V_{DS}=10V, I_D=7A

Source-Drain Diode

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Forward On Voltage[2]	V_{SD}	–	–	1.2	V	I_S=1.7A, V_{GS}=0V.
Reverse Recovery Time[2]	Trr	–	26	–	ns	Is=7A, V_{GS}=0V dl/dt=100A/us
Reverse Recovery Charge	Qrr	–	21	–	nC	

Notes: 1.Pulse width limited by Max. junction temperature.
2.Pulse width≦300us, dutycycle≦2%.
3.Surface mounted on 1 inch$_2$ copper pad of FR4 board; 270°C/W when mounted on min. copper pad.

Elektronische Bauelemente

SSG4565

N Channel 7.6A, 40V,$R_{DS(ON)}$ 25mΩ
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Enhancement Mode Power Mos.FET

Electrical Characteristics P-Channel(Tj=25°C Unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Drain-Source Breakdown Voltage	BV_{DSS}	-40	–	–	V	V_{GS}=0V, I_D=-250uA
Breakdown Voltage Temp. Coefficient	$\triangle BV_{DS}/\triangle Tj$	–	-0.03	–	V/°C	Reference to 25°C,I_D=-1mA
Gate Threshold Voltage	$V_{GS(th)}$	-1.0	–	-3.0	V	V_{DS}=V_{GS}, I_D=-250uA
Gate-Source Leakage Current	I_{GSS}	–	–	±100	nA	V_{GS}=±20V
Drain-Source Leakage Current (Tj=25°C)	I_{DSS}	–	–	-1	uA	V_{DS}=-40V,V_{GS}=0
Drain-Source Leakage Current (Tj=70°C)		–	–	-25	uA	V_{DS}=-32V,V_{GS}=0
Static Drain-Source On-Resistance[2]	$R_{DS(ON)}$	–	–	33	mΩ	V_{GS}=-10V, I_D=-6A
		–	–	42		V_{GS}=-4.5V, I_D=-4A
Total Gate Charge[2]	Qg	–	20	32	nC	I_D=-6A V_{DS}=-32V V_{GS}=-4.5V
Gate-Source Charge	Qgs	–	4	–		
Gate-Drain ("Miller") Charge	Qgd	–	10	–		
Turn-on Delay Time[2]	$Td_{(ON)}$	–	11	–	nS	V_{DS}=-20V I_D=-1A V_{GS}=-10V R_G=3.3Ω R_D=20Ω
Rise Time	Tr	–	7	–		
Turn-off Delay Time	$Td_{(Off)}$	–	67	–		
Fall Time	T_f	–	43	–		
Input Capacitance	Ciss	–	1440	2300	pF	V_{GS}=0V V_{DS}=-25V f=1.0MHz
Output Capacitance	Coss	–	250	–		
Reverse Transfer Capacitance	Crss	–	190	–		
Forward Transconductance	Gfs	–	10	–	S	V_{DS}=-10V, I_D=-6A

Source-Drain Diode

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Forward On Voltage[2]	V_{SD}	–	–	-1.2	V	I_S=-1.7A, V_{GS}=0V.
Reverse Recovery Time[2]	Trr	–	27	–	ns	Is=-6A, VGS=0V dl/dt=100A/us
Reverse Recovery Charge	Qrr	–	23	–	nC	

Notes: 1.Pulse width limited by Max. junction temperature.
2.Pulse width≦300us, dutycycle≦2%.
3.Surface mounted on 1 inch$_2$ copper pad of FR4 board; 270°C/W when mounted on min. copper pad.

Elektronische Bauelemente

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Enhancement Mode Power Mos.FET

Characteristics Curve N-Channel

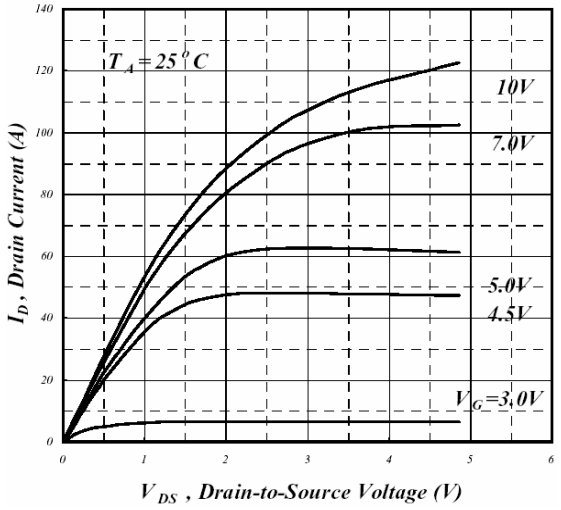

Fig 1. Typical Output Characteristics

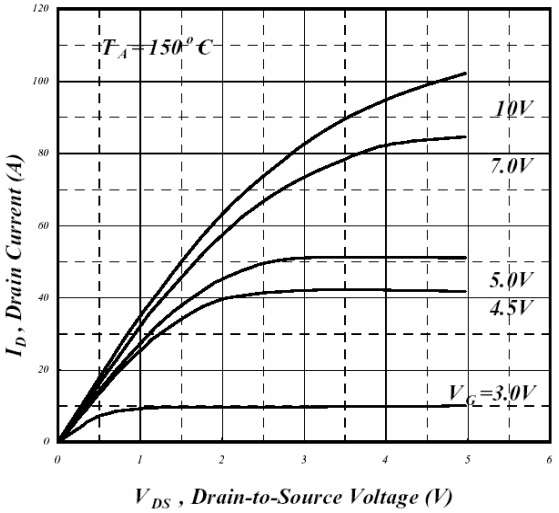

Fig 2. Typical Output Characteristics

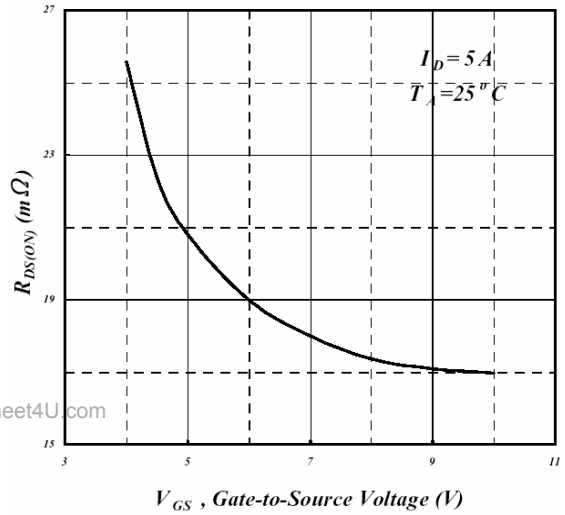

Fig 3. On-Resistance v.s. Gate Voltage

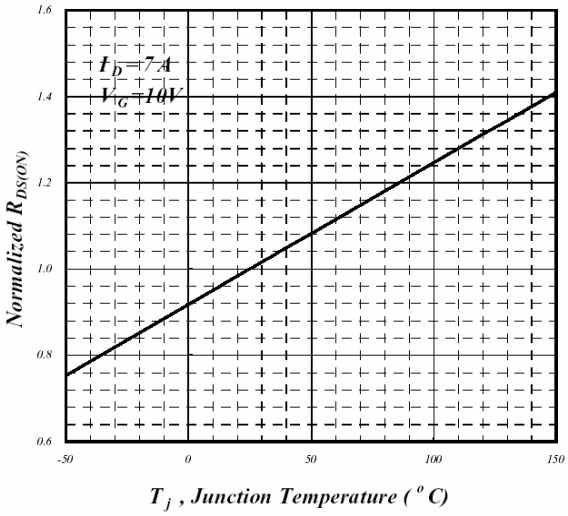

Fig 4. Normalized On-Resistance v.s. Junction Temperature

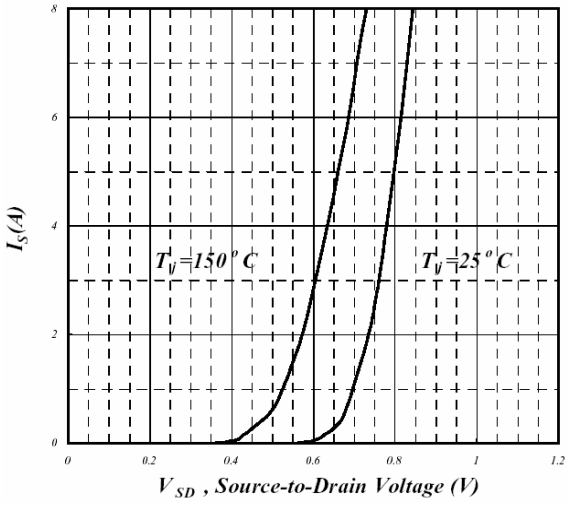

Fig 5. Forward Characteristics of Reverse Diode

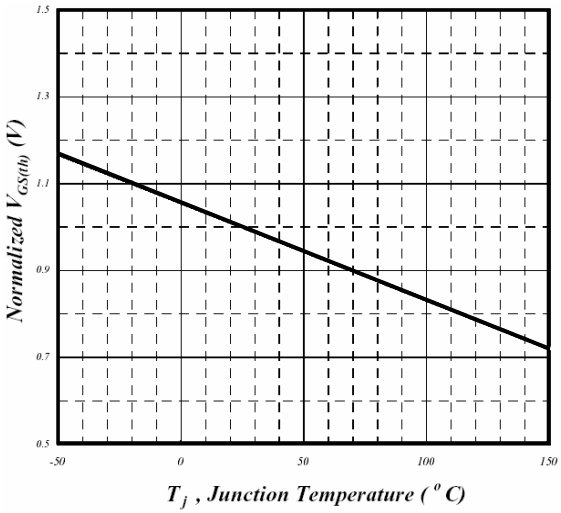

Fig 6. Gate Threshold Voltage v.s. Junction Temperature

Elektronische Bauelemente

SSG4565

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Enhancement Mode Power Mos.FET

N-Channel

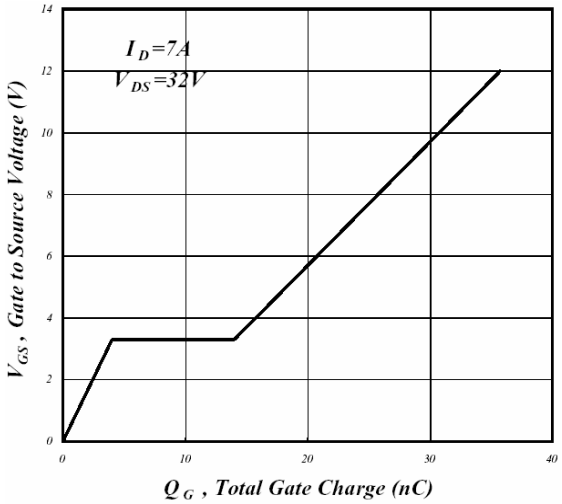

Fig 7. Gate Charge Characteristics

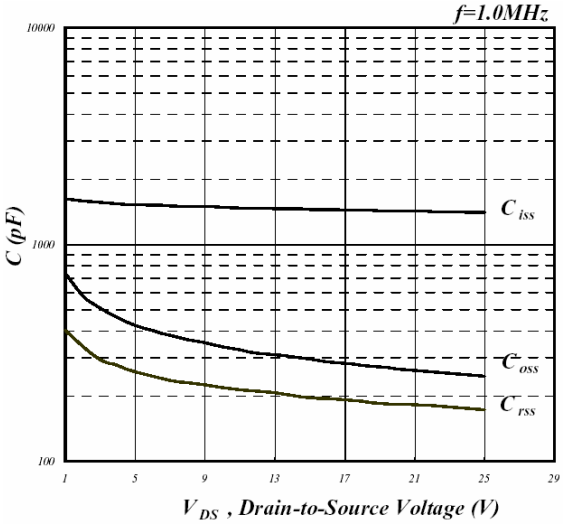

Fig 8. Typical Capacitance Characteristics

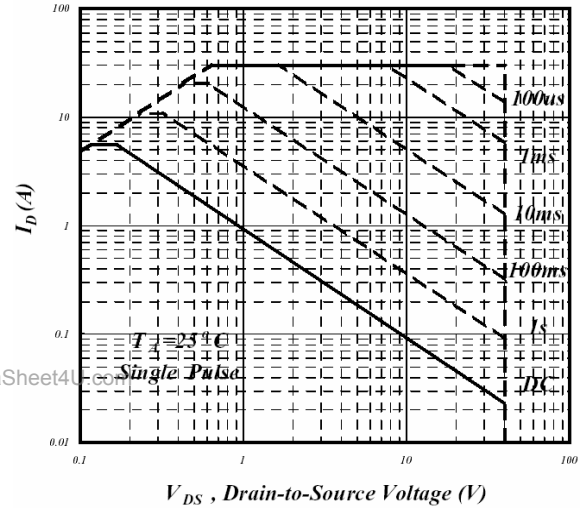

Fig 9. Maximum Safe Operating Area

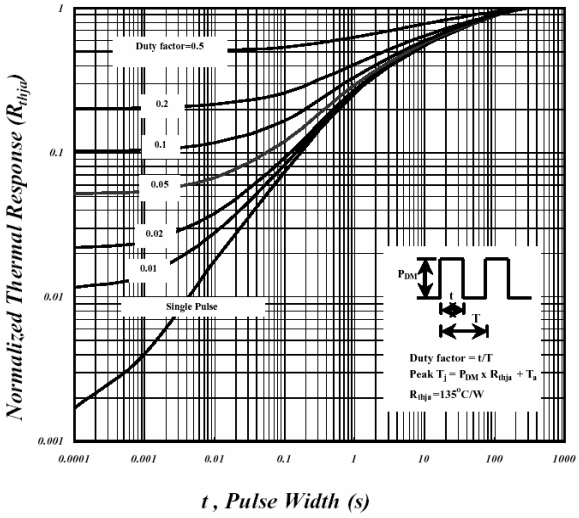

Fig 10. Effective Transient Thermal Impedance

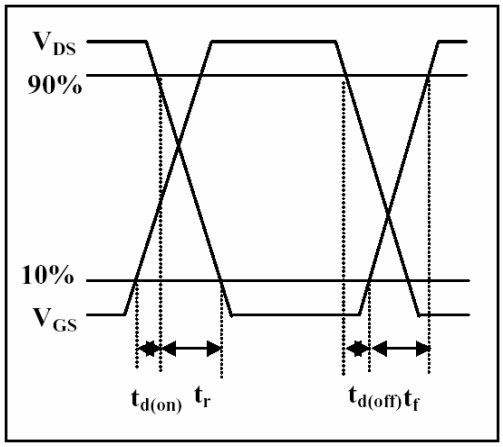

Fig 11. Switching Time Waveform

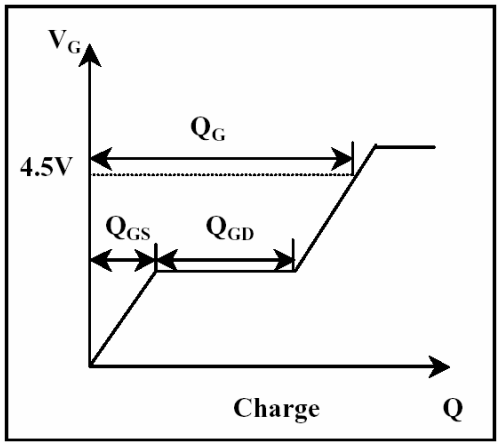

Fig 12. Gate Charge Waveform

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P-Channel

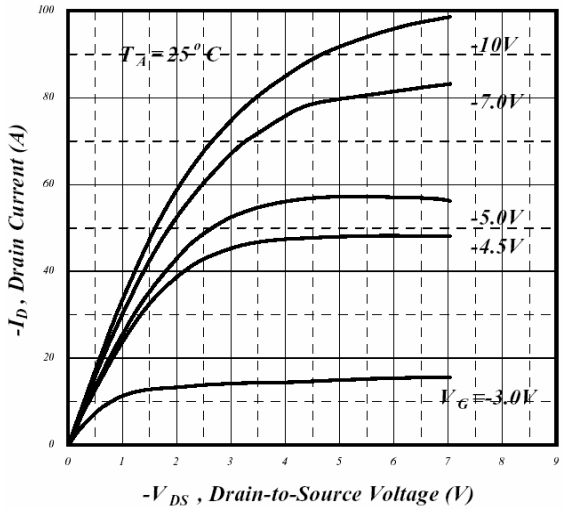

Fig 1. Typical Output Characteristics

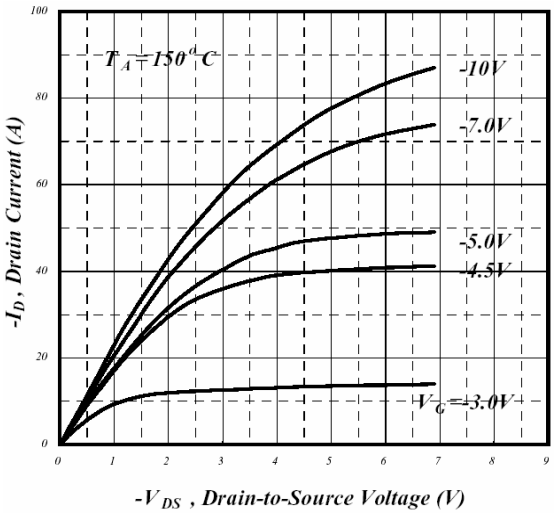

Fig 2. Typical Output Characteristics

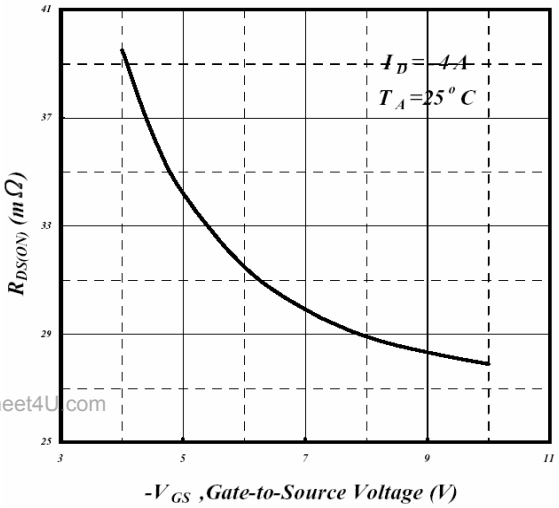

Fig 3. On-Resistance v.s. Gate Voltage

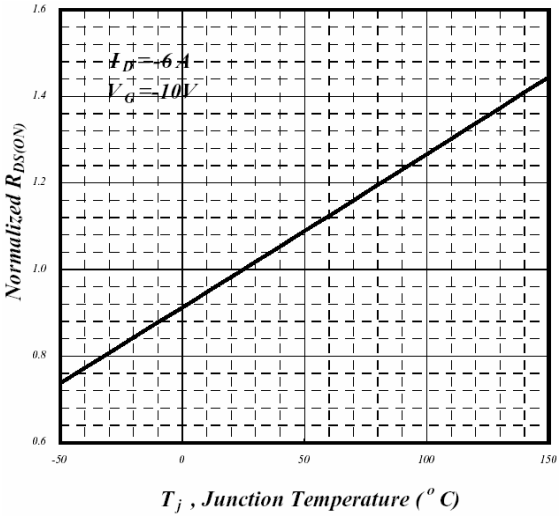

Fig 4. Normalized On-Resistance v.s. Junction Temperature

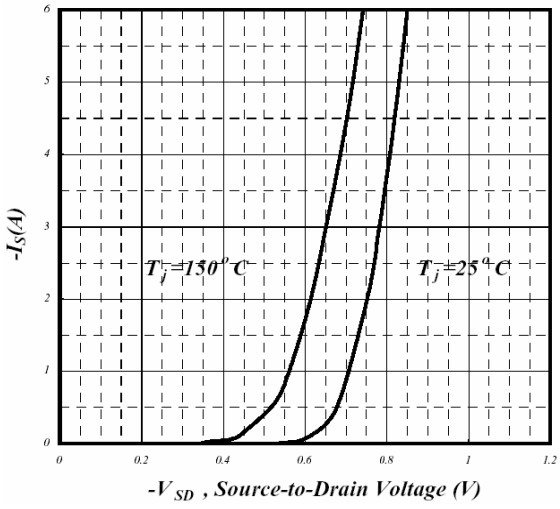

Fig 5. Forward Characteristics of Reverse Diode

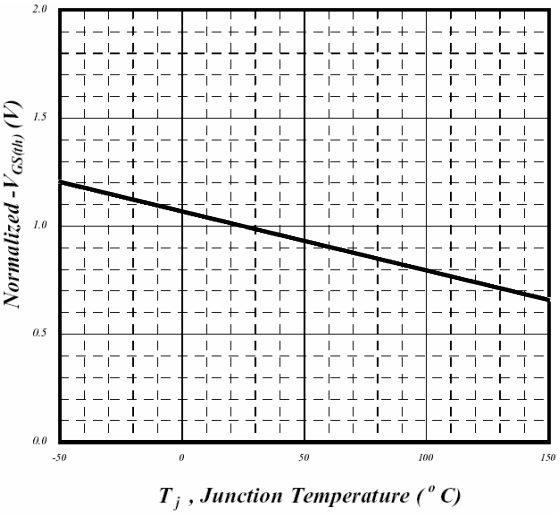

Fig 6. Gate Threshold Voltage v.s. Junction Temperature

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P-Channel

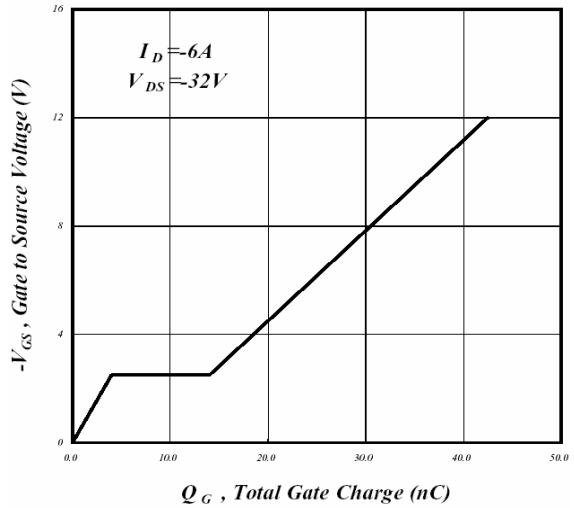


Fig 7. Gate Charge Characteristics

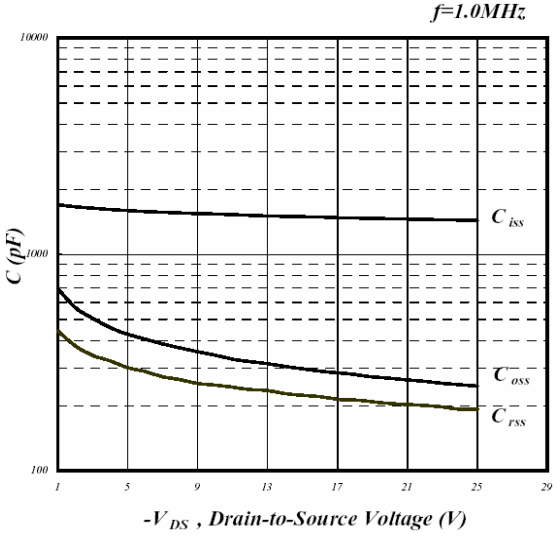
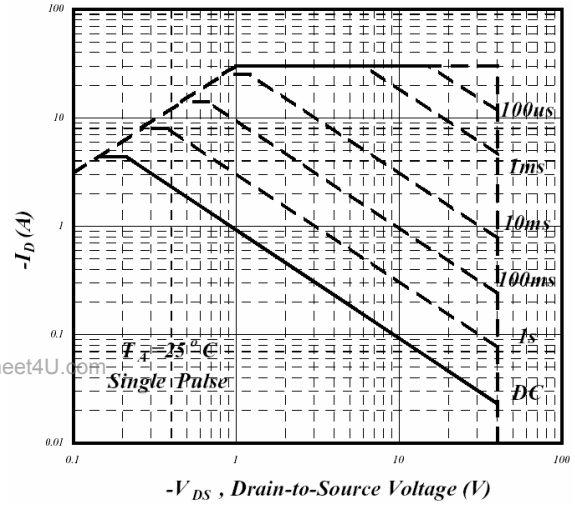


Fig 8. Typical Capacitance Characteristics



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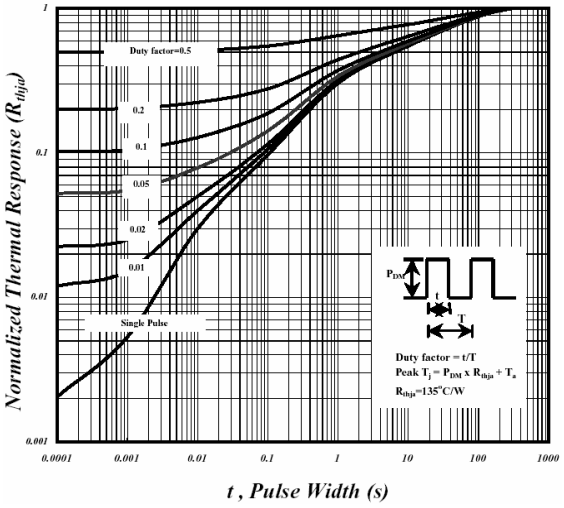

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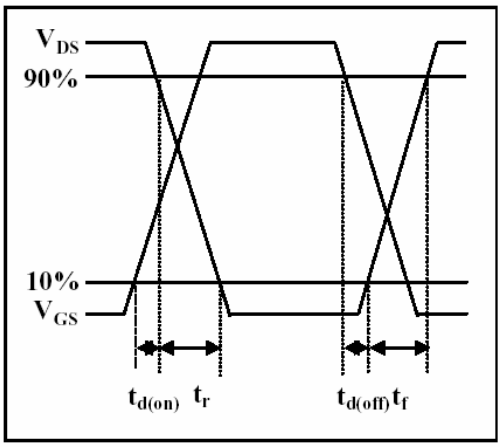

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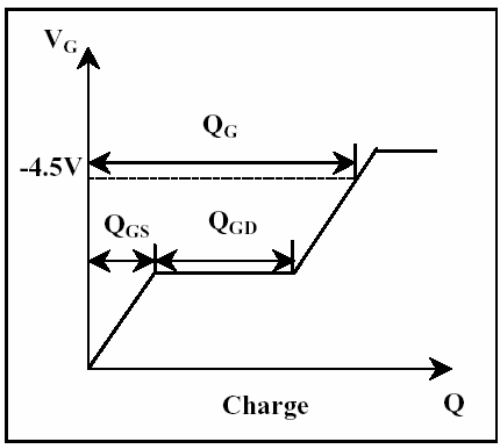

Fig 12. Gate Charge Waveform