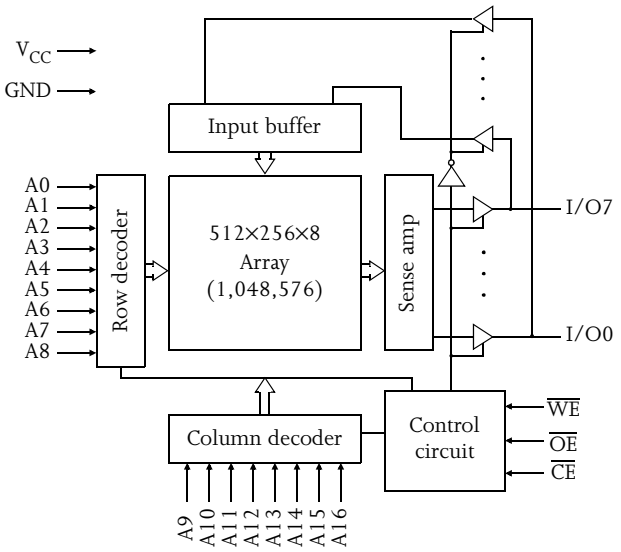
5V/3.3V 128K X 8 CMOS SRAM (Revolutionary pinout)

Features

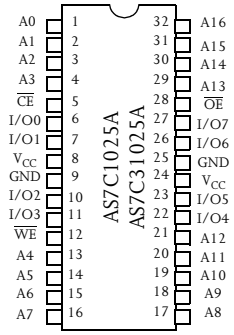
- AS7C1025A (5V version)
- AS7C31025A (3.3V version)
- Industrial and commercial temperatures
- Organization: 131,072 x 8 bits
- High speed
  - 10/10/12/15/20 ns address access time
  - 3/3/4/5 ns output enable access time
- Low power consumption: ACTIVE
  - 660 mW (AS7C1025A) / max @ 10 ns (5V)
  - 324 mW (AS7C31025A) / max @ 10 ns (3.3V)
- Low power consumption: STANDBY
  - 55 mW (AS7C1025A) / max CMOS (5V)
  - 36 mW (AS7C31025A) / max CMOS (3.3V)
- Latest 6T 0.25u CMOS technology
- 2.0V data retention
- Easy memory expansion with $\overline{CE}$, $\overline{OE}$ inputs
- Center power and ground
- TTL/LVTTL-compatible, three-state I/O
- JEDEC-standard packages
  - 32-pin, 300 mil SOJ
  - 32-pin, 400 mil SOJ
  - 32-pin, TSOP II
- ESD protection ≥ 2000 volts
- Latch-up current ≥ 200 mA

Logic block diagram

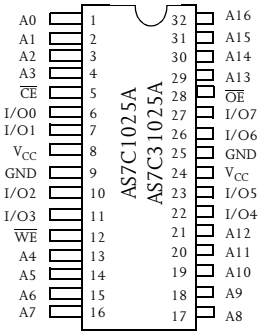


Pin arrangement

32-pin TSOP II



32-pin SOJ (300 mil)
32-pin SOJ (400 mil)



Selection guide

		AS7C1025A-10 AS7C31025A-10	AS7C1025A-12 AS7C31025A-12	AS7C1025A-15 AS7C31025A-15	AS7C1025A-20 AS7C31025A-20	Unit
Maximum address access time		10	12	15	20	ns
Maximum output enable access time		3	3	4	5	ns
Maximum operating current	AS7C1025A	120	110	100	100	mA
	AS7C31025A	90	80	80	80	mA
Maximum CMOS standby current	AS7C1025A	10	10	10	15	mA
	AS7C31025A	10	10	10	15	mA

Functional description

The AS7C1025A and AS7C31025A are high-performance CMOS 1,048,576-bit Static Random Access Memory (SRAM) devices organized as 131,072 x 8 bits. They are designed for memory applications where fast data access, low power, and simple interfacing are desired.

Equal address access and cycle times (t_{AA}, t_{RC}, t_{WC}) of 10/12/15/20 ns with output enable access times (t_{OE}) of 3/3/4/5 ns are ideal for high-performance applications. The chip enable input $\overline{CE}$ permits easy memory and expansion with multiple-bank memory systems.

When $\overline{CE}$ is high the devices enter standby mode. The standard AS7C1025A is guaranteed not to exceed 55 mW power consumption in standby mode. Both devices also offer 2.0V data retention.

A write cycle is accomplished by asserting write enable ($\overline{WE}$) and chip enable ($\overline{CE}$). Data on the input pins I/O0-I/O7 is written on the rising edge of $\overline{WE}$ (write cycle 1) or $\overline{CE}$ (write cycle 2). To avoid bus contention, external devices should drive I/O pins only after outputs have been disabled with output enable ($\overline{OE}$) or write enable ($\overline{WE}$).

A read cycle is accomplished by asserting output enable ($\overline{OE}$) and chip enable ($\overline{CE}$), with write enable ($\overline{WE}$) high. The chips drive I/O pins with the data word referenced by the input address. When either chip enable or output enable is inactive, or write enable is active, output drivers stay in high-impedance mode.

All chip inputs and outputs are TTL-compatible, and operation is from a single 5V supply (AS7C1025A) or 3.3V supply (AS7C31025A). The AS7C1025A and AS7C31025A are packaged in common industry standard packages.

Absolute maximum ratings

Parameter	Device	Symbol	Min	Max	Unit
Voltage on V_{CC} relative to GND	AS7C1025A	V_{t1}	−0.50	+7.0	V
	AS7C31025A	V_{t1}	−0.50	+5.0	V
Voltage on any pin relative to GND		V_{t2}	−0.50	V_{CC} + 0.5	V
Power dissipation		P_D	–	1.0	W
Storage temperature (plastic)		T_{stg}	−65	+150	°C
Ambient temperature with V_{CC} applied		T_{bias}	−55	+125	°C
DC current into outputs (low)		I_{OUT}	–	20	mA

NOTE: Stresses greater than those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Truth table

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	Data	Mode
H	X	X	High Z	Standby (I_{SB}, I_{SB1})
L	H	H	High Z	Output disable (I_{CC})
L	H	L	D_{OUT}	Read (I_{CC})
L	L	X	D_{IN}	Write (I_{CC})

Key: X = Don't Care, L = Low, H = High

Recommended operating conditions

Parameter	Device	Symbol	Min	Nominal	Max	Unit
Supply voltage	AS7C1025A	V_{CC}	4.5	5.0	5.5	V
	AS7C31025A	V_{CC}	3.0	3.3	3.6	V
Input voltage	AS7C1025A	V_{IH}	2.2	–	V_{CC} + 0.5	V
	AS7C31025A	V_{IH}	2.0	–	V_{CC} + 0.5	V
	Both	V_{IL}†	–0.5	–	0.8	V
Ambient operating temperature	commercial	T_A	0	–	70	°C
	industrial	T_A	–40	–	85	°C

†V_{IL} min. = –3.0V for pulse width less than $t_{RC}/2$.

DC operating characteristics (over the operating range)[1]

Parameter	Sym	Test conditions	Device	-10		-12		-15		-20		Unit
				Min	Max	Min	Max	Min	Max	Min	Max	
Input leakage current	$\lvert I_{LI} \rvert$	V_{CC} = Max, V_{IN} = GND to V_{CC}	Both	–	1	–	1	–	1	–	1	µA
Output leakage current	$\lvert I_{LO} \rvert$	V_{CC} = Max, $\overline{CE}$ = V_{IH}, V_{out} = GND to V_{CC}	Both	–	1	–	1	–	1	–	1	µA
Operating power supply current	I_{CC}	$\overline{CE}$ = V_{IL}, f = f_{Max}, I_{OUT} = 0 mA	AS7C1025A	–	120	–	110	–	100	–	100	mA
			AS7C31025A	–	90	–	80	–	80	–	80	
Standby power supply current[1]	I_{SB}	$\overline{CE}$ = V_{IH}, f = f_{Max}, f_{OUT} = 0	AS7C1025A	–	30	–	25	–	20	–	20	mA
			AS7C31025A	–	30	–	25	–	20	–	20	
	I_{SB1}	$\overline{CE} \geq V_{CC}$–0.2V, $V_{IN} \leq$ 0.2V or $V_{IN} \geq V_{CC}$ –0.2V, f = 0, f_{OUT} = 0	AS7C1025A	–	10	–	10	–	10	–	15	mA
			AS7C31025A	–	10	–	10	–	10	–	15	
Output voltage	V_{OL}	I_{OL} = 8 mA, V_{CC} = Min	AS7C1025A	–	.04	–	0.4	–	0.4	–	0.4	V
	V_{OH}	I_{OH} = –4 mA, V_{CC} = Min	AS7C31025A	2.4		2.4	–	2.4	–	2.4	–	V
Data retention current	I_{CCDR}	V_{CC} = 2.0V $\overline{CE} \geq V_{CC}$ – 0.2V $V_{IN} \geq V_{CC}$ – 0.2V or $V_{IN} \leq$ 0.2V	AS7C1025A	–	1	–	1	–	1		5	mA
			AS7C31025A	–	1	–	1	–	1	–	5	mA

Capacitance (f = 1 MHz, T_a = 25 °C, V_{CC} = NOMINAL)[2]

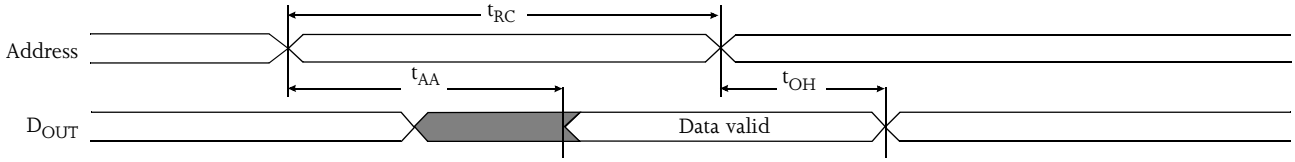
Parameter	Symbol	Signals	Test conditions	Max	Unit
Input capacitance	C_{IN}	A, $\overline{CE}$, $\overline{WE}$, $\overline{OE}$	V_{IN} = 0V	5	pF
I/O capacitance	$C_{I/O}$	I/O	V_{IN} = V_{OUT} = 0V	7	pF

Read cycle (over the operating range)[3,9]

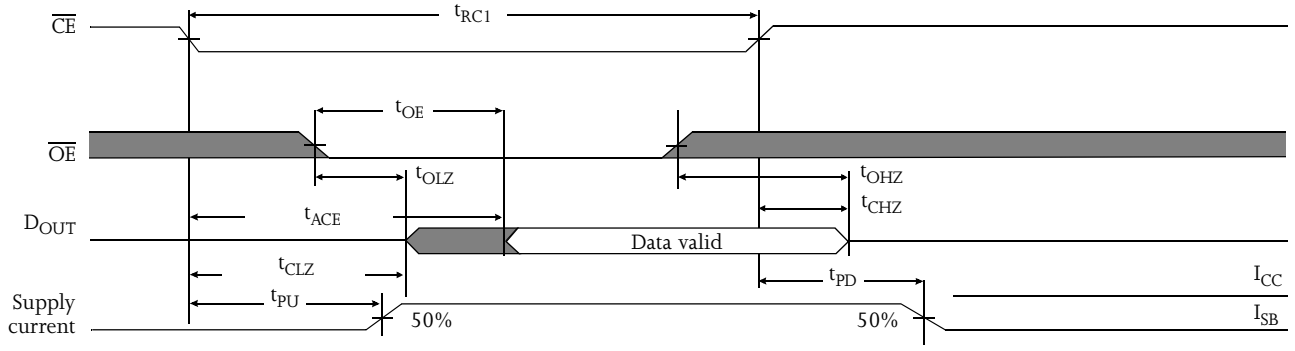
Parameter	Symbol	-10		-12		-15		-20		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Read cycle time	t_{RC}	10	–	12	–	15	–	20	–	ns	
Address access time	t_{AA}	–	10	–	12	–	15	–	20	ns	3
Chip enable ($\overline{CE}$) access time	t_{ACE}	–	10	–	12	–	15	–	20	ns	3
Output enable ($\overline{OE}$) access time	t_{OE}	–	3	–	3	–	4	–	5	ns	
Output hold from address change	t_{OH}	2	–	3	–	3	–	3	–	ns	5
$\overline{CE}$ Low to output in low Z	t_{CLZ}	0	–	0	–	0	–	0	–	ns	4, 5
$\overline{CE}$ Low to output in high Z	t_{CHZ}	–	3	–	3	–	4	–	5	ns	4, 5
$\overline{OE}$ Low to output in low Z	t_{OLZ}	0	–	0	–	0	–	0	–	ns	4, 5
$\overline{OE}$ High to output in high Z	t_{OHZ}	–	3	–	3	–	4	–	5	ns	4, 5
Power up time	t_{PU}	0	–	0	–	0	–	0	–	ns	4, 5
Power down time	t_{PD}	–	10	–	12	–	15	–	20	ns	4, 5

Key to switching waveforms

Read waveform 1 (address controlled)[3,6,7,9]



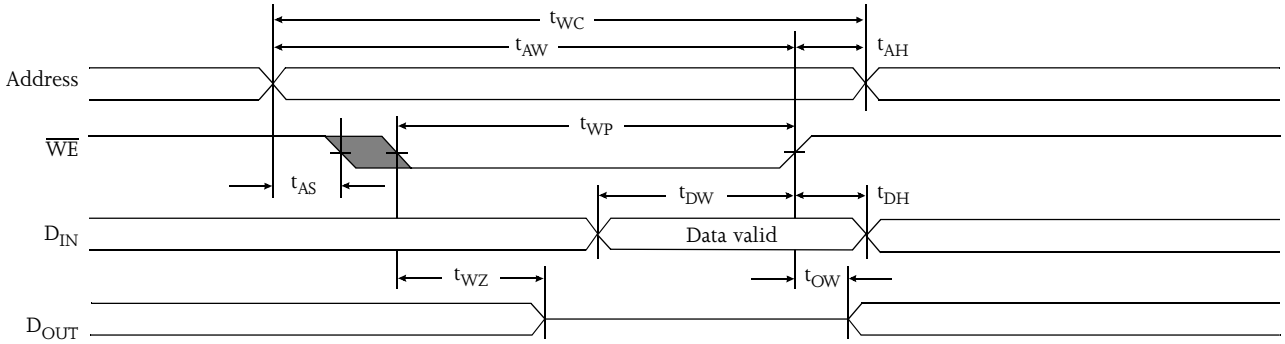
Read waveform 2 ($\overline{CE}$ and $\overline{OE}$ controlled)[3,6,8,9]



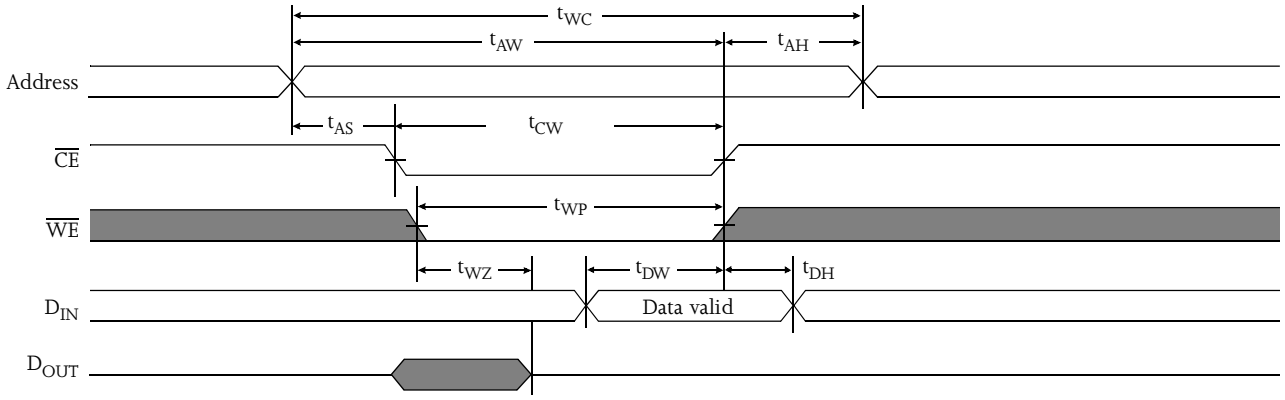
Write cycle (over the operating range)[11]

Parameter	Symbol	-10		-12		-15		-20		Unit	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Write cycle time	t_{WC}	10		12	–	15	–	20	–	ns	
Chip enable ($\overline{CE}$) to write end	t_{CW}	8		10	–	12	–	12	–	ns	
Address setup to write end	t_{AW}	8		9	–	10	–	12	–	ns	
Address setup time	t_{AS}	0		0	–	0	–	0	–	ns	
Write pulse width	t_{WP}	7		8	–	9	–	12	–	ns	
Address hold from end of write	t_{AH}	0		0	–	0	–	0	–	ns	
Data valid to write end	t_{DW}	5		6	–	8	–	10	–	ns	
Data hold time	t_{DH}	0		0	–	0	–	0	–	ns	4, 5
Write enable to output in high Z	t_{WZ}		6	–	6	–	6	–	8	ns	4, 5
Output active from write end	t_{OW}	1		1	–	1	–	2	–	ns	4, 5

Write waveform 1 ($\overline{WE}$ controlled)[10,11]



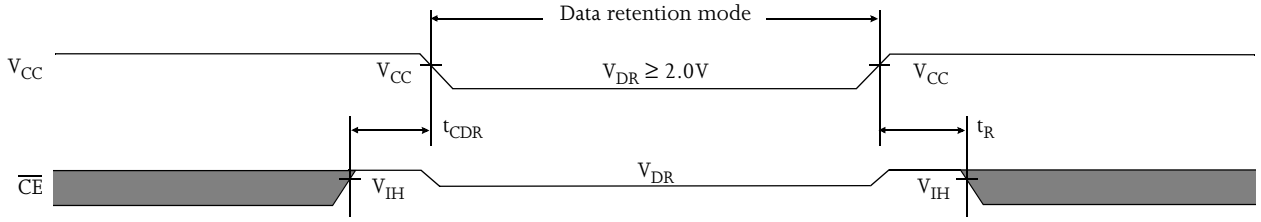
Write waveform 2 ($\overline{CE}$ controlled)[10,11]



Data retention characteristics (over the operating range)

Parameter	Symbol	Test conditions	Min	Max	Unit
V_{CC} for data retention	V_{DR}	V_{CC} = 2.0V $\overline{CE} \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$	2.0	–	V
Data retention current	I_{CCDR}		–	500	µA
Chip enable to data retention time	t_{CDR}		0	–	ns
Operation recovery time	t_R		t_{RC}	–	ns
Input leakage current	$\lvert I_{LI} \rvert$		–	1	µA

Data retention waveform



AC test conditions

- Output load: see Figure B or Figure C.
- Input pulse level: GND to 3.0V. See Figure A.
- Input rise and fall times: 2 ns. See Figure A.
- Input and output timing reference levels: 1.5V.

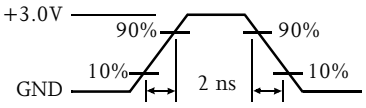


Figure A: Input pulse

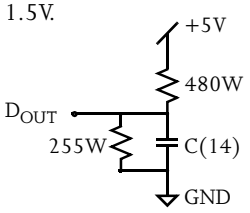


Figure B: 5V Output load

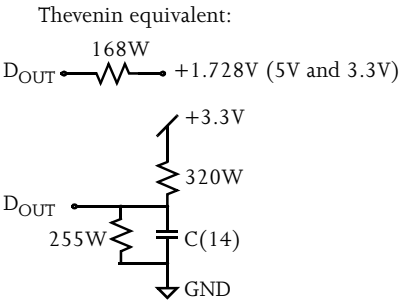


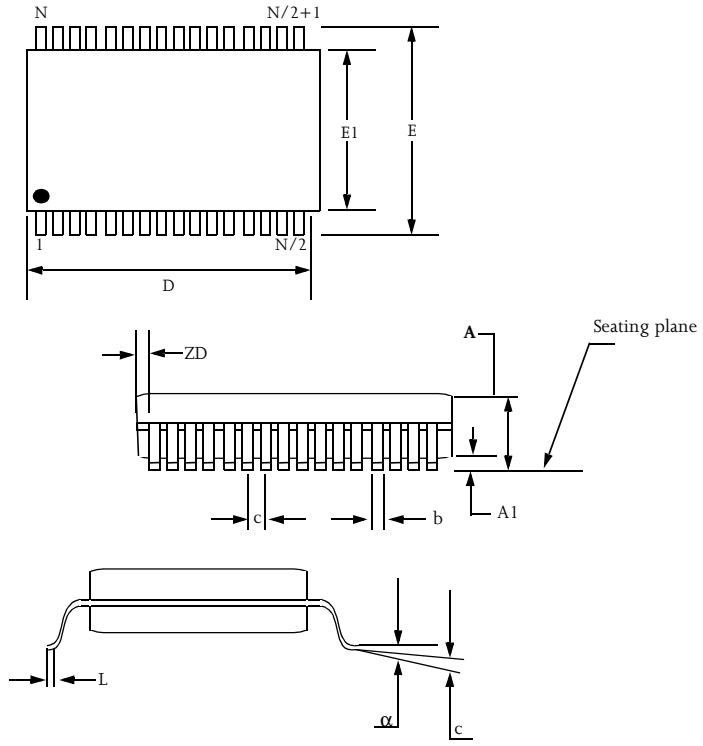
Figure C: 3.3V Output load

Notes

1 During V_{CC} power-up, a pull-up resistor to V_{CC} on $\overline{CE}$ is required to meet I_{SB} specification.
2 This parameter is sampled, but not 100% tested.
3 For test conditions, see *AC Test Conditions*, Figures A, B, and C.
4 t_{CLZ} and t_{CHZ} are specified with CL = 5pF, as in Figure C. Transition is measured ±500mV from steady-state voltage.
5 This parameter is guaranteed, but not 100% tested.
6 $\overline{WE}$ is High for read cycle.
7 $\overline{CE}$ and $\overline{OE}$ are Low for read cycle.
8 Address valid prior to or coincident with $\overline{CE}$ transition Low.
9 All read cycle timings are referenced from the last valid address to the first transitioning address.
10 $\overline{CE}$ or $\overline{WE}$ must be High during address transitions. Either $\overline{CE}$ or $\overline{WE}$ asserting high terminates a write cycle.
11 All write cycle timings are referenced from the last valid address to the first transitioning address.
12 NA.
13 C=30pF, except all high Z and low Z parameters, where C=5pF.

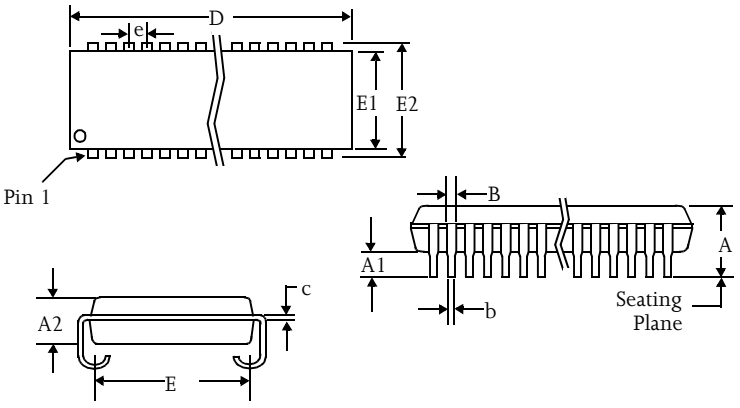
Package dimensions

32-pin TSOP II



Symbol	32-pin TSOP II (mm)	
	Min	Max
A	–	1.2
A1	0.05	0.15
b	0.3	0.52
C	0.12	0.21
D	20.82	21.08
E1	10.03	10.29
E	11.56	11.96
e	1.27 BSC	
L	0.40	0.60
ZD	0.95 REF.	
α	0°	5°

32-pin SOJ
300 mil/400 mil



Symbol	32-pin SOJ 300 mil		32-pin SOJ 400 mil	
	Min	Max	Min	Max
A	-	0.145	-	0.145
A1	0.025	-	0.025	-
A2	0.086	0.105	0.086	0.115
B	0.026	0.032	0.026	0.032
b	0.014	0.020	0.015	0.020
c	0.006	0.013	0.007	0.013
D	0.820	0.830	0.820	0.830
E	0.250	0.275	0.360	0.380
E1	0.292	0.305	0.395	0.405
E2	0.330	0.340	0.435	0.445
e	0.050 BSC		0.050 BSC	

Ordering codes

Package \ Access time	Voltage	Temperature	10 ns	12 ns	15 ns	20 ns
TSOP II	5V	Commercial	AS7C1025A-10TC	AS7C1025A-12TC	AS7C1025A-15TC	AS7C1025A-20TC
		Industrial	AS7C1025A-10TI	AS7C1025A-12TI	AS7C1025A-15TI	AS7C1025A-20TI
	3.3V	Commercial	AS7C31025A-10TC	AS7C31025A-12TC	AS7C31025A-15TC	AS7C31025A-20TC
		Industrial	AS7C31025A-10TI	AS7C31025A-12TI	AS7C31025A-15TI	AS7C31025A-20TI
300-mil SOJ	5V	Commercial	AS7C1025A-10TJC	AS7C1025A-12TJC	AS7C1025A-15TJC	AS7C1025A-20TJC
		Industrial	AS7C1025A-10TJI	AS7C1025A-12TJI	AS7C1025A-15TJI	AS7C1025A-20TJI
	3.3V	Commercial	AS7C31025A-10TJC	AS7C31025A-12TJC	AS7C31025A-15TJC	AS7C31025A-20TJC
		Industrial	AS7C31025A-10TJI	AS7C31025A-12TJI	AS7C31025A-15TJI	AS7C31025A-20TJI
400-mil SOJ	5V	Commercial	AS7C1025A-10JC	AS7C1025A-12JC	AS7C1025A-15JC	AS7C1025A-20JC
		Industrial	AS7C1025A-10JI	AS7C1025A-12JI	AS7C1025A-15JI	AS7C1025A-20JI
	3.3V	Commercial	AS7C31025A-10JC	AS7C31025A-12JC	AS7C31025A-15JC	AS7C31025A-20JC
		Industrial	AS7C31025A-10JI	AS7C31025A-12JI	AS7C31025A-15JI	AS7C31025A-20JI

Part numbering system

AS7C	X	1025	–XX	X	X
SRAM prefix	Blank=5V CMOS 3=3.3V CMOS	Device number	Access time	Package: T = TSOP II J = SOJ	Temperature range C = Commercial, 0°C to 70°C I = Industrial, -40°C to 85°C