



Winbond Bus Termination Regulator W83310S-R/N

Date: April 13, 2005 Revision: 1.0

W83310S-R/N



1. GENERAL DESCRIPTION

The W83310S-R/N is a linear regulator which provides achieves 1.5Amp bi-directional sinking and driving capability for DDR SDRAM bus terminator application. The chip simply implement a stable power supply which can track half of input power dynamically for bus terminator with a single chip; that is the chip integrates two power MOSFETs. There is no any external power device needed. The W83310S-R/N is promoted with small footprint 8-SOP 150mil package. With W83301S-R/N design, a high integration, high performance, and cost-effective solution is promoted.

2. FEATURES

- ❖ Regulates a bi-directional power with driving and sinking capability
- ❖ Provides achieve 1.5Amp driving and sinking current
- ❖ Power MOSFET integrated
- ❖ Low external component count
- ❖ Low output voltage offset
- ❖ Operates with +5V,+3.3V and +2.5V power
- ❖ Small package
- ❖ Low cost and easy to use

3. APPLICATIONS

- ❖ DDR Bus Termination Regulator
- ❖ Active Termination Bus
- ❖ SSTL-2
- ❖ SSTL-3

W83310S-R/N**4. PIN CONFIGURATION AND DESCRIPTION****- W83310S-R**

SYMBOL	PIN	FUNCTION
VIN	1	Power input pin.
GND	2	Ground.
VREF	3	Reference voltage and Chip enable.
VOUT	4	Output voltage.
VCNTL	5	Gate drive voltage.
VCNTL	6	Gate drive voltage.
VCNTL	7	Gate drive voltage.
VCNTL	8	Gate drive voltage.

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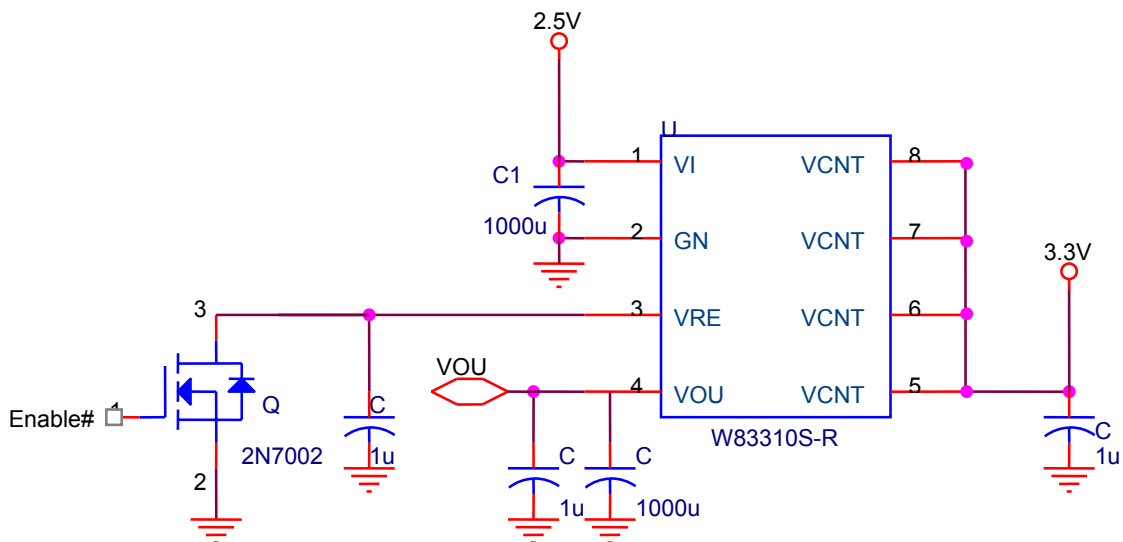
W83310S-R/N



SYMBOL	PIN	FUNCTION
N/C	1	No internal connection.
GND	2	Ground.
VSENSE	3	Feedback pin for regulating VTT.
VREF	4	Internal reference voltage of VDDQ/2.
VDDQ	5	Input for internal reference equal to VDDQ/2.
AVIN	6	Analog input pin.
PVIN	7	Power input pin.
VTT	8	Output voltage for connection to termination resistors.

5. APPLICATION CIRCUIT

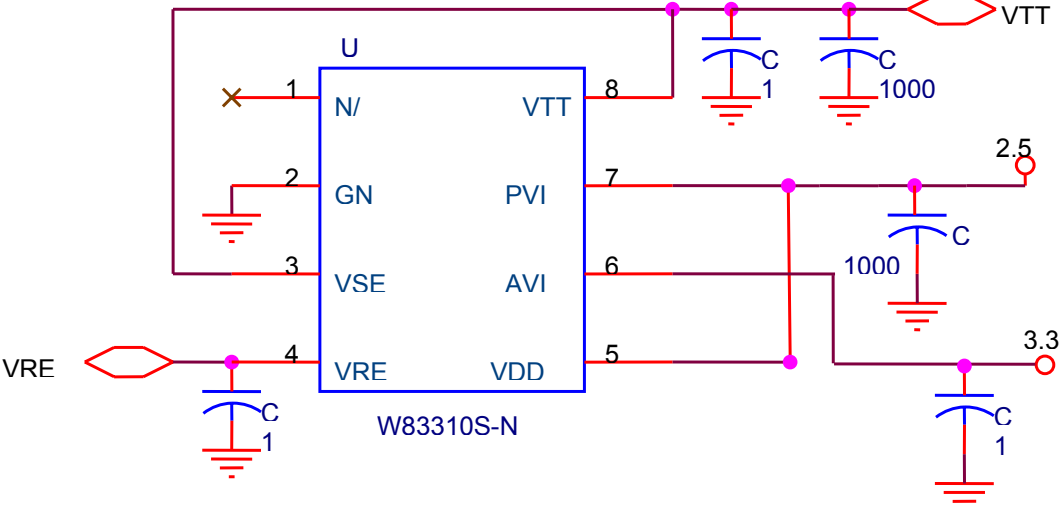
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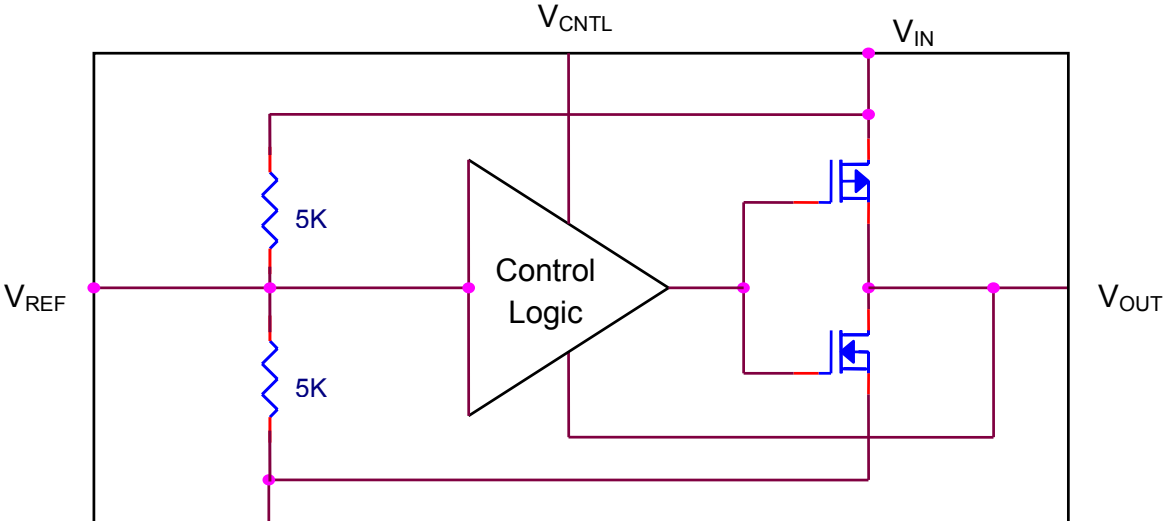




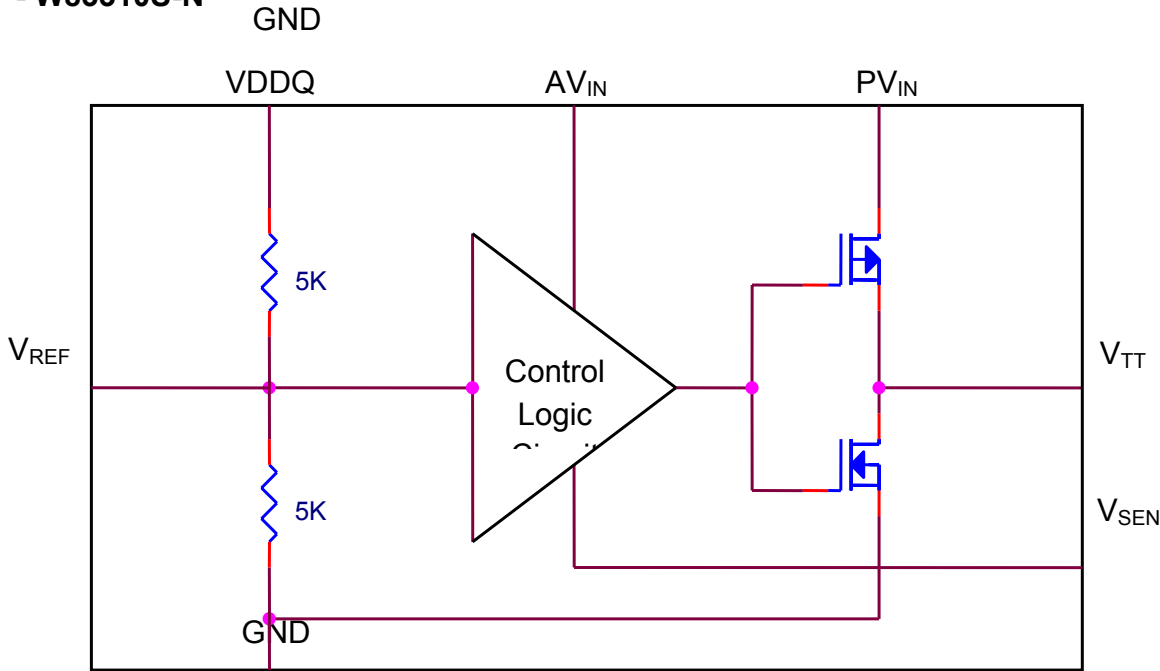
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6. INTERNAL BLOCK DIAGRAM

- W83310S-R



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7. ELECTRICAL CHARACTERISTICS

AC CHARACTERISTICS

W83310S-R						
$V_{IN}=2.5V, V_{CNTL}=3.3V, V_{REF}=1.25V, C_{out}=100\mu F, T_A = 0^\circ C \text{ to } +70^\circ C$						
Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Output Offset Voltage	V_{OS}	-5	0	+5	mV	$I_{OUT}=0A$
Load Regulation			0.8		%	Loading: $0A \rightarrow 1.5A$
			0.8			Loading: $0A \rightarrow -1.5A$
Input Voltage Range	V_{IN}		2.5		V	
	V_{CNTL}		3.3			
Operating Current of VCNTL	I_{CNTL}		0.5	1	mA	No Load ($I_{OUT}=0A$)
Shutdown Threshold Trigger		0.4			V	Output=High
				0.1	V	Output=Low
Shutdown Current	I_{SHDN}		10		μA	$V_{REF}<0.2V$ Loading=0.7A

Note: Load regulation is tested with a 10ms pulse current and measuring V_{OUT} .

W83310S-N						
$A_{VIN}=3.3V; P_{VIN}=2.5V \text{ is recommended}, V_{DDQ}=2.5V, V_{REF}=1.25V, C_{out}=100\mu F, T_A = 0^\circ C \text{ to } +70^\circ C$						
Parameter	Symbol	Min	Typ	Max	Units	Test Conditions
Output Offset Voltage	V_{OS}	-5	0	+5	mV	$I_{OUT}=0A$
Load Regulation			0.8		%	Loading: $0A \rightarrow 1.5A$
			0.8			Loading: $0A \rightarrow -1.5A$
Input Voltage Range	V_{DDQ}		2.5		V	
	P_{VIN}		2.5			
	A_{VIN}		3.3			
Operating Current of AVIN	I_{AVIN}		0.5	1	mA	No Load ($I_{OUT}=0A$)

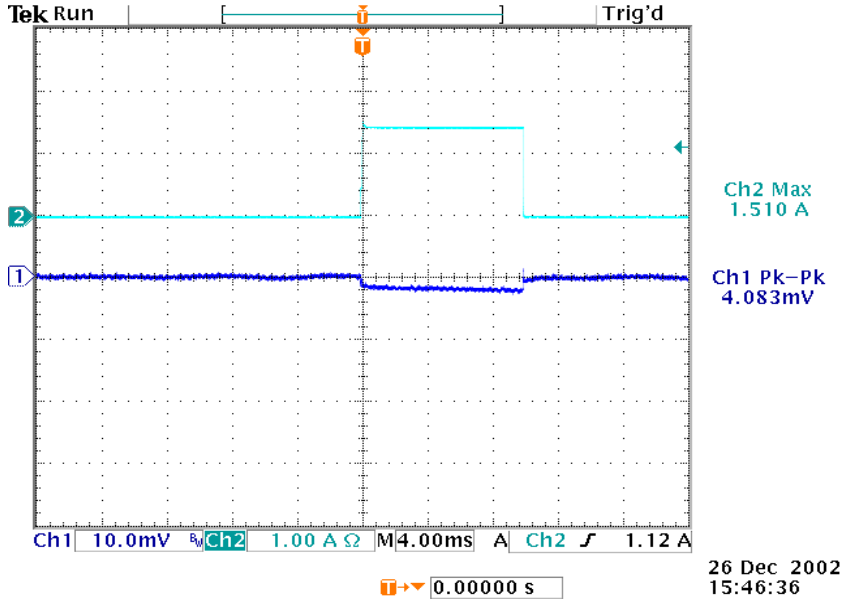
Note: Load regulation is tested with a 10ms pulse current and measuring V_{TT} .

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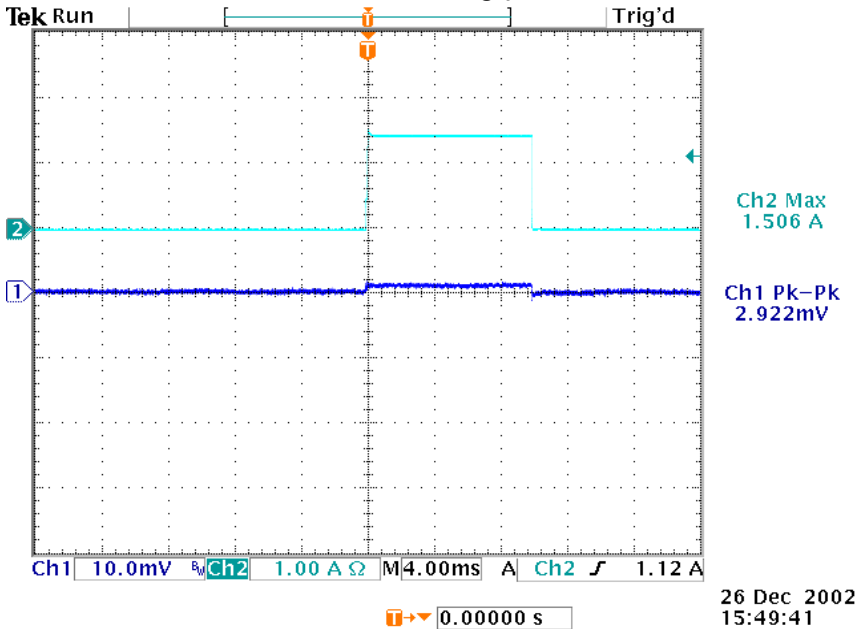


8. TYPICAL OPERATING WAVEFORM

W83310S-R V_{OUT} offset with a 1.5A/10ms driving pulse current.

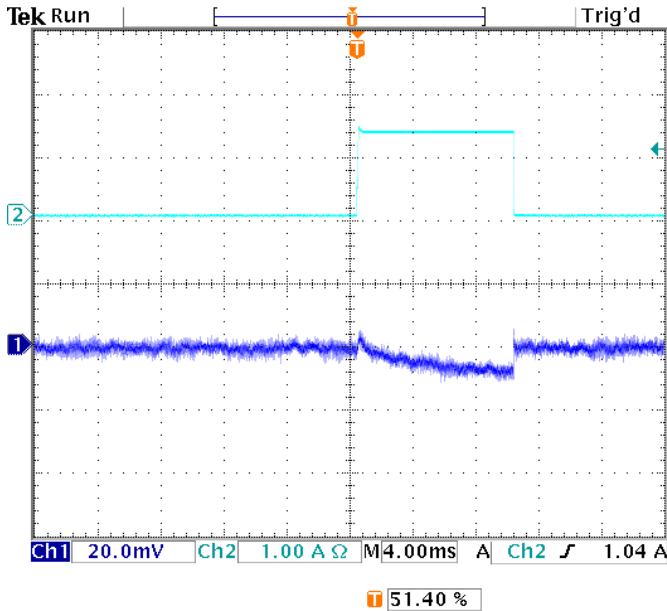


W83310S-R V_{OUT} offset with a 1.5A/10ms sinking pulse current.

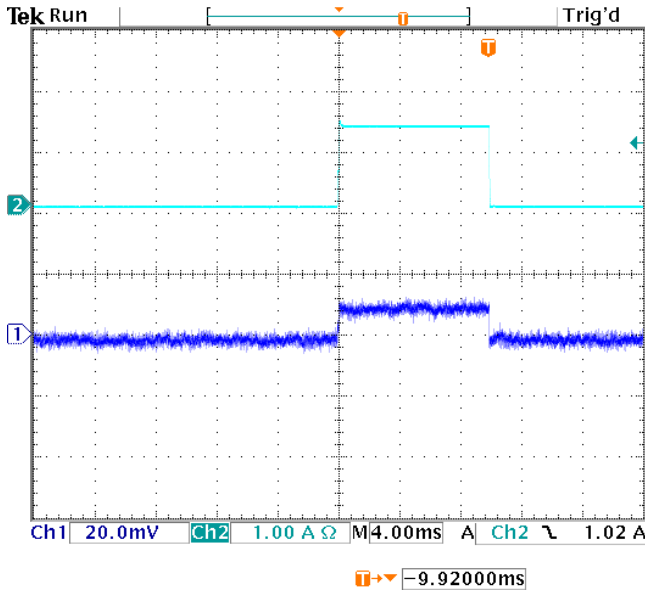


W83310S-N V_{TT} offset with a 1.5A/10ms driving pulse current.

W83310S-R/N

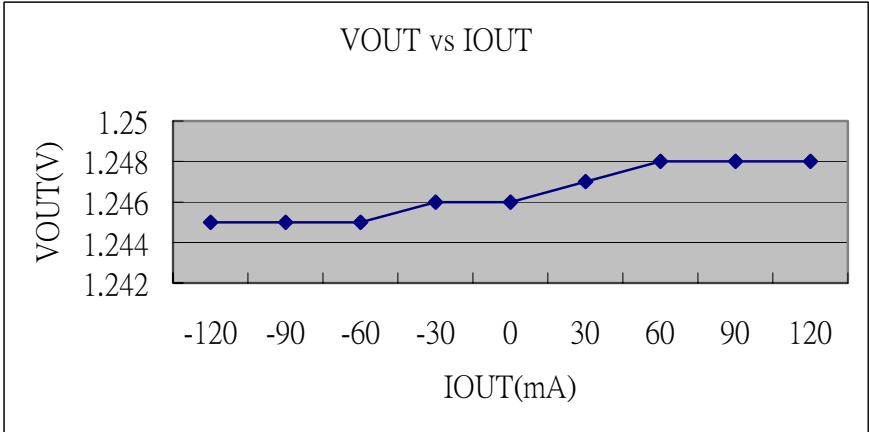


W83310S-N V_{TT} offset with a 1.5A/10ms sinking pulse current.



- Load regulation with various sinking/driving loading

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W83310S-R/N**10. ORDERING INFORMATION**

PART NUMBER	PACKAGE TYPE	PRODUCTION FLOW
W83310S-R	8PIN SOP	Commercial, 0°C to +70°C
W83310S-N	8PIN SOP	Commercial, 0°C to +70°C

11. HOW TO READ THE TOP MARKING

Left line: Winbond logo

1st & 2nd line: W83310S-R/N – the part number

3rd line: Tracking code Tracking code 249 O A

249: packages assembled in Year 02', week 49

O: assembly house ID; O means OSE, G means GR, etc.

B: the IC version

W83310S-R/N**12. REVISION HISTORY**

VERSION	DATE	PAGE	DESCRIPTION
0.51	12/2002	N.A.	The versions before 0.5 are only for internal reference.
0.60	02/2003	3	Recommend circuit update
0.61	03/2003	5	AC specification update
1.0	4/13/2005	12	Add disclaimer

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