

Absolute Maximum Ratings (Note 1)

Supply Voltage	-0.5V to 3.6V
Input Voltage (all inputs)	-0.3V to $V_{CC}+0.3V$
ESD Rating (HBM)	2kV

Input Coupling Capacitance	1.0 μF
Cable Input Voltage Swing (Note 5)	720 to 880 mV _{P-P}
Operating Free Air Temperature (T_A)	0°C to +70°C

Recommended Operating Conditions

Supply Voltage ($V_{CC} - V_{EE}$)	3.3V $\pm 5\%$
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DC Electrical Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified (Notes 2, 3).

Symbol	Parameter	Conditions	Reference	Min	Typ	Max	Units
V_{CMIN}	Input Common Mode Voltage		SDI, \overline{SDI}		1.75		V
V_{SDI}	Input Voltage Swing	0m cable length, differential, (Note 6)		720	800	950	mV _{P-P}
V_{CMOUT}	Output Common Mode Voltage		SDO, \overline{SDO}		$V_{CC} - V_{SDO}/2$		V
V_{SDO}	Output Voltage Swing	50 Ω load, differential			750		mV _{P-P}
	CLI DC Voltage	0m cable no signal	CLI		2.5 1.9		V V
	MUTE _{REF} DC Voltage (floating)		MUTE _{REF}		1.3		V
	MUTE _{REF} Range				0.69		V
	$\overline{CD}/MUTE$ Output Voltage	Carrier not present Carrier present	$\overline{CD}/MUTE$	2.6		1.2	V V
	$\overline{CD}/MUTE$ Input Voltage	Min to mute outputs Max to force outputs active		3.0		2.0	V V
I_{CC}	Supply Current				80	90	mA

AC Electrical Characteristics

Over Supply Voltage and Operating Temperature ranges, unless otherwise specified (Note 3).

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Symbol	Parameter	Conditions	Reference	Min	Typ	Max	Units
BR_{SDI}	Input Data Rate		SDI, \overline{SDI}	143		1485	Mbps
	Maximum Equalized Cable Length (with equalizer pathological)	270Mbps, Belden 1694A, 0.2UI output jitter			350		m
		270Mbps, Belden 8281, 0.2UI output jitter			280		m
		1.485Gbps, Belden 1694A, 0.25UI output jitter			140		m
		1.485Gbps, Belden 8281, 0.25UI output jitter			100		m
t_r, t_f	Output Rise Time, Fall Time	20% – 80%	SDO, \overline{SDO}		80	220	ps
	Mismatch in Rise/Fall Time					30	ps
t_{OS}	Output Overshoot	Note 4				10	%
R_{OUT}	Output Resistance	single-ended			50		Ω
RL_{IN}	Input Return Loss		SDI, \overline{SDI}	15	18-20		dB
R_{IN}	Input Resistance	single-ended			TBD		k Ω
C_{IN}	Input Capacitance	single-ended			1		pF

Note 1: "Absolute Maximum Ratings" are those parameter values beyond which the life and operation of the device cannot be guaranteed. The stating herein of these maximums shall not be construed to imply that the device can or should be operated at or beyond these values. The table of "Electrical Characteristics" specifies acceptable device operating conditions.

Note 2: Current flow into device pins is defined as positive. Current flow out of device pins is defined as negative. All voltages are stated referenced to $V_{EE} = 0$ Volts.

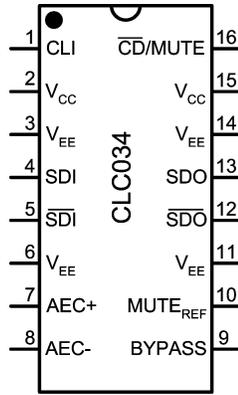
Note 3: Typical values are stated for $V_{CC} = +3.3V$ and $T_A = +25^\circ C$.

Note 4: Specification is guaranteed by design.

Note 5: These specifications assume an 800 mV_{P-P} signal at the cable input. Levels above and below 800 mV are allowable, but performance may vary. The cable will attenuate the signal prior to entering the equalizer.

Note 6: The maximum input voltage swing of 950 mV_{P-P} assumes a nonstressing, DC-balance signal; specifically, the SMPTE-recommended color bar test signal. Pathological or other stressing signals may not be used. This specification is for 0m cable only.

Connection Diagram



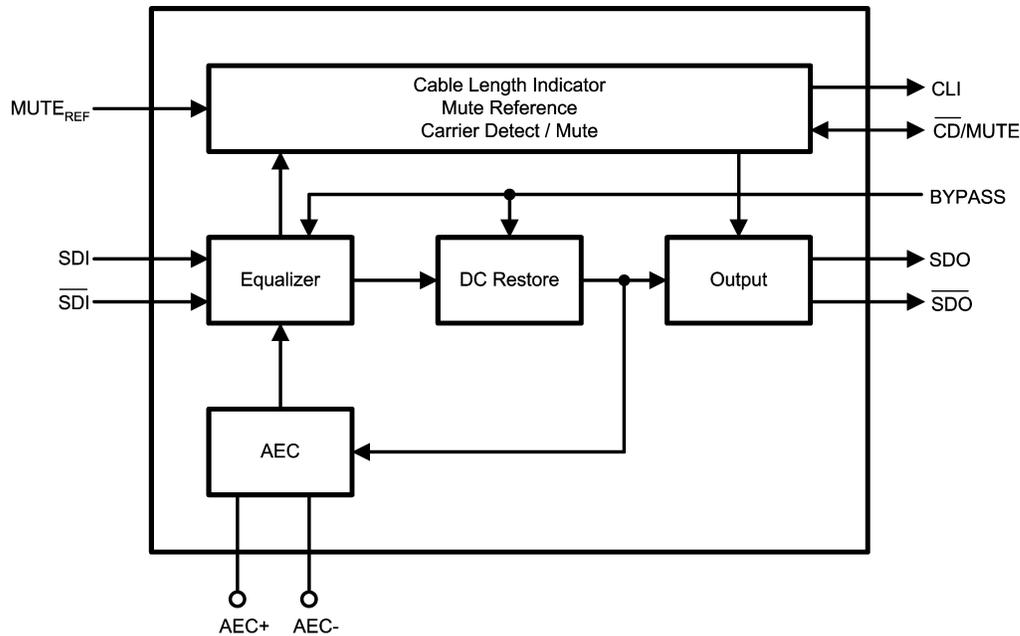
20085903

16-Pin SOIC
Order Number CLC034MA
See NS Package Number M16A

Pin Descriptions

Pin #	Name	Description
1	CLI	Cable length indicator. Provides a voltage proportional to the cable length being equalized.
2	V _{CC}	Positive power supply (+3.3V).
3	V _{EE}	Negative power supply (ground).
4	SDI	Serial data true input.
5	SDI _̄	Serial data complement input.
6	V _{EE}	Negative power supply (ground).
7	AEC+	AEC loop filter external capacitor (1μF) positive connection.
8	AEC-	AEC loop filter external capacitor (1μF) negative connection.
9	BYPASS	Bypasses equalization and DC restoration when high. No equalization occurs in this mode.
10	MUTE _{REF}	MUTE Reference. Determines the maximum cable to be equalized before muting.
11	V _{EE}	Negative power supply (ground).
12	SDO _̄	Serial data complement output.
13	SDO	Serial data true output.
14	V _{EE}	Negative power supply (ground).
15	V _{CC}	Positive power supply (+3.3V).
16	CD/MUTE	Bi-directional carrier detect and output mute. CD/MUTE is high when no signal is present. If unconnected, MUTE is controlled by the MUTE _{REF} setting. To force MUTE on, tie to V _{CC} . To disable MUTE, tie to GND. CD/MUTE has no function in BYPASS mode.

Block Diagram



20085902

Device Operation

BLOCK DESCRIPTION

The **Equalizer** block is a multi-stage adaptive filter. If Bypass is high, the equalizer is disabled.

The **DC Restore** block receives the differential signals from the equalizer filter block. This block incorporates a self-biasing DC restore circuit to fully DC restore the signals. If Bypass is high, this function is disabled.

The **Output** block produces SDO and \overline{SDO} .

The **Cable Length Indicator** provides a voltage to indicate the length of cable being equalized.

The **Mute Reference** determines the amount of cable to equalize before muting the outputs. This is set by applying a voltage proportional to the required length of cable. The higher the voltage, the lower the mute threshold.

Carrier Detect / Mute is bi-directional, serving two purposes. As an output, carrier detect monitors the signal power out of the equalizing filter and compares it to the mute reference to determine if a valid signal is present. Carrier detect provides a high voltage when no signal is present. Mute can be forced on or off by using this pin as an input.

Mute is forced off if this pin is tied to ground, and the outputs will always mute if this pin is tied to V_{CC} .

The loop response in the **AEC** block is controlled by an external $1\mu F$ capacitor placed across the $AEC+$ and $AEC-$ pins.

INPUT INTERFACING

The CLC034 accepts either differential or single-ended input. The input must be AC coupled. Transformer coupling is not supported.

The CLC034 correctly handles equalizer pathological signals for standard definition and high definition serial digital video, as described in SMPTE RP 178 and RP 198, respectively.

OUTPUT INTERFACING

The SDO and \overline{SDO} outputs are internally loaded with 50Ω . They produce a 750 mV_{P-P} differential output, or a 375 mV_{P-P} single-ended output.

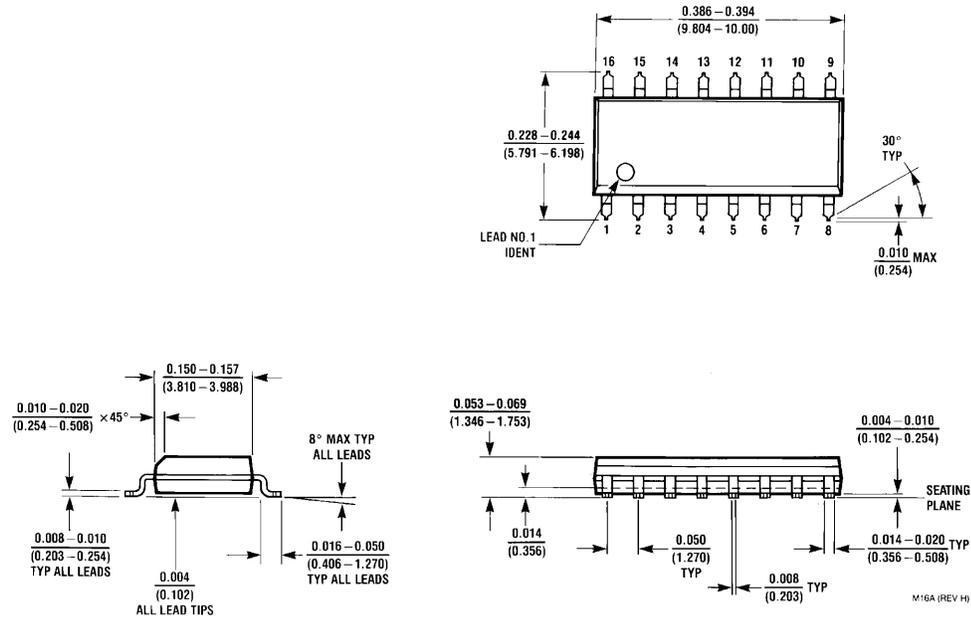
REPLACING THE GENNUM GS1524

The CLC034 is form-fit-function compatible with the Gennum GS1524.

Physical Dimensions inches (millimeters)

unless otherwise noted

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16-Pin SOIC
Order Number CLC034MA
NS Package Number M16A

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 Email: new.feedback@nsc.com
 Tel: 1-800-272-9959

National Semiconductor
Europe Customer Support Center
 Fax: +49 (0) 180-530 85 86
 Email: europe.support@nsc.com
 Deutsch Tel: +49 (0) 69 9508 6208
 English Tel: +44 (0) 870 24 0 2171
 Français Tel: +33 (0) 1 41 91 8790

National Semiconductor
Asia Pacific Customer Support Center
 Email: ap.support@nsc.com

National Semiconductor
Japan Customer Support Center
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