NEC

MOS INTEGRATED CIRCUIT

μPD78P018F

8-BIT SINGLE-CHIP MICROCOMPUTER

DESCRIPTION

The μPD78P018F is an 8-bit single-chip microcomputer which incorporates one-time PROM which can be written to once only, or EPROM to which programs can be written, erased and rewritten.

As the μPD78P018F is user-programmable, it is suitable for evaluation in system development, and for short-run and multiple device-production, and early start-up.

This document should be read in conjunction with documentation on the mask ROM products.

FEATURES

- Pin compatible with mask ROM products (except V_{PP} pin)
- Internal PROM: 60K bytes***1**
- Internal high-speed RAM: 1024 bytes***1**
- Internal expansion RAM : 1024 bytes***2**
- Buffer RAM: 32 bytes
- Operable over same supply voltage range as mask ROM product (2.0 to 6.0 V)

* **1.** The internal PROM and internal high-speed RAM size can be changed by means of the memory size switching register.

2. The capacity of the internal expansion RAM can be changed by means of the internal expansion RAM switching register.

Differences from mask ROM products are as follows:

- The same memory mapping as on a mask ROM product is possible by setting the memory size switching register and the internal expansion RAM switching register.
- There is no function for incorporating pull-up resistors by means of a mask option.

In this document, the common parts of the one-time PROM product and EPROM product are represented by PROM.

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ORDERING INFORMATION

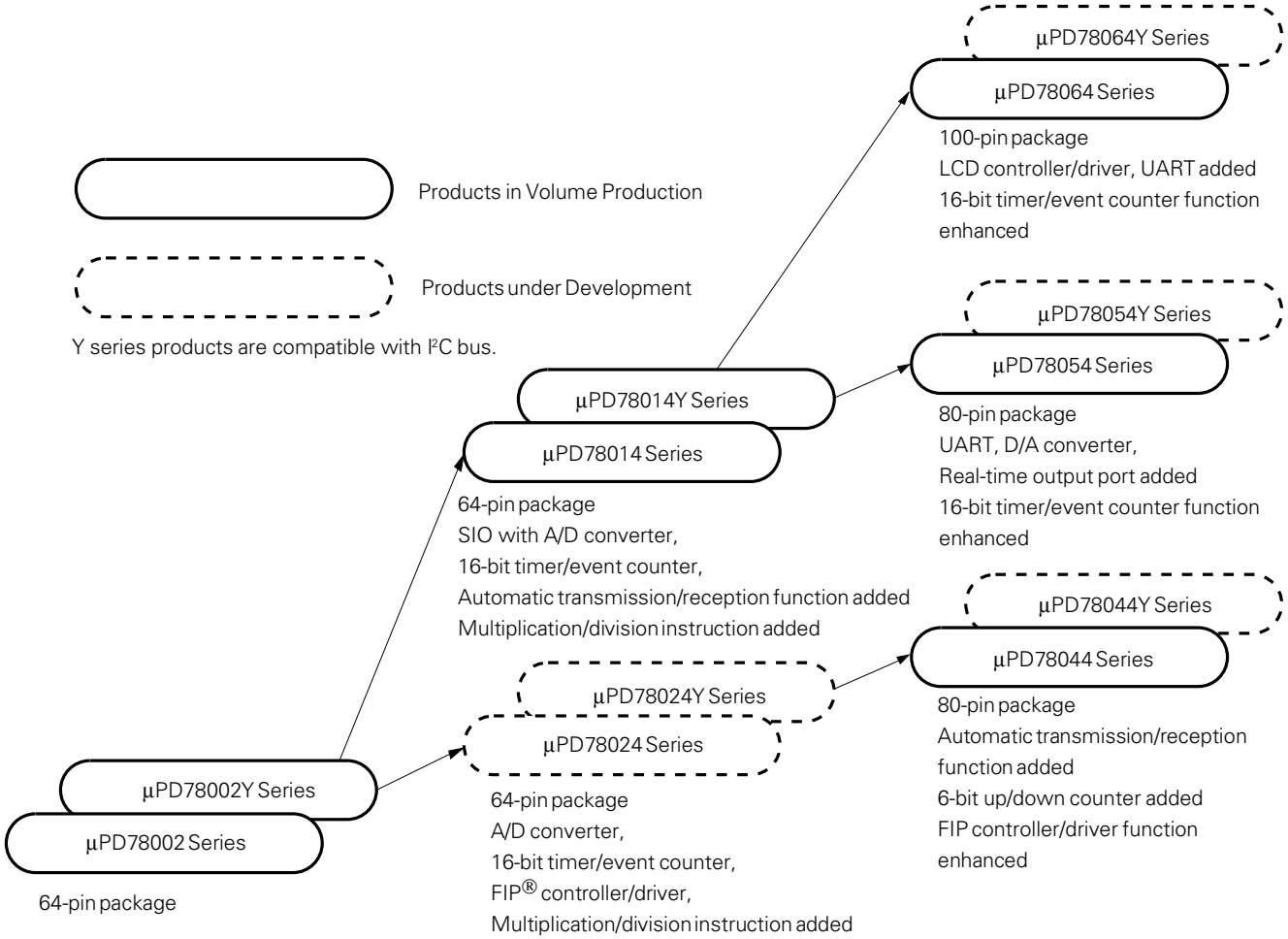
Ordering Code	Package	Internal ROM
μPD78P018FCW	64-pin plastic shrink DIP (750 mil)	One-time PROM
μPD78P018FDW	64-pin ceramic shrink DIP (with window) (750 mil)	EPROM
μPD78P018FGC-AB8	64-pin plastic QFP (□14 mm)	One-time PROM
μPD78P018FGK-8A8	64-pin plastic QFP (□12 mm)	One-time PROM
μPD78P018FKK-S	64-pin ceramic WQFN (□14 mm)	EPROM

QUALITY GRADE

Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

78K/0 SERIES DEVELOPMENT



OUTLINE OF FUNCTION

Item		Function
Internal memory		• PROM : 60K bytes*1 • RAM Internal high-speed RAM : 1024 bytes*1 Internal expansion RAM : 1024 bytes*2 Buffer RAM : 32 bytes
Memory space		64K bytes
General registers		8 bits × 32 registers (8 bits × 8 registers × 4 banks)
Instruction cycle		On-chip instruction execution time cycle modification function
	Main system clock selected	0.48 μs/0.8 μs/1.6 μs/3.2 μs/6.4 μs (at 10.0 MHz operation)
	Subsystem clock selected	122 μs (at 32.768 kHz operation)
Instruction set		• 16-bit operation • Multiplication/division (8 bits × 8 bits,16 bits ÷ 8 bits) • Bit manipulation (set, reset, test, boolean operation) • BCD correction, etc.
I/O ports		Total : 53 • CMOS input : 2 • CMOS I/O : 47 • N-channel open-drain I/O (15 V withstand voltage) : 4
A/D converter		• 8-bit resolution × 8 channels • Operable over a wide power supply voltage range: V_{DD} = 2.0 to 6.0 V
Serial interface		• 3-wire/SBI/2-wire mode selectable : 1 channel • 3-wire mode (on-chip max. 32 bytes automatic data transmit/receive function) : 1 channel
Timer		• 16-bit timer/event counter : 1 channel • 8-bit timer/event counter : 2 channels • Clock timer : 1 channel • Watchdog timer : 1 channel
Timer output		3 (14-bit PWM output × 1)
Clock output		39.1 kHz, 78.1 kHz, 156 kHz, 313 kHz, 625 kHz, 1.25 MHz (at main system clock 10.0 operation) 32.768 kHz (at subsystem clock 32.768 kHz operation)
Buzzer output		2.4 kHz, 4.9 kHz, 9.8 kHz (at main system clock 10.0 MHz operation)
Vectored interrupts	Maskable	Internal : 8, External : 4
	Non-maskable	Internal : 1
	Software	Internal : 1
Test input		Internal : 1, External : 1
Operating voltage range		V_{DD} = 2.0 to 6.0 V
Operating tempreture range		-40 to +80 °C
Package		• 64-pin plastic shrink DIP (750 mil) • 64-pin ceramic shrink DIP (with window) (750 mil) • 64-pin plastic QFP (□14 mm) • 64-pin plastic QFP (□12 mm) • 64-pin ceramic WQFN (□14 mm)

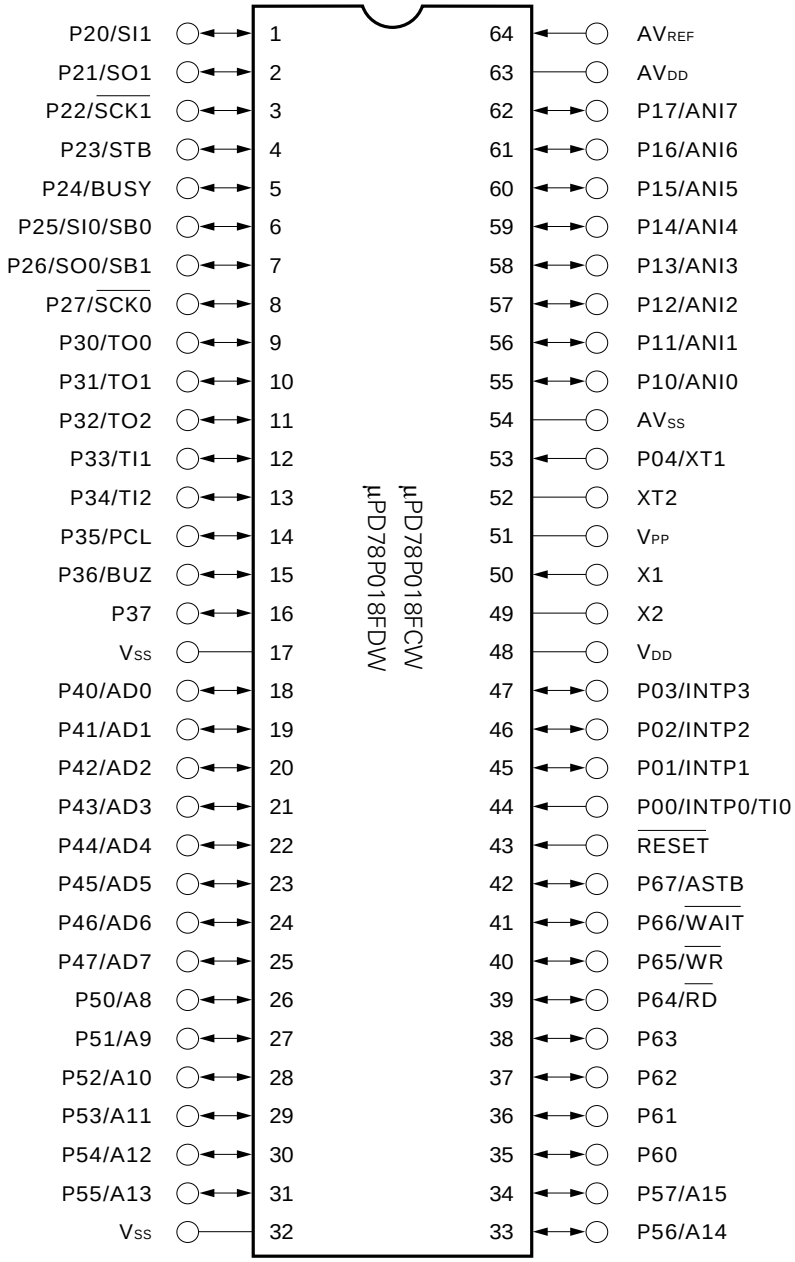
* **1.** The capacity of the internal PROM and internal high-speed RAM can be changed by means of the memory size switching register.

2. The capacity of the internal expansion RAM can be changed by means of the internal expansion RAM switching register.

PIN CONFIGURATION (TOP VIEW)

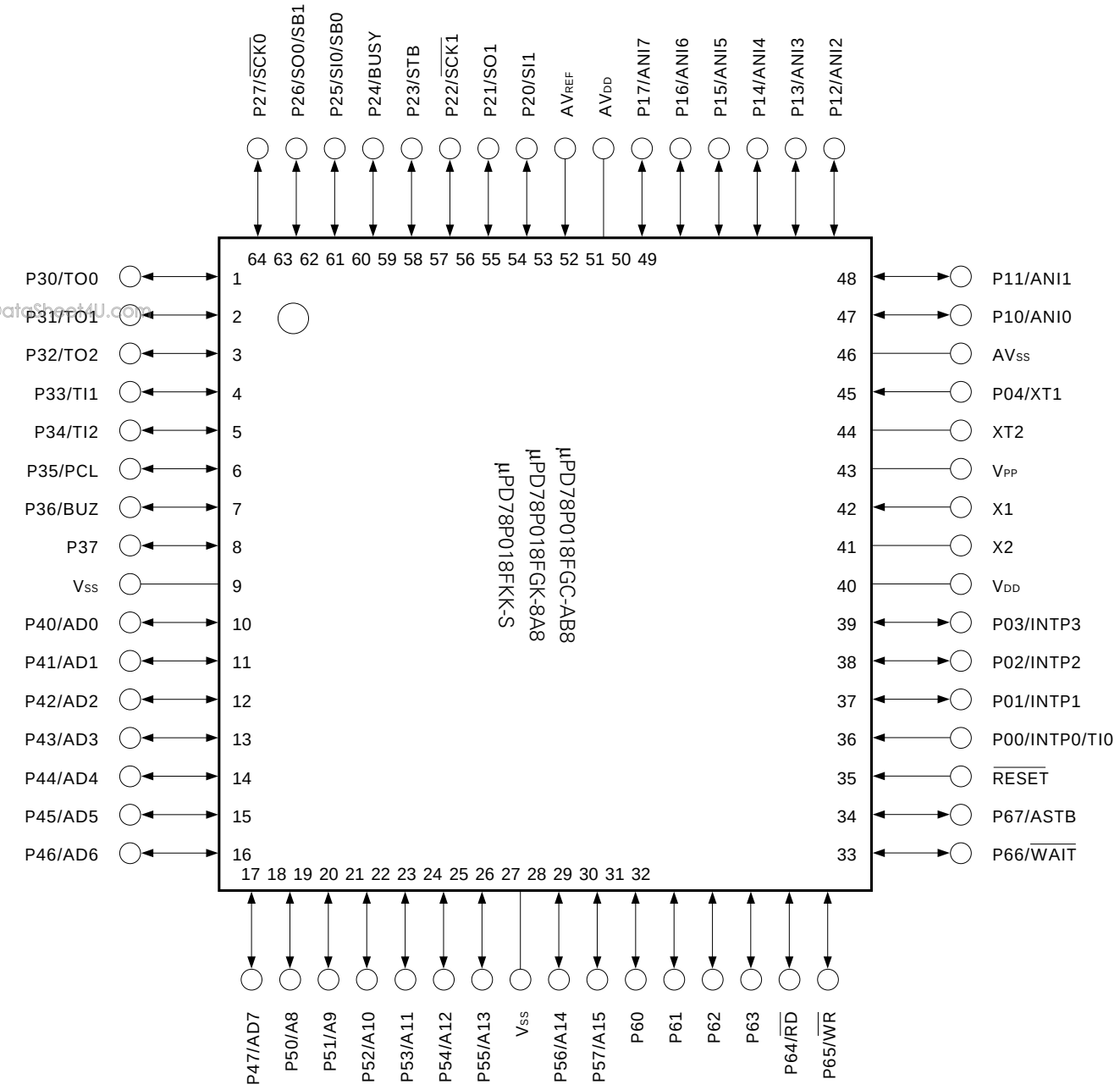
(1) Normal operating mode

64-pin plastic shrink DIP (750 mil)
64-pin ceramic shrink DIP (with window) (750 mil)



Note 1. V_{PP} pin should be connected to V_{SS}.
2. AV_{DD} pin should be connected to V_{DD}.
3. AV_{SS} pin should be connected to V_{SS}.

64-pin plastic QFP (□14 mm)
64-pin plastic QFP (□12 mm)
64-pin ceramic WQFN (□14 mm)



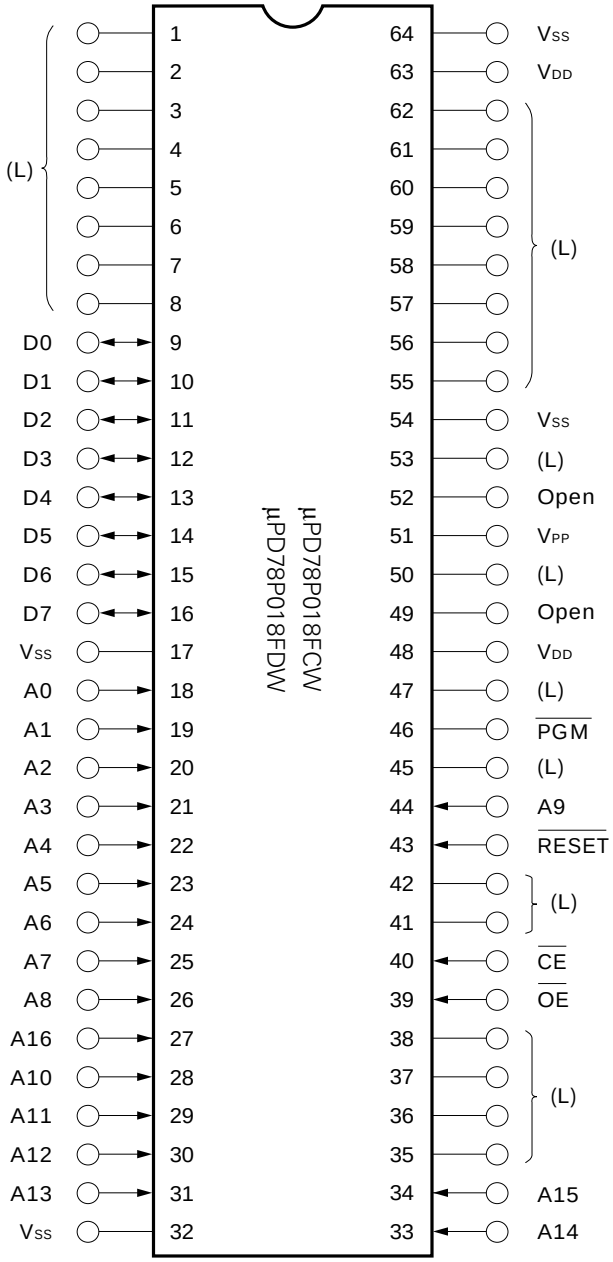
Note 1. V_{PP} pin should be connected to V_{SS}.
2. AV_{DD} pin should be connected to V_{DD}.
3. AV_{SS} pin should be connected to V_{SS}.

P00 to P04 : Port 0
P10 to P17 : Port 1
P20 to P27 : Port 2
P30 to P37 : Port 3
P40 to P47 : Port 4
P50 to P57 : Port 5
P60 to P67 : Port 6
INTP0 to INTP3 : Interrupt From Peripherals
TI0 to TI2 : Timer Input
TO0 to TO2 : Timer Output
SB0, SB1 : Serial Bus
SI0, SI1 : Serial Input
SO0, SO1 : Serial Output
$\overline{SCK0}$, $\overline{SCK1}$: Serial Clock
PCL : Programmable Clock
BUZ : Buzzer Clock
STB : Strobe
BUSY : Busy

AD0 to AD7 : Address/Data Bus
A8 to A15 : Address Bus
$\overline{RD}$: Read Strobe
$\overline{WR}$: Write Strobe
$\overline{WAIT}$: Wait
ASTB : Address Strobe
X1, X2 : Crystal (Main System Clock)
XT1, XT2 : Crystal (Subsystem Clock)
$\overline{RESET}$: Reset
ANI0 to ANI7 : Analog Input
AV_{DD} : Analog Power Supply
AV_{SS} : Analog Ground
AV_{REF} : Analog Reference Voltage
V_{DD} : Power Supply
V_{PP} : Programming Power Supply
V_{SS} : Ground

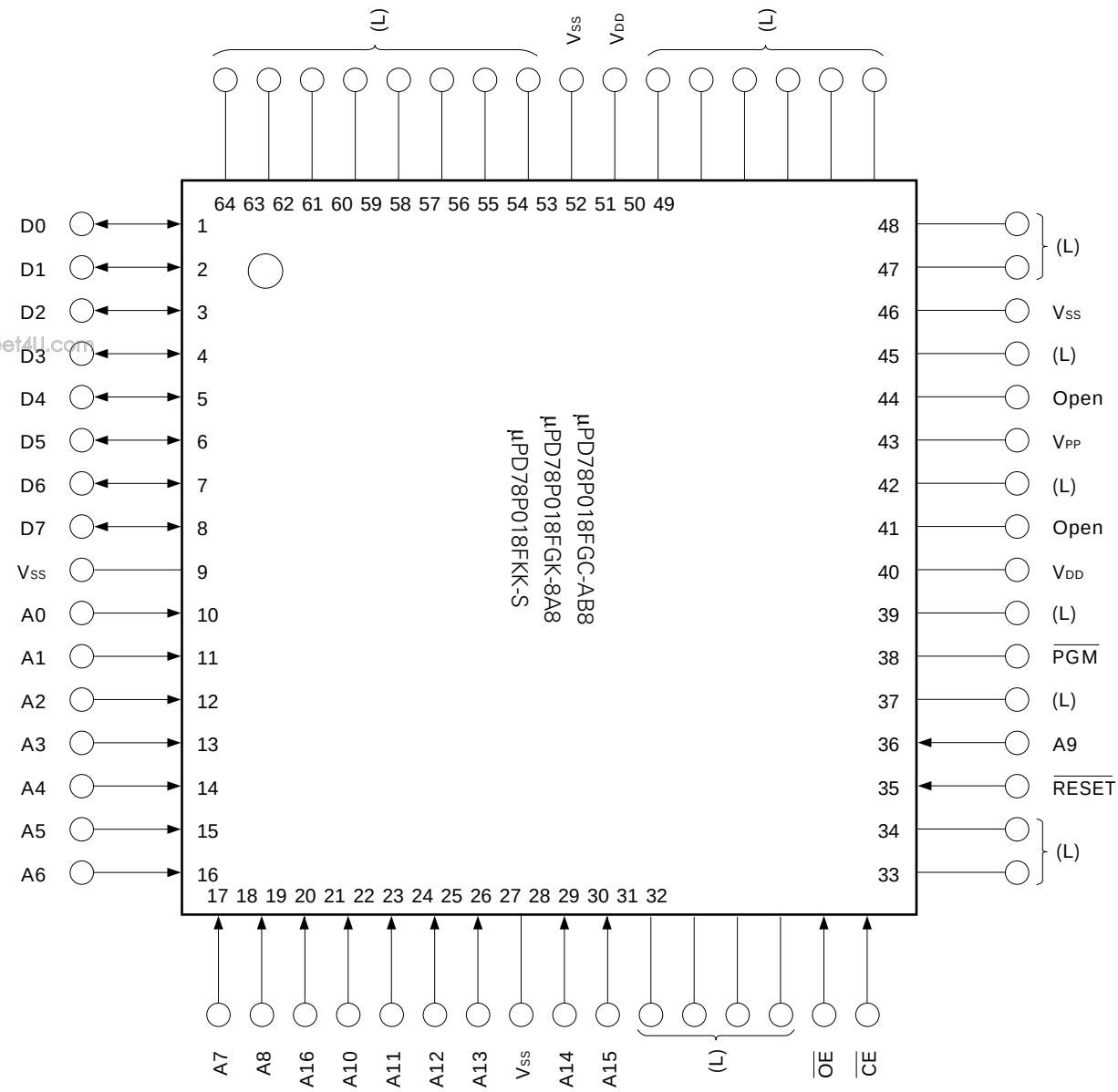
(2) PROM programming mode

64-pin plastic shrink DIP (750 mil)
64-pin ceramic shrink DIP (with window) (750 mil)



Note 1. (L) : Connect to VSS individually with a pull-down resistor.
2. VSS : Connect to ground.
3. $\overline{\text{RESET}}$: Set to low level.
4. Open : Do not make any connection.

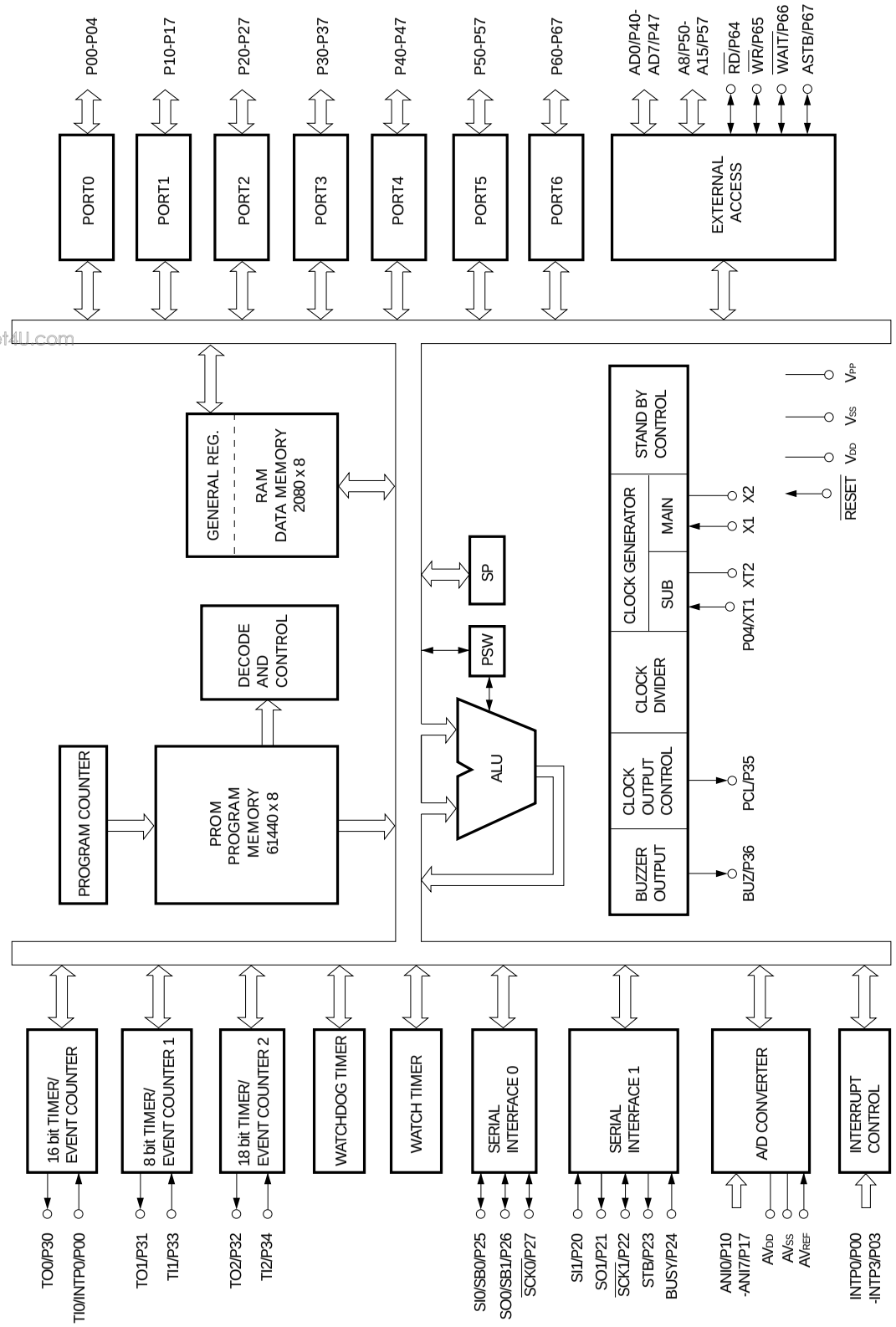
64-pin plastic QFP (□14 mm)
64-pin plastic QFP (□12 mm)
64-pin ceramic WQFN (□14 mm)



Note 1. (L) : Connect to V_{SS} individually with a pull-down resistor.
2. V_{SS} : Connect to ground.
3. RESET : Set to low level.
4. Open : Do not make any connection.

A0 to A16	: Address	$\overline{RESET}$	: Reset
D0 to D7	: Data Bus	V_{DD}	: Power Supply
$\overline{CE}$	: Chip Enable	V_{PP}	: Programming Power Supply
$\overline{OE}$	: Output Enable	V_{SS}	: Ground
$\overline{PGM}$	: Program		

BLOCK DIAGRAM



CONTENTS

1. DIFFERENCES BETWEEN μPD78P018F AND MASK ROM PRODUCT

The μPD78P018F incorporates one-time PROM which can be written to once only, or EPROM to which programs can be written, erased and rewritten.

By setting the memory size switching register and internal expansion RAM switching register it is possible to make the functions of this device, except for the PROM specification and mask option for pins P60 to P63, identical to those of a mask ROM product.

The differences between the μPD78P018F and mask ROM products are shown in Table 1-1.

Table 1-1 Differences Between μPD78P018F and Mask ROM Product

Item	μPD78P018F	Mask ROM Product
IC pin	No	Yes
V_{PP} pin	Yes	No
Mask option for pins P60 to P63	No mask option for incorporation of pull-up resistor	Pull-up resistor incorporation possible by means of mask option

Note 1. In the μPD78P018F, the capacity of the internal PROM and internal high-speed RAM can be changed by means of the memory size switching register.
After $\overline{\text{RESET}}$ input, the internal PROM capacity is 60K bytes, and the internal high-speed RAM capacity is 1K bytes.

2. In the μPD78P018F, the capacity of the internal expansion RAM can be changed by means of the internal expansion RAM switching register.
The internal expansion RAM is set to 1K bytes by means of $\overline{\text{RESET}}$ input.

2. PIN FUNCTIONS

2.1 NORMAL OPERATING MODE PINS

(1) Port pins (1/2)

Pin Name	I/O	Function		After Reset	Dual-Function Pin
P00	Input	Port 0 5-bit I/O port	Input only	Input	INTP0/TI0
P01	Input/output		Input/output can be specified in 1-bit unit. When used as an input port, pull-up resistor can be used by software.	Input	INTP1
P02					INTP2
P03					INTP3
P04***1**	Input		Input only	Input	XT1
P10 to P17	Input/output	Port 1 8-bit input/output port. Input/output can be specified in 1-bit unit. When used as an input port, pull-up resistor can be used by software.***2**		Input	ANI0 to ANI7
P20	Input/output	Port 2 8-bit input/output port. Input/output can be specified in 1-bit unit. When used as an input port, pull-up resistor can be used by software.		Input	SI1
P21					SO1
P22					$\overline{SCK1}$
P23					STB
P24					BUSY
P25					SI0/SB0
P26					SO0/SB1
P27					$\overline{SCK0}$
P30	Input/output	Port 3 8-bit input/output port. Input/output can be specified in 1-bit unit. When used as an input port, pull-up resistor can be used by software.		Input	TO0
P31					TO1
P32					TO2
P33					TI1
P34					TI2
P35					PCL
P36					BUZ
P37					—
P40 to P47	Input/output	Port 4 8-bit input/output port. Input/output can be specified in 8-bit unit. When used as an input port, pull-up resistor can be used by software. Test flag (KRIF) is set to 1 by falling edge detection.		Input	AD0 to AD7

* **1.** When using the P04/XT1 pins as an input port, set 1 in bit 6 (FRC) of the processor clock control register and do not use the internal feedback resistor of the subsystem clock oscillator.

2. When pins P10/ANI0 to P17/ANI7 are used as analog inputs of the A/D converter, the use of the pull-up resistor is automatically disabled.

(1) Port Pins (2/2)

Pin Name	I/O	Function		After Reset	Dual-Function Pin
P50 to P57	Input/output	Port 5 8-bit input/output port. LED can be driven directly. Input/output can be specified in 1-bit unit. When used as an input port, pull-up resistor can be used by software.		Input	A8 to A15
P60	Input/output	Port 6 8-bit input/output port. Input/output can be specified in 1-bit unit.	N-ch open-drain input/output port. LED can be driven directly.	Input	—
P61					
P62					
P63					
P64			When used as an input port, pull-up resistor can be used by software.		$\overline{RD}$
P65					$\overline{WR}$
P66					$\overline{WAIT}$
P67					ASTB

(2) Non port pins (1/2)

Pin Name	I/O	Function	After Reset	Dual-Function Pin
INTP0	Input	External interrupt input with specifiable valid edge (rising edge, falling edge, or both rising edge and falling edges).	Input	P00/TI0
INTP1				P01
INTP2				P02
INTP3		Falling edge detection external interrupt input.	Input	P03
SI0	Input	Serial interface serial data input.	Input	P25/SB0
SI1				P20
SO0	Output	Serial interface serial data output.	Input	P26/SB1
SO1				P21
SB0	Input/output	Serial interface serial data input/output.	Input	P25/SI0
SB1				P26/SO0
$\overline{SCK0}$	Input/output	Serial interface serial clock input/output	Input	P27
$\overline{SCK1}$				P22
STB	Output	Serial interface automatic transmission/reception strobe output.	Input	P23
BUSY	Input	Serial interface automatic transmission/reception busy input.	Input	P24
TI0	Input	Input of external count clock to 16-bit timer (TM0).	Input	P00/INTP0
TI1		Input of external count clock to 8-bit timer (TM1).		P33
TI2		Input of external count clock to 8-bit timer (TM2).		P34
TO0	Output	16-bit timer output (dual-function with 14-bit PWM output)	Input	P30
TO1		8-bit timer output		P31
TO2				P32
PCL	Output	Clock output (for main system clock subsystem clock trimming).	Input	P35
BUZ	Output	Buzzer output.	Input	P36
AD0 to AD7	Input/output	Low address/data bus when memory is expanded externally.	Input	P40 to P47
A8 to A15	Output	High address bus when memory is expanded externally.	Input	P50 to P57
$\overline{RD}$	Output	External memory read operation strobe signal output.	Input	P64
$\overline{WR}$		External memory write operation strobe signal output.		P65
$\overline{WAIT}$	Input	Wait insertion at external memory access.	Input	P66
ASTB	Output	Output of strobe which externally latches address information to be output to port 4 when accessing external memory.	Input	P67

(2) Non port pins (2/2)

Pin Name	I/O	Function	After Reset	Dual-Function Pin
ANI0 to ANI7	Input	A/D converter analog input.	Input	P10 to P17
AV_{REF}	Input	A/D converter reference voltage input.	—	—
AV_{DD}	—	A/D converter analog power supply. Connected to V_{DD}.	—	—
AV_{SS}	—	A/D converter ground potential. Connected to V_{SS}.	—	—
$\overline{RESET}$	Input	System reset input.	—	—
X1	Input	Main system clock oscillation crystal connection.	—	—
X2	—		—	—
XT1	Input	Subsystem clock oscillation crystal connection.	Input	P04
XT2	—		—	—
V_{DD}	—	Positive power supply.	—	—
V_{PP}	—	High voltage application for program write/verify. Connected V_{SS} in normal operating mode.	—	—
V_{SS}	—	Ground potential	—	—

2.2 PROM PROGRAMMING MODE PINS

Pin Name	I/O	Function
$\overline{RESET}$	Input	PROM programming mode setting. When +5 V or +12.5 V is applied to the V_{PP} pin and a low-level signal to the $\overline{RESET}$ pin, the PROM programming mode is set.
V_{PP}	Input	PROM programming mode setting and high voltage application for program write/verify.
A0 to A16	Input	Address bus.
D0 to D7	Input/output	Data bus.
$\overline{CE}$	Input	PROM enable input/program pulse input.
$\overline{OE}$	Input	PROM read strobe input.
$\overline{PGM}$	Input	PROM programming mode program/program inhibit input.
V_{DD}	—	Positive power supply.
V_{SS}	—	Ground potential.

2.3 PIN INPUT/OUTPUT CIRCUITS AND CONNECTION OF UNUSED PINS

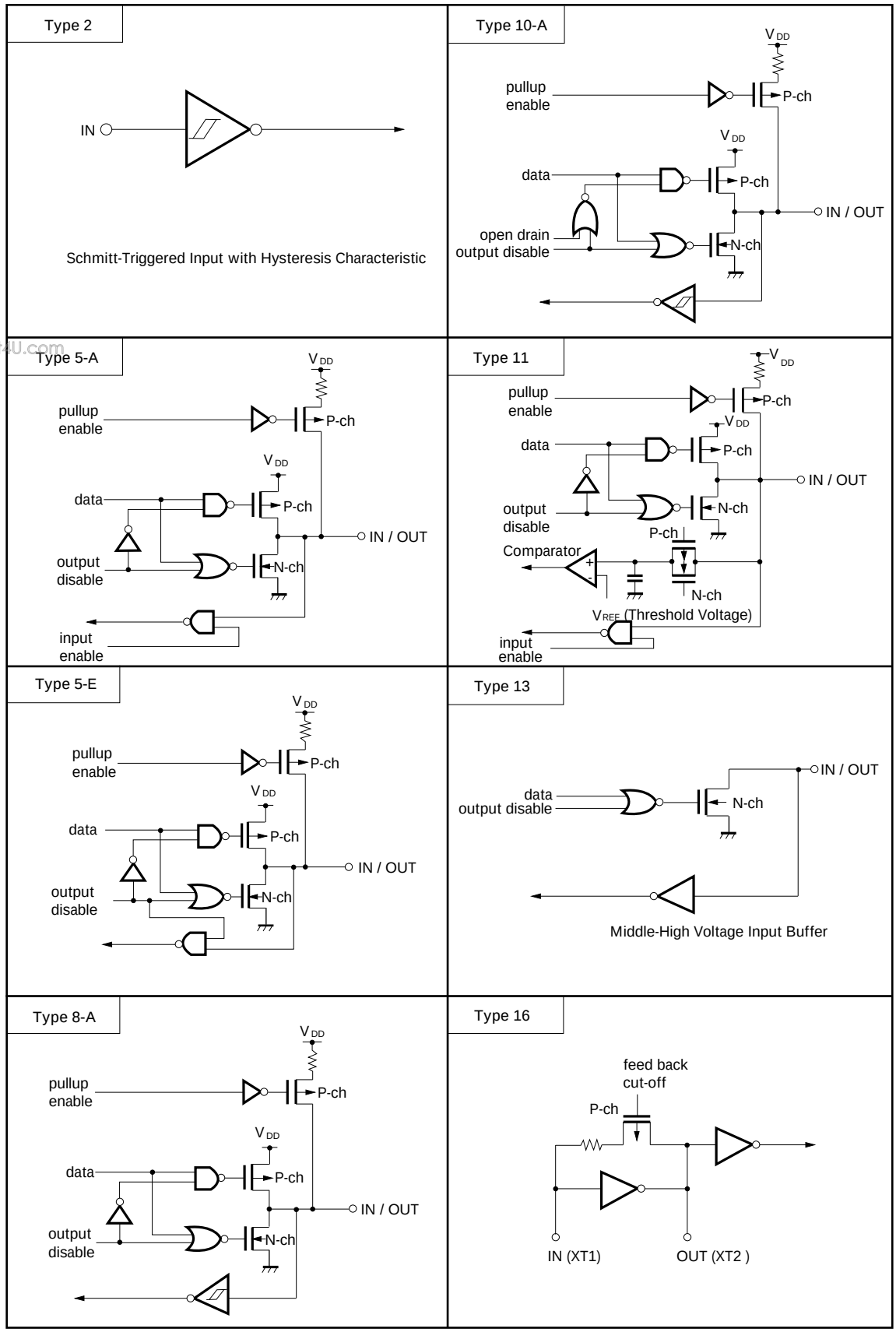
The input/output circuit type of each pin and the recommended connection of unused pins are shown in Table 2-1.

The configuration of each type of input/output circuit is shown in Fig. 2-1.

Table 2-1 Input/Output Circuit Type of Each Pin

Pin Name	Input/Output Circuit Type	I/O	Recommended Connection when not Used
P00/INTP0/TI0	2	Input	Connected to V_{SS}.
P01/INTP1	8-A	Input/output	Input : Connected to V_{SS}. Output : Leave open.
P02/INTP2			
P03/INTP3			
P04/XT1	16	Input	Connected to V_{SS}.
P10/ANI0 to P17/ANI7	11	Input/output	Input : Connected to V_{DD} or V_{SS}. Output : Leave open.
P20/SI1	8-A	Input/output	Input : Connected to V_{DD} or V_{SS}. Output : Leave open.
P21/SO1	5-A		
P22/$\overline{SCK1}$	8-A		
P23/STB	5-A		
P24/BUSY	8-A		
P25/SI0/SB0	10-A		
P26/SO0/SB1			
P27/$\overline{SCK0}$			
P30/TO0	5-A	Input/output	Input : Connected to V_{DD} or V_{SS}. Output : Leave open.
P31/TO1			
P32/TO2			
P33/TI1	8-A		
P34/TI2			
P35/PCL	5-A		
P36/BUZ			
P37			
P40/AD0 to P47/AD7	5-E	Input/output	Input : Connected to V_{SS}. Output : Leave open.
P50/A8 to P57/A15	5-A	Input/output	Input : Connected to V_{DD} or V_{SS}. Output : Leave open.
P60 to P63	13		
P64/$\overline{RD}$	5-A		
P65/$\overline{WR}$			
P66/$\overline{WAIT}$			
P67/ASTB			
$\overline{RESET}$	2	Input	—
XT2	16	—	Leave open.
AV_{REF}	—		Connected to V_{SS}.
AV_{DD}			Connected to V_{DD}.
AV_{SS}			Connected to V_{SS}.
V_{PP}			

Fig. 2-1 Pin Input/Output Circuits



3. MEMORY SIZE SWITCHING REGISTER (IMS)

This register is used to prevent part of the internal memory from being used by software. Setting the memory size switching register (IMS) enables memory mapping identical to that of a mask ROM product with different internal memory (ROM and RAM) to be used.

IMS is set by an 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input sets this register to CFH.

Fig. 3-1 Memory Size Switching Register Format

Symbol	7	6	5	4	3	2	1	0	Address	After Reset	R/W
IMS	RAM2	RAM1	RAM0	0	ROM3	ROM2	ROM1	ROM0	FFF0H	CFH	W

ROM3	ROM2	ROM1	ROM0	Internal ROM Capacity Selection
0	0	1	0	8K bytes
0	1	0	0	16K bytes
0	1	1	0	24K bytes
1	0	0	0	32K bytes
1	0	1	0	40K bytes
1	1	0	0	48K bytes
1	1	1	1	60K bytes
Other than above				Setting prohibited

RAM2	RAM1	RAM0	Internal High-Speed RAM Capacity Selection
0	0	0	768 bytes
0	0	1	640 bytes
0	1	0	512 bytes
0	1	1	384 bytes
1	0	0	256 bytes
1	0	1	Setting prohibited
1	1	0	1024 bytes
1	1	1	896 bytes

The IMS set values to make the memory map identical to various mask ROM products are shown in Table 3-1.

Table 3-1 Examples of Memory Size Switching Register Settings

Relevant Mask ROM Product	IMS Set Value
μPD78013F*	C6H
μPD78014F*	C8H
μPD78016F*	CCH

* Under development

4. INTERNAL EXPANSION RAM SWITCHING REGISTER (IXS)

This register is used to prevent part of the internal expansion RAM from being used by software. Setting the internal expansion RAM switching register enables memory mapping identical to that of a mask ROM product with different internal expansion RAM to be used.

IXS is set by an 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input sets this register to 0AH.

	7	6	5	4	3	2	1	0	Address	After Reset	R/W
IXS	0	0	0	0	IX RAM3	IX RAM2	IX RAM1	IX RAM0	FFF4H	0AH	W

IX RAM3	IX RAM2	IX RAM1	IX RAM0	Internal Expansion RAM Capacity Selection
1	0	1	0	1024 bytes (F400H to F7FFH)
1	0	1	1	512 bytes (F600H to F7FFH)
1	1	0	0	0 bytes
Other than above				Setting prohibited

5. PROM PROGRAMMING

The μPD78P018F incorporates a 60K-byte PROM as program memory. When programming the μPD78P018F, the PROM programming mode is set by means of the V_{PP} and $\overline{RESET}$ pins. For the connection of unused pins, see **"Pin Configuration, (2) PROM programming mode"**.

5.1 OPERATING MODES

When +5 V or +12.5 V is applied to the V_{PP} pin and a low-level signal is applied to the $\overline{RESET}$ pin, the μPD78P014 enters the programming mode. This is one of the operating modes shown in Table 5-1 below according to the setting of the $\overline{CE}$, $\overline{OE}$ and $\overline{PGM}$ pins.

Also, the PROM contents can be read by setting the read mode.

Table 5-1 PROM Programming Operating Modes

Operating Mode \ Pins	$\overline{RESET}$	V_{PP}	V_{DD}	$\overline{CE}$	$\overline{OE}$	$\overline{PGM}$	D0 to D7
Page data latch	L	+12.5 V	+6.5 V	H	L	H	Data input
Page write				H	H	L	High impedance
Byte write				L	H	L	Data input
Program verify				L	L	H	Data output
Program inhibit				x	H	H	High impedance
				x	L	L	
Read		+5 V	+5 V	L	L	H	Data output
Output disable				L	H	x	High impedance
Standby				H	x	x	High impedance

Remarks x : L or H.

(1) Read mode

Read mode is set by setting $\overline{CE}$ = L or $\overline{OE}$ = L.

(2) Output disable mode

Setting $\overline{OE}$ = H makes the data output high impedance, and sets the output disable mode.

Therefore, when more than one μPD78P018F is connected to the data bus, data can be read from any of the devices by controlling the $\overline{OE}$ pin.

(3) Standby mode

Standby mode is set by setting $\overline{CE}$ = H.

In this mode, the data output becomes high impedance regardless of the $\overline{OE}$ conditions.

(4) Page data latch mode

Page data latch mode is set by setting $\overline{CE}$ = H, $\overline{PGM}$ = H and $\overline{OE}$ = L at the beginning of the page write mode.

In this mode, data of 4 bytes per page is latched in the internal address/data latch circuit.

(5) Page write mode

After address and data of 4 bytes per page have been latched in the page data latch mode, page write is performed by applying a 0.1 ms program pulse (active low) to the $\overline{PGM}$ pin with $\overline{CE}$ = H, $\overline{OE}$ = H. Program verify can then be performed by setting $\overline{CE}$ = L, $\overline{OE}$ = L.

If programming cannot be performed with one program pulse, write and verify should be repeated X times (X - 10).

(6) Byte write mode

A byte write is performed by applying a 0.1 ms program pulse (active low) to the $\overline{PGM}$ pin with $\overline{CE}$ = L, $\overline{OE}$ = H. A program verify can then be performed by setting $\overline{OE}$ = L.

If programming cannot be performed with one program pulse, write and verify should be repeated X times (X - 10).

(7) Program verify mode

Program verify mode is set by setting $\overline{CE}$ = L, $\overline{PGM}$ = H and $\overline{OE}$ = L.

After a write has been executed, verification should be performed to ensure a correct write is achieved in this mode.

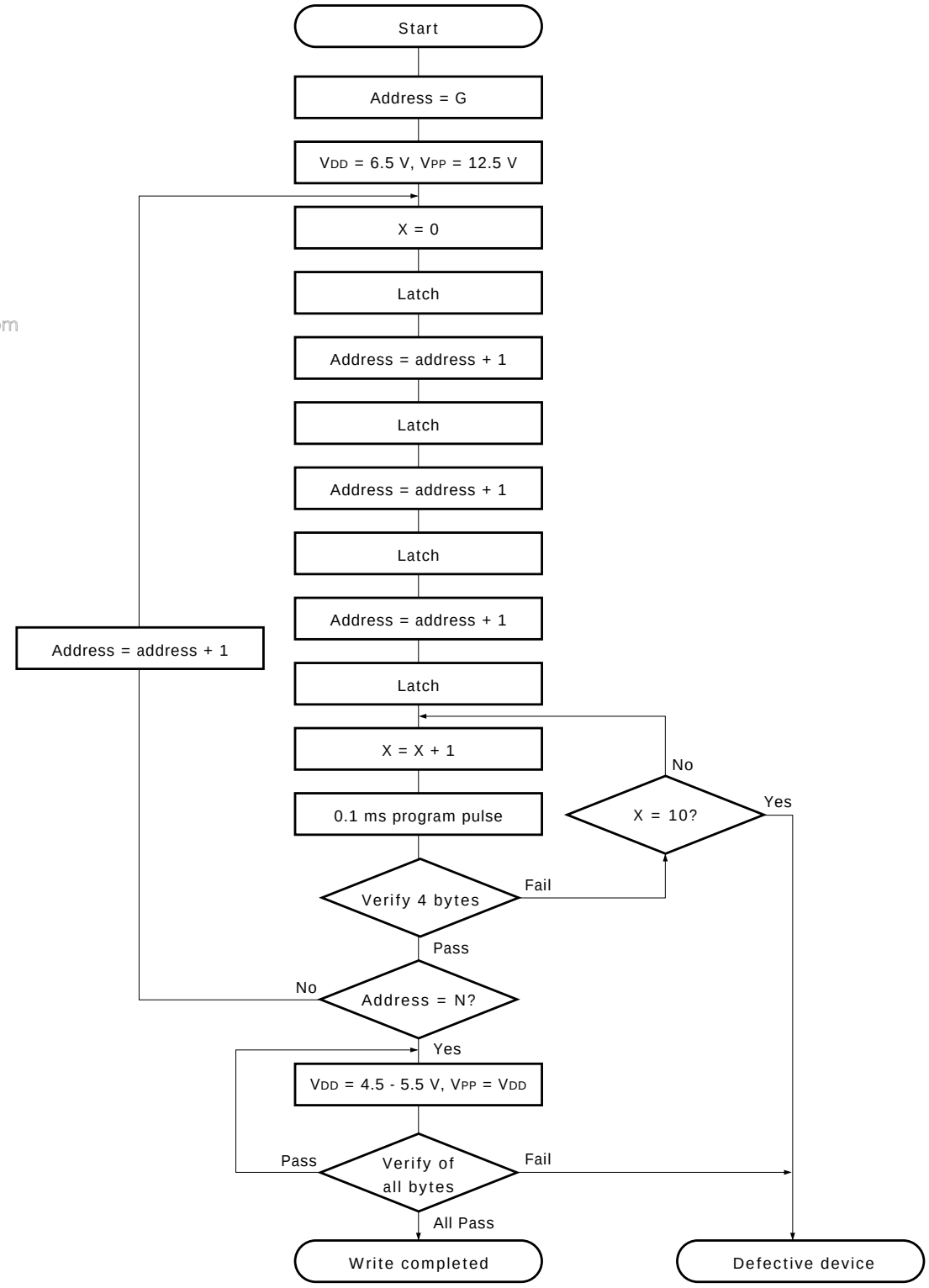
(8) Program inhibit mode

When the $\overline{OE}$ pin, V_{PP} pin and D0 to D7 pins are connected in parallel in more than one μPD78P018F, program inhibit mode is used in the case where a writing is performed to one of these devices.

The write mode or byte write mode above is used for writing. Writing is not performed to a device whose $\overline{PGM}$ pin has been driven high.

5.2 PROM WRITE PROCEDURE

Fig. 5-1 Page Program Mode Flowchart



Remarks 1. G indicates start address.
2. N indicates program final address.

Fig. 5-2 Page Program Mode Timing

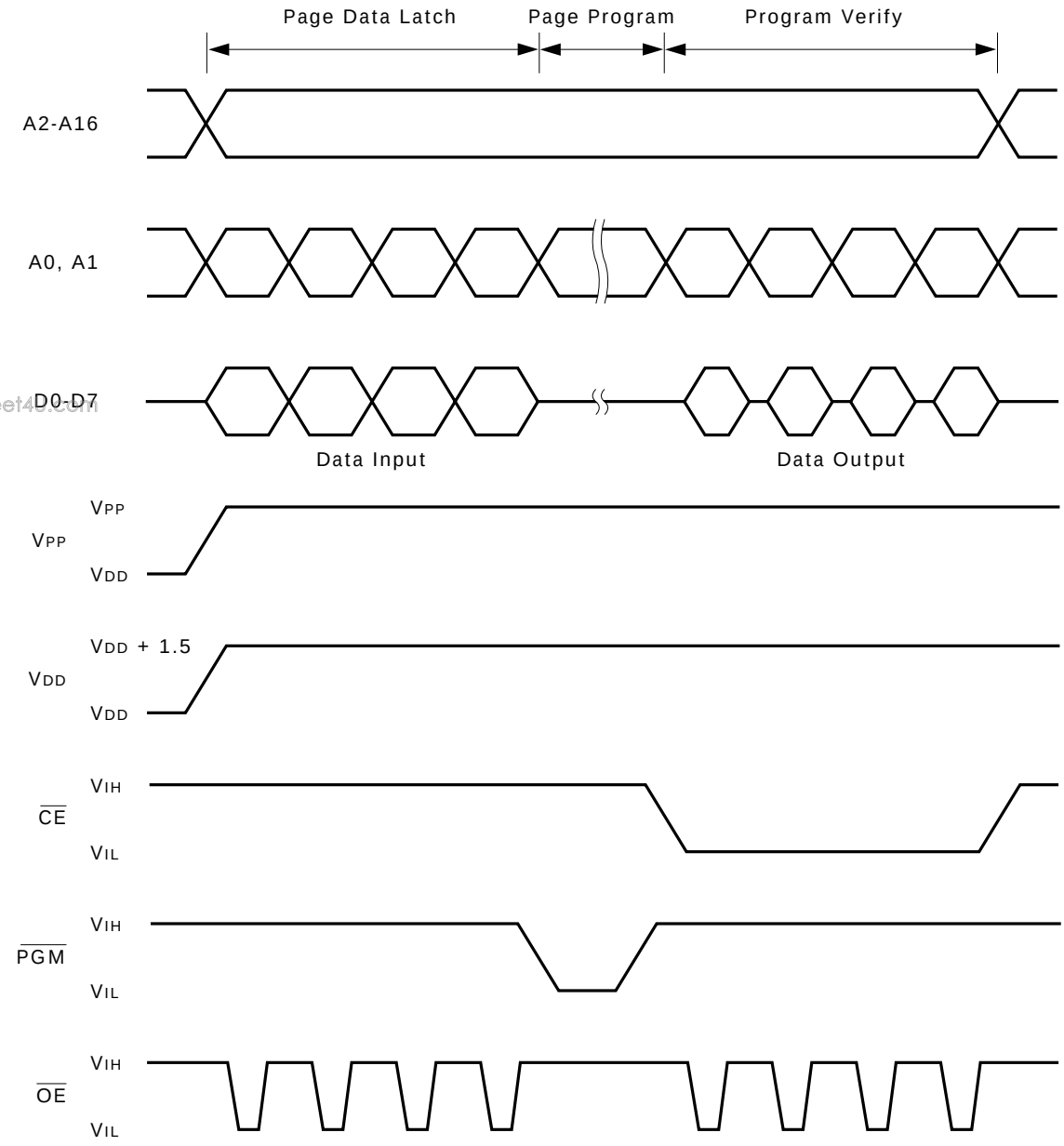
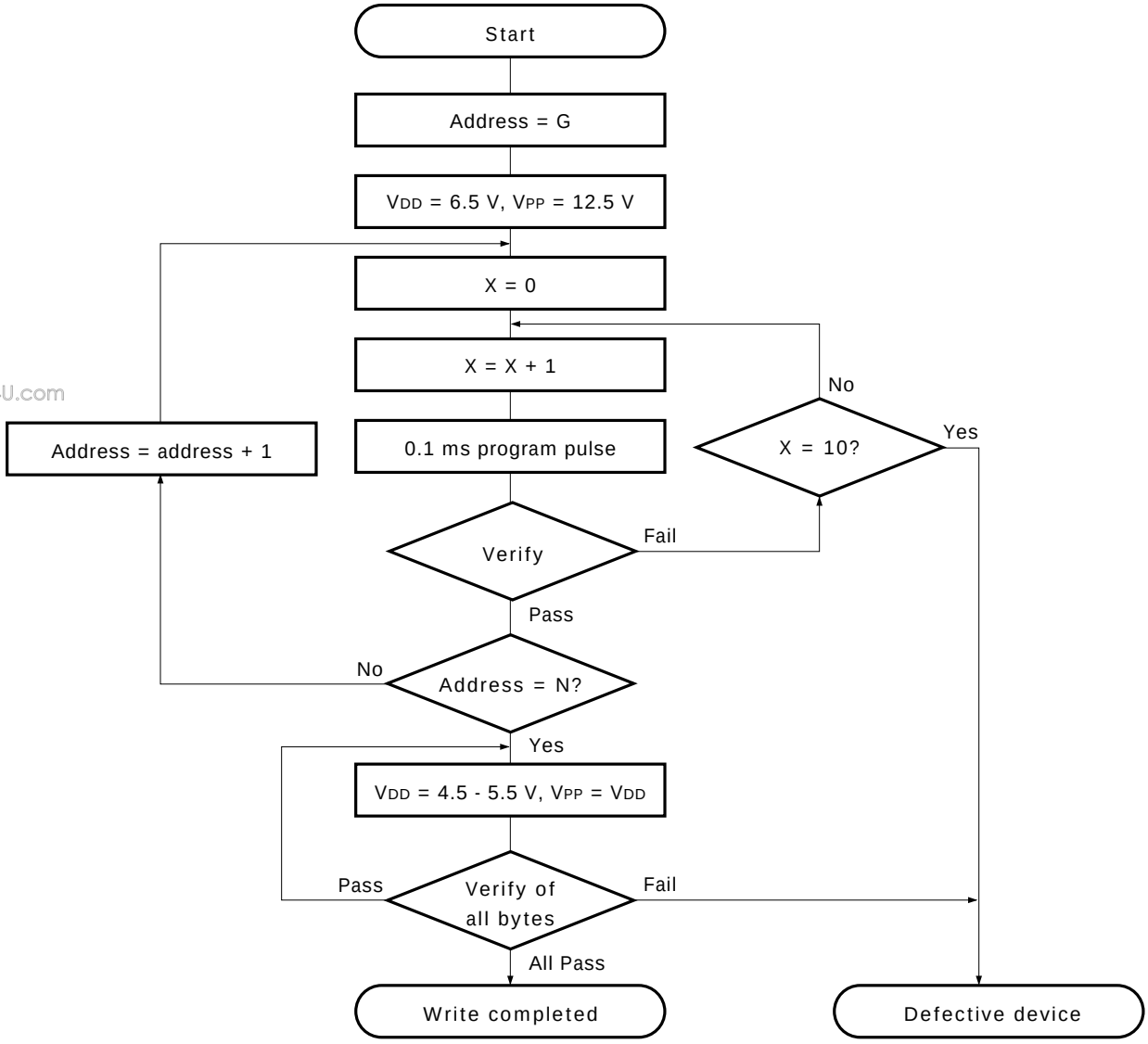


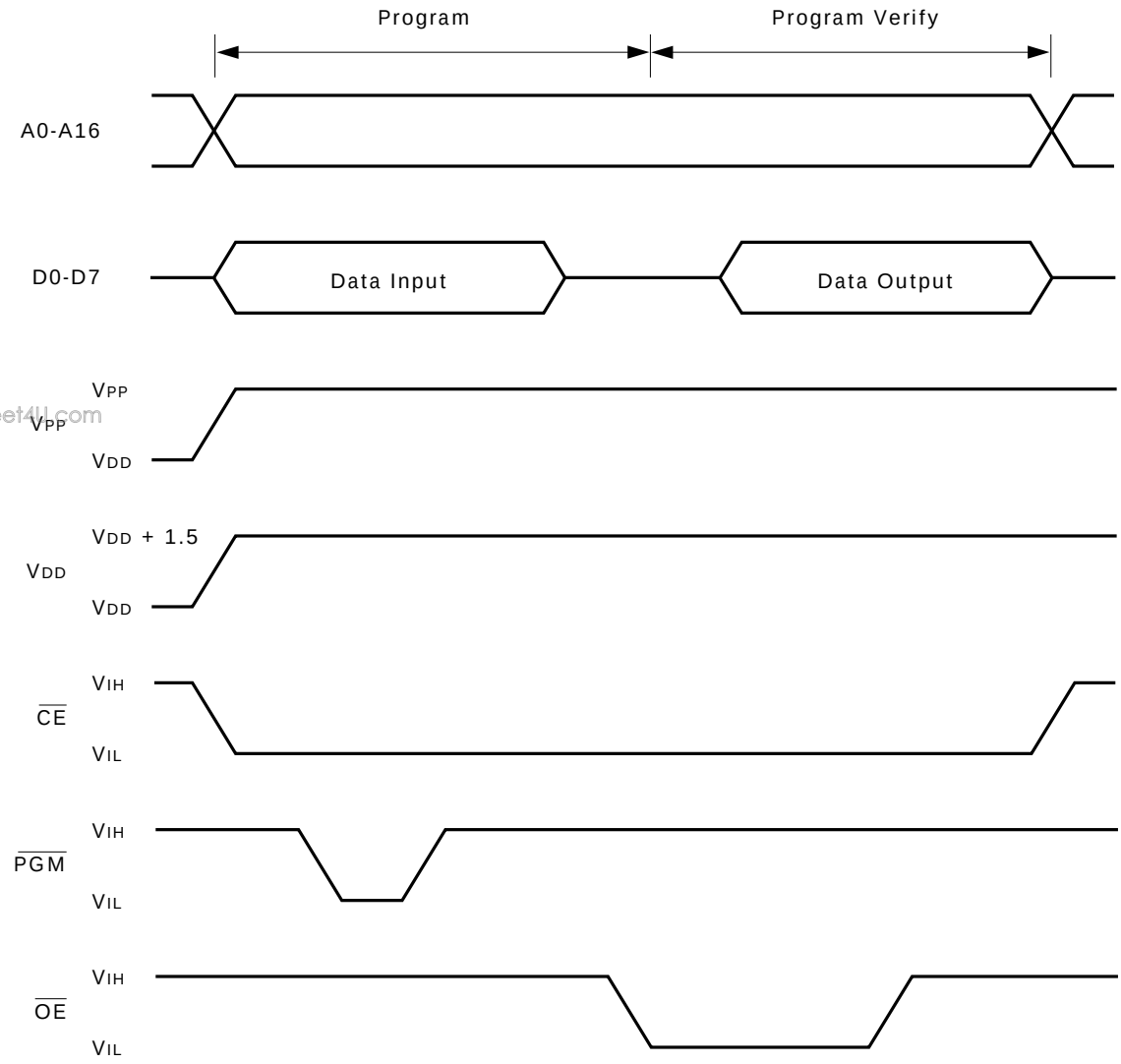
Fig 5-3 Byte Program Mode Flowchart



Remarks 1. G indicates start address.

2. N indicates program final address.

Fig 5-4 Byte Program Mode Timing



Note 1. V_{DD} should be applied before V_{PP} and disconnected after V_{PP}.

2. V_{PP} including overshoot should not exceed +13.5 V.

3. Removal and reinsertion while +12.5 V is applied to V_{PP} may have an adversary effect on reliability.

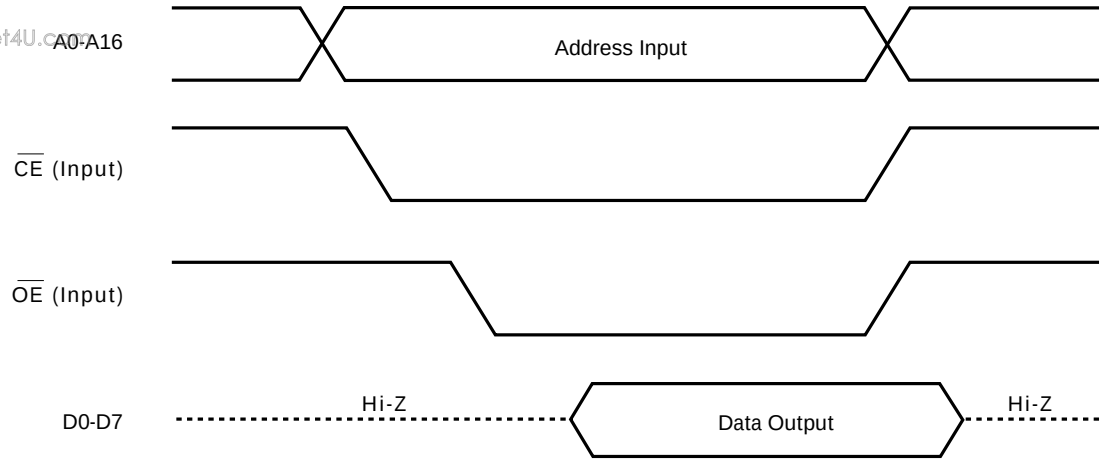
5.3 PROM READING PROCEDURE

PROM contents can be read onto the external data bus (D0 to D7) using the following procedure.

(1) Fix the $\overline{\text{RESET}}$ pin low. Supply +5 V to the V_{PP} pin. Unused pins are handled as shown in **"PIN CONFIGURATION, (2) PROM programming mode"**.
(2) Supply +5 V to the V_{DD} and V_{PP} pins.
(3) Input address of data to be read to pins A0 to A14.
(4) Read mode .
(5) Output data to pins D0 to D7.

Timing for steps (2) to (5) above is shown in Fig. 5-5.

Fig. 5-5 PROM Read Timing



6. ERASURE PROCEDURE (μPD78P018FDW/78P018FKK-S)

With the μPD78P018FDW/78P018FKK-S, it is possible to erase (set to FFH) data written to the program memory, and rewrite the memory.

The data can be erased by irradiating the window with light with a wavelength of approximately 400 nm or less. Usually, irradiation is performed with ultraviolet light with a wavelength of 254 nm. The amount of radiation required for complete erasure is shown below.

- UV intensity x erasure time: 15 W·s/cm^2 or more
- Erasure time: 15 to 20 minutes (using a 12,000 μW/cm^2 ultraviolet lamp. A longer erasure time may be required in case of deterioration of the ultraviolet lamp or dirt on the package window).

Erasure should be carried out with the ultraviolet lamp placed at a distance of 2.5 cm or less from the window. If the ultraviolet lamp is fitted with a filter, this should be removed before performing irradiation.

7. ERASURE WINDOW SEAL (μPD78P018FDW/78P018FKK-S)

A protective seal should be applied to the erasure window except when erasing the EPROM contents, in order to prevent the EPROM contents from being erroneously erased by light other than from the erasure lamp, and the internal circuits other than EPROM from misoperation due to light.

8. ONE-TIME PROM PRODUCT SCREENING

One-time PROM products (μPD78P018FCW/78P018FGC-AB8/78P018FGK-8A8) cannot be fully tested and shipped by NEC for reasons related to their structure. It is recommended that after writing the necessary data and storing at high temperature under the following conditions, screening should be conducted to verify the PROM.

Storage Temperature	Duration
125 °C	24 hours

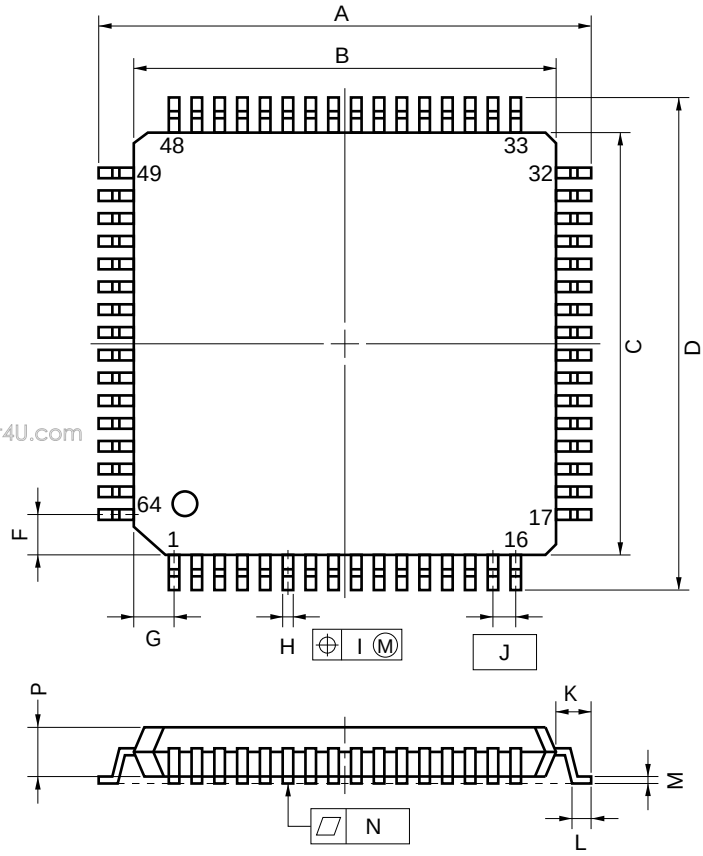
9. PACKAGE INFORMATION

64-Pin Plastic Shrink DIP (750 mil)

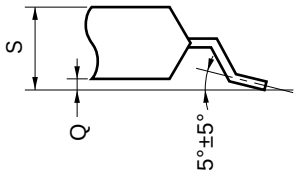
64-Pin Ceramics Shrink DIP (750 mil)

64-Pin Plastic QFP (□14)

64-Pin Plastic QFP (□12)



detail of lead end



P64GK-65-8A8

NOTE

Each lead centerline is located within 0.13 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	14.8±0.4	0.583±0.016
B	12.0±0.2	$0.472^{+0.009}_{-0.008}$
C	12.0±0.2	$0.472^{+0.009}_{-0.008}$
D	14.8±0.4	0.583±0.016
F	1.125	0.044
G	1.125	0.044
H	0.30±0.10	$0.012^{+0.004}_{-0.005}$
I	0.13	0.005
J	0.65 (T.P.)	0.026 (T.P.)
K	1.4±0.2	0.055±0.008
L	0.6±0.2	$0.024^{+0.008}_{-0.009}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.10	0.004
P	1.4	0.055
Q	0.1±0.1	0.004±0.004
S	1.7 MAX.	0.067 MAX.

64-Pin Ceramic WQFN (□14)

IN PREPARATION

APPENDIX A. DEVELOPMENT TOOLS

The following development tools are available for system development using the μPD78P018F.

Language Processing Software

RA78K/0***1,2**	78K/0 series common assembler package
CC78K/0***1,2**	78K/0 series common C compiler package
CC78K/0-L***1,2**	78K/0 series common C compiler library source file

PROM Writing Tools

PG-1500	PROM programmer
PA-78P018CW***3** PA-78P018GC***3** PA-78P018GK***3** PA-78P018KK-S***3**	Programmer adapters connected to PG-1500
PG-1500 controller***1**	PG-1500 control program

Debugging Tools

IE-78000-R	78K/0 series common in-circuit emulator
IE-78000-R-BK	78K/0 series common break board
IE-78014-R-EM-A***3**	μPD78002/78014 series common evaluation emulation board
EP-78240CW-R EP-78240GC-R EP-78012GK-R	μPD78244 series common emulation probes
EV-9200GC-64 EV-9500GK-64	Sockets to be mounted on a user system board made for 64-pin plastic QFP
SD78K/0***1**	IE-78000-R screen debugger
DF78014***1**	μPD78014 series common device file

Real-Time OS

RX78K/0***1,2**	78K/0 series common real-time OS

Fuzzy Inference Development Support System

FE9000***1**	Fuzzy knowledge data creation tool
FT9080***1**	Translator
FI78K0***1**	Fuzzy inference module
FD78K0***1,3**	Fuzzy inference debugger

***** **1.** PC-9800 series (MS-DOS™) based and IBM PC/AT™ (PC-DOS™) based
2. HP9000 series 300™ (HP-UX™) based, SPARCstation™ (Sun OS™) based, EWS-4800 series™ (EWS-UX/V™) based
3. Under development

Conversion Socket (EV-9200GC-64) External View and Recommended Board Mounting Pattern

Fig. A-1 EV-9200GC-64 External View (Reference)

Fig. A-2 EV-9200GC-64 Recommended Board Mounting Pattern (Reference)

Note The mount pad dimensions for EV-9200 may be partially different from those (for QFP) of the relevant products. Refer to " Surface Mount Technology Manual, IEI-1207" for recommended QFP mount pad dimensions.

APPENDIX B. RELATED DOCUMENTS

Device Related Documents

Document Name		Document No. (Japanese)
User's Manual		To be created
Instruction Application Table		To be created
Instruction Set		To be created
Special Function Register Application Table		To be created
Application Note	Introductory Volume I	IEA-715
	Introductory Volume II	IEA-740
	Floating-Point Operation Program Volume	IEA-718

Development Tool Documents (User's Manuals)

Document Name		Document No. (Japanese)
RA78K Series Assembler Package	Operation Volume	EEU-809
	Language Volume	EEU-815
RA78K Series Structured Assembler Preprocessor		EEU-817
CC78K Series C Compiler	Operation Volume	EEU-656
	Language Volume	EEU-655
CC78K Series Library Source File		EEU-777
PG-1500 PROM Programmer		EEU-651
PG-1500 Controller		EEU-704
IE-78000-R		EEU-810
IE-78000-R-BK		EEU-867
IE-78014-R-EM-A		To be created
SD78K/0 Screen Debugger	Primer	EEU-852
	Reference	EEU-816

Note For design purposes, etc., be sure to use the latest documents.

Built-In Software Documents (User's Manuals)

Document Name		Document No. (Japanese)
78K/0 Series Real-Time OS	Introductory Volume	EEU-912
	Installation Volume	EEU-911
	Debugger Volume	EEU-930
	Technical Volume	EEU-913
Fuzzy Knowledge Data Creation Tools		EEU-829
78/0, 78K/II, 87AD Series Fuzzy Inference Development Support System Translator		EEU-862
78K/0 Series Fuzzy Inference Development Support System Fuzzy Inference Module		EEU-858
78K/0 Series Fuzzy Inference Development Support System Fuzzy Inference Debugger		EEU-921

Other Documents

Document Name	Document No. (Japanese)
Package Manual	IEI-635
Surface Mount Technology Manual	IEI-616
Quality Grades on Semiconductor Devices	IEI-620
NEC Semiconductor Device Reliability & Quality Control	IEM-5068
Electrostatic Discharge (ESD) Test	MEM-539
Semiconductor Devices Quality Control Guarantee Guide	MEI-603
Microcomputer Related Products Guide Other Manufacturers Volume	MEI-604

Note For design purposes, etc., be sure to use the latest documents.

[MEMO]