ADVANCE INFORMATION

CDC1607F-E
Automotive Controller
Specification

Edition March 31, 2003
6251-608-2AI

MICRONAS

Contents

1. Introduction

Release Note: Revision bars indicate significant changes to the previous edition.

The IC is a single-chip controller for use in automotive applications. The CPU on the chip is an upgrade of the 65C02 with 16-bit internal data and 24-bit address bus. The chip consists of timer/counters, an interrupt controller, a multichannel A/D converter, a stepper motor and LCD driver, CAN interfaces and PWM outputs. This document provides MCM Flash hardware-specific information. General information on operating the IC can be found in the document “CDC16xxF-E Automotive Controller Family User Manual” (6251-606-2AI).

1.1. Features

Table 1–1: CDC16xxF Family Feature List

Item	CDC1605F-E EMU	This Document: CDC1607F-E MCM Flash	CDC1631F-E MASK ROM	CDC1605F-C EMU	CDC1607F-C MCM Flash	CDC1641F-C Mask ROM	CDC1652F-C Mask ROM	CDC1672F-C Mask ROM
Core								
CPU	16-bit 65C816, featuring software compatibility with its 8-bit NMOS and CMOS 6500-series predecessors							
CPU-Active Operation Modes	FAST, SLOW and DEEP SLOW			FAST and SLOW				
Power Saving Modes (CPU Inactive)	WAKE and IDLE			-				
EMI Reduction Mode	selectable in FAST mode							
Oscillators	4 MHz to 12 MHz Quartz, RC			4 MHz to 12 MHz Quartz				
RAM	6 KB		2 KB	6 KB		2.75 KB	4 KB	6 KB
ROM	ROMless, external program storage with up to 16 MB, internal 2 KB Boot ROM	256 KB Flash, bottom boot configuration, internal 2 KB Boot ROM	64 KB	ROMless, external program storage with up to 16 MB, internal 2 KB Boot ROM	256 KB Flash, bottom boot configuration, internal 2 KB Boot ROM	90 KB	128 KB	216 KB

Table 1–1: CDC16xxF Family Feature List, continued

Item	CDC1605F-E EMU	This Document: CDC1607F-E MCM Flash	CDC1631F-E MASK ROM	CDC1605F-C EMU	CDC1607F-C MCM Flash	CDC1641F-C Mask ROM	CDC1652F-C Mask ROM	CDC1672F-C Mask ROM
Multiplier, 8 by 8 bit	✔			-				
Digital Watchdog	✔							
Central Clock Divider	✔							
Interrupt Controller expanding NMI	16 inputs,16 priority levels							
Port Interrupts including Slope Selection	4 inputs							
Port Wake-Up Inputs including Slope / Level Selection	✔			-				
Patch Module	10 ROM locations		5 ROM locations	10 ROM locations		5 ROM locations	6 ROM locations	
Boot System	allows in-system downloading of code and data into RAM via serial link		-	allows in-system downloading of code and data into RAM via serial link		-	-	-
Analog								
Reset/Alarm	Combined Input for Regulator Input Supervision							
Clock and Supply Supervision	✔							
10-bit ADC, charge balance type	9 channels (5 channels selectable as digital input)							
ADC Reference	VREF Pin							
Comparators	P06COMP with 1/2 AVDD reference							
LCD	Internal processing of all analog voltages for the LCD driver							

Table 1–1: CDC16xxF Family Feature List, continued

Item	CDC1605F-E EMU	This Document: CDC1607F-E MCM Flash	CDC1631F-E MASK ROM	CDC1605F-C EMU	CDC1607F-C MCM Flash	CDC1641F-C Mask ROM	CDC1652F-C Mask ROM	CDC1672F-C Mask ROM
Communication								
DMA	1 DMA Channel for serving the Graphics Bus interface		-	1 DMA Channel for serving the Graphics Bus interface		-	1 DMA Channel for serving the Graphics Bus interface	
UART	3: UART0, UART1 and UART2		1: UART0	3: UART0, UART1 and UART2		1: UART0	3: UART0, UART1 and UART2	
Synchronous Serial Peripheral Interfaces	2: SPI0 and SPI1		1: SPI0	2: SPI0 and SPI1		1: SPI0	2: SPI0 and SPI1	
Full CAN modules V2.0B	3: CAN0, CAN1 and CAN2 with 256-byte object RAM each (LCAN000F)		1: CAN0 with 256-byte object RAM (LCAN000F)	3: CAN0, CAN1 and CAN2 with 256-byte object RAM each (LCAN0009)		1: CAN0 with 256-byte object RAM (LCAN0009)	2: CAN0 and CAN1 with 256-byte object RAM each (LCAN0009)	
DIGITbus	1 master module		-	1 master module		-	1 master module	
Input & Output								
Universal Ports selectable as 4:1 mux LCD Segment/Backplane lines or Digital I/O Ports	up to 52 I/O or 48 LCD segment lines (=192 segments), in groups of two, configurable as I/O or LCD							
Universal Port Slew Rate	HW preselectable							
Stepper Motor Control Modules with High-Current Ports	5 Modules, 24 dI/dt controlled ports							
8-bit PWM Modules	5 Modules: PWM0, PWM1, PWM2, PWM3 and PWM4		3 Modules: PWM0, PWM1, PWM2	5 Modules: PWM0, PWM1, PWM2, PWM3 and PWM4		2 Modules: PWM0, PWM1	5 Modules: PWM0, PWM1, PWM2, PWM3 and PWM4	
Audio Module with auto-decay	✔							
SW selectable Clock outputs	2							

Table 1–1: CDC16xxF Family Feature List, continued

Item	CDC1605F-E EMU	This Document: CDC1607F-E MCM Flash	CDC1631F-E MASK ROM	CDC1605F-C EMU	CDC1607F-C MCM Flash	CDC1641F-C Mask ROM	CDC1652F-C Mask ROM	CDC1672F-C Mask ROM
Polling / Flash Timer Output	1 High-Current Port output operable in Power Saving Mode			-				
Timers & Counters								
16-bit free running counters with Capture/ Compare modules	CCC0 with 3CAPCOM							
16-bit timers	1: T0							
8-bit timers	2: T1 and T2							
Real Time Clock, Delivering Hours, Minutes and Seconds	✔			-				
Miscellaneous								
Scalable layout in CAN, RAM and ROM	-	✔		-	✔			
Various randomly selectable HW options	Most options SW programmable, copy from user program storage during system start-up		Mask programmed according to user specification	Most options SW programmable, copy from user program storage during system start-up				
Core Bond-Out	✔	-		✔	-			
Supply Voltage	4.5 V to 5.5 V							
Temperature Range	T_{case}: –40 to +105C			T_{amb}: –40 to +85C				
Package								
Type	Ceramic 177PGA	Plastic 100QFP 0.65mm pitch		Ceramic 177PGA	Plastic 100QFP 0.65mm pitch			
Bonded Pins	176	100		176	100			

1.2. Abbreviations

AM	Audio Module
CAN	Controller Area Network Module
CAPCOM	Capture/Compare Module
CPU	Central Processing Unit
DMA	Direct Memory Access Module
ERM	EMI Reduction Module
IR	Interrupt Controller
LCD	Liquid Crystal Display Module
P06COMP	P0.6 Alarm Comparator
PINT	Port Interrupt Module
PSM	Power Saving Module
PWM	8-Bit Pulse Width Modulator Module
RTC	Real-time Clock
SM	Stepper Motor Control Module
SPI	Serial Synchronous Peripheral Interface
T0	16-Bit Timer 0
T1, T2	8-Bit Timers 1 and 2
UART	Universal Asynchronous Receiver Transmitter

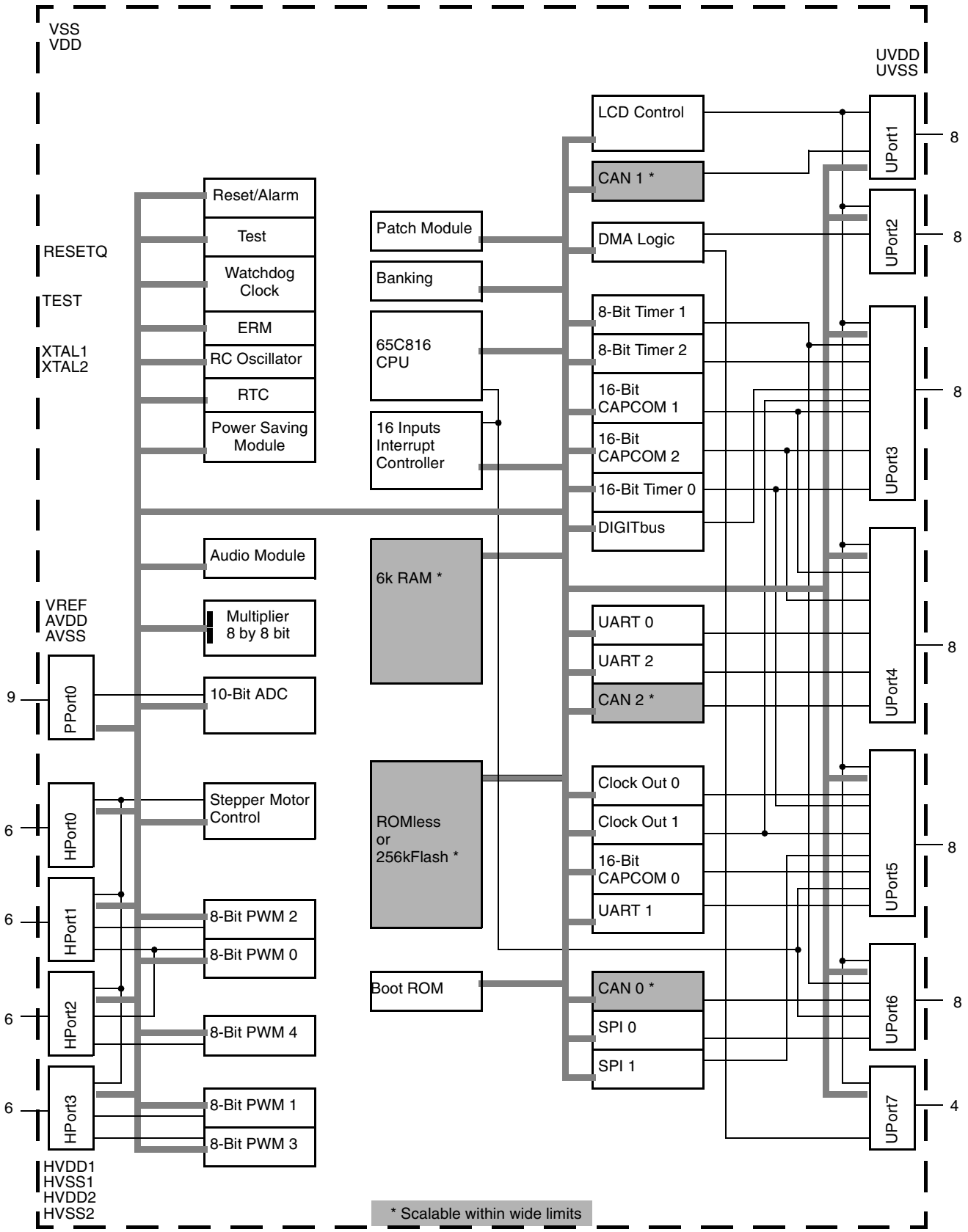


Fig. 1–1: Block diagram of CDC1605F-E/CDC1607F-E

2. Package and Pins

2.1. Package Outline Dimensions

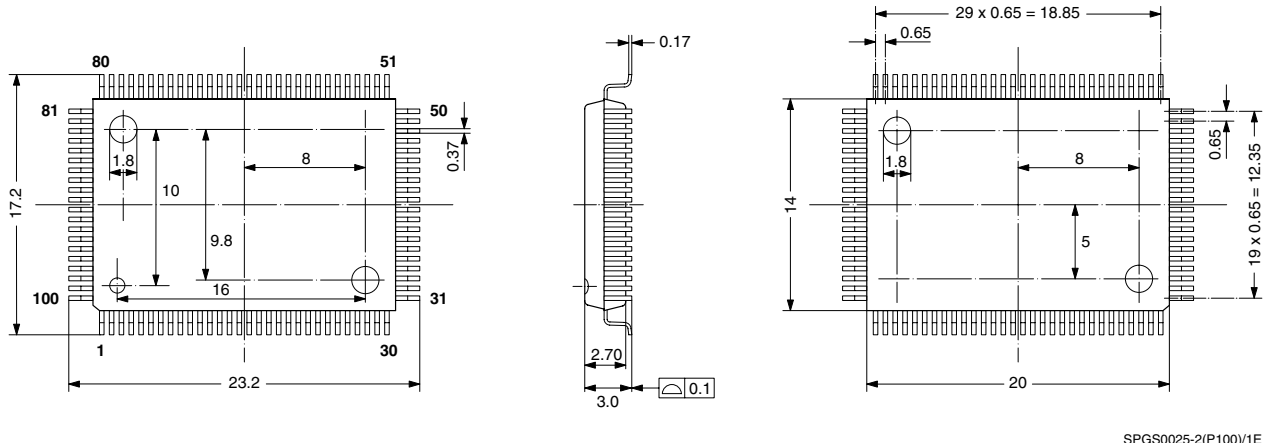
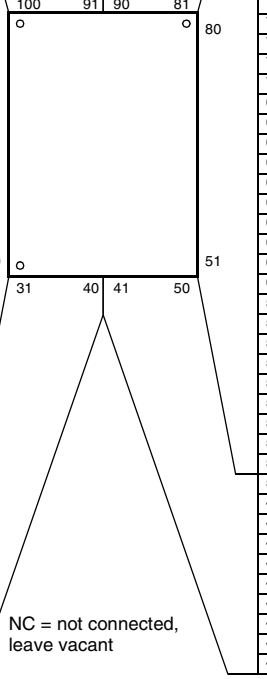


Fig. 2–1: PQFP100 Plastic Quad Flat Pack 100-Pin (Weight approx. 1.61 g)

2.2. Pin Assignment

Pin Functions						Pin No.
Bus Mode	LCD Mode	Port Special Out	Port Special In	Basic Function		
	SEG7.3	GWRQ		U7.3		91
	SEG7.2	GRDQ		U7.2		92
	SEG7.1			U7.1		93
	SEG7.0			U7.0		94
				UVSS		95
				UVDD		96
ADB7	SEG3.7	T2-OUT		U3.7		97
ADB6	SEG3.6	CC1-OUT		U3.6		98
ADB5	SEG3.5	SPI1-CLK-OUT	SPI1-CLK-IN	U3.5		99
ADB4	SEG3.4	T0-OUT	WP0	U3.4		100
ADB3	SEG3.3	CC2-OUT		U3.3		1
ADB2	SEG3.2	DIGIT-OUT	DIGIT-IN	U3.2		2
ADB1	SEG3.1	CO1	SPI1-D-IN	U3.1		3
ADB0	SEG3.0	SPI1-D-OUT		U3.0		4
	SEG6.7	CAN0-TX	MULTI-TEST-IN	U6.7		5
	SEG6.6	PINT1-OUT	CAN0-RX/WP1	U6.6		6
	SEG6.5	T1-OUT	SPI0-D-IN	U6.5		7
	SEG6.4	SPI0-D-OUT		U6.4		8
				TEST		9
				RESETQ		10
				XTAL2		11
				XTAL1		12
				VSS		13
				VDD		14
	SEG6.3	SPI0-CLK-OUT	SPI0-CLK-IN	U6.3		15
	SEG6.2	T1-OUT	PINT2-IN/WP5	U6.2		16
	SEG6.1	LCD-CLK-OUT	PINT1-IN/WP4	U6.1		17
	SEG6.0	LCD-SYNC-OUT	PINT0-IN/WP3	U6.0		18
WEQ	SEG1.7	CAN1-TX		U1.7		19
CEQ	SEG1.6		CAN1-RX/WP2	U1.6		20
ITSTOUT	SEG1.5	LCD-CLK-OUT		U1.5		21
RWQ	SEG1.4	LCD-SYNC-OUT		U1.4		22
PH2	BP3			U1.3		23
OEQ	BP2			U1.2		24
BE	BP1			U1.1		25
RDY	BP0	ITSTOUT		U1.0		26
STOPCLK		SMB1+		H1.5		27
VPQ		SMB1-		H1.4		28
VPA		SMB2+		H1.3		29
VDA		SMB2-	SMB-COMP	H1.2		30
DB7		SME1+/PWM2		H1.1		31
DB6		SME1-/PWM0		H1.0		32
				HVDD1		33
				HVSS1		34
DB5		SME2+		H0.5		35
DB4		SME2-	SME-COMP	H0.4		36
DB3		SMA1+		H0.3		37
DB2		SMA1-		H0.2		38
DB1		SMA2+		H0.1		39
DB0		SMA2-	SMA-COMP	H0.0		40



Pin No.	Pin Functions					
	Basic Function	Port Special In	Port Special Out	LCD Mode	Bus Mode	
90	U4.0	CAN2-RX/WP7		SEG4.0	ADB8	
89	U4.1		CAN2-TX	SEG4.1	ADB9	
88	U4.2	UART2-RX		SEG4.2	ADB10	
87	U4.3		UART2-TX	SEG4.3	ADB11	
86	U4.4	UART0-RX/WP8		SEG4.4	ADB12	
85	U4.5		UART0-TX	SEG4.5	ADB13	
84	U4.6	CC2-IN	CC1-OUT	SEG4.6	ADB14	
83	U4.7	CC1-IN		SEG4.7	ADB15	
82	U5.0	CC0-IN	CO1	SEG5.0		
81	U5.1	INT-TEST-IN	CC0-OUT	SEG5.1		
80	U5.2	LCD-CLK-IN	AM-PWM	SEG5.2		
79	U5.3	LCD-SYNC-IN	AM-OUT	SEG5.3		
78	U5.4	IRQ	UART1-TX	SEG5.4		
77	U5.5	ABORTQ	CO0	SEG5.5		
76	U5.6	PINT3/WP6	PWM2	SEG5.6		
75	U5.7	PINT3/UART1-RX	PINT0-OUT	SEG5.7		
74	U2.0/GD0			SEG2.0	ADB16	
73	U2.1/GD1			SEG2.1	ADB17	
72	U2.2/GD2			SEG2.2	ADB18	
71	U2.3/GD3			SEG2.3	ADB19	
70	U2.4/GD4			SEG2.4	ADB20	
69	U2.5/GD5			SEG2.5	ADB21	
68	U2.6/GD6			SEG2.6	ADB22	
67	U2.7/GD7			SEG2.7	ADB23	
66	AVSS					
65	AVDD					
64	VREF					
63	P0.1	P0.1 digital input				
62	P0.2	P0.2 digital input				
61	P0.3	P0.3 digital input				
60	P0.4	P0.4 digital input				
59	P0.5	P0.5 digital input				
58	P0.6	P0.6 Compar. inp.				
57	P0.7					
56	P0.8					
55	P0.9					
54	H2.0	SMC-COMP	SMC2-			
53	H2.1		SMC2+			
52	H2.2		SMC1-			
51	H2.3		SMC1+			
50	H2.4	WP9	PWM0			
49	H2.5/Pol		PWM4			
48	HVSS2					
47	HVDD2					
46	H3.0		PWM1			
45	H3.1		PWM3			
44	H3.2	SMD-COMP	SMD2-			
43	H3.3		SMD2+			
42	H3.4		SMD1-			
41	H3.5		SMD1+			

Fig. 2–2: Pin Assignment for **PQFP100** Package

2.3. External Components

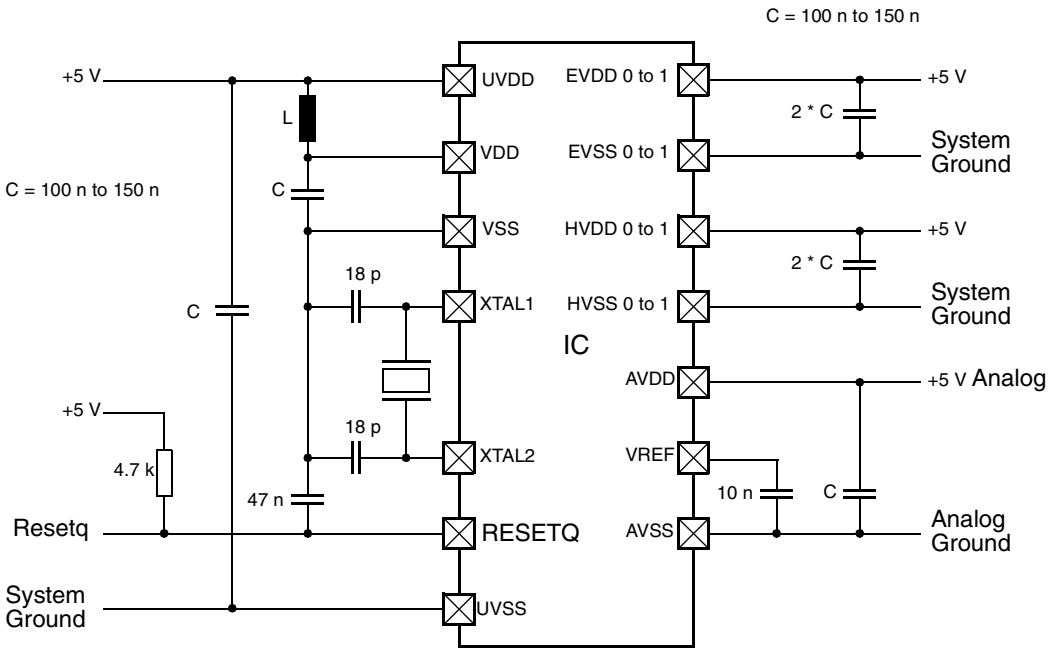


Fig. 2–3: Recommended external supply and quartz connection for low electromagnetic interference (EMI)

To provide effective decoupling and to improve EMC behavior, the small decoupling capacitors must be located as close to the supply pins as possible. The self-inductance of these capacitors and the parasitic inductance and capacitance of the interconnecting traces determine the self-resonant frequency of the decoupling network. A frequency too low will reduce decoupling effectiveness, increase RF emissions and may affect device operation adversely.

XTAL1 and XTAL2 quartz connections are especially sensitive to capacitive coupling from other PC board signals. It is strongly recommended to place quartz and oscillation capacitors as close to the pins as possible and to shield the XTAL1 and XTAL2 traces from other signals by embedding them in a VSS trace.

The RESETQ pin adjacent to XTAL2 should be supplied with a 47 nF capacitor, to prevent fast RESETQ transients from being coupled into XTAL2, to prevent XTAL2 from coupling into RESETQ, and to guarantee a time constant of ≥ 200 µs, sufficient for proper Wake Reset functionality.

3. Electrical Characteristics

3.0.1. Absolute Maximum Ratings

Table 3–1: $UV_{SS} = HV_{SS1} = HV_{SS2} = AV_{SS} = 0$ V

Symbol	Parameter	Pin Name	Min.	Max.	Unit
V_{SUP}	Core Supply Voltage Port Supply Voltage Analog Supply Voltage SM Supply Voltage 1 SM Supply Voltage 2	VDD UVDD AVDD HVDD1 HVDD2	–0.3	6.0	V
ΔV_{DD}	Voltage Difference between VDD and AVDD, resp. UVDD	VDD, AVDD UVDD	–0.5	0.5	V
I_{SUP}	Core Supply Current Port Supply Current	VDD, VSS UVDD, UVSS	–100	100	mA
IA_{SUP}	Analog Supply Current	AVDD, AVSS	–20	20	mA
IH_{SUP}	SM Supply Current @T_j=105C, Duty Factor = 0.71 [1)]	HVDD1, HVSS1 HVDD2, HVSS2	–380	380	mA
V_{in}	Input Voltage	U-Ports, XTAL,RESETQ, TEST	UV_{SS}–0.5	UV_{DD}+0.7	V
		P0-Ports VREF	UV_{SS}–0.5	AV_{DD}+0.7	V
		H-Ports	HV_{SS}–0.5	HV_{DD}+0.7	V
I_{in}	Input Current	all Inputs	0	2	mA
I_o	Output Current	U-Ports	–5	5	mA
		H-Ports	–60	60	mA
t_{oshsl}	Duration of Short Circuit in Port SLOW Mode to UVSS or UVDD	U-Ports except U3.2 in DP Mode		indefinite	s
T_j	Junction Temperature under Bias		–45	115	°C
T_s	Storage Temperature		–45	125	°C
P_{max}	Maximum Power Dissipation			0.8	W

[1)] This condition represents the worst case load with regard to the intended application

Stresses beyond those listed in the “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these or any other conditions beyond those indicated in the “Recommended Operating Conditions/Characteristics” of this specification is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

3.0.2. Recommended Operating Conditions

Table 3–2: UVSS = HVSS1= HVSS2 = AVSS = 0 V

Symbol	Parameter	Pin Name	Min.	Typ [1)]	Max.	Unit
V_{DD}	Supply Voltage Port Supply Voltage Analog Supply Voltage	VDD UVDD AVDD	4.5	5	5.5	V
HV_{DD}	SM Supply Voltage 1 SM Supply Voltage 2	HVDD1 HVDD2	4.75	5	5.25	V
ΔV_{DD}	Voltage Difference between VDD and AVDD resp. UVDD	VDD, AVDD UVDD	–0.2		0.2	V
dAV_{DD}	AVDD Ripple, Peak to Peak	AVDD			200	mV
f_{XTAL}	XTAL Clock Frequency	XTAL1	4		12	MHz
	XTAL Clock Frequency using ERM	XTAL1	4		10	MHz
T_j	Junction Temperature		–40		110	C
V_{il}	Low Input Voltage	U-Ports H-Ports P0-Ports TEST			$0.51*V_{DD}$	V
V_{ih}	High Input Voltage	U-Ports H-Ports P0-Ports TEST	$0.86*V_{DD}$			V
RV_{il}	Reset Active Input Voltage	RESETQ			0.9	V
WRV_{il}	Reset Active Input Voltage during Power Saving Modes and Wake Reset	RESETQ			0.6	V
RV_{im}	Reset Inactive and Alarm Active Input Voltage	RESETQ	1.6		2.1	V
RV_{ih}	Reset Inactive and Alarm Inactive Input Voltage	RESETQ	2.9			V
WRV_{ih}	Reset Inactive during Power Saving Modes	RESETQ	UV_{DD} - 0.4V			V
V_{REFi}	ADC Reference Input Voltage	VREF	2.56		AV_{DD}	V
$P0V_i$	P0 ADC Input Port Input Voltage	P0-Ports	0		V_{REFi}	V
Clock Input from External Generator						
XV_{il}	Clock Input Low Voltage	XTAL1			$0.2*V_{DD}$	V
XV_{ih}	Clock Input High Voltage	XTAL1	$0.8*V_{DD}$			V
D_{XTAL}	Clock Input High-to-Low Ratio	XTAL1	0.45		0.55	

[1)] Typical values describe typical behavior at room temperature (25 °C, unless otherwise noted), with typical Recommended Operating Conditions applied (derived from device characterization, not 100% tested).

3.0.3. Characteristics differing from Characteristics described in document "CDC16xxF-E Automotive Controller Family User Manual"

Table 3–3: $UV_{SS} = HV_{SS1} = HV_{SS2} = AV_{SS} = 0$ V, 4.5 V < $V_{DD} = AV_{DD} = UV_{DD}$ < 5.5 V, 4.75 V < $HV_{DD1} = HV_{DD2}$ < 5.25 V, T_{CASE} = –40 °C to +105 °C, f_{XTAL} = 10 MHz

Symbol	Parameter	Pin Name	Min.	Typ [1]	Max.	Unit	Test Conditions
Package							
R_{thjc}	Thermal Resistance from Junction to Case			25		C/W	
R_{thja}	Thermal Resistance from Junction to Ambient			60		C/W	
Supply Currents							CMOS levels on all Inputs, no Loads on Outputs, difference between any two VDDs within ±0.2 V
I_{DDF}	VDD FAST Mode Supply Current	VDD			60	mA	Flash Read [6]
					80		Flash Write/Erase [6]
I_{DDS}	VDD SLOW Mode Supply Current	VDD			1.8	mA	all Modules OFF [2], [6]
I_{DDD}	VDD DEEP SLOW Mode Supply Current	VDD			1.5		all Modules OFF [2], [6]
I_{DDI}	VDD IDLE Mode Supply Current	VDD		50	75	µA	f_{xtal} = 4 MHz [6]
				60	90	µA	f_{xtal} = 10 MHz [6]
				70	100	µA	internal RC oscill.
I_{DDW}	VDD WAKE Mode Supply Current	VDD		30	50	µA	
UI_{DDa}	UVDD Active Supply Current	UVDD			0.3	mA	no Output Activity, LCD Module ON
AI_{DDa}	AVDD Active Supply Current	AVDD		0.2	0.4	mA	ADC ON, ERM OFF
				1	2	mA	ERM ON, f_{XTAL}=8.4MHz
AI_{DDq}	Quiescent Supply Current	AVDD		1	10	µA	ADC and ERM OFF
UI_{DDq}		UVDD		1	10	µA	no Output Activity, LCD Module OFF
EI_{DDq}		EVDD1 EVDD2		1	10	µA	no Output Activity, LCD Module OFF
HI_{DDq}		Sum of all HVDD1 HVDD2		1	20	µA	no Output Activity, SM Module OFF

[1] Typical values describe typical behavior at room temperature (25 °C, unless otherwise noted), with typical Recommended Operating Conditions applied (derived from device characterization, not 100% tested).

[2] Value may be exceeded with unusual Hardware Option setting
[3] Design value only, the actually observable hysteresis may be lower due to system activity and related supply noise
[4] When the ERM is active, this time value is increased by 0.121/fXTAL, e.g. 15.125 ns at 8 MHz.
[5] When the ERM is active, this time value is decreased by 0.121/fXTAL, e.g. 15.125 ns at 8 MHz.
[6] Measured with external clock. Add 170 µA at 4 MHz, 200 µA at 10 MHz for operation on typical quartz with SR3.XTAL = 0 (Oscillator RUN mode).

3.0.4. Recommended Crystal Characteristics

Table 3–4: $UV_{SS} = HV_{SS1} = HV_{SS2} = AV_{SS} = 0$ V, 4.5 V < $V_{DD} = AV_{DD} = UV_{DD}$ < 5.5 V, 4.75 V < $HV_{DD1} = HV_{DD2}$ < 5.25 V, T_{CASE} = –40 °C to +105 °C

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
f_P	Parallel Resonance Frequency @ C_L = 12 pF	4		12	MHz	
R_1	Series Resonance Res. for 50 ms Oscillation Start-Up time @C_L= 12 pF @ f_P = 4 MHz			380 320	Ohm	START-UP RUN
	@ f_P = 6 MHz			230 160	Ohm	START-UP RUN
	@ f_P = 8 MHz			150 95	Ohm	START-UP RUN
	@ f_P = 10 MHz			100 60	Ohm	START-UP RUN
C_{EXT}	External Oscillation Capacitances for C_L = 12 pF, connected to VSS		18		pF	

4. CPU, RAM, ROM and Banking

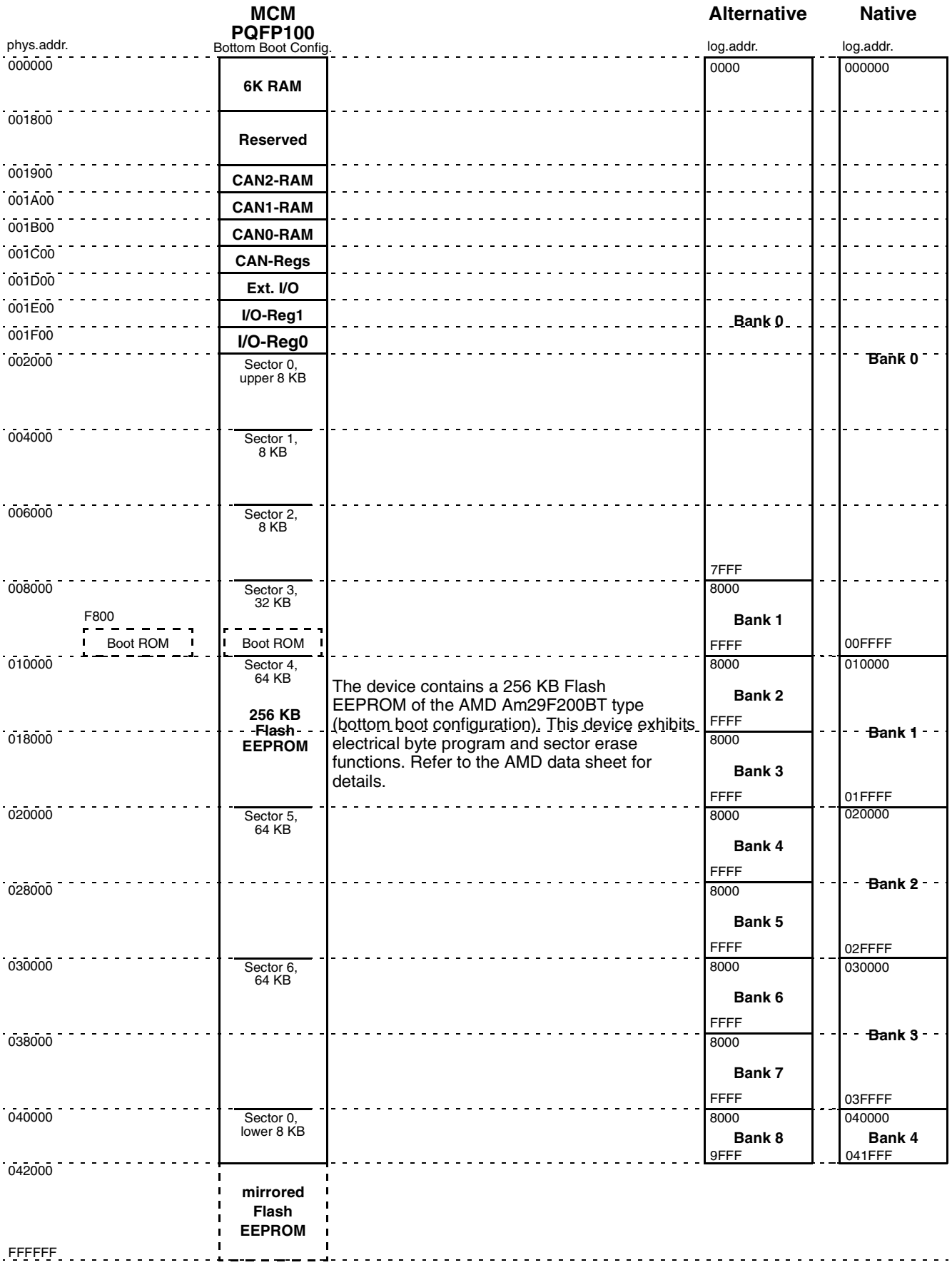


Fig. 4–1: Address Map

5. Core Logic

5.1. Control Register CR

The Control Register CR serves to configure the ways by which certain system resources are accessed during operation. The main purpose is to obtain a variable system configuration during IC test.

Upon each HIGH transition on the RESETQ pin, internal hardware reads data from the address location 00FFF3h and stores it to the CR. The state of the TEST and ESTOPCLK pins at this timepoint specifies which program storage source is accessed for this read:

Table 5–1: Control byte source

TEST	Control byte source
0 or NC	internal BOOT ROM (standard for stand-alone operation)
1	external, via multifunction pins in Bus mode (for test purposes only)

The system will thus start up according to the configuration defined in address location 00FFF3h, automatically copied to register CR.

CR Control Register

	7	6	5	4	3	2	1	0	
r/w	RESLNG	TSTTOG	x	MFM	TSTROM	IROM	IRAM	ICPU	ROM
r/w	RESLNG	TSTTOG	EBTRI	MFM	FLASH	IROM	IRAM	ICPU	Emu
	Value of 00FFF3h								Res

RESLNG **Reset Pulse Length**
r/w1: Pulse length is $4095/F_{XTAL}$
r/w0: Pulse length is $16/F_{XTAL}$
This bit specifies the length of the reset pulse which is output at pin RESETQ following an internal reset. If pin TEST is 1 the first reset after power on is short. The following resets are as programmed by RESLNG. If pin TEST is 0, all resets are long.

TSTTOG **TEST Pin Toggle** (Tables 5–2 and 5–3)
This bit is used for test purposes only. If TSTTOG is true in IC active mode, pin TEST can toggle the multifunction pins between Bus mode and normal mode.

EBTRI **Emulator Data Bus Tristate** (Table 5–3)

MFM **Multifunction Pin Mode** (Tables 5–2 and 5–3)

Table 5–2: TSTTOG and MFM usage in mask ROM parts

TSTTOG	MFM	TEST pin	Multifunction Pins
0	0	x	Bus mode
1	0	0	Bus mode
		1	normal mode
x	1	x	normal mode

Table 5–3: TSTTOG, EBTRI and MFM usage in Flash and EMU parts

TST-TOG	EBTRI	MFM	TEST pin	Multi-function Pins	Emula-tor Bus Pins
0	x	0	x	Bus mode	Flash mode
1	x	0	0	Bus mode	Flash mode
			1	normal mode	
x	0	1	x	normal mode	Emula-tor mode
	1				Flash mode

TSTROM **TestROM** (Table 5–4)

FLASH **FLASH EEPROM** (Table 5–5)

IROM **Internal ROM** (Tables 5–4 and 5–5)

Table 5–4: TSTROM and IROM usage in mask ROM parts

TSTROM	IROM	selected program storage
1	1	internal ROM
0		internal TestROM
x	0	external via Multifunction pins in Bus mode

Table 5–5: FLASH and IROM usage in FLASH and EMU parts

FLASH	IROM	selected program storage
1	1	internal FLASH EEPROM resp. Emulator Bus
0		internal BOOT ROM
x	0	external via Multifunction pins in Bus mode

IRAM **Internal RAM**
r/w1: Enable internal RAM.
r/w0: Disable internal RAM.

ICPU **Internal CPU**
r/w1: Enable internal CPU.
r/w0: Disable internal CPU.

Table 5–6: Some commonly used settings for address location 00FFF3h. A copy is automatically transferred to the CR during IC start-up.

Code	TEST Pin	Operation Mode
FFh	0	Stand-alone with internal ROM or Flash
ABh	1	External program storage connected to multifunction pins in Bus mode
DFh	0	Emulator mode (CPGA177 package)

6. Hardware Options

6.1. Functional Description

Hardware Options are available in several areas to adapt the IC function to the host system requirements:

– clock signal selection for most of the peripheral modules from f_{osc} to $f_{osc}/2^{17}$ plus some internal signals. (see table in Chapter Hardware Options of document “CDC16xxF-E Automotive Controller Family User Manual”.)

– interrupt source selection for interrupt inputs 5, 6, 7, 13, 14 and 15

– Special Out signal selection for some U and H-ports

– Rx/Tx polarity selection for SPI and UART modules

– U-port Port Slow Mode selection

Hardware Option setting requires two steps:

1. selection is done by programming dedicated address locations with the desired options’ code

2. activation is done by a read access to these dedicated address locations at least once after each reset.

Address locations 00FFB8h through 00FFBFh do not allow random setting. Their respective Hardware Options are hard-wired and can only be altered by changing a production mask for this IC. By default, the Port Slow Option is set for all U-Ports, with the exception of U1.0 to U1.3 (Port Fast Option is set). The Watchdog and Clock Monitor are activated via software by default.

Future mask ROM derivatives of this IC will not require (but will tolerate) activation of option settings by read accesses, as the ROM as well as the options will be hard-wired. Instead, the manufacturer will automatically process the setting of the dedicated address locations, as given in the ROM code file, to set the required mask changes.

To ensure compatible option settings in this IC and mask ROM derivatives when run with the same ROM code, it is recommended to always read locations 00FFA0h through 00FFC3h directly after reset. Please note that the non-programmable locations 00FFB8h through 00FFBFh may not be compatible within this IC and the mask ROM derivative.

7. Differences

This chapter describes differences of this document to predecessor document “CDC1607F-E Automotive Controller Specification”, Feb. 17, 2003, 6251-606-1AI.

#	Section	Description
1	Introduction	Table 1–1: "CDC16xxF Family Feature List" on page 3: Name and features of “Example E-Family” changed into “CDC1631F-E”, Multiplier, 8 by 8 bit added.
		Fig. 1–1: “Block diagram of CDC1605F-E/CDC1607F-E” on page 8: Multiplier, 8 by 8 bit added
2	External Components	Value of C at RESETQ changed from 47 µ to 47 n, value of C at VREF changed from 10 µ to 10 n and text added.
3	Core Logic	Table 5–1: "Control byte source" on page 17: Updated / minimized
4	CPU, RAM, ROM and Banking	Fig. 4–1: “Address Map” on page 16: Layout format corrected.
5	Differences	New Chapter

8. Data Sheet History

1. Advance Information: “CDC1607F-E Automotive Controller Specification”, Feb. 17, 2003, 6251-608-1AI. First release of the advance information. Originally created for the HW version CDC1607F-E1.

2. Advance Information: “CDC1607F-E Automotive Controller Specification”, March 31, 2003, 6251-608-2AI. Second release of the advance information. Originally created for the HW version CDC1607F-E2.

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