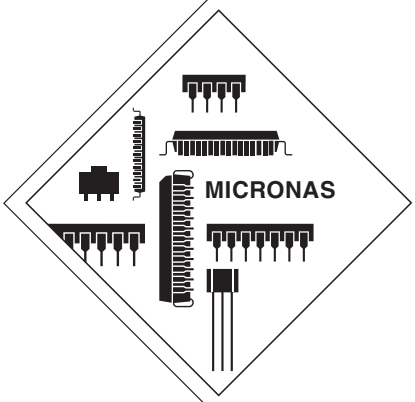

ADVANCE INFORMATION

CDC 3257G-C2
Automotive Controller

ARM POWERED®

Edition Dec. 5, 2003
6251-634-1AI

MICRONAS

Contents

1. Introduction

The device is a microcontroller for use in automotive applications. The on-chip CPU is an ARM® processor ARM7TDMI™ with 32-bit data and address bus, which supports Thumb™ format instructions.

The chip contains timer/counters, interrupt controller, multi channel AD converter, stepper motor and LCD driver, CAN interfaces and PWM outputs and a crystal clock multiplying PLL.

This document provides MCM Flash hardware specific information. General information on operating the IC can be found in the document “CDC32xxG-C Hardware Manual and CDC3205G-C Data Sheet (1PD)”.

1.1. Features

Table 1–1: CDC32xxG-C Family Feature List

			This Device:		
Item	**CDC3205G-C EMU**	**CDC3207G-C MCM Flash**	**CDC3257G-C2 MCM Flash**	**CDC3272G-C Mask ROM**	**CDC3231G-C Mask ROM**
Core					
CPU	32-bit ARM7TDMI™				
CPU-Active Operation Modes	DEEP SLOW, SLOW, FAST and PLL				
Power Saving Modes (CPU Inactive)	IDLE, WAKE and STANDBY				
CPU clock multiplication	PLL delivering up to 50MHz				
EMI Reduction Mode	selectable in PLL mode				
Oscillators	4 to 5MHz Quartz and 20 to 50kHz Internal RC				
RAM, zero wait state, 32 bit wide	32kByte		12kByte	16kByte	6kByte
ROM	ROMless, ext. up to 4M x 32/ 8M x 16	512-kByte Flash (256K x 16) top boot conf.	256-kByte Flash (128K x 16) top boot conf.	384kByte (96K x 32/ 192K x 16)	128kByte (32K x 32/ 64K x 16)
Boot ROM	8kByte (Special Function ROM)				
Digital Watchdog	✔				
Central Clock Divider	✔				
Interrupt Controller expanding IRQ	40 inputs, 16 priority levels				26 inputs, 16 priority levels
Port Interrupts including Slope Selection	6 inputs				5 inputs
Port Wake-Up Inputs including Slope / Level Selection	10 inputs				
Patch Module	10 ROM locations				
Boot System	allows in-system downloading of external code to Flash memory via JTAG			-	
Device Lock Module	Inhibits Access to internal Firmware, Lock settable by Customer			-	

Table 1–1: CDC32xxG-C Family Feature List

	This Device:				
Item	**CDC3205G-C EMU**	**CDC3207G-C MCM Flash**	**CDC3257G-C2 MCM Flash**	**CDC3272G-C Mask ROM**	**CDC3231G-C Mask ROM**
Analog					
Reset/Alarm	Combined Input for Regulator Input Supervision				
Clock and Supply Supervision	✔				
10-bit ADC, charge balance type	16 channels (each selectable as digital input)				
ADC Reference	VREF Pin, P1.0 Pin, P1.1 Pin or VREFINT Internal Bandgap selectable				
Comparators	P06COMP with 1/2 AVDD reference, WAITCOMP with Internal Bandgap reference				
LCD	Internal processing of all analog voltages for the LCD driver				
Communication					
DMA	3 DMA Channels, one each for serving the Graphics Bus interface, SPI0 and SPI1				-
UART	2: UART0 and UART1				UART0
Synchronous Serial Peripheral Interfaces	2: SPI0 and SPI1, DMA supported				
Full CAN modules V2.0B with 512-byte object RAM each (LCAN000E)	4: CAN0, CAN1, CAN2 and CAN3		2: CAN0 and CAN1		1: CAN0
DIGITbus	1 master module				-
I^2C	2 master modules: I2C0 and I2C1				I2C0
Graphics Bus Interface	8-bit data bus, DMA supported, e.g. for connection of EPSON SED 1560 LCD controller				-
Input & Output					
Universal Ports selectable as 4:1 mux LCD Segment/Backplane lines or Digital I/O Ports	up to 52 I/O or 48 LCD segment lines (=192 segments), individually configurable as I/O or LCD				up to 50 I/O or 46LCD segment lines (=184 segments)
Universal Port Slew Rate	SW selectable				
Stepper Motor Control Modules with High-Current Ports	7 Modules, 32 dI/dt controlled ports				4 Modules 23 dI/dt controlled ports
PWM Modules, each configurable as two 8-bit PWMs or one 16-bit PWM	6 Modules: PWM0/1, PWM2/3, PWM4/5, PWM6/7, PWM8/9 and PWM10/11				5 Modules: PWM0/1, PWM2/3, PWM4/5, PWM6/7, PWM8/9
Phase-Frequency Modulator	2: PFM0 and PFM1				-
Audio Module with auto-decay	✔				
SW selectable Clock outputs	2				

Table 1–1: CDC32xxG-C Family Feature List

	This Device:				
Item	**CDC3205G-C EMU**	**CDC3207G-C MCM Flash**	**CDC3257G-C2 MCM Flash**	**CDC3272G-C Mask ROM**	**CDC3231G-C Mask ROM**
Polling / Flash Timer Output	1 High-Current Port output operable in Power Saving Modes				
Timers & Counters					
16-bit free running counters with Capture/Compare modules	CCC0 with 4 CAPCOM CCC1 with 2 CAPCOM				CCC0 with 4 CAPCOM
16-bit timers	1: T0				
8-bit timers	4: T1, T2, T3 and T4				
Real Time Clock, Delivering Hours, Minutes and Seconds	✔				
Miscellaneous					
Scalable layout in CAN, RAM and ROM	-	✔			
Various randomly selectable HW options	Set by copy from user program storage during system start-up				
JTAG interface	allows Flash programming			✔	✔
On Chip Debug Aids	Embedded Trace Module, JTAG	JTAG			
Core Bond-Out	✔	-			
Supply Voltage	3.5 to 5.5V (limited I/O performance below 4.5V)				
Case Temperature Range	0 to +70C	-40 to +105C			
Package					
Type	Ceramic 257PGA	Plastic 128QFP 0.5mm pitch			
Bonded Pins	256	128	128	126	111

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1.2. Abbreviations

ADC	Analog-to-Digital Converter
AM	Audio Module
CAN	Controller Area Network Module
CAPCOM	Capture/Compare Module
CCC	Capture/Compare Counter
CPU	Central Processing Unit
DMA	Direct Memory Access Module
ERM	EMI Reduction Mode
ETM	Embedded Trace Module
I2C	I^2C Interface Module
LCD	Liquid Crystal Display Module
P06COMP	P0.6 Alarm Comparator
PWM	Pulse Width Modulator Module
SM	Stepper Motor Control Module
SPI	Serial Synchronous Peripheral Interface
T	Timer
UART	Universal Asynchronous Receiver Transmitter
WAITCOMP	Wait Comparator

1.3. Block Diagram

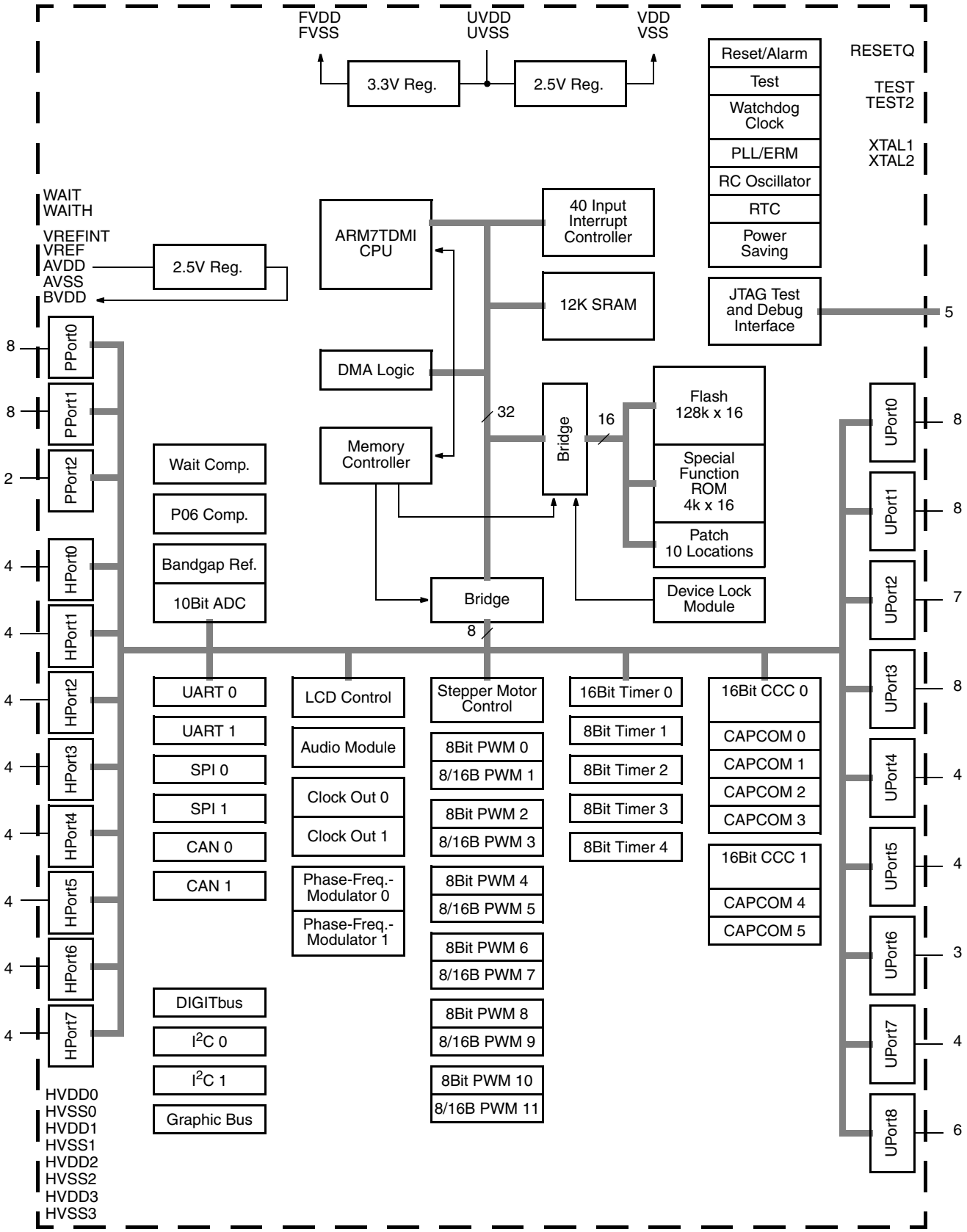
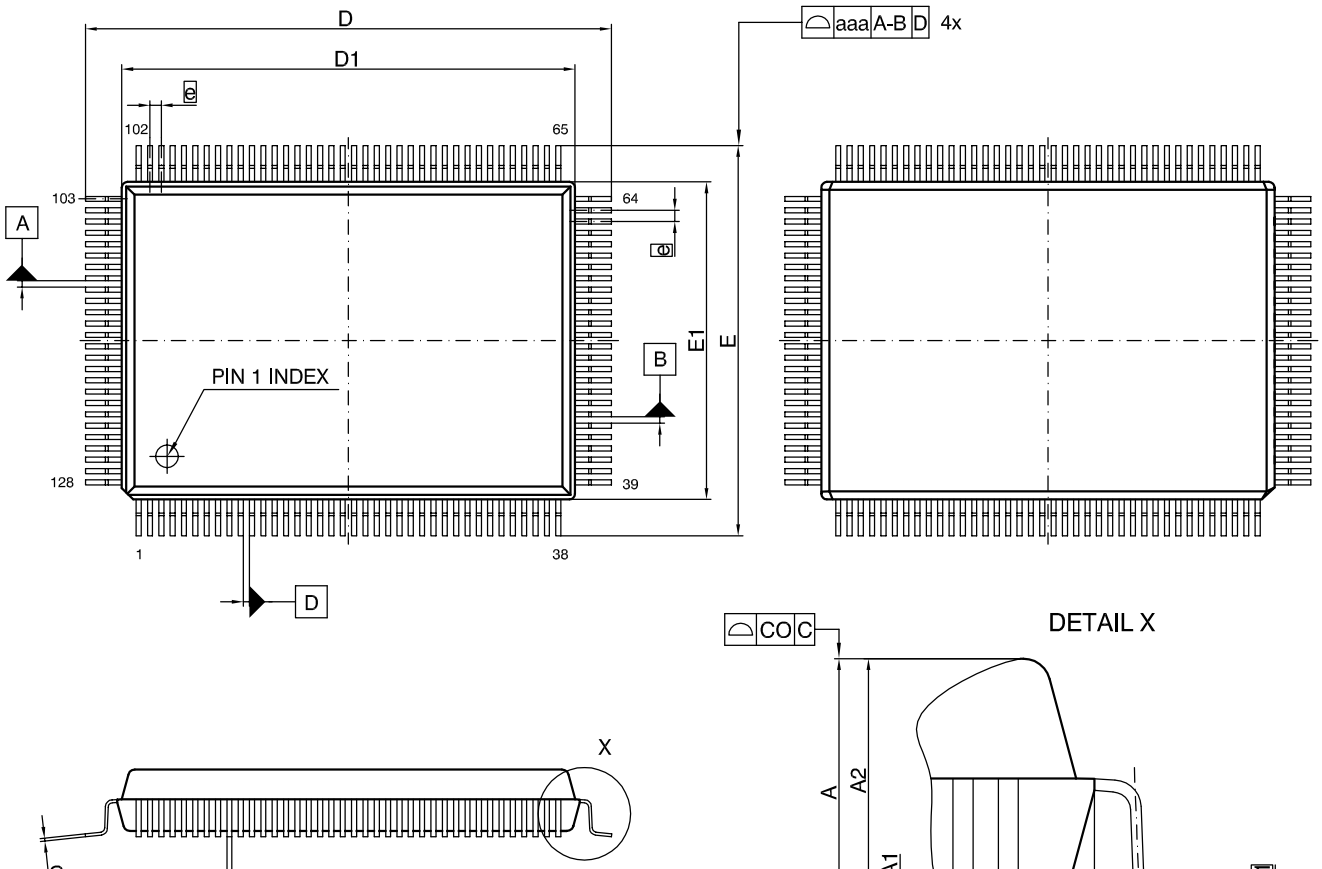


Fig. 1–1: Block diagram

2. Packages and Pins

2.1. Package Outline Dimensions



UNIT	L2	Θ
mm	1.7 1.5	0°-7°

* does not include dambar protrusion of 0.08 max. per side

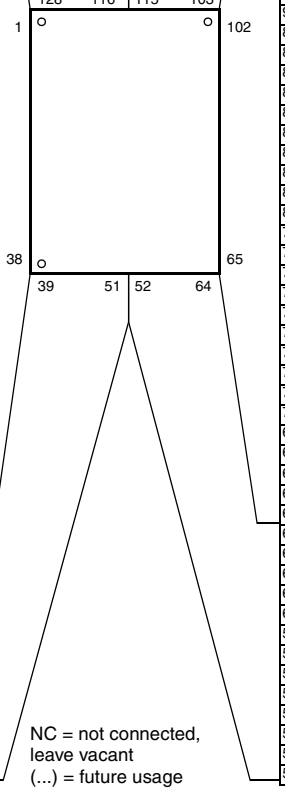
UNIT	A	A1	A2	aaa	b	Bd	c	CO	D	D1	E	E1	e	L	L1
mm	3.2 2.8	0.5 0.1	2.8 2.6	0.2	0.27 0.17	0.2	0.21 0.13	0.1	23.2	20.0	17.2	14.0	0.5	1.03 0.73	0.25

JEDEC STANDARD		ANSI	ISSUE DATE YY-MM-DD	DRAWING-NO.	SPZG-NO.
ISSUE	ITEM NO.				
B	MS-022		03-04-16	06607.0001.4	SPZG001007_001_02

Fig. 2–1:
PMQFP128-2: Plastic **M**etric **Q**uad **F**lat **P**ackage, **128** leads, 14 × 20 × 2.7 mm^3
Ordering code: MF
Weight approximately 1.81 g

2.2. Pin Assignment

Pin Functions				Note	Pin No.
LCD Mode	Port Special Out	Port Special In	Basic Function		
SEG3.1	CC1-OUT	CC1-IN / TMS	U3.1		116
SEG3.0	CC2-OUT	CC2-IN / TDI	U3.0		117
			TEST2		118
			UVDD		119
			UVSS		120
SEG2.6	DIGIT-OUT	DIGIT-IN	U2.6		121
SEG2.5	CC1-OUT	UART0-RX	U2.5		122
SEG2.4	UART0-TX	DIGIT-IN/CC1-IN	U2.4		123
SEG2.3	CC2-OUT	UART1-RX	U2.3		124
SEG2.2	UART1-TX	CC2-IN	U2.2		125
SEG7.7	CO0		U7.7/GD7		126
SEG7.6	CO1		U7.6/GD6		127
SEG7.5	LCK/PFM1		U7.5/GD5		128
SEG7.4	CC5-OUT	CC5-IN	U7.4/GD4		1
			FVDD		2
			FVSS		3
SEG5.3	CC4-OUT	CC4-IN	U5.3/GD3		4
SEG5.2	SDA1	SDA1	U5.2/GD2		5
SEG5.1	SCL1	SCL1	U5.1/GD1		6
SEG5.0	PFM0		U5.0/GD0		7
SEG2.1	SDA0	WP6/SDA0/CAN0-RX	U2.1		8
SEG2.0	SCL0/CAN0-TX	SCL0	U2.0		9
SEG1.7	PFM0	WP0/PINT0	U1.7		10
SEG1.6	INTRES/CO0	PINT1	U1.6		11
SEG1.5	CO1/CO0Q	PINT2	U1.5		12
			TEST		13
			RESETQ/ALARMQ		14
			XTAL2		15
			XTAL1		16
			VSS		17
			VDD		18
SEG1.4	ITSTOUT/AM-OUT		U1.4		19
SEG1.3	MTO/AM-PWM	WP3	U1.3		20
SEG1.2	INTRES/T0-OUT	MTI/ITSTIN	U1.2		21
SEG1.1	T1-OUT		U1.1		22
SEG1.0	T2-OUT		U1.0		23
SEG0.7	T3-OUT	WP4	U0.7		24
SEG0.6	CC3-OUT/T4-OUT	CC3-IN	U0.6		25
SEG0.5	CC3-OUT	PINT4	U0.5		26
SEG0.4	CO1	PINT5	U0.4		27
SEG0.3	PWM0		U0.3		28
SEG0.2	PWM1		U0.2		29
SEG0.1	PWM2		U0.1		30
SEG0.0	PWM3		U0.0		31
	SME1+/PWM4	SME-COMP3	H7.3		32
	SME1-/PWM6	SME-COMP2	H7.2		33
	SME2+/PWM8	SME-COMP1	H7.1		34
	SME2-/PWM9	SME-COMP0	H7.0		35
			HVDD2		36
			HVSS2		37
	PWM8		H6.3		38
	PWM9		H6.2		39
	PWM10		H6.1		40
	PWM11		H6.0		41
	SMD1+	SMD-COMP3	H5.3		42
	SMD1-	SMD-COMP2	H5.2		43
			HVDD0		44
			HVSS0		45
	SMD2+	SMD-COMP1	H5.1		46
	SMD2-	SMD-COMP0	H5.0		47
	SMA1+	SMA-COMP3	H4.3		48
	SMA1-	SMA-COMP2	H4.2		49
	SMA2+	SMA-COMP1	H4.1		50
	SMA2-	SMA-COMP0	H4.0		51



Pin No.	Note	Pin Functions			
		Basic Function	Port Special In	Port Special Out	LCD Mode
115		U3.2	CC0-IN / TCK	CC0-OUT	SEG3.2
114		U3.3		CO0/TDO	SEG3.3
113		U3.4	SPI0-CLK-IN	SPI0-CLK-OUT	SEG3.4
112		U3.5	SPI0-D-IN	TO3	SEG3.5
111		U3.6		SPI0-D-OUT	SEG3.6
110		U3.7	SPI1-CLK-IN	SPI1-CLK-OUT	SEG3.7
109		U4.0	SPI1-D-IN	CC0-OUT	BP0
108		U4.1	CC0-IN	SPI1-D-OUT	BP1
107		U4.2		CAN0-TX	BP2
106		U4.3	CAN0-RX/WP5	TO2	BP3
105		U8.0		CC4-OUT	SEG8.0
104		U8.1		CC3-OUT	SEG8.1
103		U8.2	LCD-CLK-IN		SEG8.2
102		U8.3	WP9	LCD-CLK-OUT	SEG8.3
101		U8.4	LCD-SYNC-IN		SEG8.4
100		U8.5	PINT3/WP8	LCD-SYNC-OUT	SEG8.5
99		U6.0		CAN1-TX	SEG6.0
98		U6.1	CAN1-RX/WP7	GOEQ	SEG6.1
97		U6.2		GWEQ	SEG6.2
96		P2.0			
95		P2.1			
94		P0.0	CC4-IN		
93		P0.1			
92		P0.2			
91		P0.3			
90		P0.4			
89		P0.5			
88		P0.6	P0.6 Comp.		
87		P0.7			
86		WAITH			
85		WAIT			
84		BVDD			
83		AVSS			
82		AVDD			
81		VREFINT			
80		VREF			
79		P1.0	VREF0/WP1		
78		P1.1	VREF1/WP2		
77		P1.2	PINT0		
76		P1.3	PINT1		
75		P1.4	PINT2		
74		P1.5	PINT3		
73		P1.6	PINT4		
72		P1.7	PINT5		
71		H0.0	SMG-COMP0	SMG2-/PWM7	
70		H0.1	SMG-COMP1	SMG2+/PWM5	
69		H0.2	SMG-COMP2	SMG1-/PWM3/POL	
68		H0.3	SMG-COMP3	SMG1+/PWM1	
67		HVSS3			
66		HVDD3			
65		H1.0	SMF-COMP0	SMF2-	
64		H1.1	SMF-COMP1	SMF2+	
63		H1.2	SMF-COMP2	SMF1-	
62		H1.3	SMF-COMP3	SMF1+	
61		H2.0	SMC-COMP0	SMC2-	
60		H2.1	SMC-COMP1	SMC2+	
59		HVSS1			
58		HVDD1			
57		H2.2	SMC-COMP2	SMC1-	
56		H2.3	SMC-COMP3	SMC1+	
55		H3.0	SMB-COMP0	SMB2-	
54		H3.1	SMB-COMP1	SMB2+	
53		H3.2	SMB-COMP2	SMB1-	
52		H3.3	SMB-COMP3	SMB1+	

Fig. 2–1: Pin Assignment for PQFP128 Package

2.3. Pin Function Description (differing from CDC32xxG-C User Manual)

TEST2
For normal operation with internal code connect TEST2 to System Ground (no internal pull-down).

2.4. External Components

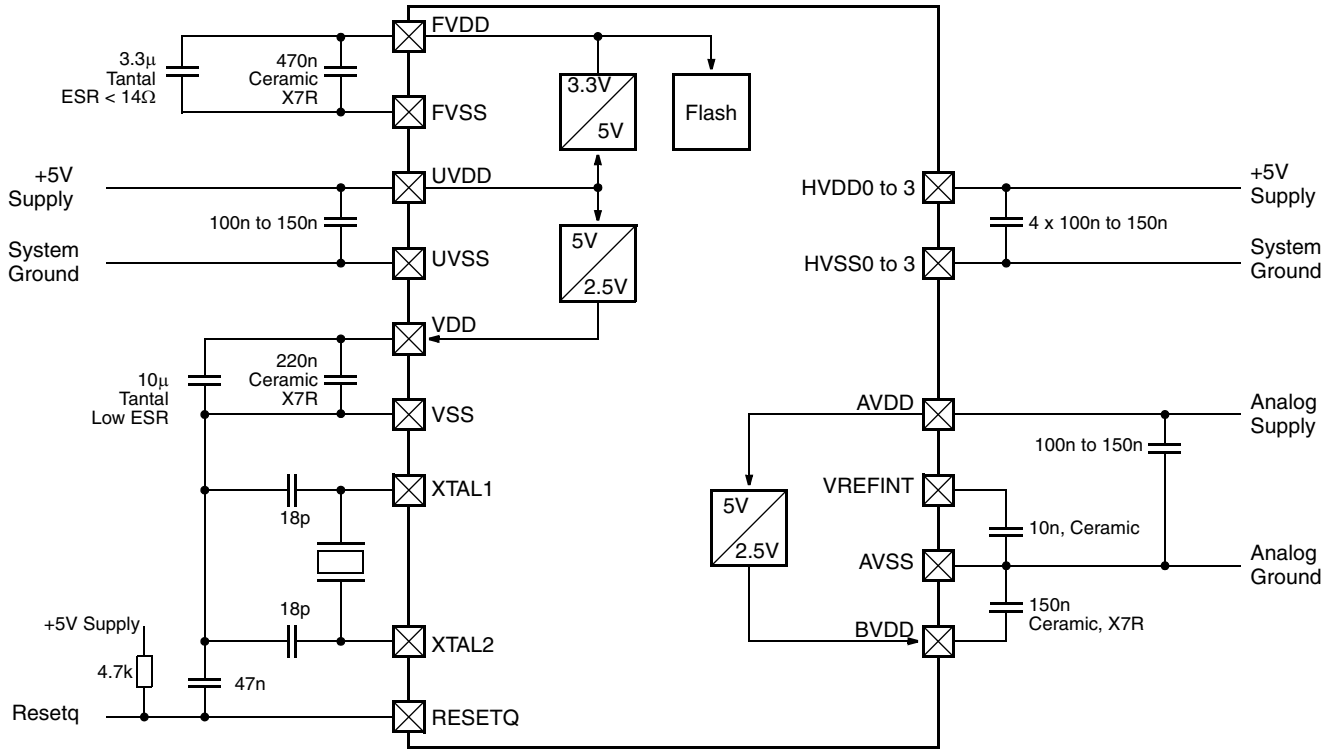


Fig. 2–2: Recommended external supply and quartz connection.

To provide effective decoupling and to improve EMC behaviour, the small decoupling capacitors must be located as close to the supply pins as possible. The self-inductance of these capacitors and the parasitic inductance and capacitance of the interconnecting traces determine the self-resonant frequency of the decoupling network. Too low a frequency will reduce decoupling effectiveness, will increase RF emissions and may adversely affect device operation.

XTAL1 and XTAL2 quartz connections are especially sensitive to capacitive coupling from other pc board signals. It is strongly recommended to place quartz and oscillation capacitors as close to the pins as possible and to shield the XTAL1 and XTAL2 traces from other signals by embedding them in a VSS trace.

The RESETQ pin adjacent to XTAL2 should be supplied with a 47nF capacitor, to prevent fast RESETQ transients from being coupled into XTAL2, to prevent XTAL2 from coupling into RESETQ, and to guarantee a time constant of ≥200µs sufficient for proper Wake Reset functionality.

3. Electrical Data

3.1. Absolute Maximum Ratings

Stresses beyond those listed in the “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these conditions is not implied. Exposure to absolute maximum ratings conditions for extended periods will affect device reliability.

This device contains circuitry to protect the inputs and outputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than absolute maximum-rated voltages to this high-impedance circuit.

Table 3–1: All voltages listed are referenced to ground (UV_{SS}=HV_{SSn}=AV_{SS}=0V), except where noted. All grounds except VSS must be connected externally low-ohmic.

Symbol	Parameter	Pin Name	Min.	Max.	Unit
V_{SUP}	Main Supply Voltage Analog Supply Voltage SM Supply Voltage	UVDD AVDD HVDD0 .. HVDD3	-0.3	6.0	V
V_{REG}	Flash Supply Voltage	FVDD	-0.3	4.0	V
	Core Supply Voltage PLL Supply Voltage	VDD BVDD	-0.3	3.0	V
I_{SUP}	Core Supply Current Main Supply Current	VDD, VSS, UVDD, UVSS	-100	100	mA
	Analog Supply Current	AVDD, AVSS	-20	20	mA
	SM Supply Current @T_{CASE}=105 °C, Duty Factor=0.71 [1])	HVDD0 .. HVDD3 HVSS0 .. HVSS3	-250	250	mA
	Flash Supply Current	FVDD, FVSS	-50	50	mA
	PLL Supply Current	BVDD	-20	20	mA
V_{in}	Input Voltage	U-Ports, XTAL,RESETQ, TEST, TEST2	UV_{SS}-0.5	UV_{DD}+0.7	V
		P-Ports VREF	UV_{SS}-0.5	AV_{DD}+0.7	V
		H-Ports	HV_{SS}-0.5	HV_{DD}+0.7	V
I_{in}	Input Current	all Inputs	0	2	mA
I_o	Output Current	U-Ports, RESETQ, WAITH	-5	5	mA
		H-Ports	-60	60	mA
t_{oshsl}	Duration of Short Circuit to UVSS or UVDD, Port SLOW Mode enabled	U-Ports, except in DP Mode		indefinite	s
T_j	Junction Temperature under Bias		-45	115	°C
T_s	Storage Temperature		-45	125	°C
P_{max}	Maximum Power Dissipation			0.8	W

[1]) This condition represents the worst case load with regard to the intended application

3.2. Recommended Operating Conditions

Do not insert the device into a live socket. Instead, apply power by switching on the external power supply.

Keep UV_{DD}=AV_{DD} during all power-up and power-down sequences.

Failure to comply with the above recommendations will result in unpredictable behavior of the device and may result in device destruction**.**

Functional operation of the device beyond those indicated in the “Recommended Operating Conditions” of this specification is not implied, may result in unpredictable behavior of the device and may reduce reliability and lifetime.

Table 3–2: All voltages listed are referenced to ground (UV_{SS}=HV_{SSn}=AV_{SS}=0V), except where noted. All grounds except VSS must be connected externally low-ohmic.

Symbol	Parameter	Pin Name	Min.	Typ	Max.	Unit
V_{SUP}	Main Supply Voltage Analog Supply Voltage	UVDD=AVDD	3.5	5	5.5	V
HV_{SUP}	SM Supply Voltage	HVDDn	4.75	5	5.25	V
dV_{DD}	Ripple, Peak to Peak	UVDD AVDD BVDD FVDD VDD			200	mV
dV_{DD}/dt	Supply Voltage Up/Down Ramping Rate	UVDD AVDD			20	V/µs
f_{XTAL}	XTAL Clock Frequency	XTAL1	4	4	5	MHz
f_{SYS}	CPU Clock Frequency, PLL on		For a list of available settings see Tables 4–1 and 4–2.			
f_{BUS}	Program Storage Clock Frequency, PLL on					
V_{il} (see Table 2-2 for a list of input types and their supply voltages)	Automotive Low Input Voltage	U-Ports H-Ports P-Ports			0.5*xV_{DD}	V
	CMOS Low Input Voltage	U-Ports, TEST, TEST2 H-Ports P-Ports			0.3*xV_{DD}	V
V_{ih} (see Table 2-2 for a list of input types and their supply voltages)	Automotive High Input Voltage	U-Ports H-Ports P-Ports	0.86*xV_{DD}			V
	CMOS High Input Voltage	U-Ports,TEST, TEST2 H-Ports P-Ports	0.7*xV_{DD}			V
RV_{il}	Reset Active Input Voltage	RESETQ			0.75	V
WRV_{il}	Reset Active Input Voltage during Power Saving Modes and Wake Reset	RESETQ			0.4	V
RV_{im}	Reset Inactive and Alarm Active Input Voltage	RESETQ	1.5		2.3	V
RV_{ih}	Reset Inactive and Alarm Inactive Input Voltage	RESETQ	3.2			V

Table 3–2: All voltages listed are referenced to ground (UV_{SS}=HV_{SSn}=AV_{SS}=0V), except where noted. All grounds except VSS must be connected externally low-ohmic.

Symbol	Parameter	Pin Name	Min.	Typ	Max.	Unit
WRV_{ih}	Reset Inactive Input Voltage during Power Saving Modes and Wake Reset	RESETQ	UV_{DD}-0.4V			V
V_{REFi}	Ext. ADC Reference Input Voltage	VREF	2.56		AV_{DD}	V
PV_i	ADC Port Input Voltage referenced to int. VREF Reference ADC Port Input Voltage referenced to ext. VREFINT Reference	P-Ports	0 0		V_{REFi} V_{REFINT}	V

3.3. Characteristics

Listed are only those characteristics that are differing from Chapter 3.3 of Document “CDC32xxG-C, Automotive Controller Family User Manual, CDC3205G-C Automotive Controller” (1PD). All not differing characteristics, that are not listed here, apply, but in a T_{CASE} temperature range extended to -40 °C to +105 °C.

Table 3–3: UV_{SS}=FV_{SS}=HV_{SSn}=AV_{SS}=0V, 3.5V<AV_{DD}=UV_{DD}<5.5V, 4.75V<HV_{DDn}<5.25V, T_{CASE}=-40 °C to +105 °C, f_{XTAL}=5MHz, external components according to Fig. 2–2 (unless otherwise noted)

Symbol	Parameter	Pin Na.	Min.	Typ [1]	Max.	Unit	Test Conditions
Package							
R_{thjc}	Thermal Resistance from Junction to Case			9		C/W	measured on Micronas typical 2-layer board, 1s1p, described in document “Integrated Circuits - Thermal Characterization of Packages” (6200-266-1E) (modified JESD-51.3)
R_{thja}	Thermal Resistance from Junction to Ambient			31		C/W	
Supply Currents (CMOS levels on all inputs, i.e. V_{il}=xV_{SS}±0.3V and V_{ih}=xV_{DD}±0.3V, no loads on outputs)							
UI_{DDp}	UVDD PLL Mode Supply Current	UVDD			50	mA	Flash Read, f_{SYS}=24MHz
UI_{DDprog}	VDD Flash Program Supply Current	UVDD			45	mA	Flash Write/Erase, all Modules OFF, [2]
UI_{DDf}	UVDD FAST Mode Supply Current	UVDD			22	mA	all Modules OFF, [2]
UI_{DDs}	UVDD SLOW Mode Supply Current	UVDD		see Fig. 3–1	1.4	mA	all Modules OFF [2] [3]
UI_{DDd}	UVDD DEEP SLOW Mode Supply Current	UVDD		see Fig. 3–1	0.9	mA	all Modules OFF [3]
UI_{DDw}	UVDD WAKE Mode Supply Current	UVDD	0	20	50	µA	RC and XTAL oscillators OFF
[1] Typical values describe typical behavior at room temperature (25 °C, unless otherwise noted), with typical Recommended Operating Conditions applied, and are not 100% tested.							

Table 3–3: $UV_{SS}=FV_{SS}=HV_{SSn}=AV_{SS}=0V$, $3.5V<AV_{DD}=UV_{DD}<5.5V$, $4.75V<HV_{DDn}<5.25V$, T_{CASE}=-40 °C to +105 °C, f_{XTAL}=5MHz, external components according to Fig. 2–2 (unless otherwise noted)

Symbol	Parameter	Pin Na.	Min.	Typ [1)]	Max.	Unit	Test Conditions
UI_{DDst}	UVDD STANDBY Mode Supply Current	UVDD		35	75	µA	RC oscillator ON, XTAL OFF
		UVDD		60	100	µA	XTAL oscillator ON, RC OFF [3)]
UI_{DDi}	UVDD IDLE Mode Supply Current	UVDD		50	TBD	µA	RC oscillator ON, XTAL OFF
				75	TBD	µA	XTAL oscillator ON, RC OFF [3)]
AI_{DDa}	AVDD Active Supply Current	AVDD		0.35	0.6	mA	ADC ON, PLL OFF
				1	2	mA	ADC and PLL ON, f_{SYS}=24MHz
AI_{DDq}	Quiescent Supply Current	AVDD	0	1	10	µA	SLOW, DEEP SLOW and power saving modes, ADC and PLL OFF
HI_{DDq}		Sum of all HVDDn	0	1	40	µA	no Output Activity, SM Module OFF
Inputs							
I_i	Input Leakage Current	TEST2	-1		1	µA	$0<V_i<UV_{DD}$
[1)] Typical values describe typical behavior at room temperature (25 °C, unless otherwise noted), with typical Recommended Operating Conditions applied, and are not 100% tested.							

[2)] Value may be exceeded with unusual Hardware Option setting

[3)] Measured with external clock. Add typically 120µA for operation on quartz with SR0.XTAL=0 (Oscillator RUN mode).

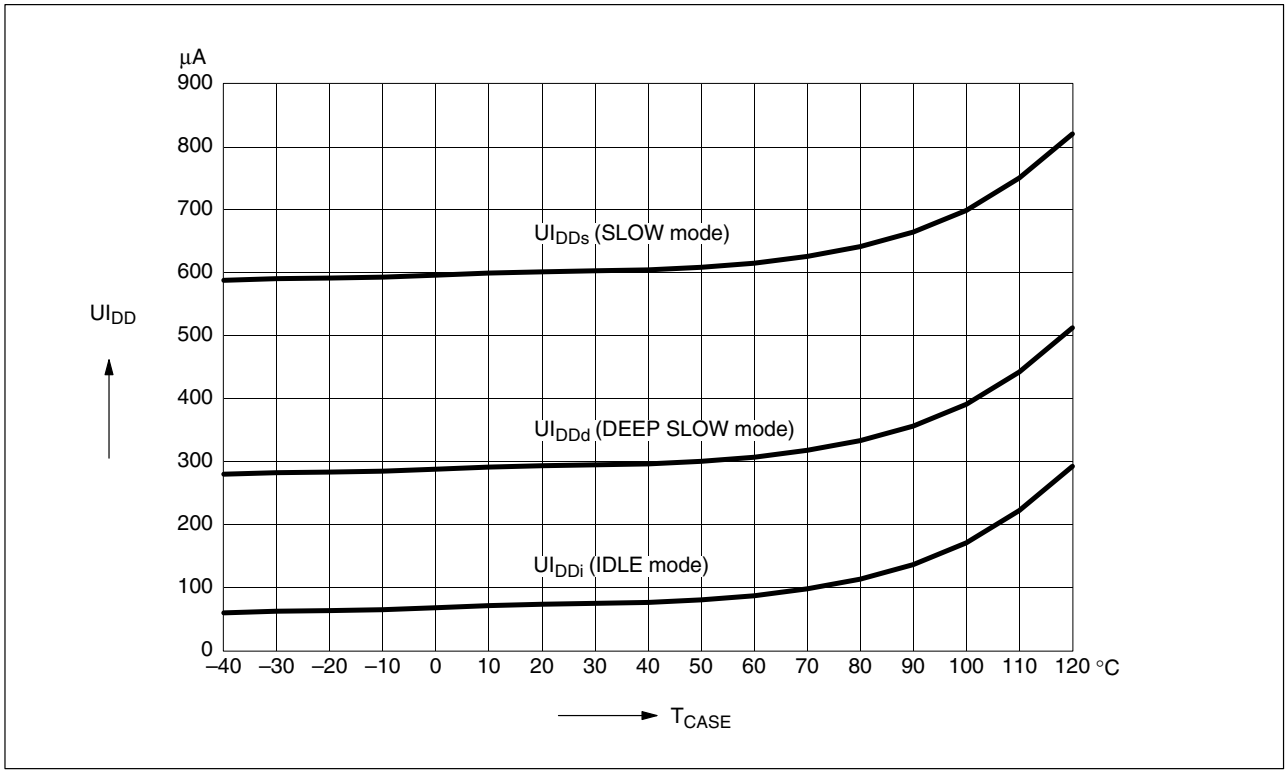


Fig. 3–1: Typical UI_{DD} characteristics over temperature @ f_{XTAL}=4MHz, 5V

3.4. Recommended Quartz Crystal Characteristics

See Chapter 3.4 of document “CDC32xxG-C, Automotive Controller Hardware Manual, CDC3205G-C EMU Data Sheet (1PD)”.

4. CPU and Clock System

4.1. Recommended Register Settings

Other settings for PMF, IOP and WSR than those given in Tables 4–1 and 4–2 shall not be used and may result in undefined behaviour. It is required not to operate I/O faster than Flash.

Suppression Strength (SUP) and Clock Tolerance (TOL) may be varied between zero and the values for strong settings according to the rules in Section 4.4.2 of the CDC32xxG-C Hardware Manual. The given limits must not be exceeded

Table 4–1: PLL and ERM Modes: Recommended Settings and Resulting Operating Frequencies (MHz)

f_{XTAL}	CPU		Flash		I/O		ERMC.EOM = 1						ERMC.EOM = 2 or 3					
							Weak		Normal		Strong		Weak		Normal		Strong	
	f_{SYS}	PLLC. PMF	f_{BUS}	WSR	$f_{IO}=f_0$	IOC. IOP	SUP	TOL	SUP	TOL	SUP	TOL	SUP	TOL	SUP	TOL	SUP	TOL
4	8	1	8	0x00	8	0	0	4	0	7	0	11	4	2	7	4	11	6
	16	3	8	0x11	8	1	0	8	0	14	0	15	8	4	14	7	22	11
	24	5	8	0x22	8	2	0	12	0	15	0	15	12	6	21	11	31	12
			12	0x11			0	10	0	10	0	10	12	2	21	2	33	2
	32	7	8	0x33	8	3	0	12	0	12	0	12	16	8	28	12	31	12
			10.67	0x22			0	12	0	12	0	12	16	8	19 23 28	9 7 6	19 23 37	9 7 6
	40	9	10	0x33	8	4	0	6	0	6	0	6	21	6	35	6	37	6
	48	11	12	0x33	8	5	0	1	0	1	0	1	25	1	42	1	42	1
5	10	1	10	0x00	10	0	0	5	0	8	0	14	5	3	8	4	14	7
	20	3	10	0x11	10	1	0	10	0	15	0	15	10	5	17	8	28	8
	30	5	10	0x22	10	2	0	14	0	14	0	14	15	8	24 26	12 11	28 30 35	10 9 8
	40	7	10	0x33	10	3	0	6	0	6	0	6	21	6	35	6	37	6
	50	9	12.5	0x33	10	4	set ERMC.EOM=0						set ERMC.EOM=0					

Table 4–2: PLL2 and ERM Modes: Settings Sacrificing Unlimited Operation of Peripheral Modules and Resulting Operating Frequencies (MHz)

f_{XTAL}	CPU		Flash		I/O		ERMC.EOM = 1						ERMC.EOM = 2 or 3					
							Weak		Normal		Strong		Weak		Normal		Strong	
	f_{SYS}	PLLC. PMF	f_{BUS}	WSR	$f_{IO}=f_0$	IOC. IOP	SUP	TOL	SUP	TOL	SUP	TOL	SUP	TOL	SUP	TOL	SUP	TOL
4	12	2	6	0x11	4	2	0	6	0	10	0	15	6	3	10	5	16	8
			12	0x00			0	5	0	5	0	5	6	2	10	2	16	2
	20	4	10	0x11	4	4	0	10	0	15	0	15	10	5	17	8	28	8
5	15	2	7.5	0x11	5	2	0	7	0	13	0	15	7	4	13	7	21	11

5. Memory and Special Function ROM (SFR) System

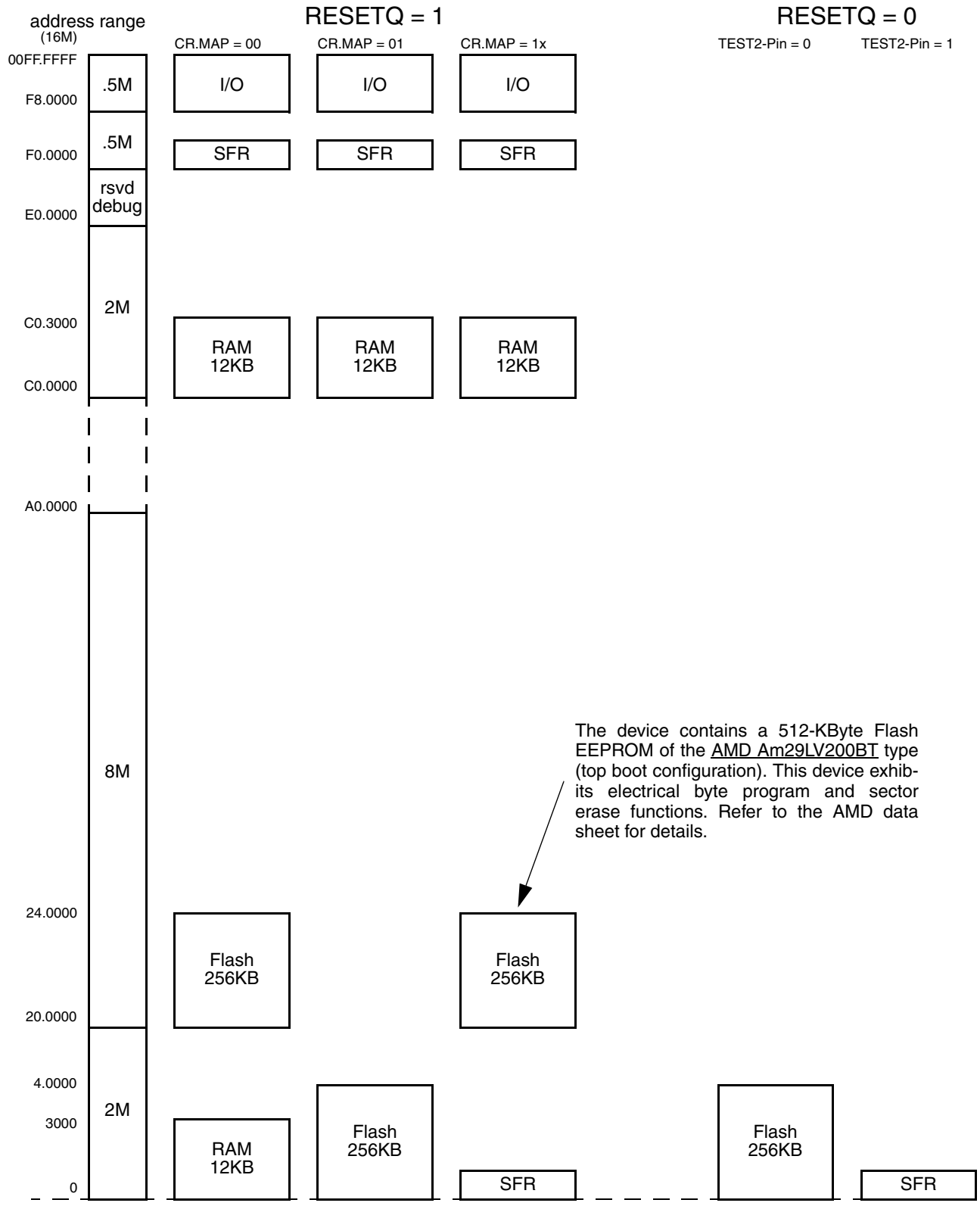


Fig. 5–1: Address Map. Most Common Settings

6. Core Logic

6.1. Control Word (CW)

A number of important system configuration properties are selectable during device start-up by means of a unique Control Word (CW).

6.1.1. Reset Active

At the end of the reset period, the device fetches this CW from address locations 0x20 to 0x23 of a source that is determined by the state of pins TEST and TEST2 and flag MFPLR.MFPL, see Table 6–1 for MCM parts, Table 6–2 for ROM parts.

Table 6–1: CW fetch in MCM parts (QFP128)

Control Word Fetch desired from	Necessary Reset configuration		
	TEST2	TEST	MFPL
Int. Flash	0	0	x
Int. Flash	0	1	1
Ext. via Multi Function port			0 [1)]
Int. Special Function ROM	1	x	x
[1)] Only available after a non-Power-On RESET with MFPL = 0 set before			

As can be seen from Table 6–1, the device disables external access (through the Multi Function port) to internal code, as long as MFPLR.MFPL is 1 (= state after UVDD power-up). Setting it to 0 requires internal SW. By this means, an effective device lock mechanism is implemented, that prevents unauthorized access to internal SW.

In ROM parts, flag MFPLR.MFPL is available, but does not lock the Multi Function port. Thus Table 6–1 reduces to Table 6–2.

Table 6–2: CW fetch in ROM parts (QFP128)

Control Word Fetch desired from	Necessary Reset config. of pins	
	TEST2	TEST
Internal ROM	0	0
External via Multi Function port	0	1
Int. Special Function ROM	1	x

6.1.2. Reset Inactive

When exiting Reset, the CW is read and stored in the Control Register (CR) and the system will start up according to the configuration defined therein.

Normally the CW is fetched from the same memory that the system will start executing code from. Table 6–3 gives fix CWs for a list of the most commonly used configurations.

Table 6–3: Some common system configurations and the corresponding CW setting

Part Type	Program Start desired from	Additional desired properties	Necessary CW	
			31:16	15:0
MCM	int. 16-Bit Flash (Am29LV200BT)	-	Don’t care	0x7F5F
ROM	int. 16-Bit ROM	-	Don’t care	0x7F5F

7. IRQ Interrupt Controller Unit (ICU)

Table 7–1: ICU Input Availability

ISN	Interrupt Source
0	Default vector, not connected
1	CC0OR
2	CC1OR
3	PINT0
4	PINT1
5	CAN0
6	SPI0
7	Timer 1
8	Timer 0
9	P06 COMP
10	RESET/ALARM
11	WAIT COMP
12	UART0
13	PINT2
14	WAPI
15	CC2OR
16	CC3OR
17	Timer 2
18	RTC
19	I2C0
20	Timer 3
21	SPI1
22	COMMRX/TX
23	PINT5
24	PINT3
25	DIGITbus
26	I2C1
27	CAN1
28	CC4OR
29	CC5OR

Table 7–1: ICU Input Availability

ISN	Interrupt Source
30	Timer 4
31	UART1
32	(Not connected)
33	(Not connected)
34	CC0COMP
35	CC1COMP
36	CC2COMP
37	CC3COMP
38	PINT4
39	GBus

8. Hardware Options

8.1. Functional Description

Hardware Options are available in several areas to adapt the IC function to the host system requirements. For details see the CDC32xxG-C Hardware Manual.

Hardware Option setting requires two steps:

1. selection is done by programming dedicated address locations in the HW Options field with the desired options' code.

2. activation is done by copying the HW Options field to the corresponding HW Options registers at least once after each reset.

In EMU and MCM devices all HW Options are SW progammable.

In mask ROM derivatives the clock options and the Watchdog, Clock and Supply Monitors are hard wired according to the HW Options field of the ROM code hex file. Those options can only be altered by changing a production mask.

To ensure compatible option settings in this IC and mask ROM derivatives when run with the same ROM code, it is mandatory to always write the HW Options field to the HW option registers directly after reset.

9. Register Cross Reference Table

9.1. 8-Bit I/O Region

Table 9–1: Base address 0x00F80000

Offs.	Byte Address				Remarks	
	3	2	1	0		Module
0xFFC					6 CAN reserved	CAN RAM
0x400						
0x3FC					CAN 1	
0x200						
0x1FC					CAN 0	
0x000						

Table 9–2: Base address 0x00F81000

Offs.	Byte Address				Remarks	
	3	2	1	0		Module
0x1FC					6 CAN reserved	CAN register
0x080						
0x07C					CAN1	
0x054						
0x050			CTIM			
0x04C	ESM	REC	TEC	OCR		
0x048	ICR	BT3	BT2	BT1		
0x044	IDM					
0x040	IDX	ESTR	STR	CTR		
0x03C					CAN0	
0x014						
0x010			CTIM			
0x00C	ESM	REC	TEC	OCR		
0x008	ICR	BT3	BT2	BT1		
0x004	IDM					
0x000	IDX	ESTR	STR	CTR		

Table 9–3: Base address 0x00F90000 (formerly 1F00)

Offs.	Byte Address				Remarks	
	3	2	1	0		Module
0x0FC	TST2	TST1	TST3	TST4		Test
0x0F8	TST5		TSTAD3	TSTAD2		
0x0F4	DGRTMA	DGTD	DGS1TA	DGTL		DIGITBus
0x0F0	DGRTMD	DGS0	DGC1	DGC0		
0x0EC					64 byte	
0x0B0						
0x0AC				ANAA		ADC
0x0A8			AD1	AD0		
0x0A4		UA0IF	UA0CA	UA0IM		UART0
0x0A0	UA0BR1	UA0BR0	UA0C	UA0D		
0x09C					32 byte	
0x080						
0x07C			CCC0H	CCC0L		CAPCOM0
0x078	CC3H	CC3L	CC3I	CC3M	CC3	
0x074	CC2H	CC2L	CC2I	CC2M	CC2	
0x070	CC1H	CC1L	CC1I	CC1M	CC1	
0x06C	CC0H	CC0L	CC0I	CC0M	CC0	
0x068					8 byte	
0x064						
0x060			DBG	CSW1		Core Logic
0x05C	SMVMUX		SMVCMP	SMVCOS		Stepper Motor Module VDO
0x058	SMVSIN	SMVC				
0x054	TIM4	TIM3	TIM2	TIM1		Timer
0x050						
0x04C	TIM0H	TIM0L			Timer0	
0x048			CCC1H	CCC1L		CAPCOM1
0x044	CC5H	CC5L	CC5I	CC5M	CC5	
0x040	CC4H	CC4L	CC4I	CC4M	CC4	
0x03C					16 byte	
0x030						
0x02C	AMDEC	AMF	AMAS	AMPRE		Audio Module
0x028	IRPM1	IRPM0				Port Interrupt
0x024					8 byte	
0x020						
0x01C		UA1IF	UA1CA	UA1IM		UART1
0x018	UA1BR1	UA1BR0	UA1C	UA1D		
0x014				CO0SEL		Core Logic
0x010	SPI1M	SPI1D	SPI0M	SPI0D		SPI
0x00C	SR1					Core Logic
0x008	SR0					
0x004				ANAU		
0x000				CSW0		

Table 9–4: Base address 0x00F90100 (formerly 1E00)

Offs.	Byte Address				Remarks	
	3	2	1	0		Module
0x0FC					16 byte	HW Options
0x0F0						
0x0EC			UA1	UA0		
0x0E8			PM			
0x0E4						
0x0E0						
0x0DC	P7P	P7C	P5P	P5C		
0x0D8	P3P	P3C	P1P	P1C		
0x0D4	P11P	P11C	P9P	P9C		
0x0D0	SP2C	SP1C	SP0C	SMC		
0x0CC	PF0C	AC	LC	DC		
0x0C8	C1C	C0C	CO1C	DMAC		
0x0C4	RZPC	CO01C	CO00C	T4C		
0x0C0	T3C	T2C	T1C	T0C		
0x0BC					96 byte	
0x060						
0x05C						PFM
0x058						
0x054	PFM1					
0x050	PFM0					
0x04C	PWMC					PWM
0x048	PWM11	PWM10	PWM9	PWM8		
0x044	PWM7	PWM6	PWM5	PWM4		
0x040	PWM3	PWM2	PWM1	PWM0		
0x03C					32 byte	
0x020						
0x01C					I2C1	I2C
0x018	I2CM1					
0x014	I2CRS1	I2CRD1	I2CWP11	I2CWP01		
0x010	I2CWD11	I2CWD01	I2CWS11	I2CWS01		
0x00C					I2C0	
0x008	I2CM0					
0x004	I2CRS0	I2CRD0	I2CWP10	I2CWP00		
0x000	I2CWD10	I2CWD00	I2CWS10	I2CWS00		

Table 9–5: Base address 0x00F90400

Offs.	Byte Address				Remarks	
	3	2	1	0		Module
0x0FC				HxPIN	H-Port7	H-Ports
0x0F8	HxLVL	HxNS	HxTRI	HxD		
0x0F4				HxPIN	H-Port6	
0x0F0	HxLVL	HxNS	HxTRI	HxD		
0x0EC				HxPIN	H-Port5	
0x0E8	HxLVL	HxNS	HxTRI	HxD		
0x0E4				HxPIN	H-Port4	
0x0E0	HxLVL	HxNS	HxTRI	HxD		
0x0DC				HxPIN	H-Port3	
0x0D8	HxLVL	HxNS	HxTRI	HxD		
0x0D4				HxPIN	H-Port2	
0x0D0	HxLVL	HxNS	HxTRI	HxD		
0x0CC				HxPIN	H-Port1	
0x0C8	HxLVL	HxNS	HxTRI	HxD		
0x0C4				HxPIN	H-Port0	
0x0C0	HxLVL	HxNS	HxTRI	HxD		
0x0BC						P-Ports
0x0B8	P2LVL		P2IE	P2PIN	P-Port 2	
0x0B4	P1LVL		P1IE	P1PIN	P-Port1	
0x0B0	P0LVL		P0IE	P0PIN	P-Port 0	
0x0AC					reserved	U-Ports
0x090						
0x084	UxMODE	UxPIN	UxLVL	UxSLOW	U-Port 8	
0x080	UxDPM	UxNS	UxTRI	UxD		
0x074	UxMODE	UxPIN	UxLVL	UxSLOW	U-Port 7	
0x070	UxDPM	UxNS	UxTRI	UxD		
0x064	UxMODE	UxPIN	UxLVL	UxSLOW	U-Port 6	
0x060	UxDPM	UxNS	UxTRI	UxD		
0x054	UxMODE	UxPIN	UxLVL	UxSLOW	U-Port 5	
0x050	UxDPM	UxNS	UxTRI	UxD		
0x044	UxMODE	UxPIN	UxLVL	UxSLOW	U-Port 4	
0x040	UxDPM	UxNS	UxTRI	UxD		
0x034	UxMODE	UxPIN	UxLVL	UxSLOW	U-Port 3	
0x030	UxDPM	UxNS	UxTRI	UxD		
0x024	UxMODE	UxPIN	UxLVL	UxSLOW	U-Port 2	
0x020	UxDPM	UxNS	UxTRI	UxD		
0x014	UxMODE	UxPIN	UxLVL	UxSLOW	U-Port 1	
0x010	UxDPM	UxNS	UxTRI	UxD		
0x004	UxMODE	UxPIN	UxLVL	UxSLOW	U-Port 0	
0x000	UxDPM	UxNS	UxTRI	UxD		

Table 9–6: Base address 0x00F90500

Offs.	Byte Address				Remarks	
	3	2	1	0		Module
0x0FC					128 Bytes	reserved
0x080						
0x07C				SMX		Power Saving
0x078			POL		Polling	
0x074				RTCC	RTC	
0x070				OSC		
0x06C						
0x068				WSC		
0x064				WPM8	Wake Ports mode	
0x060	WPM6	WPM4	WPM2	WPM0		
0x05C	RTC				RTC	
0x058	SSC					
0x054	SSR					
0x050			WUS		Wake-up source	
0x04C					reserved	GBus
0x048						
0x044				GC		
0x040				GD		
0x03C			MDL		Memory Ctrl.	Core Logic
0x030				MFPLR	DLM	
0x02C				WSR	Clock, PLL, ERM	
0x028				IOC		
0x024	ERMC					
0x020				PLLC		
0x01C					reserved	LCD
0x014						
0x010				ULCDLD		
0x00C						Patch
0x008	PER					
0x004	PDR					
0x000	PAR					

9.2. 32-Bit I/O Region

Table 9–7: Base address 0x00FFFD00

Offs.	Byte Address				Remarks	
	3	2	1	0		Module
0x0FC					252 bytes reserved	Core Logic
0x004						
0x000	CR				Control Register	

Table 9–8: Base address 0x00FFFE00

Offs.	Byte Address				Remarks	
	3	2	1	0		Module
0x0FC					rsvd Channel 4 to 31	DMA
0x020						
0x018			DC3M		Channel 3	
0x010			DC2M		Channel 2	
0x008			DC1M		Channel 1	
0x004				DST	Control	
0x000	DVB					

Table 9–9: Base address 0x00FFFF00

Offs.	Byte Address				Remarks	
	3	2	1	0		Module
0x0FC					12 bytes reserved	IRQ and FIQ Interrupt Controller
0x0F4						
0x0F0			CRF	PRF	FIQ registers	
0x0EC					40 bytes reserved	
0x0C8						
0x0C4	VTB				IRQ registers	
0x0C0	PESRC	PEPRIO	AFP	CRI		
0x0BC					128 bytes reserved	
0x040						
0x03C					Interrupt source nodes	
0x028						
0x024	ISN39	ISN38	ISN37	ISN36		
:	:	:	:	:		
0x004	ISN7	ISN6	ISN5	ISN4		
0x000	ISN3	ISN2	ISN1	ISN0		

9.3. Modified Registers

Listed are only those registers that are differing from Document “CDC32xxG-C, Automotive Controller Family User Manual, CDC3205G-C Automotive Controller” (1PD).

9.3.1. Standby Registers (cf. chapter 6.3 in User Manual)

SR0 Standby Register 0

	7	6	5	4	3	2	1	0	Offs
r/w	I2C1	I2C0	x	x	x	x	x	CAN1	3
r/w	TIM2	TIM3	TIM4	UART1	x	DGB	CCC1	x	2
r/w	LCD	x	PSLW	UART0	ADC	x	TIM1	XTAL	1
r/w	SM	x	x	x	SPI1	CAN0	CCC0	SPI0	0
	0x00000100								Res

Standby Register 0 (SR0) flags CAN2 and CAN3 at byte offest 3, bit number 1 and 2 are not available in this part.

10. Data Sheet History

1. Advance Information: “CDC3257G-C2 Automotive Controller Specification”, Dec. 5, 2003, 6251-634-1AI.
First release of the advance information.
Originally created for HW version CDC3257G-C2.

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