NTQD4154Z

Power MOSFET

20 V, 7.5 A, Common−Drain, Dual N−Channel TSSOP−8

Features

- Common Drain for Ease of Circuit Connection
- Low $R_{DS(on)}$ Extending Battery Life
- ESD Protected Gate

Applications

- Li−Ion Battery Protection Circuit
- Power Management in Portable and Battery−Powered Products

MAXIMUM RATINGS (T_J = 25°C unless otherwise stated)

Parameter			Symbol	Value	Units
Drain−to−Source Voltage			V_{DSS}	20	V
Gate−to−Source Voltage			V_{GS}	±12	V
Continuous Drain Current (Note 1)	Steady State	T_A = 25°C	I_D	7.5	A
		T_A = 75°C		5.8	
Power Dissipation (Note 1)	T_A = 25°C		P_D	1.52	W
Continuous Drain Current (Note 2)	t ≤ 10 s	T_A = 25°C	I_D	9.8	A
		T_A = 75°C		7.6	
Power Dissipation (Note 2)	t ≤ 10 s	T_A = 25°C	P_D	2.6	W
Pulsed Drain Current	tp = 10 μs		I_{DM}	30	A
Operating Junction and Storage Temperature			T_J, T_{STG}	−55 to 150	°C
Source Current (Body Diode)			I_S	2.2	A
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			T_L	260	°C

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Units
Junction−to−Ambient – Steady State	$R_{\theta JA}$	82	°C/W
Junction−to−Ambient − t ≤ 10 s	$R_{\theta JA}$	48	

1. Mounted onto a 2″ square FR−4 board (1″ sq. 2 oz. cu. 0.06″ thick single−sided), steady state.
2. Mounted onto a 2″ square FR−4 board (1″ sq. 2 oz. cu. 0.06″ thick single−sided), t ≤ 10 secs.

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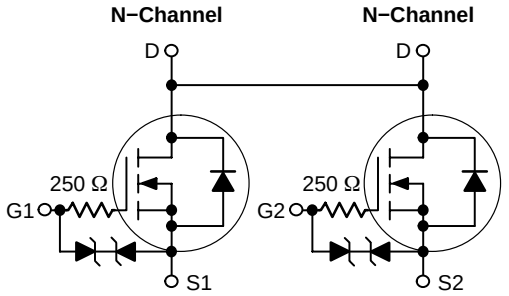
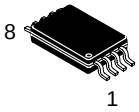
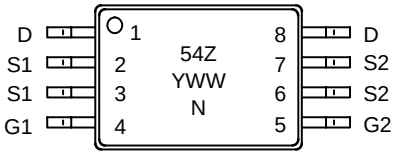
$V_{(BR)DSS}$	$R_{DS(on)}$ TYP	I_D MAX
20 V	15 mΩ @ 4.5 V	7.5 A
	21 mΩ @ 2.5 V	





TSSOP−8
CASE 948S
PLASTIC

MARKING DIAGRAM & PIN ASSIGNMENT



Top View

54Z = Device Code
Y = Year
WW = Work Week
N = MOSFET

ORDERING INFORMATION

Device	Package	Shipping†
NTQD4154Z	TSSOP−8	100 Units/Rail
NTQD4154ZR2	TSSOP−8	4000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (T_J=25°C unless otherwise stated)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 μA		20			V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$				12		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 16 V	T_J = 25°C			1.0	μA
			T_J = 125°C			25	
Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±4.5 V				±1.0	μA
ON CHARACTERISTICS (Note 3)							
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250 μA		0.6		1.5	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$				4.1		mV/°C
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = 4.5 V, I_D = 7.5 A			15	19	mΩ
		V_{GS} = 2.5 V, I_D = 5.5 A			21	26	
Forward Transconductance	g_{FS}	V_{GS} = 10 V, I_D = 7.5 A			46		S
CHARGES AND CAPACITANCES							
Input Capacitance	C_{ISS}	V_{GS} = 0 V, f = 1.0 MHz, V_{DS} = 16 V			1485		pF
Output Capacitance	C_{OSS}				220		
Reverse Transfer Capacitance	C_{RSS}				175		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 4.5 V, V_{DS} = 10 V, I_D = 7.5 A			21.5		nC
Threshold Gate Charge	$Q_{G(TH)}$				4.0		
Gate−to−Source Charge	Q_{GS}				6.0		
Gate−to−Drain Charge	Q_{GD}				5.5		
SWITCHING CHARACTERISTICS (Note 4)							
Turn−On Delay Time	$t_{d(ON)}$	V_{GS} = 4.5 V, V_{DD} = 10 V, I_D = 7.5 A, R_G = 6.0 Ω			0.2		μs
Rise Time	t_r				0.5		
Turn−Off Delay Time	$t_{d(OFF)}$				1.12		
Fall Time	t_f				0.86		
DRAIN−SOURCE DIODE CHARACTERISTICS (Note 3)							
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = 6.5 A	T_J = 25°C		0.8	1.2	V
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, dI_{SD}/dt = 100 A/μs, I_S = 6.5 A			1.02		μs
	t_a				0.32		
	t_b				0.7		
	Q_{RR}				11.6		μC

3. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
4. Switching characteristics are independent of operating junction temperatures.

TYPICAL PERFORMANCE CURVES (T_J = 25°C unless otherwise noted)

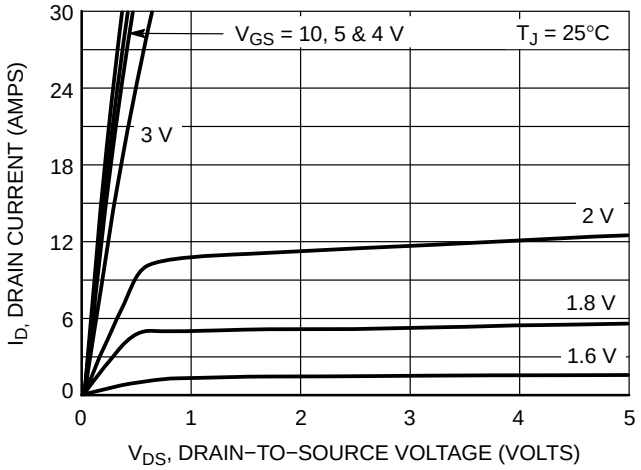


Figure 1. On−Region Characteristics

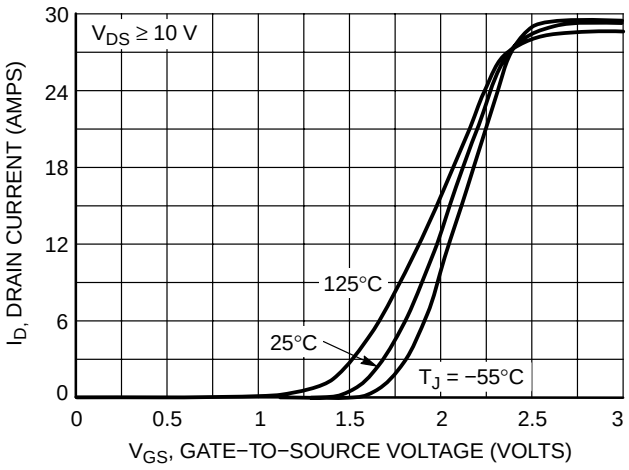


Figure 2. Transfer Characteristics

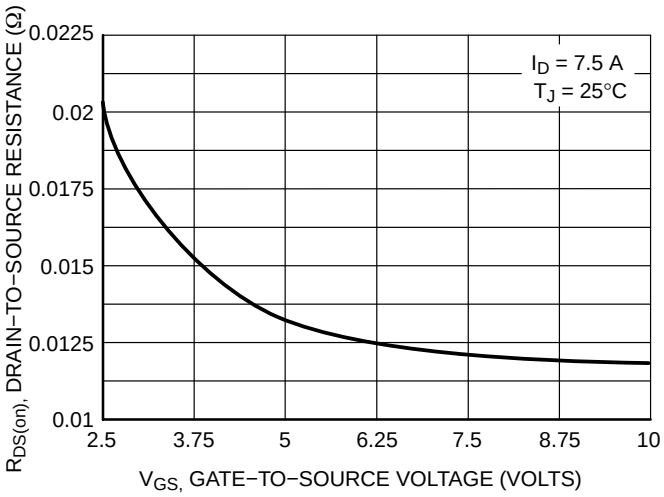


Figure 3. On−Resistance vs. Gate−to−Source Voltage

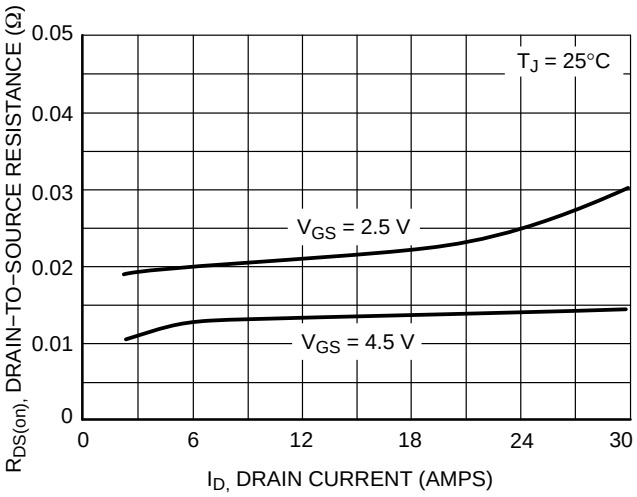


Figure 4. On−Resistance vs. Drain Current and Gate Voltage

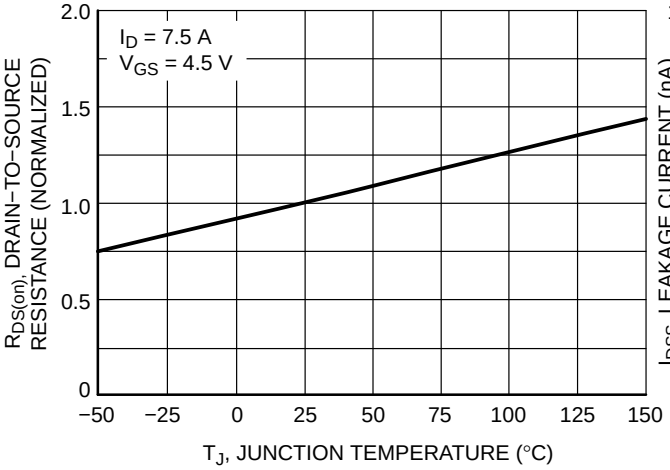


Figure 5. On−Resistance Variation with Temperature

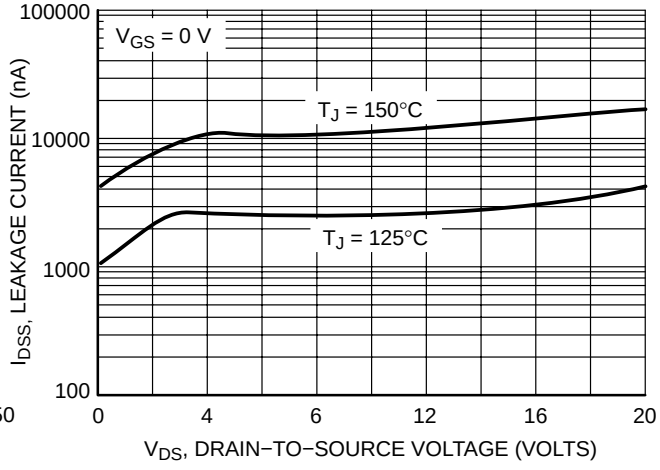


Figure 6. Drain−to−Source Leakage Current vs. Voltage

TYPICAL PERFORMANCE CURVES (T_J = 25°C unless otherwise noted)

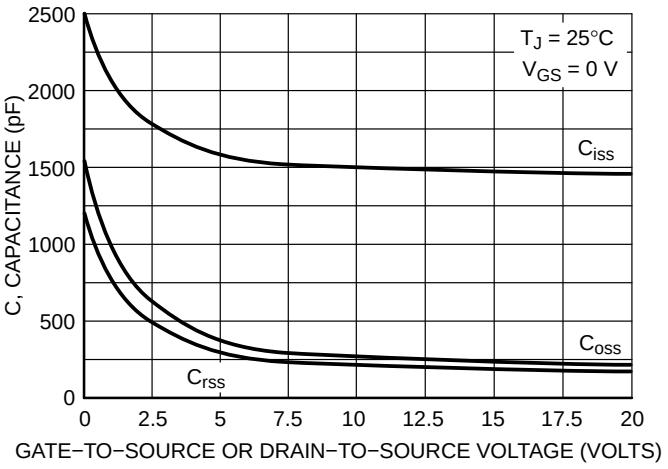


Figure 7. Capacitance Variation

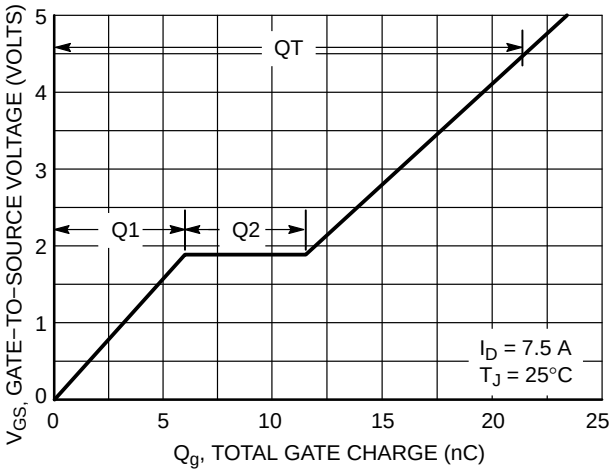


Figure 8. Gate−to−Source Voltage vs. Total Gate Charge

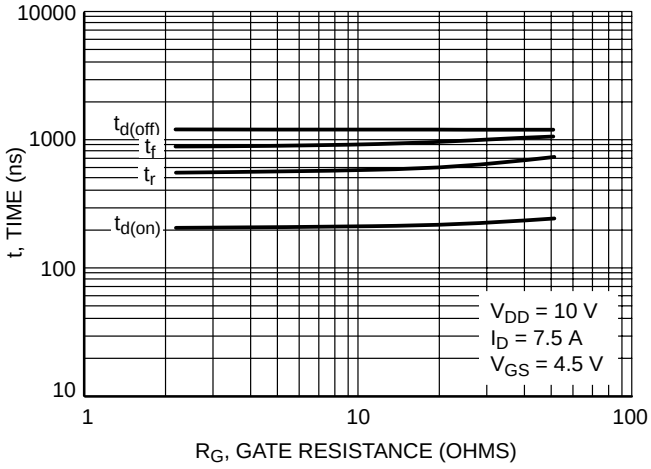


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

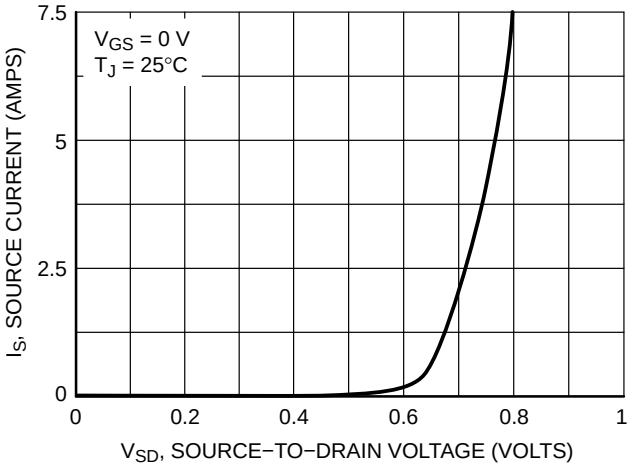


Figure 10. Diode Forward Voltage vs. Current

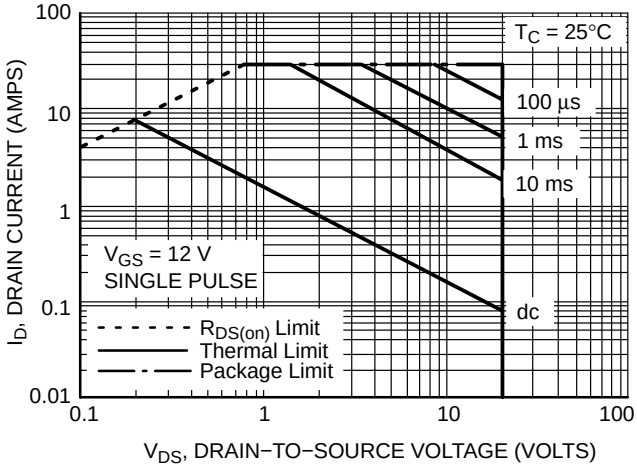


Figure 11. Maximum Rated Forward Biased Safe Operating Area

PACKAGE DIMENSIONS

TSSOP−8
CASE 948S−01
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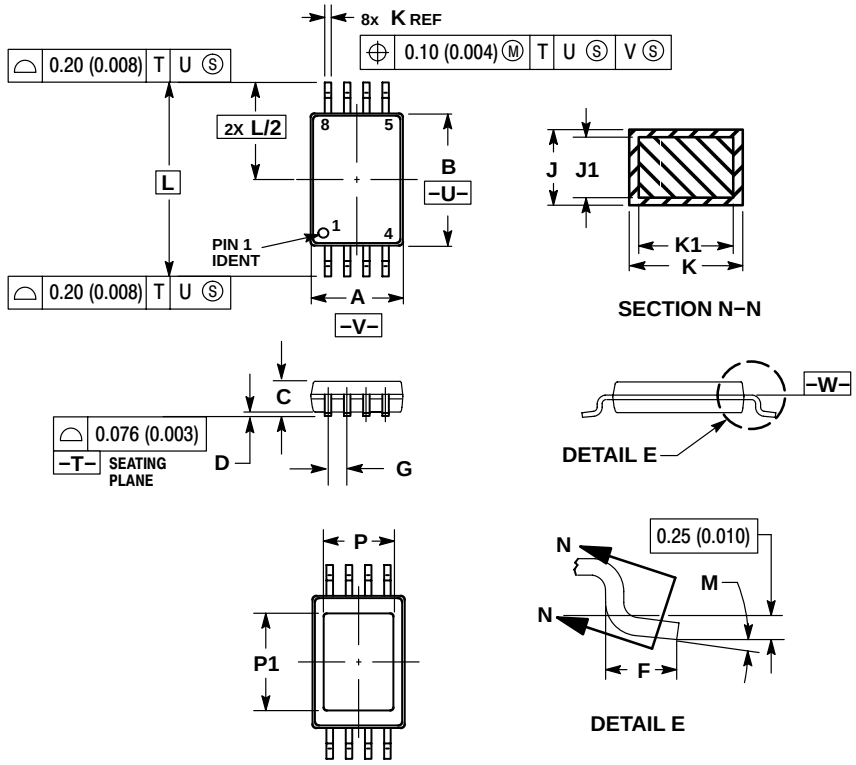
ISSUE O



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B	4.30	4.50	0.169	0.177
C	---	1.10	---	0.043
D	0.05	0.15	0.002	0.006
F	0.50	0.70	0.020	0.028
G	0.65 BSC		0.026 BSC	
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°
P	---	2.20	---	0.087
P1	---	3.20	---	0.126

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