National Semiconductor

# LM49150

## Boomer® Audio Power Amplifier Series

March 4, 2009

# Mono Class D Audio Subsystem with Earpiece Driver and Stereo Ground Referenced Headphone Amplifiers

## General Description

The LM49150 is a fully integrated audio subsystem designed for portable handheld applications such as cellular phones. Part of National's Power Wise® product family, the LM49150 consumes very low power in the various modes of operation and still providing great audio performance. The LM49150 combines a 1.25W mono E²S (Enhanced Emission Suppression) class D amplifier, 135mW Class AB earpiece amplifier, 42mW/channel stereo ground reference headphone amplifiers, volume control, and mixing circuitry into a single device.

The filterless class D amplifier delivers 1.25W into an 8Ω load with <1% THD+N with a 5V supply. The E²S class D amplifier features a patented, ultra low EMI PWM architecture that significantly reduces RF emissions while preserving audio quality. The 42mW/channel headphone drivers feature National's ground referenced architecture that creates a ground-referenced output from a single supply, eliminating the need for bulky and expensive DC-blocking capacitors, saving space and minimizing cost.

The LM49150 features a fully differential mono input, and two single-ended stereo inputs. The three inputs can be mixed/multiplexed to either the speaker or headphone amplifiers. Each input channel has an independent, 32-step digital volume control. The headphone output stage features an additional, 8-step gain control, while the speaker output stage has a selectable 6dB or 12dB gain. The mixer, volume control and device mode select are controlled through an I²C compatible serial interface.

The LM49150's superior click and pop suppression eliminates audible transients on power-up/down and during shutdown. The LM49150 is available in a ultra-small 20-bump micro SMD package (2.225mm X 2.644mm).

## Key Specifications

- Output power at $V_{DD}$ = 5V:

| | |
|---|---|
| Speaker: | |
| $R_L$ = 8Ω BTL, THD+N ≤ 1% | 1.25W (typ) |
| Headphone: | |
| $R_L$ = 32Ω SE, THD+N ≤ 1% | 42mW (typ) |
| Earpiece: | |
| $R_L$ = 8Ω SE, THD+N ≤ 1% | 135mW (typ) |

- Output power at $V_{DD}$ = 3.3V:

| | |
|---|---|
| Speaker: | |
| $R_L$ = 8Ω BTL, THD+N ≤ 1% | 520mW (typ) |
| Headphone: | |
| $R_L$ = 32Ω BTL, THD+N ≤ 1% | 42mW (typ) |
| Earpiece: | |
| $R_L$ = 8Ω SE, THD+N ≤ 1% | 35mW (typ) |

- Output Offset

| | |
|---|---|
| LS Mode | 9mV (typ) |
| HP Mode | 1mV (typ) |
| Earpiece | 1mV (typ) |

- Single Supply Operation ($V_{DD}$) 2.7 to 5.5V
- I²C Single Supply Operation 1.7 to 5.5V

## Features

- E²S class D amplifier
- Ground referenced headphone outputs — eliminates output coupling capacitors
- I²C volume and mode control
- Mono earpiece amplifier
- Flexible output for speaker and headphone output
- 20–bump micro SMD package
- Soft enable function
- "Click and Pop" suppression circuitry
- Thermal shutdown protection
- Low supply current
- Micro-power shutdown

## Applications

- Mobile Phones
- PDAs
- Portable Electronics

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LM49150 Mono Class D Audio Subsystem with Earpiece Driver and Stereo Ground Referenced Headphone Amplifiers

## Typical Application

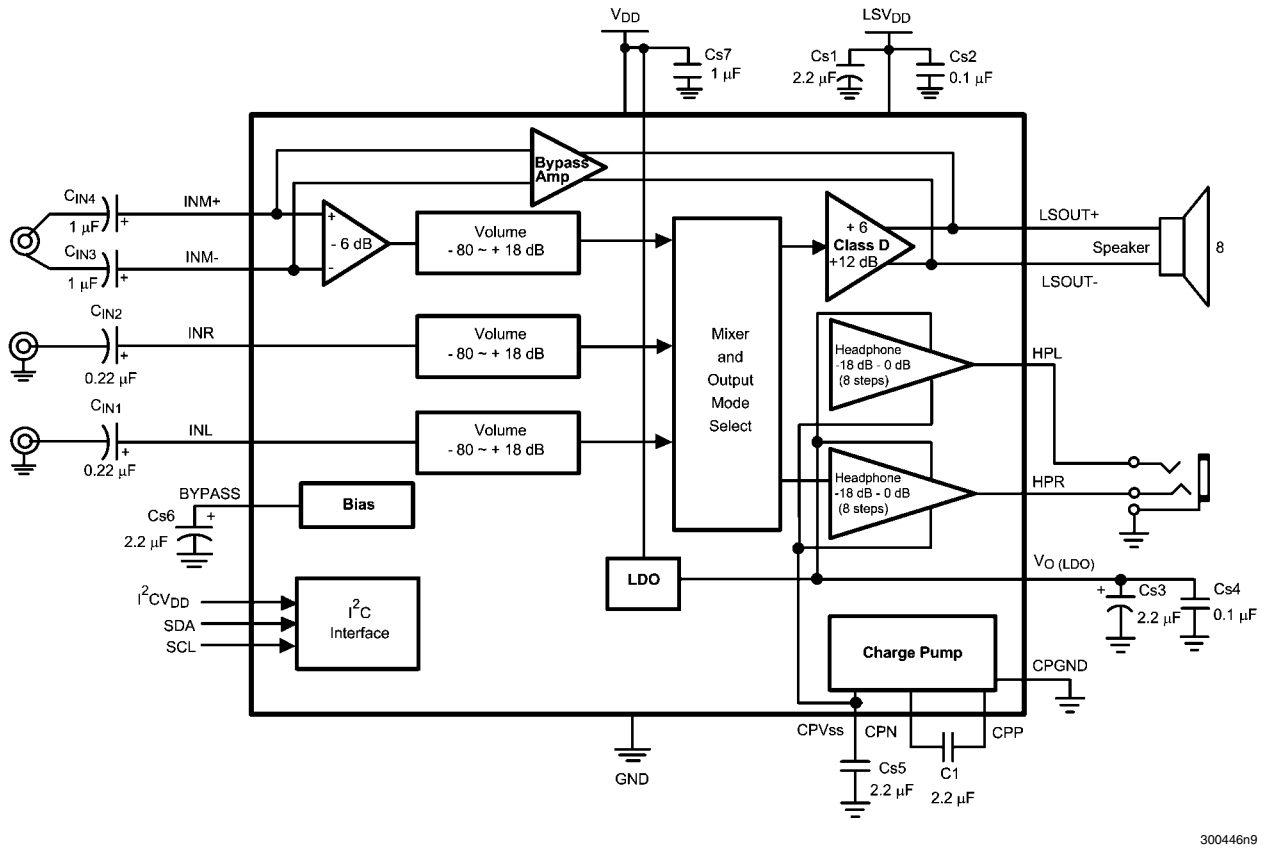
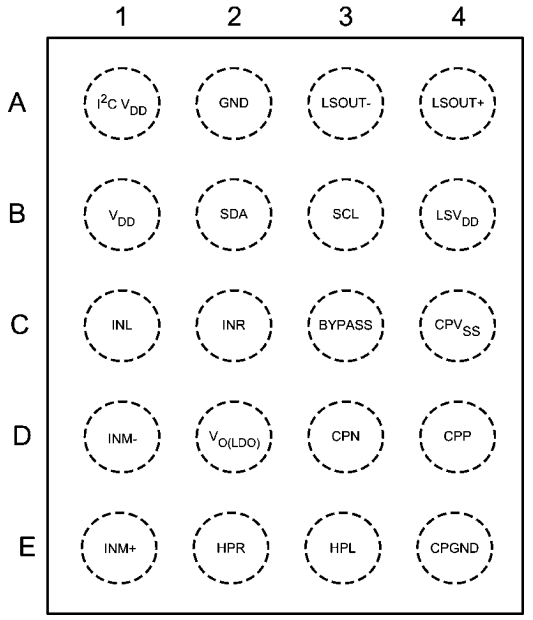



**FIGURE 1. Typical Audio Amplifier Application Circuit-Output Capacitor-less**

## Connection Diagrams

**20 Bump micro SMD Package**

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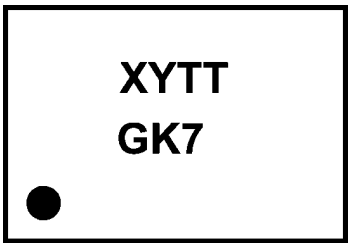
**Top View**
**(Bump Side Down)**
**(See NS Package Number TLA20KGA)**

**Top Markings**

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**Top View**
**XY - Date Code**
**TT - Die Traceability**
**G- Boomer**
**K7 - LM49150TL**

**Ordering Information**

| Order Number | Package | Package DWG # | Transport Media | Green Status |
|---|---|---|---|---|
| LM49150TL | 20 Bump micro SMD | TLA20KGA | 250 units on tape and reel | NOPB |
| LM49150TLX | 20 Bump micro SMD | TLA20KGA | 3000 units on tape and reel | NOPB |

## Bump Descriptions

| Bump | Name | Description |
|---|---|---|
| A1 | $I^2CV_{DD}$ | $I^2C$ Power Supply |
| A2 | GND | Ground |
| A3 | LSOUT- | Inverting Loudspeaker Output |
| A4 | LSOUT+ | Non-Inverting Loudspeaker Output |
| B1 | $V_{DD}$ | Analog Power Supply |
| B2 | SDA | $I^2C$ Data Input |
| B3 | SCL | $I^2C$ Clock Input |
| B4 | $LSV_{DD}$ | Loudspeaker Power Supply |
| C1 | INL | Left Channel Input |
| C2 | INR | Right Channel Input |
| C3 | BYPASS | Mid-Rail Supply Bypass |
| C4 | $CPV_{SS}$ | Charge Pump Output |
| D1 | INM- | Mono Channel Inverting Input |
| D2 | $V_{O(LDO)}$ | Internal LDO Output |
| D3 | CPN | Charge Pump Flying Capacitor - Negative Terminal |
| D4 | CPP | Charge Pump Flying Capacitor - Positive Terminal |
| E1 | INM+ | Mono Channel Non-Inverting Input |
| E2 | HPR | Right Channel Headphone Amplifier Output |
| E3 | HPL | Left Channel Headphone Amplifier Output |
| E4 | CPGND | Charge Pump Ground |

## Absolute Maximum Ratings (Notes 1, 2)

**If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.**

| | |
|---|---|
| Supply Voltage (Note 1) | 6.0V |
| Storage Temperature | −65°C to +150°C |
| Input Voltage | −0.3 to $V_{DD}$ +0.3 |
| Power Dissipation (Note 3) | Internally Limited |
| ESD Rating (Note 4) | 2.0kV |
| ESD Rating (Note 5) | 200V |
| Junction Temperature | 150°C |
| Soldering Information | See AN-1112 "Micro SMD Wafer Level Chip Scale Package" |
| Thermal Resistance | |
| $\theta_{JA}$ (typ) - TLA20KGA | 46.1°C/W |

## Operating Ratings

| | |
|---|---|
| Temperature Range | −40°C to 85°C |
| Supply Voltage | $2.7V \leq V_{DD} \leq 5.5V$ |
| Supply Voltage ($I^2C$) (Note 10) | $1.7V \leq I^2CV_{DD} \leq 5.5V$ |

## Electrical Characteristics 3.3V (Note 2)

The following specifications apply for $V_{DD}$ = $LSV_{DD}$ = 3.3V, $A_V$ = 0dB, Loudspeaker $R_L$ = 15µH+8Ω+15µH (Note 8), Earpiece $R_L$ = 8Ω, f = 1kHz, unless otherwise specified. Limits apply for $T_A$ = 25C. LS = Loudspeaker, HP = Headphone, EP = Earpiece.

| Symbol | Parameter | Conditions | LM49150 Typical (Note 6) | LM49150 Limits (Note 7) | Units (Limits) |
|---|---|---|---|---|---|
| $I_{DD}$ | Supply Current | $V_{IN}$ = 0, No Load | | | |
| | | LS mode 1 | 3.7 | 5 | mA (max) |
| | | HP mode 8 | 4.7 | 6.7 | mA (max) |
| | | EP Bypass mode | 0.8 | 1.2 | mA (max) |
| | | LS + HP mode 5 and mode 10 | 7 | 9.5 | mA (max) |
| | | LS mode 1, GAMP_SD = 1 | 3 | 4 | mA (max) |
| | | HP mode 8, GAMP_SD = 1 | 4.3 | 6.1 | mA (max) |
| $I_{SD}$ | Shutdown Current | | 0.04 | 1 | µA (max) |
| $V_{OS}$ | Output Offset Voltage | $V_{IN}$ = 0V, LS, $R_L$ = 8Ω<br>LS Gain = 6dB, Stereo mode 10 | 9 | 40 | mV (max) |
| | | $V_{IN}$ = 0V, HP, $R_L$ = 32Ω<br>Ground Referenced, Stereo mode 10 | 1 | 5 | mV (max) |
| | | $V_{IN}$ = 0V, EP Bypass only, $R_L$ = 8Ω | 0.8 | 5 | mV (max) |
| $P_O$ | Output Power | LS mode 1, THD+N = 1%, f = 1kHz<br>LS Gain = 6dB, $R_L$ = 4Ω | 845 | | mW |
| | | LS mode 1, THD+N = 1%, f = 1kHz<br>LS Gain = 6dB, $R_L$ = 8Ω | 520 | 450 | mW (min) |
| | | HP mode 8, THD+N = 1%, f = 1kHz<br>HP Attenuation = 0dB, $R_L$ = 16Ω | 42 | | mW |
| | | HP mode 8, THD+N = 1%, f = 1kHz<br>HP Attenuation = 0dB, $R_L$ = 32Ω | 43 | 39 | mW (min) |
| | | EP Bypass only, THD+N = 1%, f = 1kHz<br>$R_L$ = 8Ω | 35 | 28 | mW (min) |
| THD+N | Total Harmonic Distortion + Noise | LS mode 1, f = 1kHz<br>$P_{OUT}$ = 250mW; $R_L$ = 8Ω | 0.02 | | % |
| | | HP mode 8, f = 1kHz<br>$P_{OUT}$ = 20mW; $R_L$ = 32Ω | 0.009 | | % |
| | | EP Bypass only, f = 1kHz<br>$P_{OUT}$ = 20mW; $R_L$ = 8Ω | 0.15 | | % |
| η | Efficiency | LS output | 88 | | % |

| Symbol | Parameter | Conditions | LM49150 | | Units (Limits) |
|---|---|---|---|---|---|
| | | | Typical (Note 6) | Limits (Note 7) | |
| $\epsilon_{OUT}$ | Output Noise | A-weighted, inputs terminated to AC GND, Output referred | | | |
| | | EP Bypass | 11 | | µV |
| | | LS; Mode 1 | 41 | | µV |
| | | LS; Mode 2 | 41 | | µV |
| | | LS; Mode 3 | 43 | | µV |
| | | HP; Mode 4 | 9 | | µV |
| | | HP; Mode 8 | 10 | | µV |
| | | HP; Mode 12 | 12 | | µV |
| PSRR | Power Supply Rejection Ratio | $V_{RIPPLE}$ = 200m$V_{PP}$; f = 217Hz, $R_L$ = 8Ω, $C_B$ = 2.2µF, All audio inputs terminated to AC GND, output referred | | | |
| | | EP Bypass | 95 | | dB |
| | | Loudspeaker Output; LS Gain = 6dB | | | |
| | | LS; Mode 1 | 72 | | dB |
| | | LS; Mode 2 | 67 | | dB |
| | | LS; Mode 3 | 71 | | dB |
| | | Headphone Output, HP Attenuation = 0dB | | | |
| | | HP; Mode 4 | 91 | | dB |
| | | HP; Mode 8 | 83 | | dB |
| | | HP; Mode 12 | 81 | | dB |
| | Volume Control Step Size Error | | ±0.2 | | dB |
| | Digital Volume Control Range | Maximum Attenuation | -92 | | dB |
| | | Volume Step 2 | -46.5 | -49<br>-44 | dB (min)<br>dB (max) |
| | | Maximum Gain | 18 | 17<br>19 | dB (min)<br>dB (max) |
| $A_M$ | Mute Attenuation | HP | 98 | | dB |
| | | LS | 98 | | dB |
| $Z_{IN}$ | Mono Channel Input Impedance<br>$L_{IN}$ and $R_{IN}$ Input Impedance | Maximum gain setting | 12.9 | 10<br>15 | kΩ (min)<br>kΩ (max) |
| | | Maximum attenuation setting | 111 | 90<br>130 | kΩ (min)<br>kΩ (max) |
| | EP Bypass Resistance | | 62 | 50<br>80 | kΩ (min)<br>kΩ (max) |
| CMRR | Common-Mode Rejection Ratio | f = 217Hz, $V_{CM}$ = 1$V_{P-P}$, $R_L$ = 8Ω<br>EP Bypass | 55 | | dB |
| | | f = 217Hz, $V_{CM}$ = 1$V_{P-P}$, $R_L$ = 8Ω<br>LS, Mode 1 | 55 | | dB |
| | | f = 217Hz, $V_{CM}$ = 1$V_{P-P}$, $R_L$ = 32Ω<br>HP, Mode 4 | 61 | | dB |
| $X_{TALK}$ | Crosstalk | HP mode 8; $P_O$ = 12mW<br>$R_L$ = 32Ω, f = 1kHz | 78 | | dB |
| $T_{ON}$ | Turn-On Time | $C_B$ = 2.2µF, HP,<br>Normal Turn-On Mode | 27 | | ms |
| | | $C_B$ = 2.2µF, HP,<br>Fast Turn-On Mode | 15 | | ms |

## Electrical Characteristics 5.0V (Notes 2, 7)

The following specifications apply for $V_{DD}$ = $LSV_{DD}$ = 5.0V, $A_V$ = 0dB, Loudspeaker $R_L$ = 15µH+8Ω+15µH (Note 8), Earpiece $R_L$ = 8Ω, f = 1kHz, unless otherwise specified. Limits apply for $T_A$ = 25C. LS = Loudspeaker, HP = Headphone, EP = Earpiece.

| Symbol | Parameter | Conditions | LM49150 | | Units (Limits) |
|---|---|---|---|---|---|
| | | | Typical (Note 6) | Limits (Note 7) | |
| $I_{DD}$ | Supply Current | $V_{IN}$ = 0, No Load | | | |
| | | LS mode 1 | 4.5 | | mA |
| | | HP mode 8 | 4.9 | | mA |
| | | EP Bypass Mode | 0.9 | | mA |
| | | LS + HP Mode 5 and Mode 10 | 7.7 | | mA |
| | | LS Mode 1, GAMP_SD = 1 | 3.7 | | mA |
| | | HP Mode 8, GAMP_SD = 1 | 4.4 | | mA |
| $I_{SD}$ | Shutdown Current | | 0.02 | 1 | µA (max) |
| $V_{OS}$ | Output Offset Voltage | $V_{IN}$ = 0V, LS, $R_L$ = 8Ω<br>LS Gain = 6dB, Stereo Mode 10 | 9 | 40 | mV (max) |
| | | $V_{IN}$ = 0V, HP, $R_L$ = 32Ω<br>Ground Reference, Stereo Mode 10 | 1 | 5 | mV (max) |
| | | $V_{IN}$ = 0V, EP Bypass only, $R_L$ = 8Ω | 1 | 5 | mV (max) |
| $P_O$ | Output Power | LS Mode 1, THD+N = 1%, f = 1kHz<br>LS Gain = 6dB, $R_L$ = 4Ω | 2.1 | | W |
| | | LS Mode 1, THD+N = 1%, f = 1kHz<br>LS Gain = 6dB, $R_L$ = 8Ω | 1.25 | | W |
| | | HP Mode 8, THD+N = 1%, f = 1kHz<br>HP Attenuation = 0dB, $R_L$ = 16Ω | 42 | | mW |
| | | HP Mode 8, THD+N = 1%, f = 1kHz<br>HP Attenuation = 0dB, $R_L$ = 32Ω | 42 | | mW |
| | | EP Bypass Only, THD+N = 1%<br>f = 1kHz, $R_L$ = 8Ω | 135 | | mW |
| THD+N | Total Harmonic Distortion + Noise | LS Mode 1, f = 1kHz<br>$P_{OUT}$ = 600mW; $R_L$ = 8Ω | 0.015 | | % |
| | | HP Mode 8, f = 1kHz<br>$P_{OUT}$ = 20mW; $R_L$ = 32Ω | 0.01 | | % |
| | | EP Bypass only, f = 1kHz,<br>$P_{OUT}$ = 60mW; $R_L$ = 8Ω | 0.08 | | % |
| η | Efficiency | LS Output | 88 | | % |
| $\in_{OUT}$ | Output Noise | A-weighted,<br>inputs terminated to AC GND, Output referred | | | |
| | | EP Bypass | 10 | | µV |
| | | LS; Mode 1 | 40 | | µV |
| | | LS; Mode 2 | 47 | | µV |
| | | LS; Mode 3 | 48 | | µV |
| | | HP; Mode 4 | 9 | | µV |
| | | HP; Mode 8 | 10 | | µV |
| | | HP; Mode 12 | 11 | | µV |

| Symbol | Parameter | Conditions | LM49150 | | Units (Limits) |
|---|---|---|---|---|---|
| | | | Typical (Note 6) | Limits (Note 7) | |
| PSRR | Power Supply Rejection Ratio | $V_{RIPPLE}$ = 200m$V_{PP}$; f = 217Hz, $R_L$ = 8Ω, $C_B$ = 2.2µF, All audio inputs terminated to AC GND; output referred | | | |
| | | EP Bypass | 97 | | dB |
| | | Loudspeaker Output; LS Gain = 6dB | | | |
| | | LS; Mode 1 | 75 | | dB |
| | | LS; Mode 2 | 71 | | dB |
| | | LS; Mode 3 | 71 | | dB |
| | | Headphone Output, HP Attenuation = 0dB | | | |
| | | HP; Mode 4 | 91 | | dB |
| | | HP; Mode 8 | 80 | | dB |
| | | HP; Mode 12 | 79 | | dB |
| | Volume Control Step Size Error | | ±0.2 | | dB |
| | Digital Volume Control Range | Maximum Attenuation | -92 | | dB |
| | | Volume Step 2 | -46.5 | -49<br>-44 | dB (min)<br>dB (max) |
| | | Maximum Gain | 18 | 17<br>19 | dB (min)<br>dB (max) |
| $A_M$ | Mute Attenuation | HP | 98 | | dB |
| | | LS | 98 | | dB |
| $Z_{IN}$ | Mono Channel Input Impedance<br>$L_{IN}$ and $R_{IN}$ Input Impedance | Maximum gain setting | 12 | | kΩ |
| | | Maximum attenuation setting | 111 | | kΩ |
| | EP Bypass Resistance | | 62 | 50<br>80 | kΩ (min)<br>kΩ (max) |
| CMRR | Common-Mode Rejection Ratio | f = 217Hz, $V_{CM}$ = 1$V_{P-P}$ , $R_L$ = 8Ω<br>EP Bypass | 55 | | dB |
| | | f = 217Hz, $V_{CM}$ = 1$V_{P-P}$, $R_L$ = 8Ω<br>LS, Mode 1 | 55 | | dB |
| | | f = 217Hz, $V_{CM}$ = 1$V_{P-P}$, $R_L$ = 32Ω<br>HP, Mode 4 | 61 | | dB |
| $X_{TALK}$ | Crosstalk | HP mode 8; $P_O$ = 12mW<br>$R_L$ = 32Ω, f = 1kHz | 78 | | dB |
| $T_{ON}$ | Turn-On Time | $C_B$ = 2.2µF, HP,<br>Normal Turn-On Mode | 27 | | ms |
| | | $C_B$ = 2.2µF, HP,<br>Fast Turn-On Mode | 15 | | ms |

## I²C micro (Note 2)

The following specifications apply for $V_{DD}$ = 5.0V and 3.3V, $T_A$ = 25°C, 2.2V ≤ I²C_$V_{DD}$ ≤ 5.5V, unless otherwise specified.

| Symbol | Parameter | Conditions | LM49150 | | Units (Limits) |
|---|---|---|---|---|---|
| | | | Typical (Note 4) | Limits (Notes 7, 5) | |
| $t_1$ | I²C Clock Period | | | 2.5 | µs (min) |
| $t_2$ | I²C Data Setup Time | | | 100 | ns (min) |
| $t_3$ | I²C Data Stable Time | | | 0 | ns (min) |
| $t_4$ | Start Condition Time | | | 100 | ns (min) |
| $t_5$ | Stop Condition Time | | | 100 | ns (min) |
| $t_6$ | I²C Data Hold Time | | | 100 | ns (min) |
| $V_{IH}$ | I²C Input Voltage High | | | 0.7xI²C$V_{DD}$ | V (min) |
| $V_{IL}$ | I²C Input Voltage Low | | | 0.3xI²C$V_{DD}$ | V (max) |

## I²C micro (Note 2)

The following specifications apply for $V_{DD}$ = 5.0V and 3.3V, $T_A$ = 25°C, 1.7V ≤ I²C_$V_{DD}$ ≤ 2.2V, unless otherwise specified.

| Symbol | Parameter | Conditions | LM49150 | | Units (Limits) |
|---|---|---|---|---|---|
| | | | Typical (Note 6) | Limits (Note 7) | |
| $t_1$ | I²C Clock Period | | | 2.5 | µs (min) |
| $t_2$ | I²C Data Setup Time | | | 250 | ns (min) |
| $t_3$ | I²C Data Stable Time | | | 0 | ns (min) |
| $t_4$ | Start Condition Time | | | 250 | ns (min) |
| $t_5$ | Stop Condition Time | | | 250 | ns (min) |
| $t_6$ | I²C Data Hold Time | | | 250 | ns (min) |
| $V_{IH}$ | I²C Input Voltage High | | | 0.7xI²C$V_{DD}$ | V (min) |
| $V_{IL}$ | I²C Input Voltage Low | | | 0.3xI²C$V_{DD}$ | V (max) |

**Note 1:** *"Absolute Maximum Ratings"* indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the *Absolute Maximum Ratings* or other conditions beyond those indicated in the *Recommended Operating Conditions* is not implied. The *Recommended Operating Conditions* indicate conditions at which the device is functional and the device should not be operated beyond such conditions. All voltages are measured with respect to the ground pin, unless otherwise specified

**Note 2:** The *Electrical Characteristics* tables list guaranteed specifications under the listed *Recommended Operating Conditions* except as otherwise modified or specified by the *Electrical Characteristics Conditions* and/or Notes. Typical specifications are estimations only and are not guaranteed.

**Note 3:** The maximum power dissipation must be derated at elevated temperatures and is dictated by $T_{JMAX}$, $\theta_{JA}$, and the ambient temperature, $T_A$. The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX} - T_A) / \theta_{JA}$ or the number given in *Absolute Maximum Ratings*, whichever

**Note 4:** Human body model, applicable std. JESD22-A114C.

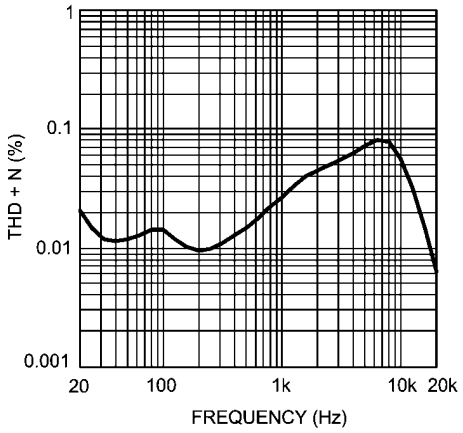
**Note 5:** Machine model, applicable std. JESD22-A115-A.

**Note 6:** Typical values represent most likely parametric norms at $T_A$ = +25ºC, and at the *Recommended Operation Conditions* at the time of product characterization and are not guaranteed.

**Note 7:** Datasheet min/max specification limits are guaranteed by test or statistical analysis.

## Typical Performance Characteristics

**THD+N vs Frequency**
**$V_{DD}$ = 3.3V, $R_L$ = 8Ω, $P_{OUT}$ = 250mW**
**Speaker Mode 1**

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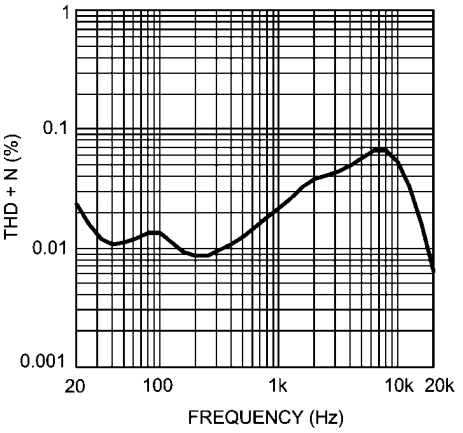
**THD+N vs Frequency**
**$V_{DD}$ = 3.6V, $R_L$ = 8Ω, $P_{OUT}$ = 300mW**
**Speaker Mode 1**

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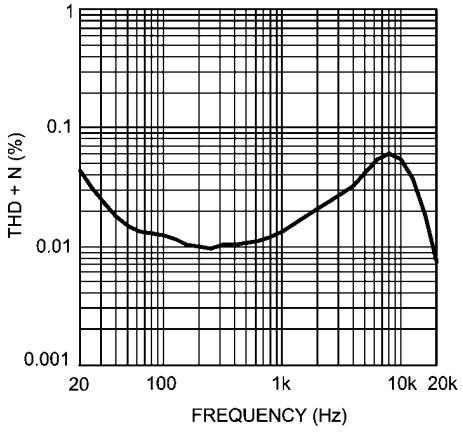
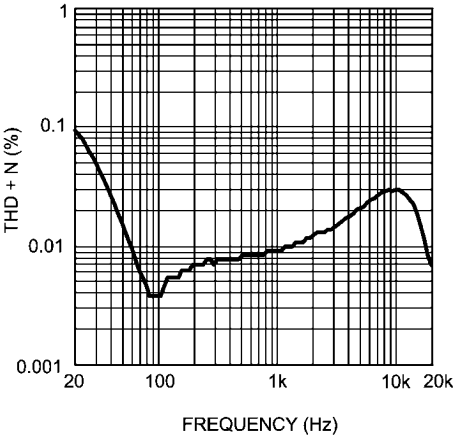
**THD+N vs Frequency**
**$V_{DD}$ = 5V, $R_L$ = 8Ω, $P_{OUT}$ = 600mW**
**Speaker Mode 1**




300446p2

**THD+N vs Frequency**
**$V_{DD}$ = 3.3V, $R_L$ = 32Ω, $P_{OUT}$ = 20mW**
**Headphone Mode 8**

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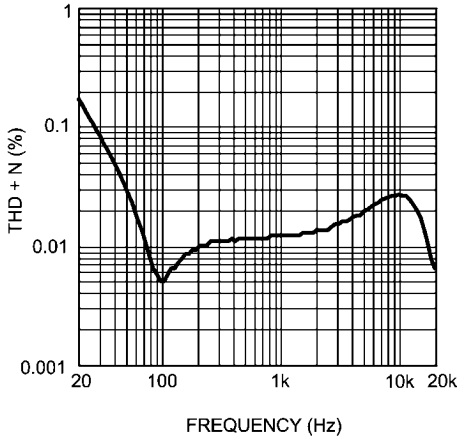
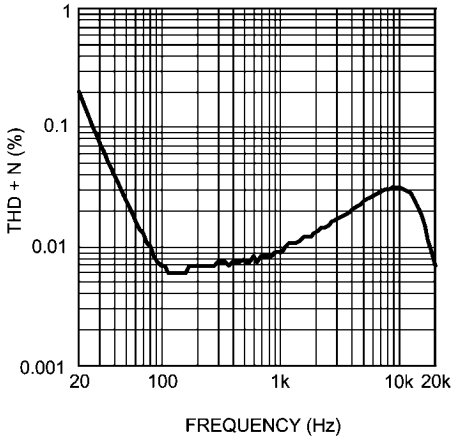
**THD+N vs Frequency**
**$V_{DD}$ = 3.6V, $R_L$ = 8Ω, $P_{OUT}$ = 20mW**
**Headphone Mode**




300446q3

**THD+N vs Frequency**
**$V_{DD}$ = 5V, $R_L$ = 32Ω, $P_{OUT}$ = 20mW**
**Headphone Mode 8**

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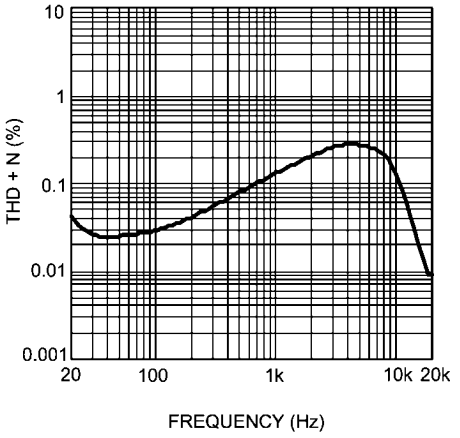
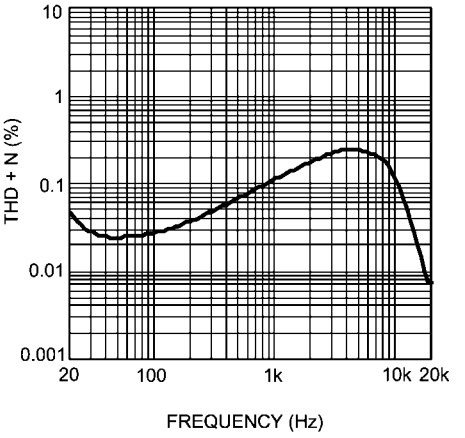
**THD+N vs Frequency**
**$V_{DD}$ = 3.3V, $R_L$ = 8Ω, $P_{OUT}$ = 20mW**
**Earpiece Bypass Mode**



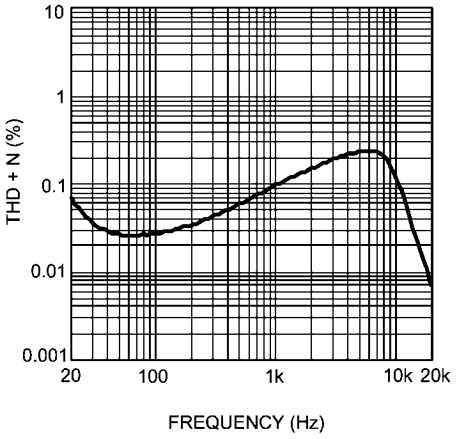

300446o4

**THD+N vs Frequency**
**$V_{DD}$ = 3.6V, $R_L$ = 8Ω, $P_{OUT}$ = 30mW**
**Earpiece Bypass Mode**



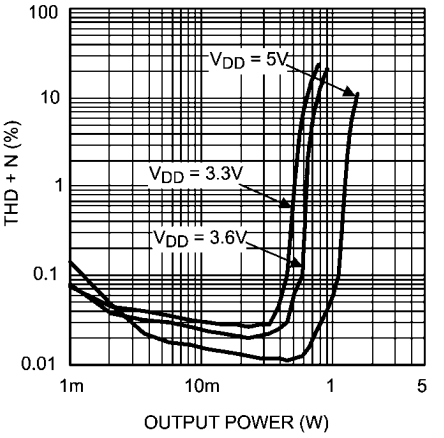

300446o5

**THD+N vs Frequency**
**$V_{DD}$ = 5V, $R_L$ = 8Ω, $P_{OUT}$ = 60mW**
**Earpiece Bypass Mode**



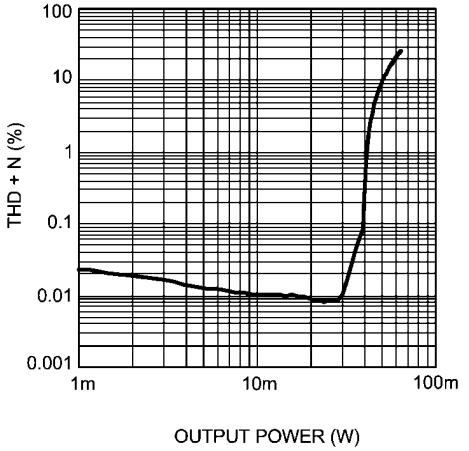

300446o6

**THD+N vs Output Power**
**$R_L$ = 8Ω, f = 1kHz**
**Speaker Mode 1**



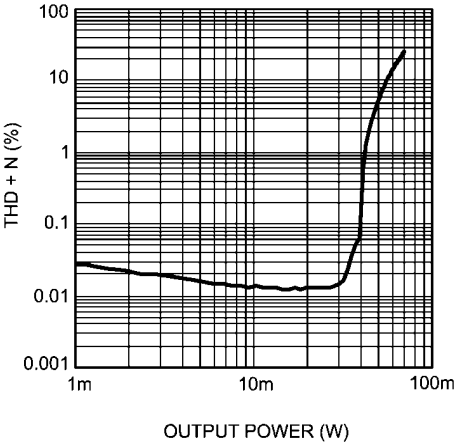

300446p7

**THD+N vs Output Power**
**$V_{DD}$ = 3.3V, $R_L$ = 32Ω, f = 1kHz**
**Headphone Mode 8**



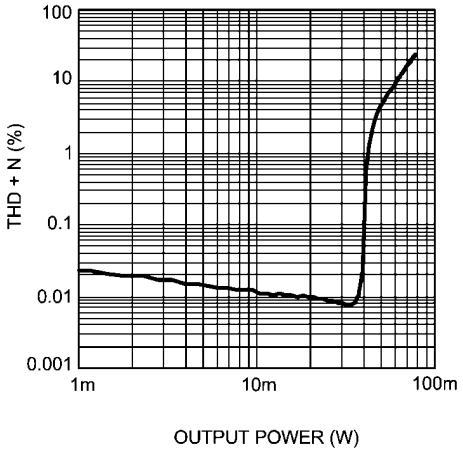

300446p4

**THD+N vs Output Power**
**$V_{DD}$ = 3.6V, $R_L$ = 32Ω, f = 1kHz**
**Headphone Mode 8**



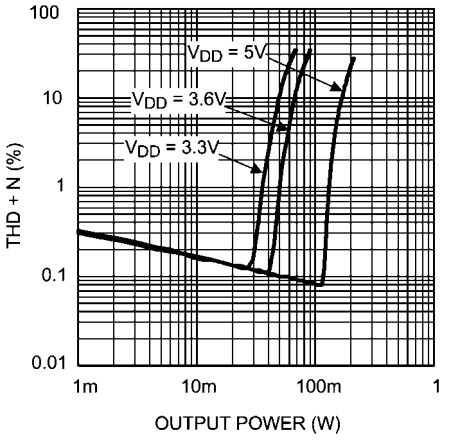

300446p5

**THD+N vs Output Power**
**$V_{DD}$ = 5V, $R_L$ = 32Ω, f = 1kHz**
**Headphone Mode 8**



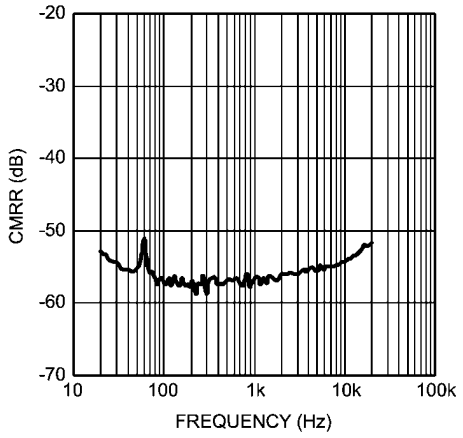

300446p6

**THD+N vs Output Power**
**$R_L$ = 8Ω, f = 1kHz**
**Earpiece Bypass Mode**



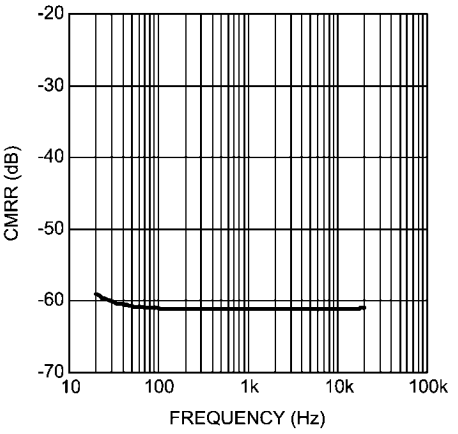

300446p3

**CMRR vs Frequency**
**$V_{DD}$ = 3.3V, $V_{CM}$ = 1$V_{P-P}$ $R_L$ = 8Ω**
**Loudspeaker Mode 1**



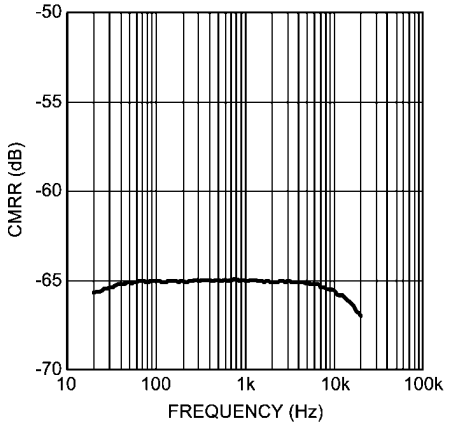

300446t2

**CMRR vs Frequency**
**$V_{DD}$ = 3.3V, $V_{CM}$ = 1$V_{P-P}$ $R_L$ = 32Ω**
**Headphone Mode 4**



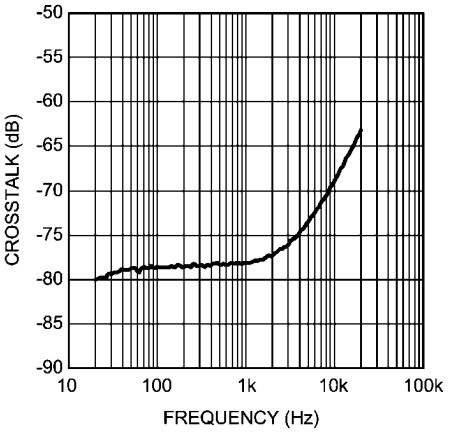

300446t3

**CMRR vs Frequency**
**$V_{DD}$ = 3.3V, $V_{CM}$ = 1$V_{P-P}$ $R_L$ = 8Ω**
**Earpiece Bypass Mode**



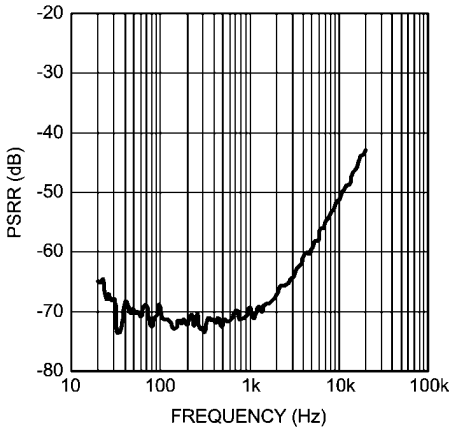

300446r8

**Crosstalk vs Frequency**
**$V_{DD}$ = 3.3V, $V_{CM}$ = 1$V_{P-P}$ $R_L$ = 32Ω**
**Headphone Mode 8**



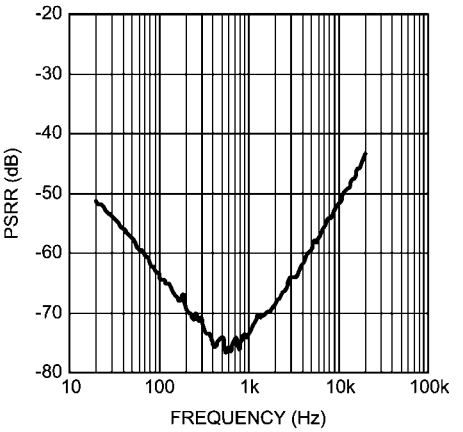

300446r9

**PSRR vs Frequency**
**$V_{DD}$ = 3.3V, $V_{RIPPLE}$ = 200m$V_{P-P}$ $R_L$ = 8Ω**
**Loudspeaker Mode 1**



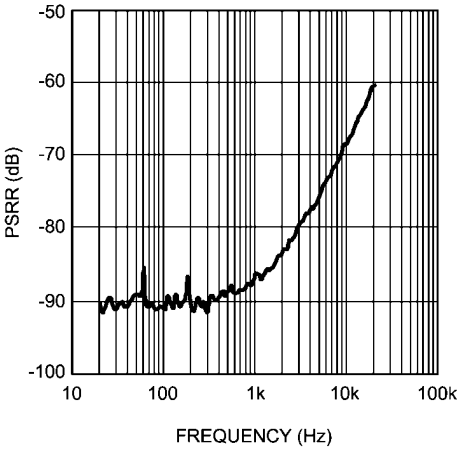

300446t0

**PSRR vs Frequency**
**$V_{DD}$ = 3.3V, $V_{RIPPLE}$ = 200$V_{P-P}$ $R_L$ = 8Ω**
**Loudspeaker Mode 2**



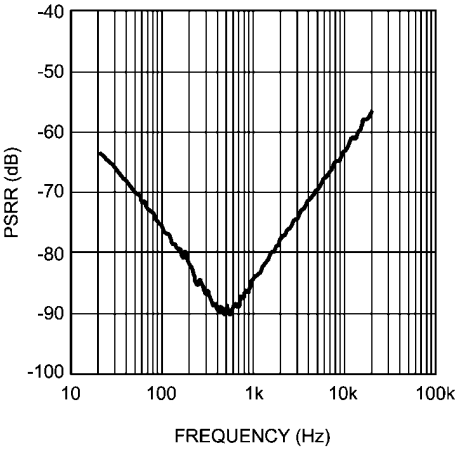

300446t1

**PSRR vs Frequency**
**$V_{DD}$ = 3.3V, $V_{RIPPLE}$ = 200$V_{P-P}$ $R_L$ = 32Ω**
**Headphone Mode 4**



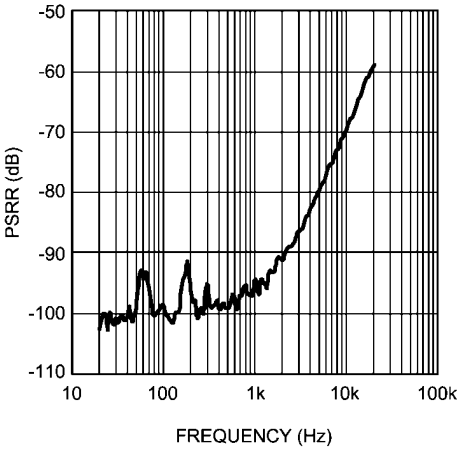

300446r3

**PSRR vs Frequency**
**$V_{DD}$ = 3.3V, $V_{RIPPLE}$ = 200$V_{P-P}$ $R_L$ = 32Ω**
**Headphone Mode 8**



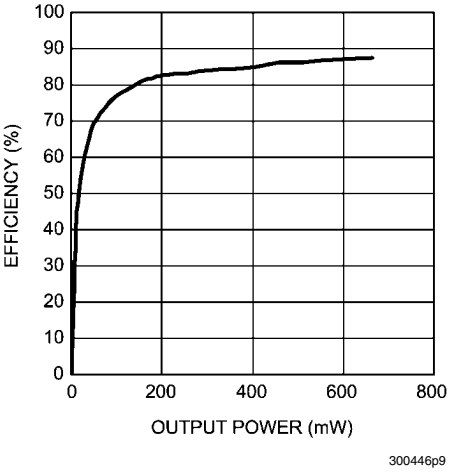

300446r4

**PSRR vs Frequency**
**$V_{DD}$ = 3.3V, $V_{RIPPLE}$ = 200$V_{P-P}$ $R_L$ = 8Ω**
**Earpiece Bypass Mode**



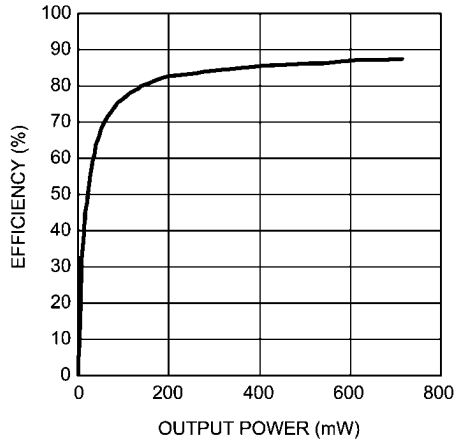

300446r5

**Efficiency vs Output Power**
**$V_{DD}$ = 3.3V, $R_L$ = 8Ω, f = 1kHz**
**Speaker Mode 1**



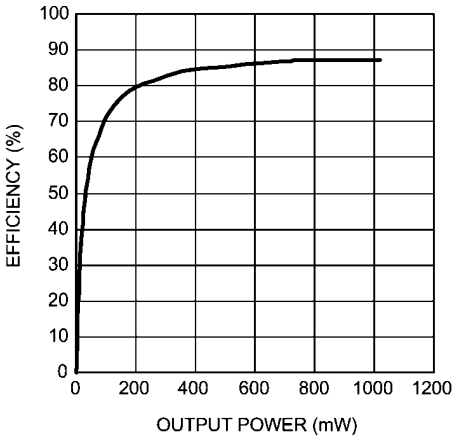

300446p9

**Efficiency vs Output Power**
**$V_{DD}$ = 3.6V, $R_L$ = 8Ω, f = 1kHz**
**Speaker Mode 1**



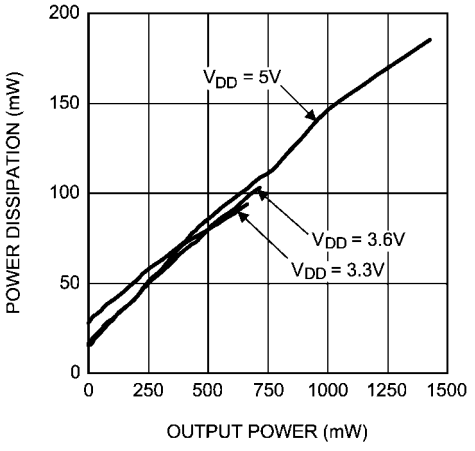

300446q0

**Efficiency vs Output Power**
**$V_{DD}$ = 5V, $R_L$ = 8Ω, f = 1kHz**
**Speaker Mode 1**



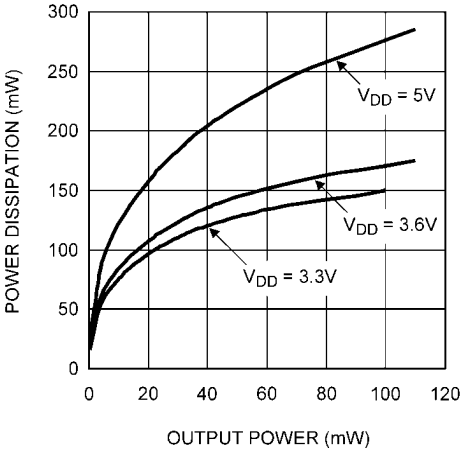

300446q1

**Power Dissipation vs Output Power**
**$R_L$ = 8Ω, f = 1kHz**
**Speaker Mode 1**



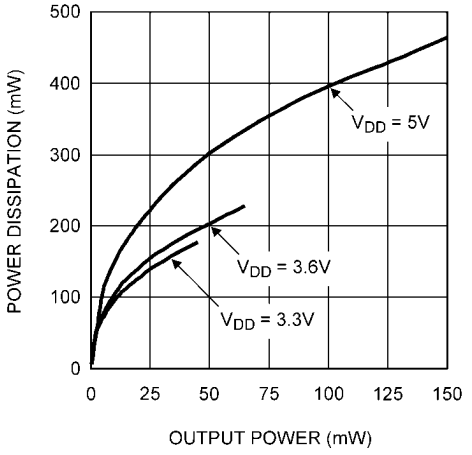

300446p8

**Power Dissipation vs Output Power**
**$R_L$ = 32Ω, f = 1kHz**
**Headphone Mode 8**



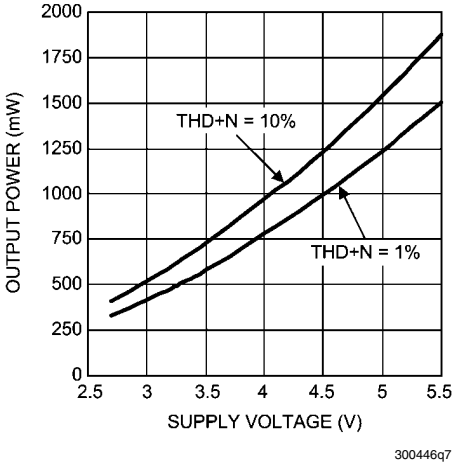

300446o1

**Power Dissipation vs Output Power**
**$R_L$ = 8Ω, f = 1kHz**
**Earpiece Bypass Mode**



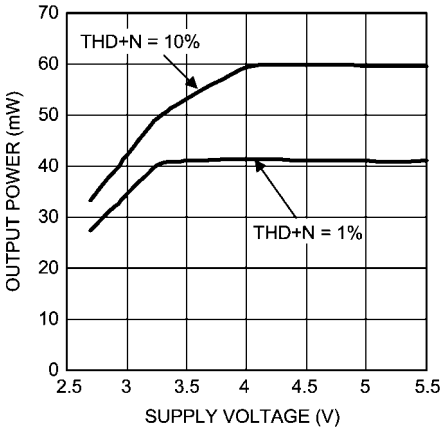

300446o0

**Output Power vs Supply Voltage**
**$R_L$ = 8Ω, f = 1kHz**
**Speaker Mode 1**



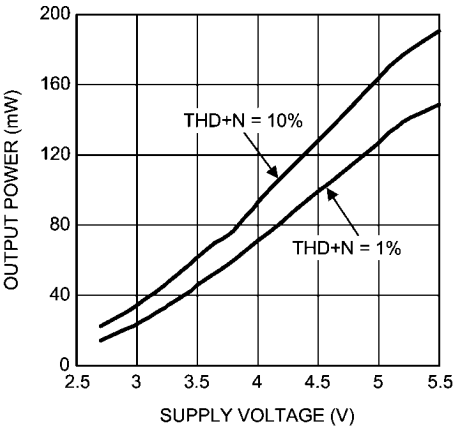

300446q7

**Output Power vs Supply Voltage**
**$R_L$ = 32Ω, f = 1kHz**
**Headphone Mode 8**



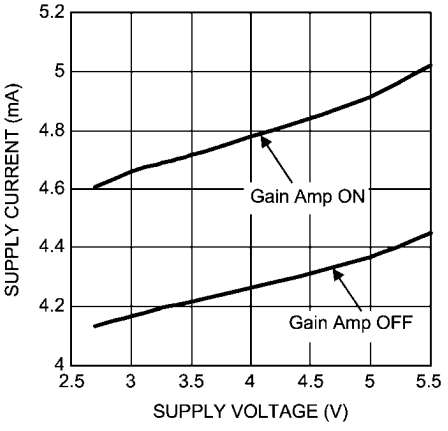

300446q6

**Output Power vs Supply Voltage**
**$R_L$ = 8Ω, f = 1kHz**
**Earpiece Bypass Mode**



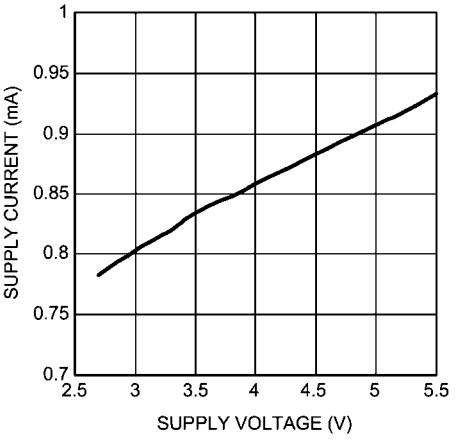

300446r0

**Supply Current vs Supply Voltage**
**Headphone Mode 1, No Load**




300446q8

**Supply Current vs Supply Voltage**
**Earpiece Bypass Mode, No Load**




300446q9

# Application Information

## I²C COMPATIBLE INTERFACE

The LM49150 is controlled through an I²C compatible serial interface that consists of a serial data line (SDA) and a serial clock (SCL). The clock line is uni-directional. The data line is bi-directional (open drain). The LM49150 and the master can communicate at clock rates up to 400kHz. Figure 2 shows the I²C interface timing diagram. Data on the SDA line must be stable during the HIGH period of SCL. The LM49150 is a transmit/receive slave-only device, reliant upon the master to generate the SCL signal. Each transmission sequence is framed by a START condition and a STOP condition (Figure 3). Each data word, device address and data, transmitted over the bus is 8 bits long and is always followed by an acknowledge pulse (Figure 4). The LM49150 device address is 11111000.

## I²C INTERFACE POWER SUPPLY PIN (I²C$V_{DD}$)

The LM49150's I²C interface is powered up through the I²C$V_{DD}$ pin. The LM49150's I²C interface operates at a voltage level set by the I²C$V_{DD}$ pin which can be set independent to that of the main power supply pin $V_{DD}$. This is ideal whenever logic levels for the I²C interface are dictated by a microcontroller or microprocessor that is operating at a lower supply voltage than the main battery of a portable system.

## I²C BUS FORMAT

The I²C bus format is shown in Figure 4. The START signal, the transition of SDA from HIGH to LOW while SCL is HIGH, is generated, alerting all devices on the bus that a device address is being written to the bus.

The 7-bit device address is written to the bus, most significant bit (MSB) first, followed by the R/$\overline{W}$ bit. R/$\overline{W}$ = 0 indicates the master is writing to the slave device, R/$\overline{W}$ = 1 indicates the master wants to read data from the slave device. Set R/$\overline{W}$ = 0; the LM49150 is a WRITE-ONLY device and will not respond to the R/$\overline{W}$ = 1. The data is latched in on the rising edge of the clock. Each address bit must be stable while SCL is HIGH. After the last address bit is transmitted, the master device releases SDA, during which time, an acknowledge clock pulse is generated by the slave device. If the LM49150 receives the correct address, the device pulls the SDA line low, generating an acknowledge bit (ACK).

Once the master device registers the ACK bit, the 8-bit register data word is sent. Each data bit should be stable while SCL is HIGH. After the 8-bit register data word is sent, the LM49150 sends another ACK bit. Following the acknowledgement of the register data word, the master issues a STOP bit, allowing SDA to go high while SCL is high.

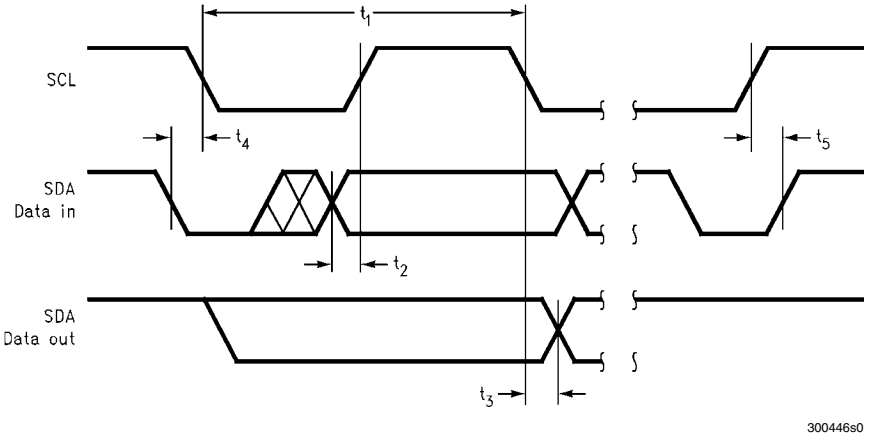



**FIGURE 2. I²C Timing Diagram**

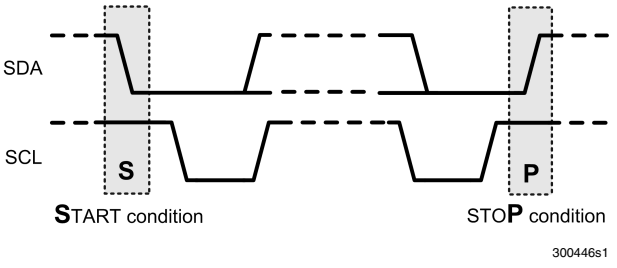



**FIGURE 3. Start and Stop Diagram**

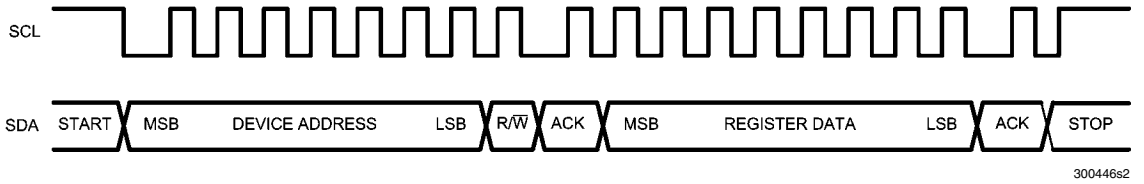



**FIGURE 4. Start and Stop Diagram**

**TABLE 1. Chip Address**

| | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 (R/$\overline{W}$) |
|---|---|---|---|---|---|---|---|---|
| Chip Address | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 |

**TABLE 2. Control Registers**

| | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
|---|---|---|---|---|---|---|---|---|
| Shutdown Control | 0 | 0 | Spread Spectrum | GAMP_SD | 0 | $I^2CV_{DD}$_SD | Turn_On _Time | PWR_On |
| Output Mode Control | 0 | 1 | EP Bypass | HPR_SD | MC3 (HP L&R) | MC2 (HP Mono) | MC1 (LS L&R) | MC0 (LS Mono) |
| Output Gain Control | 1 | 0 | 0 | INPUT_MUTE | LS_GAIN | HP_GAIN2 | HP_GAIN1 | HP_GAIN0 |
| Mono Input Volume Control | 1 | 0 | 1 | MG4 | MG3 | MG2 | MG1 | MG0 |
| Left Input Volume Control | 1 | 1 | 0 | LG4 | LG3 | LG2 | LG1 | LG0 |
| Right Input Volume Control | 1 | 1 | 1 | RG4 | RG3 | RG2 | RG1 | RG0 |

**TABLE 3. Shutdown Control Register**

| Bit | Name | Value | Description |
|---|---|---|---|
| B5 | Spread Spectrum | 0 | Spread Spectrum Disabled |
| | | 1 | Spread Spectrum Enabled |
| B4 | GAMP_SD | 0 | Normal Operation |
| | | 1 | Disables the gain amplifiers that are not in use, to minimize $I_{DD}$. Recommended for Output Modes 1, 2, 4, 5, 8, 10 |
| B3 | | 0 | |
| B2 | $I^2CV_{DD}$_SD | 0 | $I^2CV_{DD}$ acts as an active low RESET input. If $I^2CV_{DD}$ drops below 1.1V, the device resets and the $I^2C$ registers are restored to their default state. |
| | | 1 | Normal Operation. $I^2CV_{DD}$ voltage does not reset the device. |
| B1 | Turn_On_Time | 0 | Normal Turn-On Time (27ms) |
| | | 1 | Fast Turn-On Time (15ms) |
| B0 | PWR_On | 0 | Device Disabled |
| | | 1 | Device Enabled |

**TABLE 4. Output Mode Control Register**

| Bit | Name | Value | Description |
|---|---|---|---|
| B5 | EP Bypass | 0 | Normal Output Mode Operation |
| | | 1 | Speaker and Headphone amplifier goes into shutdown mode and enables Receiver Bypass path |
| B4 | HPR_SD | 0 | Normal Operation |
| | | 1 | Disables Right Headphone Output |

**TABLE 5. Output Mode Selection (see legend below)**

| Output Mode Number | MC3 | MC2 | MC1 | MC0 | LS Output | HP R Output | HP L Output |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | SD | SD | SD |
| 1 | 0 | 0 | 0 | 1 | $G_P$ x M | SD | SD |
| 2 | 0 | 0 | 1 | 0 | 2 x ($G_L$ x L + $G_R$ x R) | SD | SD |
| 3 | 0 | 0 | 1 | 1 | 2 x ($G_L$ x L + $G_R$ x R) + $G_P$ x M | SD | SD |
| 4 | 0 | 1 | 0 | 0 | SD | $G_P$ x M/2 | $G_P$ x M/2 |
| 5 | 0 | 1 | 0 | 1 | $G_P$ x M | $G_P$ x M/2 | $G_P$ x M/2 |
| 6 | 0 | 1 | 1 | 0 | 2 x ($G_L$ x L + $G_R$ x R) | $G_P$ x M/2 | $G_P$ x M/2 |
| 7 | 0 | 1 | 1 | 1 | 2 x ($G_L$ x L + $G_R$ x R) + $G_P$ x M | $G_P$ x M/2 | $G_P$ x M/2 |
| 8 | 1 | 0 | 0 | 0 | SD | $G_R$ x R | $G_L$ x L |
| 9 | 1 | 0 | 0 | 1 | $G_P$ x M | $G_R$ x R | $G_L$ x L |
| 10 | 1 | 0 | 1 | 0 | 2 x ($G_L$ x L + $G_R$ x R) | $G_R$ x R | $G_L$ x L |
| 11 | 1 | 0 | 1 | 1 | 2 x ($G_L$ x L + $G_R$ x R) + $G_P$ x M | $G_R$ x R | $G_L$ x L |
| 12 | 1 | 1 | 0 | 0 | SD | $G_R$ x R + $G_P$ x M/2 | $G_L$ x L + $G_P$ x M/2 |
| 13 | 1 | 1 | 0 | 1 | $G_P$ x M | $G_R$ x R + $G_P$ x M/2 | $G_L$ x L + $G_P$ x M/2 |
| 14 | 1 | 1 | 1 | 0 | 2 x ($G_L$ x L + $G_R$ x R) | $G_R$ x R + $G_P$ x M/2 | $G_L$ x L + $G_P$ x M/2 |
| 15 | 1 | 1 | 1 | 1 | 2 x ($G_L$ x L + $G_R$ x R) + $G_P$ x M | $G_R$ x R + $G_P$ x M/2 | $G_L$ x L + $G_P$ x M/2 |

MC3: HP Select L and R In
MC2: HP Select Mono In
MC1: Loud Speaker Select L and R In
MC0: Loud Speaker Select Mono In
M : Phone In (Mono)
R: Right In
L: Left In
SD: Shutdown
$G_P$: Phone In (Mono) Volume Control Gain
$G_R$: Right Stereo Volume Control Gain
$G_L$: Left Stereo Volume Control Gain

| MC1 | MC0 | LSOUT |
|---|---|---|
| 0 | 0 | SD |
| 0 | 1 | M |
| 1 | 0 | L+R |
| 1 | 1 | M+L+R |

| MC3 | MC2 | HPR Output | HPL Output |
|---|---|---|---|
| 0 | 0 | SD | SD |
| 0 | 1 | M | M |
| 1 | 0 | L | R |
| 1 | 1 | M+L | M+R |

**TABLE 6. Output Gain Control (Loudspeaker)**

| Bit | Value | Gain (dB) |
|---|---|---|
| LS_GAIN | 0 | +6 |
| | 1 | +12 |

**TABLE 7. Headphone Output Gain Setting**

| HP_Gain2 | HP_Gain1 | HP_Gain0 | Gain (dB) |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | –1.2 |
| 0 | 1 | 0 | –2.5 |
| 0 | 1 | 1 | –4.0 |
| 1 | 0 | 0 | –6.0 |
| 1 | 0 | 1 | –8.5 |
| 1 | 1 | 0 | –12 |
| 1 | 1 | 1 | –18 |

**TABLE 8. Volume Control Table**

| Volume Step | (1) xG4 | xG3 | xG2 | xG1 | xG0 | (2) Gain (dB) |
|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 0 | 0 | 0 | –80.00 |
| 2 | 0 | 0 | 0 | 0 | 1 | –46.50 |
| 3 | 0 | 0 | 0 | 1 | 0 | –40.50 |
| 4 | 0 | 0 | 0 | 1 | 1 | –34.50 |
| 5 | 0 | 0 | 1 | 0 | 0 | –30.00 |
| 6 | 0 | 0 | 1 | 0 | 1 | –27.00 |
| 7 | 0 | 0 | 1 | 1 | 0 | –24.00 |
| 8 | 0 | 0 | 1 | 1 | 1 | –21.00 |
| 9 | 0 | 1 | 0 | 0 | 0 | –18.00 |
| 10 | 0 | 1 | 0 | 0 | 1 | –15.00 |
| 11 | 0 | 1 | 0 | 1 | 0 | –13.50 |
| 12 | 0 | 1 | 0 | 1 | 1 | –12.00 |
| 13 | 0 | 1 | 1 | 0 | 0 | –10.50 |
| 14 | 0 | 1 | 1 | 0 | 1 | –9.00 |
| 15 | 0 | 1 | 1 | 1 | 0 | –7.50 |
| 16 | 0 | 1 | 1 | 1 | 1 | –6.00 |
| 17 | 1 | 0 | 0 | 0 | 0 | –4.50 |
| 18 | 1 | 0 | 0 | 0 | 1 | –3.00 |
| 19 | 1 | 0 | 0 | 1 | 0 | –1.50 |
| 20 | 1 | 0 | 0 | 1 | 1 | 0.00 |
| 21 | 1 | 0 | 1 | 0 | 0 | 1.50 |
| 22 | 1 | 0 | 1 | 0 | 1 | 3.00 |
| 23 | 1 | 0 | 1 | 1 | 0 | 4.50 |
| 24 | 1 | 0 | 1 | 1 | 1 | 6.00 |
| 25 | 1 | 1 | 0 | 0 | 0 | 7.50 |
| 26 | 1 | 1 | 0 | 0 | 1 | 9.00 |
| 27 | 1 | 1 | 0 | 1 | 0 | 10.50 |
| 28 | 1 | 1 | 0 | 1 | 1 | 12.00 |
| 29 | 1 | 1 | 1 | 0 | 0 | 13.50 |
| 30 | 1 | 1 | 1 | 0 | 1 | 15.00 |
| 31 | 1 | 1 | 1 | 1 | 0 | 16.50 |
| 32 | 1 | 1 | 1 | 1 | 1 | 18.00 |

(1.) x = M, L and R
(2.) Gain / Attenuation is from input to output

## SHUTDOWN FUNCTION

The LM49150 features the following shutdown controls.

Bit B4 (GAMP_SD) of the SHUTDOWN CONTROL register controls the gain amplifiers. When GAMP_SD = 1, it disables the gain amplifiers that are not in use. For example, in Modes 1, 4 and 5, the Mono inputs are in use, so the Left and Right input gain amplifiers are disabled, causing the $I_{DD}$ to be minimized.

Bit B0 (PWR_On) of the SHUTDOWN CONTROL register is the global shutdown control for the entire device. Set PWR_On = 0 for normal operation. PWR_On = 1 overrides any other shutdown control bit.

## OUTPUT MODE CONTROL

In the LM49150 OUTPUT MODE CONTROL register (Table 4), Bit B5 (EP Bypass) controls the operation of the Earpiece Bypass path. If EP Bypass = 0, it would act under normal output mode operation set by bits B3, B2, B1, and B0. If EP Bypass = 1, it overrides the B3, B2, B1, and B0 Bits and enables the Receiver Bypass path, a class AB amplifier, to the speaker output.

Bit B4 (HPR_SD) of the OUPUT MODE CONTROL register controls the right headphone shutdown. If HPR_SD = 1, the right headphone output is disabled.

## DIFFERENTIAL AMPLIFIER EXPLANATION

The LM49150 features a differential input stage, which offers improved noise rejection compared to a single-ended input amplifier. Because a differential input amplifier amplifies the difference between the two input signals, any component common to both signals is cancelled. An additional benefit of the differential input structure is the possible elimination of the DC input blocking capacitors. Since the DC component is common to both inputs, and thus cancelled by the amplifier, the LM49150 can be used without input coupling capacitors when configured with a differential input signal.

## SINGLE-ENDED INPUT CONFIGURATION

The left and right stereo inputs of the LM49150 are configured for single-ended sources (see Figure 1).

## INPUT CAPACITOR SELECTION

Input capacitors may be required for some applications, or when the audio source is single-ended. Input capacitors block the DC component of the audio signal, eliminating any conflict between the DC component of the audio source and the bias voltage of the LM49150. The input capacitors create a high-pass filter with the input resistors $R_{IN}$. The -3dB point of the high-pass filter is found using Equation (1) below.

$$f = 1 / 2\pi R_{IN} C_{IN} \quad (Hz) \qquad (1)$$

Where the value of $R_{IN}$ is given in the Electrical Characteristics Table.

High-pass filtering the audio signal helps protect the speakers. When the LM49150 is using a single-ended source, power supply noise on the ground is seen as an input signal. Setting the high-pass filter point above the power supply noise frequencies, 217Hz in a GSM phone, for example, filters out the noise such that it is not amplified and heard on the output. Capacitors with a tolerance of 10% or better are recommended for impedance matching and improved CMRR and PSRR.

## INPUT MIXER/MULTIPLEXER

The LM49150 includes a comprehensive mixer multiplexer controlled through the I²C interface. The mixer/multiplexer allows any input combination to appear on any output of LM49150. Multiple input paths can be selected simultaneously. Under these conditions, the selected inputs are mixed together and output on the selected channel. Table 5 shows how the input signals are mixed together for each possible input selection.

## CLASS D AMPLIFIER

The LM49150 features a high-efficiency, filterless, class D amplifier, which features a filterless modulation scheme. When there is no input signal applied, the output switches between $V_{DD}$ and GND at a 50% duty cycle. Since the outputs of the LM49150 class D amplifier are differential and in phase, the result is zero net voltage across the speaker and no load current during the ideal state, thus conserving power. The switching frequency of each output is 300kHz.

When an input signal is applied, the duty cycle(pulse width) changes. For increasing output voltages, the duty cycle of one output increases while the duty cycle of the output decreases. For decreasing output voltages, the converse occurs. The difference between the two pulse widths yields the differential output voltage across the load.

## SPREAD SPECTRUM

The LM49150 features a filterless spread spectrum modulation scheme. The switching frequency varies by +/-30% about a 300kHz center frequency, reducing the wideband spectral content, reducing EMI emissions radiated by the speaker and associated cables and traces. When a fixed frequency class D exhibits large amounts of spectral energy at multiples of switching frequency, the spread spectrum architecture of the LM49150 spreads that energy over a larger bandwidth. The cycle-to-cycle variation of the switching period does not affect the audio reproduction, efficiency, or PSRR. To enable spread spectrum, set the spread spectrum bit, B5 = 1 of the SHUTDOWN CONTROL register (see Table 3).

## ENHANCED EMMISIONS SUPPRESSION (E²S)

The LM49150 features National's patented E²S system that reduces EMI, while maintaining high quality audio reproduction and efficiency. The LM49150 features Edge Rate Control (ERC) that greatly reduces the high frequency components of the output square waves by controlling the output rise and fall times, slowing the transitions to reduce RF emissions, while optimizing THD+N and efficiency performance.

## LDO GENERAL INFORMATION

The LM49150 has different supplies for each portion of the device, allowing for the optimum combination of headroom, power dissipation and noise immunity. The speaker amplifiers are powered from $LSV_{DD}$. The ground reference headphone amplifiers are powered from the internal LDO. The separate power supplies allow the loudspeaker amplifier to operate from a higher voltage for maximum headroom, while the headphone amplifiers operate from a lower voltage, improving power dissipation.

## GROUND REFERENCED HEADPHONE AMPLIFIER

The LM49150 features a low noise inverting charge pump that generates an internal negative supply voltage. This allows the headphone outputs to be biased about GND instead of a nominal DC voltage, like traditional headphone amplifiers. Because there is no DC component, the large DC blocking capacitors (typically 220µF) are not necessary. The coupling capacitors are replaced by two small ceramic charge pump capacitors, saving board space and cost. Eliminating the output coupling capacitors also improves low frequency response. In traditional headphone amplifiers, the headphone impedance and the output capacitor from a high-pass filter that not only blocks the DC component of the output, but also attenuates low frequencies, impacting the bass response. Because the LM49150 does not require the output coupling capacitors, the low frequency response of the device is not degraded by external components. In addition to eliminating the output coupling capacitors, the ground referenced output nearly doubles the available dynamic range of the LM49250 headphone amplifiers when compared to a traditional headphone amplifier operating from the same supply voltage.

## CHARGE PUMP CAPACITOR SELECTION

Use low ESR ceramic capacitors (less than 100mΩ) for optimum performance.

## CHARGE PUMP FLYING CAPACITOR (C1)

The flying capacitor (C1), see Figure 1, affects the load regulation and output impedance of the charge pump. A C1 value that is too low results in a loss of current drive, leading to a loss of amplifier headroom. A higher valued C1 improves load regulation and lowers charge pump output impedance to an extent. Above 2.2µF, the $R_{DS(ON)}$ of the charge pump switches and the ESR of C1 and Cs5 dominate the output impedance. A lower value capacitor can be used in systems with low maximum output power requirements.

## CHARGE PUMP HOLD CAPACITOR (Cs5)

The value and ESR of the hold capacitor (Cs5) directly affects the ripple on $CPV_{SS}$. Increasing the value of Cs5 reduces output ripple. Decreasing the ESR of Cs5 reduces both output ripple and charge pump output impedance. A lower value capacitor can be used in systems with low maximum output power requirements.

# LM49150 Demoboard Bill Of Materials

**TABLE 9. Bill Of Materials**

| Location | Qty | Description | Part Number | Manufacturer |
|---|---|---|---|---|
| CIN2, CIN1 | 2 | 0.22uF, 1206, 10V, X7R Ceramic Capacitor | GRM319R71C224KA01D | Murata |
| CS4, CS2 | 2 | 0.1uF, 0805, 10V, X7R Ceramic Capacitor | GRM219R71C104KA01D | Murata |
| CS7 | 1 | 1.0uF, 0805, 10V, X7R Ceramic Capacitor | GRM21BR71A105KA01L | Murata |
| CIN3, CIN4 | 2 | 1.0uF 1206, 10V, X7R Ceramic Capacitor | GRM319R71C105KAA3D | Murata |
| CS5, C1 | 2 | 2.2uF, 0603, 10V, X7R, Ceramic Capacitor | GRM188R71A225KE15D | Murata |
| CS1, CS3, CS6 | 3 | 2.2uF, Size A, Tantalum Capactior | 293D225X9010A2TE3 | Vishay |
| U2 | 1 | LM49150, 16 bump uSMD | LM49510 | NSC |
| R1, R2 | 2 | 5K ohm 1/10W 0.05% 0603 SMD | CRCW06035R1KJNEA | Vishay |
| J11, J12, J13, J14 | 4 | 3–Header | | |
| J1, J2, J3, J7, J8, J9, J10 | 7 | 2–Header | | |
| J6 | 1 | Header_3M 8516–4500PL | | |
| U1 | 1 | Headphone Jack | | |

## Layout Guidelines

Minimize trace impedance of the power, ground and all output traces for optimum performance. Voltage loss due to trace resistance between the LM49150 and the load results in decreased output power and efficiency. Trace resistance between the power supply and the GND of the LM49150 has the same effect as a poorly regulated supply, increased ripple and reduced peak output power. Use wide traces, for power-supply inputs and amplifier outputs to minimize losses due to trace resistance, as well as providing heat dissipation from the device. Proper grounding improves audio performance, minimizes crosstalk between channels and prevents switching noise from interfering with audio signal. Use of power and ground planes is recommended.

The following recommendations should be considered when laying out the different grounds of the LM49150. Refer to the Demo Board Schematic for the corresponding component designators. Bypass capacitors for $AV_{DD}$ (CS7), $LSV_{DD}$ (CS1, CS2), $V_{O(LDO)}$ (CS3, CS4) should be grounded to the GND pin via a ground plane. Bypass capacitor for $CPV_{SS}$(CS5) should be grounded via a wide trace or a ground plane to the CPGND pin. The headphone grounds should be connected to the GND via a separate trace also. This will help prevent noise from the charge pump from feeding into the power supplies and the output.

Place all digital components and digital signal traces as far as possible from analog components and traces. Do not run digital and analog traces in parallel on the same PCB layer.

# Demo Board Schematic

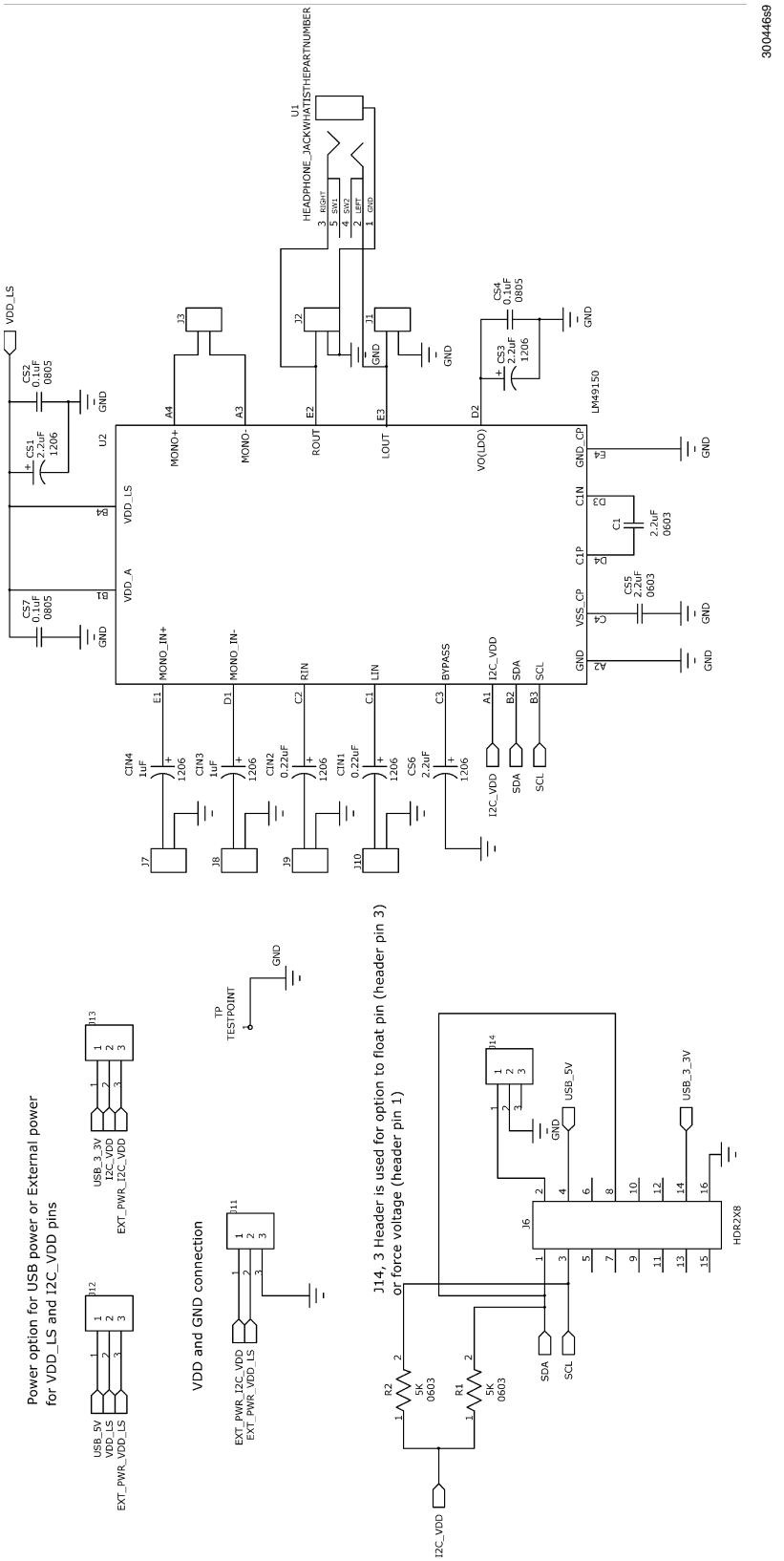
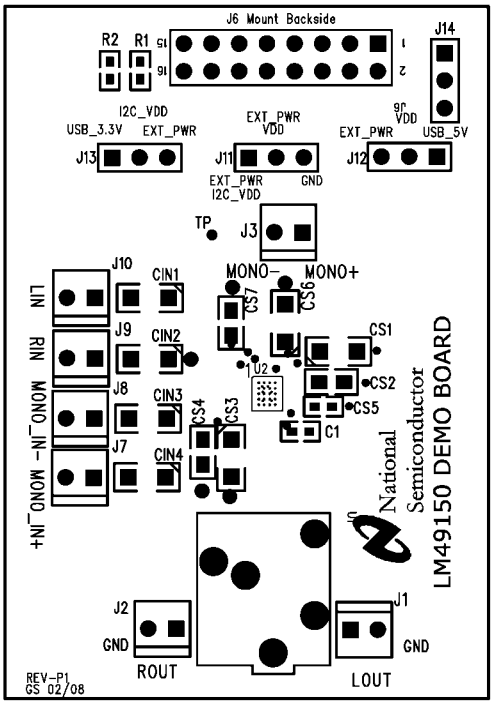


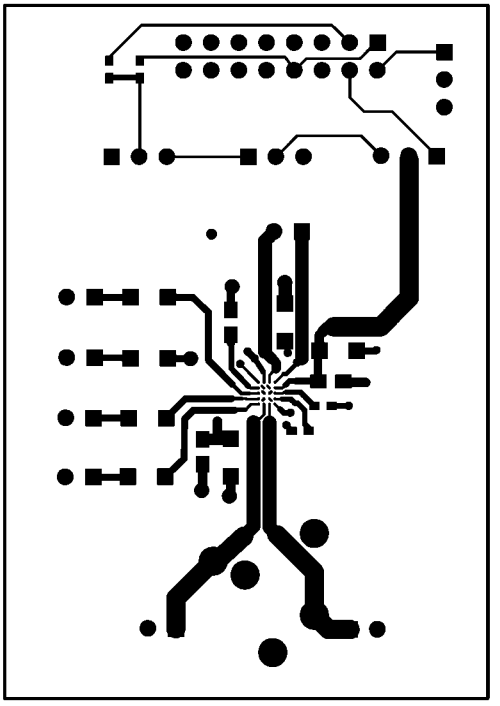

**FIGURE 5. LM49150 Demo Board Schematic**

## PC Board Layout



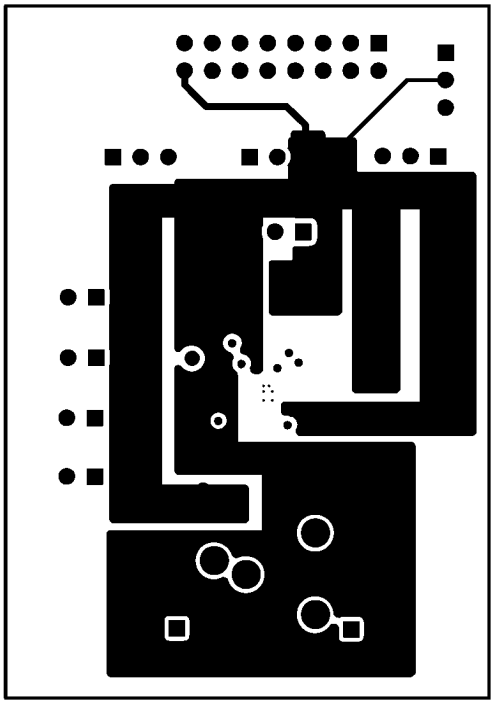

300446s8

**Top Silkscreen Layer**



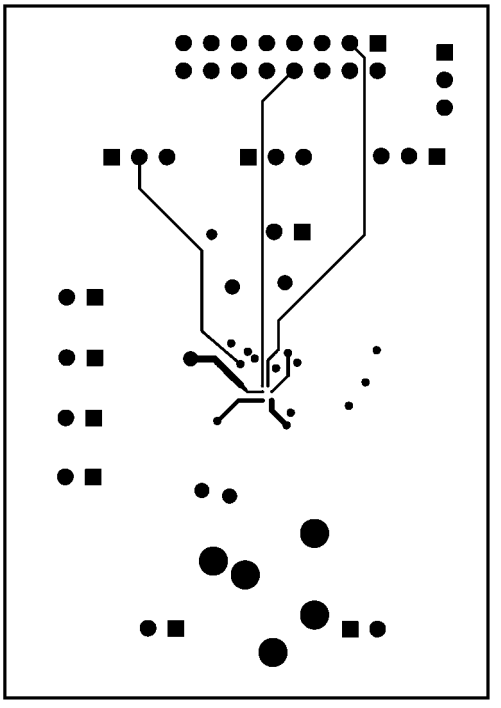
300446s7

**Top Layer**



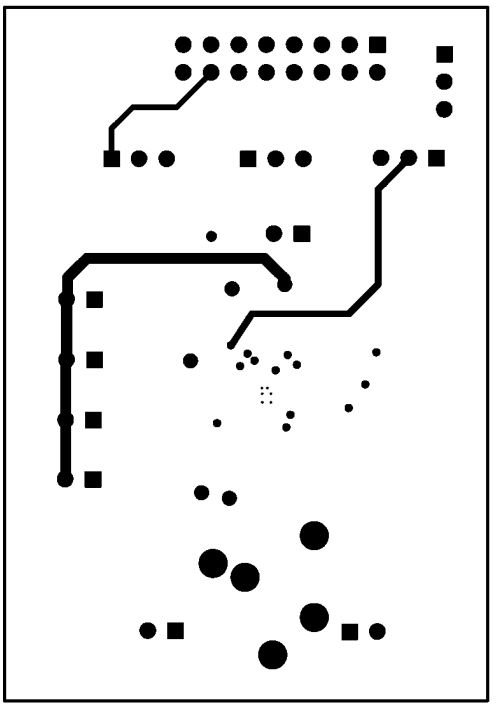
300446s5

**Layer 2**



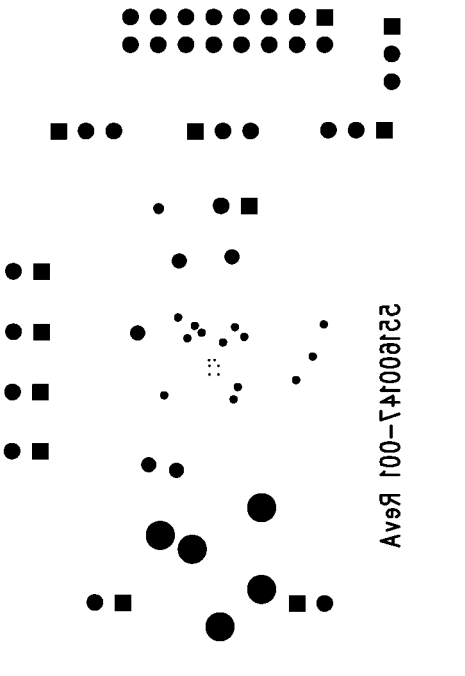
300446s6

**Layer 3**



300446s3

**Bottom Layer**



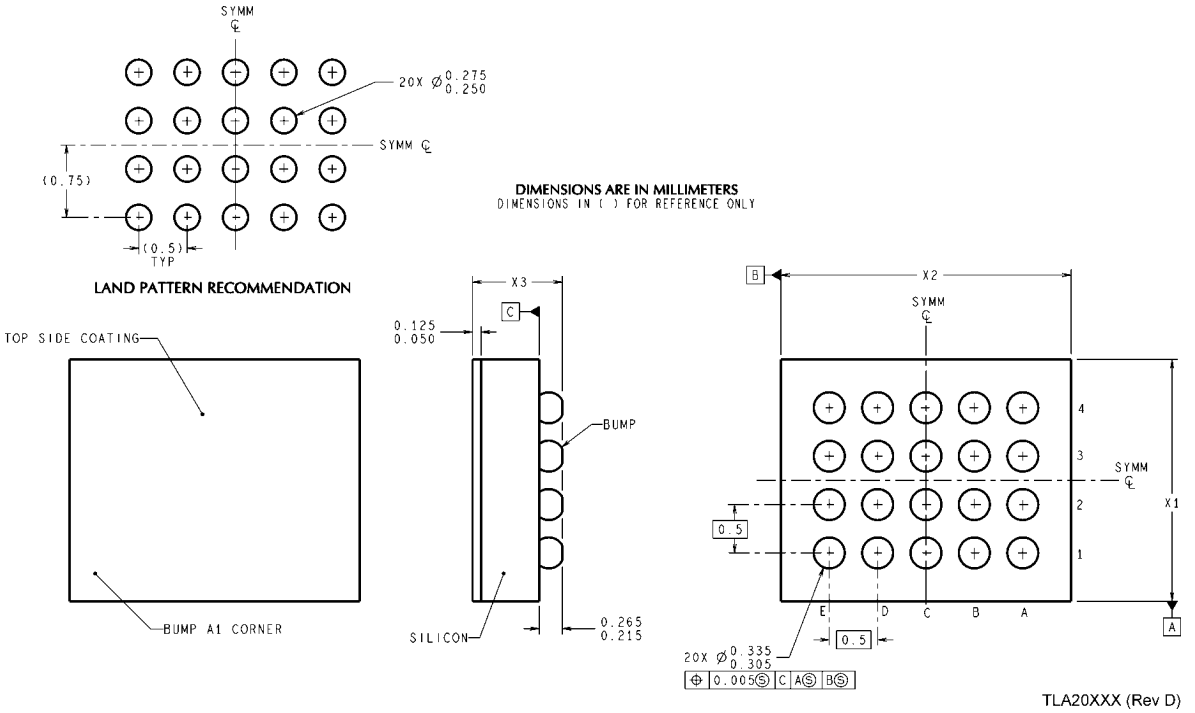

300446s4

**Bottom Silkscreen**

## Revision History

| Rev | Date | Description |
|---|---|---|
| 1.0 | 08/27/08 | Initial release. |
| 1.01 | 09/09/08 | Edited Table 6. |
| 1.02 | 03/04/09 | Added the Layout Guidelines section. |

## Physical Dimensions inches (millimeters) unless otherwise noted




TLA20XXX (Rev D)

**20 – Bump micro SMD Package**
**Order Number LM49150TL**
**NS Package Number TLA20KGA**
**$X_1$ = 2225µm, $X_2$ = 2644µm, $X_3$ = 600µm**

# Notes

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