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1/3-Inch SOC 1.3Mp CMOS Digital Image Sensor

MT9M131

Refer to the latest data sheet on Aptina's Web site: www.aptina.com

Features

- DigitalClarity® CMOS imaging technology
- System-on-a-Chip (SOC)—completely integrated camera system
- Ultra-low power, cost effective, progressive scan CMOS image sensor
- Superior low-light performance
- On-chip image flow processor (IFP) performs sophisticated processing:
  - Color recovery and correction
  - Sharpening, gamma, lens shading correction
  - On-the-fly defect correction
- Electronic pan, tilt, and zoom
- Automatic features:
  - Auto exposure (AE), auto white balance (AWB), auto black reference (ABR), auto flicker avoidance, auto color saturation, auto defect identification and correction
  - Fully automatic Xenon and LED-type flash support
- Fast exposure adaptation
- Multiple parameter contexts
- Easy and fast mode switching
- Camera control sequencer automates:
  - Snapshots
  - Snapshots with flash
  - Video clips
- Simple two-wire serial programming interface
- ITU-R BT.656 (YCbCr), 565RGB, 555RGB, or 444RGB formats (progressive scan)
- Raw and processed Bayer formats
- Output FIFO and integer clock divider:
  - Uniform pixel clocking

Applications

- Security
- Biometrics
- Videoconferencing
- Toys

Table 1: Key Performance Parameters

Parameter		Value
Optical format		1/3-inch (5:4)
Active imager size		4.6mm(H) x 3.7mm(V), 5.9mm diagonal
Active pixels		1280H x 1024V
Pixel size		3.6 x 3.6µm
Color filter array		RGB Bayer pattern
Shutter type		Electronic rolling shutter (ERS)
Maximum data rate/master clock		27 MPS/54 MHz
Frame rate	SXGA (1280 x 1024)	15 fps at 54 MHz
	VGA (640 x 480)	30 fps at 54 MHz
Maximum resolution at 60 fps/54 MHz clock		640 x 512
ADC resolution		10-bit, dual on-chip
Responsivity		1.0 V/lux-sec (550nm)
Dynamic range		71dB
SNR_{MAX}		44dB
Supply Voltage	I/O digital	1.8–3.1V
	Core digital	2.5–3.1V
	Analog	2.5–3.1V
Power consumption		170mW SXGA at 15 fps (54 MHz EXTCLK)
Operating temperature		–30°C to +70°C
Packaging		48-pin CLCC

Ordering Information

Table 2: Available Part Numbers

Part Number	Description
MT9M131C12STC	48-pin CLCC (color) (lead-free)
MT9M131C12STCD	48-pin CLCC demo kit (color)
MT9M131C12STCH	48-pin CLCC headboard (color)

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General Description

The MT9M131 is an SXGA-format single-chip camera with a 1/3-inch CMOS active-pixel digital image sensor. This device combines the MT9M011 image sensor core with fourth-generation digital image flow processor technology from Aptina. It captures high-quality color images at SXGA resolution.

The MT9M131 features DigitalClarity—Aptina's breakthrough low-noise CMOS imaging technology that achieves near-CCD image quality (based on signal-to-noise ratio and low-light sensitivity) while maintaining the inherent size, cost and integration advantages of CMOS.

The sensor is a complete camera-on-a-chip solution designed specifically to meet the demands of products such as security, biometrics, and videoconferencing cameras. It incorporates sophisticated camera functions on-chip and is programmable through a simple two-wire serial interface.

The MT9M131 performs sophisticated processing functions including color recovery, color correction, sharpening, programmable gamma correction, auto black reference clamping, auto exposure (AE), automatic 50Hz/60Hz flicker avoidance, lens shading correction (LC), auto white balance (AWB), and on-the-fly defect identification and correction. Additional features include day/night mode configurations; special camera effects such as sepia tone and solarization; and interpolation to arbitrary image size with continuous filtered zoom and pan. The device supports both xenon and LED-type flash light sources in several snapshot modes.

The MT9M131 can be programmed to output progressive-scan images up to 30 frames per second (fps) in preview power-saving mode, and 15 fps in full-resolution (SXGA) mode. In either mode, the image data can be output in any one of six formats:

- ITU-R BT.656 (formerly CCIR656, progressive scan only) YCbCr
- 565RGB
- 555RGB
- 444RGB
- Raw Bayer
- Processed Bayer

The FV and LV signals are output on dedicated signals, along with a pixel clock that is synchronous with valid data.

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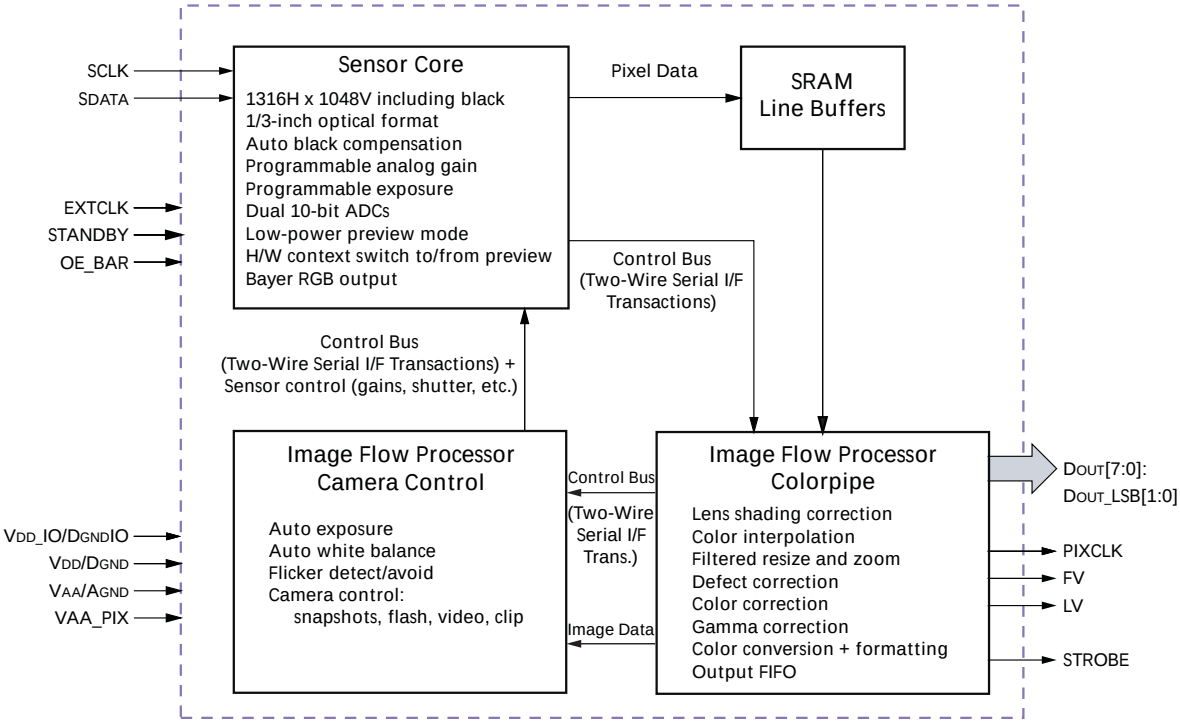
Functional Overview

The MT9M131 is a fully-automatic, single-chip camera, requiring only a power supply, lens, and clock source for basic operation. Output video is streamed through a parallel 8- or 10-bit DOUT port, shown in Figure 1.

Figure 1: Functional Block Diagram



The output pixel clock is used to latch data, while FV and LV signals indicate the active video. The MT9M131 internal registers are configured using a two-wire serial interface.

The device can be put in low-power sleep mode by asserting STANDBY and shutting down the clock. Output pins can be tri-stated by de-asserting the OE_BAR. Both tri-stating output pins and entry in standby mode also can be achieved by two-wire serial interface register writes.

The MT9M131 accepts input clocks up to 54 MHz, delivering up to 15 fps for SXGA resolution images, and up to 30 fps for QSXGA (full field-of-view [FOV], sensor pixel skipping) images. The device also supports a low- power preview configuration that delivers SXGA images at 7.5 fps and QSXGA images at 30 fps. The device can be programmed to slow the frame rate in low light conditions to achieve longer exposures and better image quality.

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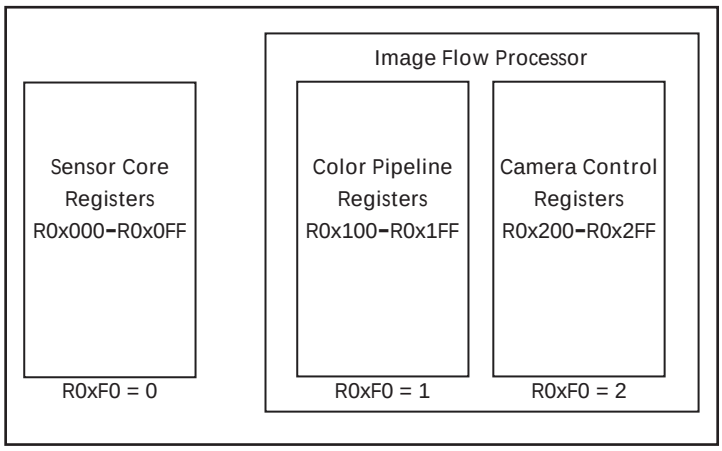
Internal Architecture

Internally, the MT9M131 consists of a sensor core and an IFP. The IFP is divided in two sections: the colorpipe (CP), and the camera controller (CC). The sensor core captures raw Bayer-encoded images that are then input in the IFP. The CP section of the IFP processes the incoming stream to create interpolated, color-corrected output, and the CC section controls the sensor core to maintain the desired exposure and color balance, and to support snapshot modes. The sensor core, CP, and CC registers are grouped in three separate address spaces, as shown in Figure 2.

Figure 2: Internal Registers Grouping



Notes: 1. Internal registers are grouped in three address spaces. Register R0xF0 in each page selects the desired address space.

When accessing internal registers through the two-wire serial interface, select the desired address space by programming the R0xF0 shared register.

The MT9M131 accelerates mode switching with hardware-assisted context switching and supports taking snapshots, flash snapshots, and video clips using a configurable sequencer.

The MT9M131 supports a range of color formats derived from four primary color representations: YCbCr, RGB, raw Bayer (unprocessed, directly from the sensor), and processed Bayer (Bayer format data regenerated from processed RGB). The device also supports a variety of output signaling/timing options:

- Standard FV/LV video interface with gated pixel clocks
- Standard video interface with uniform clocking
- Progressive ITU-R BT.656 marker-embedded video interface with either gated or uniform pixel clocking

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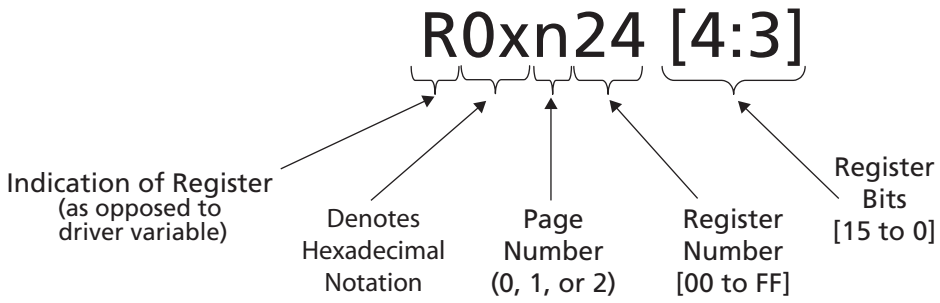
Register Operations

This data sheet refers to various registers that the user reads from or writes to for altering the MT9M131 operation. Hardware registers appear as follows and may be read from or written to by sending the address and data information over the two-wire serial interface.

Figure 3: Register Legend



The MT9M131 was designed to facilitate customizations to optimize image quality processing. Multiple parameters are allowed to be adjusted at various stages of the image processing pipeline to tune the quality of the output image.

The MT9M131 contains three register pages: sensor, colorpipe, and camera control. The register page must be set prior to writing to a register in the page.

For example, to write to register R0x106 (register 6 in page 1):

- Write the value of “1” to the page map register (0xF0)
- Write the desired value to register R0x06

The sensor maintains the page number once set. The page map register is located at address 0xF0 for all three register pages.

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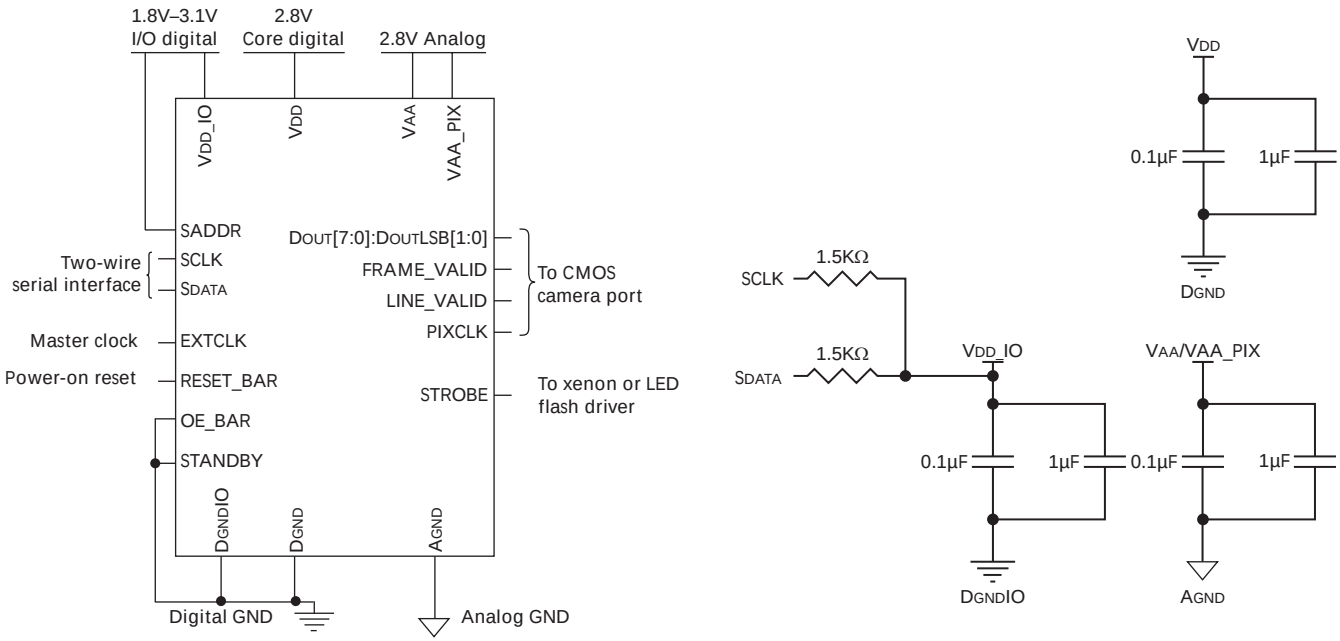
Typical Connection

Figure 4 shows typical MT9M131 device connections.

Figure 4: Typical Configuration (connection)



Notes:
1. For two-wire serial interface, Aptina recommends a 1.5KΩ resistor; however, larger values may be used for slower two-wire speed.
2. VDD, VAA, VAA_PIX must all be at the same potential, though if connected, care must be taken to avoid excessive noise injection in the VAA/VAA_PIX power domains.
3. Logic levels of all input pins, that is, SADDR, EXTCLK, SCLK, SDATA, OE_BAR, STANDBY, and RESET_BAR must be equal to VDD_IO.

For low-noise operation, the MT9M131 requires separate power supplies for analog and digital. Incoming digital and analog ground conductors can be tied together next to the die. Both power supply rails should be decoupled to ground using ceramic capacitors. The use of inductance filters is not recommended.

The MT9M131 also supports different digital core (VDD/DGND) and I/O power (VDD_IO/DGNDIO) power domains that can be at different voltages.

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Pin/Ball Assignment

The MT9M131 is available in the CLCC package configuration. Figure 5 shows the 48-Pin CLCC assignment.

Figure 5: 48-Pin CLCC Assignment

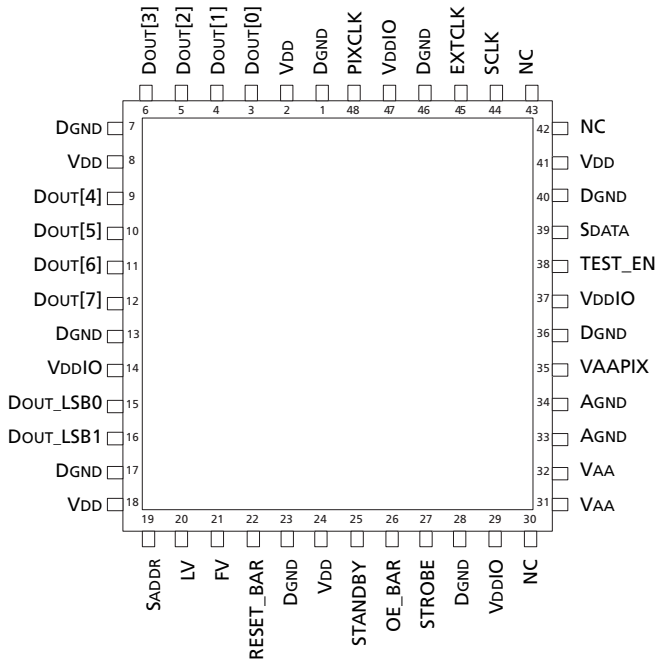

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Table 3: Pin/Ball Descriptions

Signal	Type	Default Operation	Description
EXTCLK	I/O	Input	Master clock in sensor.
OE_BAR	I/O	Input	Active LOW: output enable for DOUT[7:0].
RESET_BAR	I/O	Input	Active LOW: asynchronous reset.
SADDR	I/O	Input	Two-wire serial interface DeviceID selection 1:0xBA, 0:0x90.
SCLK	I/O	Input	Two-wire serial interface clock.
STANDBY	I/O	Input	Active HIGH: disables imager.
SDATA	I/O	Input	Two-wire serial interface data I/O.
TEST_EN	I/O	Input	Tie to DGND for normal operation (manufacturing use only).
DOUT0	I/O	Output	
DOUT1	I/O	Output	
DOUT2	I/O	Output	
DOUT3	I/O	Output	
DOUT4	I/O	Output	
DOUT5	I/O	Output	
DOUT6	I/O	Output	
DOUT7	I/O	Output	
DOUT_LSB0	I/O	Output	Sensor bypass mode output 0—typically left unconnected for normal SOC operation.
DOUT_LSB1	I/O	Output	Sensor bypass mode output 1—typically left unconnected for normal SOC operation.
FRAME_VALID(FV)	I/O	Output	Active HIGH: FV; indicates active frame.
LINE_VALID (LV)	I/O	Output	Active HIGH: LV, DATA_VALID; indicates active pixel.
PIXCLK	I/O	Output	Pixel clock output.
STROBE	I/O	Output	Active HIGH: strobe (xenon) or turn on (LED) flash.
AGND	Supply		Analog ground.
DGND	Supply		Core digital ground.
DGNDIO	Supply		I/O digital ground.
VAA	Supply		Analog power (2.5–3.1V).
VAAPIX	Supply		Pixel array analog power supply (2.5–3.1V).
VDD	Supply		Core digital power (2.5–3.1V).
VDDIO	Supply		I/O digital power (1.8–3.1V).
NC	–		No connect.

Notes: 1. All inputs and outputs are implemented with bidirectional buffers. Care must be taken to ensure that all inputs are driven and all outputs are driven if tri-stated.

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Output Data Ordering

Table 4: Data Ordering in YCbCr Mode

Mode	Byte			
Default	Cbi	Yi	Cri	Yi+1
Swap CrCb	Cri	Yi	Cbi	Yi+1
SwapYC	Yi	Cbi	Yi+1	Cri
Swap CrCb, SwapYC	Yi	Cri	Yi+1	Cbi

Table 5: Output Data Ordering in Processed Bayer Mode

Mode	Line	Byte			
Default	First	Gi	Ri+1	Gi+2	Ri+3
	Second	Bi	Gi+1	Bi+2	Gi+3
Flip Bayer col	First	Ri	Gi+1	Ri+2	Gi+3
	Second	Gi	Bi+1	Gi+2	Bi+3
Flip Bayer row	First	Bi	Gi+1	Bi+2	Gi+3
	Second	Gi	Ri+1	Gi+2	Ri+3
Flip Bayer col, Flip Bayer row	First	Gi	Bi+1	Gi+2	Bi+3
	Second	Ri	Gi+1	Ri+2	Gi+3

Table 6: Output Data Ordering in RGB Mode

Mode (Swap Disabled)	Byte	D7	D6	D5	D4	D3	D2	D1	D0
565RGB	First	R7	R6	R5	R4	R3	G7	G6	G5
	Second	G4	G3	G2	B7	B6	B5	B4	B3
555RGB	First	0	R7	R6	R5	R4	R3	G7	G6
	Second	G5	G4	G3	B7	B6	B5	B4	B3
444xRGB	First	R7	R6	R5	R4	G7	G6	G5	G4
	Second	B7	B6	B5	B4	0	0	0	0
x444RGB	First	0	0	0	0	R7	R6	R5	R4
	Second	G7	G6	G5	G4	B7	B6	B5	B4

Table 7: Output Data Ordering in (8 + 2) Bypass Mode

Mode	Byte	D7	D6	D5	D4	D3	D2	D1	D0
8 + 2 bypass	First	B9	B8	B7	B6	B5	B4	B3	B2
	Second	0	0	0	0	0	0	B1	B0

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IFP Register List

Table 8: Colorpipe Registers (Address Page 1)

Register Number Dec (Hex)	Register Name	Data Format (Binary)	Default Value Dec (Hex)	Module
R5 (R0x105)	Aperture correction	0000 0000 0000 dddd	3 (0003)	Interp
R6 (R0x106)	Operating mode control	dddd dddd 0ddd dddd	28686 (700E)	Cfg
R8 (R0x108)	Output format control	0000 0ddd dddd dddd	128 (0080)	Cfg
R16 (R0x110)	Reserved	–	61437 (EFFD)	–
R17 (R0x111)	Reserved	–	64831 (FD3F)	–
R18 (R0x112)	Reserved	–	16367 (3FEF)	–
R19 (R0x113)	Reserved	–	N/A	–
R20 (R0x114)	Reserved	–	N/A	–
R21 (R0x115)	Reserved	–	N/A	–
R27 (R0x11B)	Reserved	–	0 (0000)	–
R28 (R0x11C)	Reserved	–	0 (0000)	–
R29 (R0x11D)	Reserved	–	N/A	–
R30 (R0x11E)	Reserved	–	512 (0200)	–
R37 (R0x125)	Color saturation control	0000 0000 00dd dddd	5 (0005)	rgb2yuv
R52 (R0x134)	Luma offset	dddd dddd dddd dddd	16 (0010)	CamInt
R53 (R0x135)	Luma clip	dddd dddd dddd dddd	61456 (F010)	CamInt
R58 (R0x13A)	Output format control 2—context A	0ddd dddd dddd dddd	512 (0200)	CamInt
R59 (R0x13B)			1066 (042A)	LensCorr
R60 (R0x13C)			1024 (0400)	LensCorr
R71 (R0x147)			24 (0018)	
R72 (R0x148)	Test pattern generator control	0000 0000 d000 0ddd	0 (0000)	FifoInt
R76 (R0x14C)	Defect correction context A	0000 0000 0000 0ddd	0 (0000)	DfctCorr
R77 (R0x14D)	Defect correction context B	0000 0000 0000 0ddd	0 (0000)	DfctCorr
R78 (R0x14E)	Reserved	–	10 (000A)	–
R80 (R0x150)			N/A	
R82 (R0x152)	Reserved	–	0 (0000)	–
R83 (R0x153)			7700 (1E14)	GmaCorr
R84 (R0x154)			17966 (462E)	GmaCorr
R85 (R0x155)			34666 (876A)	GmaCorr
R86 (R0x156)			47008 (B7A0)	GmaCorr
R87 (R0x157)			57548 (E0CC)	GmaCorr
R88 (R0x158)			0 (0000)	GmaCorr
R104 (R0x168)	Reserved	–	17 (0011)	–
R128 (R0x180)			7 (0007)	LensCorr
R129 (R0x181)			56588 (DD0C)	LensCorr
R130 (R0x182)			62696 (F4E8)	LensCorr
R131 (R0x183)			1276 (04FC)	LensCorr
R132 (R0x184)			57868 (E20C)	LensCorr
R133 (R0x185)			63212 (F6EC)	LensCorr
R134 (R0x186)			764 (02FC)	LensCorr
R135 (R0x187)			56588 (DD0C)	LensCorr
R136 (R0x188)			62696 (F4E8)	LensCorr
R137 (R0x189)			250 (00FA)	LensCorr

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Table 8: Colorpipe Registers (Address Page 1) (Continued)

Register Number Dec (Hex)	Register Name	Data Format (Binary)	Default Value Dec (Hex)	Module
R138 (R0x18A)			34866 (8832)	LensCorr
R139 (R0x18B)			56754 (DDB2)	LensCorr
R140 (R0x18C)			63466 (F7EA)	LensCorr
R141 (R0x18D)			2 (0002)	LensCorr
R142 (R0x18E)			47646 (BA1E)	LensCorr
R143 (R0x18F)			60627 (ECD3)	LensCorr
R144 (R0x190)			63473 (F7F1)	LensCorr
R145 (R0x191)			255 (00FF)	LensCorr
R146 (R0x192)			48926 (BF1E)	LensCorr
R147 (R0x193)			61142 (EED6)	LensCorr
R148 (R0x194)			63474 (F7F2)	LensCorr
R149 (R0x195)			3 (0003)	LensCorr
R153 (R0x199)	Line counter	???? ???? ???? ????	N/A	CamInt
R154 (R0x19A)	Frame counter	???? ???? ???? ????	N/A	CamInt
R155 (R0x19B)	Output format control 2—context B	0ddd dddd dddd dddd	512 (0200)	CamInt
R157 (R0x19D)	Reserved	–	9390 (24AE)	–
R158 (R0x19E)	Reserved	–	N/A	–
R159 (R0x19F)	Reducer horizontal pan—context B	0d00 0ddd dddd dddd	0 (0000)	Interp
R160 (R0x1A0)	Reducer horizontal zoom—context B	0000 0ddd dddd dddd	1280 (0500)	Interp
R161 (R0x1A1)	Reducer horizontal size—context B	0000 0ddd dddd dddd	1280 (0500)	Interp
R162 (R0x1A2)	Reducer vertical pan—context B	0d00 0ddd dddd dddd	0 (0000)	Interp
R163 (R0x1A3)	Reducer vertical zoom—context B	0000 0ddd dddd dddd	1024 (0400)	Interp
R164 (R0x1A4)	Reducer vertical size—context B	0000 0ddd dddd dddd	1024 (0400)	Interp
R165 (R0x1A5)	Reducer horizontal pan—context A	0d00 0ddd dddd dddd	0 (0000)	Interp
R166 (R0x1A6)	Reducer horizontal zoom—context A	0000 0ddd dddd dddd	1280 (0500)	Interp
R167 (R0x1A7)	Reducer horizontal size—context A	0000 0ddd dddd dddd	640 (0280)	Interp
R168 (R0x1A8)	Reducer vertical pan—context A	0d00 0ddd dddd dddd	0 (0000)	Interp
R169 (R0x1A9)	Reducer vertical zoom—context A	0000 0ddd dddd dddd	1024 (0400)	Interp
R170 (R0x1AA)	Reducer vertical size—context A	0000 0ddd dddd dddd	512 (0200)	Interp
R171 (R0x1AB)	Reducer current zoom horizontal	???? 0??? ???? ????	N/A	Interp
R172 (R0x1AC)	Reducer current zoom vertical	???? 0??? ???? ????	N/A	Interp
R174 (R0x1AE)	Reducer zoom step size	dddd dddd dddd dddd	1284 (0504)	Interp
R175 (R0x1AF)	Reducer zoom control	0000 00dd 0ddd dddd	16 (0010)	Interp
R179 (R0x1B3)	Global clock control	0000 0000 0000 00dd	2 (0002)	ClockRst
R180 (R0x1B4)			32 (0020)	
R181 (R0x1B5)			257 (0101)	
R182 (R0x1B6)			4363 (110B)	LensCorr
R183 (R0x1B7)			15399 (3C27)	LensCorr
R184 (R0x1B8)			4362 (110A)	LensCorr
R185 (R0x1B9)			12834 (3222)	LensCorr
R186 (R0x1BA)			5643 (160B)	LensCorr
R187 (R0x1BB)			12836 (3224)	LensCorr
R188 (R0x1BC)			9228 (240C)	LensCorr
R189 (R0x1BD)			24124 (5E3C)	LensCorr
R190 (R0x1BE)			127 (007F)	LensCorr

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Table 8: Colorpipe Registers (Address Page 1) (Continued)

Register Number Dec (Hex)	Register Name	Data Format (Binary)	Default Value Dec (Hex)	Module
R191 (R0x1BF)			8200 (2008)	LensCorr
R192 (R0x1C0)			20023 (4E37)	LensCorr
R193 (R0x1C1)			100 (0064)	LensCorr
R194 (R0x1C2)			8463 (210F)	LensCorr
R195 (R0x1C3)			19250 (4B32)	LensCorr
R196 (R0x1C4)			100 (0064)	LensCorr
R200 (R0x1C8)	Global context control	dddd dddd dddd dddd	0 (0000)	CntxCtl
R201 (R0x1C9)	Reserved	–	N/A	–
R202 (R0x1CA)	Reserved	–	N/A	–
R203 (R0x1CB)	Reserved	–	N/A	–
R204 (R0x1CC)	Reserved	–	N/A	–
R205 (R0x1CD)	Reserved	–	N/A	–
R206 (R0x1CE)	Reserved	–	N/A	–
R207 (R0x1CF)	Reserved	–	N/A	–
R208 (R0x1D0)	Reserved	–	N/A	–
R220 (R0x1DC)			7700 (1E14)	GmaCorr
R221 (R0x1DD)			17966 (462E)	GmaCorr
R222 (R0x1DE)			34666 (876A)	GmaCorr
R223 (R0x1DF)			47008 (B7A0)	GmaCorr
R224 (R0x1E0)			57548 (E0CC)	GmaCorr
R225 (R0x1E1)			0 (0000)	GmaCorr
R226 (R0x1E2)	Effects mode	dddd dddd 0000 0ddd	28672 (7000)	GmaCorr
R227 (R0x1E3)	Effects sepia	dddd dddd dddd dddd	45091 (B023)	GmaCorr
R240 (R0x1F0)	Page map	0000 0000 0000 0ddd	0 (0000)	Cfg
R241 (R0x1F1)	Byte-wise address	–	Reserved	–

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Table 9: Camera Control Registers (Address Page 2)

Register Number Dec (Hex)	Register Name	Data Format (Binary)	Default Value Dec (Hex)	Module
R2 (R0x202)			110 (006E)	ColorCorr
R3 (R0x203)			10531 (2923)	ColorCorr
R4 (R0x204)			1316 (0524)	ColorCorr
R9 (R0x209)			146 (0092)	ColorCorr
R10 (R0x20A)			22 (0016)	ColorCorr
R11 (R0x20B)			8 (0008)	ColorCorr
R12 (R0x20C)			171 (00AB)	ColorCorr
R13 (R0x20D)			147 (0093)	ColorCorr
R14 (R0x20E)			88 (0058)	ColorCorr
R15 (R0x20F)			77 (004D)	ColorCorr
R16 (R0x210)			169 (00A9)	ColorCorr
R17 (R0x211)			160 (00A0)	ColorCorr
R18 (R0x212)			N/A	ColorCorr
R19 (R0x213)			N/A	ColorCorr
R20 (R0x214)			N/A	ColorCorr
R21 (R0x215)			373 (0175)	ColorCorr
R22 (R0x216)			22 (0016)	ColorCorr
R23 (R0x217)			67 (0043)	ColorCorr
R24 (R0x218)			12 (000C)	ColorCorr
R25 (R0x219)			0 (0000)	ColorCorr
R26 (R0x21A)			21 (0015)	ColorCorr
R27 (R0x21B)			31 (001F)	ColorCorr
R28 (R0x21C)			22 (0016)	ColorCorr
R29 (R0x21D)			152 (0098)	ColorCorr
R30 (R0x21E)			76 (004C)	ColorCorr
R31 (R0x21F)			160 (00A0)	AWB
R32 (R0x220)			51220 (C814)	AWB
R33 (R0x221)			32896 (8080)	AWB
R34 (R0x222)			55648 (D960)	AWB
R35 (R0x223)			55648 (D960)	AWB
R36 (R0x224)			32512 (7F00)	AWB
R38 (R0x226)	Auto exposure window horizontal boundaries	dddd dddd dddd dddd	32768 (8000)	AutoExp
R39 (R0x227)	Auto exposure window vertical boundaries	dddd dddd dddd dddd	32776 (8008)	AutoExp
R40 (R0x228)			61188 (EF04)	AWB
R41 (R0x229)			36211 (8D73)	AWB
R42 (R0x22A)			208 (00D0)	AWB
R43 (R0x22B)	Auto exposure center horizontal window boundaries	dddd dddd dddd dddd	24608 (6020)	AutoExp
R44 (R0x22C)	Auto exposure center vertical window boundaries	dddd dddd dddd dddd	24608 (6020)	AutoExp
R45 (R0x22D)	AWB window boundaries	dddd dddd dddd dddd	61600 (F0A0)	AWB
R46 (R0x22E)	Auto exposure target and precision control	dddd dddd dddd dddd	3146 (0C4A)	AutoExp
R47 (R0x22F)	Auto exposure speed and sensitivity control—context A	dddd dddd dddd dddd	57120 (DF20)	AutoExp
R48 (R0x230)			N/A	AWB
R49 (R0x231)			N/A	AWB
R50 (R0x232)			N/A	AWB
R51 (R0x233)			5230 (146E)	AutoExp

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Table 9: Camera Control Registers (Address Page 2) (Continued)

Register Number Dec (Hex)	Register Name	Data Format (Binary)	Default Value Dec (Hex)	Module
R54 (R0x236)			30736 (7810)	AutoExp
R55 (R0x237)			768 (0300)	AutoExp
R56 (R0x238)			1088 (0440)	AutoExp
R57 (R0x239)			1676 (068C)	AutoExp
R58 (R0x23A)			1676 (068C)	AutoExp
R59 (R0x23B)			1676 (068C)	AutoExp
R60 (R0x23C)			1676 (068C)	AutoExp
R61 (R0x23D)			6105 (17D9)	AutoExp
R62 (R0x23E)			7423 (1CFF)	AWB
R63 (R0x23F)			N/A	AutoExp
R70 (R0x246)			55552 (D900)	AutoExp
R75 (R0x24B)	Reserved	–	0 (0000)	–
R76 (R0x24C)			N/A	AutoExp
R77 (R0x24D)			N/A	AutoExp
R79 (R0x24F)	Reserved	–	N/A	–
R87 (R0x257)			537 (0219)	AutoExp
R88 (R0x258)			644 (0284)	AutoExp
R89 (R0x259)			537 (0219)	AutoExp
R90 (R0x25A)			644 (0284)	AutoExp
R91 (R0x25B)	Flicker control 0	?000 0000 0000 0ddd	2 (0002)	FD
R92 (R0x25C)			4620 (120C)	
R93 (R0x25D)			5394 (1512)	
R94 (R0x25E)			26684 (683C)	ColorCorr
R95 (R0x25F)			12296 (3008)	ColorCorr
R96 (R0x260)			2 (0002)	ColorCorr
R97 (R0x261)			32896 (8080)	
R98 (R0x262)	Auto exposure digital gains monitor	???? ???? ???? ????	N/A	AutoExp
R99 (R0x263)	Reserved	–	N/A	–
R100 (R0x264)	Reserved	–	23036 (59FC)	–
R101 (R0x265)			0 (0000)	AutoExp
R103 (R0x267)	Auto exposure digital gain limits	dddd dddd dddd dddd	16400 (4010)	AutoExp
R104 (R0x268)	Reserved	–	17 (0011)	–
R106 (R0x26A)	Reserved	–	N/A	–
R107 (R0x26B)	Reserved	–	N/A	–
R108 (R0x26C)	Reserved	–	N/A	–
R109 (R0x26D)	Reserved	–	N/A	–
R110 (R0x26E)	Reserved	–	N/A	–
R111 (R0x26F)	Reserved	–	N/A	–
R112 (R0x270)	Reserved	–	N/A	–
R113 (R0x271)	Reserved	–	N/A	–
R114 (R0x272)	Reserved	–	N/A	–
R115 (R0x273)	Reserved	–	N/A	–
R116 (R0x274)	Reserved	–	N/A	–
R117 (R0x275)	Reserved	–	N/A	–
R118 (R0x276)	Reserved	–	N/A	–

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Table 9: Camera Control Registers (Address Page 2) (Continued)

Register Number Dec (Hex)	Register Name	Data Format (Binary)	Default Value Dec (Hex)	Module
R119 (R0x277)	Reserved	–	N/A	–
R120 (R0x278)	Reserved	–	N/A	–
R121 (R0x279)	Reserved	–	N/A	–
R122 (R0x27A)	Reserved	–	N/A	–
R123 (R0x27B)	Reserved	–	N/A	–
R124 (R0x27C)	Reserved	–	N/A	–
R125 (R0x27D)	Reserved	–	N/A	–
R130 (R0x282)			1020 (03FC)	AutoExp
R131 (R0x283)			769 (0301)	AutoExp
R132 (R0x284)			193 (00C1)	AutoExp
R133 (R0x285)			929 (03A1)	AutoExp
R134 (R0x286)			980 (03D4)	AutoExp
R135 (R0x287)			983 (03D7)	AutoExp
R136 (R0x288)			921 (0399)	AutoExp
R137 (R0x289)			1016 (03F8)	AutoExp
R138 (R0x28A)			28 (001C)	AutoExp
R139 (R0x28B)			957 (03BD)	AutoExp
R140 (R0x28C)			987 (03DB)	AutoExp
R141 (R0x28D)			957 (03BD)	AutoExp
R142 (R0x28E)			1020 (03FC)	AutoExp
R143 (R0x28F)			990 (03DE)	AutoExp
R144 (R0x290)			990 (03DE)	AutoExp
R145 (R0x291)			990 (03DE)	AutoExp
R146 (R0x292)			990 (03DE)	AutoExp
R147 (R0x293)			31 (001F)	AutoExp
R148 (R0x294)			65 (0041)	AutoExp
R149 (R0x295)			867 (0363)	AutoExp
R150 (R0x296)	Reserved	–	0 (0000)	–
R151 (R0x297)	Reserved	–	N/A	–
R152 (R0x298)	Reserved	–	255 (00FF)	–
R153 (R0x299)	Reserved	–	1 (0001)	–
R156 (R0x29C)	Auto exposure speed and sensitivity control—context B	dddd dddd dddd dddd	57120 (DF20)	AutoExp
R180 (R0x2B4)	Reserved	–	32 (0020)	–
R181 (R0x2B5)	Reserved	–	N/A	–
R198 (R0x2C6)	Reserved	–	0 (0000)	–
R199 (R0x2C7)	Reserved	–	N/A	–
R200 (R0x2C8)	Global context control	dddd dddd dddd dddd	0 (0000)	CntxCtl
R201 (R0x2C9)			N/A	CamCtl
R202 (R0x2CA)			N/A	CamCtl
R203 (R0x2CB)			0 (0000)	CamCtl
R204 (R0x2CC)			0 (0000)	CamCtl
R205 (R0x2CD)			8608 (21A0)	CamCtl
R206 (R0x2CE)			7835 (1E9B)	CamCtl
R207 (R0x2CF)			19018 (4A4A)	CamCtl
R208 (R0x2D0)			5773 (168D)	CamCtl

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Table 9: Camera Control Registers (Address Page 2) (Continued)

Register Number Dec (Hex)	Register Name	Data Format (Binary)	Default Value Dec (Hex)	Module
R209 (R0x2D1)			77 (004D)	CamCtl
R210 (R0x2D2)			0 (0000)	CamCtl
R211 (R0x2D3)			0 (0000)	CntxCtl
R212 (R0x2D4)			520 (0208)	CamCtl
R213 (R0x2D5)			0 (0000)	CamCtl
R239 (R0x2EF)			8 (0008)	AWB
R240 (R0x2F0)	Page map	0000 0000 0000 0ddd	0 (0000)	Cfg
R241 (R0x2F1)	Byte-wise address	–	Reserved	–
R242 (R0x2F2)			0 (0000)	AWB
R243 (R0x2F3)	Reserved	–	0 (0000)	–
R244 (R0x2F4)			110 (006E)	ColorCorr
R245 (R0x2F5)			135 (0087)	ColorCorr
R246 (R0x2F6)			54 (0036)	ColorCorr
R247 (R0x2F7)			13 (000D)	ColorCorr
R248 (R0x2F8)			171 (00AB)	ColorCorr
R249 (R0x2F9)			136 (0088)	ColorCorr
R250 (R0x2FA)			72 (0048)	ColorCorr
R251 (R0x2FB)			87 (0057)	ColorCorr
R252 (R0x2FC)			94 (005E)	ColorCorr
R253 (R0x2FD)			122 (007A)	ColorCorr
R254 (R0x2FE)			20543 (503F)	ColorCorr
R255 (R0x2FF)			43136 (A880)	ColorCorr

Notes: 1. Data Format Key:
0 = “Don't Care” bit. The exceptions: R0x200 and R0x2FF, which are hardwired R/O binary values.
d = R/W bit
? = R/O bit.

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IFP Register Description

Configuration

The vast majority of IFP registers associate naturally to one of the IFP modules. These modules are identified in Table 9 on page 17. Detailed register descriptions follow in Table 10. A few registers create effects across a number of module functions. These include R0xF0 page map register (R/W); R0x106 operating mode control register (R/W); R0x108 output format control register (R/W); the R0x23E gain types and CCM threshold register—the gain threshold for CCM adjustment (R/W)

Colorpipe Registers

Unless noted otherwise in this document, colorpipe registers take effect immediately. This can result in one or more distorted output frames. These registers should be adjusted during FV LOW or the resulting image should be hidden for one or two frames.

Colorpipe resize registers are updated shortly after FV goes HIGH. They are not examined again until the next frame.

Table 10: Colorpipe Register Description Address Page 1

Register Number Dec–Hex	Description
R5:1—R0x105 - Aperture correction	
Default	0x0003
Description	Aperture correction scale factor, used for sharpening.
Bit 3	Enables automatic sharpness reduction control (see R0x233).
Bits 2:0	Sharpening factor: “000”—No sharpening. “001”—25% sharpening. “010”—50% sharpening. “011”—75% sharpening. “100”—100% sharpening. “101”—125% sharpening. “110”—150% sharpening. “111”—200% sharpening.
R6:1—R0x106 - Operating mode control (R/W)	
Default	0x700E
Description	This register specifies the operating mode of the IFP.
Bit 15	Enables manual white balance. User can set the base matrix and color channel gains. This bit must be asserted and de-asserted with a frame in between to force new color correction settings to take effect.
Bit 14	Enables auto exposure.
Bit 13	Enables on-the-fly defect correction.
Bit 12	Clips aperture corrections. Small aperture corrections (< 8) are attenuated to reduce noise amplification.
Bit 11	Load color correction matrix 1: In manual white balance mode, triggers the loading of a new base matrix in color correction and the loading of new base sensor gain ratios. 0: Enables the matrix to be changed “offline.”
Bit 10	Enables lens shading correction. 1: Enables lens shading correction.
Bit 9	Reserved.

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Table 10: Colorpipe Register Description Address Page 1 (Continued)

Register Number Dec–Hex	Description
Bit 8	Reserved.
Bit 7	Enables flicker detection. 1: Enables automatic flicker detection.
Bit 6	Reserved for future expansion.
Bit 5	Reserved.
Bit 4	Bypasses color correction matrix. 1: Outputs raw color, bypassing color correction. 0: Normal color processing.
Bits 3:2	Auto exposure back light compensation control. "00"—Auto exposure sampling window is specified by R0x226 and R0x227 ("large window"). "01"—Auto exposure sampling window is specified by R0x22B and R0x22C ("small window"). "1X"—Auto exposure sampling window is specified by the weighted sum of the large window and the small window, with the small window weighted four times more heavily.
Bit 1	Enables AWB. 1: Enables auto white balance. 0: Freezes white balance at current values.
Bit 0	Reserved for future expansion.
R8:1—R0x108 - Output format control (R/W)	
Default	0x0080
Description	This register specifies the output timing and format in conjunction with R0x13A or R0x19B (depending on the context).
Bits 15:10	Reserved for future expansion.
Bit 9	Flip Bayer columns in processed Bayer output mode. 0: Column order is green, red and blue, green. 1: Column order is red, green and green, blue.
Bit 8	Flip Bayer row in processed Bayer output mode. 0: First row contains green and red; the second row contains blue and green. 1: First row contains blue and green; the second row contains green and red.
Bit 7	Controls the values used for the protection bits in Rec. ITU-R BT.656 codes. 0: Use zeros for the protection bits. 1: Use the correct values.
Bit 5	Multiplexes Y (in YCbCr mode) or green (in RGB mode) channel on all channels (monochrome). 1: Forces Y/G onto all channels.
Bit 4	Disables Cab color output channel (Cb = 128) in YCbCr mode and disables the blue color output channel (B = 0) in RGB mode. 1: Forces Cab to 128 or B to 0.
Bit 3	Disables Y color output channel (Y = 128) in YCbCr and disables the green color output channel (G = 0) in RGB mode. 1: Forces Y to 128 or G to 0.
Bit 2	Disables Cr color output channel (Cr = 128) in YCbCr mode and disables the red color output channel (R = 0) in RGB mode. 1: Forces Cr to 128 or R to 0.
Bit 1	Toggles the assumptions about Bayer vertical CFA shift. 0: Row containing red comes first. 1: Row containing blue comes first.
Bit 0	Toggles the assumptions about Bayer horizontal CFA shift. 0: Green comes first. 1: Red or blue comes first.

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Table 10: Colorpipe Register Description Address Page 1 (Continued)

Register Number Dec–Hex	Description
R37:1—R0x125 - Color saturation control (R/W)	
Default	0x0005
Description	This register specifies the color saturation control settings.
Bit 5:3	Specify overall attenuation of the color saturation. "000"—Full color saturation. "001"—75% of full saturation. "010"—50% of full saturation. "011"—37.5% of full saturation. "100"—25% of full saturation. "101"—150% of full saturation. "110"—black and white
Bit 2:0	Specify color saturation attenuation at high luminance (linearly increasing attenuation from no attenuation to monochrome at luminance of 224). "000"—No attenuation. "001"—Attenuation starts at luminance of 216. "010"—Attenuation starts at luminance of 208. "011"—Attenuation starts at luminance of 192. "100"—Attenuation starts at luminance of 160. "101"—Attenuation starts at luminance of 96.
R52:1—R0x134 - Luma offset (R/W)	
Default	0x0010
Description	Offset added to the luminance prior to output.
Bits 15:8	Y Offset in YCbCr mode.
Bits 7:0	Offset in RGB mode.
R53:1—R0x135 - Luma clip (R/W)	
Default	0xF010
Description	Clipping limits for output luminance.
Bits 15:8	Highest value of output luminance.
Bits 7:0	Lowest value of output luminance.
R58:1—R0x13A - Output format control 2—context A (R/W)	
Default	0x0200
Description	Output format control 2A.
Bit 14	Output processed Bayer data.
Bit 13	Reserved
Bit 12	
Bit 11	Enables embedding Rec. ITU-R BT.656 synchronization codes in the output data. See R0x19B
Bit 10	Entire image processing is bypassed and raw bayer is output directly. In YCbCr or RGB mode: 0: Normal operation, sensor core data flows through IFP. 1: Bypass IFP and output Imager data directly (full 10 bits). The image data still passes through the camera interface FIFO and the 10 bits are formatted to two output bytes through the camera interface; that is, 8 + 2. Data rate is effectively the same as default 16-bit /per pixel modes. Auto exposure/AWB, etc. still function and control the sensor, though they are assuming some gain/correction through the colorpipe. See R0x19B
Bit 9	Invert output pixel clock. Inverts output pixel clock. By default, this bit is asserted. 0: output data transitions on the rising edge of PIXCLK for capture by the receiver on the falling edge. 1: output data transitions on the falling edge of PIXCLK for capture by the receiver on the rising edge.

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Table 10: Colorpipe Register Description Address Page 1 (Continued)

Register Number Dec–Hex	Description
Bit 8	Enables RGB output. 0: Output YCbCr data. 1: Output RGB format data as defined by R0x13A[7:6].
Bits 7:6	RGB output format: "00"—16-bit 565RGB. "01"—15-bit 555RGB. "10"—12-bit 444xRGB. "11"—12-bit x444RGB.
Bits 5:4	Test ramp output: "00"—Off. "01"—By column. "10"—By row. "11"—By frame.
Bit 3	Outputs RGB or YCbCr values are shifted 3 bits up. Use with R0x13A[5:4] to test LCDs with low color depth.
Bit 2	Averages two nearby chrominance bytes. See R0x19B
Bit 1	In YCbCr mode swap C and Y bytes. In RGB mode, swap odd and even bytes. See R0x19B
Bit 0	In YCbCr mode, swaps Cb and Cr channels. In RGB mode, swaps R and B channels. See R0x19B
R72:1—0x148 - Test pattern generator control (R/W)	
Default	0x0000
Description	This register enables test pattern generation at the input of the image processor. Values greater than "0" turn on the test pattern generator. The brightness of the flat color areas depends on the value programmed (from 6–1) in this register. The value 7 produces the color bar pattern. Value 0 selects the sensor image.
Bit 7	1: Forces WB digital gains to 1.0. 0: Normal operation.
Bits 2:0	Test pattern selection.
R76:1—0x14C - Defect correction—context A (R/W)	
Default	0x0000
Description	Context A register with defect correction, mode enables, and calibration bits.
Bit 2	Reserved
Bit 1	Reserved
Bit 0	Enables 2D defect correction.
R77:1—0x14D - Defect correction—context B (R/W)	
Default	0x0000
Description	Context B register with defect correction, mode enables, and calibration bits.
Bit 2	Reserved
Bit 1	Reserved
Bit 0	Enables 2D defect correction.
R153:1—0x199 - Line counter (R/O)	
Default	N/A
Description	Use line counter to determine the number of the line currently being output.
Bits 12:0	Line count.
R154:1—0x19A - Frame counter (R/O)	
Default	N/A
Description	Use frame counter to determine the index of the frame currently being output.
Bits 15:0	Frame count.

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Table 10: Colorpipe Register Description Address Page 1 (Continued)

Register Number Dec–Hex	Description
R155:1—0x19B - Output format control 2—context B (R/W)	
Default	0x0200
Description	Output format control 2B.
Bit 14	Output processed Bayer data.
Bit 13	Reserved.
Bit 12	
Bit 11	Enables embedding Rec. ITU-R BT.656 synchronization codes to the output data. See R0x13A
Bit 10	Entire image processing is bypassed and raw bayer is output directly. In YCbCr or RGB mode: 0: Normal operation, sensor core data flows through IFP. 1: Bypass IFP and output Imager data directly (full 10 bits). The image data still passes through the camera interface FIFO and the 10 bits are formatted to 2 output bytes through the camera interface; that is, 8 + 2. Data rate is effectively the same as default 16-bit /per pixel modes. AE/AWB, and so on, still function and control the sensor, though they are assuming some gain/correction through the colorpipe. See R0x13A
Bit 9	Invert output pixel clock. Inverts output pixel clock. By default, this bit is asserted. 0: Output data transitions on the rising edge of PIXCLK for capture by the receiver on the falling edge. 1: Output data transitions on the falling edge of PIXCLK for capture by the receiver on the rising edge
Bit 8	Enables RGB output. 0: Output YCbCr data. 1: Output RGB format data as defined by R0x19B[7:6]. See R0x13A
Bits 7:6	RGB output format: “00”—16-bit 565RGB. “01”—15-bit 555RGB. “10”—12-bit 444xRGB. “11”—12-bit x444RGB.
Bits 5:4	Test Ramp output: “00”—Off. “01”—By column. “10”—By row. “11”—By frame.
Bit 3	Output RGB or YCbCr values are shifted 3 bits up. Use with R0x13A[5:4] to test LCDs with low color depth.
Bit 2	Averages two nearby chrominance bytes. See R0x13A
Bit 1	In YCbCr mode swap C and Y bytes. In RGB mode, swap odd and even bytes. See R0x13A
Bit 0	In YCbCr mode, swaps Cb and Cr channels. In RGB mode, swaps R and B channels. See R0x13A
R159:1—0x19F - Reducer horizontal pan—context B (R/W)	
Default	0x0000
Description	Controls reducer horizontal pan in context B
Bit 14	0: MT9V111-compatible origin at X = 0. 1: Centered origin at 640 for more convenient zoom and resize.
Bits 10:0	X pan: Unsigned offset from x = 0 (Bit 14 = 0), or two’s complement from X = 640 (Bit 14 = 1).
R160:1—0x1A0 - Reducer horizontal zoom—context B (R/W)	
Default	0x0500
Description	Controls reducer horizontal width of zoom window for FOV in context B.
Bits 10:0	X zoom B. Must be ≥ X size B
R161:1—0x1A1 - Reducer horizontal output size—context B (R/W)	
Default	0x0500
Description	Controls reducer horizontal output size in context B.

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Table 10: Colorpipe Register Description Address Page 1 (Continued)

Register Number Dec–Hex	Description
Bits 10:0	X size B. Must be ≤ X zoom B.
R162:1—0x1A2 - Reducer vertical pan—context B (R/W)	
Default	0x0000
Description	Controls reducer vertical pan in context B.
Bit 14	0: MT9V111-compatible origin at Y = 0. 1: Centered origin at Y = 512 for more convenient zoom and resize.
Bits 10:0	Y pan: unsigned offset from Y = 0 (Bit 14 = 0), or two's complement from Y = 512 (Bit 14 = 1).
R163:1—0x1A3 - Reducer vertical zoom—context B (R/W)	
Default	0x0400
Description	Controls reducer vertical height of zoom window for FOV in context B.
Bits 10:0	Y zoom B. Must be ≥ Y size B.
R164:1—0x1A4 - Reducer vertical output size—context B (R/W)	
Default	0x0400
Description	Controls reducer vertical output size in context B.
Bits 10:0	Y size B. Must be ≤ Y zoom B.
R165:1—0x1A5 - Reducer horizontal pan—context A (R/W)	
Default	0x0000
Description	Controls reducer horizontal pan in context A.
Bit 14	0: MT9V111-compatible offset from X = 0. 1: Centered origin at 640 for more convenient zoom and resize.
Bits 10:0	X pan: Unsigned offset from X = 0 (Bit 14 = 0), or two's complement from X = 640 (Bit 14 = 1).
R166:1—0x1A6 - Reducer horizontal zoom—context A (R/W)	
Default	0x0500
Description	Controls reducer horizontal width of zoom window for FOV in context A.
Bits 10:0	X zoom A. Must be ≥ X size A.
R167:1—0x1A7 - Reducer horizontal output size—context A (R/W)	
Default	0x0280
Description	Controls reducer horizontal output size in context A.
Bits 10:0	X size A. Must be ≤ X zoom A.
R168:1—0x1A8 - Reducer vertical pan—context A (R/W)	
Default	0x0000
Description	Controls reducer vertical pan in context A.
Bit 14	0: MT9V111-compatible origin at Y = 0. 1: Centered origin at Y = 512 for more convenient zoom and resize.
Bits 10:0	Y pan: unsigned offset from y = 0 (Bit 14 = 0), or two's complement from Y = 512 (Bit 14 = 1).
R169:1—0x1A9 - Reducer vertical zoom—context A (R/W)	
Default	0x0400
Description	Controls reducer vertical height of zoom window for FOV in context A.
Bits 10:0	Y zoom A. Must be ≥ Y size A.
R170:1—0x1AA - Reducer vertical output size—context A (R/W)	
Default	0x0200
Description	Controls reducer vertical output size in context A.
Bits 10:0	Y sizeA. Must be ≤ Y zoom A.

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Table 10: Colorpipe Register Description Address Page 1 (Continued)

Register Number Dec–Hex	Description
R171:1—0x1AB - Reducer current horizontal zoom (R/O)	
Default	N/A
Description	Current horizontal zoom.
Bits 10:0	Current zoom Window Width. After automatic zoom (R0x1AF), copy R0x1AB to the snapshot X zoom register R0x1A6 (context A) or R0x1A0 (context B) so the snapshot has the same FOV as preview. Also copy to snapshot X size register R0x1A7 (context A) or R0x1A1 (context B) for largest snapshot.
Bits 15:12	Reserved. Mask off these bits before performing the above copy operation.
R172:1—0x1AC - Reducer current vertical zoom (R/O)	
Default	N/A
Description	Current vertical zoom.
Bits 10:0	Current zoom Window Height. After automatic zoom (R0x1AF), copy R0x1AC to the snapshot Y zoom register R0x1A9 (context A) or R0x1A3 (context B) so the snapshot will have the same FOV as preview. Also copy to snapshot X size register R0x1AA (context A) or R0x1A4 (context B) for largest snapshot.
Bits 15:12	Reserved. Mask off these bits before performing the above copy operation.
R174:1—0x1AE - Reducer zoom step size (R/W)	
Default	0x0504
Description	Zoom step sizes. Should be a multiple of the aspect ratio 5:4 for SXGA or 4:3 VGA or 11:9 for CIF.
Bits 15:8	Zoom step size in X.
Bits 7:0	Zoom step size in Y.
R175:1—0x1AF - Reducer zoom control (R/W)	
Default	0x0010
Description	Resize interpolation and zoom control.
Bit 9	Starts automatic “zoom out” in step sizes defined in R0x1AE.
Bit 8	Starts automatic “zoom in” in step sizes defined in R0x1AE.
Bit 6	
Bit 5	
Bit 4	
Bit 3	Auto switch to classic interpolation at full resolution.
Bit 1	Reserved.
Bit 0	Reserved.
R179:1—0x1B3 - Global clock control (R/W)	
Default	0x0002
Description	Configures assorted aspects of the clock controller.
Bits 15:2	Not used.
Bit 1	Tri-states signals in standby mode.
Bit 0	
R182:1—0x1B6 - Lens vertical red Knees 6 and 5 (R/W)	

R200:1—0x1C8 - Global context control (R/W)	
Default	0x0000
Description	Defines sensor and colorpipe context for current frame. Registers R0x0C8, R0x1C8, and R0x2C8 are shadows of each other. See description in R0x2C8. It is recommended that all updates to R0xnC8 are handled by means of a write to R0x2C8.
Bit 15:0	See R0x2C8[15:0].

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Table 10: Colorpipe Register Description Address Page 1 (Continued)

Register Number Dec–Hex	Description
R226:1—0x1E2 - Effects mode (R/W)	
Default	0x7000
Description	This register specifies which of several special effects to apply to each pixel passing through the pixel pipe.
Bits 15:8	Solarization threshold.
Bits 2:0	Specification of the effects mode. "000"—No effect (pixels pass through unchanged). "001"—Monochrome (chromas set to 0). "010"—Sepia (chromas set to the value in the Effects Sepia register). "011"—Negative (all color channels inverted). "100"—Solarize (luma conditionally inverted). "101"—Solarize2 (luma conditionally inverted, chromas inverted when luma inverted).
R227:1—0x1E3 - Effects sepia (R/W)	
Default	0xB023
Description	This register specifies the chroma values for the sepia effect. In sepia mode, the chroma values of each pixel are set to this value. By default, this register contains a brownish color, but it can be set to an arbitrary color.
Bit 15	Sign of Cb.
Bits 14:8	Magnitude of Cb in 0.7 fixed point.
Bit 7	Sign of Cr.
Bits 6:0	Magnitude of Cr in 0.7 fixed point.
R240:1—0x1F0 - Page map (R/W)	
Default	0x0000
Description	This register specifies the register address page for the two-wire interface protocol.
Bits 2:0	Page Address: "000"—Sensor address page. "001"—Colorpipe address page. "010"—Camera control address page.
R241:1—0x1F1 - Byte-wise address (R/W)	
Default	N/A
Description	Special address to perform 8-bit reads and writes to the sensor. For additional information, see "Two-Wire Serial Interface Sample" on page 61 and "Appendix A – Serial Bus Description" on page 59.

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Camera Control Registers

Register WRITEs reach the camera control registers immediately. For non-AE/AWB/CCM registers, register writes take effect immediately.

For AE/AWB and CCM registers, the effects of register writes are dependent on the state of the AE and AWB engines. It may take from zero to many frames for the changes to take effect. Monitor AWB/CCM changes by watching for stable settings in R0x212 (current CCM position), in R0x213 (current AWB red channel), and in R0x214 (current AWB blue channel). Monitor AE changes by watching register R0x24C (AE current luma exposure), and register R0x262 (AE digital gains monitor).

Table 11: Camera Control Register Description

Register Number Dec—Hex	Description
R38:2—0x226 - Auto exposure window horizontal boundaries (R/W)	
Default	0x8000
Description	This register specifies the left and right boundaries of the window used by the AE measurement engine. The values programmed in the registers are the fractional percentage, where 128 (decimal) is the right-most edge of the frame, 64 (decimal) is the middle of the frame, and 0 is the left-most edge of the frame.
Bits 15:8	Right window boundary.
Bits 7:0	Left window boundary.
R39:2—0x227 - Auto exposure window vertical boundaries (R/W)	
Default	0x8008
Description	This register specifies the top and bottom boundaries of the window used by the AE measurement engine. The values programmed in the registers are the fractional percentage, where 128 (decimal) is the bottom edge of the frame, 64 (decimal) is the middle of the frame, and 0 is the top edge of the frame.
Bits 15:8	Bottom window boundary.
Bits 7:0	Top window boundary.
R42:2—0x22A - WB zone validity limits (R/W)	
R43:2—0x22B - Auto exposure center window horizontal boundaries (R/W)	
Default	0x6020
Description	This register specifies the left and right boundaries of the window used by the AE measurement engine in backlight compensation mode. The values programmed in the registers are the fractional percentage, where 128 (decimal) is the right-most edge of the frame, 64 (decimal) is the middle of the frame, and 0 is the left-most edge of the frame.
Bits 15:8	Right window boundary.
Bits 7:0	Left window boundary.
R44:2—0x22C - Auto exposure center window vertical boundaries (R/W)	
Default	0x6020

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Table 11: Camera Control Register Description (Continued)

Register Number Dec—Hex	Description
Description	This register specifies the top and bottom boundaries of the window used by the AE measurement engine in backlight compensation mode. The values programmed in the registers are the fractional percentage, where 128 (decimal) is the bottom edge of the frame, 64 (decimal) is the middle of the frame, and 0 is the top edge of the frame.
Bits 15:8	Bottom window boundary.
Bits 7:0	Top window boundary.
R45:2—0x22D - AWB window boundaries (R/W)	
Default	0xF0A0
Description	This register specifies the boundaries of the window used by the AWB measurement engine. Essentially, it describes the AWB measurement window in terms relative to the size of the image—horizontally, in units of 1/10ths of the width of the image; vertically, in units of 1/16 of the height of the image. So although the positioning is highly quantized, the window remains roughly in place as the resolution changes.
Bits 15:12	Bottom window boundary (in units of 1 block).
Bits 11:8	Top window boundary (in units of 1 block).
Bits 7:4	Right window boundary (in units of 2 blocks).
Bits 3:0	Left window boundary (in units of 2 blocks).
R46:2—0x22E - Auto exposure target and precision control (R/W)	
Default	0x0C4A
Description	This register specifies the luma target of the AE algorithm and the size of the window/range around the target in which no AE adjustment is made. This window is centered on target, but the value programmed in the register is 1/2 of the window size.
Bits 15:8	Half-size of the AE stability window/range.
Bits 7:0	Luma value of the AE target.
R47:2—0x22F - Auto exposure speed and sensitivity control—context A (R/W)	
Default	0xDF20
Description	This register specifies the speed and sensitivity to changes of AE in context A.
Bit 15	Reserved.
Bit 14	
Bits 13:12	
Bit 11	Reserved.
Bit 10	Reserved.
Bit 9	Reserved.
Bits 8:6	Factor of reduction of the difference between current luma and target luma. In one adjustment AE advances from current luma to target as follows: “000”—1/4 way going down, 1/8 going up. “001”—1/4 way in both directions. “010”—1/2 way in both directions. “011”—1/2 way going down, 1/4 going up. “100”—All the way in both directions (fast adaptation!). “101”—3/4 way in both directions. “110”—7/8 way in both directions. “111”—Reserved. Currently the same as “100”
Bit 5	Reserved.
Bits 4:3	Auto exposure luma is updated every N frames, where N is given by this field.

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Table 11: Camera Control Register Description (Continued)

Register Number Dec—Hex	Description
Bits 2:0	Hysteresis control through time-averaged smoothing of luma data. Luma measurements for AE are time-averaged as follows: "000"—Auto exposure luma = current luma. "001"—Auto exposure luma = 1/2 current luma + 1/2 buffered value. "010"—Auto exposure luma = 1/4 current luma + 3/4 buffered value. "011"—Auto exposure luma = 1/8 current luma + 7/8 buffered value. "100"—Auto exposure luma = 1/16 current luma + 15/16 buffered value. "101"—Auto exposure luma = 1/32 current luma + 31/32 buffered value. "110"—Auto exposure luma = 1/64 current luma + 63/64 buffered value. "111"—Auto exposure luma = 1/128 current luma + 127/128 buffered value.

R55:2—0x237 - Auto exposure gain zone limits (R/W)

R57:2—0x239 - Auto exposure line size—context A (R/W)

R91:2—0x25B - Flicker control (R/W)	
Default	0x0002
Description	Primary flicker control register.
Bit 15	(Read only) 50Hz/60Hz detected. 0: 50Hz detected. 1: 60Hz detected.
Bit 2	
Bit 1	When in "manual" flicker mode (R0x25B[0] = 1), defines which flicker frequency to avoid. 0: Forces 50Hz detection. 1: Forces 60Hz detection.
Bit 0	0: Auto flicker detection. 1: Manual mode.
R98:2—0x262 - Auto exposure digital gains monitor (R/W*)	
Default	N/A
Description	These digital gains are applied within the IFP; they are independent of the Imager gains.
Bits 15:8	Post-lens-correction digital gain (*writable if AE is disabled).
Bits 7:0	Pre-lens-correction digital gain (*writable if AE is disabled).

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Table 11: Camera Control Register Description (Continued)

Register Number Dec—Hex	Description
R103:2—0x267 - Auto exposure digital gain limits (R/W)	
Default	0x4010
Description	This register specifies the upper limits of the digital gains used by the AE algorithm. The values programmed to this register are 16 times the absolute gain values. The value of 16 represents the gain 1.0.
Bits 15:8	Maximum limit on post-lens-correction digital gain.
Bits 7:0	Maximum limit on pre-lens-correction digital gain.
R135:2—0x287 - Auto exposure gain Zone 6 deltas (R/W)	
R156:2—0x29C - Auto exposure speed and sensitivity control—context B (R/W)	
Default	0xDF20
Description	This register specifies the speed and sensitivity to AE changes in context B.
Bit 15	Reserved.
Bit 14	
Bits 13:12	
Bit 11	Reserved.
Bit 10	Reserved.
Bit 9	Reserved.
Bits 8:6	Factor of reduction of the difference between current luma and target luma. In one adjustment, AE advances from current luma to target as follows: “000”—1/4 way going down, 1/8 going up. “001”—1/4 way in both directions. “010”—1/2 way in both directions. “011”—1/2 way going down, 1/4 going up. “100”—All the way in both directions (fast adaptation!). “101”—3/4 way in both directions. “110”—7/8 way in both directions. “111”—Reserved. Currently the same as “100.”
Bit 5	Reserved.
Bits 4:3	Auto exposure luma is updated every N frames, where N is given by this field.

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Table 11: Camera Control Register Description (Continued)

Register Number Dec—Hex	Description
Bits 2:0	Hysteresis control through time-averaged smoothing of luma data. Luma measurements for AE are time-averaged as follows: "000"—Auto exposure luma = current luma. "001"—Auto exposure luma = 1/2 current luma + 1/2 buffered value. "010"—Auto exposure luma = 1/4 current luma + 3/4 buffered value. "011"—Auto exposure luma = 1/8 current luma + 7/8 buffered value. "100"—Auto exposure luma = 1/16 current luma + 15/16 buffered value. "101"—Auto exposure luma = 1/32 current luma + 31/32 buffered value. "110"—Auto exposure luma = 1/64 current luma + 63/64 buffered value. "111"—Auto exposure luma = 1/128 current luma + 127/128 buffered value.
R180:2—Reserved	
R200:2—0x2C8 - Global context control (R/W)	
Default	0x0000
Description	Defines sensor and colorpipe context for current frame. Context A is typically used to define preview or viewfinder mode, while context B is typically used for snapshots. The bits of this register *directly* control the respective functions, so care must be taken when writing to this register if a bad frame is to be avoided during the context switch.
Bit 15	Controls assertion of sensor restart on update of global context control register. This helps ensure that the very next frame is generated with the new context (a problem with regard to exposure due to the rolling shutter). This bit is automatically cleared once the restart has occurred. 0: Do not restart sensor. 1: Restart sensor.
Bit 14	Reserved.
Bit 13	Reserved.
Bit 12	Defect correction context. See R0x14C and R0x14D. 0: Context A 1: Context B
Bit 11	
Bit 10	Resize/zoom context. Switch resize/zoom contexts: 0: Context A 1: Context B
Bit 9	Output format control 2 context. See R0x13A and R0x19B. 0: Context A 1: Context B
Bit 8	Gamma table context. 0: Context A 1: Context B
Bit 7	Arm xenon flash.
Bit 6	Blanking control. This is primarily for use by the internal sequencer when taking automated (for example, flash) snapshots. Setting this bit stops frames from being sent over the BT656 external pixel interface. This is useful for ensuring that the desired frame during a snapshot sequence is the only frame captured by the host. 0: Do not blank frames to host. 1: Blank frames to host
Bit 5	Reserved.
Bit 4	Reserved.
Bit 3	Sensor read mode context (skip mode, power mode, see R0x33:0 and R0x32:0. 0: Context A 1: Context B

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Table 11: Camera Control Register Description (Continued)

Register Number Dec—Hex	Description
Bit 2	LED flash ON: 0: Turn off LED Flash 1: Turn on LED Flash
Bit 1	Vertical blanking context: 0: Context A 1: Context B
Bit 0	Horizontal blanking context: 0: Context A 1: Context B
R240:2—0x2F0 - Page map (R/W)	
Default	0x0000
Description	This register specifies the register address page for the two-wire interface protocol.
Bits 2:0	Page address: “000”—Sensor address page. “001”—Colorpipe address page. “010”—Camera control address page.
R241:2—0x2F1 - Byte-wise address (R/W)	
Default	N/A
Description	Special address to perform 8-bit READs and WRITEs to the sensor. For additional information, see “Two-Wire Serial Interface Sample” on page 61 and “Appendix A – Serial Bus Description” on page 59.

Note: Registers marked “(R/W*)” are normally read-only (R/O) registers, except under special circumstances (detailed in the register description), when some or all bits of the register become read-writable (R/W).

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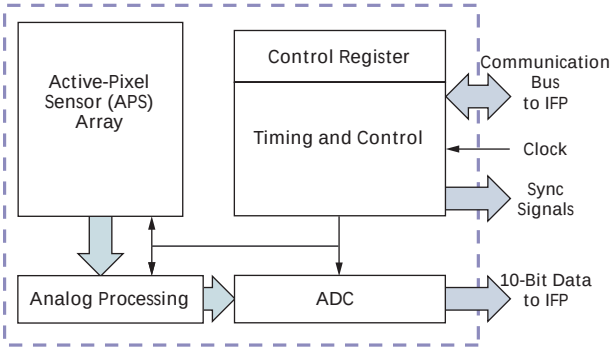
Sensor Core Overview

The sensor consists of a pixel array of 1316 x 1048 total, an analog readout chain, 10-bit ADC with programmable gain and black offset, and timing and control.

Figure 6: Sensor Core Block Diagram

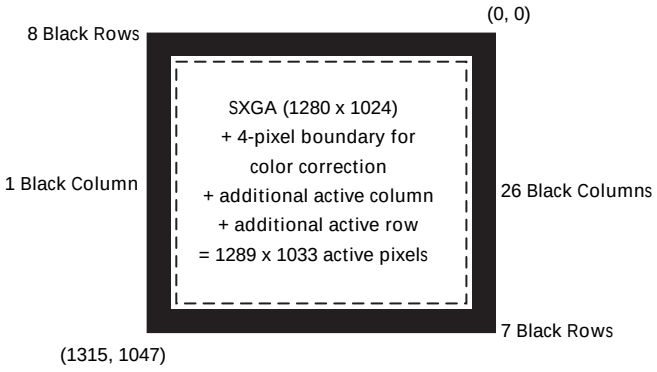


Pixel Data Format

Pixel Array Structure

The MT9M131 sensor core pixel array is configured as 1316 columns by 1048 rows (shown in Figure 7). The first 26 columns and the first 8 rows of pixels are optically black, and can be used to monitor the black level. The last column and the last 7 rows of pixels also are optically black. The black row data is used internally for the automatic black level adjustment. However, the first 8 black rows can also be read out by setting the sensor to raw data output mode (R0x022). There are 1289 columns by 1033 rows of optically-active pixels that provide a 4-pixel boundary around the SXGA (1280 x 1024) image to avoid boundary effects during color interpolation and correction. The additional active column and additional active row are used to enable horizontally and vertically mirrored readout to start on the same color pixel.

Figure 7: Pixel Array Description



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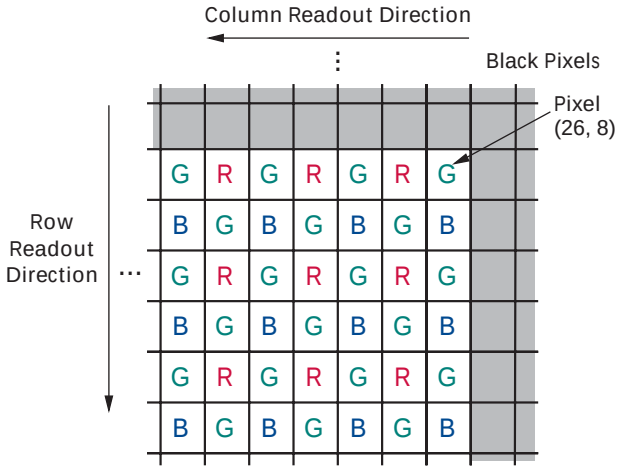
The MT9M131 sensor core uses an RGB Bayer color pattern, as shown in Figure 8. The even-numbered rows contain green and red color pixels, and odd-numbered rows contain blue and green color pixels. Even-numbered columns contain green and blue color pixels; odd-numbered columns contain red and green color pixels. Because there are odd numbers of rows and columns, the color order can be preserved during mirrored readout.

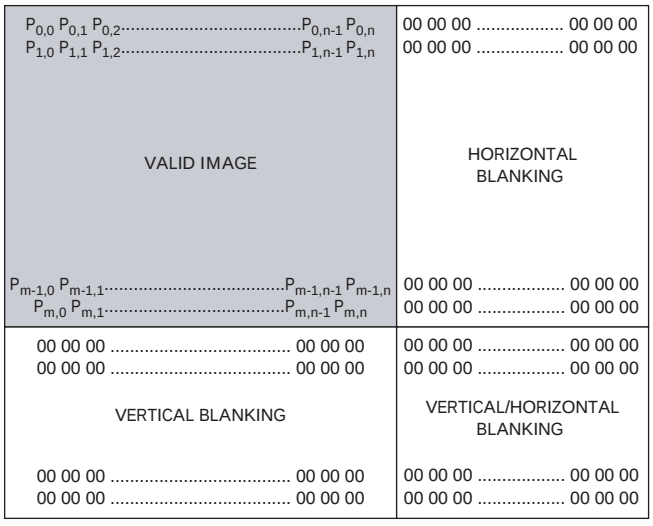
Figure 8: Pixel Color Pattern Detail (Top Right Corner)



Output Data Format

The MT9M131 sensor core image data is read out in a progressive scan. Valid image data is surrounded by horizontal blanking and vertical blanking, shown in Figure 9. LV is HIGH during the shaded region of the figure. FV timing is described in "Appendix A – Serial Bus Description" on page 59.

Figure 9: Spatial Illustration of Image Readout



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Sensor Core Register List

Table 12: Sensor Registers (Address Page 0)
0 = "Don't Care" bit; d = R/W bit; ? = R/O bit. The exceptions: Rx00:0 and R0xFF:0, which are hardwired R/O binary values.

Register Number Dec (Hex)	Register Name	Data Format (Binary)	Default Value Dec (Hex)
0 (0x00)	Chip version	0001 0100 0011 1010 (LSB)	5178 (0x143A)
1 (0x01)	Row start	0000 0ddd dddd dddd	12 (0x000C)
2 (0x02)	Column start	0000 0ddd dddd dddd	30 (0x001E)
3 (0x03)	Window height	0000 0ddd dddd dddd	1024 (0x0400)
4 (0x04)	Window width	0000 0ddd dddd dddd	1280 (0x0500)
5 (0x05)	Horizontal blanking—context B	00dd dddd dddd dddd	388 (0x0184)
6 (0x06)	Vertical blanking—context B	0ddd dddd dddd dddd	42 (0x002A)
7 (0x07)	Horizontal blanking—context A	00dd dddd dddd dddd	190 (0x00BE)
8 (0x08)	Vertical blanking—context A	0ddd dddd dddd dddd	17 (0x0011)
9 (0x09)	Shutter width	dddd dddd dddd dddd	537 (0x0219)
10 (0x0A)	Row speed	ddd0 000d dddd dddd	17 (0x0011)
11 (0x0B)	Extra delay	00dd dddd dddd dddd	0 (0x0000)
12 (0x0C)	Shutter delay	00dd dddd dddd dddd	0 (0x0000)
13 (0x0D)	Reset	d000 00dd 00dd dddd	8 (0x0008)
32 (0x20)	Read mode—context B	dd00 0ddd dddd dddd	768 (0x0300)
33 (0x21)	Read mode—context A	0000 0d00 0000 dd00	1036 (0x040C)
34 (0x22)			297 (0x0129)
35 (0x23)	Flash control	??dd dddd dddd dddd	1544 (0x0608)
36 (0x24)			32875 (0x806B)
43 (0x2B)	Green1 gain	0000 0ddd dddd dddd	32 (0x0020)
44 (0x2C)	Blue gain	0000 0ddd dddd dddd	32 (0x0020)
45 (0x2D)	Red gain	0000 0ddd dddd dddd	32 (0x0020)
46 (0x2E)	Green2 gain	0000 0ddd dddd dddd	32 (0x0020)
47 (0x2F)	Global gain	0000 0ddd dddd dddd	32 (0x0020)
48 (0x30)			1066 (0x042A)
49 (0x31)	Reserved	–	7168 (0x1C00)
50 (0x32)	Reserved	–	0 (0x0000)
51 (0x33)	Reserved	–	841 (0x0349)
52 (0x34)	Reserved	–	49177 (0xC019)
54 (0x36)	Reserved	–	61680 (0xF0F0)
55 (0x37)	Reserved	–	0 (0x0000)
59 (0x3B)	Reserved	–	33 (0x0021)
60 (0x3C)	Reserved	–	6688 (0x1A20)
61 (0x3D)	Reserved	–	8222 (0x201E)
62 (0x3E)	Reserved	–	8224 (0x2020)
63 (0x3F)	Reserved	–	8224 (0x2020)
64 (0x40)	Reserved	–	8220 (0x201C)
65 (0x41)			215 (0x00D7)
66 (0x42)	Reserved	–	1911 (0x0777)
89 (0x59)			12 (0x000C)
90 (0x5A)	Reserved	–	49167 (0xC00F)

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Table 12: Sensor Registers (Address Page 0) (Continued)
0 = "Don't Care" bit; d = R/W bit; ? = R/O bit. The exceptions: Rx00:0 and R0xFF:0, which are hardwired R/O binary values.

Register Number Dec (Hex)	Register Name	Data Format (Binary)	Default Value Dec (Hex)
91 (0x5B)			N/A
92 (0x5C)			N/A
93 (0x5D)			N/A
94 (0x5E)			N/A
95 (0x5F)			8989 (0x231D)
96 (0x60)			128 (0x0080)
97 (0x61)			0 (0x0000)
98 (0x62)			0 (0x0000)
99 (0x63)			0 (0x0000)
100 (0x64)			0 (0x0000)
101 (0x65)	Reserved	–	0 (0x0000)
112 (0x70)	Reserved	–	31498 (0x7B0A)
113 (0x71)	Reserved	–	31498 (0x7B0A)
114 (0x72)	Reserved	–	6414 (0x190E)
115 (0x73)	Reserved	–	6159 (0x180F)
116 (0x74)	Reserved	–	22322 (0x5732)
117 (0x75)	Reserved	–	22068 (0x5634)
118 (0x76)	Reserved	–	29493 (0x7335)
119 (0x77)	Reserved	–	12306 (0x3012)
120 (0x78)	Reserved	–	30978 (0x7902)
121 (0x79)	Reserved	–	29958 (0x7506)
122 (0x7A)	Reserved	–	30474 (0x770A)
123 (0x7B)	Reserved	–	30729 (0x7809)
124 (0x7C)	Reserved	–	32006 (0x7D06)
125 (0x7D)	Reserved	–	12560 (0x3110)
126 (0x7E)	Reserved	–	126 (0x007E)
128 (0x80)	Reserved	–	127 (0x007F)
129 (0x81)	Reserved	–	127 (0x007F)
130 (0x82)	Reserved	–	22282 (0x570A)
131 (0x83)	Reserved	–	22539 (0x580B)
132 (0x84)	Reserved	–	18188 (0x470C)
133 (0x85)	Reserved	–	18446 (0x480E)
134 (0x86)	Reserved	–	23298 (0x5B02)
135 (0x87)	Reserved	–	92 (0x005C)
200 (0xC8)	Context control	d000 0000 d000 dddd	0 (0x0000)
240 (0xF0)	Page map	0000 0000 0000 0ddd	0 (0x0000)
241 (0xF1)	Byte-wise address	Reserved	Reserved
245 (0xF5)	Reserved	–	2047 (0x07FF)
246 (0xF6)	Reserved	–	2047 (0x07FF)
247 (0xF7)	Reserved	–	0 (0x0000)
248 (0xF8)	Reserved	–	0 (0x0000)
249 (0xF9)	Reserved	–	124 (0x007C)
250 (0xFA)	Reserved	–	0 (0x0000)
251 (0xFB)	Reserved	–	0 (0x0000)

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Table 12: Sensor Registers (Address Page 0) (Continued)
0 = "Don't Care" bit; d = R/W bit; ? = R/O bit. The exceptions: Rx00:0 and R0xFF:0, which are hardwired R/O binary values.

Register Number Dec (Hex)	Register Name	Data Format (Binary)	Default Value Dec (Hex)
252 (0xFC)	Reserved	–	0 (0x0000)
253 (0xFD)	Reserved	–	0 (0x0000)
255 (0xFF)	Chip version	0001 0100 0011 1010	5178 (0x143A)

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Sensor Core Registers

Sensor registers are generally updated before the next FV is asserted. See the column titled "Synced to Frame Start" in Table 13 for per-register information.

Note: **Notation used in the sensor core register description table:**

Sync'd to frame start

0 = Not applicable, for example, read-only register.
N = No. The register value is updated and used immediately.
Y = Yes. The register value is updated at next frame start as long as the synchronize changes bit is "0." Frame start is defined as when the first dark row is read out. By default, this is 8 rows before FV goes HIGH.

Bad frame

A bad frame is a frame where all rows do not have the same integration time, or offsets to the pixel values changed during the frame.
0 = Not applicable, for example, read-only register.
N = No. Changing the register value does not produce a bad frame.
Y = Yes. Changing the register value might produce a bad frame.
YM = Yes, but the bad frame is masked out unless the "show bad frames" feature is enabled.

Read/Write

R—Read-only register/bit.
W—Read/write register/bit.

Table 13: Sensor Core Register Descriptions

Bit Field	Description	Default (Hex)	Synced to Frame Start	Bad Frame	Read/ Write
R0:0—0x000 - Chip version (R/O)					
Bits 15:0	Hardwired read-only.	0x143A			R
R1:0—0x001 - Row start					
Bits 10:0 Row start	The first row to be read out (not counting dark rows that may be read). To window the image down, set this register to the starting Y value. Setting a value less than 8 is not recommended since the dark rows should be read using R0x022.	0xC	Y	YM	W
R2:0—0x002 - Column start					
Bits 10:0 Col start	The first column to be read out (not counting dark columns that may be read). To window the image down, set this register to the starting X value. Setting a value below 0x18 is not recommended since readout of dark columns should be controlled by R0x022.	0x1E	Y	YM	W
R3:0—0x003 - Window height					
Bits 10:0 Window height	Number of rows in the image to be read out (not counting dark rows or border rows that may be read).	0x400	Y	YM	W
R4:0—0x004 - Window width					
Bits 10:0 Window width	Number of columns in image to be read out (not counting dark columns or border columns that may be read).	0x500	Y	YM	W
R5:0—0x005 - Horizontal blanking—context B					

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Table 13: Sensor Core Register Descriptions (Continued)

Bit Field	Description	Default (Hex)	Synced to Frame Start	Bad Frame	Read/ Write
Bits 10:0 Horizontal blanking B	Number of blank columns in a row when context B is chosen (R0x0C8[0] = 1). If set smaller than the minimum value, the minimum value is used. With default settings, the minimum horizontal blanking is 202 columns in full-power readout mode and 114 columns in low-power readout mode.	0x184	Y	YM	W
R6:0—0x006 - Vertical blanking—context B					
Bits 14:0 Vertical Blanking B	Number of blank rows in a frame when context B is chosen (R0x0C8[1] = 1). This number must be equal to or larger than the number of dark rows read out in a frame specified by R0x022.	0x2A	Y	N	W
R7:0—0x007 - Horizontal blanking—context A					
Bits 10:0 Horizontal Blanking A	Number of blank columns in a row when context A is chosen (R0x0C8[0] = 0). The extra columns are added at the beginning of a row. If set smaller than the minimum value, the minimum value is used. With default settings, the minimum horizontal blanking is 202 columns in full-power readout mode and 114 columns in low-power readout mode.	0xBE	Y	YM	W
R8:0—0x008 - Vertical blanking—context A					
Bits 14:0 Vertical blanking A	Number of blank rows in a frame when context A is chosen (R0x0C8[1] = 1). This number must be equal to or larger than the number of dark rows read out in a frame specified by R0x022.	0x11	Y	N	W
R9:0—0x009 - Shutter width					
Bits 15:0 Shutter width	Integration time in number of rows. In addition to this register, the shutter delay register (R0x00C) and the overhead time influences the integration time for a given row time.	0x219	Y	N	W
R10:0—0x00A - Row speed					
Bits 15:13	Reserved.	–	–	–	–
Bit 8 Invert pixel clock	Invert pixel clock. When set, LV, FV, and DATA_OUT are set to the falling edge of PIXCLK. When clear, they are set to the rising edge if there is no pixel clock delay.	0x0	N	0	W
Bits 7:4 Delay pixel clock	Delay PIXCLK in half-master-clock cycles. When set, the pixel clock can be delayed in increments of half-master- clock cycles compared to the synchronization of FV, LV, and DATA_OUT.	0x1	N	0	W
Bits 3:0 Pixel clock speed	Pixel clock period in master clocks when full-power readout mode is used (R0x020/0x021, bit 10 = 0). In this case, the ADC clock has twice the clock period. If low-power readout mode is used, the pixel clock period is automatically doubled, so the ADC clock period remains the same for one programmed register value. The value “0” is not allowed, and “1” is used instead.	0x1	Y	YM	W
R11:0—0x00B - Extra delay					
Bits 13:0 Extra delay	Extra blanking inserted between frames specified in pixel clocks. Can be used to get a more exact frame rate. For integration times less than a frame, however, it might affect the integration times for parts of the image.	0x0	Y	0	W

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Table 13: Sensor Core Register Descriptions (Continued)

Bit Field	Description	Default (Hex)	Synced to Frame Start	Bad Frame	Read/ Write
R12:0—0x00C - Shutter delay					
Bits 10:0 Shutter delay	The amount of time from the end of the sampling sequence to the beginning of the pixel reset sequence. This variable is automatically halved in low-power readout mode, so the time in use remains the same. This register has an upper value defined by the fact that the reset needs to finish prior to readout of that row to prevent changes in the row time.	0x0	Y	N	W
R13:0—0x00D - Reset					
Bit 15 Synchronize changes	0: Normal operation, updates changes to registers that affect image brightness at the next frame boundary (integration time, integration delay, gain, horizontal blanking and vertical blanking, window size, row/column skip, or row mirror. 1: Do not update any changes to these settings until this bit is returned to "0." All registers that are frame synchronized are affected by this bit setting.	0x0	N	0	W
Bit 9 Restart bad frames	When set, a forced restart occurs when a bad frame is detected. This can shorten the delay when waiting for a good frame because the delay when masking out a bad frame is the integration time rather than the full frame time.	0x0	N	0	W
Bit 8 Show bad frames	0: Only output good frames (default) A bad frame is defined as the first frame following a change to: window size or position, horizontal blanking, pixel clock speed, zoom, row or column skip, or mirroring. 1: Output all frames (including bad frames)	0x0	N	0	W
Bit 5 Reset SOC	This reset signal is fed directly to the SOC part of the chip, and has no functionality in a stand-alone sensor.	0x0	N	0	W
Bit 4 Output disable	When set, the output signals are tri-stated.	0x0	N	0	W
Bit 3 Chip enable	0: Stop sensor readout. 1: Normal operation. When this is returned to "1," sensor readout restarts and begins resetting the starting row in a new frame. To reduce the digital power, the master clock to the sensor can be disabled or STANDBY can be used.	0x1	N	YM	W
Bit 2 Analog standby	0: Normal operation (default) 1: Disable analog circuitry. Whenever this bit is set to "1" the chip enable bit (bit 3) should be set to "0."	0x0	N	YM	W
Bit 1 Restart	Setting this bit causes the sensor to abandon the current frame and start resetting the first row. The delay before the first valid frame is read out equals the integration time. This bit always reads "0."	0x0	N	YM	W
Bit 0 Reset	Setting this bit puts the sensor in reset mode; this sets the sensor to its default power-up state. Clearing this bit resumes normal operation.	0x0	N	YM	W
R32:0—0x020 - Read mode—context B					
Bit 15 XOR Line Valid	0: LV determined by bit 9. Ineffective if "Continuous" LV is set. 1: LV = Continuous LV XOR FV.	0x0	N	0	W
Bit 14 Continuous Line Valid	0: Normal LV (default, no line valid during vertical blanking). 1: "Continuous" LV (continue producing LV during vertical blanking).	0x0	N	0	W

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Table 13: Sensor Core Register Descriptions (Continued)

Bit Field	Description	Default (Hex)	Synced to Frame Start	Bad Frame	Read/ Write
Bit 10 Power readout mode—context B	When read mode context B is selected (R0x0C8[3] = 1): 0: Full-power readout mode, maximum readout speed. 1: Low-power readout mode. Maximum readout frequency is now half of the master clock, and the pixel clock is automatically adjusted as described for the pixel clock speed register.	0x0	Y	YM	W
Bit 9 Show border	This bit indicates whether to show the border enabled by bit 8. When bit 8 is "0," this bit has no meaning. When bit 8 is "1," this bit decides whether the border pixels should be treated as extra active pixels (1) or extra blanking pixels (0).	0x1	N	0	W
Bit 8 Oversized	When this bit is set, a 4-pixel border is output around the active image array independent of readout mode (skip, zoom, mirror, and so on). Setting this bit therefore adds 8 to the numbers of rows and columns in the frame.	0x1	Y	YM	W
Bit 7		0x0	Y	YM	W
Bit 5 Column skip 4x	0: Normal readout. 1: Read out 2 columns, and then skip 6 columns (as with rows).	0x0	Y	YM	W
Bit 4 Row skip 4x	0: Normal readout. 1:Readout 2 rows, and then skip 6 rows (that is, row 8, row 9, row 16, row 17...).	0x0	Y	YM	W
Bit 3 Column skip 2x—context B	When read mode context B is selected (R0x0C8[3] = 1): 0: Normal readout. 1: Read out 2 columns, and then skip 2 columns (as with rows).	0x0	Y	YM	W
Bit 2 Row skip 2x—context B	When read mode context B is selected (R0x0C8[3] = 1): 0: Normal readout. 1: Read out 2 rows, then skip 2 rows (that is, row 8, row 9, row 12, row 13...).	0x0	Y	YM	W
Bit 1 Mirror columns	Read out columns from right to left (mirrored). When set, column readout starts from column (Col Start + Col size) and continues down to (Col Start + 1). When clear, readout starts at Col Start and continues to (Col Start + Col size 1). This ensures that the starting color is maintained.	0x0	Y	YM	W
Bit 0 Mirror rows	Read out rows from bottom to top (upside down). When set, row readout starts from row (Row Start + Row size) and continues down to (Row Start + 1). When clear, readout starts at Row Start and continues to (Row Start + Row size 1). This ensures that the starting color is maintained.	0x0	Y	YM	W
R33:0—0x021 - Read mode—context A					
Bit 10 Power readout mode—context A	When read mode context A is selected (R0x0C8[3] = 0): 0: Full-power readout mode, maximum readout speed. 1: Low-power readout mode. Maximum readout frequency is now half of the master clock, and the pixel clock is automatically adjusted as described for the pixel clock speed register.	0x1	Y	YM	W
Bit 3 Column skip 2x—context A	When read mode context A is selected (R0x0C8[3] = 0): 0: Normal readout. 1: Readout 2 columns, and then skip 2 columns (as with rows).	0x1	Y	YM	W
Bit 2 Row skip 2x—context A	When read mode context A is selected (R0x0C8[3] = 0): 0: Normal readout. 1: Readout 2 rows, and then skip 2 rows (that is, row 8, row 9, row 12, row 13...).	0x1	Y	YM	W

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Table 13: Sensor Core Register Descriptions (Continued)

Bit Field	Description	Default (Hex)	Synced to Frame Start	Bad Frame	Read/ Write
R35:0—0x023 - Flash control					
Bit 15 Flash Strobe	Read-only bit that indicates whether FLASH_STROBE is enabled.	0x0	0	0	R
Bit 14	Reserved.	—	—	—	—
Bit 13 xenon flash	Enable xenon flash. When set, FLASH_STROBE output is pulsed HIGH for the programmed period during vertical blanking. This is achieved by keeping the integration time equal to one frame and the pulse width less than the vertical blanking time.	0x0	Y	N	W
Bits 12:11 Frame delay	Delay of the flash pulse measured in frames.	0x0	N	N	W
Bit 10 End of reset	0: In xenon mode, the flash should be enabled after the readout of a frame. 1: In xenon mode, the flash should be triggered after the resetting of a frame.	0x1	N	N	W
Bit 9 Every frame	0: Flash should be enabled for 1 frame only. 1: Flash should be enabled every frame.	0x1	N	N	W
Bit 8 LED flash	Enables LED flash. When set, FLASH_STROBE goes on prior to the start of a frame reset. When disabled, the FLASH_STROBE remains HIGH until readout of the current frame completes.	0x0	Y	Y	W
Bits 7:0 xenon count	Length of FLASH_STROBE pulse when xenon flash is enabled. The value specifies the length in 1,024 master clock cycle increments.	0x08	N	N	W
R43:0—0x02B - Green1 gain					
Bits 6:0 Initial gain	Initial gain = bits (6:0) x 0.03125.	0x20	Y	N	W
Bits 8:7 Analog gain	Analog gain = (Bit 8 + 1) x (Bit 7 + 1) x initial gain (each bit gives 2x gain).	0x0	Y	N	W
Bits 10:9 Digital gain	Total gain = (Bit 9 + 1) x (Bit 10 + 1) x analog gain (each bit gives 2X gain).	0x0	Y	N	W
R44:0—0x02C - Blue gain					
Bits 10:9 Digital gain	Total gain = (Bit 9 + 1) x (Bit 10 + 1) x analog gain (each bit gives 2X gain).	0x0	Y	N	W
Bits 8:7 Analog gain	Analog gain = (Bit 8 + 1) x (Bit 7 + 1) x initial gain (each bit gives 2X gain).	0x0	Y	N	W
Bits 6:0 Initial gain	Initial gain = bits (6:0) x 0.03125.	0x20	Y	N	W
R45:0—0x02D - Red gain					
Bits 10:9 Digital gain	Total gain = (Bit 9 + 1) x (Bit 10 + 1) x analog gain (each bit gives 2X gain).	0x0	Y	N	W
Bits 8:7 Analog gain	Analog gain = (Bit 8 + 1) x (Bit 7 + 1) x initial gain (each bit gives 2X gain).	0x0	Y	N	W
Bits 6:0 Initial gain	Initial gain = bits (6:0) x 0.03125.	0x20	Y	N	W

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Table 13: Sensor Core Register Descriptions (Continued)

Bit Field	Description	Default (Hex)	Synced to Frame Start	Bad Frame	Read/ Write
R46:0—0x02E - Green2 gain					
Bits 10:9 Digital gain	Total gain = (Bit 9 + 1) x (Bit 10 + 1) x analog gain threshold (each bit gives 2X gain).	0x0	Y	N	W
Bits 8:7 Analog gain	Analog gain = (Bit 8 + 1) x (Bit 7 + 1) x initial gain (each bit gives 2X gain).	0x0	Y	N	W
Bits 6:0 Initial gain	Initial gain = bits (6:0) x 0.03125.	0x20	Y	N	W
R47:0—0x02F - Global gain					
Bits 10:0 Global gain	This register can be used to set all 4 gains at once. When read, it returns the value stored in R0x2B.	0x20	Y	N	W
R91:0—0x05B - Dark green1 frame average (R/O)					
R92:0—0x05C - Dark blue frame average (R/O)					
R200:0—0x0C8 - Context control					
Bit 15 Restart	Setting this bit causes the sensor to abandon the current frame and start resetting the first row. Same physical register as R0x00D[1].	0x0	N	YM	W
Bit 7 xenon flash enable	Enable xenon flash. Same physical register as R0x023[13].	0x0	Y	N	W
Bit 3 Read mode select	0: Use read mode, context A, R0x021. 1: Use read mode, context B, R0x020. Note that bits found only in the read mode context B register is always taken from that register.	0x0	Y	YM	W
Bit 2 LED flash enable	Enable LED flash. Same physical register as R0x023[8].	0x0	Y	Y	W
Bit 1 Vertical blanking select	0: Use vertical blanking, context A, R0x008. 1: Use vertical blanking, context B, R0x006.	0x0	Y	YM	W
Bit 0 Horizontal blanking select	0: Use horizontal blanking, context A, R0x007. 1: Use horizontal blanking, context B, R0x005.	0x0	Y	YM	W
R240:0—0x0F0 - Page map					
Bits 2:0 Page map	Page mapping register. Must be kept at "0" to be able to write to/read from sensor. Used in the SOC to access other pages with registers.	0x0	N	0	W
R241:0—0x0F1 - Byte-wise address					
Bit 0 Byte-wise address	Special address to perform 8-bit (instead of 16-bit) reads and writes to the sensor. For additional information, see "Two-Wire Serial Interface Sample" on page 61 and "Appendix A – Serial Bus Description" on page 59.	N/A	0	0	0
R255:0—0x0FF - Chip version (R/O)					

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Table 13: Sensor Core Register Descriptions (Continued)

Bit Field	Description	Default (Hex)	Synced to Frame Start	Bad Frame	Read/ Write
Bits 15:0	Hardwired value.	0x143A			R

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Sensor Read Modes and Timing

This section provides an overview of typical usage modes for the MT9M131. It focuses on two primary configurations: the first is suitable for low-power viewfinding, the second for full resolution snapshots. It also describes mechanisms for switching between these modes.

Contexts

The MT9M131 supports hardware-accelerated context switching. A number of parameters have two copies of their setup registers; this allows two contexts to be loaded at any given time. These are referred to as context A and context B. Context selection for any single parameter is determined by the global context control register (GCCR, see R0x2C8). There are copies of this register in each address page. A write to any one of them has the identical effect. However, a READ from address page 0 only returns the subset bits of R0xC8 that are specific to the sensor core.

The user can employ contexts for a variety of purposes; thus the generic naming convention. One typical usage model is to define context A as viewfinder or preview mode and context B as snapshot mode. The device defaults are configured with this in mind. This mechanism enables the user to have settings for viewfinder and snapshot modes loaded at the same time, and then switch between them with a single write to R0x2C8.

Viewfinder/Preview and Full-Resolution/Snapshot Modes

In the MT9M131, the sensor core supports two primary readout modes: low-power preview mode and full-resolution snapshot mode.

Low-Power Preview Mode

QSXGA (640 x 512) images are generated at up to 30 fps. The reduced-size images are generated by skipping pixels in the sensor, that is, decimation. The key sensor registers that define this mode are read mode context A register (R0x021) and read mode context B register (R0x020). Only certain bits in these registers are context switchable; any bits that do not have multiple contexts are always defined by their values in R0x020. Any active sets of these registers are defined by the state of R0xNC8[3]. On reset, R0xNC8[3] = 0 selecting R0x021; setups specific to preview are defined by this register.

Full-Resolution Snapshot Mode

SXGA (1280 x 1024) images are generated at up to 15 fps. This is typically selected by setting R0x0C8[3] = 1 selecting R0x020 (context B) as the primary read mode register.

Switching Modes

Typically, switching to full-resolution or snapshot mode is achieved by writing R0x2C8 = 0x9F0B. This restarts the sensor and sets most contexts to context B. Following this write, a READ from R0x1C8 or R0x2C8 results in 0x1F0B being read. Note that the most significant bit (MSB) is cleared automatically by the sensor. A READ from R0x0C8 results in 0x000B, as only the lower 4 bits and the restart MSB are implemented in the sensor core.

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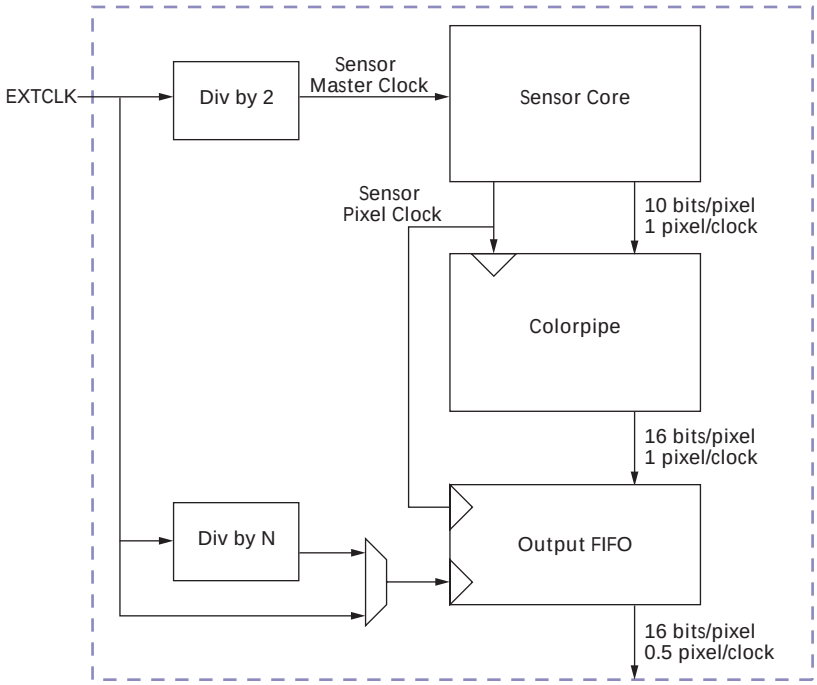
Clocks

The sensor core is a master in the system. The sensor core frame rate defines the overall image flow pipeline frame rate. Horizontal and vertical blanking are influenced by the sensor configuration, and are also a function of certain IFP functions—particularly resize. The relationship of the primary clocks are depicted in Figure 10.

Figure 10: Primary Sensor Core Clock Relationships



The IFP typically generates up to 16 bits per pixel, for example YCbCr or 565RGB, but has only an 8-bit port through which to communicate this pixel data. There is no phase locked loop (PLL), so the primary input clock (EXTCLK) must be twice the fundamental pixel rate (defined by the sensor pixel clock).

To generate SXGA images at 15 fps, the sensor core requires a clock in the 24 to 27 MHz range; this is also the fundamental pixel clock rate (sensor pixel clock) for full-power operation. To achieve this pixel rate, EXTCLK must be in the 48 to 54 MHz range. The device defaults assume a 54 MHz clock. Minimum clock frequency is 2 MHz.

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Primary Operating Modes

The MT9M131 supports two primary modes of operation with respect to the sensor core that affect pixel rate, frame rate, and blanking.

Full-Power Readout Mode

The sensor is in full resolution mode, generating 1.3 megapixels (SXGA = 1,280 x 1,024 + border) for interpolation. The SXGA image fed from the sensor to the colorpipe can be resized in the colorpipe, but the frame rate is still defined by sensor core operation. In full-power readout mode, with full FOV, the frame rate is invariant with the final image size:

Context:	Typically context B
Sensor read mode settings:	No skipping Full-power readout, that is, full data rate
Sensor pixel clock:	27 MHz for 54 MHz master clock: Maximum pixel rate of 27 megapixels per second
Maximum frame rate:	For 54 MHz master clock, 15 fps

Low-Power Readout Mode

Running under low-power readout, the sensor is in skip mode, and generates QSXGA frames (640 x 512 + border = 336,960 pixels). This full FOV QSXGA image can be resized, but only to resolutions smaller than QSXGA. The frame rate is defined by the operating mode of the sensor:

Context:	Typically context A
Sensor read mode settings:	Row skip 2X Column skip 2X Low-power readout maximum data rate is half that of full-power readout
Sensor pixel clock:	13.5 MHz for 54 MHz master clock: Maximum pixel rate of 13.5 megapixels per second
Maximum frame rate:	For 54 MHz master clock, 30 fps

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Tuning Frame Rates

Actual frame rates can be tuned by adjusting various sensor parameters. The sensor registers are in page 0, thus the "0" at the begining of each register address:

Table 14: Register Address Functions

Register	Function
R0x004	Window width, typically 1280 in the MT9M131
R0x003	Window height, typically 1024 in the MT9M131
Low-power readout mode—context A	
R0x007	Horizontal blanking, default is 190 (units of sensor pixel clocks)
R0x008	Vertical blanking, default is 17 (rows including black rows)
Full-power readout mode—context B	
R0x005	Horizontal blanking, default is 388 (units of sensor pixel clocks)
R0x006	Vertical blanking, default is 42 (rows including black rows)

In the MT9M131, the sensor core adds 4 border pixels all the way around the image, taking the active image size to 1288 x 1032 in full-power snapshot resolution, and 648 x 520 when skipping rows in low-power preview resolution. This is achieved through the default settings:

- Read mode context B: R0x020
- Oversize and show border bits are set by default
- Oversize and show border bits are not context switchable, thus their location only in read mode context B

Default Blanking Calculations

The MT9M131 default blanking calculations are a function of context, as follows:

[REG<a> | REG<b>]:

- Reg<a>
  Low-power readout = context A, typically used for viewfinder
- Reg<b>
  Full power readout = context B, typically used for snapshots

Table 15: Blanking Parameter Calculations

Parameter	Calculation
PC_PERIOD Sensor pixel clock period	Full-power readout: (2/54)?s = 0.0370?s Low-power readout: (4/54)?s = 0.0185?s
A: Active data time (per line): R0x004 + 8 (border) x PC_PERIOD	Full-power readout: A = 1,288 x (2/54)?s = 47.704?s Low-power readout: A = 648 x (4 / 54)?s = 48.000 ?s
Q: Horizontal blanking: [R0x005 | R0x007] x PC_PERIOD	Full-power readout: Q = 388 x (2/54)?s = 14.370?s Low-power readout: Q = 190 x (4/54)?s = 14.074?s
Row Time = Q + A:	Full-power readout: 62.074?s Low-power readout: 62.074?s
P: Frame start / End blanking: 4 x PC_PERIOD	Full-power readout: P = 4 x (2/54)?s = 0.148?s Low-power readout: P = 4 x (4 / 54)?s = 0.296?s
V: Vertical blanking: [R0x006 | R0x008] x (Q + A) + (Q - 2 x P)	Full-power readout: V = (42 x 62.074) + (14.370 - 0.296) = 2,621.333?s Low-power readout: V = (17 x 62.074) + (14.074 - 0.593) = 1,068.740?s
F: Total frame time:	Full-power readout: F = (1,032 + 42) x 62.074?s = 66,667.556?s ≥ 15 fps

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Table 15: Blanking Parameter Calculations

Parameter	Calculation
(R0x003 + [R0x006 | R00x008]) x (Q + A)	Low-power readout: F = (520 + 17) x 62.074?s = 33,333.778?s ≥ 30 fps

Notes: 1. The line rate (row rate) is the same for both low power and full power readout modes. This ensures that when switching modes, exposure time does not change; the pre-existing shutter width remains valid.

User Blanking Calculations

When calculating blanking for different clock rates, minimum values for horizontal blanking and vertical blanking must be taken into account. Table 16 shows minimum values for each register.

Table 16: User Blanking Minimum Values

Parameter	Register	Minimum
Horizontal blanking	Full-power readout (context B): R0x005 Low-power readout (context A): R0x007	202 (sensor pixel clocks) 114 (sensor pixel clocks)
Vertical blanking	Full-power readout (context B): R0x006 Low-power readout (context A): R0x008	5 (rows) 5 (rows)

Exposure and Sensor Context Switching

The MT9M131 incorporates device setup features that prevent changes in sensor context from causing a change in exposure when switching between preview/viewfinder and full resolution/snapshot modes. This is achieved by keeping the line rate consistent between modes.

Exposure

Defined by the shutter width. This is the number of lines to be reset before starting a frame read. If line rate does not change when a mode changes, exposure does not change.

Switching From Context A to Context B

Under typical/default settings, the sensor pixel rate doubles when switching from preview (context A) to full resolution (context B). Additionally, the number of pixels to be read per line nearly doubles. This naturally keeps the line rates roughly equal. The difference occurs due to border pixels: for SOC operation, there are always 8 border pixels regardless of context, thus the number of pixels in each line is not quite doubled.

Horizontal Blanking

Defined in terms of sensor pixel clocks. The sensor pixel clock rate doubles when switching from low-power readout mode (preview context A) to full-power readout mode (full resolution context B). To maintain the same horizontal blanking time, the value for horizontal blanking must double. This is handled by the dual, context-switchable horizontal blanking registers.

Switching Modes

Initiate mode switches from preview (context A) to snapshot (context B) during vertical blanking; switching should be accompanied by a sensor restart. Ensure that R0x0C8[15] is written as “1” when changing contexts.

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Switching Frequency

The user can switch between sensor contexts as frequently as necessary (without affecting exposure) constant switches can occur as often as once per frame.

Simple Snapshots

To take a snapshot, simply switch from context A to context B (with restart) for a few frames, then switch back again, capturing one of the context B frames as the snapshot. Alternative methods are supported by an internal sequencer. These additional methods are advantageous for taking flash snapshots.

Output Timing

Figure 11: Vertical Timing

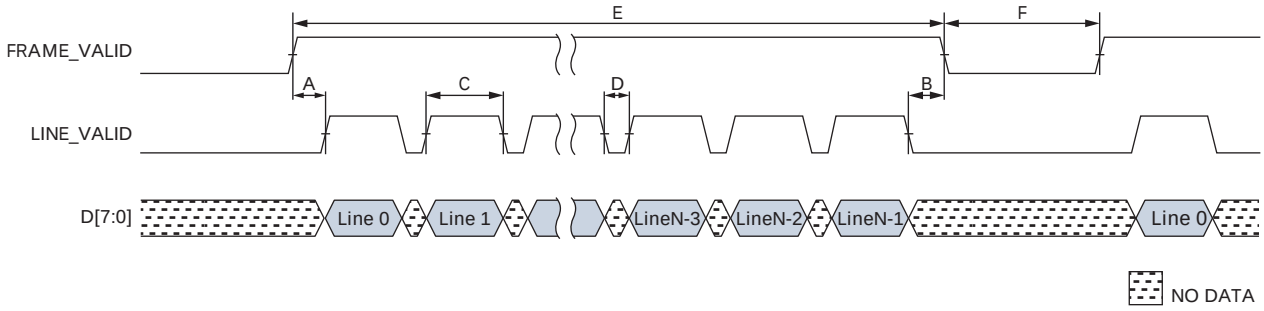
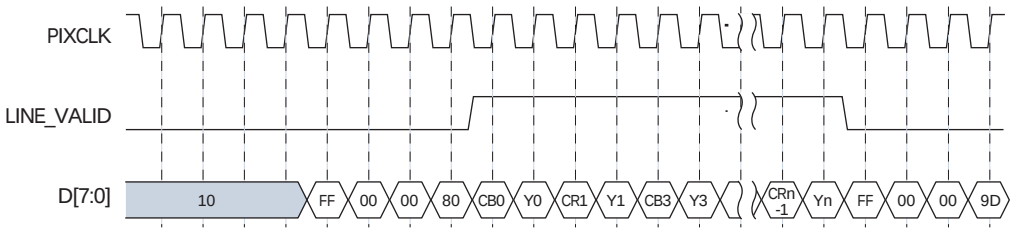


Figure 12: Horizontal Timing



Notes:
1. Line start: FF00 0080.
2. Line end: FF00 009D.

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Typical Resolutions, Modes, and Timing

The parameters in Table 17 are illustrated in waveform diagram Figure 11 on page 52. Table 22 on page 56 provides values for these parameters in some common resolutions and operating modes.

Table 17: Blanking Definitions

Designation	Definition
A	FV (rising edge) to LV (rising edge) delay
B	LV (falling edge) to FV (falling edge) delay
C	LV (HIGH/valid) time
D	LV (LOW/horizontal blanking) time
E	FV (HIGH/valid) time
F	FV (LOW/vertical blanking) time

Reset, Clocks, and Standby

Functional Operation

Power-up reset is asserted/de-asserted on RESET_BAR. It is active LOW. In this reset state, all control registers have the default values. All internal clocks are turned off except for the divided-by-2 clock to the sensor core.

Soft reset is asserted/de-asserted by the two-wire serial interface program. There are sensor core soft resets and SOC soft resets. In soft reset mode, the two-wire serial interface and register ring bus are still running. All control registers are reset using default values. See R0x00D.

Hard standby is asserted/de-asserted on STANDBY. It is active HIGH. In this hard standby state, all internal clocks are turned off and analog block is in standby mode to save power consumption.

Note: Following the assertion of hard standby, at least 24 master clock cycles must be delivered to complete the transition to the hard standby state.

Soft standby is asserted/de-asserted differently in the sensor page or colorpipe page. The sensor soft standby bit is in R0x00D[2]. Colorpipe soft standby disables some of the SOC clocks, including the pixel clock. This bit is R0x1B3[0]. The colorpipe must first be brought out of standby through R0x1B3[0].

The colorpipe soft standby is provided to enable the user to turn off the colorpipe and the sensor independently.

By default, all outputs except SDATA are disabled during hard standby. This feature can be disabled by setting R0x1B3[1] = 0. Independent control of the outputs is available either through OE_BAR or R0x00D[4]. All outputs are implemented using bidirectional buffers, thus should not be left tri-stated. In dual camera applications, ensure that one camera is driving the bus, or that the bus is pulled to VGNDIO or VDDIO, even during standby.

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Electrical Specifications

Table 18: Electrical Characteristics and Operating Conditions
T_A = Ambient = 25°C

Parameter	Condition	Min	Typ	Max	Unit
I/O digital voltage (V_{DD}_IO)		1.8	–	3.1	V
Core digital voltage (V_{DD})		2.5	2.8	3.1	V
Analog voltage (V_{AA})		2.5	2.8	3.1	V
Pixel supply voltage (VAA_PIX)		2.5	2.8	3.1	V
Leakage current	STANDBY, no clocks	–	–	10	?A
Operating temperature	Measured at junction	–30	–	+70	°C

Note: V_{DD}, V_{AA}, and VAAPIX must all be at the same potential to avoid excessive current draw. Care must be taken to avoid excessive noise injection in the analog supplies if all three supplies are tied together.

Table 19: I/O Parameters

Signal	Parameter	Definitions	Condition	Min	Typ	Max	Unit
All outputs		Load capacitance		–	–	30	pF
		Output pin slew	2.8V, 30pF load	–	0.72	–	V/ns
			2.8V, 5pF load	–	1.25	–	V/ns
			1.8V, 30pF load	–	0.34	–	V/ns
			1.8V, 5pF load	–	0.51	–	V/ns
	V_{OH}	Output HIGH voltage		V_{DD}IO – 0.3	–	V_{DD}IO	V
	V_{OL}	Output LOW voltage		0	–	0.3	V
	I_{OH}	Output HIGH current	V_{DD}_IO = 2.8V, V_{OH} = 2.4V	16	–	26.5	mA
			V_{DD}_IO = 1.8V, V_{OH} = 1.4V	8	–	15	mA
	I_{OL}	Output LOW current	V_{DD}_IO = 2.8V, V_{OL} = 0.4V	15.9	–	21.3	mA
			V_{DD}_IO = 1.8V, V_{OL} = 0.4V	10.1	–	16.2	mA
	I_{OZ}	Tri-state output leakage current		–	–	10	?A
All inputs	V_{IH}	Input HIGH voltage	V_{DD}IO = 2.8V	2.0	–	–	V
			V_{DD}IO = 1.8V	1.2	–	–	V
	V_{IL}	Input LOW voltage	V_{DD}IO = 2.8V	–	–	0.9	V
			V_{DD}IO = 1.8V	–	–	0.6	V
	I_{IN}	Input leakage current		–5	–	+5	?A
	PIN CAP	Ball input capacitance		–	3.5	–	pF
EXTCLK	Freq	Master clock frequency	Absolute minimum	2	–	–	MHz
			SXGA at 15 fps	48	–	54	MHz

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Caution **Stresses above those listed in Table 20 may cause permanent damage to the device.**

Table 20: Absolute Maximum Ratings

Symbol	Parameter	Rating		Unit
		Min	Max	
V_{SUPPLY}	Power supply voltage (all supplies)	–0.3	4.0	V
I_{SUPPLY}	Total power supply current	150		mA
I_{GND}	Total ground current	150		mA
V_{IN}	DC input voltage	–0.3	V_{DDIO} + 0.3	V
V_{OUT}	DC output voltage	–0.3	V_{DDIO} + 0.3	V
T_{STG}	Storage temperature	–40	85	°C

Note: This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the product specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Power Consumption

Table 21: Power Consumption at 2.8V (in mW)

Mode	Sensor	Image Flow Processor	I/Os (10pF)	Total Power Consumption
SXGA at 15 fps	90	71	9	170
QSXGA at 30 fps	50	36	4	90
QSXGA at 15 fps	50	18	2	70
QVGA at 30 fps	50	32	1	83

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I/O Timing

By default, the MT9M131 launches pixel data, FV, and LV synchronously with the falling edge of PIXCLK. This is reflected by the default setting of R0x13A[9] and R0x19B[9] = 1. The expectation is that the user captures DOUT, FV, and LV using the rising edge of PIXCLK.

Figure 13: AC Output Timing Diagram

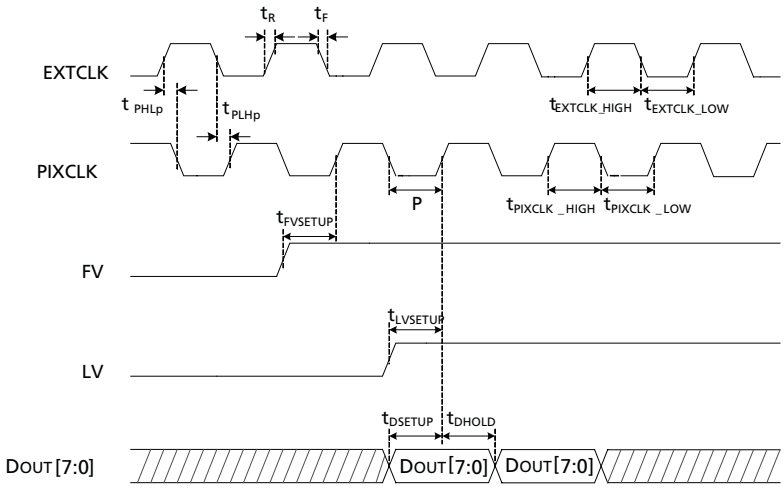

Table 22: AC Output Timing Data

Parameters	Description	Min	Typ	Max	Unit
^{f}EXTCLK	Input clock frequency	–	–	54	MHz
^{t}EXTCLK_HIGH	Input clock (EXTCLK) HIGH time	40	50	60	%
^{t}EXTCLK_LOW	Input clock (EXTCLK) LOW time	40	50	60	%
^{t}R	EXTCLK rise time	–	4.5	8	ns
^{t}F	EXTCLK fall time	–	4.5	8	ns
^{t}R DOUT	Data out rise time	–	4.5	9	ns
^{t}F DOUT	Data out fall time	–	4.5	9	ns
^{t}PHLP	Propagation delay from CLK HIGH to PIXCLK LOW	7	9	15	ns
^{t}PLHP	Propagation delay from CLK LOW to PIXCLK HIGH	7	9	15	ns
^{t}PIXCLK_HIGH	Pixel clock HIGH time	40	50	60	%
^{t}PIXCLK_LOW	Pixel clock LOW time	40	50	60	%
^{t}FVSETUP	Frame valid setup time	4	8	P	ns
^{t}LVSETUP	Line valid setup time	4	8	P	ns
^{t}DSETUP	Data out setup time	4	8	P	ns
^{t}DHOLD	Data out hold time	4	8	P	ns

Notes:
1. Measurements for the above table were done at:
   T_A = +25°C, VAA = VAA_PIX = VDD = VDD_IO = 2.8V
2. FV, LV, PIXCLK ,and DOUT are referenced from EXTCLK and, therefore, have the same propagation delay with respect to EXTCLK.
3. P = (½) PIXCLK Period
4. Minimum and maximum (rise and fall) times for EXTCLK and DOUT will depend on the type of input signal and load capacitance.

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Figure 14: Spectral Response Chart

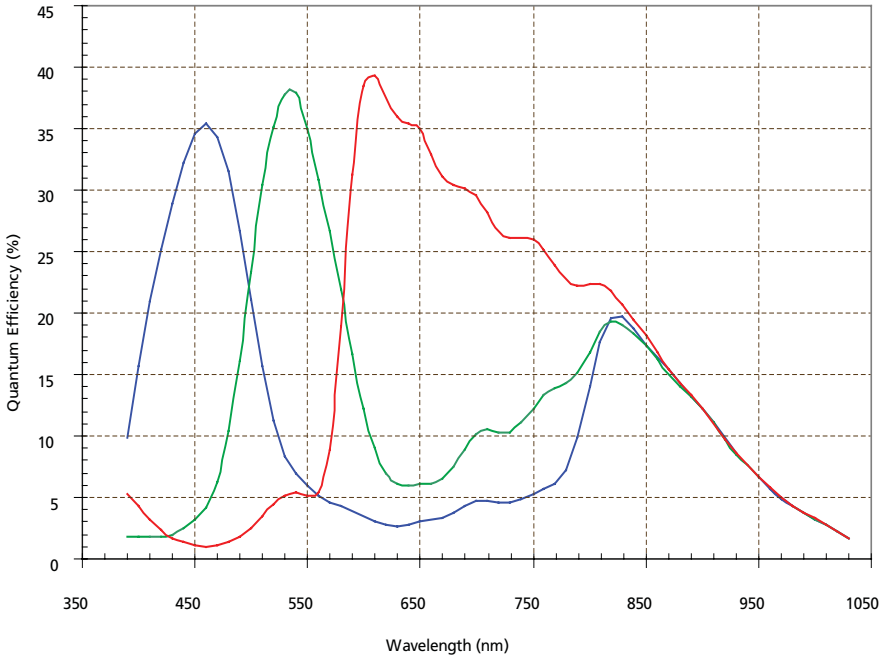


Figure 15: CRA versus Image Height

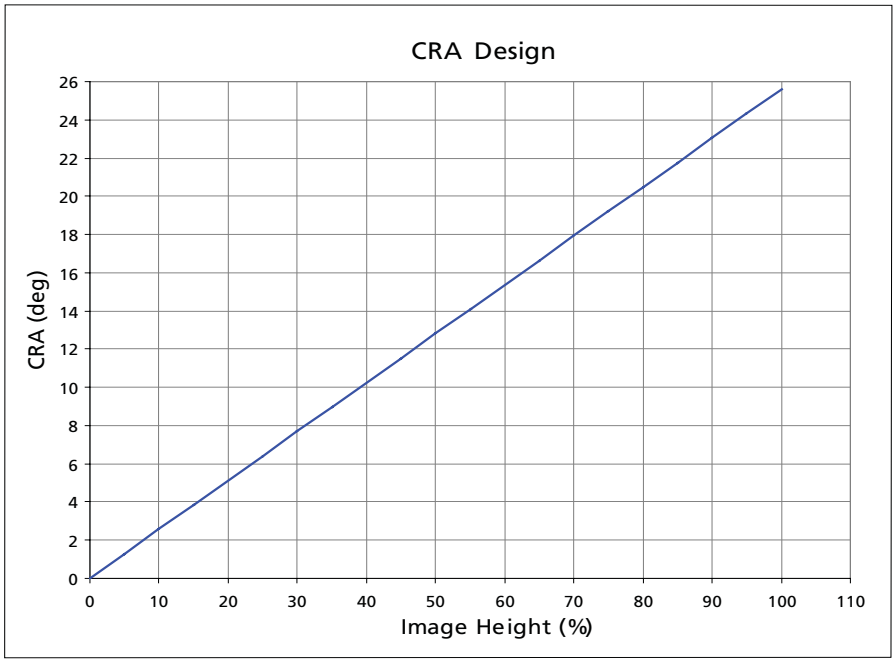
CRA versus Image Height Plot	Image Height (%)	Image Height (mm)	CRA (°)
	0	0	0
	5	0.148	1.28
	10	0.295	2.56
	15	0.443	3.84
	20	0.590	5.12
	25	0.738	6.40
	30	0.885	7.68
	35	1.033	8.96
	40	1.180	10.25
	45	1.328	11.53
	50	1.475	12.81
	55	1.623	14.09
	60	1.770	15.37
	65	1.918	16.65
	70	2.065	17.93
	75	2.213	19.21
	80	2.360	20.49
	85	2.508	21.77
	90	2.656	23.05
	95	2.803	24.33
	100	2.951	25.61

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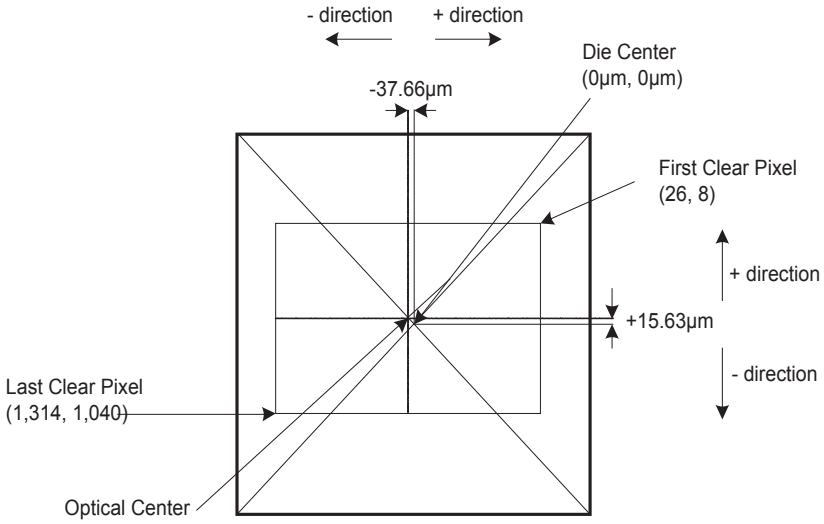
Figure 16: Optical Center Diagram



Note: Figure not to scale.

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Appendix A – Serial Bus Description

Registers are written to and read from the MT9M131 through the two-wire serial interface bus. The sensor is a serial interface slave and is controlled by the serial clock (SCLK). SLCK is driven by the serial interface master. Data is transferred into and out of the MT9M131 through the serial data (SDATA) line. The SDATA line is pulled up to VDDIO off-chip by a 1.5KΩ resistor. Either the slave or the master device can pull the SDATA line down—the two-wire serial interface protocol determines which device is allowed to pull the SDATA line down at any given time.

Protocol

The two-wire serial interface defines several different transmission codes, as shown in the following sequence:

1. Astart bit
2. The slave device 8-bit address. The SADDR pin is used to select between two different addresses in case of conflict with another device. If SADDR is LOW, the slave address is 0x90; if SADDR is HIGH, the slave address is 0xBA.
3. An (a no) acknowledge bit
4. An 8-bit message
5. Astop bit

Sequence

A typical READ or WRITE sequence is executed as follows:

1. The master sends a start bit.
2. The master sends the 8-bit slave device address. The last bit of the address determines if the request is a READ or a WRITE, where a “0” indicates a WRITE and a “1” indicates a READ.
3. The slave device acknowledges receipt of the address by sending an acknowledge bit to the master.
4. If the request is a WRITE, the master then transfers the 8-bit register address, indicating where the WRITE takes place.
5. The slave sends an acknowledge bit, indicating that the register address has been received.
6. The master then transfers the data, 8 bits at a time, with the slave sending an acknowledge bit after each 8 bits.

The MT9M131 uses 16-bit data for its internal registers, thus requiring two 8-bit transfers to write to one register. After 16 bits are transferred, the register address is automatically incremented so that the next 16 bits are written to the next register address. The master stops writing by sending a start or stop bit.

A typical READ sequence is executed as follows.

1. The master sends the write-mode slave address and 8-bit register address, just as in the write request.
2. The master then sends a start bit and the read-mode slave address, and clocks out the register data, 8 bits at a time.
3. The master sends an acknowledge bit after each 8-bit transfer. The register address is automatically incremented after every 16 bits is transferred.
4. The data transfer is stopped when the master sends a no-acknowledge bit.

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Bus Idle State

The bus is idle when both the data and clock lines are HIGH. Control of the bus is initiated with a start bit, and the bus is released with a stop bit. Only the master can generate the start and stop bits.

Start Bit

The start bit is defined as a HIGH-to-LOW transition of the data line while the clock line is HIGH.

Stop Bit

The stop bit is defined as a LOW-to-HIGH transition of the data line while the clock line is HIGH.

Slave Address

The 8-bit address of a two-wire serial interface device consists of seven bits of address and 1 bit of direction. A "0" in the least significant bit (LSB) of the address indicates write mode, and a "1" indicates read mode. The write address of the sensor is 0xBA; the read address is 0xBB. This applies only when the SADDR is set HIGH.

Data Bit Transfer

One data bit is transferred during each clock pulse. The serial interface clock pulse is provided by the master. The data must be stable during the HIGH period of the two-wire serial interface clock—it can only change when the serial clock is LOW. Data is transferred 8 bits at a time, followed by an acknowledge bit.

Acknowledge Bit

The master generates the acknowledge clock pulse. The transmitter (which is the master when writing, or the slave when reading) releases the data line, and the receiver signals an acknowledge bit by pulling the data line LOW during the acknowledge clock pulse.

No-Acknowledge Bit

The no-acknowledge bit is generated when the data line is not pulled down by the receiver during the acknowledge clock pulse. A no-acknowledge bit is used to terminate a read sequence.

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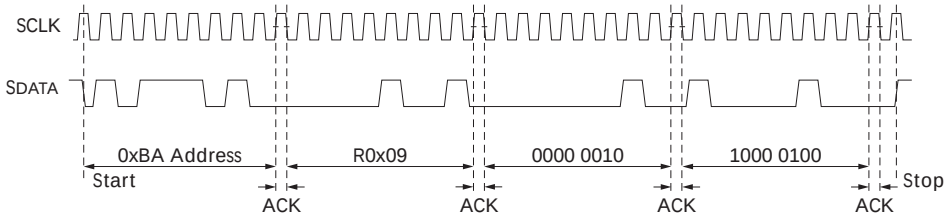
Two-Wire Serial Interface Sample

WRITE and READ Sequences (SADDR = 1)

16-Bit Write Sequence

A typical WRITE sequence for writing 16 bits to a register is shown in Figure 17. A start bit sent by the master starts the sequence, followed by the write address. The image sensor sends an acknowledge bit and expects the register address to come first, followed by the 16-bit data. After each 8-bit transfer, the image sensor sends an acknowledge bit. All 16 bits must be written before the register is updated. After 16 bits are transferred, the register address is automatically incremented so that the next 16 bits are written to the next register. The master stops writing by sending a start or stop bit.

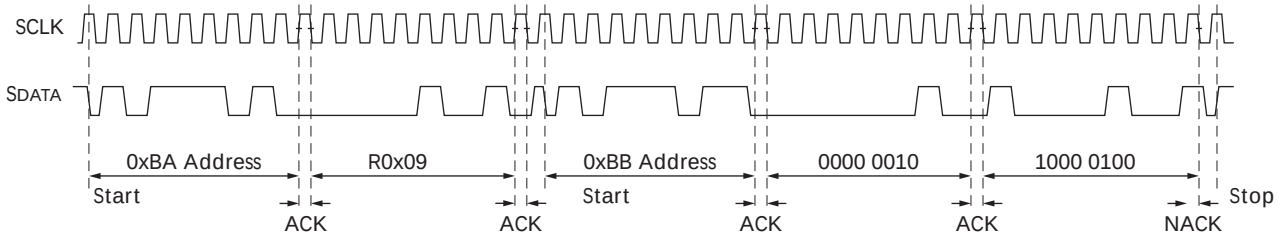
Figure 17: Write Timing to R0x009—Value 0x0284



16-Bit Read Sequence

A typical READ sequence is shown in Figure 18. The master writes the register address, as in a WRITE sequence. Then a start bit and the read address specify that a read is about to occur from the register. The master then clocks out the register data, 8 bits at a time. The master sends an acknowledge bit after each 8-bit transfer. The register address should be incremented after every 16 bits is transferred. The data transfer is stopped when the master sends a no-acknowledge bit.

Figure 18: Read Timing from R0x009; Returned Value 0x0284



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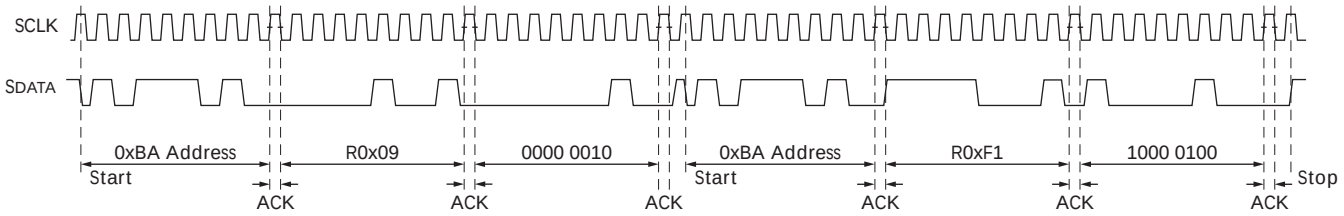
8-Bit Write Sequence

To be able to write one byte at a time to the register, a special register address is added. The 8-bit WRITE is started by writing the upper 8 bits to the desired register, then writing the lower 8 bits to the special register address (R0x0F1). The register is not updated until all 16 bits have been written. It is not possible to update just half of a register. Figure 19 shows a typical sequence for an 8-bit WRITE. The second byte is written to the special register (R0x0F1).

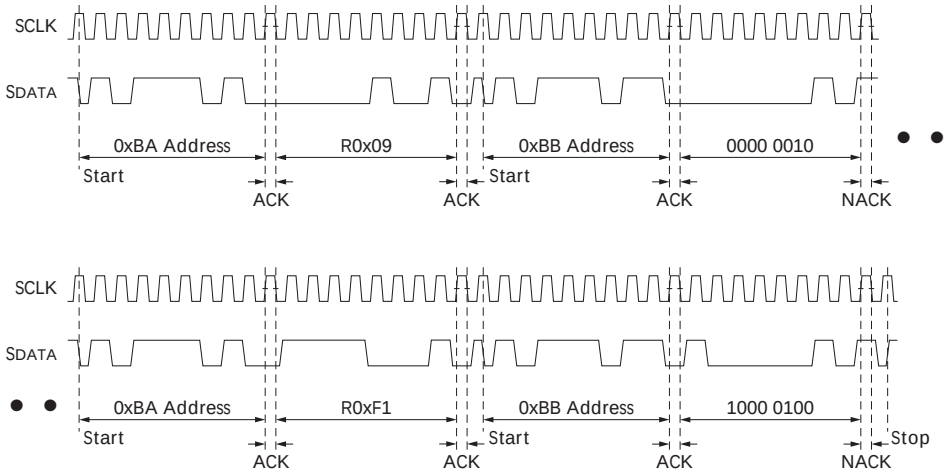
Figure 19: Write Timing to R0x009—Value 0x0284



8-Bit Read Sequence

To read one byte at a time, the same special register address is used for the lower byte. The upper 8 bits are read from the desired register. By following this with a READ from the special register (R0x0F1), the lower 8 bits are accessed (Figure 20). The master sets the no-acknowledge bits.

Figure 20: Read Timing from R0x009; Returned Value 0x0284



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Two-Wire Serial Bus Timing

The two-wire serial bus operation requires certain minimum master clock cycles between transitions. These are specified in the Figure 21 and Figure 22 in master clock cycles.

Figure 21: Two-Wire Serial Interface Timing Diagram at the Pins of the Sensor

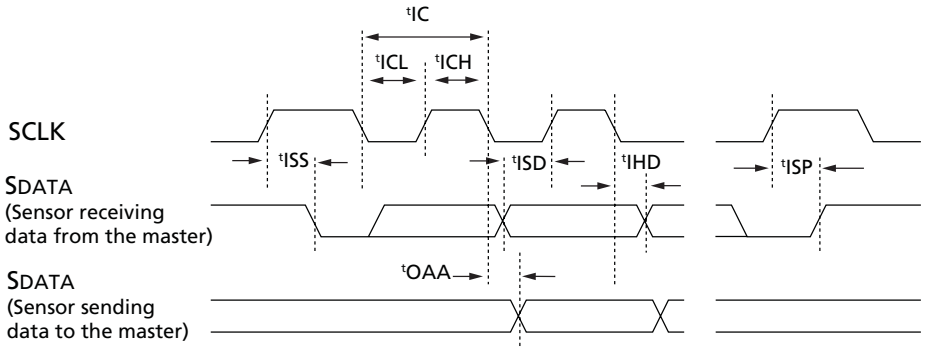

Figure 22: Two-Wire Serial Interface Timing Diagram at the Pins of the Sensor (2)

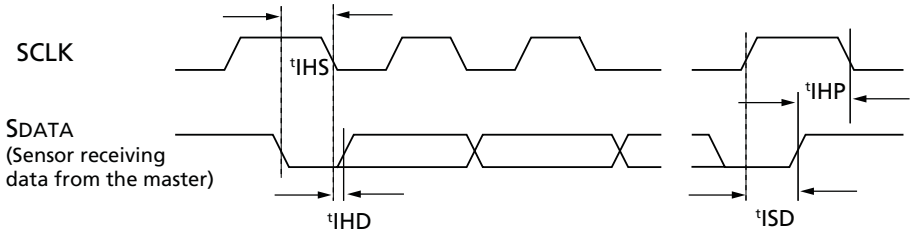

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Table 23: Two-Wire Serial Interface Timing

V_{DD} = V_{AA} = VAA_PIX = V_{DD}_IO = 2.8V, T = –30°C to +70°C

Symbol	Definition	Min	Typ	Max	Unit
^{f}IC	Two-wire serial bus input clock frequency	–	–	400	KHz
^{t}IC	Two-wire serial bus input clock period	2500	–	–	ns
^{t}ICL	Two-wire serial bus clock LOW	–	1250	–	ns
^{t}ICH	Two-wire serial bus clock HIGH	–	1250	–	ns
^{t}ISS	Setup time for start condition	600	–	–	ns
^{t}IHS	Hold time for start condition	600	–	–	ns
^{t}ISD	Setup time for input data	600	–	–	ns
^{t}IHD	Hold time for input data	600	–	–	ns
^{t}OAA	Output delay time	–	–	600	ns
^{t}ISP	Setup time of stop condition	600	–	–	ns
^{t}IHP	Hold time for stop condition	600	–	–	ns
$C_{SCLCK/SDATA}$	SCLCK and SDATA load capacitance	–	–	30	pF
$R_{SCLCK/SDATA}$	SCLCK and SDATA pull-up resistor	–	1.5	–	kΩ

Note: A minimum EXTCLK frequency of 4 MHz is required for the two-wire serial interface to operate at 400 KHz.

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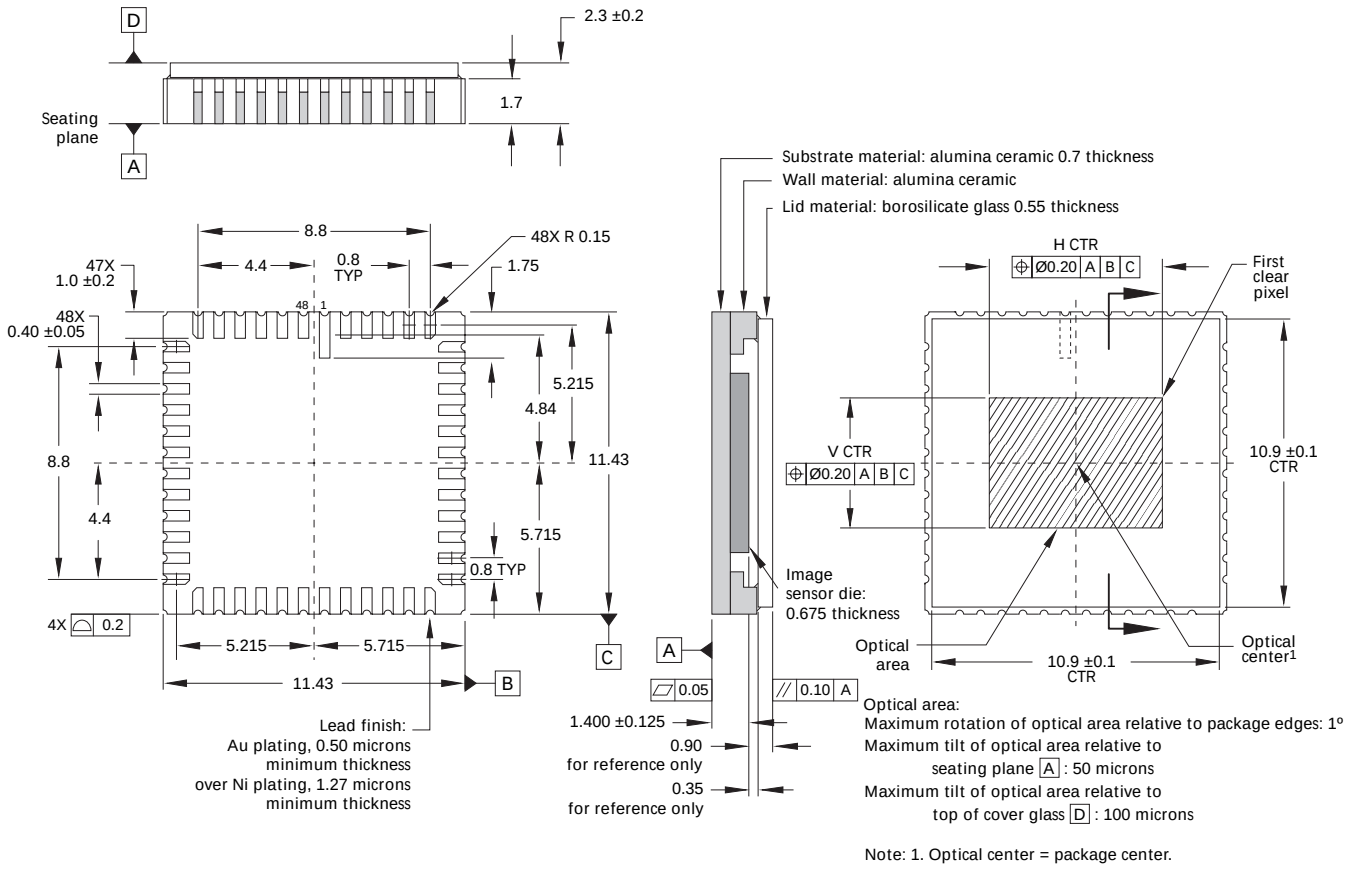
Package Dimensions

The MT9M131 comes in a 48-pin CLCC package, shown in Figure 23.

Figure 23: 48-Pin CLCC Package



Notes:
1. An IR-cut filter is required to obtain optimal image quality.
2. All dimensions are in millimeters.

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Revision History

Rev D 2/23/09

- Updated to Aptina template
- Deleted all mention of 44-pin iCSP package as this is no longer available
- Removed ES designation from 48-pin CLCC package part numbers

Rev. C 2/1/2008

- Updated registers from decimal to hex format
- Updated Figure 14: “Spectral Response Chart,” on page 57
- Added Figure 15: “CRA versus Image Height,” on page 57

Rev. B 03/02/2007

- Updated "Features" on page 1
- Updated Table 1, “Key Performance Parameters,” on page 1
- Added Table 2, “Available Part Numbers,” on page 1
- Updated "General Description" on page 6
- Updated "Functional Overview" on page 7
- Updated Figure 1: “Functional Block Diagram,” on page 7
- Updated "Internal Architecture" on page 8
- Updated Figure 2: “Internal Registers Grouping,” on page 8
- Updated "Register Operations" on page 9
- Updated Figure 4: “Typical Configuration (connection),” on page 10
- Updated "Pin/Ball Assignment" on page 11
- Updated Figure 5: “48-Pin CLCC Assignment,” on page 11
- Updated Figure 6: “IFP Block Diagram,” on page 9
- Updated "ITU-R BT.656 and RGB Output" on page 12
- Updated "Configuration" on page 21
- Updated "Camera Control Registers" on page 29
- Updated "I/O Timing" on page 56
- Updated Figure 14: “Spectral Response Chart,” on page 57
- Updated Table 22, “AC Output Timing Data,” on page 56
- Updated Figure 23: “48-Pin CLCC Package,” on page 65

Rev. A, Preliminary 5/11/06

- Initial release

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