

PJP4N60 / PJF4N60

600V N-Channel Enhancement Mode MOSFET

FEATURES

- 4A , 600V, $R_{DS(ON)}=2.4\Omega@V_{GS}=10V, I_D=2.0A$
- Low ON Resistance
- Fast Switching
- Low Gate Charge
- Fully Characterized Avalanche Voltage and Current
- Specially Designed for AC Adapter, Battery Charge and SMPS
- In compliance with EU RoHs 2002/95/EC Directives

MECHANICAL DATA

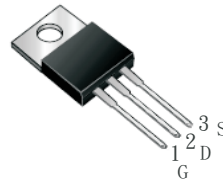
- Case: TO-220AB / ITO-220AB Molded Plastic
- Terminals : Solderable per MIL-STD-750,Method 2026

ORDERING INFORMATION

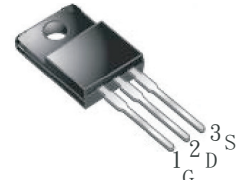
TYPE	MARKING	PACKAGE	PACKING
PJP4N60	P4N60	TO-220AB	50PCS/TUBE
PJF4N60	F4N60	ITO-220AB	50PCS/TUBE

TO-220AB / ITO-220AB

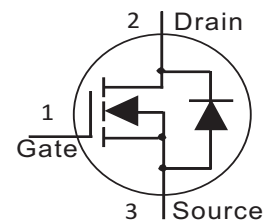
TO-220AB



ITO-220AB



INTERNAL SCHEMATIC DIAGRAM



Maximum RATINGS and Thermal Characteristics ($T_A=25^{\circ}C$ unless otherwise noted)

PARAMETER	Symbol	PJP4N60	PJF4N60	Units
Drain-Source Voltage	V_{DS}	600		V
Gate-Source Voltage	V_{GS}	± 30		V
Continuous Drain Current	I_D	4	4	A
Pulsed Drain Current ¹⁾	I_{DM}	16	16	A
Maximum Power Dissipation Derating Factor	P_D	70 0.56	26 0.2	W
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 to +150		$^{\circ}C$
Avalanche Energy with Single Pulse $I_{AS}=4.4A, V_{DD}=85V, L=30mH$	E_{AS}	330		mJ
Junction-to-Case Thermal Resistance	$R_{\theta JC}$	1.75	4.8	$^{\circ}C/W$
Junction-to Ambient Thermal Resistance(PCB mounted) ²	$R_{\theta JA}$	62.5	100	$^{\circ}C/W$

Note : 1. Maximum DC current limited by the package

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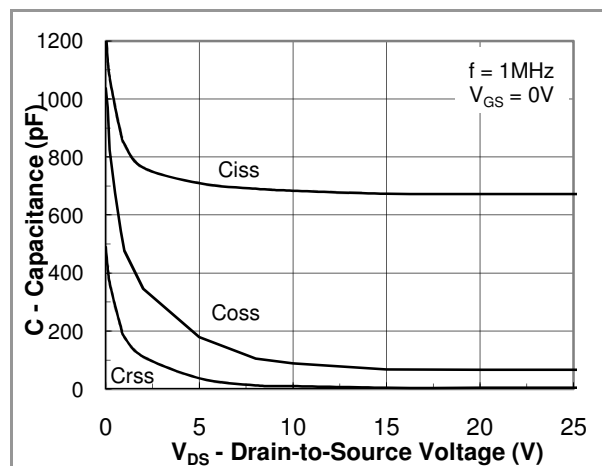
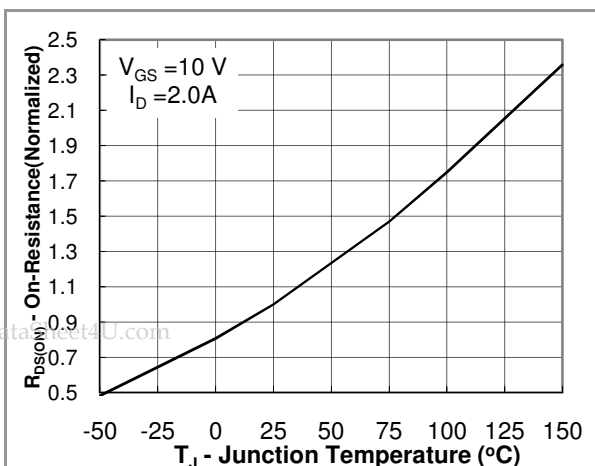
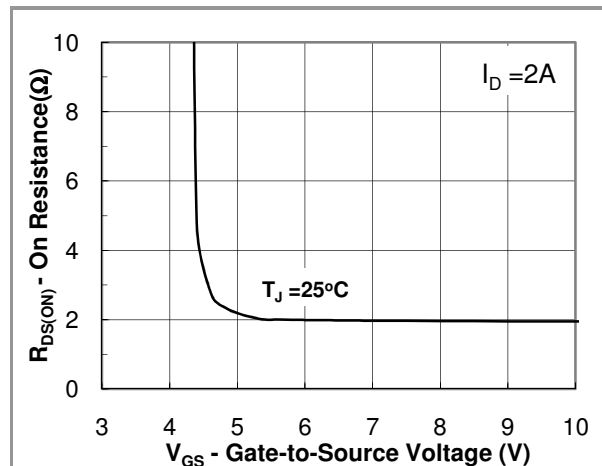
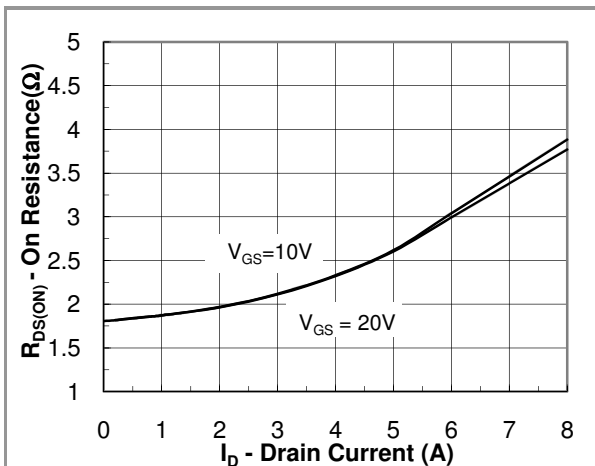
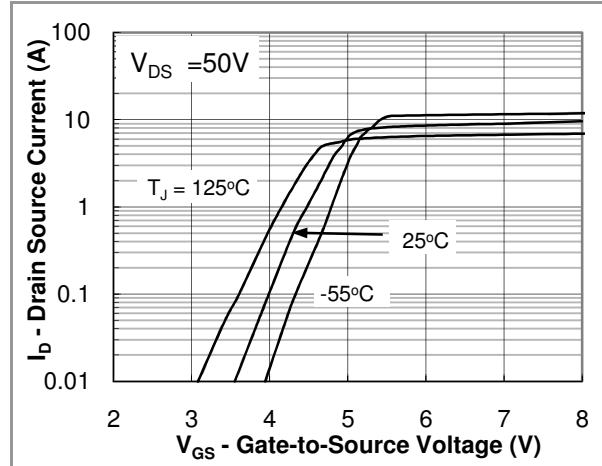
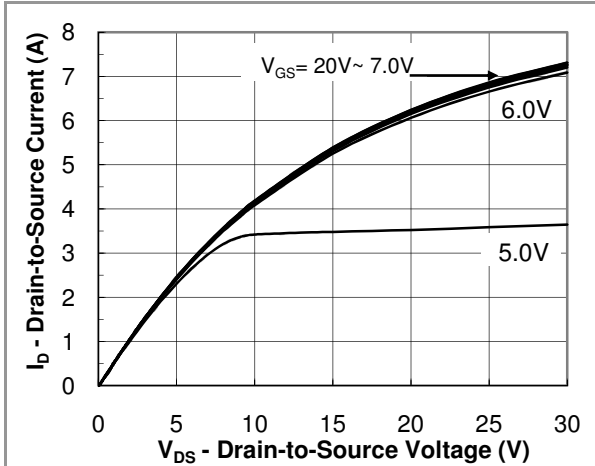
ELECTRICAL CHARACTERISTICS (T_A=25°C unless otherwise noted)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Units
Static						
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	600	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	2.0	-	4.0	V
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=2.0A$	-	2.0	2.4	Ω
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=600V, V_{GS}=0V$	-	-	10	μA
Gate Body Leakage	I_{GSS}	$V_{GS}=\pm 30V, V_{DS}=0V$	-	-	± 100	nA
Dynamic						
Total Gate Charge	Q_g	$V_{DS}=480V, I_D=4A$ $V_{GS}=10V$	-	17.2	-	nC
Gate-Source Charge	Q_{gs}		-	4.6	-	
Gate-Drain Charge	Q_{gd}		-	5.2	-	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD}=300V, I_D=4A$ $V_{GS}=10V, R_G=25\Omega$	-	11.6	16.8	ns
Turn-On Rise Time	t_r		-	10.6	15.2	
Turn-Off Delay Time	$t_{d(off)}$		-	25.8	36.8	
Turn-Off Fall Time	t_f		-	9.2	14.2	
Input Capacitance	C_{iss}	$V_{DS}=25V, V_{GS}=0V$ $f=1.0MHz$	-	560	680	pF
Output Capacitance	C_{oss}		-	55	66	
Reverse Transfer Capacitance	C_{rss}		-	5.2	9.6	
Source-Drain Diode						
Max. Diode Forward Current	I_S	-	-	-	4.0	A
Max.Pulsed Source Current	I_{SM}	-	-	-	16	A
Diode Forward Voltage	V_{SD}	$I_S=4A, V_{GS}=0V$	-	-	1.4	V
Reverse Recovery Time	t_{rr}	$V_{GS}=0V, I_F=4A$ $di/dt=100A/\mu s$	-	300	-	ns
Reverse Recovery Charge	Q_{rr}		-	2.2	-	μC

NOTE : Plus Test : Pluse Width ≤ 300us, Duty Cycle ≤ 2%.

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Typical Characteristics Curves ($T_a=25^\circ\text{C}$, unless otherwise noted)



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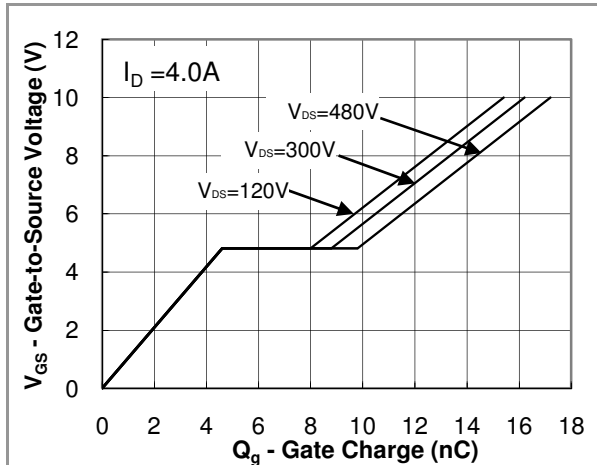


Fig. 7 Gate Charge Waveform

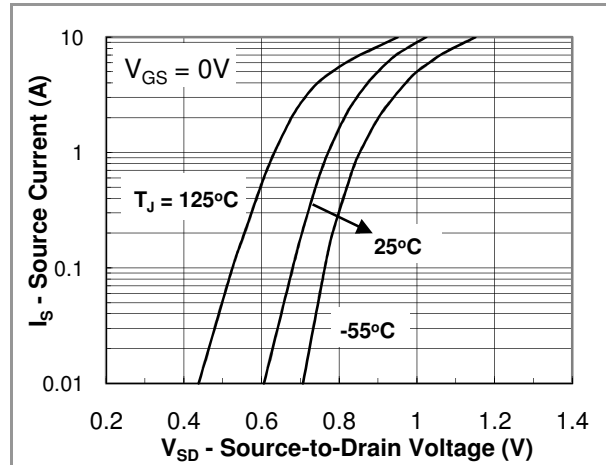


Fig. 8 Source-Drain Diode Forward Voltage

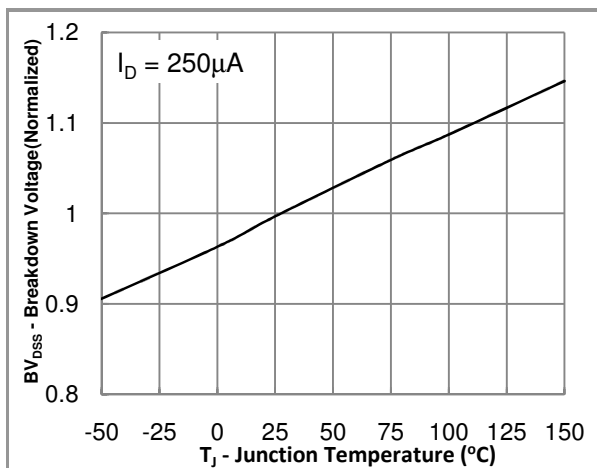


Fig. 9 Breakdown Voltage vs Junction Temperature



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