

MOS FIELD EFFECT TRANSISTOR
2SJ449

**SWITCHING
 P-CHANNEL POWER MOS FET
 INDUSTRIAL USE**

DESCRIPTION

The 2SJ449 is P-Channel MOS Field Effect Transistor designed for high voltage switching applications.

FEATURES

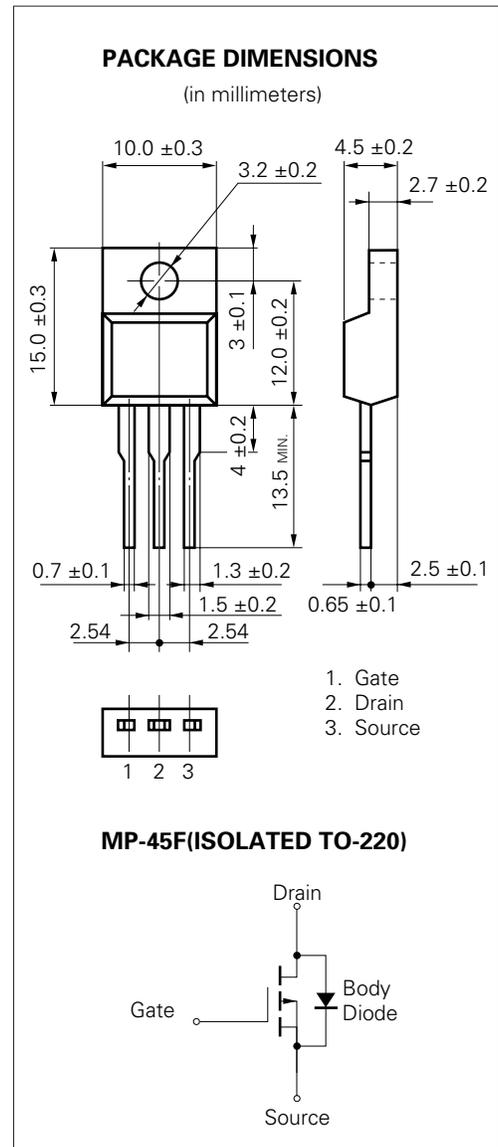
- Low On-Resistance
 $R_{DS(on)} = 0.8 \Omega \text{ MAX. (@ } V_{GS} = -10 \text{ V, } I_D = -3.0 \text{ A)}$
- Low C_{iss} $C_{iss} = 1040 \text{ pF TYP.}$
- High Avalanche Capability Ratings
- Isolated TO-220 Package

ABSOLUTE MAXIMUM RATINGS (TA = 25 °C)

| | | | |
|--------------------------------------|----------------|-------------|----|
| Drain to Source Voltage | V_{DSS} | -250 | V |
| Gate to Source Voltage | V_{GSS} | ± 30 | V |
| Drain Current (DC) | $I_{D(DC)}$ | ± 6.0 | A |
| Drain Current (pulse)* | $I_{D(pulse)}$ | ± 24 | A |
| Total Power Dissipation (Tc = 25 °C) | P_{T1} | 35 | W |
| Total Power Dissipation (TA = 25 °C) | P_{T2} | 2.0 | W |
| Channel Temperature | T_{ch} | 150 | °C |
| Storage Temperature | T_{stg} | -55 to +150 | °C |
| Single Avalanche Current** | I_{AS} | -6.0 | A |
| Single Avalanche Energy** | E_{AS} | 180 | mJ |

* $PW \leq 10 \mu s$, Duty Cycle $\leq 1 \%$

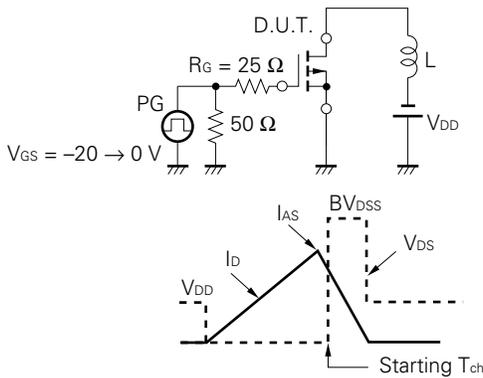
** Starting $T_{ch} = 25 \text{ °C}$, $R_G = 25 \Omega$, $V_{GS} = -20 \text{ V} \rightarrow 0$



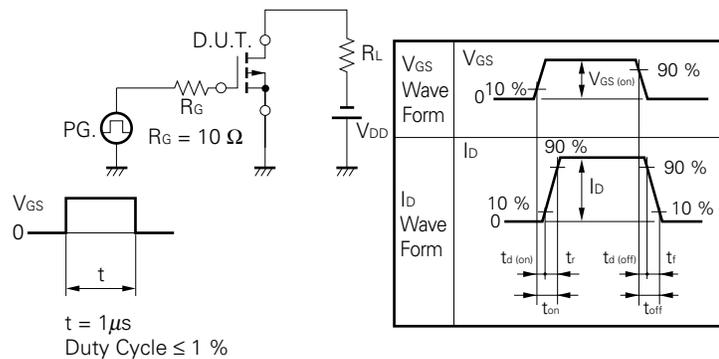
ELECTRICAL CHARACTERISTICS (T_A = 25 °C)

| CHARACTERISTIC | SYMBOL | MIN. | TYP. | MAX. | UNIT | TEST CONDITIONS |
|--------------------------------|----------------------|------|------|------|------|--|
| Drain to Source On-Resistance | R _{DS(on)} | | 0.55 | 0.8 | Ω | V _{GS} = -10 V, I _D = -3.0 A |
| Gate to Source Cutoff Voltage | V _{GS(off)} | -4.0 | -4.8 | -5.5 | V | V _{DS} = -10 V, I _D = -1 mA |
| Forward Transfer Admittance | y _{fs} | 2.0 | 3.5 | | S | V _{DS} = -10 V, I _D = -3.0 A |
| Drain Leakage Current | I _{DSS} | | | -100 | μA | V _{DS} = -250 V, V _{GS} = 0 |
| Gate to Source Leakage Current | I _{GSS} | | | ±100 | nA | V _{GS} = ±30 V, V _{DS} = 0 |
| Input Capacitance | C _{iss} | | 1040 | | pF | V _{DS} = -10 V |
| Output Capacitance | C _{oss} | | 360 | | pF | V _{GS} = 0 |
| Reverse Transfer Capacitance | C _{rss} | | 70 | | pF | f = 1 MHz |
| Turn-On Delay Time | t _{d(on)} | | 24 | | ns | I _D = -3.0 A |
| Rise Time | t _r | | 16 | | ns | V _{GS(on)} = -10 V |
| Turn-Off Delay Time | t _{d(off)} | | 47 | | ns | V _{DD} = -125 V |
| Fall Time | t _f | | 14 | | ns | R _G = 10 Ω, R _L = 42 Ω |
| Total Gate Charge | Q _G | | 23.1 | | nC | I _D = -6.0 A |
| Gate to Source Charge | Q _{GS} | | 7.1 | | nC | V _{DD} = -200 V |
| Gate to Drain Charge | Q _{GD} | | 12.9 | | nC | V _{GS} = -10 V |
| Body Diode Forward Voltage | V _{F(S-D)} | | 0.92 | | V | I _F = -6.0 A, V _{GS} = 0 |
| Reverse Recovery Time | t _{rr} | | 155 | | ns | I _F = -6.0 A, V _{GS} = 0 |
| Reverse Recovery Charge | Q _{rr} | | 930 | | nC | di/dt = 50 A/μs |

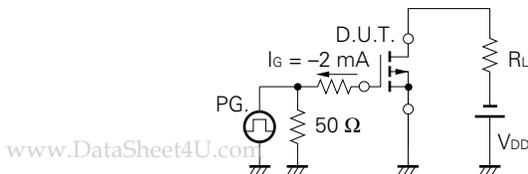
Test Circuit 1 Avalanche Capability



Test Circuit 2 Switching Time



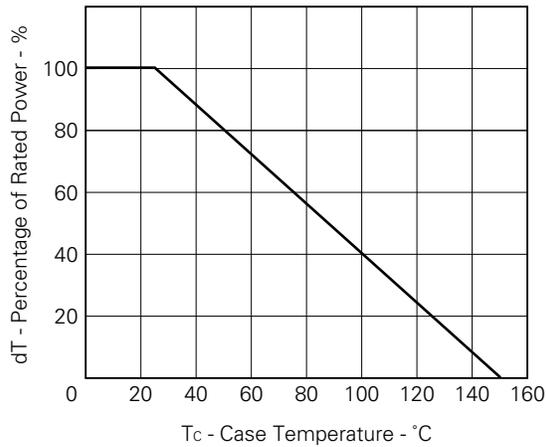
Test Circuit 3 Gate Charge



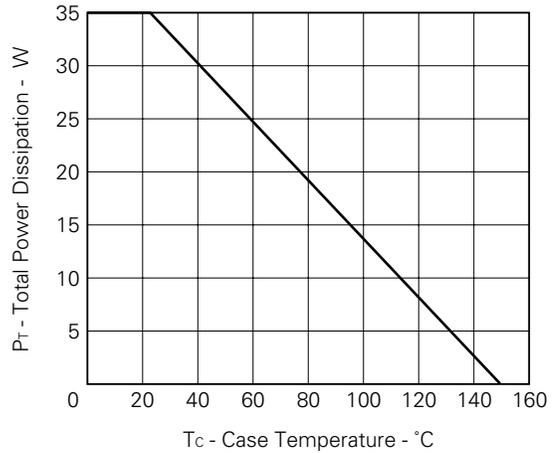
The application circuits and their parameters are for references only and are not intended for use in actual design-in's.

TYPICAL CHARACTERISTICS (T_A = 25 °C)

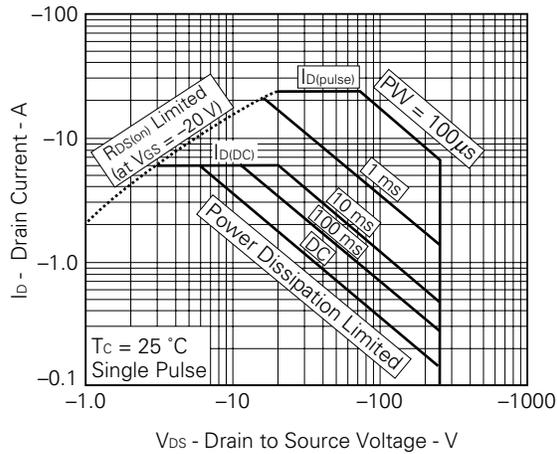
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



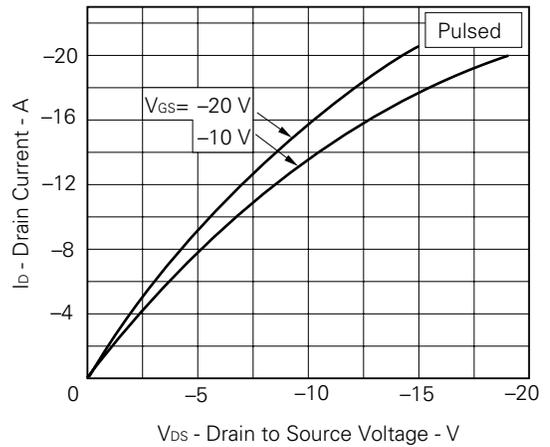
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



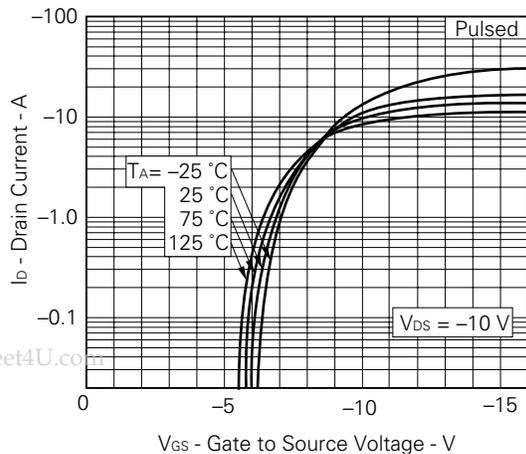
FORWARD BIAS SAFE OPERATING AREA



DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE

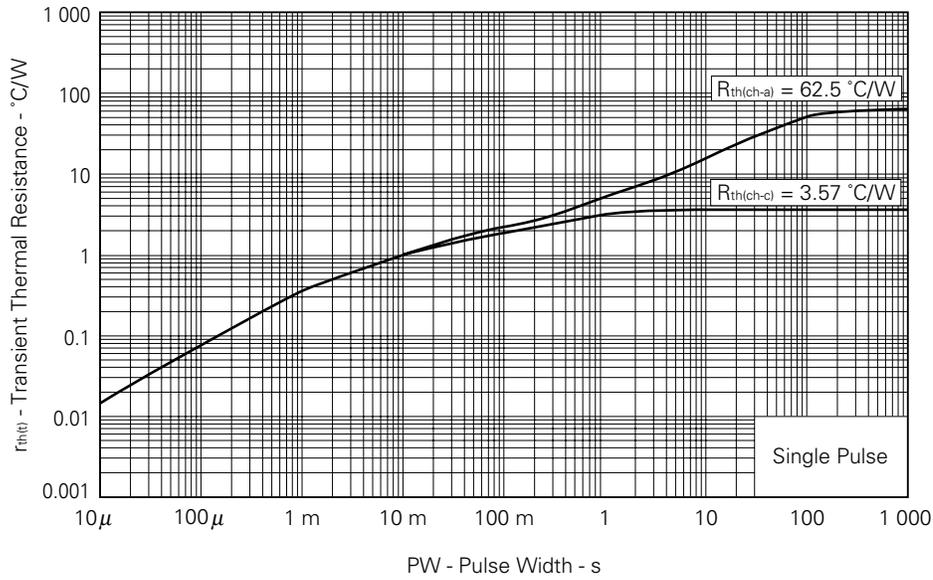


FORWARD TRANSFER CHARACTERISTICS

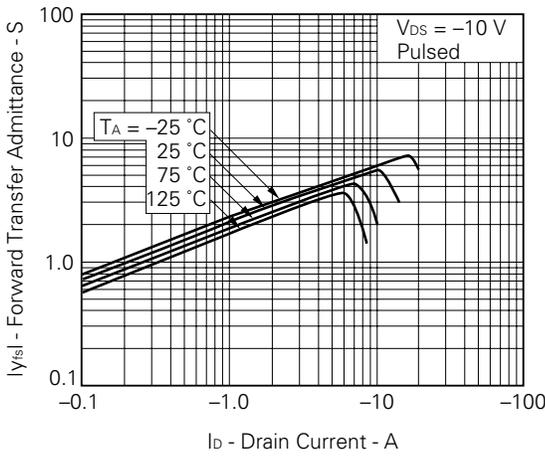


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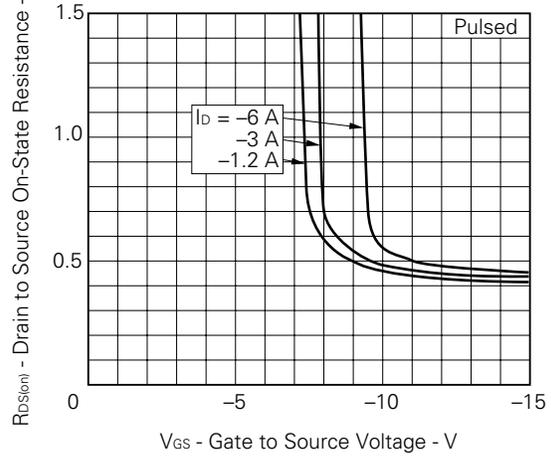
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



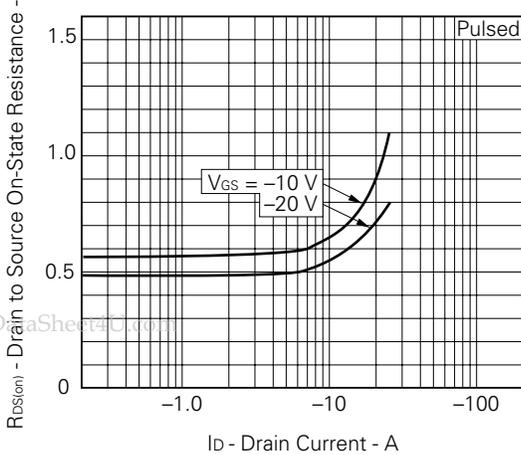
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



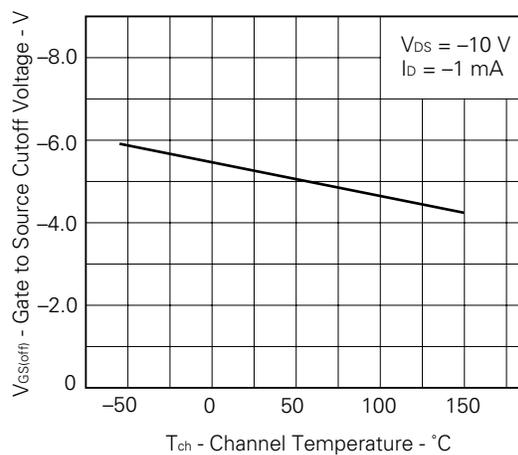
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT

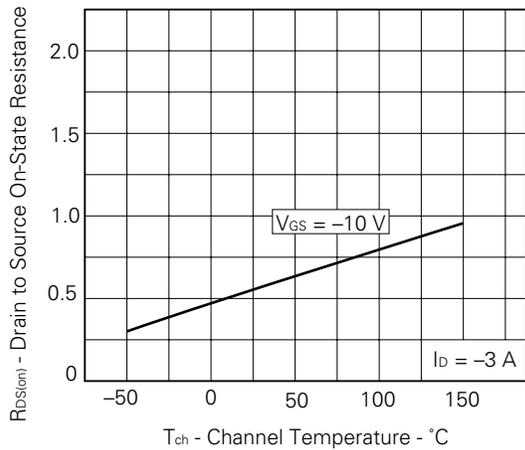


GATE TO SOURCE CUTOFF VOLTAGE vs. CHANNEL TEMPERATURE

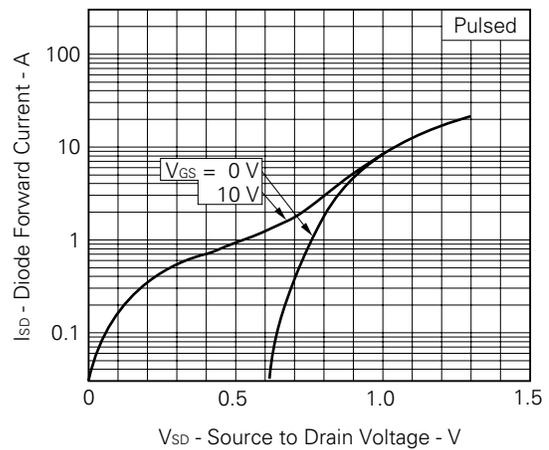


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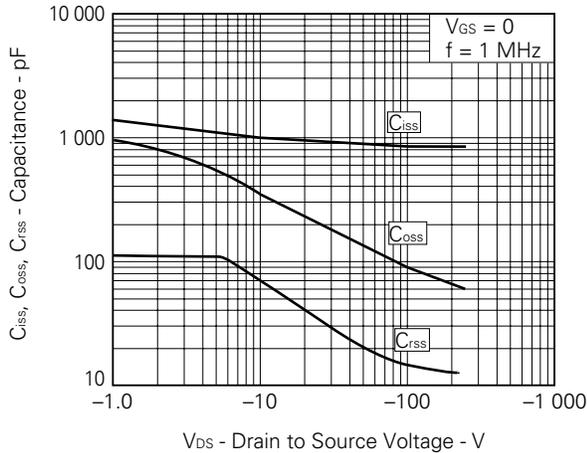
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



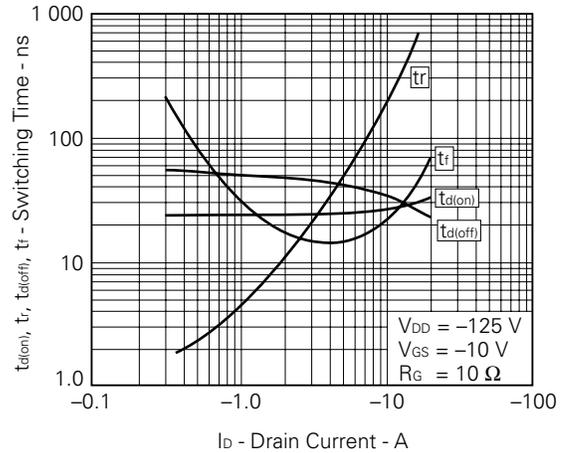
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



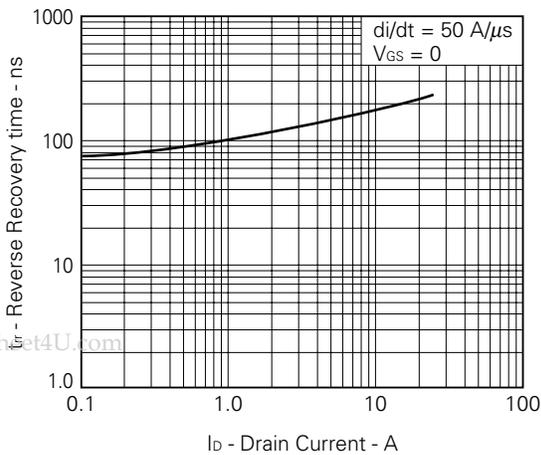
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



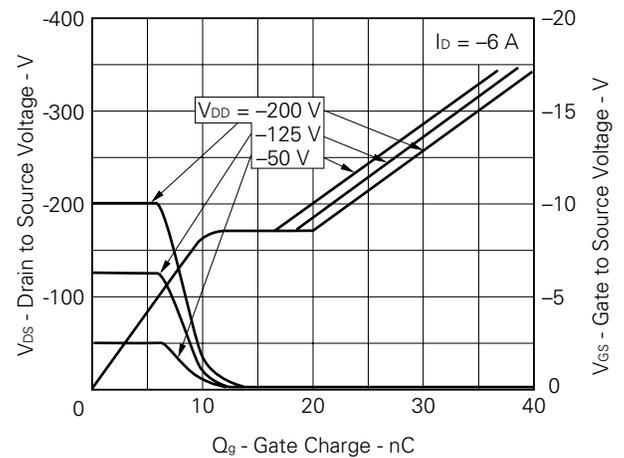
SWITCHING CHARACTERISTICS



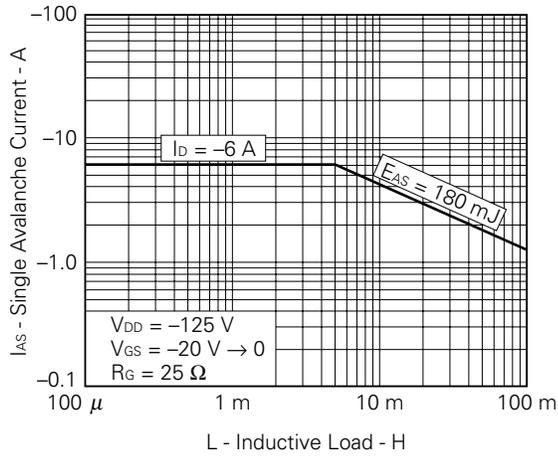
REVERSE RECOVERY TIME vs. DRAIN CURRENT



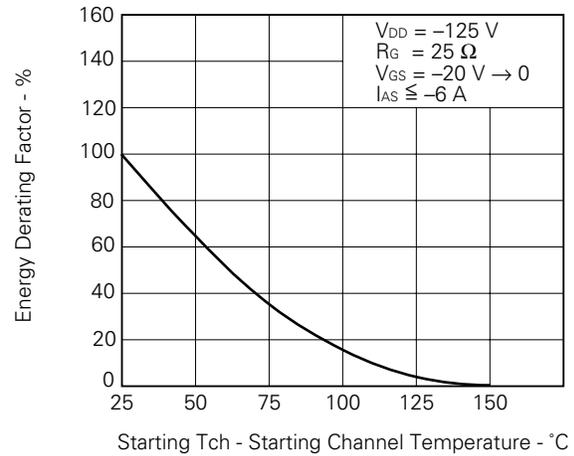
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



SINGLE AVALANCHE CURRENT vs. INDUCTIVE LOAD



SINGLE AVALANCHE ENERGY DERATING FACTOR



REFERENCE

| Document Name | Document No. |
|--|--------------|
| NEC semiconductor device reliability/quality control system. | TEI-1202 |
| Quality grade on NEC semiconductor devices. | IEI-1209 |
| Semiconductor device mounting technology manual. | IEI-1207 |
| Semiconductor device package manual. | IEI-1213 |
| Guide to quality assurance for semiconductor devices. | MEI-1202 |
| Semiconductor selection guide. | MF-1134 |
| Power MOS FET features and application switching power supply. | TEA-1034 |
| Application circuits using Power MOS FET. | TEA-1035 |
| Safe operating area of Power MOS FET. | TEA-1037 |

The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device is actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

[MEMO]

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Anti-radioactive design is not implemented in this product.

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