

Linear Systems replaces discontinued Siliconix SST405

The SST405 is a Low Noise, Low Drift, Monolithic Dual N-Channel JFET

The SST405 is a high-performance monolithic dual JFET featuring extremely low noise, tight offset voltage and low drift over temperature specifications, and is targeted for use in a wide range of precision instrumentation applications. The SST405 features a 5-mV offset and 10- $\mu\text{V}/^\circ\text{C}$ drift. The SST405 is a direct replacement for discontinued Siliconix SST405.

The 8 Pin P-DIP and 8 Pin SOIC provide ease of manufacturing, and the symmetrical pinout prevents improper orientation.

(See Packaging Information).

SST405 Applications:

- Wideband Differential Amps
- High-Speed, Temp-Compensated Single-Ended Input Amps
- High-Speed Comparators
- Impedance Converters and vibrations detectors.

FEATURES

LOW DRIFT	$ V_{GS1-2}/T = 10\mu\text{V}/^\circ\text{C}$ TYP.
LOW NOISE	$e_n = 6\text{nV}/\text{Hz}$ @ 10Hz TYP.
LOW PINCHOFF	$V_p = 2.5\text{V}$ TYP.

ABSOLUTE MAXIMUM RATINGS

@ 25°C (unless otherwise noted)

Maximum Temperatures

Storage Temperature	-65°C to +150°C
Operating Junction Temperature	+150°C

Maximum Voltage and Current for Each Transistor – Note 1

-V _{GSS}	Gate Voltage to Drain or Source	50V
-V _{DSO}	Drain to Source Voltage	50V
-I _{G(f)}	Gate Forward Current	10mA

Maximum Power Dissipation

Device Dissipation @ Free Air – Total	300mW
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MATCHING CHARACTERISTICS @ 25°C UNLESS OTHERWISE NOTED

SYMBOL	CHARACTERISTICS	VALUE	UNITS	CONDITIONS
$ V_{GS1-2}/T $ max.	DRIFT VS. TEMPERATURE	40	$\mu\text{V}/^\circ\text{C}$	$V_{DG}=10\text{V}$, $I_D=200\mu\text{A}$ $T_A=-55^\circ\text{C}$ to $+125^\circ\text{C}$
$ V_{GS1-2} $ max.	OFFSET VOLTAGE	20	mV	$V_{DG}=10\text{V}$, $I_D=200\mu\text{A}$

ELECTRICAL CHARACTERISTICS @ 25°C (unless otherwise noted)

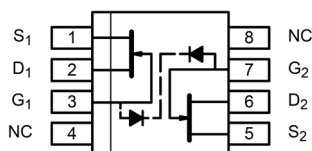
SYMBOL	CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS	CONDITIONS
BV _{GSS}	Breakdown Voltage	50	60	--	V	$V_{DS}=0$ $I_D=1\text{nA}$
BV _{GGO}	Gate-To-Gate Breakdown	± 50	--	--	V	$I_G=1\text{nA}$ $I_D=0$ $I_S=0$
TRANSCONDUCTANCE						
Y _{FSS}	Full Conduction	2000	--	7000	μmho	$V_{DG}=10\text{V}$ $V_{GS}=0\text{V}$ $f=1\text{kHz}$
Y _{FS}	Typical Operation	1000	--	2000	μmho	$V_{DG}=15\text{V}$ $I_D=200\mu\text{A}$ $f=1\text{kHz}$
$ Y_{FS1-2}/Y_{FS} $	Mismatch	--	0.6	3	%	
DRAIN CURRENT						
I _{DSS}	Full Conduction	0.5	--	10	mA	$V_{DG}=10\text{V}$ $V_{GS}=0\text{V}$
$ I_{DSS1-2}/I_{DSS} $	Mismatch at Full Conduction	--	1	5	%	
GATE VOLTAGE						
V _{GS(off)} or V _p	Pinchoff voltage	-0.5	--	-2.5	V	$V_{DS}=15\text{V}$ $I_D=1\text{nA}$
V _{GS(on)}	Operating Range	--	--	-2.3	V	$V_{DS}=15\text{V}$ $I_D=200\mu\text{A}$
GATE CURRENT						
-I _G max.	Operating	--	-4	-15	pA	$V_{DG}=15\text{V}$ $I_D=200\mu\text{A}$
-I _G max.	High Temperature	--	--	-10	nA	$T_A=+125^\circ\text{C}$
-I _{GSS} max.	At Full Conduction	--	--	100	pA	$V_{DS}=0$
-I _{GSS} max.	High Temperature	5	5	5	pA	$V_{DG}=15\text{V}$ $T_A=+125^\circ\text{C}$
OUTPUT CONDUCTANCE						
Y _{OSS}	Full Conduction	--	--	20	μmho	$V_{DG}=10\text{V}$ $V_{GS}=0\text{V}$
Y _{OS}	Operating	--	0.2	2	μmho	$V_{DG}=15\text{V}$ $I_D=500\mu\text{A}$
COMMON MODE REJECTION						
CMR	$-20 \log V_{GS1-2}/V_{DS} $	95	--	--	dB	$V_{DS}=10$ to 20V $I_D=30\mu\text{A}$
NOISE						
NF	Figure	--	--	0.5	dB	$V_{DS}=15\text{V}$ $V_{GS}=0\text{V}$ $R_G=10\text{M}$ $f=100\text{Hz}$ $\text{NBW}=6\text{Hz}$
e _n	Voltage	--	20	--	nV/ $\sqrt{\text{Hz}}$	$V_{DS}=15\text{V}$ $I_D=200\mu\text{A}$ $f=10\text{Hz}$ $\text{NBW}=1\text{Hz}$
CAPACITANCE						
C _{ISS}	Input	--	--	8	pF	$V_{DS}=15\text{V}$ $I_D=200\mu\text{A}$ $f=1\text{MHz}$
C _{RSS}	Reverse Transfer	--	--	1.5	pF	

Note 1 – These ratings are limiting values above which the serviceability of any semiconductor may be impaired

Available Packages:

SST405 in PDIP / SOIC
SST405 available as bare die
Please contact [Micross](http://www.micross.com) for full package and die dimensions

PDIP / SOIC (Top View)



Micross Components Europe



Tel: +44 1603 788967
Email: chipcomponents@micross.com
Web: <http://www.micross.com/distribution>