

Linear Systems replaces discontinued Siliconix / National SST5912C

The SST5912C are monolithic dual JFETs. The monolithic dual chip design reduces parasitics and gives better performance at very high frequencies while ensuring extremely tight matching. These devices are an excellent choice for use as wideband differential amplifiers in demanding test and measurement applications. The SST5912C is a direct replacement for discontinued Siliconix and National SST5912C.

The 8 Pin SOIC provides ease of manufacturing, and the symmetrical pinout prevents improper orientation. (See Packaging Information).

SST5912C Applications:

- Wideband Differential Amps
- High-Speed, Temp-Compensated Single-Ended Input Amps
- High-Speed Comparators
- Impedance Converters and vibrations detectors.

FEATURES

Improved Direct Replacement for SILICONIX & NATIONAL SST5912C

LOW NOISE (10KHz)

$e_n \sim 4\text{nV}/\sqrt{\text{Hz}}$

HIGH TRANSCONDUCTANCE (100MHz)

$g_{fs} \geq 4000\mu\text{S}$

ABSOLUTE MAXIMUM RATINGS¹
@ 25°C (unless otherwise noted)

Maximum Temperatures

Storage Temperature -65°C to +150°C

Operating Junction Temperature -55°C to +135°C

Maximum Power Dissipation

Continuous Power Dissipation (Total) 500mW

Maximum Currents

Gate Current 50mA

Maximum Voltages

Gate to Drain -25V

Gate to Source -25V

MATCHING CHARACTERISTICS @ 25°C (unless otherwise stated)

SYMBOL	CHARACTERISTIC	MIN	TYP	MAX	UNITS	CONDITIONS
$ V_{GS1} - V_{GS2} $	Differential Gate to Source Cutoff Voltage	--	--	40	mV	$V_{DG} = 10\text{V}, I_D = 5\text{mA}$
$\Delta V_{GS1} - V_{GS2} / \Delta T$	Differential Gate to Source Cutoff Voltage Change with Temperature	--	--	40	$\mu\text{V}/^\circ\text{C}$	$V_{DG} = 10\text{V}, I_D = 5\text{mA}$ $T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$
I_{DSS1} / I_{DSS2}	Gate to Source Saturation Current Ratio	0.95	--	1	%	$V_{DS} = 10\text{V}, V_{GS} = 0\text{V}$
$ I_{G1} - I_{G2} $	Differential Gate Current	--	--	20	nA	$V_{DG} = 10\text{V}, I_D = 5\text{mA}$ $T_A = +125^\circ\text{C}$
g_{fs1} / g_{fs2}	Forward Transconductance Ratio ²	0.95	--	1	%	$V_{DS} = 10\text{V}, I_D = 5\text{mA}, f = 1\text{kHz}$
CMRR	Common Mode Rejection Ratio	--	85	--	dB	$V_{DG} = 5\text{V}$ to $10\text{V}, I_D = 5\text{mA}$

ELECTRICAL CHARACTERISTICS @ 25°C (unless otherwise noted)

SYMBOL	CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS	CONDITIONS
BV_{GSS}	Gate to Source Breakdown Voltage	-25	--	--	V	$I_G = -1\mu\text{A}, V_{DS} = 0\text{V}$
$V_{GS(off)}$	Gate to Source Cutoff Voltage	-1	--	-5		$V_{DS} = 10\text{V}, I_D = 1\text{nA}$
$V_{GS(F)}$	Gate to Source Forward Voltage	--	0.7	--		$I_G = 1\text{mA}, V_{DS} = 0\text{V}$
V_{GS}	Gate to Source Voltage	-0.3	--	-4		$V_{DG} = 10\text{V}, I_G = 5\text{mA}$
I_{DSS}	Gate to Source Saturation Current ³	7	--	40	mA	$V_{DS} = 10\text{V}, V_{GS} = 0\text{V}$
I_{GSS}	Gate Leakage Current ³	--	-1	-50	pA	$V_{GS} = -15\text{V}, V_{DS} = 0\text{V}$
I_G	Gate Operating Current	--	-1	-50		$V_{DG} = 10\text{V}, I_D = 5\text{mA}$
g_{fs}	Forward Transconductance	4000	--	10000	μS	$V_{DG} = 10\text{V}, I_D = 5\text{mA}$
		4000	--	10000		
g_{os}	Output Conductance	--	--	100		
		--	--	150		
C_{iss}	Input Capacitance	--	--	5	pF	$V_{DG} = 10\text{V}, I_D = 5\text{mA}, f = 1\text{MHz}$
C_{rss}	Reverse Transfer Capacitance	--	--	1.2		
NF	Noise Figure	--	--	1	dB	$V_{DG} = 10\text{V}, I_D = 5\text{mA}, f = 10\text{kHz}, R_G = 100\text{K}\Omega$
e_n	Equivalent Input Noise Voltage	--	7	20	nV/ $\sqrt{\text{Hz}}$	$V_{DG} = 10\text{V}, I_D = 5\text{mA}, f = 100\text{Hz}$
		--	4	10		$V_{DG} = 10\text{V}, I_D = 5\text{mA}, f = 10\text{kHz}$

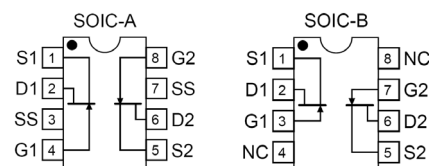
Notes: 1. Absolute Maximum ratings are limiting values above which serviceability may be impaired

2. Pulse Test: $PW \leq 300\mu\text{s}$ Duty Cycle $\leq 3\%$

3. Assumes smaller value in numerator

Available Packages:

SST5912C in SOIC
SST5912C available as bare die



Please contact Micross for full package and die dimensions:

Email: chipcomponents@micross.com
Web: www.micross.com/distribution.aspx