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YSS920B

EVE

32-bit DSP Engine for Various sound Effects

■ **Outline**

YSS920B is a 32-bit digital signal processor exclusively designed for sound field processing. As a post-processing DSP after surround sound decoding, YSS920B can process various sound fields such as various simulation surround and virtual surround through user programs, which can provide wide variation of sound field effects on audio equipments.

■ **Features**

YSS920B has following features:

- Basic compatibility with the SubDSP section of YSS922/932 for DSP program
- High precision processing by 32-bit floating-point operation
- Capability to process various sound effects by downloading external programs to the built-in RAM
- 16 channels processing capability (input: 16ch, output: 16ch)
- Zero data detecting function on each channel
- 32-bit data transmission ability between multiple YSS920Bs
- Connectability to most types of ADC, DAC and DIR through control register setting
- Built-in delay memory with 32 bits × 1024 words (Max. 21.3 ms at fs = 48 kHz)
- Ability to execute up to 2.73 seconds delay (at fs = 48 kHz) when connected with an external DRAM or SRAM
- Support for sampling frequencies from 32 kHz to 192 kHz
- DSP section specifications
  - Internal operating frequency: 30.72 to 50.00 MHz
  - Data bus width: 32 bits
  - MAC: 32 bits (floating-point) × 16 bits (fixed-point) + 49 bits → 49 bits
  - Program RAM: 50 bits × 1024 words
  - Coefficient RAM: 16 bits × 1024 words
- Ability to use up to 20 general-purpose input/output terminals
- Power supply voltage: 2.5 V (for internal and PLL circuits), 3.3 V (for I/O)
- Si-gate CMOS process
- Lead-free 100-pin SQFP package:YSS920B-SZ

YAMAHA CORPORATION

YSS920B CATALOG
CATALOG No.: LSI-4SS920B21
2006.8

■ Application

Sound field processing for AV amplifiers and audio mixers such as:
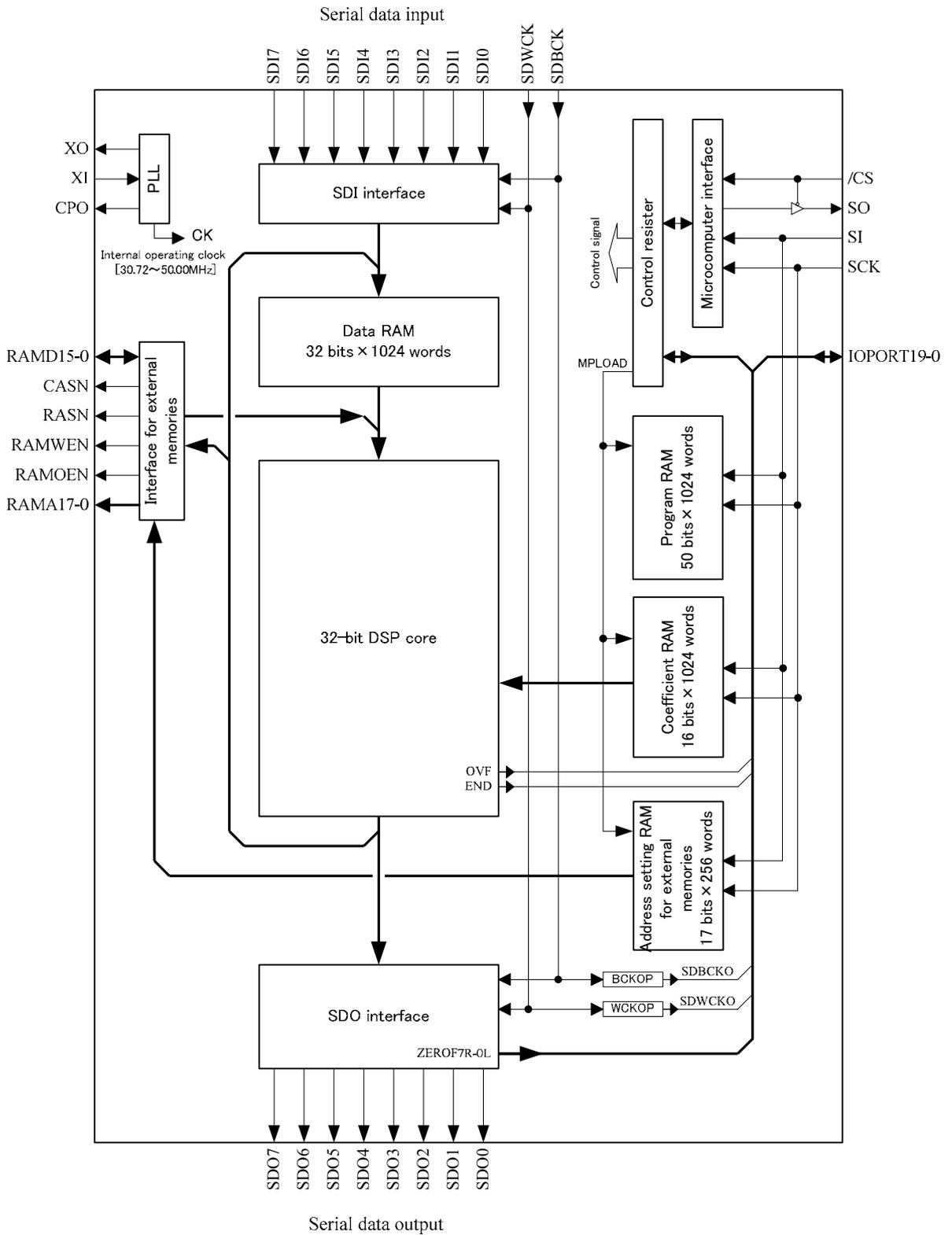1) Simulation surrounds for Hall, Theater, Church, Stadium, Disco, Jazz, and Live
2) Virtual surround
3) Bass Management
4) Filtering process for LPF, HPF, equalizer, etc.
5) Fader and Level meters
6) Generating white noise, pink noise, sine waves, etc.
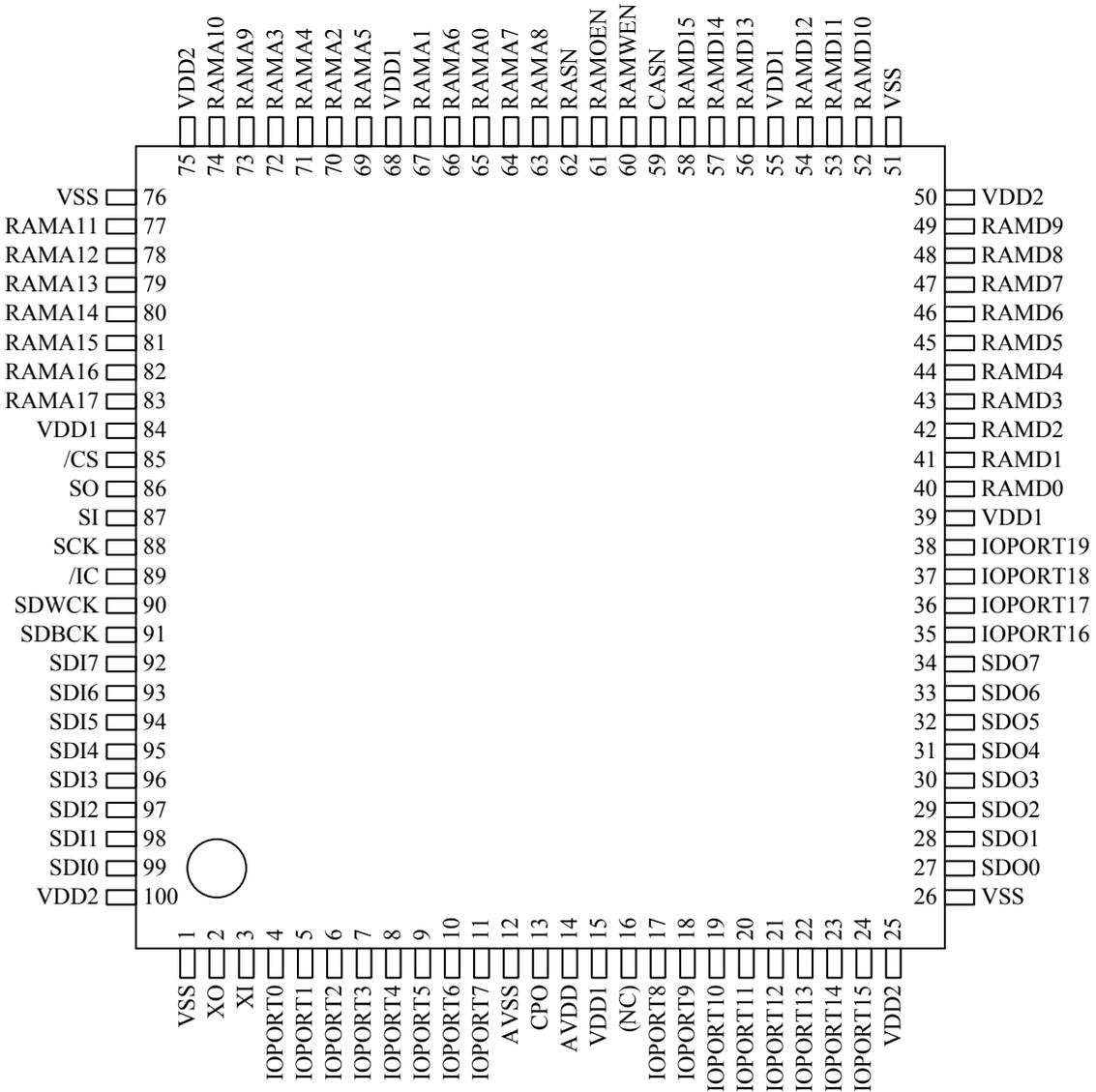
■ Difference between YSS920B and YSS920

The principal differences are as follows. Please sufficiently check that no problem occurs in your product when you replace YSS920 by YSS920B.

	Item	YSS920B	YSS920
1	Internal operating frequency	30.72 to 50.00MHz	30.72 to 40.96MHz
2	Power consumption (V_{DD1})	45mW (typ) / 65mW (max)	30mW (typ) / 45mW(max)
3	Power consumption (V_{DD2}/AV_{DD})	120mW (typ) / 145mW (max)	80mW (typ) / 115mW (max)
4	Power supply start-up order)	Defined (see p18 Power-on)	Undefined

■ Block Diagram

Serial data input

SDI7 SDI6 SDI5 SDI4 SDI3 SDI2 SDI1 SDI0 SDWCK SDBCK

XO
XI
CPO

PLL

CK

Internal operating clock
[30.72~50.00MHz]

SDI interface

Control resister

Microcomputer interface

Control signal

/CS
SO
SI
SCK

Data RAM
32 bits × 1024 words

RAMD15-0
CASN
RASN
RAMWEN
RAMOEN
RAMA17-0

Interface for external memories

MPLOAD

IOPORT19-0

Program RAM
50 bits × 1024 words

32-bit DSP core

Coefficient RAM
16 bits × 1024 words

OVF
END

Address setting RAM
for external
memories
17 bits × 256 words

SDO interface

BCKOP
WCKOP

SDBCKO
SDWCKO

ZEROF7R-0L

SDO7 SDO6 SDO5 SDO4 SDO3 SDO2 SDO1 SDO0

Serial data output

■ Pin Configuration

Top pins (left to right, 75 → 51):
VDD2, RAMA10, RAMA9, RAMA3, RAMA4, RAMA2, RAMA5, VDD1, RAMA1, RAMA6, RAMA0, RAMA7, RAMA8, RASN, RAMOEN, RAMWEN, CASN, RAMD15, RAMD14, RAMD13, VDD1, RAMD12, RAMD11, RAMD10, VSS

Left pins (76 → 100):
Pin	Name
76	VSS
77	RAMA11
78	RAMA12
79	RAMA13
80	RAMA14
81	RAMA15
82	RAMA16
83	RAMA17
84	VDD1
85	/CS
86	SO
87	SI
88	SCK
89	/IC
90	SDWCK
91	SDBCK
92	SDI7
93	SDI6
94	SDI5
95	SDI4
96	SDI3
97	SDI2
98	SDI1
99	SDI0
100	VDD2

Right pins (50 → 26):
Pin	Name
50	VDD2
49	RAMD9
48	RAMD8
47	RAMD7
46	RAMD6
45	RAMD5
44	RAMD4
43	RAMD3
42	RAMD2
41	RAMD1
40	RAMD0
39	VDD1
38	IOPORT19
37	IOPORT18
36	IOPORT17
35	IOPORT16
34	SDO7
33	SDO6
32	SDO5
31	SDO4
30	SDO3
29	SDO2
28	SDO1
27	SDO0
26	VSS

Bottom pins (left to right, 1 → 25):
VSS, XO, XI, IOPORT0, IOPORT1, IOPORT2, IOPORT3, IOPORT4, IOPORT5, IOPORT6, IOPORT7, AVSS, CPO, AVDD, VDD1, (NC), IOPORT8, IOPORT9, IOPORT10, IOPORT11, IOPORT12, IOPORT13, IOPORT14, IOPORT15, VDD2

< 100-pin SQFP top view >

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■ Pin Function

No.	Name	I/O	Functions
1	VSS	-	Digital ground pin
2	XO	O	Crystal oscillator connecting pin
3	XI	I	Crystal oscillator connecting pin (12.288 to 15.000 MHz)
4	IOPORT0	I+/O	General-purpose input/output pin / SDO 0 Lch zero-flag output pin / Program branch condition input/output pin
5	IOPORT1	I+/O	General-purpose input/output pin / SDO 0 Rch zero-flag output pin / Program branch condition input/output pin
6	IOPORT2	I+/O	General-purpose input/output pin / SDO 1 Lch zero-flag output pin / Program branch condition input/output pin
7	IOPORT3	I+/O	General-purpose input/output pin / SDO 1 Rch zero-flag output pin / Program branch condition input/output pin
8	IOPORT4	I+/O	General-purpose input/output pin / SDO 2 Lch zero-flag output pin / Program branch condition input/output pin
9	IOPORT5	I+/O	General-purpose input/output pin / SDO 2 Rch zero-flag output pin / Program branch condition input/output pin
10	IOPORT6	I+/O	General-purpose input/output pin / SDO 3 Lch zero-flag output pin / Program branch condition input/output pin
11	IOPORT7	I+/O	General-purpose input/output pin / SDO 3 Rch zero-flag output pin / Program branch condition input/output pin
12	AVSS	-	Analog ground pin (for PLL)
13	CPO	A	PLL filter connection pin
14	AVDD	-	+2.5 V analog power supply pin (for PLL)
15	VDD1	-	+3.3 V digital power supply pin (for input/output pin)
16	(NC)	-	(No connection)
17	IOPORT8	I+/O	General-purpose input/output pin / SDO 4 Lch zero-flag output pin
18	IOPORT9	I+/O	General-purpose input/output pin / SDO 4 Rch zero-flag output pin
19	IOPORT10	I+/O	General-purpose input/output pin / SDO 5 Lch zero-flag output pin
20	IOPORT11	I+/O	General-purpose input/output pin / SDO 5 Rch zero-flag output pin
21	IOPORT12	I+/O	General-purpose input/output pin / SDO 6 Lch zero-flag output pin / Chip address setting input pin 0
22	IOPORT13	I+/O	General-purpose input/output pin / SDO 6 Rch zero-flag output pin / Chip address setting input pin 1
23	IOPORT14	I+/O	General-purpose input/output pin / SDO 7 Lch zero-flag output pin / Chip address setting input pin 2
24	IOPORT15	I+/O	General-purpose input/output pin / SDO 7 Rch zero-flag output pin / Chip address setting input pin 3
25	VDD2	-	+2.5 V digital power supply pin (for internal circuits)
26	VSS	-	Digital ground pin
27	SDO0	O	PCM output pin
28	SDO1	O	PCM output pin
29	SDO2	O	PCM output pin
30	SDO3	O	PCM output pin
31	SDO4	O	PCM output pin
32	SDO5	O	PCM output pin
33	SDO6	O	PCM output pin
34	SDO7	O	PCM output pin
35	IOPORT16	I+/O	General-purpose input/output pin / Overflow detection output pin
36	IOPORT17	I+/O	General-purpose input/output pin / Program end detection output pin
37	IOPORT18	I+/O	General-purpose input/output pin / 64fs clock output pin
38	IOPORT19	I+/O	General-purpose input/output pin / fs clock output pin
39	VDD1	-	+3.3 V digital power supply pin (for input/output pin)
40	RAMD0	I+/O	Data input/output pin for external memory 0
41	RAMD1	I+/O	Data input/output pin for external memory 1
42	RAMD2	I+/O	Data input/output pin for external memory 2
43	RAMD3	I+/O	Data input/output pin for external memory 3
44	RAMD4	I+/O	Data input/output pin for external memory 4
45	RAMD5	I+/O	Data input/output pin for external memory 5
46	RAMD6	I+/O	Data input/output pin for external memory 6
47	RAMD7	I+/O	Data input/output pin for external memory 7
48	RAMD8	I+/O	Data input/output pin for external memory 8
49	RAMD9	I+/O	Data input/output pin for external memory 9

50	VDD2	-	+2.5 V digital power supply pin (for internal circuit)
51	VSS	-	Digital ground pin
52	RAMD10	I+/O	Data input/output pin for external memory 10
53	RAMD11	I+/O	Data input/output pin for external memory 11
54	RAMD12	I+/O	Data input/output pin for external memory 12
55	VDD1	-	+3.3 V digital power supply pin (for input/output pin)
56	RAMD13	I+/O	Data input/output pin for external memory 13
57	RAMD14	I+/O	Data input/output pin for external memory 14
58	RAMD15	I+/O	Data input/output pin for external memory 15
59	CASN	O	Column-address strobe output pin for external DRAM
60	RAMWEN	O	Write enable output pin for external memory
61	RAMOEN	O	Output-enable output pin for external memory
62	RASN	O	Row address strobe output pin for external DRAM
63	RAMA8	O	Address output pin for external memory 8
64	RAMA7	O	Address output pin for external memory 7
65	RAMA0	O	Address output pin for external memory 0
66	RAMA6	O	Address output pin for external memory 6
67	RAMA1	O	Address output pin for external memory 1
68	VDD1	-	+3.3 V digital power supply pin (for input/output pin)
69	RAMA5	O	Address output pin for external memory 5
70	RAMA2	O	Address output pin for external memory 2
71	RAMA4	O	Address output pin for external memory 4
72	RAMA3	O	Address output pin for external memory 3
73	RAMA9	O	Address output pin for external memory 9
74	RAMA10	O	Address output pin for external memory 10
75	VDD2	-	+2.5 V digital power supply pin (for internal circuit)
76	VSS	-	Digital ground pin
77	RAMA11	O	Address output pin for external memory 11
78	RAMA12	O	Address output pin for external memory 12
79	RAMA13	O	Address output pin for external memory 13
80	RAMA14	O	Address output pin for external memory 14
81	RAMA15	O	Address output pin for external memory 15
82	RAMA16	O	Address output pin for external memory 16
83	RAMA17	O	Address output pin for external memory 17
84	VDD1	-	+3.3 V digital power supply pin (for input/output pin)
85	/CS	Is	Microcomputer interface Chip select input pin
86	SO	Ot	Microcomputer interface Data output pin
87	SI	Is	Microcomputer interface Data input pin
88	SCK	Is	Microcomputer interface Clock input pin
89	/IC	Is	Initial clear input pin
90	SDWCK	I	Word clock (fs) input pin for SDI/SDO interface
91	SDBCK	Is	Bit clock (64fs) input pin for SDI/SDO interface
92	SDI7	I	PCM input pin
93	SDI6	I	PCM input pin
94	SDI5	I	PCM input pin
95	SDI4	I	PCM input pin
96	SDI3	I	PCM input pin
97	SDI2	I	PCM input pin
98	SDI1	I	PCM input pin
99	SDI0	I	PCM input pin
100	VDD2	-	+2.5 V digital power supply pin (for internal circuit)

I: Input terminal
Is: Schmitt trigger input terminal
I+:   Input terminal with pull-up circuit (*)
0:      Digital output terminal
0t: 3-state digital output terminal
A: Analog terminal

* Built in pull-up circuit cannot be used for Hi-level output of the LSI, because of this ability is only keep
Hi-level for input pin when it is open. Depending on a circuit, please use pull-up resistance.

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■ Pin Description

1) Serial data interface

- **SDI7-0**

  PCM data input pin for this LSI. Up to 16 channels of PCM data can be input.

  Connect unused pins to VSS.

  Select the input format by setting the SDI register.

- **SDO7-0**

  Output pin for the PCM signal processed by the DSP. Up to 16 channels of PCM data can be output.

  Select the output format by setting the SDO register.

- **SDBCK and SDWCK**

  Clock input pins for SDI input and SDO output.

  Input clock signals at 64fs to SDBCK and fs to SDWCK.

  See "■ Format for serial data interface" for the format.

2) External memory interface

- **RAMA17-0, RAMD15-0, RAMWEN, RAMOEN, CASN, and RASN**

  Pins for connecting the external memory for data delay.

  See "RAM interface" in " 4) AC characteristics" for the access timing.

3) Microprocessor interface

- **/CS, SCK, SI, and SO**

  4-line serial interfaces for reading/writing of the control register and for program downloading.

  See "■ Microprocessor interface format" for the format.

4) General-purpose input/output pins

- **IOPORT19-0**

  IOPORT0 to IOPORT19 can be used as general-purpose input/output ports.

  Select whether to use the pins as input pins (IPORT) or output pins (OPORT) by setting IOSEL 19-0 bits of the IOSEL registers (IOSEL_H, IOSEL_M, and IOSEL_L).

  If setup as an output pin (OPORT), you can select whether to output the value set to registers (OPORT_H, OPORT_M, and OPORT_L) or output various status signals by setting OPSEL 19-0 bits of registers (OPSEL_H, OPSEL_M, and OPSEL_L).

  Functions of the IOPORT pins can be set as follows:

Bit position	IOSEL setting	OPSEL setting	IOPORT function	Remarks
11-0	0	--	General input (IPORT)	IOPORT7-0 can be used for the conditional branching of DSP programs. See Note 4).
15-12	0	--	General input (IPORT)	Combined use with chip address setting terminal. See Note 1).
19-16	0	--	General input (IPORT)	
11-0	1	0	General output (OPORT)	IOPORT7-0 can be used for the conditional branching of DSP programs. See Note 4).
	1	1	Zero detection output	See Note 2)
15-12	1	0	General output (OPORT)	
	1	1	Zero detection output	See Note 2)
19-16	1	0	General output (OPORT)	
	1	1	Status output	See Note 3)

Note 1) Pins for chip address setting (IOPORT 15-12)
    These pins are also used as chip address setting pins:
            IOPORT 12-----chip address 0 (CA0)
            IOPORT 13-----chip address 1 (CA1)
            IOPORT 14-----chip address 2 (CA2)
            IOPORT 15-----chip address 3 (CA3)

Note 2) ZEROF output pins (IOPORT 15-0)
    By setting the IOSEL and the OPSEL, IOPORT 15-0 operate as digital zero detection pins for SDO output signal.
    If the SD0 output signal remains at digital zero consecutively for the number of samples specified by the ZEROB register, the flag output pin of the corresponding channel is set to H. This flag output pin can be used for analog mute after DAC.
    The channels correspond to the pins as follows:

            IOPORT0 -----   ZEROF0L (SDO0 Lch)
            IOPORT1 -----   ZEROF0R (SDO0 Rch)
            IOPORT2 -----   ZEROF1L (SDO1 Lch)
            IOPORT3 -----   ZEROF1R (SDO1 Rch)
            IOPORT4 -----   ZEROF2L (SDO2 Lch)
            IOPORT5 -----   ZEROF2R (SDO2 Rch)
            IOPORT6 -----   ZEROF3L (SDO3 Lch)
            IOPORT7 -----   ZEROF3R (SDO3 Rch)
            IOPORT8 -----   ZEROF4L (SDO4 Lch)
            IOPORT9 -----   ZEROF4R (SDO4 Rch)
            IOPORT10-----   ZEROF5L (SDO5 Lch)
            IOPORT11-----   ZEROF5R (SDO5 Rch)
            IOPORT12-----   ZEROF6L (SDO6 Lch)
            IOPORT13-----   ZEROF6R (SDO6 Rch)
            IOPORT14-----   ZEROF7L (SDO7 Lch)
            IOPORT15-----   ZEROF7R (SDO7 Rch)

Note 3) Various status signal output pins

By setting the IOSEL and the OPSEL, the following status signals will be output from each pin:

IOPORT16-----	OVF
IOPORT17-----	END
IOPORT18-----	SDBCKO (64fs clock)
IOPORT19-----	SDWCKO (fs clock)

OVF   If overflow occurs in the operation result of the DSP, OVF is set to H.
The H interval is from the occurrence of the overflow to the output start of the next PCM sample from the SDO interface. When the next PCM sample output starts, OVF is reset to L. This pin is used for DSP programming and debugging.

END   END is set to H when the DSP program counter is active. It is set to L when all processes have been finished and the program counter stops. When the program is operating correctly, the pin is always set to L once per sample. If it is not, this indicates that the program has not finished correctly to the end. This pin is used for DSP programming and debugging.

SDBCKO   This pin outputs 64fs clock synchronized to the SDO output signal. This clock can be used as a 64fs clock for the devices in subsequent stages. The polarity of the SDBCKO clock can be selected by setting BCKOP of the SDO register.

SDWCKO   This pin outputs fs clock synchronized to the SDO output signal. This clock can be used as an fs clock for the devices in subsequent stages. The polarity of the SDWCKO clock can be selected by setting WCKOP of the SDO register.

The structure of the LSI for each pin of IOPORT 19-0 is shown below:

Structure of the LSI
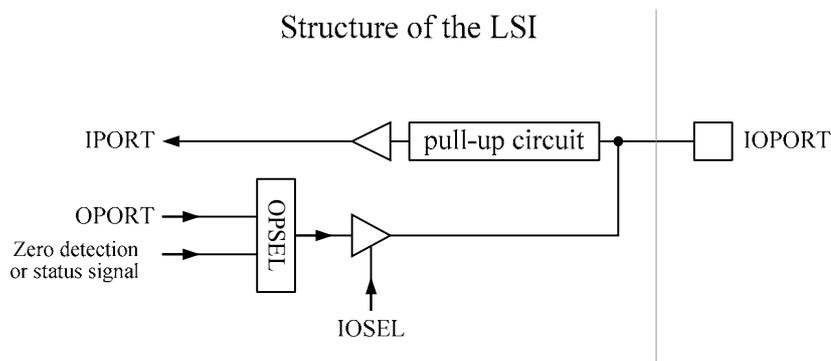
Note 4) When the pins are set to input mode, set a branch condition directly to each pin.
When the pins are set to output mode, IOPORT output can be used as the branch condition.

5) Clock

- ### XI and XO

Pins for connecting a crystal oscillator (12.288 to 15.000 MHz). Use a crystal oscillator with a fundamental wave.

If an external clock is used, connect it to XI.

Internal operation clock (ck) is set with the oscillating frequency of this crystal oscillator and the setting of the CKUP bit of the ERAM register.

	CKUP=0	CKUP=1
I=12.288 MHz	CK=30.72 MHz	CK=40.96 MHz
⋮	⋮	⋮
XI=14.000 MHz	CK=35.00 MHz	CK=46.66MHz
⋮	⋮	—
XI=15.000 MHz	CK=37.50 MHz	CK=50.00MHz

- ### CPO, AVDD, and AVSS

Pins for connecting external elements for the PLL used to generate a clock pulse in the DSP section. Connect resistor and capacitors near the CPO as shown below.

Connect decoupling capacitors near the pin between AVDD and AVSS.

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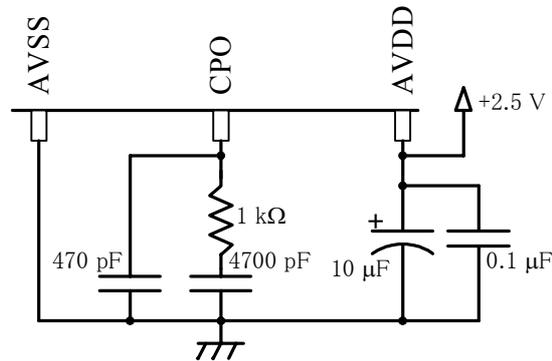
■ Register map

This LSI is controlled by reading/writing the registers below through the microcomputer interface (/CS, SCK, SI, and SO).

See "■ Microprocessor interface format" for the microcomputer interface format.

All the registers except addresses 0x13 and 0x14 are reset to 0 when initial clear (/IC=L) is executed. The initial values of addresses 0x13 and 0x14 are undefined.

Address	Name	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0x00	CHIP ADR	CAE				CA3-0			
0x01	SDI	NOEXP		SDIFMT1-0		SDIBIT1-0		SDWP	SDBP
0x02	SDO			SDOFMT1-0		SDOBIT1-0		WCKOP	BCKOP
0x03	ERAM	CKUP				RASREF	ERAMMOD	ERAMSEL1-0	
0x04	IOSEL_H					IOSEL19-16			
0x05	IOSEL_M	IOSEL15-8							
0x06	IOSEL_L	IOSEL7-0							
0x07	OPSEL_H					OPSEL19-16			
0x08	OPSEL_M	OPSEL15-8							
0x09	OPSEL_L	OPSEL7-0							
0x0A	OPORT_H					OPORT19-16			
0x0B	OPORT_M	OPORT15-8							
0x0C	OPORT_L	OPORT7-0							
0x0D	IPORT_H					IPORT19-16			
0x0E	IPORT_M	IPORT15-8							
0x0F	IPORT_L	IPORT7-0							
0x10	MPCNT_H	MPLOAD	MPCLEARN	DSPMUTEN		MPCNT11-8			
0x11	MPCNT_L	MPCNT7-0							
0x12	ZEROB	ZEROB7-0							
0x13	ZEROF_H	ZEROF7R	ZEROF7L	ZEROF6R	ZEROF6L	ZEROF5R	ZEROF5L	ZEROF4R	ZEROF4L
0x14	ZEROF_L	ZEROF3R	ZEROF3L	ZEROF2R	ZEROF2L	ZEROF1R	ZEROF1L	ZEROF0R	ZEROF0L
0x15	MI STATE	MI7S	MI6S	MI5S	MI4S	MI3S	MI2S	MI1S	MI0S
0x16	TEST								
0x17	TEST								
0x18 : 0x1F	Invalid	Output of SO pin becomes High-Z.							
0x20	MI00	MI0REG31-24							
0x21	MI01	MI0REG23-16							
0x22	MI02	MI0REG15-8							
0x23	MI03	MI0REG7-0							
0x24	MI10	MI1REG31-24							
0x25	MI11	MI1REG23-16							
0x26	MI12	MI1REG15-8							
0x27	MI13	MI1REG7-0							
0x28	MI20	MI2REG31-24							
0x29	MI21	MI2REG23-16							
0x2A	MI22	MI2REG15-8							
0x2B	MI23	MI2REG7-0							
0x2C	MI30	MI3REG31-24							
0x2D	MI31	MI3REG23-16							
0x2E	MI32	MI3REG15-8							
0x2F	MI33	MI3REG7-0							
0x30	MI40	MI4REG31-24							
0x31	MI41	MI4REG23-16							

0x32	MI42	MI4REG15-8							
0x33	MI43	MI4REG7-0							
0x34	MI50	MI5REG31-24							
0x35	MI51	MI5REG23-16							
0x36	MI52	MI5REG15-8							
0x37	MI53	MI5REG7-0							
0x38	MI60	MI6REG31-24							
0x39	MI61	MI6REG23-16							
0x3A	MI62	MI6REG15-8							
0x3B	MI63	MI6REG7-0							
0x3C	MI70	MI7REG31-24							
0x3D	MI71	MI7REG23-16							
0x3E	MI72	MI7REG15-8							
0x3F	MI73	MI7REG7-0							
0x40 : 0x7E	Invalid	Output of SO pin becomes High-Z.							
0x7F	DEVICE ID	0	0	0	0	0	0	1	0

Note

i) [shaded box] Do not write '1' in the shaded area in the above table, because test bits are allocated.

ii) Do not access addresses 0x16 and 0x17 because they are test registers.

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■ Format for serial data interface

Input/output of PCM signals are performed through:
- · SDI interface, and
- · SDO interface.

1) SDI interface: (Serial data input)

The input format of serial data is as follows in accordance with the setting of the SDI register.
Regardless of the setting, the input signal to the SDI7-0 pins is processed as 32-bit data consisting of 28-bit mantissa and 4-bit exponent.
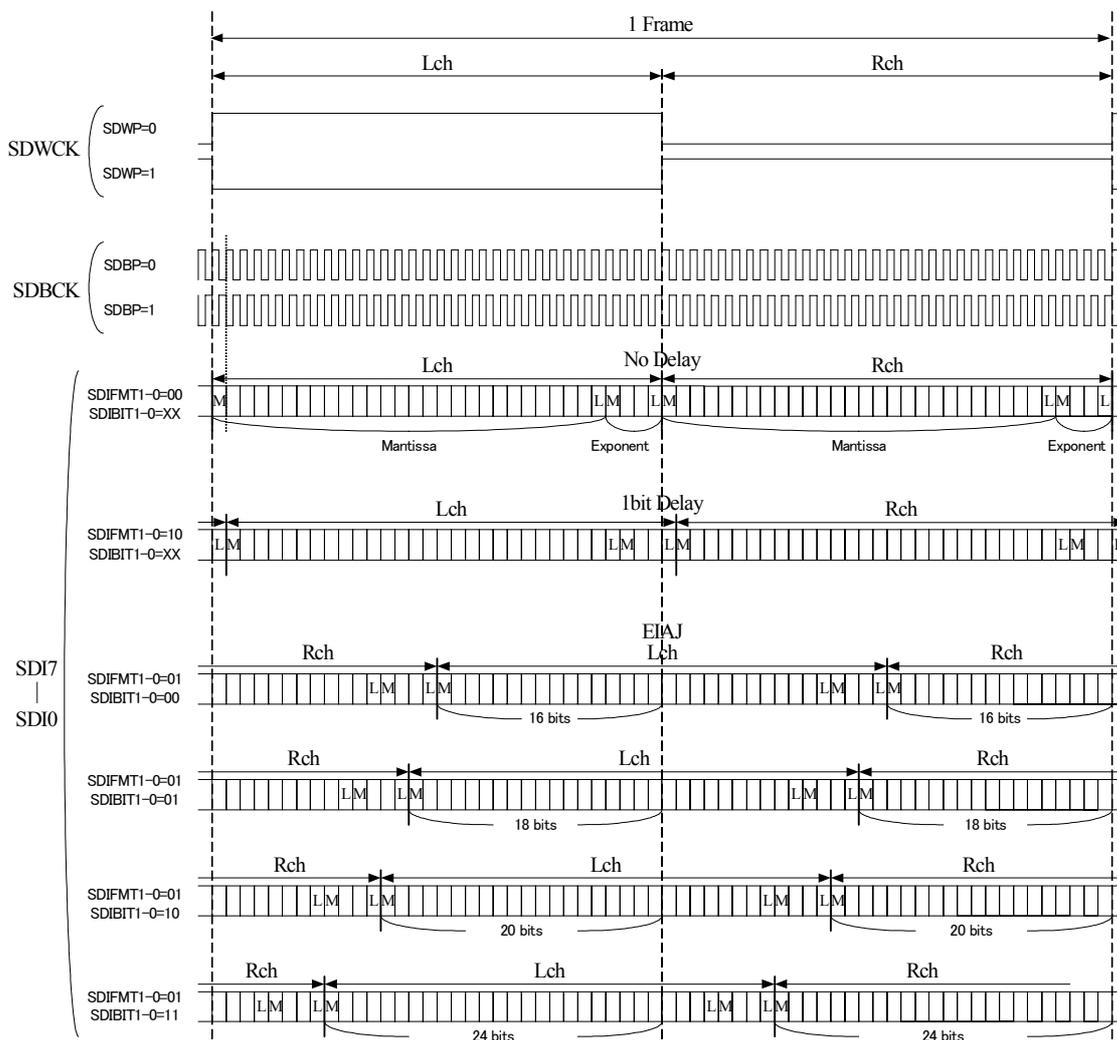
M : MSB   L : LSB

2) SDO interface: (Serial data output)

The output format of serial data is as follows in accordance with the setting of the SDO register. Regardless of the setting, 32-bit data consisting of 28-bit mantissa and 4-bit exponent is always output from the SDO7-0 pins.

When passing the SDO7-0 output to other devices such as the D/A, specify fixed-point number (linear) output in the DSP program. When multiple YSS920Bs are used, 32-bit data consisting of 28-bit mantissa and 4-bit exponent can be passed by specifying floating-point (float) output.

M : MSB   L : LSB

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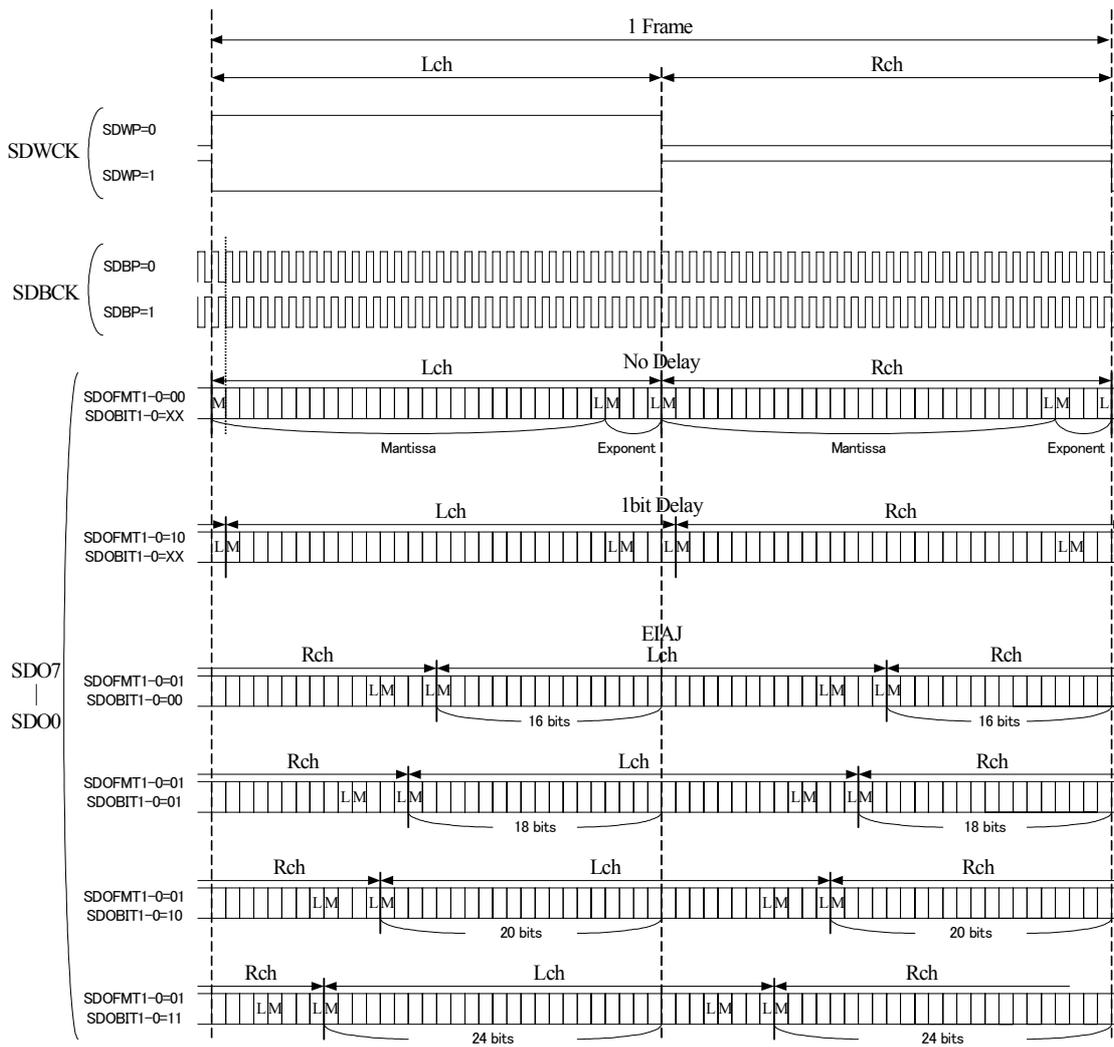
■ Microprocessor interface format

Reading/writing of the internal control register is performed through the 4-line serial interface as shown below:

1) When /CS is used only by one device
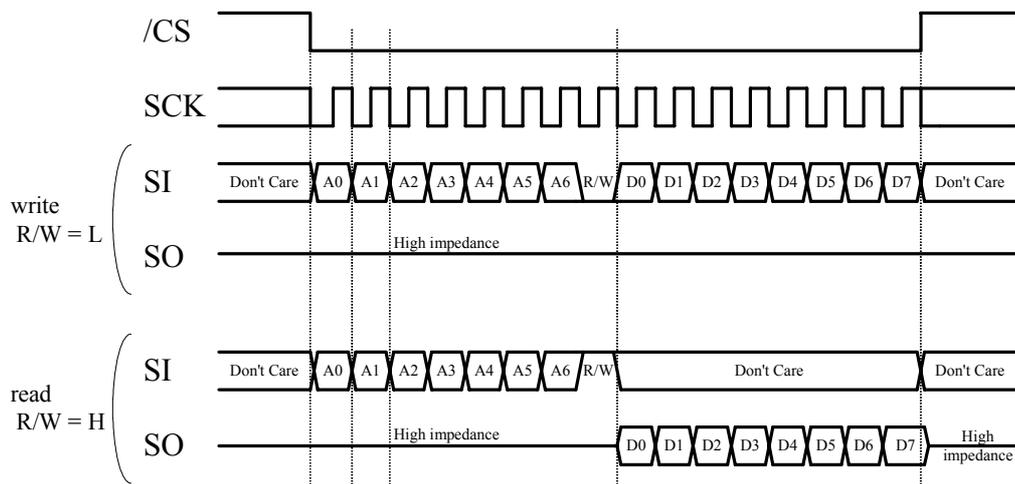
SO is set to output mode only when all of the following conditions are met:
- When /CS=L
- When reading a valid address setting
- During the output timing of data (8-bit).

In all other cases, it is set to High-Z, so that SO, SI, and SCK can be shared with devices having similar interfaces. When multiple YSS920Bs are used, /CS can also be shared by specifying CHIP ADR register CA3-0. See the next Section " 2) ".

If the general-purpose input/output pin (IOPORT19-0) is used as an input pin (IPORT), then the IOPORT (IPORT) value during the period of "R/W" shown above will be read through SO.
If it is used as an output pin (OPORT), then the IOPORT (OPORT) output will be switched over at the time of SCK rising edge on "D7" shown above.

[Note]   Set /CS to H during initial clear (/IC=L).

2) When /CS is shared with multiple devices

When multiple YSS920Bs are used or /CS is shared with other LSI, be sure to set CAE=1 and CA 3-0 immediately after the falling edge of /CS as shown in the following figure.

For details, refer to "0x00 CHIP ADR Register" description in the section 3.2 Register Details.
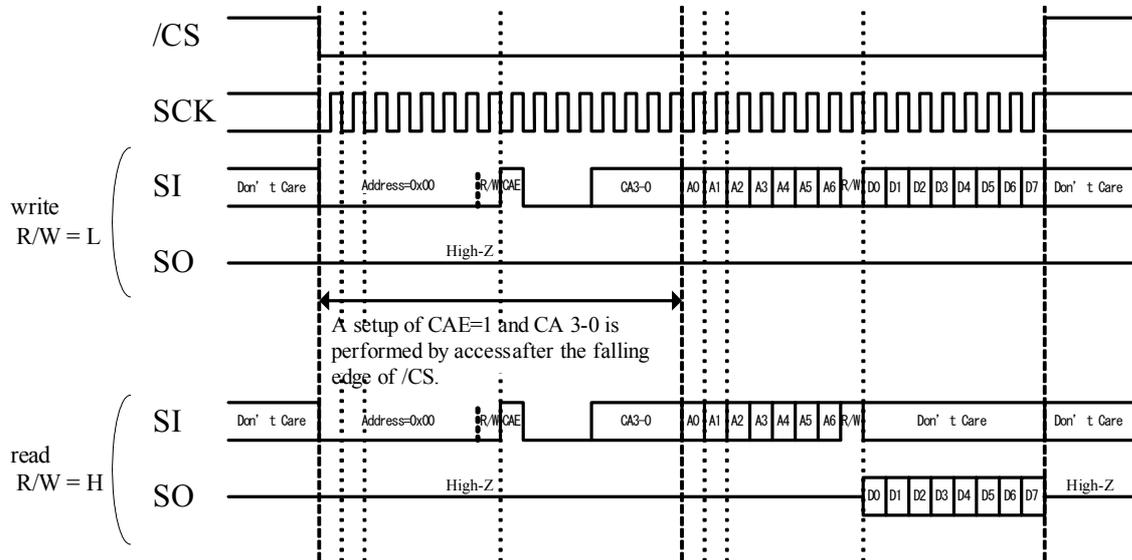
[Note]   Set /CS = high during initial clear (/IC = low).

YSS920B

■ Electrical characteristics

1) Absolute maximum ratings

Items	Symbol	Condition	Min	Typ	Max	Unit
Power-supply voltage	V_{DD1}		V_{SS} -0.5		V_{SS} +4.6	V
	AV_{DD}		V_{SS} -0.5		V_{SS} +3.6	V
	V_{DD2}		V_{SS} -0.5		V_{SS} +3.6	V
Input voltage	VI	Pins other than XI pin *1	-0.5		V_{SS} +5.75	V
		XI pin	-0.5		V_{DD1}+0.5	V
Storage temperature	Tstg		-50		125	°C

*1: Using a 5 V tolerant input pin.

2) Recommended operating conditions

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Power supply voltage	V_{DD1}	Internal Operation Frequency 30.72MHz to 50.00MHz	3.0	3.3	3.6	V
	AV_{DD}		2.3	2.5	2.7	V
	V_{DD2}		2.3	2.5	2.7	V
Operating temperature	Top		-40	25	85	°C

3) DC characteristics

Condition: Under recommended condition

Items	Symbol	Condition	Min	Typ	Max	Unit
Input voltage H level (1)	V_{IH1}	*1	0.7 V_{DD1}			V
Input voltage L level (1)	V_{IL1}	*1			0.3 V_{DD1}	V
Input voltage H level (2)	V_{IH2}	*2	2.4			V
Input voltage L level (2)	V_{IL2}	*2			0.8	V
Input voltage H level (3)	V_{IH3}	*3	2.2			V
Input voltage L level (3)	V_{IL3}	*3			0.8	V
Output voltage H level	V_{OH}	I_{OH} = -80 μ A	V_{DD1}-0.4			V
Output voltage L level	V_{OL}	I_{OL} = 1.0 mA			0.4	V
Input leak current (1)	I_{LI1}	Applies to all input pins other than pull-up pin.			$\pm$10	μ A
Input leak current (2)	I_{LI2}	Applies to pull-up pin			+10／-90	μ A
Power consumption (V_{DD1})	P_{D1}	*4		45	65	mW
Power consumption (V_{DD2} /AV_{DD})	P_{D2}	*4		120	145	mW

*1　Applied to the XI input pin.
*2　Applied to the /IC input pin.
*3　Applied to the input pins other than above.
*4　Power consumption largely depends on the DSP program, DSP internal operation clock, and other items to be operated.
　　Values listed above are measured under the following conditions:
　　　　・50.00 MHz DSP internal operation clock
　　　　・fs=96 kHz data input to SDI7-0 pin
　　　　・Using SRAM (ERAMSEL1-0=10) as external RAM
　　　　・Using a YAMAHA evaluation board
　　　　・Using programs that are assumed to produce a high level of processing (maximum number of
　　　　　steps, frequent access to external RAM)
　　"The standard values" are obtained at V_{DD1}=3.3 V and V_{DD2}=AV_{DD}=2.5 V
　　"The Maximum values" are obtained at V_{DD1}=3.6 V and V_{DD2}=AV_{DD}=2.7 V

4) AC characteristics

Condition: Under recommended condition

● **Clock**

No.	Item	Symbol	Condition	Min.	Typ.	Max.	Unit
1	XI clock frequency	f_{xin}		12.288		15.000	MHz
2	XI clock duty	X_{duty}		40		60	%
3	PLL lock frequency	f_{xpll}			$f_{xin} \times 10$		MHz
4	PLL lock-up time	t_{lpll}				900	μs
5	CK (Internal operation clock)	t_{ckc}	CKUP = 0 $12.288_{MHz} \leq f_{xin} \leq 15.000_{MHz}$	26.66	$1/(f_{xpll}/4)$	32.55	ns
			CKUP = 1 f_{xin} = 12.288 MHz	20.00	$1/(f_{xpll}/3)$	24.41	ns

● **Power-on / Hardware Reset**

No.	Items	Symbol	Condition	Min.	Typ.	Max.	Unit
6	/IC low time	t_{icl}	*1	1			ms
7	Power-on time *4	t_{V1V2}	*2	0		1	s
			*3	-1		1	s
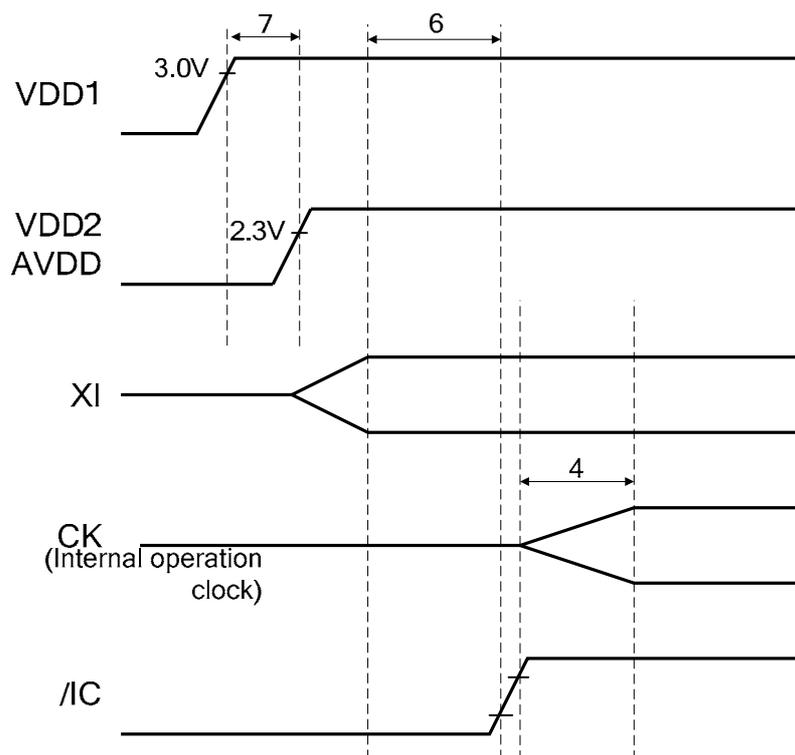
*1: Be sure to set /IC to L at power-up. Set /IC to H 1 ms after VDD1, VDD2, and AVDD of the power supply and XI input have stabilized.
Also, the initial setting of the control register and the downloading of programs shall be started 1 ms after setting /IC to H.

*2: When a Schottky barrier diode is not connected
The 3.3 V power supply (VDD1) voltage should be higher than the 2.5V power supply (VDD2 and AVDD) voltage at anytime (at the time of power on and power off).

*3: When a Schottky barrier diode is connected

Insert a Schottky barrier diode with a forward voltage of 0.4 V or less between the 3.3 V power supply (VDD1) and 2.5 V power supply (VDD2 and AVDD) (cathode is VDD1 and anode is VDD2). Power on and power off order do not matter and it do not need to care voltage relation for the 3.3 V power supply and the 2.5 V power supply.

*4: The time lag of power ON or OFF between 3.3V power supply and 2.5V power supply must be within one second. Only one power keeps on supplying, LSI would be damaged.

● **Microprocessor interface**

No.	Items	Symbol	Condition	Min.	Typ.	Max.	Unit
1	SCK cycle	tcc		160			ns
2	SCK rise time	tcr				20	ns
3	SCK fall time	tcf				20	ns
4	SCK high level time	tch		80			ns
5	SCK low level time	tcl		80			ns
6	/CS, SI setup time	tset		10			ns
7	/CS, SI hold time	thold		50			ns
8	SO delay time	tdelay	C_L=50 pF			50	ns
9	/CS high level time	tcsnh		160			ns

(when reading)
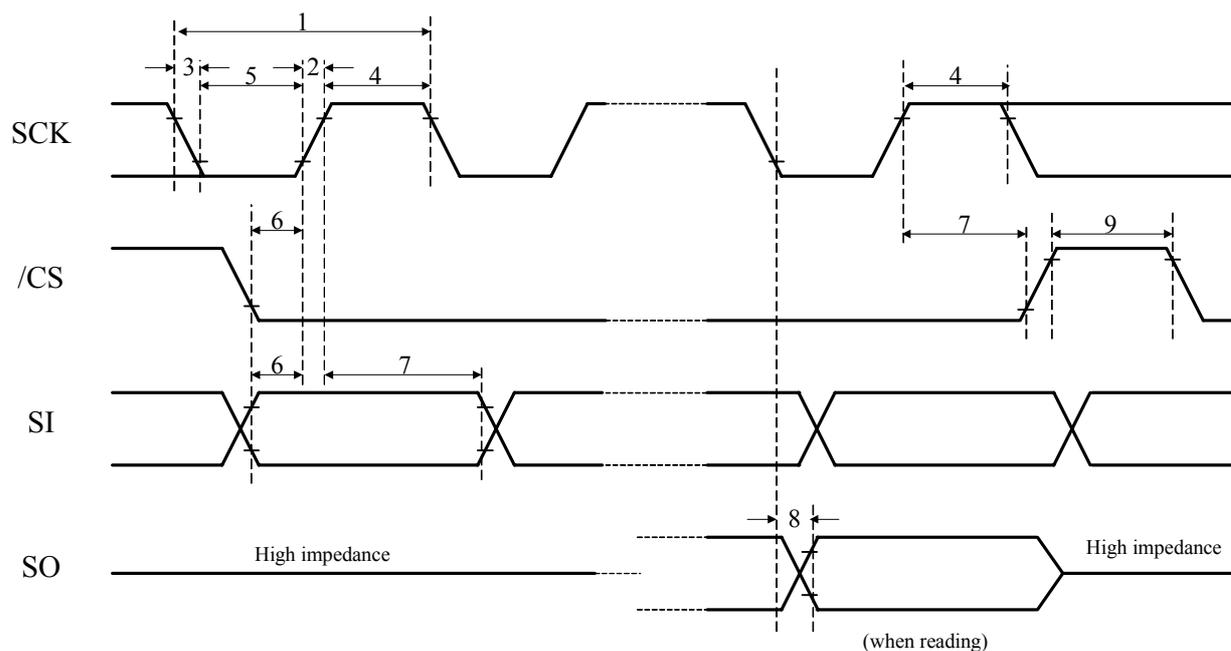
● **Serial data interface**

No.	Items	Symbol	Condition	Min.	Typ.	Max.	Unit
1	SDBCK input frequency	f_{bck}		2		12.3	MHz
2	SDBCK rise time	t_{ibr}				20	ns
3	SDBCK fall time	t_{ibf}				20	ns
4	Input setup time	t_{is}		5			ns
5	Input hold time	t_{ih}		10			ns
6	Output delay from input clock	t_{iodly}	$C_L=50$ pF			50	ns
7	Clock delay time	t_{bdly}	$C_L=50$ pF			50	ns
8	Output delay time from output clock	t_{oodly}	$C_L=50$ pF	-10		10	ns
9	SDBCKO rise time	t_{obr}	$C_L=50$ pF			20	ns
10	SDBCKO fall time	t_{obf}	$C_L=50$ pF			20	ns
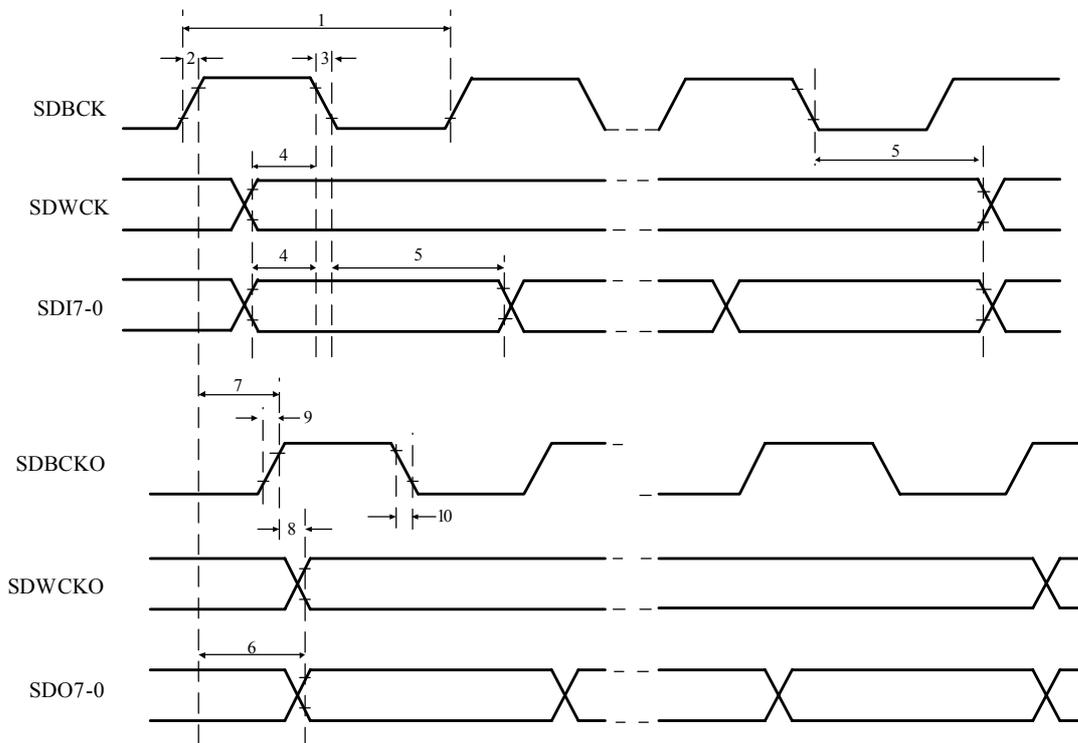
・ SDBCKO will be output from the IOPORT18 pin by setting IOSEL18=1 and OPSEL18=1.
・ SDWCKO will be output from the IOPORT19 pin by setting IOSEL19=1 and OPSEL19=1.
・ When SDBP=1, the polarity of SDBCK is inverted.
・ When BCKOP=1, the polarity of SDBCK becomes opposite to SDBCKO.
・ When WCKOP=1, the polarity of SDWCK becomes opposite to SDWCKO.

● **RAM interface**

In ERAMSEL 1-0=1* (SRAM/high speed SRAM mode)   (CL=20 pF)

No.	Items	Symbol	Condition	Min.	Typ.	Max.	Unit
1	(When reading) Read cycle	t_{rc}	ERAMSEL1-0=11		$t_{ckc} \times 2$		ns
			ERAMSEL1-0=10		$t_{ckc} \times 3$		ns
2	Data input setup time	t_{dis}		20			ns
3	Data input hold time	t_{dih}		0			ns
4	Address delay time	t_{ad}				10	ns
5	(When writing) Write cycle time	t_{wc}	ERAMSEL1-0=11		$t_{ckc} \times 2$		ns
			ERAMSEL1-0=10		$t_{ckc} \times 3$		ns
6	Address setup time	t_{as}		0			ns
7	Write pulse width	t_{wp}	ERAMSEL1-0=11	$t_{ckc} \times 1$			ns
			ERAMSEL1-0=10	$t_{ckc} \times 2$			ns
8	Write recovery time	t_{wr}		0			ns
9	Data output delay time	t_{dod}				8	ns
10	Data output hold time	t_{doh}		0			ns

Note) See "● Clock in the 4) AC characteristics" for t_{ckc} (=internal operation clock cycle time).
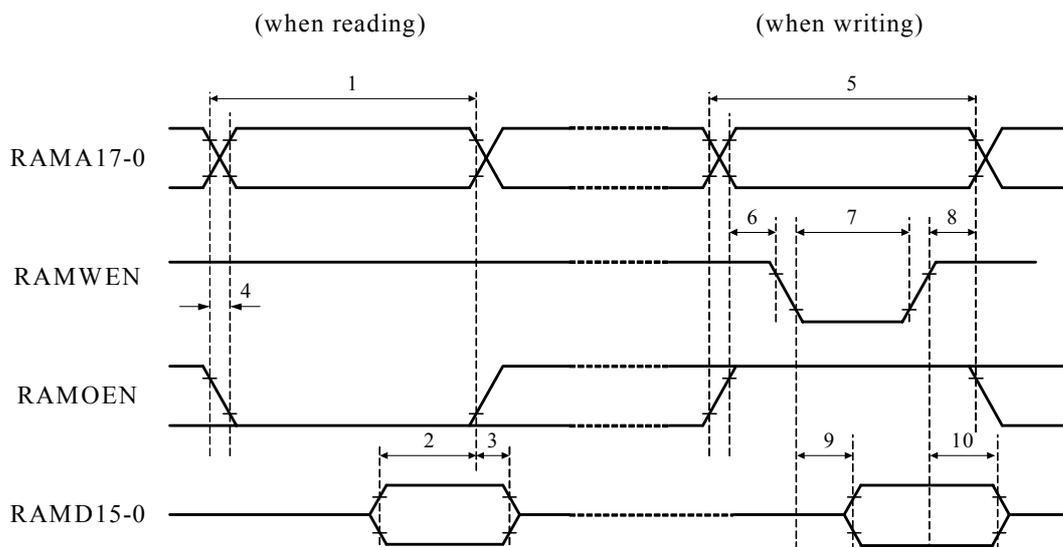
When ERAMSEL 1-0=00 (DRAM mode)   (CL=20 pF)

No.	Items	Symbol	Condition	Min.	Typ.	Max.	Unit
1	Setup time for Row address	tras		5			ns
2	Hold time for Row address	trah		10			ns
3	RASN pulse width	trpw		115			ns
4	RASN pre-charge time	trpt		55			ns
5	Setup time for Column address	tcas		5			ns
6	Hold time for Column address	tcah		40			ns
7	CASN pulse width	tcpw		40			ns
8	CASN pre-charge time	tcpt		10			ns
9	CASN access time	tcat				30	ns
10	Access time from Column address	taat				45	ns
11	Access time from RASN	trat				60	ns
12	Hold time for read data	trdh		0			ns
13	Setup time for write data	twds		5			ns
14	Hold time for write data	twdh		40			ns
15	Setup time for write command	twcs		5			ns
16	Hold time for write command	twch		40			ns
17	CASN high-RASN low delay time	tcrd		40			ns
18	Refresh cycle time	trc	RASREF=1			200	ns

Note) Set the internal operation clock cycle time tckc to 32.55 ns (30.72 MHz) in DRAM mode.

(when reading)
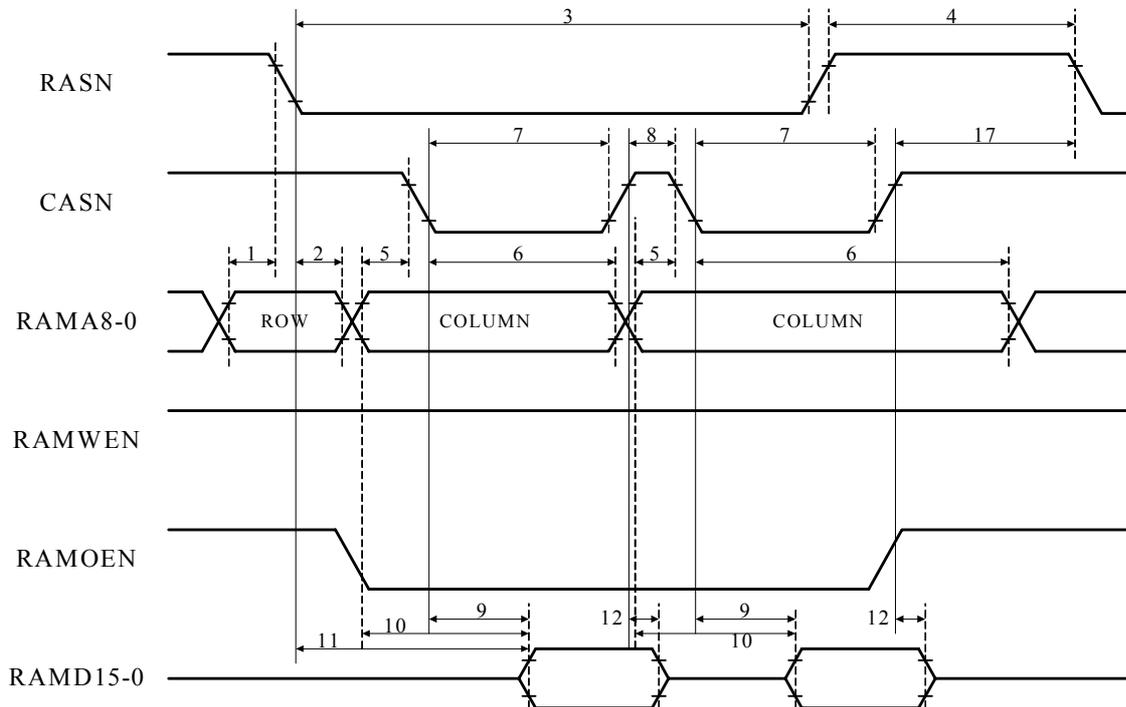
(when writing)
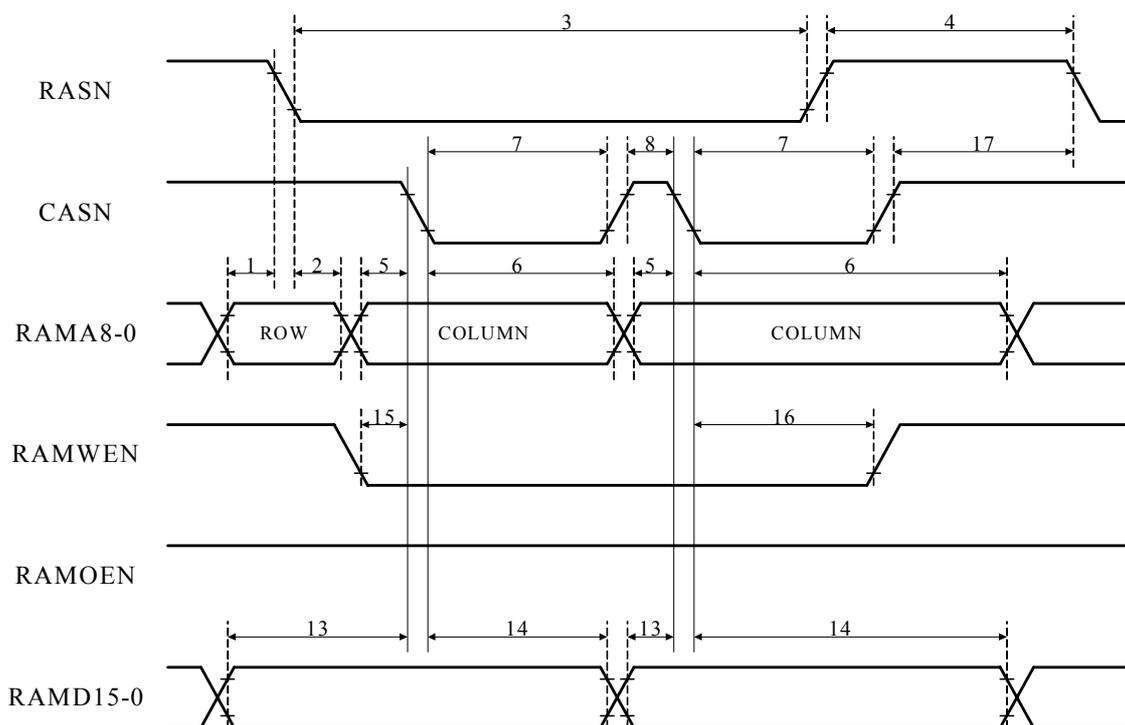
(during /RAS only refresh (RASREF = 1))
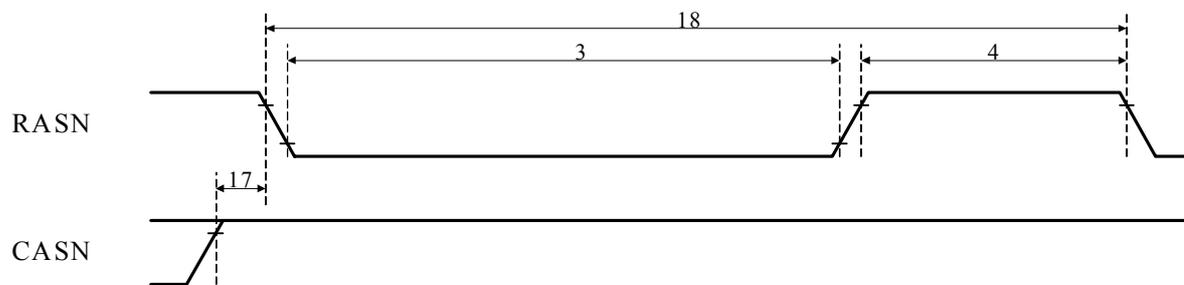
■ Example of Connection Diagrams

1) When using one YSS920B

An example of the basic connection when one YSS920B is used is indicated below:
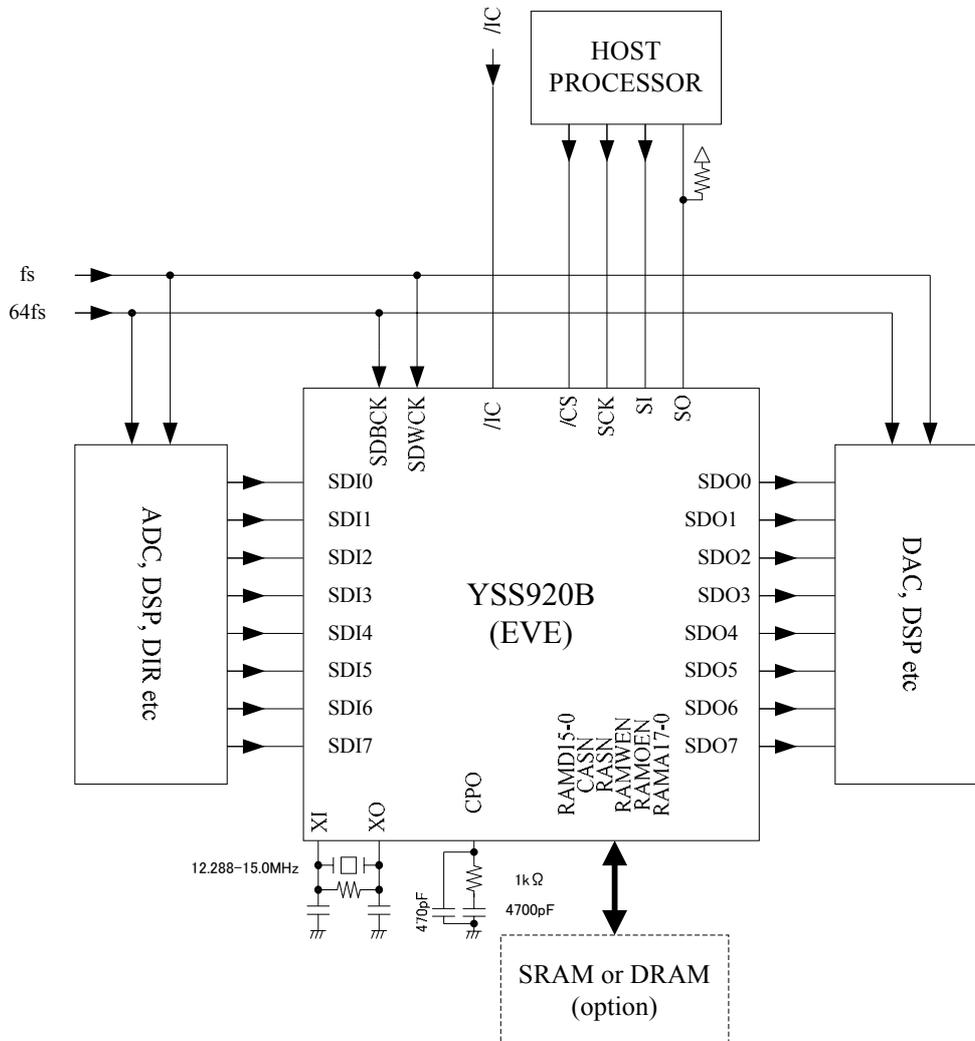
- It is not necessary to set chip address (CA3-0) when using one YSS920B.
- The SO pin may become High-Z. Therefore, pull-up resistors may be necessary on some systems.
- On peripheral devices such as the ADC and DAC that require a bit clock with inversed polarity, use the SDBCKO output from the IOPORT18 pin by setting IOSEL18=1, OPSEL18=1, and BCKOP=1.

YSS920B

2) When using multiple YSS920Bs

An example of the basic connection when multiple YSS920Bs are used is indicated below:
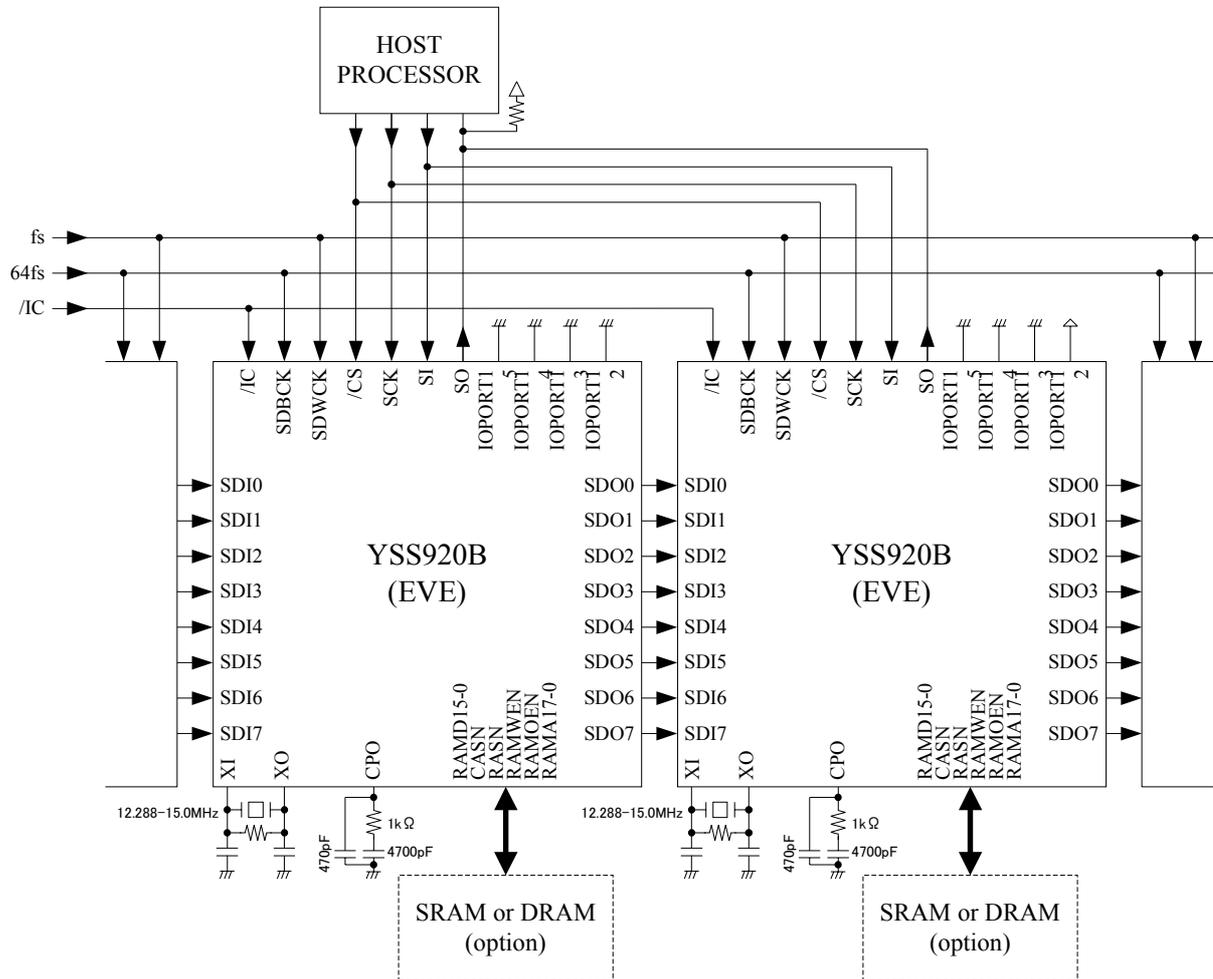
- /CS can be shared by setting chip addresses (CA3-0) to the IOPORT15-12 pins.
  When switching the device to control, rewrite the control register address 0x00 (CA3-0).
  For example, in the case above:
     To control the left device, set the register as CAE=1 and CA3-0=0000,
     To control the right device, set the register as CAE=1 and CA3-0=0001.

- On peripheral devices such as the ADC and DAC that require a bit clock with inversed polarity, use the SDBCKO output from the IOPORT18 pin by setting IOSEL18=1, OPSEL18=1, and BCKOP=1.

- The SO pin may become High-Z. Therefore, pull-up resistors may be necessary on some systems.

■ Package Dimensions

C-PK100SP-2

16.00±0.40
14.00±0.30
75　　　51
76　　　50
14.00±0.30
16.00±0.40
100　　26
1　　　25

0.20±0.10
or 0.18±0.10
P-0.50TYP

0 Min.(STAND OFF)
1.70MAX.
1.40±0.20

(1.0)
0-10°
0.50±0.20
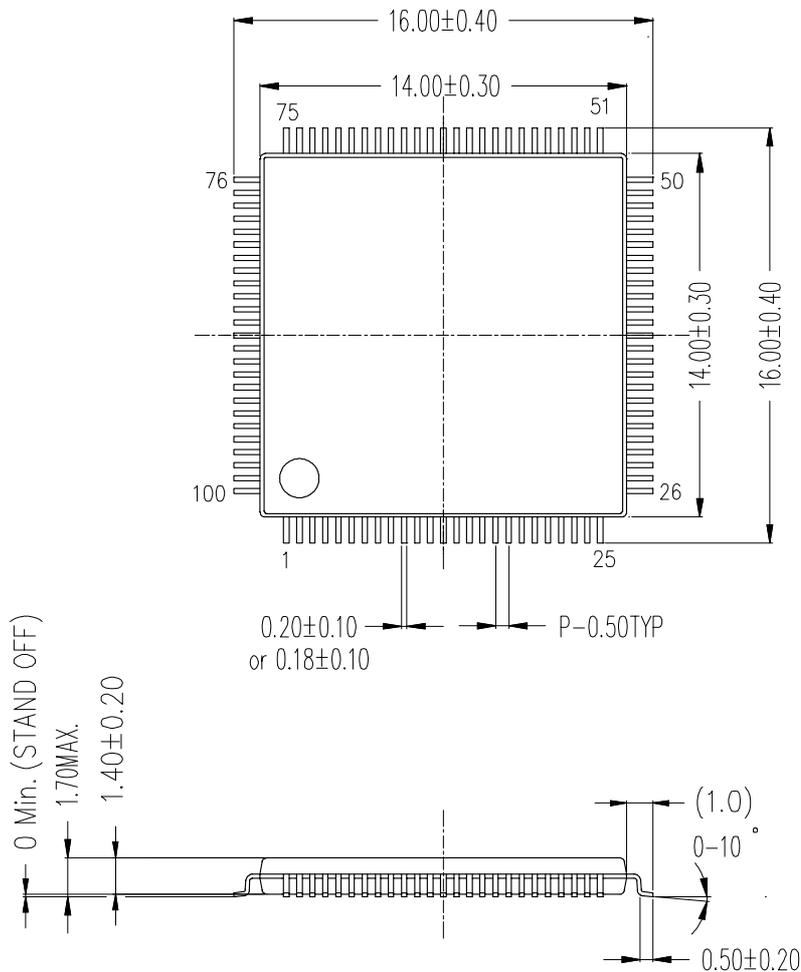
端子厚さ/Lead Thickness：0.125or0.15

モールドコーナー形状は、この図面と若干異なるタイプもあります。
カッコ内の寸法値は参考値です。
モールド外形寸法はバリを含みません。
単位：mm

The shape of the molded corner may slightly differ from the shape in this diagram.
The figure in the parentheses ( ) should be used as a reference.
Plastic body dimensions do not include resin burr.
UNIT: mm

注）　表面実装LSIは、保管条件、及び半田付けについての特別な配慮が必要です。
　　　詳しくはヤマハ代理店までお問い合わせください。

Note:　The storage and soldering of LSIs for surface mounting need special consideration.
　　　　For detailed information, please contact your local Yamaha agent.

IMPORTANT NOTICE

Notice The specifications of this product are subject to improvement changes without prior notice.

AGENT

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