HITACHI

Hitachi Displays,Ltd.

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TECHNICAL DATA

TFTMD48110CBB

CONTENTS

DESCRIPTION

The following specifications are applied to the 19-inch Super-TFT module.

Note : Inverter for back light unit is not built in a module.

Product Name : TFTMD48110CBB

General Specifications

Effective Display Area	:(H)386.4×(V)289.8	(mm)
Number of Pixels	:(H)1600×(V)1200	(pixels)
Pixel Pitch	:(H)0.2415×(V)0.2415	(mm)
Color Pixel Arrangement	:R·G·B Vertical Stripe	
Display Mode	:Transmissive Mode Normally Black Mode	
Top Polarizer Type	:Anti-glare	
Number of Colors	:16,777,216	(colors)
Viewing Angle Range	:Super Wide Version (Horizontal & Vertical : 170° , CR≧10)	
Input Signal	:2-channel LVDS (LVDS: Low Voltage Differential Signaling)	
Back Light	:10 pcs. of CCFL	
External Dimensions	:(H)415×(V)332.2×(t)29.6	(mm)
Weight	:Max.2100	(g)

1. ABSOLUTE MAXIMUM RATINGS

1.1 Environmental Absolute Maximum Ratings

ITEM	Operating		Storage		Unit	Note
	Min.	Max.	Min.	Max.		
Temperature	0	50	-20	60	℃	1)
Humidity	2)		2)		%RH	1)
Vibration	-	4.9(0.5G)	-	14.7 (1.5G)	m/s 2	3)
Shock	-	29.4(3G)	-	294 (30G)	m/s 2	4)
Corrosive Gas	Not Acceptable		Not Acceptable		-	
Illuminance of LCD Surface	-	50,000	-	50,000	lx	

Notes 1) Temperature and Humidity should be applied to the glass surface of a Super-TFT module, not to the system installed with a module.
The temperature at the center of rear surface should be less than 65℃ on the condition of operating.
The brightness of a CCFL tends to drop at low temperature. Besides, the life-time becomes shorter at low temperature.

2) Ta≦ 40 ℃ · · · · · · Relative humidity should be less than 85%RH max. Dew is prohibited.
Ta＞ 40 ℃ · · · · · · Relative humidity should be lower than the moisture of the 85%RH at 40℃.

3) Frequency of the vibration is between 15Hz and 100Hz. (Remove the resonance point)

4) Pulse width of the shock is 10 ms.

1.2 Electrical Absolute Maximum Ratings

(1)Super-TFT Module

Vss = 0 V

ITEM	SYMBOL	Min.	Max.	Unit	Note
Power Supply Voltage	V_{DD}	0	14.0	V	
Input Voltage for logic	V_I	-0.3	3.6	V	1)
Electrostatic Durability	V_{ESD0}	±100		V	2),3)
	V_{ESD1}	±8		kV	2),4)

Notes 1) It is applied to pixel data signal and clock signal.
2) Discharge Coefficient : 200pF-250Ω, Environmental : 25℃-70%RH
3) It is applied to I/F connector pins.
4) It is applied to the surface of a metallic bezel and a LCD panel.

(2) Back-light

ITEM	SYMBOL	Min.	Max.	Unit	Note
Input Current	IL	-	6.5	mArms	1)
Input Voltage	VL	-	1800	Vrms	2)

Notes 1) The specification shall be applied to each CFL. The specification is defined at ground line.
2) The specification shall be applied at connector pins for a CFL at start-up.

2. OPTICAL CHARACTERISTICS

The following optical characteristics are measured under stable conditions. It takes about 30 minutes to reach stable conditions. The measuring point is the center of display area unless otherwise noted. The optical characteristics should be measured in a dark room or equivalent state.

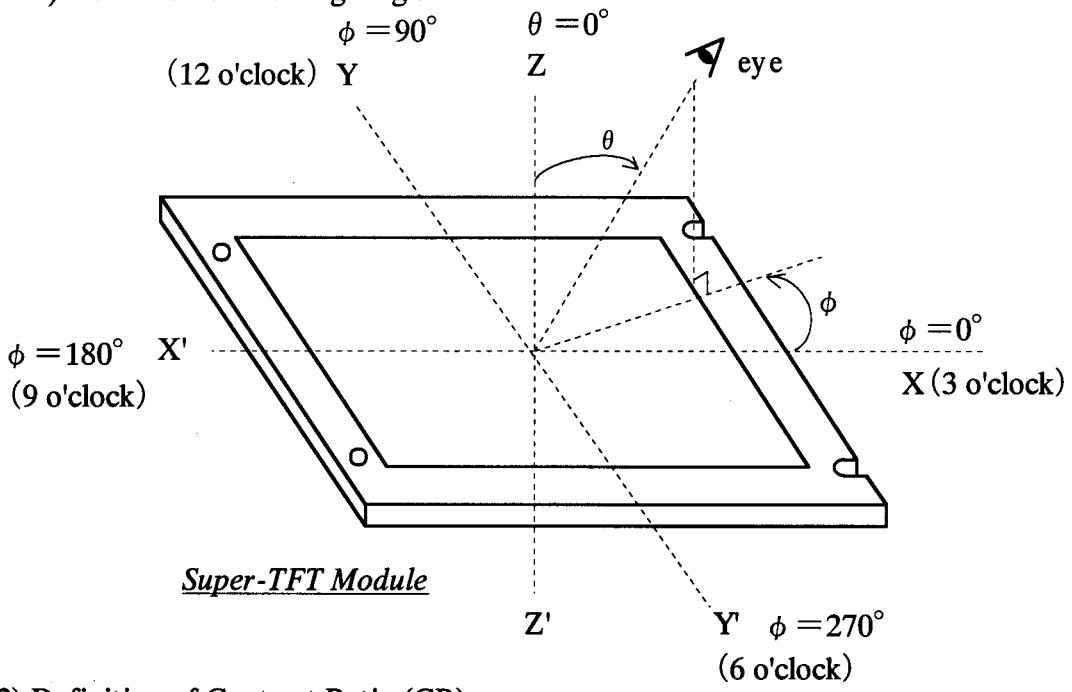
Measuring equipment : Pritchard 1980A, or equivalent

Ta=25℃、VDD=12.0V、f V=60Hz、

IL=5.5mA (average of 10 pieces of CFLs)

ITEM		SYMBOL	CONDITION	Min.	Typ.	Max.	UNIT	NOTE
Contrast Ratio		CR		150	300	-	-	2)
Response Time	Rise	ton		-	20	30	ms	3)
	Fall	toff		-	20	30	ms	3)
Brightness of white		Bwh		160	200	-	cd/m^2	
Brightness uniformity		Buni		-	-	25	%	4)
Color Chromaticity (CIE)	Red	x	θ =0° 1)	0.61	0.64	0.67	-	[Gray scale =255]
		y		0.31	0.34	0.37		
	Green	x		0.26	0.29	0.32		
		y		0.58	0.61	0.64		
	Blue	x		0.11	0.14	0.17		
		y		0.05	0.08	0.11		
	White	x		0.28	0.31	0.34		
		y		0.29	0.32	0.35		
Variation of Color Position (CIE)	Red	Δx	θ =+50° φ =0° 、90° 180° 、270° 1)	-	-	0.04	-	5) [Gray scale =255]
		Δy		-	-	0.04		
	Green	Δx		-	-	0.04		
		Δy		-	-	0.04		
	Blue	Δx		-	-	0.04		
		Δy		-	-	0.04		
	White	Δx		-	-	0.04		
		Δy		-	-	0.04		
Contrast Ratio at 85°		CR85°		10	-	-	-	

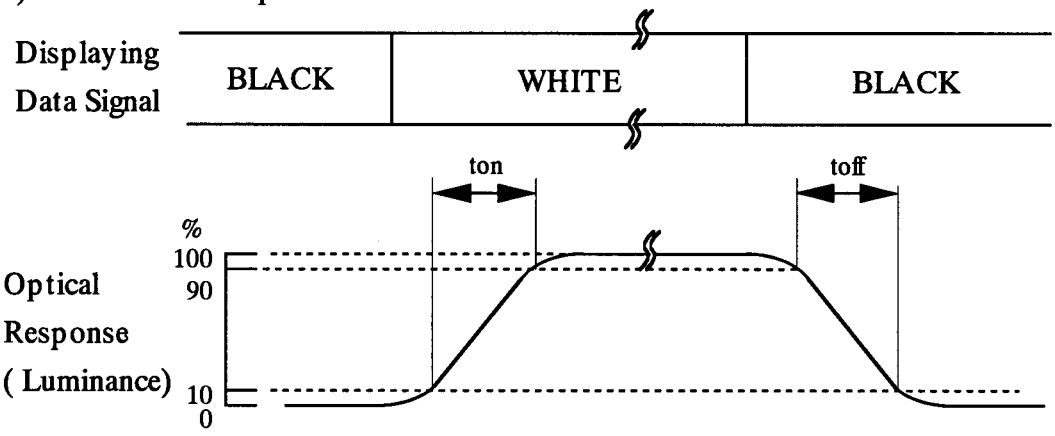
Notes 1) Definition of Viewing Angle



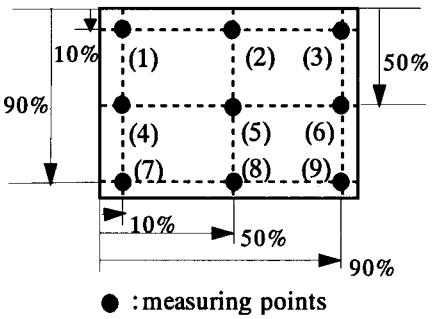
2) Definition of Contrast Ratio (CR)

$$CR = \frac{\text{(Luminance at displaying WHITE)}}{\text{(Luminance at displaying BLACK)}}$$

3) Definition of Response Time



4) Definition of Brightness Uniformity



● : measuring points

Display pattern is white (255 level) and gray scale. The brightness uniformity is defined as the following equation. Brightness at each point is measured, and average, maximum and minimum brightness is calculated.

$$Buni = \frac{|Bmax \text{ or } Bmin - Bave|}{Bave} \times 100$$

where, Bmax = Maximum brightness

Bmin = Minimum brightness

$$Bave = \text{Average brightness} = \frac{\sum_{k=1}^{9} (B(k))}{9}$$

5) Variation of color position on CIE is defined as difference between colors at $\theta = 0°$ and at $\theta = 50°$ & $\phi = 0°$,90° ,180° ,270° .

3. ELECTRICAL CHARACTERISTICS

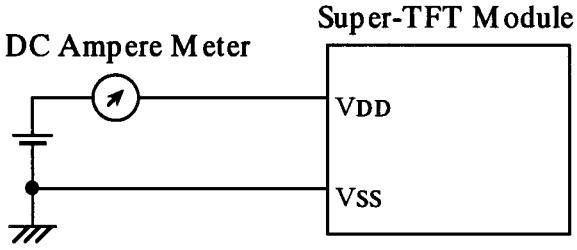
3.1 TFT-LCD Module

Ta=25℃, Vss=0V

ITEM	SYMBOL	Min.	Typ.	Max.	Unit	Note
Power Supply Voltage	V_{DD}	10.8	12	13.2	V	
Power Supply Current	I_{DD}	—	—	1.0	A	1),2)
Vsync Frequency	f_V	—	60	60	Hz	
Hsync Frequency	f_H	—	72	73.5	kHz	
DCLK Frequency	f_{CLK}	—	67.5	68.7	MHz	
Input Signals	V_I	—	—	—	V	3)

Dimensions in parentheses are reference value.

Notes 1) DC current at fv=60Hz, fCLK=67.5MHz and VDD=12.0V



2) Current fuse(1.6A) is built in a module. Current capacity of power supply for VDD should be larger than 4A, so that the fuse can be opened at the trouble of power supply.

3) Characteristics of input signals are shown in LVDS data sheets. (Receiver:THC63LVDF84B)

3.2 Back Light

ITEM	SYMBOL	Min.	Typ.	Max.	Unit	Note
Input Current	I_L	—	5.5	6.0	mArms	1)
Input Voltage	V_L	—	620	—	Vrms	
Frequency	f0	—	54	—	kHz	2)
Kick-Off Voltage	V_S	—	—	1750	V	3)

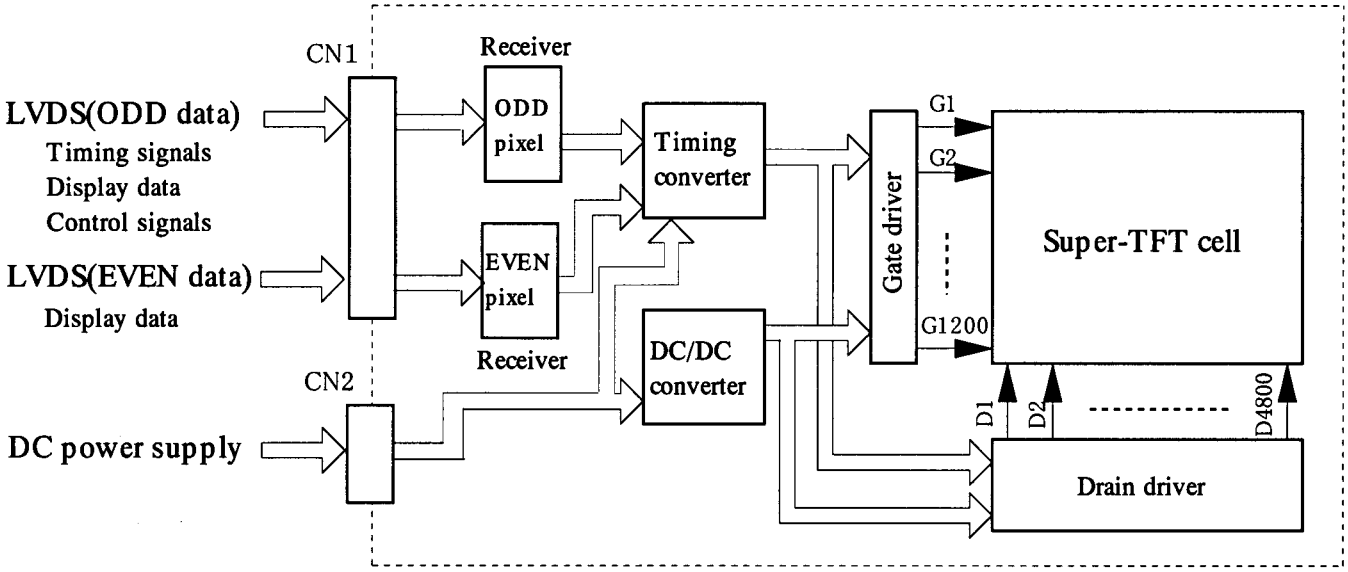
Notes 1) The specification shall be applied to each CFL. The specification is defined at ground line.

2) Frequency of power supply for a CFL may cause the interference with HSYNC frequency and cause beat or flicker on the display. Therefore, lamp frequency shall be as different as possible from HSYNC frequency in order to avoid the interference.

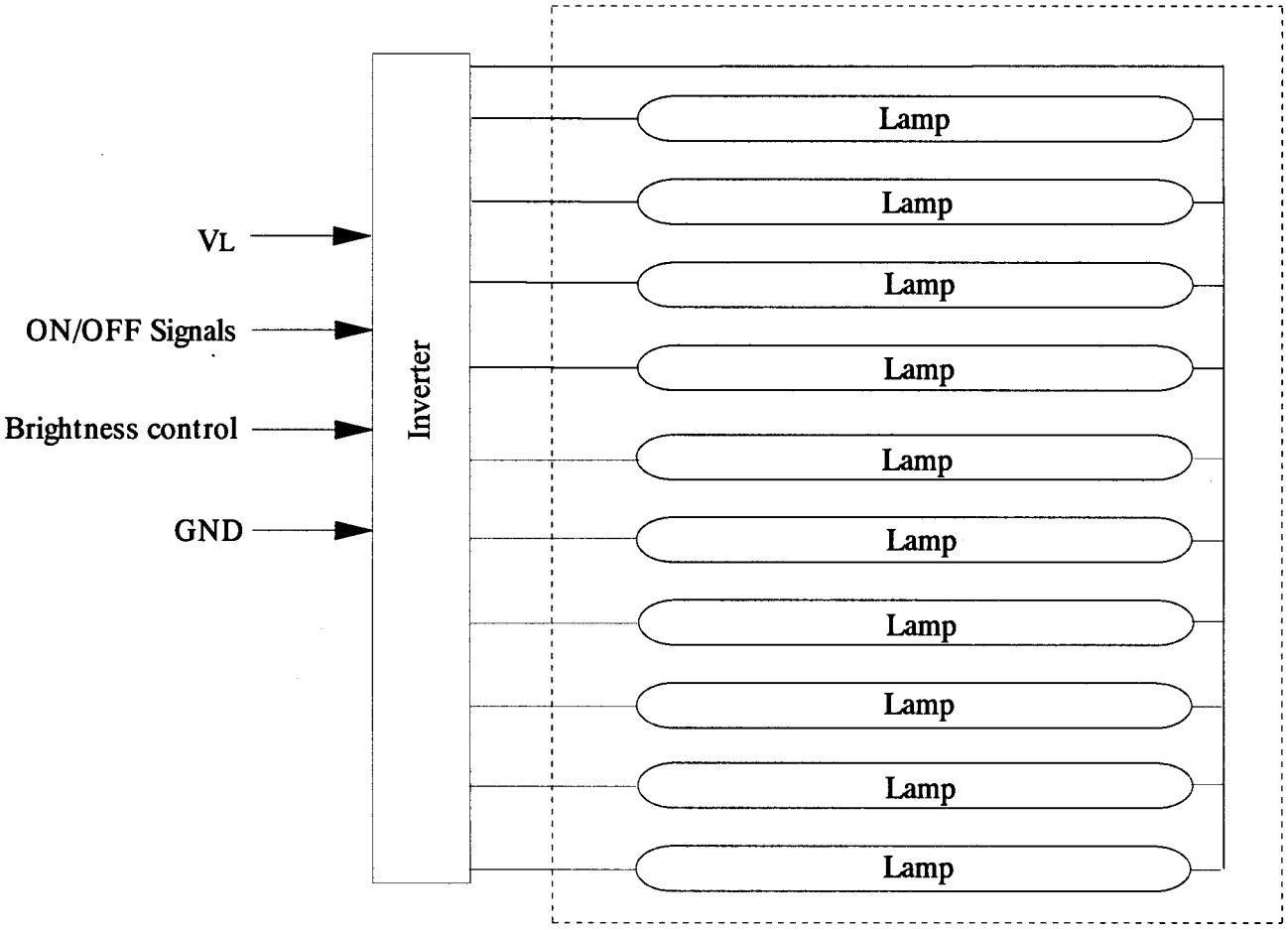
3) Ta = 0 degree

4. BLOCK DIAGRAM

(1) Super-TFT Module



(2) Back light unit



Note 1) The inverter for driving CFLs is not built in a module.

2) Color of wires from CFL to CN3-CN8

CN3-CN7(VL):Pink

CN8 (GND):White

5. INTERFACE PIN ASSIGNMENT

CN1 : JAE FI-X30S-HF

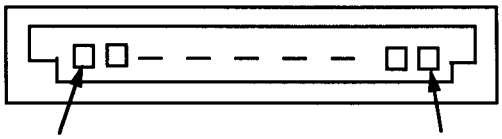
(Matching connector : JAE FI-X30H or FI-X30M)

Pin No.	Symbol	Function	
1	Vss	GND (0V)	1)
2	RAIN0-	ODD pixel data	2)
3	RAIN0+		
4	Vss	GND (0V)	1)
5	RAIN1-	ODD pixel data	2)
6	RAIN1+		
7	Vss	GND (0V)	1)
8	RAIN2-	ODD pixel data	2)
9	RAIN2+		
10	Vss	GND (0V)	1)
11	RACLKIN-	ODD pixel clock	2)
12	RACLKIN+		
13	Vss	GND (0V)	1)
14	RAIN3-	ODD pixel data	2)
15	RAIN3+		
16	Vss	GND (0V)	1)
17	RBIN0-	EVEN pixel data	2)
18	RBIN0+		
19	Vss	GND (0V)	1)
20	RBIN1-	EVEN pixel data	2)
21	RBIN1+		
22	Vss	GND (0V)	1)
23	RBIN2-	EVEN pixel data	2)
24	RBIN2+		
25	Vss	GND (0V)	1)
26	RBCLKIN-	EVEN pixel clock	2)
27	RBCLKIN+		
28	Vss	GND (0V)	1)
29	RBIN3-	EVEN pixel data	2)
30	RBIN3+		

Notes 1) All Vss pins should be grounded.

2) RnINm+ and RnINm- (n=A,B m=0,1,2,3) should be wired by twist-pairs or side-by-side FPC patterns, respectively.

3) Pin assignment is as follows.

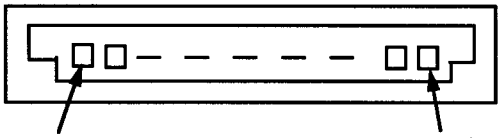


(Figure from top-view)

CN2:JAE FI-S 6P-HF (Matching connector: JAE FI-S 6S)

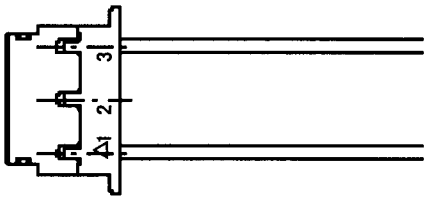
Pin No.	SYMBOL	Function
1	VDD	Power supply (typ.12V) 1)
2	VDD	
3	VDD	
4	VSS	GND(0V) 2)
5	VSS	
6	VSS	

Notes 1) All VDD pins should be connected to +12.0 V(typ.).
2) All Vss pins should be grounded.
3) Pin assignment of CN2 is as follows.



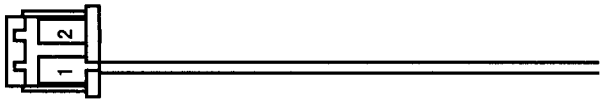
CN3 - 7:JST BHR-03VS-1 (Matching connector: JST SM02(8.0)B-BHS-1-TB)

Pin No.	SYMBOL	Function
1	V_L	Power Supply
2	NC	No connection
3	V_L	Power Supply

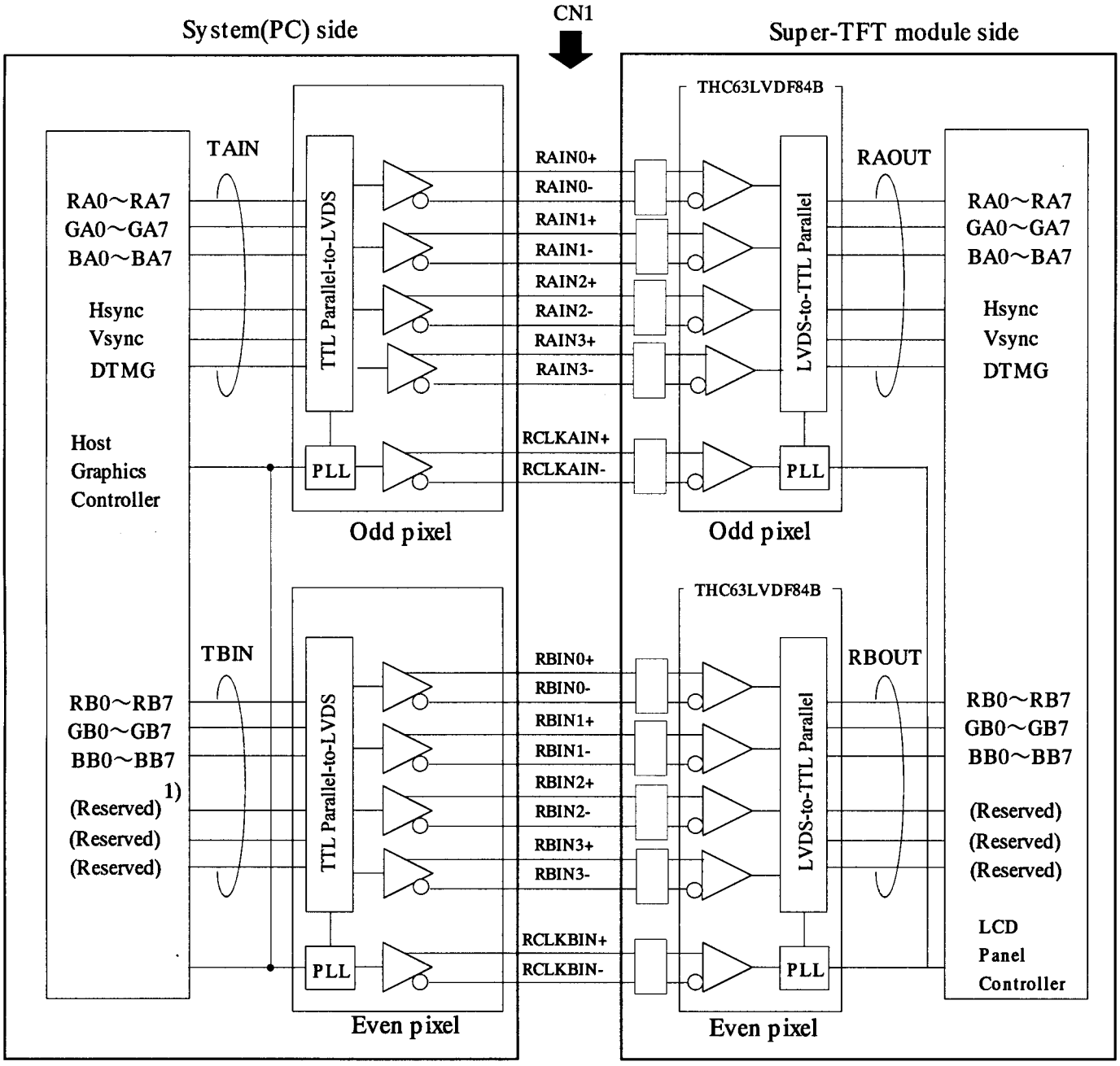


CN8:JST ZHR-2 (Matching connector: JST S2B-ZR-SM3A-TF)

Pin No.	SYMBOL	Function
1	GND	GND
2	NC	No connection



BLOCK DIAGRAM OF INTERFACE



Receiver : THC63LVDF84B by Thine

RA0~7, RB0~7 : R data
GA0~7, GB0~7 : G data
BA0~7, BB0~7 : B data
Hsync : Horizontal synchronization
Vsync: Vertical synchronization
DTMG : Display timing data

Notes 1) RSVD(reserved) pins on a transmitter should be connected with Vss.

2) The system must have a LVDS transmitter to drive a module.

3) The impedance of LVDS cable should be 50 ohms per a signal line or about 100 ohms per a twist-pair line when it is used differentially.

LVDS INTERFACE

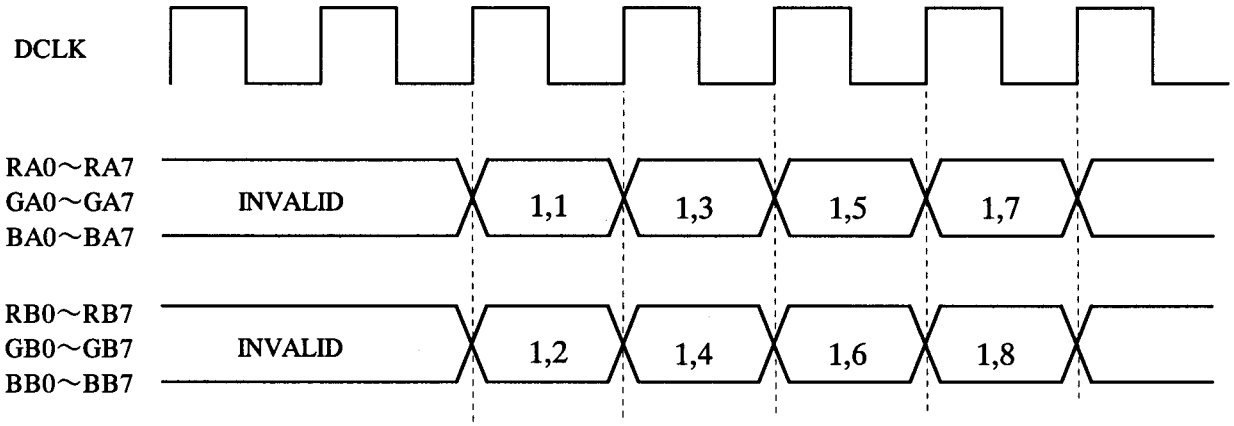
	INPUT SIGNAL	Transmitter		Interface connector		Receiver THC63LVDF84B		TFT control input
		pin	INPUT	System side	Super-TFT module	pin	OUTPUT	
LVDS Odd	RA2	51	TAIN0	TA OUT0+	RA IN0+	27	RAOUT0	RA2
	RA3	52	TAIN1			29	RAOUT1	RA3
	RA4	54	TAIN2			30	RAOUT2	RA4
	RA5	55	TAIN3			32	RAOUT3	RA5
	RA6	56	TAIN4	TA OUT0-	RA IN0-	33	RAOUT4	RA6
	RA7	3	TAIN6			35	RAOUT6	RA7
	GA2	4	TAIN7			37	RAOUT7	GA2
	GA3	6	TAIN8	TA OUT1+	RA IN1+	38	RAOUT8	GA3
	GA4	7	TAIN9			39	RAOUT9	GA4
	GA5	11	TAIN12			43	RAOUT12	GA5
	GA6	12	TAIN13			45	RAOUT13	GA6
	GA7	14	TAIN14	TA OUT1-	RA IN1-	46	RAOUT14	GA7
	BA2	15	TAIN15			47	RAOUT15	BA2
	BA3	19	TAIN18			51	RAOUT18	BA3
	BA4	20	TAIN19	TA OUT2+	RA IN2+	53	RAOUT19	BA4
	BA5	22	TAIN20			54	RAOUT20	BA5
	BA6	23	TAIN21			55	RAOUT21	BA6
	BA7	24	TAIN22			1	RAOUT22	BA7
	HSYNC	27	TAIN24			3	RAOUT24	HSYNC
	VSYNC	28	TAIN25	TA OUT2-	RA IN2-	5	RAOUT25	VSYNC
	DTMG	30	TAIN26			6	RAOUT26	DTMG
	RA0	50	TAIN27	TA OUT3+	RA IN3+	7	RAOUT27	RA0
	RA1	2	TAIN5			34	RAOUT5	RA1
	GA0	8	TAIN10			41	RAOUT10	GA0
	GA1	10	TAIN11			42	RAOUT11	GA1
	BA0	16	TAIN16			49	RAOUT16	BA0
	BA1	18	TAIN17	TA OUT3-	RA IN3-	50	RAOUT17	BA1
	RSVD 1)	25	TAIN23			2	RAOUT23	RSVD
	DCLK	31	TCLKA IN	TCLKA OUT+ TCLKA OUT-	RCLKA IN+ RCLKA IN-	26	RCLKA OUT	DCLK
LVDS Even	RB2	51	TBIN0	TB OUT0+	RB IN0+	27	RBOUT0	RB2
	RB3	52	TBIN1			29	RBOUT1	RB3
	RB4	54	TBIN2			30	RBOUT2	RB4
	RB5	55	TBIN3			32	RBOUT3	RB5
	RB6	56	TBIN4	TB OUT0-	RB IN0-	33	RBOUT4	RB6
	RB7	3	TBIN6			35	RBOUT6	RB7
	GB2	4	TBIN7			37	RBOUT7	GB2
	GB3	6	TBIN8	TB OUT1+	RB IN1+	38	RBOUT8	GB3
	GB4	7	TBIN9			39	RBOUT9	GB4
	GB5	11	TBIN12			43	RBOUT12	GB5
	GB6	12	TBIN13			45	RBOUT13	GB6
	GB7	14	TBIN14	TB OUT1-	RB IN1-	46	RBOUT14	GB7
	BB2	15	TBIN15			47	RBOUT15	BB2
	BB3	19	TBIN18			51	RBOUT18	BB3
	BB4	20	TBIN19	TB OUT2+	RB IN2+	53	RBOUT19	BB4
	BB5	22	TBIN20			54	RBOUT20	BB5
	BB6	23	TBIN21			55	RBOUT21	BB6
	BB7	24	TBIN22			1	RBOUT22	BB7
	RSVD 1)	27	TBIN24			3	RBOUT24	RSVD
	RSVD 1)	28	TBIN25	TB OUT2-	RB IN2-	5	RBOUT25	RSVD
	RSVD 1)	30	TBIN26			6	RBOUT26	RSVD
	RB0	50	TBIN27	TB OUT3+	RB IN3+	7	RBOUT27	RB0
	RB1	2	TBIN5			34	RBOUT5	RB1
	GB0	8	TBIN10			41	RBOUT10	GB0
	GB1	10	TBIN11			42	RBOUT11	GB1
	BB0	16	TBIN16			49	RBOUT16	BB0
	BB1	18	TBIN17	TB OUT3-	RB IN3-	50	RBOUT17	BB1
	RSVD 1)	25	TBIN23			2	RBOUT23	RSVD
	DCLK	31	TCLKB IN	TCLKB OUT+ TCLKB OUT-	RCLKB IN+ RCLKB IN-	26	RCLKB OUT	DCLK

CORRESPONDENCE BETWEEN INPUT DATA AND DISPLAY IMAGE

RA	(1, 1) GA	BA	RB	(1, 2) GB	BB

Odd pixel : RA0～RA7 : R data
GA0～GA7 : G data
BA0～BA7 : B data
Even pixel : RB0～RB7 : R data
GA0～GA7 : G data
BB0～BB7 : B data

1,1	1,2	1,3	----------	1,1600
2,1	2,2	2,3	----------	2,1600
3,1	3,2	3,3	----------	3,1600
⋮	⋮	⋮		⋮
1200,1	1200,2	1200,3	----------	1200,1600



RELATIONSHIP BETWEEN DISPLAY COLORS AND INPUT SIGNALS

Color	Input data	R data								G data								B data							
		RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0	GA7	GA6	GA5	GA4	GA3	GA2	GA1	GA0	BA7	BA6	BA5	BA4	BA3	BA2	BA1	BA0
		RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	GB7	GB6	GB5	GB4	GB3	GB2	GB1	GB0	BB7	BB6	BB5	BB4	BB3	BB2	BB1	BB0
		MSB							LSB	MSB							LSB	MSB							LSB
BASIC COLOR	BLACK	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED(255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	GREEN(255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	BLUE(255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	CYAN	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	MAGENTA	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	YELLOW	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	WHITE	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
RED	BLACK	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED(1)	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED(2)	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	RED(254)	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	RED(255)	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
GREEN	BLACK	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	GREEN(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
	GREEN(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	GREEN(254)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0
	GREEN(255)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
BLUE	BLACK	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	BLUE(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	BLUE(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
	BLUE(254)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0
	BLUE(255)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1

Notes 1) Definition of gray scale : Color (n)

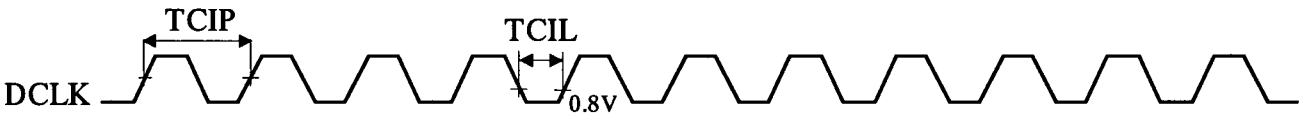
n indicates gray scale level. Higher n means brighter level.

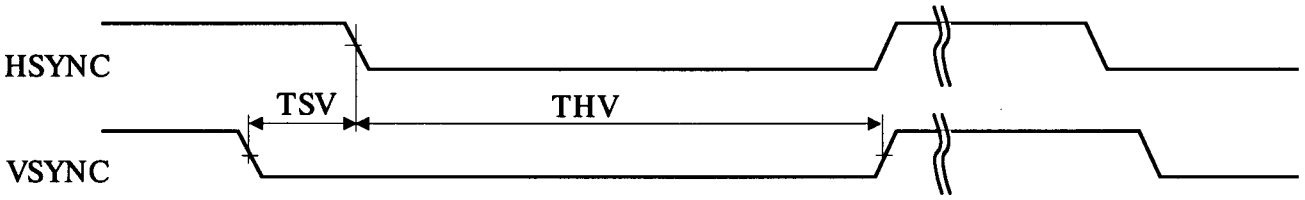
2) Data signals : 1:High, 0:Low

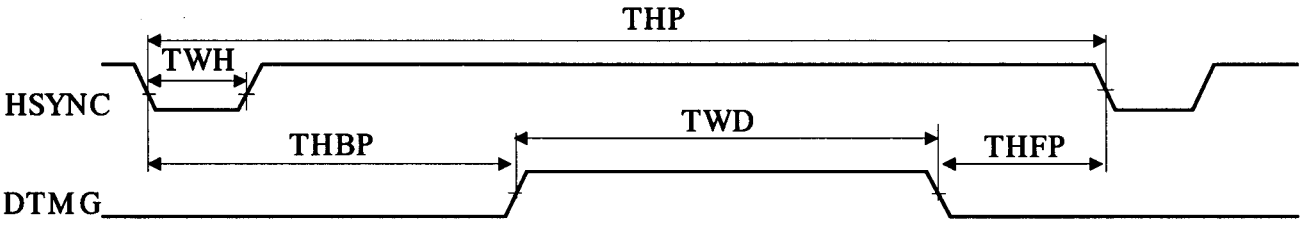
6. TIMING DIAGRAMS OF INTERFACE TIMING

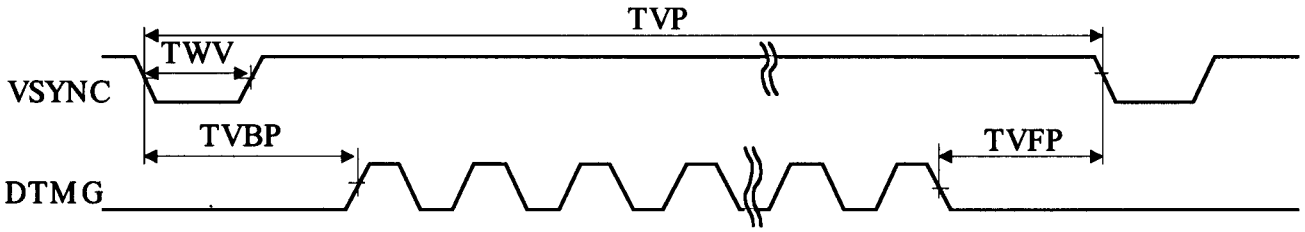
6.1 Timing chart

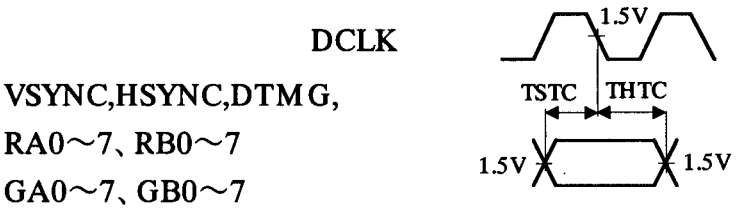
The following timing chart is defined at input of a LVDS transmitter.











VSYNC,HSYNC,DTMG,
RA0～7、RB0～7
GA0～7、GB0～7
BA0～7、BB0～7

Notes 1) Reference level of timing signals is 1.5 V unless it is stated on the chart. However, high level voltage (V_{IH}) and low level voltage (V_{IL}) are defined as follows:

$V_{IH} \geqq 2.0V$ $V_{IL} \leqq 0.8V$

The above definitions come from specifications of THC63LVDM83A(Thine).

2) The timing of DCLK to other signals comes from specifications of THC63LVDM83A. It is recommended to check specifications of the LVDS.

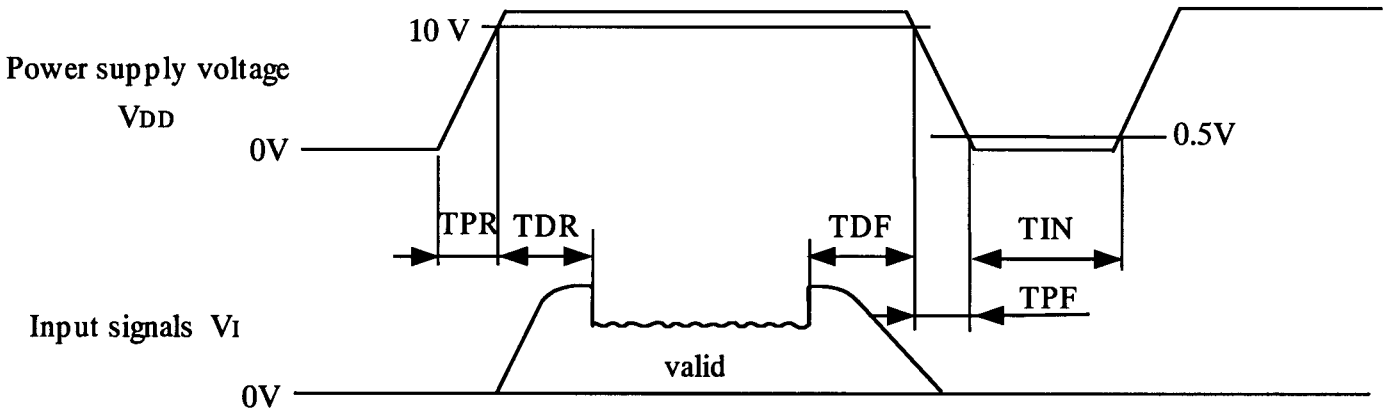
3) HSYNC and VSYNC is a timing in negative polarity.

4) Hsync should be continued during blanking period.

6.2 INTERFACE TIMING SPECIFICATIONS

ITEM		SYMBOL	Min.	Typ.	Max.	Unit	Notes
DCLK	Period	TCIP	-	14.8	-	ns	
	Duty	TCIL	-	0.57	-	TCIP	
HSYNC	Period	THP	-	936	-	TCIP	
	Width-active	TWH	-	16	-	TCIP	
VSYNC	Set up time	TSV	-	0	-	TCIP	to HSYNC
	Hold time	THV	-	1	-	TCIP	to HSYNC
	Period	TVP	-	1203	-	THP	
	Width-active	TWV	-	1	-	THP	
DTMG	Horizontal back porch	THBP	-	136	-	TCIP	
	Horizontal front porch	THFP	-	0	-	TCIP	
	Vertical back porch	TVBP	-	2	-	THP	
	Vertical front porch	TVFP	-	1	-	THP	
	Width-active	TWD	-	800	-	TCIP	
COMMON	Set up time	TSTC	2.5	-	-	ns	
	Hold time	THTC	4.0	-	-	ns	

6.3 TIMING BETWEEN INTERFACE SIGNALS AND POWER SUPPLY



Timing of power supply voltage and input signals should be used under the following specifications.

$0ms \leqq TPR \leqq 30ms$

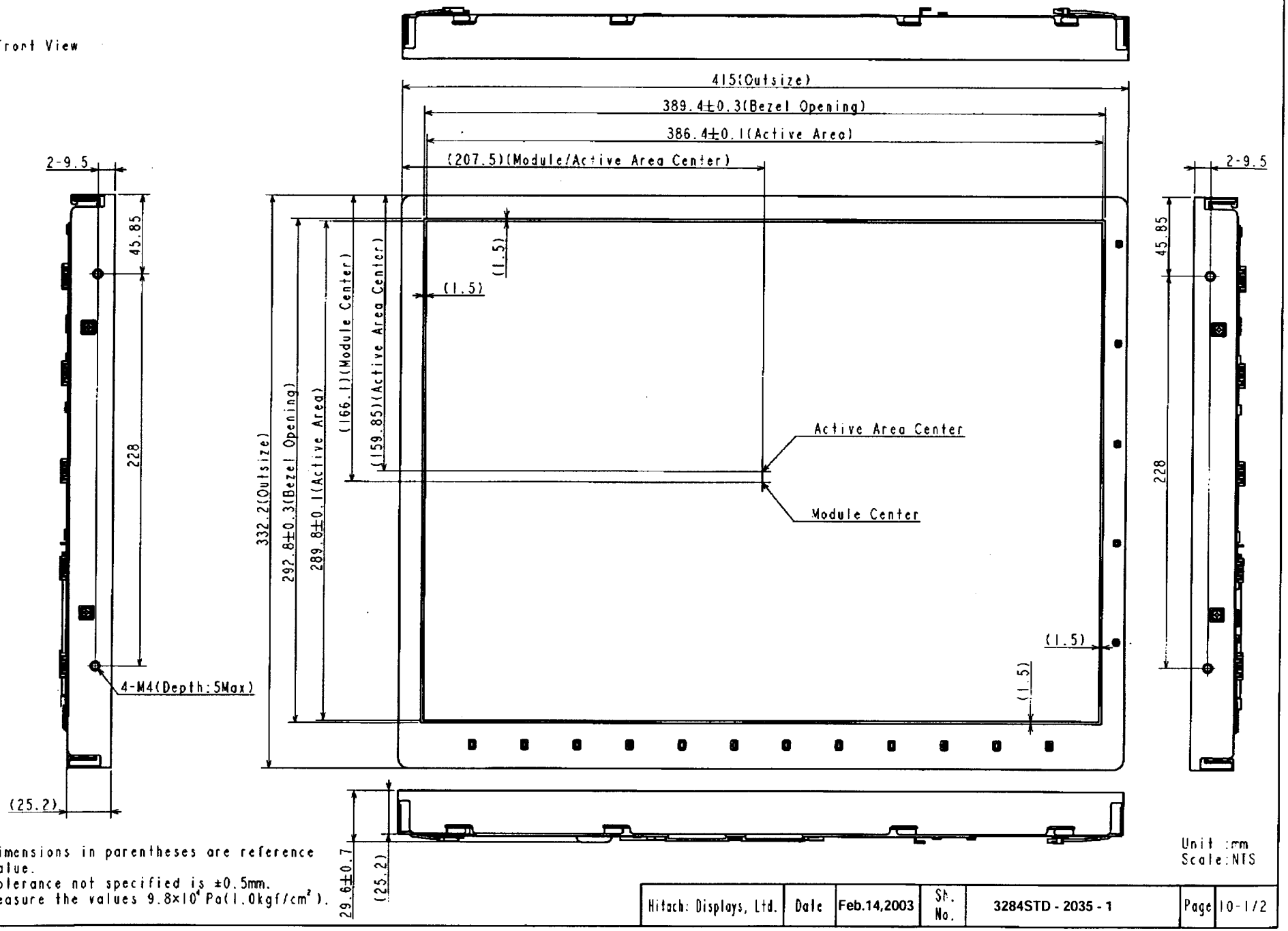
$0ms \leqq TDR \leqq 500ms$

$0ms \leqq TDF \leqq 500ms$

$TIN \geqq 500ms$

$TPF \leqq 500ms$

(1)Front View



Note 1)Dimensions in parentheses are reference value.
2)Tolerance not specified is ±0.5mm.
3)Measure the values 9.8×10^{4} Pa($1.0kgf/cm^{2}$).

Unit :mm
Scale:NTS

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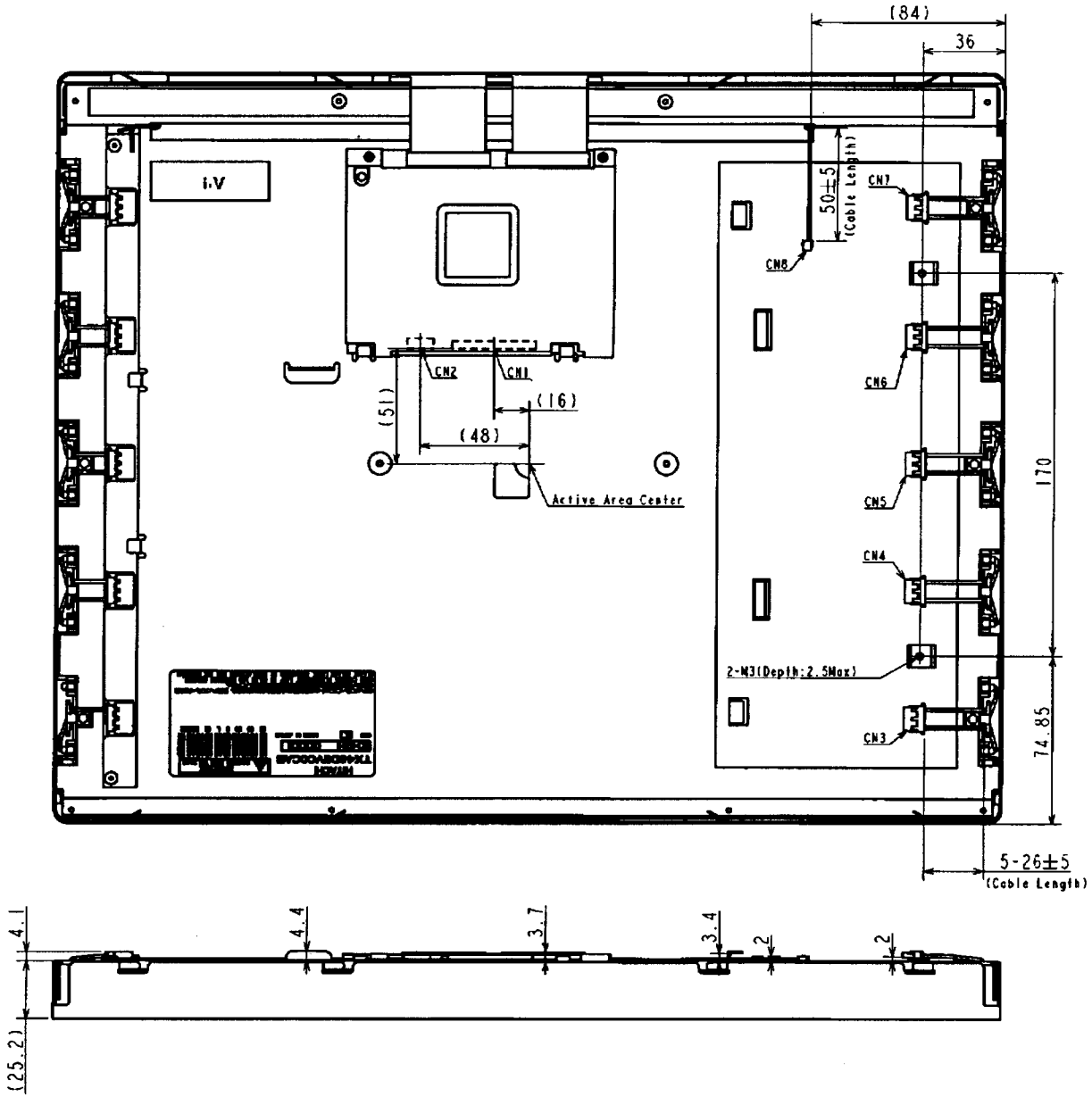
(2)Rear View



Unit :mm
Scale:NTS

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