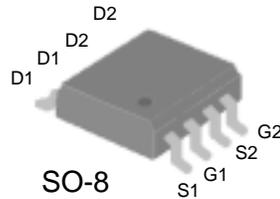


## DUAL N-CANNEL ENHANCEMENT-MODE POWER MOSFETS

- Simple drive requirement
- Lower gate charge
- Fast switching characteristics

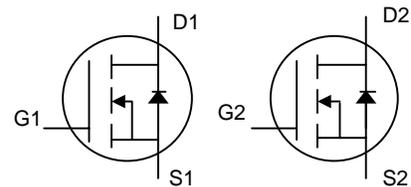


$BV_{DSS}$	40V
$R_{DS(ON)}$	25m $\Omega$
$I_D$	7A

### Description

Advanced Power MOSFETs from Silicon Standard provide the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost-effectiveness.

The SSM9962M is in the SO-8 package, which is widely preferred for commercial and industrial surface mount applications, and is well suited for low voltage applications such as DC/DC converters.



**Pb** This device is available with Pb-free lead finish (second-level interconnect) as SSM9962GM.

### Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
$V_{DS}$	Drain-Source Voltage	40	V
$V_{GS}$	Gate-Source Voltage	$\pm 20$	V
$I_D @ T_A=25^\circ\text{C}$	Continuous Drain Current <sup>3</sup>	7	A
$I_D @ T_A=100^\circ\text{C}$	Continuous Drain Current <sup>3</sup>	5.5	A
$I_{DM}$	Pulsed Drain Current <sup>1</sup>	20	A
$P_D @ T_A=25^\circ\text{C}$	Total Power Dissipation	2	W
	Linear Derating Factor	0.016	W/ $^\circ\text{C}$
$T_{STG}$	Storage Temperature Range	-55 to 150	$^\circ\text{C}$
$T_J$	Operating Junction Temperature Range	-55 to 150	$^\circ\text{C}$

### Thermal Data

Symbol	Parameter	Value	Unit
$R_{thj-a}$	Thermal Resistance Junction-ambient <sup>3</sup>	Max. 62.5	$^\circ\text{C}/\text{W}$

**Electrical Characteristics @  $T_j=25^\circ\text{C}$  (unless otherwise specified)**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	40	-	-	V
$\Delta BV_{DSS}/\Delta T_j$	Breakdown Voltage Temperature Coefficient	Reference to $25^\circ\text{C}$ , $I_D=1\text{mA}$	-	0.1	-	$V/^\circ\text{C}$
$R_{DS(ON)}$	Static Drain-Source On-Resistance <sup>2</sup>	$V_{GS}=10V, I_D=7A$	-	-	25	$\text{m}\Omega$
		$V_{GS}=4.5V, I_D=5A$	-	-	40	$\text{m}\Omega$
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	1	-	3	V
$g_{fs}$	Forward Transconductance	$V_{DS}=10V, I_D=7A$	-	11	-	S
$I_{DSS}$	Drain-Source Leakage Current ( $T_j=25^\circ\text{C}$ )	$V_{DS}=40V, V_{GS}=0V$	-	-	1	$\mu A$
	Drain-Source Leakage Current ( $T_j=70^\circ\text{C}$ )	$V_{DS}=32V, V_{GS}=0V$	-	-	25	$\mu A$
$I_{GSS}$	Gate-Source Leakage	$V_{GS}=\pm 20V$	-	-	$\pm 100$	nA
$Q_g$	Total Gate Charge <sup>2</sup>	$I_D=7A$	-	25.8	-	nC
$Q_{gs}$	Gate-Source Charge	$V_{DS}=32V$	-	4.4	-	nC
$Q_{gd}$	Gate-Drain ("Miller") Charge	$V_{GS}=4.5V$	-	9.1	-	nC
$t_{d(on)}$	Turn-on Delay Time <sup>2</sup>	$V_{DS}=20V$	-	10.6	-	ns
$t_r$	Rise Time	$I_D=1A$	-	6.8	-	ns
$t_{d(off)}$	Turn-off Delay Time	$R_G=5.7\Omega, V_{GS}=10V$	-	26.3	-	ns
$t_f$	Fall Time	$R_D=20\Omega$	-	12	-	ns
$C_{iss}$	Input Capacitance	$V_{GS}=0V$	-	1165	-	pF
$C_{oss}$	Output Capacitance	$V_{DS}=25V$	-	205	-	pF
$C_{rss}$	Reverse Transfer Capacitance	$f=1.0\text{MHz}$	-	142	-	pF

**Source-Drain Diode**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
$V_{SD}$	Forward On Voltage <sup>2</sup>	$I_S=1.7A, V_{GS}=0V$	-	-	1.2	V
$t_{rr}$	Reverse Recovery Time	$I_S=1.7A, V_{GS}=0V,$	-	21.2	-	ns
$Q_{rr}$	Reverse Recovery Charge	$di/dt=100A/\mu s$	-	16	-	nC

**Notes:**

1. Pulse width limited by max. junction temperature.
2. Pulse width  $\leq 300\mu s$ , duty cycle  $\leq 2\%$ .
3. Surface mounted on 1 in<sup>2</sup> copper pad of FR4 board; 135°C/W when mounted on min. copper pad.

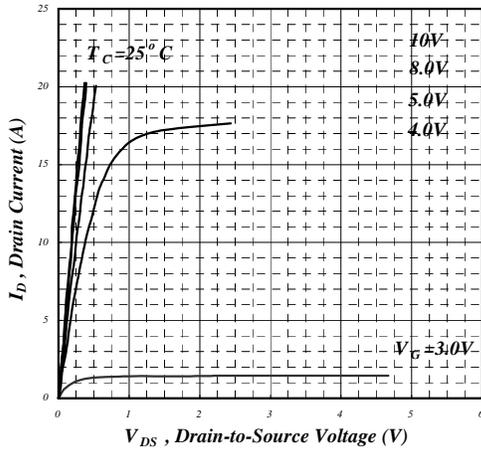


Fig 1. Typical Output Characteristics

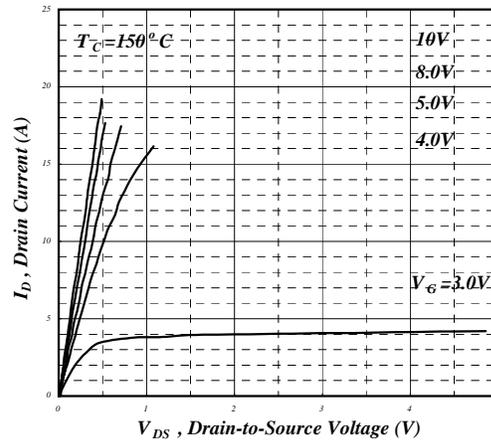


Fig 2. Typical Output Characteristics

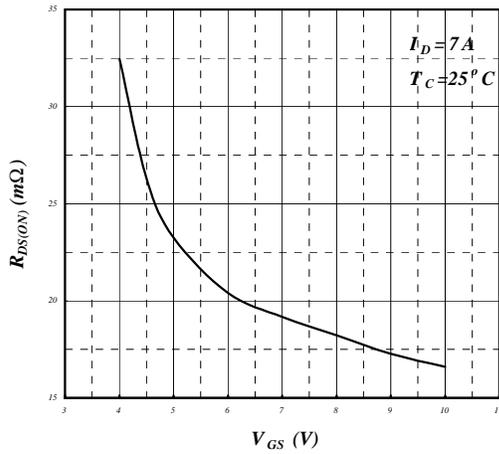


Fig 3. On-Resistance vs. Gate Voltage

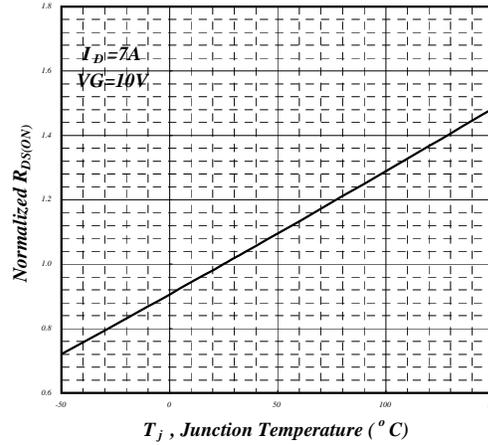


Fig 4. Normalized On-Resistance vs. Junction Temperature

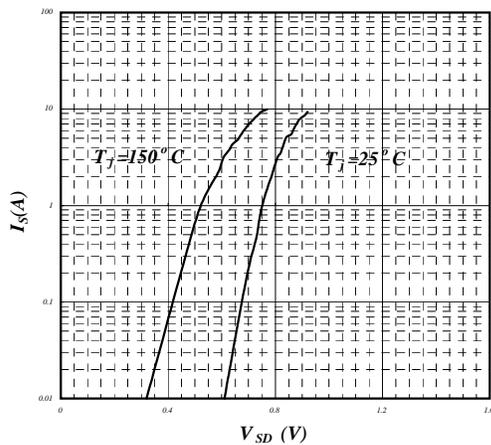


Fig 5. Forward Characteristic of Reverse Diode

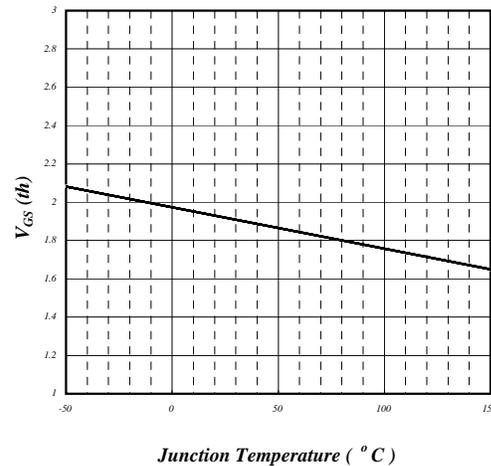


Fig 6. Gate Threshold Voltage vs. Junction Temperature

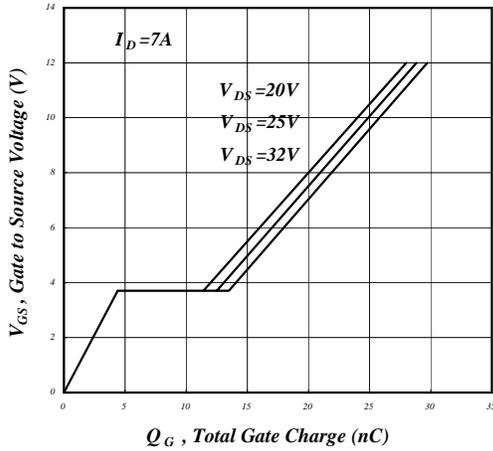


Fig 7. Gate Charge Characteristics

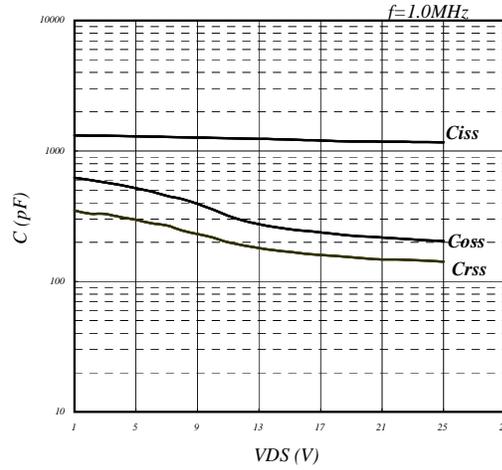


Fig 8. Typical Capacitance Characteristics

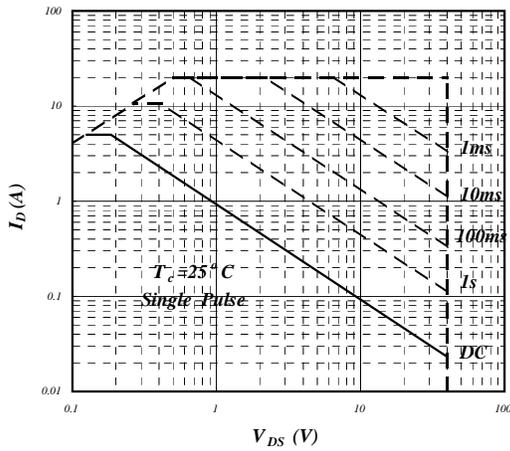


Fig 9. Maximum Safe Operating Area

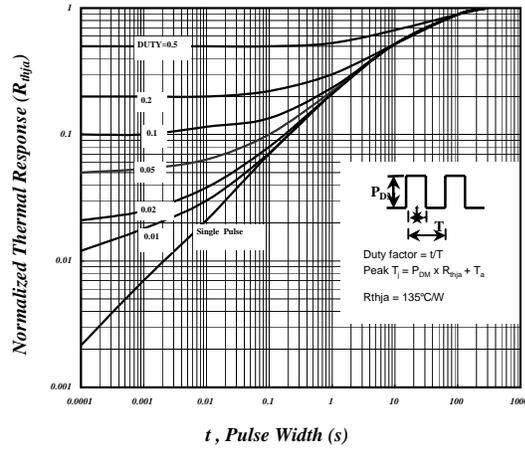


Fig 10. Effective Transient Thermal Impedance

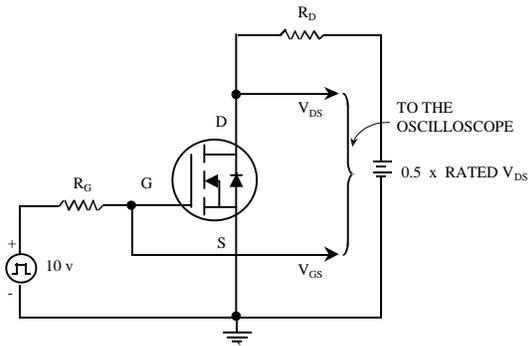


Fig 11. Switching Time Circuit

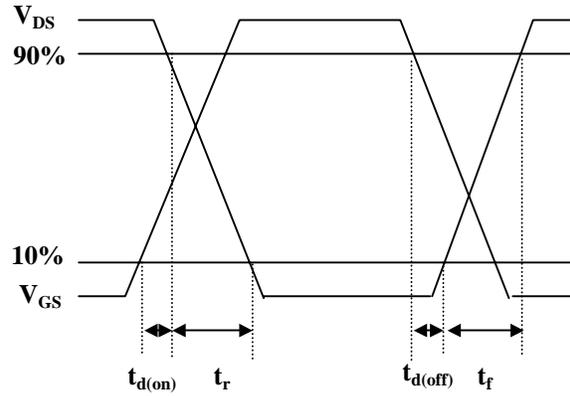


Fig 12. Switching Time Waveform

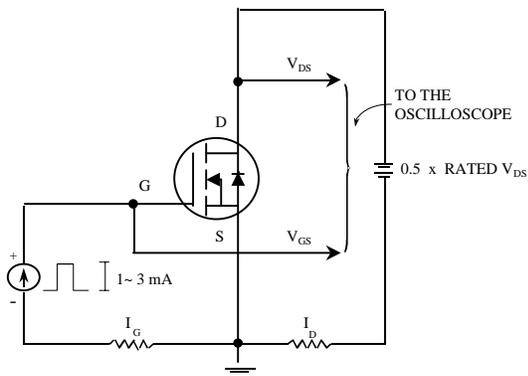


Fig 13. Gate Charge Circuit

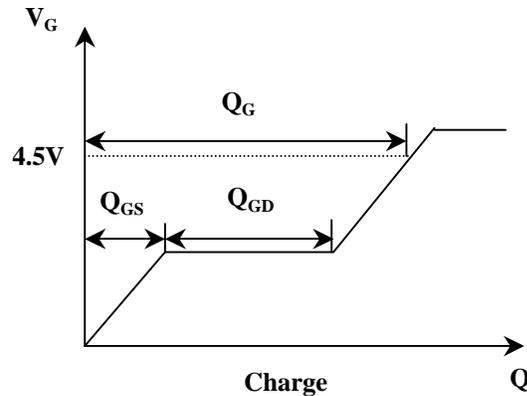


Fig 14. Gate Charge Waveform

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