TC1798

32-Bit Single-Chip Microcontroller

User´s Manual

V1.1 2011-03

Microcontrollers

Edition 2011-03

Published by
Infineon Technologies AG
81726 Munich, Germany

Legal Disclaimer

The information given in this document shall in no event be regarded as a guarantee of conditions or characteristics. With respect to any examples or hints given herein, any typical values stated herein and/or any information regarding the application of the device, Infineon Technologies hereby disclaims any and all warranties and liabilities of any kind, including without limitation, warranties of non-infringement of intellectual property rights of any third party.

Information

For further information on technology, delivery terms and conditions and prices, please contact the nearest Infineon Technologies Office (**www.infineon.com**).

Warnings

Due to technical requirements, components may contain dangerous substances. For information on the types in question, please contact the nearest Infineon Technologies Office.

Infineon Technologies components may be used in life-support devices or systems only with the express written approval of Infineon Technologies, if a failure of such components can reasonably be expected to cause the failure of that life-support device or system or to affect the safety or effectiveness of that device or system. Life support devices or systems are intended to be implanted in the human body or to support and/or maintain and sustain and/or protect human life. If they fail, it is reasonable to assume that the health of the user or other persons may be endangered.

TC1798

32-Bit Single-Chip Microcontroller

User´s Manual

V1.1 2011-03

Microcontrollers

TC1798 User´s Manual

Revision History: V1.1, 2011-03

Previous Version: V1.0	
Chapter	Subjects (major changes since last revision)
Changes from TC1798 UMV1.0 to TC1798 UM V1.1	
1	Introduction: • No functional changes
2	CPU: • No functional changes
3	SCU: • No functional changes
4	On-Chip System Buses and Bus Bridges: • XBARDBCON.Master description and increased bitfield to 6 bit
5	PMU: • Chapter ´Robust EEPROM Emulation´: Highlighted in the description of the robust EEPROM emulation that program VER flags should be ignored • Chapter ´Advice for EEPROM Emulation´ and ´Robust EEPROM Emulation´: Some minor fixes to the description of the EEPROM emulation. Replaced all “ignore SBE” by ignore correctable error and the same for DBE. Noted in the EEPROM advice that the “Other page” should be compared also. Noted how a marker should be programmed • Chapter ´Flash Read Access´: Corrected that data reads by Tricore from cached PFlash are not performed by BTR2 but BTR4
6	LMU: • No functional changes
7	Data Access Overlay: • No functional changes
8	Firmware: • No functional changes
9	Memory Maps: • No functional changes

TC1798 User´s Manual

Revision History: V1.1, 2011-03

10	General Purpose I/O Ports and Peripheral I/O Lines: • Added description of strong sharp minus and strong medium minus for Class A2 pads. • Added description for driver strength selection for Class B pads
11	PCP: • No functional module changes
12	DMA: • No functional module changes
13	SDMA: • No functional module changes
14	FCE: • Changed reset value of the FCE_CLC register
15	External Bus Unit: • No functional module changes
16	Interrupt System: • Changed text that target is to support CONECYC=´1´ up to the max fpi frequency • Corrected number of GPT12 interrupts from 4 to 6
17	System Timer: • No functional module changes
18	BMU • No functional module changes
19	OCDS: • No functional module changes
20	ASC: • No functional module changes
21	SSC: • No functional module changes
22	SSCG: • No functional module changes
23	MSC: • No functional module changes
24	MultiCAN: • No functional module changes

TC1798 User´s Manual

Revision History: V1.1, 2011-03

25	SENT: • No functional module changes
26	E-Ray: • No functional module changes
27	MLI: • Corrected description of register TCMDR • Maximum baud rate frequencies where replaced by a baud rate formula
28	GPTAv5: • No functional module changes
29	CCU6: • No functional module changes
30	GPT12: • No functional module changes
31	ADC: • No functional module changes
32	FADC: • No functional module changes

Trademarks

TriCore®, Infineon®, Infineon Technologies® and GPTA® are trademarks of Infineon Technologies AG.

We Listen to Your Comments

Is there any information in this document that you feel is wrong, unclear or missing? Your feedback will help us to continuously improve the quality of this document. Please send your proposal (including a reference to this document) to:

mcdocu.comments@infineon.com

Table of Contents

1 Introduction 1-1
1.1 About this Document 1-1
1.1.1 Related Documentations 1-1
1.1.2 Text Conventions 1-1
1.1.3 Reserved, Undefined, and Unimplemented Terminology 1-3
1.1.4 Register Access Modes 1-3
1.1.5 Abbreviations and Acronyms 1-4
1.2 System Architecture of the TC1798 1-8
1.2.1 TC1798 Block Diagram 1-9
1.2.2 CPU Cores of the TC1798 1-10
1.2.2.1 High-performance 32-bit CPU 1-10
1.2.2.2 High-performance 32-bit Peripheral Control Processor 1-11
1.3 On-Chip System Units 1-12
1.3.1 Flexible Interrupt System 1-12
1.3.1.1 Feature List 1-12
1.3.2 Direct Memory Access Controller (DMA) 1-12
1.3.2.1 Feature List 1-12
1.3.3 Safe Direct Memory Access Controller 1-13
1.3.3.1 Feature List 1-13
1.3.4 Flexible CRC Engine (FCE) 1-14
1.3.4.1 Feature List 1-14
1.3.5 System Timer (STM) 1-15
1.3.5.1 Feature List 1-15
1.3.6 System Control Unit (SCU) 1-17
1.3.6.1 Clock Generation Unit (CGU) 1-17
1.3.6.2 Features of the Watchdog Timer (WDT) 1-17
1.3.6.3 Reset Operation 1-18
1.3.6.4 External Interface (ESR, ERU) 1-18
1.3.6.5 Die Temperature Measurement (DTS) 1-18
1.3.7 General Purpose I/O Ports and Peripheral I/O Lines (Ports) 1-19
1.3.7.1 Feature List 1-19
1.3.8 Program Memory Unit (PMU) 1-20
1.3.8.1 Feature List 1-20
1.3.9 Secure Hardware Extension (SHE) 1-22
1.3.10 Local Memory Unit (LMU) 1-22
1.3.10.1 Feature List 1-22
1.3.11 Data Access Overlay (OVC) 1-23
1.3.11.1 Feature List 1-23
1.4 On-Chip Peripheral Units of the TC1798 1-24
1.4.1 Asynchronous/Synchronous Serial Interfaces (ASC) 1-24
1.4.1.1 Feature List 1-25

1.4.2 High-Speed Synchronous Serial Interfaces (SSC) 1-27
1.4.2.1 Feature List 1-27
1.4.3 Synchronous Serial Interface Guardian (SSCG) 1-29
1.4.3.1 Feature List 1-29
1.4.4 Micro Second Channel Interface (MSC) 1-31
1.4.4.1 Feature List 1-32
1.4.5 FlexRay™ Protocol Controller (E-Ray) 1-33
1.4.5.1 E-Ray Kernel Description 1-33
1.4.5.2 Overview 1-34
1.4.5.3 Features List 1-34
1.4.6 MultiCAN Controller 1-36
1.4.6.1 MultiCAN Feature List 1-37
1.4.6.2 TTCAN Feature List 1-38
1.4.7 Micro Link Serial Bus Interface (MLI) 1-39
1.4.7.1 MLI Feature List 1-39
1.4.8 Single Edge Nibble Transmission (SENT) 1-41
1.4.8.1 SENT Kernel Description 1-41
1.4.9 SENT Feature Overview 1-42
1.4.10 General Purpose Timer Array (GPTAv5) 1-44
1.4.10.1 GPTA0 and GPTA1 Feature List 1-44
1.4.10.2 LTCA2 Feature List 1-46
1.4.11 Capture/Compare Unit 6 (CCU6) 1-47
1.4.11.1 Feature List. 1-47
1.4.12 General Purpose Timer (GPT12) 1-48
1.4.12.1 Feature List 1-49
1.4.13 External Bus Interface (EBU) 1-50
1.4.13.1 Feature List 1-50
1.4.14 Analog-to-Digital Converters (ADC/FADC) 1-51
1.4.15 ADC Module 1-51
1.4.15.1 Feature List 1-52
1.4.16 FADC Module 1-52
1.4.16.1 FADC Feature List 1-54
1.5 On-Chip Debug Support (OCDS) 1-55
1.5.1 On-Chip Debug Support 1-55
1.5.2 Real Time Trace 1-56
1.5.3 Calibration Support 1-56
1.5.4 Tool Interfaces 1-56
1.5.5 Self-Test Support 1-57
1.5.6 FAR Support 1-57

2 CPU Subsystem 2-1
2.1 TC1798 Processor Subsystem 2-1
2.2 Central Processing Unit Features 2-2

2.2.1 CPU Diagram . . . 2-4
2.2.2 Instruction Fetch Unit . . . 2-5
2.2.3 Execution Unit . . . 2-6
2.2.4 General Purpose Register File . . . 2-7
2.3 Summary of functional changes from TC1.3.1 . . . 2-8
2.4 CPU Implementation-Specific Features . . . 2-10
2.4.1 Context Save Areas . . . 2-10
2.4.2 Program Counter (PC) Register . . . 2-10
2.4.3 Store Buffers . . . 2-10
2.4.4 Interrupt System . . . 2-12
2.4.4.1 Interrupt Acknowledge Decoupling for Safety Systems . . . 2-12
2.4.5 Trap System . . . 2-12
2.4.6 Memory Integrity Error Handling . . . 2-13
2.4.6.1 Program Side Memories . . . 2-14
2.4.6.2 Data Side Memories . . . 2-16
2.5 CPU Subsystem Registers . . . 2-19
2.6 CPU Core Special Function Registers (CSFR) . . . 2-20
2.6.1 Registers . . . 2-22
2.7 CPU General Purpose Registers . . . 2-30
2.8 CPU Memory Protection Registers . . . 2-33
2.9 Temporal Protection Registers . . . 2-37
2.10 FPU Registers . . . 2-38
2.10.1 Registers . . . 2-39
2.11 Memory Integrity Registers . . . 2-40
2.11.1 Register Descriptions . . . 2-42
2.12 CPU Slave Interface (CPS) Registers . . . 2-59
2.12.1 Register Descriptions . . . 2-60
2.13 Core Debug and Performance Counter Registers . . . 2-62
2.14 Implementation Specific Reset Values . . . 2-65
2.15 CPU Instruction Timing . . . 2-66
2.15.1 Integer-Pipeline Instructions . . . 2-67
2.15.1.1 Simple Arithmetic Instruction Timings . . . 2-67
2.15.1.2 Multiply Instruction Timings . . . 2-71
2.15.1.3 Multiply Accumulate (MAC) Instruction Timing . . . 2-72
2.15.1.4 Control Flow Instruction Timing . . . 2-73
2.15.2 Load-Store Pipeline Instructions . . . 2-74
2.15.2.1 Address Arithmetic Timing . . . 2-74
2.15.2.2 CSA Control Flow Instruction Timing . . . 2-75
2.15.2.3 Load Instruction Timing . . . 2-75
2.15.2.4 Store Instruction Timing . . . 2-77
2.15.3 Floating Point Pipeline Timing . . . 2-78
2.16 Program Memory Interface (PMI) . . . 2-79
2.16.1 PMI Features . . . 2-79

2.16.2 Scratchpad RAM . . . 2-80
2.16.3 Instruction Cache . . . 2-80
2.16.4 Program Line Buffer . . . 2-82
2.16.5 CPU Slave Interface (CPS) . . . 2-82
2.16.6 PMI Registers . . . 2-82
2.16.6.1 PMI Register Descriptions . . . 2-83
2.17 Data Memory Interface (DMI) . . . 2-88
2.17.1 DMI Features . . . 2-88
2.17.2 Data Scratchpad RAM (DSPR) . . . 2-89
2.17.3 Data Cache . . . 2-89
2.17.4 DMI Trap Generation . . . 2-90
2.18 Memory Configuration . . . 2-92
2.18.1 DMI Registers . . . 2-93
2.18.1.1 DMI Register Descriptions . . . 2-94
2.19 Safety Features . . . 2-99
2.19.1 SRI Address Phase Error Injection . . . 2-99
2.19.2 SRI Data Phase Error Capture . . . 2-99
2.19.3 Safety Interrupt Acknowledge Decoupling . . . 2-99
2.19.4 Registers Implementing Safety Features . . . 2-100

3 System Control Unit (SCU) . . . 3-1
3.1 Clock System Overview . . . 3-2
3.1.1 Clock Generation Unit . . . 3-4
3.1.1.1 Overview . . . 3-4
3.1.1.2 Oscillator Circuit (OSC) . . . 3-5
3.1.1.3 Phase-Locked Loop (PLL) Module . . . 3-7
3.1.1.4 ERAY Phase-Locked Loop (PLL_ERAY) Module . . . 3-16
3.1.1.5 Clock Control Unit . . . 3-23
3.1.1.6 External Clock Output . . . 3-26
3.1.1.7 CGU Registers . . . 3-31
3.1.2 Module Clock Generation . . . 3-53
3.1.2.1 Clock Control Register CLC . . . 3-54
3.2 Reset Operation . . . 3-68
3.2.1 Overview . . . 3-68
3.2.2 Reset Types . . . 3-68
3.2.3 Reset Sources Overview . . . 3-69
3.2.4 Module Reset Behavior . . . 3-69
3.2.5 General Reset Operation . . . 3-70
3.2.6 Reset State Machine . . . 3-71
3.2.7 Reset Counters (RSTCNTA and RSTCNTD) . . . 3-72
3.2.8 De-assertion of a Reset . . . 3-73
3.2.8.1 Example1: . . . 3-73
3.2.8.2 Example2: . . . 3-73

3.2.8.3 Example3: . . . 3-73
3.2.9 Reset Triggers . . . 3-74
3.2.9.1 Specific Reset Triggers . . . 3-74
3.2.9.2 Configurable Reset Triggers . . . 3-74
3.2.10 Debug Specific Behavior . . . 3-74
3.2.11 EEC Reset Specific Behavior . . . 3-74
3.2.12 Reset Controller Registers . . . 3-75
3.2.12.1 Status Registers . . . 3-75
3.2.12.2 Configuration Registers . . . 3-77
3.3 External Interface . . . 3-82
3.3.1 External Service Requests (ESRx) . . . 3-82
3.3.1.1 ESRx as Reset Request Trigger . . . 3-82
3.3.1.2 ESRx as Reset Output . . . 3-83
3.3.1.3 ESR Registers . . . 3-84
3.3.2 External Request Unit (ERU) . . . 3-91
3.3.2.1 Introduction . . . 3-91
3.3.2.2 ERU Pin Connections . . . 3-93
3.3.2.3 External Request Select Unit (ERS) . . . 3-93
3.3.2.4 Event Trigger Logic (ETL) . . . 3-94
3.3.2.5 Connecting Matrix . . . 3-96
3.3.2.6 Output Gating Unit (OGU) . . . 3-98
3.3.2.7 ERU Output Connections . . . 3-102
3.3.2.8 External Request Unit Registers . . . 3-104
3.4 Power Management . . . 3-120
3.4.1 Power Management Overview . . . 3-120
3.4.2 Power Management Modes . . . 3-121
3.4.2.1 Idle Mode . . . 3-121
3.4.2.2 Sleep Mode . . . 3-122
3.4.3 Power Management Control and Status Register, PMCSR . . . 3-122
3.5 Software Boot Support . . . 3-125
3.5.1 Configuration done with Start-up . . . 3-125
3.5.2 Start-up Configuration Options . . . 3-125
3.5.3 Start-up Registers . . . 3-126
3.5.3.1 Start-up Status Register . . . 3-126
3.6 ECC Error Handling . . . 3-129
3.6.1 ECC Software Testing Support . . . 3-129
3.6.2 ECC Registers . . . 3-130
3.7 Die Temperature Measurement . . . 3-136
3.7.1 Die Temperature Sensor Register . . . 3-137
3.8 Watchdog Timer . . . 3-139
3.8.1 Watchdog Timer Overview . . . 3-139
3.8.2 Features of the Watchdog Timer . . . 3-139
3.8.3 The Endinit Function . . . 3-140

3.8.3.1 Password Access to WDT_CON0 . . . 3-142
3.8.3.2 Modify Access to WDT_CON0 . . . 3-143
3.8.3.3 Access to Endinit-Protected Registers . . . 3-144
3.8.4 Timer Operation . . . 3-145
3.8.4.1 Timer Modes . . . 3-145
3.8.4.2 WDT Reset Behavior . . . 3-146
3.8.4.3 WDT Operation During Power-Saving Modes . . . 3-148
3.8.4.4 Suspend Mode Support . . . 3-148
3.8.5 Watchdog Timer Registers . . . 3-149
3.8.5.1 Watchdog Timer Control Register 0 . . . 3-149
3.8.5.2 Watchdog Timer Control Register 1 . . . 3-151
3.8.5.3 Watchdog Timer Status Register . . . 3-152
3.9 Emergency Stop Output Control . . . 3-155
3.9.1 Emergency Stop Register . . . 3-157
3.10 Interrupt Generation . . . 3-159
3.10.1 Interrupt Control Registers . . . 3-160
3.11 NMI Trap Generation . . . 3-171
3.11.1 Trap Control Registers . . . 3-172
3.12 Miscellaneous System Control Register . . . 3-181
3.12.1 GPTA Input IN1 Control . . . 3-181
3.12.2 System Control Register . . . 3-181
3.12.3 Identification Registers . . . 3-183
3.12.4 Memory Test Register . . . 3-187
3.12.4.1 Register MEMTEST . . . 3-187
3.12.5 SCU Kernel Registers . . . 3-187
3.12.6 SCU Address Area . . . 3-193

4 On-Chip System Buses and Bus Bridges . . . 4-1
4.1 What is new . . . 4-1
4.2 SRI Crossbar (XBar_SRI) . . . 4-3
4.2.1 Introduction . . . 4-3
4.2.1.1 XBar_SRI Features . . . 4-5
4.2.2 SRI Transactions . . . 4-5
4.2.3 SRI Op-Codes . . . 4-6
4.2.4 SRI Error Conditions . . . 4-7
4.2.5 SRI Transaction ID Error Conditions . . . 4-7
4.2.6 Operational Overview . . . 4-8
4.2.6.1 Functional Blocks . . . 4-9
4.2.7 Functional Overview . . . 4-12
4.2.7.1 Arbitration Block . . . 4-12
4.2.7.2 Default Slave . . . 4-17
4.2.7.3 SRI ECC Error Handling . . . 4-18
4.2.7.4 Error Tracking Capability . . . 4-19

4.2.7.5 Debug Trigger Event Generation (OCDS Level 1) 4-21
4.2.7.6 Interrupt and Debug Events of the XBar_SRI Module 4-22
4.2.8 Implementation of the Cross Bar (XBar_SRI) in the TC1798 4-24
4.2.8.1 Mapping of SRI Master Modules to XBar_SRI Master Interfaces . 4-24
4.2.8.2 Mapping of SRI Slave modules to XBar_SRI Slave Interfaces . . . 4-25
4.2.8.3 TC1798 SRI Master / Slave Interconnection Matrix 4-26
4.2.8.4 Connection Master-Slave in XBar_SRI 4-26
4.2.9 SRI Crossbar Registers 4-28
4.2.9.1 TC1798 Control Registers 4-34
4.3 Shared Resource Interconnect to FPI Bus Interface (SFI Bridge) 4-64
4.3.1 Functional Overview 4-64
4.4 System Peripheral Bus 4-65
4.4.1 Overview 4-65
4.4.2 Bus Transaction Types 4-67
4.4.3 Reaction of a Busy Slave 4-67
4.4.4 Address Alignment Rules 4-68
4.4.5 FPI Bus Basic Operations 4-68
4.5 FPI Bus Control Unit (SBCU) 4-70
4.5.1 FPI Bus Arbitration 4-70
4.5.1.1 Arbitration on the System Peripheral Bus 4-70
4.5.1.2 Starvation Prevention 4-72
4.5.2 FPI Bus Error Handling 4-72
4.5.3 BCU Debug Support 4-75
4.5.3.1 Address Triggers 4-75
4.5.3.2 Signal Status Triggers 4-76
4.5.3.3 Combination of Triggers 4-77
4.5.3.4 BCU Breakpoint Generation Examples 4-77
4.5.4 System Bus Control Unit Registers 4-80
4.5.4.1 SBCU ID Register Description 4-82
4.5.4.2 SBCU Control Registers Descriptions 4-83
4.5.4.3 SBCU Error Registers Descriptions 4-84
4.5.4.4 SBCU OCDS Registers Descriptions 4-88
4.5.4.5 SBCU Service Request Control Register Description 4-102
4.6 On Chip Bus Master TAG Assignments 4-103

5 Program Memory Unit (PMU) 5-1
5.1 Generic Feature List 5-1
5.2 PMU Configuration of TC1798 5-2
5.2.1 Features of the BootROM 5-3
5.2.2 Features of Program and Data Flash 5-4
5.3 BootROM 5-5
5.4 Tuning Protection 5-5
5.5 Flash 5-6

5.5.1 Definition of Terms . . . 5-6
5.5.2 Flash Structure . . . 5-7
5.5.3 Flash Read Access . . . 5-9
5.5.4 Flash Operations . . . 5-10
5.5.4.1 Modes of Operation . . . 5-10
5.5.4.2 Command Sequences . . . 5-10
5.5.4.3 Command Sequence Definitions . . . 5-11
5.5.4.4 Concurrent Operations . . . 5-18
5.5.5 Flash Protection . . . 5-19
5.5.5.1 Effective Flash Read Protection . . . 5-20
5.5.5.2 Effective Flash Write Protection . . . 5-20
5.5.5.3 Configuring Flash Protection in the UCB . . . 5-21
5.5.5.4 System Wide Effects of Flash Protection . . . 5-22
5.5.6 Data Integrity and Safety . . . 5-23
5.5.6.1 ECC . . . 5-23
5.5.6.2 Margin Checks . . . 5-24
5.5.7 Interrupts and Traps . . . 5-25
5.5.8 Reset and Startup . . . 5-25
5.5.9 Power Reduction . . . 5-26
5.6 Register Set . . . 5-27
5.6.1 PMU Registers . . . 5-27
5.6.1.1 PMU Identification . . . 5-28
5.6.2 Flash Registers . . . 5-30
5.6.2.1 Flash Status . . . 5-31
5.6.2.2 Flash Configuration Control . . . 5-40
5.6.2.3 Flash Read Buffer Configuration . . . 5-46
5.6.2.4 Flash Identification Register . . . 5-46
5.6.2.5 Flash Reservation Semaphore . . . 5-48
5.6.2.6 Margin Check Control . . . 5-50
5.6.2.7 Protection Configuration Indication . . . 5-52
5.6.2.8 Flash ECC Access . . . 5-60
5.6.2.9 SHE Secure Internal Flash Boot . . . 5-62
5.7 Application Hints . . . 5-64
5.7.1 Changes with Respect to Audo-NG and Audo-F . . . 5-64
5.7.2 Performing Flash Operations . . . 5-65
5.7.3 EEPROM Emulation With DFlash . . . 5-67
5.7.3.1 Robust EEPROM Emulation . . . 5-68
5.7.4 Performance Considerations . . . 5-68
5.7.5 Handling Flash Protection . . . 5-69
5.7.6 Cooperation with SHE . . . 5-70
5.7.7 Handling Errors . . . 5-71
5.7.7.1 Handling Errors During Operation . . . 5-71
5.7.7.2 Handling Errors During Startup . . . 5-75

5.7.8 Resets During Flash Operation 5-76
5.7.8.1 General Advice 5-77
5.7.8.2 Advice for EEPROM Emulation 5-77
5.7.8.3 Recovery From Aborted Logical Sector Erase (“ALSE”) 5-78
5.7.9 ECC 5-79

6 Local Memory Unit (LMU) 6-1
6.1 Feature List 6-1
6.2 Local Memory 6-1
6.3 Emulation Memory (EMEM) 6-2
6.4 Online Data Acquisition (OLDA) and its Overlay 6-3
6.5 Clock Control 6-3
6.6 LMU Registers 6-4

7 Data Access Overlay (OVC) 7-1
7.1 Basic Overlay Control 7-1
7.2 Online Data Acquisition (OLDA) and its Overlay 7-4
7.3 Enable Control of Overlay Blocks 7-4
7.4 Target and Overlay Memories 7-5
7.4.1 Target Memories 7-5
7.4.2 Internal Overlay Memory 7-5
7.4.3 Emulation Overlay Memory 7-6
7.4.4 External Overlay Memory 7-6
7.5 Change of Overlay Parameters and Overlay Start 7-6
7.6 Concurrent Matches and Access Performance 7-6
7.7 Overlay Control Registers 7-7

8 BootROM Content 8-1
8.1 Startup Software 8-1
8.1.1 Boot Options Summary 8-1
8.1.2 Startup Software Main Flow 8-2
8.1.2.1 Entering the Startup Software 8-3
8.1.2.2 Initial Handling of the Startup Configuration 8-3
8.1.2.3 Flash Rampup 8-3
8.1.2.4 Basic Device Settings 8-4
8.1.2.5 Select and Prepare Startup Modes 8-4
8.1.2.6 Final Chip Settings 8-6
8.1.2.7 Ending the SSW and Starting the User Code 8-8
8.1.3 Specific SSW Features 8-9
8.1.3.1 Header Check in Alternate Boot Modes 8-9
8.1.4 Startup Errors Handling 8-12
8.2 Bootstrap Loaders 8-13
8.2.1 Common Procedures for all Bootloaders 8-13
8.2.2 ASC Bootstrap loader 8-14

8.2.3 CAN Bootstrap Loader 8-14
8.3 Additional information and usage hints 8-16
8.3.1 Conditions upon user code start 8-16
8.3.2 RAMs Handling 8-16
8.3.3 Influencing the next SSW-execution 8-16
8.3.4 TC1798 registers modified by SSW 8-17

9 Memory Maps 9-1
9.1 What is new 9-2
9.2 How to Read the Address Maps 9-4
9.3 Contents of the Segments 9-6
9.4 Address Map of the On Chip Bus System 9-8
9.4.1 Segments 0 to 14 9-8
9.4.2 Segment 15 9-13
9.5 Memory Module Access Restrictions 9-21
9.6 Side Effects from Modules to Data Scratch Pad SRAM (DSPR) 9-22

10 General Purpose I/O Ports and Peripheral I/O Lines (Ports) 10-1
10.1 Basic Port Operation 10-3
10.2 Description Scheme for the Port IO Functions 10-5
10.3 Port Register Description 10-7
10.3.1 Port Input/Output Control Registers 10-11
10.3.2 Pad Driver Mode Register 10-16
10.3.3 Pin Function Decision Control Register 10-20
10.3.4 Port Output Register 10-21
10.3.5 Port Output Modification Register 10-22
10.3.6 Emergency Stop Register 10-24
10.3.7 Port Input Register 10-25
10.4 Port 0 10-27
10.4.1 Port 0 Configuration 10-27
10.4.2 Port 0 Function Table 10-28
10.4.3 Port 0 Registers 10-32
10.4.3.1 Port 0 Emergency Stop Register 10-32
10.5 Port 1 10-33
10.5.1 Port 1 Configuration 10-33
10.5.2 Port 1 Function Table 10-34
10.5.3 Port 1 Registers 10-37
10.5.3.1 Port 1 Emergency Stop Register 10-38
10.6 Port 2 10-39
10.6.1 Port 2 Configuration 10-39
10.6.2 Port 2 Function Table 10-39
10.6.3 Port 2 Registers 10-44
10.6.3.1 Port 2 Output Register 10-44
10.6.3.2 Port 2 Output Modification Register 10-44

10.6.3.3 Port 2 Input/Output Control Register 0 10-45
10.6.3.4 Port 2 Input Register 10-45
10.6.3.5 Port 2 Pad Driver Mode 0 Register 10-46
10.6.3.6 Port 2 Emergency Stop Register 10-46
10.7 Port 3 10-48
10.7.1 Port 3 Configuration 10-48
10.7.2 Port 3 Function Table 10-48
10.7.3 Port 3 Registers 10-54
10.8 Port 4 10-55
10.8.1 Port 4 Configuration 10-55
10.8.2 Port 4 Function Table 10-55
10.8.3 Port 4 Registers 10-60
10.9 Port 5 10-62
10.9.1 Port 5 Configuration 10-64
10.9.2 Port 5 Function Table 10-64
10.9.3 Port 5 Registers 10-69
10.9.3.1 Port 5 Output Register 10-69
10.9.3.2 Port 5 Output Modification Register 10-69
10.9.3.3 Port 5 Input Register 10-69
10.9.3.4 Port 5 Emergency Stop Register 10-69
10.10 Port 6 10-70
10.10.1 Port 6 Configuration 10-70
10.10.2 Port 6 Function Table 10-71
10.10.3 Port 6 Registers 10-75
10.10.3.1 Port 6 Output Register 10-75
10.10.3.2 Port 6 Output Modification Register 10-75
10.10.3.3 Port 6 Input Register 10-75
10.10.3.4 Port 6 Pad Driver Mode 0 Register 10-76
10.11 Port 7 10-77
10.11.1 Port 7 Configuration 10-77
10.11.2 Port 7 Function Table 10-78
10.11.3 Port 7 Registers 10-80
10.11.3.1 Port 7 Output Register 10-80
10.11.3.2 Port 7 Output Modification Register 10-80
10.11.3.3 Port 7 Input Register 10-80
10.12 Port 8 10-81
10.12.1 Port 8 Configuration 10-81
10.12.2 Port 8 Function Table 10-82
10.12.3 Port 8 Register 10-85
10.12.3.1 Port 8 Output Register 10-85
10.12.3.2 Port 8 Output Modification Register 10-85
10.12.3.3 Port 8 Input Register 10-85
10.12.3.4 Port 8 Emergency Stop Register 10-85

10.13 Port 9 10-86
10.13.1 Port 9 Configuration 10-86
10.13.2 Port 9 Function Table 10-87
10.13.3 Port 9 Registers 10-92
10.13.3.1 Port 9 Output Register 10-92
10.13.3.2 Port 9 Output Modification Register 10-92
10.13.3.3 Port 9 Input/Output Control Register 8 10-93
10.13.3.4 Port 9 Input Register 10-93
10.13.3.5 Port 9 Pad Driver Mode 1 Register 10-94
10.13.3.6 Port 9 Pad Driver Mode 1 Register 10-95
10.13.3.7 Port 9 Emergency Stop Register 10-95
10.14 Port 10 10-96
10.14.1 Port 10 Configuration 10-96
10.14.2 Port 10 Function Table 10-96
10.14.3 Port 10 Registers 10-98
10.14.3.1 Port 10 Output Register 10-98
10.14.3.2 Port 10 Output Modification Register 10-98
10.14.3.3 Port 10 Input/Output Control Register 4 10-99
10.14.3.4 Port 10 Input Register 10-99
10.14.3.5 Port 10 Pad Driver Mode 0 Register 10-100
10.15 Port 11 10-101
10.15.1 Port 11 Configuration 10-101
10.15.2 Port 11 Function Table 10-102
10.15.3 Port 11 Registers 10-106
10.16 Port 12 10-107
10.16.1 Port 12 Configuration 10-107
10.16.2 Port 12 Function Table 10-108
10.16.3 Port 12 Registers 10-109
10.16.3.1 Port 12 Output Register 10-110
10.16.3.2 Port 12 Output Modification Register 10-110
10.16.3.3 Port 12 Input Register 10-110
10.17 Port 13 10-111
10.17.1 Port 13 Configuration 10-111
10.17.2 Port 13 Function Table 10-112
10.17.3 Port 13 Registers 10-117
10.17.3.1 Port 13 Emergency Stop Register 10-117
10.18 Port 14 10-118
10.18.1 Port 14 Configuration 10-118
10.18.2 Port 14 Function Table 10-119
10.18.3 Port 14 Registers 10-124
10.18.3.1 Port 14 Emergency Stop Register 10-124
10.19 Port 15 10-125
10.19.1 Port 15 Configuration 10-125

10.19.2 Port 15 Function Table 10-126
10.19.3 Port 15 Registers 10-131
10.20 Port 16 10-132
10.20.1 Port 16 Configuration 10-132
10.20.2 Port 16 Function Table 10-133
10.20.3 Port 16 Registers 10-137
10.20.3.1 Port 16 Output Register 10-137
10.20.3.2 Port 16 Output Modification Register 10-137
10.20.3.3 Port 16 Input/Output Control Register 12 10-138
10.20.3.4 Port 16 Input Register 10-138
10.20.3.5 Port 16 Emergency Stop Register 10-139
10.20.3.6 Port 16 Pad Driver Mode 1 Register 10-140
10.21 Port 17 10-141
10.21.1 Port 17 Configuration 10-141
10.21.2 Port 17 Function Table 10-142
10.21.3 Port 17 Registers 10-144
10.21.4 Port 17 Input/Output Control Registers 10-145
10.21.5 Port 17 Pin Function Decision Control Register 10-148
10.22 Port 18 10-152
10.22.1 Port 18 Configuration 10-152
10.22.2 Port 18 Function Table 10-153
10.22.3 Port 18 Registers 10-155
10.22.3.1 Port 18 Output Register 10-155
10.22.3.2 Port 18 Output Modification Register 10-155
10.22.3.3 Port 18 Input Register 10-155
10.22.3.4 Port 18 Emergency Stop Register 10-155

11 Peripheral Control Processor (PCP) 11-1
11.1 PCP Feature/Enhancement History List 11-1
11.1.1 Switchable Core Clock Ratio 11-2
11.2 Peripheral Control Processor Overview 11-2
11.2.1 High Integrity Operation 11-2
11.3 PCP Architecture 11-3
11.3.1 PCP Processor 11-4
11.3.2 PCP Code Memory 11-5
11.3.2.1 CMEM Protection 11-5
11.3.3 PCP Parameter RAM 11-5
11.3.3.1 PRAM Protection 11-6
11.3.4 FPI Bus Interface 11-6
11.3.5 PCP Interrupt Control Unit and Service Request Nodes 11-6
11.4 PCP Programming Model 11-8
11.4.1 General Purpose Register Set of the PCP 11-8
11.4.1.1 Register R0 11-9

11.4.1.2 Registers R1, R2, and R3 . . . 11-9
11.4.1.3 Registers R4 and R5 . . . 11-9
11.4.1.4 Register R6 . . . 11-10
11.4.1.5 Register R7 . . . 11-11
11.4.2 Contexts and Context Models . . . 11-13
11.4.2.1 Context Models . . . 11-13
11.4.2.2 Context Save Area . . . 11-16
11.4.2.3 Context Restore Operation for CR6 and CR7 . . . 11-19
11.4.2.4 Context Save Operation for CR6 and CR7 . . . 11-23
11.4.2.5 Initialization of the Contexts . . . 11-26
11.4.2.6 Context Save Optimization . . . 11-26
11.4.3 Channel Programs . . . 11-27
11.4.3.1 Channel Restart Mode . . . 11-27
11.4.3.2 Channel Resume Mode . . . 11-28
11.5 PCP Operation . . . 11-30
11.5.1 PCP Initialization . . . 11-30
11.5.2 Channel Invocation and Context Restore Operation . . . 11-30
11.5.3 Channel Exit and Context Save Operation . . . 11-31
11.5.3.1 Normal Exit . . . 11-31
11.5.3.2 Error Condition Channel Exit . . . 11-32
11.5.3.3 Debug Exit . . . 11-33
11.6 PCP Interrupt Operation . . . 11-34
11.6.1 Issuing Service Requests to CPU or PCP . . . 11-35
11.6.2 PCP Interrupt Control Unit . . . 11-35
11.6.3 PCP Service Request Nodes . . . 11-35
11.6.4 Issuing PCP Service Requests . . . 11-36
11.6.4.1 Service Request on EXIT Instruction . . . 11-37
11.6.4.2 Service Request on Suspension of Interrupt . . . 11-37
11.6.4.3 Service Request on Error . . . 11-38
11.6.4.4 Queue Full Operation . . . 11-38
11.7 PRAM Protection . . . 11-39
11.7.1 Protection of PRAM against FPI Writes . . . 11-41
11.7.2 Protection of PRAM against Internally Generated PRAM Writes . . . 11-41
11.7.2.1 Context Save Region Protection . . . 11-41
11.7.2.2 Protected Channel PRAM Protection . . . 11-42
11.8 FPI Interface . . . 11-42
11.8.1 Operation as an FPI Master . . . 11-42
11.8.2 Operation as an FPI Slave . . . 11-43
11.9 PCP Error Handling . . . 11-44
11.9.1 PRAM Protection Violation . . . 11-44
11.9.1.1 Enforced PRAM Partitioning . . . 11-44
11.9.1.2 Protected Channel PRAM . . . 11-45
11.9.2 FPI Write Window Violation . . . 11-45

11.9.3 Channel Watchdog 11-45
11.9.4 Invalid Opcode 11-45
11.9.5 Instruction Address Error 11-46
11.10 Software In-System Test Support 11-46
11.11 Memory Integrity Error Detection and Correction 11-47
11.11.1 Definitions 11-48
11.11.2 Architectural Extensions - Registers 11-48
11.11.3 Memory Integrity Error Control 11-48
11.12 Instruction Set Overview 11-49
11.12.1 DMA Primitives 11-49
11.12.2 Load and Store 11-50
11.12.3 Arithmetic and Logical Instructions 11-51
11.12.4 Bit Manipulation 11-53
11.12.5 Flow Control 11-53
11.12.6 Addressing Modes 11-54
11.12.6.1 FPI Bus Addressing 11-54
11.12.6.2 PRAM Addressing 11-55
11.12.6.3 Bit Addressing 11-55
11.12.6.4 Flow Control Destination Addressing 11-55
11.13 FPI Interface 11-57
11.13.1 Access to the PCP Control Registers from the FPI Bus 11-57
11.13.1.1 PCP Control Register Protection 11-57
11.13.2 Access to the PRAM from the FPI Bus 11-58
11.13.3 Access to the CMEM from the FPI Bus 11-58
11.14 Debugging the PCP 11-60
11.15 PCP Registers 11-62
11.16 PCP Registers Address Space 11-66
11.17 Registers 11-67
11.17.1 PCP Clock Control Register, PCP_CLC 11-67
11.17.2 PCP Module Identification Register, PCP_ID 11-68
11.17.3 PCP Control and Status Register, PCP_CS 11-69
11.17.4 PCP Error/Debug Status Register, PCP_ES 11-71
11.17.5 PCP Interrupt Control Register, PCP_ICR 11-73
11.17.6 PCP Interrupt Threshold Register, PCP_ITR 11-76
11.17.7 PCP Interrupt Configuration Register, PCP_ICON 11-77
11.17.8 PCP Stall Status Register, PCP_SSR 11-79
11.17.9 SIST Mode Access Control Register, PCP_SMACON 11-81
11.17.10 Memory Integrity Error Control Register, PCP_MIECON 11-82
11.17.11 Memory Integrity Error Status Register for PRAM, PCP_MIESTATP 11-83
11.17.12 Memory Integrity Error Status Register for CMEM, PCP_MIESTATC 11-84
11.17.13 Register Protection Register, PCP_RPROT 11-85
11.17.14 CMEM Protection Register, PCP_CPROT 11-86

11.17.15 PRAM Protection Register, PCP_PPROT 11-87
11.17.16 FPI Write Window Register, PCP_FWWIN 11-91
11.17.17 PCP Service Request Control Registers m, PCP_SRC[1:0] 11-92
11.17.18 PCP Service Request Control Registers m, PCP_SRC[3:2] 11-94
11.17.19 PCP Service Request Control Registers m, PCP_SRC[8:4] 11-95
11.17.20 PCP Service Request Control Registers m, PCP_SRC[11:9] 11-96
11.18 PCP Instruction Set Details 11-98
11.18.1 Instruction Codes and Fields 11-98
11.18.1.1 Conditional Codes 11-99
11.18.1.2 Instruction Fields 11-100
11.18.2 Counter Operation for COPY Instruction 11-103
11.18.3 Counter Operation for BCOPY Instruction 11-104
11.18.4 Divide and Multiply Instructions 11-105
11.18.5 ADD, 32-bit Addition 11-106
11.18.6 AND, 32-bit Logical AND 11-107
11.18.7 BCOPY, DMA Operation 11-108
11.18.8 CHKB, Check Bit 11-109
11.18.9 CLR, Clear Bit 11-109
11.18.10 COMP, 32-bit Compare 11-110
11.18.11 COPY, DMA Instruction 11-111
11.18.12 DEBUG, Debug Instruction 11-112
11.18.13 DINIT, Divide Initialization 11-113
11.18.14 DSTEP, Divide Instruction 11-114
11.18.15 EXIT, Exit Instruction 11-115
11.18.16 INB, Insert Bit 11-116
11.18.17 JC, Jump Conditionally 11-117
11.18.18 JL, Jump Long Unconditional 11-118
11.18.19 LD, Load 11-118
11.18.20 LDL, Load 16-bit Value 11-120
11.18.21 MINIT, Multiply Initialization 11-120
11.18.22 MOV, Move Register to Register 11-121
11.18.23 Multiply Instructions 11-122
11.18.24 NEG, Negate 11-123
11.18.25 NOP, No Operation 11-123
11.18.26 NOT, Logical NOT 11-123
11.18.27 OR, Logical OR 11-124
11.18.28 PRAM Bit Operations 11-125
11.18.29 PRI, Prioritize 11-126
11.18.30 RL, Rotate Left 11-127
11.18.31 RR, Rotate Right 11-127
11.18.32 SET, Set Bit 11-128
11.18.33 SHL, Shift Left 11-128
11.18.34 SHR, Shift Right 11-129

11.18.35 ST, Store . . . 11-130
11.18.36 SUB, 32-bit Subtract . . . 11-131
11.18.37 XCH, Exchange . . . 11-132
11.18.38 XOR, 32-bit Logical Exclusive OR . . . 11-133
11.18.39 Flag Updates of Instructions . . . 11-134
11.18.40 Instruction Timing . . . 11-135
11.19 Instruction Encoding . . . 11-139
11.20 Programming of the PCP . . . 11-145
11.20.1 Initial PC of a Channel Program . . . 11-145
11.20.1.1 Channel Entry Table . . . 11-145
11.20.1.2 Channel Resume . . . 11-146
11.20.2 Channel Management for Small and Minimum Contexts . . . 11-147
11.20.3 Unused Registers as Global's or Constants . . . 11-147
11.20.4 Dispatch of Low Priority Tasks . . . 11-148
11.20.5 Code Reuse Across Channels (Call and Return) . . . 11-148
11.20.6 Case-like Code Switches (Computed Go-To) . . . 11-149
11.20.7 Simple DMA Operation . . . 11-149
11.20.7.1 COPY Instruction . . . 11-149
11.20.7.2 BCOPY Instruction (Burst Copy) . . . 11-150
11.21 PCP Programming Notes and Tips . . . 11-151
11.21.1 Notes on PCP Configuration . . . 11-151
11.21.2 General Purpose Register Use . . . 11-151
11.21.3 Use of Channel Interruption . . . 11-153
11.21.3.1 Dynamic Interrupt Masking . . . 11-153
11.21.3.2 Control of Channel Priority (CPPN) . . . 11-153
11.21.4 Implementing Divide Algorithms . . . 11-154
11.21.5 Implementing Multiply Algorithms . . . 11-155
11.22 Implementation of the PCP in the TC1798 . . . 11-157
11.22.1 PCP Memories . . . 11-157
11.22.2 BCOPY Instruction . . . 11-157
11.22.3 PCP Reset Operation . . . 11-157

12 Direct Memory Access Controller (DMA) . . . 12-1
12.1 What is new . . . 12-1
12.2 DMA Controller Kernel Description . . . 12-2
12.2.1 Features . . . 12-3
12.2.2 Definition of Terms . . . 12-4
12.2.3 DMA Principles . . . 12-5
12.2.4 DMA Channel Functionality . . . 12-6
12.2.4.1 Shadowed Source or Destination Address . . . 12-6
12.2.4.2 DMA Channel Request Control . . . 12-10
12.2.4.3 DMA Channel Operation Modes . . . 12-11
12.2.4.4 Error Conditions . . . 12-15

12.2.4.5 Channel Reset Operation 12-16
12.2.4.6 Transfer Count and Move Count 12-17
12.2.4.7 Circular Buffer 12-19
12.2.5 Transaction Control Engine 12-20
12.2.6 Bus Switch, Bus Switch Priorities 12-21
12.2.7 DMA Module Priorities on On Chip Busses (FPI Bus, SRI Bus) . . . 12-23
12.2.8 DMA Module: On Chip Bus Access Rights, RMW support 12-24
12.2.9 DMA Module On Chip Bus Master Interfaces 12-25
12.2.10 DMA Module Bridge Functionality 12-26
12.2.11 On-Chip Debug Capabilities 12-27
12.2.11.1 Hard-suspend Mode 12-27
12.2.11.2 Soft-suspend Mode 12-27
12.2.11.3 Break Signal Generation 12-28
12.2.12 Interrupts 12-30
12.2.12.1 Channel Interrupts 12-30
12.2.12.2 Transaction Lost Interrupt 12-32
12.2.12.3 Move Engine Interrupts 12-33
12.2.12.4 Wrap Buffer Interrupts 12-35
12.2.12.5 Interrupt Request Compressor 12-36
12.2.13 Pattern Detection 12-37
12.2.13.1 Pattern Compare Logic 12-39
12.2.13.2 Pattern Detection for 8-bit Data Width 12-40
12.2.13.3 Pattern Detection for 16-bit Data Width 12-41
12.2.13.4 Pattern Detection for 32-bit Data Width 12-43
12.2.14 Access Protection 12-44
12.3 DMA Module Registers 12-47
12.3.1 System Registers 12-53
12.3.2 General Control/Status Registers 12-59
12.3.3 Move Engine Registers 12-78
12.3.4 Channel Control/Status Registers 12-85
12.3.5 Channel Address Registers 12-97
12.4 DMA Module Implementation 12-100
12.4.1 DMA Request Wiring Matrix 12-101
12.4.2 Access Protection Assignment 12-111
12.4.3 Implementation-specific DMA Registers 12-123
12.4.3.1 Clock Control Register 12-125
12.4.3.2 DMA Interrupt Registers 12-126
12.4.3.3 MLI Interrupt Registers 12-127
12.4.4 Address Map 12-129
12.5 Memory Checker Module 12-130
12.5.1 Functional Description 12-130
12.5.1.1 Ethernet CRC-32 Endianness 12-131
12.5.2 Memory Checker Module Registers 12-132

12.5.2.1 Memory Checker Module Control Registers 12-133

13 Safe Direct Memory Access Controller (SDMA) 13-1
13.1 What is new 13-1
13.2 SDMA Controller Kernel Description 13-2
13.2.1 Features 13-3
13.2.2 Definition of Terms 13-4
13.2.3 SDMA Principles 13-5
13.2.4 SDMA Channel Functionality 13-6
13.2.4.1 Shadowed Source or Destination Address 13-6
13.2.4.2 SDMA Channel Request Control 13-10
13.2.4.3 SDMA Channel Operation Modes 13-11
13.2.4.4 Error Conditions 13-15
13.2.4.5 Channel Reset Operation 13-16
13.2.4.6 Transfer Count and Move Count 13-17
13.2.4.7 Circular Buffer 13-19
13.2.5 Transaction Control Engine 13-20
13.2.6 Bus Switch, Bus Switch Priorities 13-21
13.2.7 SDMA Module: On Chip Bus Access Rights, RMW support 13-21
13.2.8 SDMA On Chip Bus FPI Master Interface 13-21
13.2.9 On-Chip Debug Capabilities 13-23
13.2.9.1 Hard-suspend Mode 13-23
13.2.9.2 Soft-suspend Mode 13-23
13.2.9.3 Break Signal Generation 13-24
13.2.10 Interrupts 13-26
13.2.10.1 Channel Interrupts 13-26
13.2.10.2 Transaction Lost Interrupt 13-28
13.2.10.3 Move Engine Interrupt 13-29
13.2.10.4 Wrap Buffer Interrupts 13-30
13.2.10.5 Interrupt Request Compressor 13-31
13.2.11 Pattern Detection 13-32
13.2.11.1 Pattern Compare Logic 13-34
13.2.11.2 Pattern Detection for 8-bit Data Width 13-35
13.2.11.3 Pattern Detection for 16-bit Data Width 13-36
13.2.11.4 Pattern Detection for 32-bit Data Width 13-38
13.2.12 Memory Protection 13-38
13.2.13 SDMA Checksums 13-39
13.3 SDMA Module Registers 13-40
13.3.1 System Registers 13-46
13.3.2 General Control/Status Registers 13-51
13.3.3 Move Engine Registers 13-62
13.3.4 Channel Control/Status Registers 13-65
13.3.5 Channel Address Registers 13-77

13.3.6 Memory Protection Registers . . . 13-80
13.3.7 Channel CRC Registers . . . 13-82
13.4 SDMA Module Implementation . . . 13-84
13.4.1 SDMA Request Wiring Matrix . . . 13-84
13.4.2 Implementation-specific SDMA Registers . . . 13-90
13.4.2.1 Clock Control Register . . . 13-92
13.4.2.2 SDMA Interrupt Registers . . . 13-94
13.4.3 Address Map . . . 13-95

14 Flexible CRC Engine (FCE) . . . 14-1
14.1 Related documentation . . . 14-2
14.2 FCE Features . . . 14-3
14.3 Operational overview . . . 14-4
14.4 FCE Functional Description . . . 14-6
14.5 Interfaces of the FCE Module . . . 14-13
14.6 FCE Module Registers . . . 14-14
14.6.1 System Registers . . . 14-17
14.6.2 CRC Kernel Control/Status Registers . . . 14-21
14.7 Programming Guide . . . 14-28
14.8 Properties of CRC code . . . 14-31

15 SRI External Bus Unit (EBU) . . . 15-1
15.1 Overview . . . 15-1
15.2 References . . . 15-1
15.3 Feature List . . . 15-2
15.4 Differences between Audo-Future and Audo-Max EBUs . . . 15-3
15.5 EBU Interface Signals . . . 15-5
15.5.1 Address/Data Bus, AD[31:0] . . . 15-6
15.5.2 Address Bus, A[27:0] . . . 15-6
15.5.3 Global Chip Select, CSCOMB . . . 15-6
15.5.4 Chip Selects, CS[3:0] . . . 15-6
15.5.5 Read/Write Control Lines, RD, RD/WR . . . 15-7
15.5.6 Address Valid, ADV . . . 15-7
15.5.7 Byte Controls, BC[3:0] . . . 15-7
15.5.8 Burst Flash Clock Output/Input, BFCLKO/BFCLKO/BFCLKI . . . 15-8
15.5.9 Wait Input, WAIT . . . 15-8
15.5.10 Burst Address Advance, BAA . . . 15-8
15.5.11 Motorola Peripheral Write Signal, MR/W . . . 15-8
15.5.12 ONFI 2.0 clock Output, OCLKO . . . 15-9
15.5.13 DDR Clock Output/Input DDRCLKO/DDRCLKO/SDCLKI . . . 15-9
15.5.14 LPDDR-NVM, DDRAM, SDRAM Control Signals, CKE, CAS and RAS . . . 15-9
15.5.15 DDR Data Strobes, DQS[3:0] . . . 15-9
15.5.16 Bus Arbitration Signals, HOLD, HLDA, and BREQ . . . 15-9

15.5.17 EBU Reset . . . 15-10
15.5.17.1 Allocation of Unused Signals as GPIO . . . 15-10
15.6 Bus State During Reset . . . 15-12
15.7 Memory Controller Structure . . . 15-13
15.8 Memory Controller Read Architecture . . . 15-15
15.9 Access Arbitration . . . 15-15
15.9.1 Programming Sequence Locking . . . 15-15
15.9.2 Source Access Inhibit . . . 15-16
15.10 Clocking Strategy and Local Clock Generation . . . 15-16
15.10.1 Clocking Modes . . . 15-16
15.10.2 Local Clock Divider . . . 15-17
15.10.3 Standby Mode . . . 15-19
15.10.4 DLL Operation . . . 15-20
15.10.4.1 Locking the DLL . . . 15-21
15.10.4.2 DLL Operating Modes . . . 15-21
15.10.4.3 DLL Related Access Error Conditions . . . 15-22
15.10.4.4 DQ and DQM Outputs (EBU_DLLCON.WR_EN=1_B) . . . 15-22
15.10.4.5 DQS Inputs (EBU_DLLCON.RD_EN=1_B) . . . 15-22
15.10.4.6 Duty Cycle Correction . . . 15-23
15.10.5 DLL Drift detector . . . 15-23
15.10.6 Generation of DDR Control Signals without using the DLL . . . 15-24
15.10.7 Read Data Capture for DDR Devices . . . 15-24
15.10.7.1 Read Data FIFO . . . 15-25
15.10.7.2 FIFO Bypass Mode . . . 15-25
15.10.8 External Bus Clock Generation . . . 15-26
15.11 External Bus Arbitration . . . 15-28
15.11.1 External Bus Modes . . . 15-28
15.11.2 Arbitration Signals and Parameters . . . 15-28
15.11.3 Arbitration Modes . . . 15-30
15.11.3.1 No Bus Arbitration Mode . . . 15-30
15.11.3.2 Sole Master Arbitration Mode . . . 15-30
15.11.3.3 Arbiter Mode Arbitration Mode . . . 15-30
15.11.3.4 “Participant Mode” Arbitration Mode . . . 15-35
15.11.4 Switching Arbitration Modes . . . 15-38
15.11.4.1 Exiting No Bus Mode . . . 15-38
15.11.4.2 Exiting Sole Master Mode . . . 15-38
15.11.4.3 Exiting Arbiter Mode . . . 15-38
15.11.4.4 Exiting Participant Mode . . . 15-39
15.11.5 Arbitration Input Signal Sampling . . . 15-39
15.11.6 Locking the External Bus . . . 15-39
15.11.7 Interaction with Debug System . . . 15-40
15.11.8 Arbitrating SDRAM control signals . . . 15-40
15.12 Start-Up/Boot Process . . . 15-41

15.12.1 Disabled (arbitration mode is “nobus”) 15-41
15.12.2 External Boot Mode 15-41
15.12.2.1 Configuration Word Fetch Process 15-42
15.12.2.2 Boot Configuration Value 15-44
15.13 Accessing the External Bus 15-45
15.13.1 External Memory Regions 15-45
15.13.2 Address Comparison 15-48
15.13.2.1 Operation Address Comparison 15-48
15.13.3 SRI Bus Width Translation 15-51
15.13.4 Address Alignment During Bus Accesses 15-52
15.13.5 SRI Data Buffering 15-52
15.13.6 Chip Select Control 15-53
15.13.7 Combined Chip Select (CSCOMB) 15-53
15.14 Connecting External Memories 15-53
15.14.1 Programmable Device Types 15-54
15.14.2 Support for Multiplexed Device Configurations 15-55
15.14.2.1 Twin 16-bit Multiplexed Device Configuration 15-56
15.14.2.2 16-bit Multiplexed Memory/Peripheral Configuration 15-57
15.14.2.3 8-bit Multiplexed Memory/Peripheral Configuration 15-58
15.14.2.4 32-bit Multiplexed Memory/Peripheral Configuration 15-58
15.14.3 Support for Non-Multiplexed Device Configurations 15-59
15.14.3.1 16-bit non-Multiplexed Memory/Peripheral Configuration 15-60
15.14.3.2 8-bit non-Multiplexed Memory/Peripheral Configuration 15-60
15.14.3.3 32-bit non-Multiplexed Memory/Peripheral Configuration 15-61
15.14.3.4 Twin, 16-bit non-Multiplexed Memory/Peripheral Configuration . 15-61
15.15 Phases for Asynchronous and Synchronous Accesses 15-62
15.15.1 Address Phase (AP) 15-63
15.15.2 Address Hold Phase (AH) 15-64
15.15.3 Command Delay Phase (CD) 15-64
15.15.4 Command Phase (CP) 15-64
15.15.5 Data Hold Phase (DH) 15-65
15.15.5.1 Exceptional use of Data Hold 15-65
15.15.6 Burst Phase (BP) 15-65
15.15.7 Control Hold (CH) 15-66
15.15.8 Recovery Phase (RP) 15-67
15.16 Asynchronous Read/Write Accesses 15-69
15.16.1 Signal List 15-69
15.16.2 Standard Asynchronous Access Phases 15-70
15.16.3 Example Waveforms 15-70
15.16.4 Control of $\overline{\text{ADV}}$ & Other Signal Delays During Asynchronous Accesses 15-73
15.16.5 Programmable Parameters 15-74
15.16.6 Asynchronous Access Control 15-75

15.16.6.1 External Extension of the Command Phase by WAIT 15-76
15.16.7 Interaction with DDR Signal Timing 15-80
15.16.8 Interfacing to Asynchronous Nand Flash Devices 15-80
15.16.8.1 NAND flash page mode 15-81
15.17 Synchronous Read/Write Accesses 15-85
15.17.1 Signals 15-86
15.17.2 Support for four Burst FLASH device types 15-86
15.17.3 Typical Burst Flash Connection 15-87
15.17.4 Standard Access Phases 15-88
15.17.5 Example Waveforms 15-88
15.17.6 Burst Length Control 15-91
15.17.7 Burst Flash Clock 15-91
15.17.8 Control of ADV & Control Signal Delays During Synchronous Accesses 15-92
15.17.9 Interaction with DDR Signal Timing 15-95
15.17.10 Burst Flash Clock Feedback 15-96
15.17.11 Asynchronous Address Phase 15-96
15.17.12 Critical Word First Read Accesses 15-96
15.17.13 Example Burst Flash Access Cycle 15-97
15.17.14 External Cycle Control via the WAIT Input 15-99
15.17.15 Flash Non-Array Access Support 15-101
15.17.16 Termination of a Burst Access 15-101
15.17.17 Burst Flash Device Programming Sequences 15-101
15.17.18 Cellular RAM 15-102
15.17.18.1 Synchronous Write Access 15-102
15.17.18.2 Fujitsu FCRAM Support (burst write with WR active during data phase) 15-104
15.17.19 DDR Burst Flash Support 15-104
15.17.19.1 DDR NOR Burst Flash 15-105
15.17.19.2 ONFI 2.0 NAND Flash 15-108
15.17.20 Programmable Parameters 15-111
15.18 SDRAM Interface 15-113
15.18.1 Features 15-113
15.18.2 Signal List 15-114
15.18.3 External Interface 15-115
15.18.4 SDRAM External Bus Clock Generation 15-117
15.18.5 SDRAM Characteristics 15-118
15.18.6 Supported SDRAM commands 15-119
15.18.7 SDRAM device size 15-120
15.18.8 Power Up Sequence 15-121
15.18.9 Initialization sequence 15-121
15.18.9.1 Cold Start Initialisation 15-121
15.18.9.2 Warm Start Initialisation 15-123

15.18.10 Mobile SDRAM Support 15-124
15.18.11 Burst Accesses 15-124
15.18.12 Short Burst Accesses and Byte Writes 15-125
15.18.13 SDRAM Addressing Scheme 15-125
15.18.14 Bank Address Multiplexing 15-126
15.18.15 Column Address Multiplexing 15-127
15.18.16 Row Address Multiplexing 15-128
15.18.17 Supported SDRAM Configurations 15-129
15.18.18 SDRAM Bank Management 15-131
15.18.18.1 Decisions over “row hit” 15-132
15.18.19 Banks Precharge 15-132
15.18.20 Refresh Cycles 15-133
15.18.21 Self-Refresh Mode 15-133
15.18.22 Power Down Mode 15-134
15.18.23 SDRAM Recovery Phases 15-135
15.18.23.1 Recovery after SDRAM Command 15-136
15.18.23.2 Write Recovery Time (T_{WRC}) 15-136
15.18.24 Status Register Definition 15-136
15.18.24.1 Refresh Error (REFERR) 15-136
15.18.24.2 SDRAM Controller Busy (SDRMBUSY) 15-137
15.18.24.3 SDRAM Read Error (SDERR) 15-137
15.18.24.4 DLL Drift Detected (DRIFT_WARN) 15-137
15.18.25 Programmable Parameters 15-137
15.19 DDRAM/Mobile DDRAM Support 15-140
15.19.1 DDR Mode Address Outputs 15-142
15.19.2 DDRAM Initialization sequence 15-142
15.19.2.1 Cold Start Initialisation 15-143
15.19.2.2 Warm Start Initialisation 15-143
15.19.3 DDR External Bus Clock Generation 15-144
15.20 LPDDR NVM Flash Support (JEDEC 42.4 LPDDR-NVM Protocol) . 15-144
15.20.1 Overview 15-144
15.20.2 Implementation Requirements 15-145
15.20.3 Initialisation 15-145
15.20.4 Additional Supported Commands 15-146
15.20.5 Normal operating mode 15-146
15.20.6 Status Register Reads 15-148
15.20.7 Discrete Mode Register Writes 15-149
15.20.8 Page Preload 15-149
15.20.9 Page Tag Control 15-150
15.20.10 Overlay Window Control 15-150
15.20.11 Clearing The Read FIFO error flag 15-151
15.20.12 LPDDR-NVM Access Programmable Parameters 15-151
15.21 EBU Registers 15-153

15.21.1 Clock Control Register, CLC 15-156
15.21.2 Configuration Register, MODCON 15-158
15.21.3 External Boot Configuration Control Register, EXTBOOT 15-161
15.21.4 Address Select Register, ADDRSELx 15-163
15.21.5 Bus Configuration Register, BUSRCONx 15-165
15.21.6 Bus Write Configuration Register, BUSWCONx 15-169
15.21.7 Bus Read Access Parameter Register, BUSRAPx 15-172
15.21.8 Bus Write Access Parameter Register, BUSWAPx 15-175
15.21.9 SDRAM Control Register, SDRMCON 15-178
15.21.10 SDRAM Mode Register, SDRMOD 15-180
15.21.11 SDRAM Refresh Control Register, SDRMREF 15-183
15.21.12 SDRAM Status Register, SDRSTAT 15-185
15.21.13 DLL Control Register, EBU_DLLCON 15-187
15.21.14 LPDDR NVM Configuration Register, DDRNCON 15-190
15.21.15 LPDDR NVM Mode Register, DDRNMOD 15-192
15.21.16 LPDDR NVM Extended Mode Register, DDRNMOD2 15-194
15.21.17 LPDDR NVM Status Register, DDRNSRR 15-196
15.21.18 DDR Preload Register, DDRNPRLD 15-197
15.21.19 DDR Tag Register, DDRNTAGx 15-198
15.21.20 Test/Control Configuration Register, USERCON 15-199
15.22 Registers for SFR Extraction 15-200

16 Interrupt System 16-1
16.1 Overview 16-1
16.2 Service Request Nodes 16-3
16.2.1 Service Request Control Registers 16-3
16.2.1.1 General Service Request Control Register Format 16-3
16.2.1.2 Request Set and Clear Bits (SETR, CLRR) 16-5
16.2.1.3 Enable Bit (SRE) 16-5
16.2.1.4 Service Request Flag (SRR) 16-5
16.2.1.5 Type-Of-Service Control (TOS) 16-6
16.2.1.6 Service Request Priority Number (SRPN) 16-6
16.3 Interrupt Control Units 16-8
16.3.1 Interrupt Control Unit (ICU) 16-8
16.3.1.1 ICU Interrupt Control Register (ICR) 16-8
16.3.1.2 Operation of the Interrupt Control Unit (ICU) 16-10
16.3.2 PCP Interrupt Control Unit (PICU) 16-11
16.4 Arbitration Process 16-12
16.4.1 Controlling the Number of Arbitration Cycles 16-12
16.4.2 Controlling the Duration of Arbitration Cycles 16-13
16.5 Entering an Interrupt Service Routine 16-13
16.6 Exiting an Interrupt Service Routine 16-14
16.7 Interrupt Vector Table 16-15

16.8 Usage of the TC1798 Interrupt System 16-18
16.8.1 Spanning Interrupt Service Routines Across Vector Entries 16-18
16.8.2 Configuring Ordinary Interrupt Service Routines 16-19
16.8.3 Interrupt Priority Groups 16-19
16.8.4 Splitting Interrupt Service Across Different Priority Levels 16-20
16.8.5 Using different Priorities for the same Interrupt Source 16-21
16.8.6 Interrupt Priority 1 16-22
16.8.7 Software-Initiated Interrupts 16-22
16.8.8 External Interrupts 16-22
16.9 Service Request Node Table 16-23

17 System Timer (STM) 17-1
17.1 Overview 17-1
17.2 Operation 17-1
17.2.1 Resolution and Ranges 17-4
17.2.2 Compare Register Operation 17-5
17.2.3 Compare Match Interrupt Control 17-6
17.3 STM Registers 17-7
17.3.1 Clock Control Register 17-9
17.3.2 Timer/Capture Registers 17-11
17.3.3 Compare Registers 17-14
17.3.4 Interrupt Registers 17-17
17.4 STM Module Implementation 17-21
17.4.1 On-chip Service Request Connections 17-21
17.4.2 STM Address Map 17-21

18 Bus Monitor Unit (BMU) 18-1
18.1 Related documentation 18-2
18.2 BMU Features 18-3
18.3 Operational overview 18-4
18.3.1 Microcontroller Monitoring Framework 18-4
18.3.2 Bus Monitor Unit Overview 18-6
18.4 BMU Functional Description 18-8
18.4.1 BMU Microarchitecture 18-8
18.4.2 Handling of FPI corner cases 18-11
18.4.3 Bus Transaction Table 18-12
18.4.4 Write Operation and Fifo Structure 18-14
18.4.5 Read Operation and Fifo Structure 18-15
18.4.6 Fullness Monitoring 18-16
18.4.7 Error Correction Code (ECC) 18-18
18.4.8 Usage in non safety applications 18-20
18.4.9 BMU interrupts 18-21
18.4.10 Peripheral Monitoring Selection 18-22
18.5 Interfaces of the BMU Module 18-25

18.6 BMU Module Registers 18-27
18.6.1 System Registers description 18-30
18.6.2 BMU Control/Status Registers 18-33
18.6.3 BMU: Bus Logging Configuration Registers 18-36
18.6.4 BMU: Fifo Monitoring Registers 18-43
18.6.5 BMU: SIST Mode Access Control Register 18-46
18.6.6 Interrupt System Registers 18-49

19 On-Chip Debug Support (OCDS) 19-1
19.1 Overview 19-1
19.2 OCDS Level 1 19-5
19.2.1 TriCore CPU OCDS Level 1 19-6
19.2.1.1 Basic Concept 19-6
19.2.1.2 Debug Event Generation 19-7
19.2.1.3 Debug Actions 19-8
19.2.1.4 TriCore OCDS Registers 19-8
19.2.2 PCP OCDS Level 1 19-9
19.2.3 SBCU OCDS Level 1 19-9
19.2.4 DMA/SDMA OCDS Level 1 19-9
19.3 Debug Interface (Cerberus) 19-10
19.3.1 RW Mode 19-10
19.3.2 Communication Mode 19-11
19.3.3 Triggered Transfers 19-11
19.3.4 Multi Core Break Switch 19-11
19.4 JTAG Interface 19-13
19.5 Device Access Port (DAP) 19-13
19.5.1 DAP Telegram Format 19-13
19.5.2 DAP Telegram Catalog 19-13
19.6 Cerberus and JTAG Registers 19-14

20 Asynchronous/Synchronous Serial Interface (ASC) 20-1
20.1 ASC Kernel Description 20-1
20.1.1 Overview 20-2
20.1.2 General Operation 20-3
20.1.3 Asynchronous Operation 20-4
20.1.3.1 Asynchronous Data Frames 20-5
20.1.3.2 Asynchronous Transmission 20-7
20.1.3.3 Asynchronous Reception 20-7
20.1.3.4 RXD/TXD Data Path Selection in Asynchronous Modes 20-8
20.1.4 Synchronous Operation 20-9
20.1.4.1 Synchronous Transmission 20-10
20.1.4.2 Synchronous Reception 20-10
20.1.4.3 Synchronous Timing 20-11
20.1.5 Baud Rate Generation 20-12

20.1.5.1 Baud Rates in Asynchronous Mode 20-13
20.1.5.2 Baud Rates in Synchronous Mode 20-16
20.1.6 Hardware Error Detection Capabilities 20-17
20.1.7 Interrupts 20-17
20.2 ASC Kernel Registers 20-19
20.2.1 Control Registers 20-20
20.2.2 Data Registers 20-28
20.3 ASC0/ASC1 Module Implementation 20-30
20.3.1 Interfaces of the ASC Modules 20-30
20.3.2 ASC0/ASC1 Module Related External Registers 20-32
20.3.2.1 Clock Control Register 20-33
20.3.2.2 Peripheral Input Select Register 20-35
20.3.2.3 Port Control Registers 20-37
20.3.2.4 Interrupt Control Registers 20-39
20.3.3 DMA Requests 20-40
20.3.4 Address Map 20-42
20.3.5 Application Hint Regarding the ATM Feature 20-44

21 Synchronous Serial Interface (SSC) 21-1
21.1 SSC Kernel Description 21-1
21.1.1 Overview 21-2
21.1.2 General Operation 21-3
21.1.2.1 Operating Mode Selection 21-5
21.1.2.2 Full-Duplex Operation 21-6
21.1.2.3 Half-Duplex Operation 21-9
21.1.2.4 Continuous Transfers 21-10
21.1.2.5 Parity Mode 21-11
21.1.2.6 Port Control 21-12
21.1.2.7 Baud Rate Generation 21-14
21.1.2.8 Slave Select Input Operation 21-16
21.1.2.9 Slave Select Output Generation Unit 21-17
21.1.2.10 Error Detection Mechanisms 21-20
21.1.2.11 Queued SSC Mode 21-24
21.2 SSC Kernel Registers 21-27
21.2.1 Module Identification Register 21-28
21.2.2 Control Registers 21-29
21.2.3 Data Registers 21-42
21.3 SSC0/SSC1/SSC2/SSC3 Module Implementation 21-43
21.3.1 Module Identification Registers 21-43
21.3.2 Interfaces of the SSC Modules 21-43
21.3.3 On-Chip Connections 21-46
21.3.4 SSC0/SSC1/SSC2/SSC3 Module Related External Registers 21-46
21.3.4.1 Clock Control 21-48

21.3.4.2 Port Control 21-53
21.3.4.3 Interrupt Control Registers 21-58
21.3.5 Address Map of the SSC Modules 21-59

22 Synchronous Serial Interface Guardian (SSCG) 22-1
22.1 Overview 22-1
22.1.1 General Operation 22-2
22.2 SSCG Kernel Description 22-3
22.2.1 Details on the Operation Principles and the Architecture 22-3
22.2.1.1 Monitoring the Slave Select and Serial Clock Signals 22-6
22.3 SSCG Kernel Registers, inherited from SSC 22-8
22.3.1 Module Identification Register 22-10
22.3.2 Control Registers 22-11
22.3.3 Data Registers 22-24
22.3.4 SSCG Specific Registers 22-25
22.4 SSCG0 Module Implementation 22-30
22.4.1 Module Identification Registers 22-30
22.4.2 Interfaces of the SSCG Modules 22-30
22.4.3 On-Chip Connections 22-32
22.4.3.1 Receive Input Selection 22-32
22.4.4 SSC0/SSC1 Module Related External Registers 22-33
22.4.4.1 Clock Control 22-34
22.4.4.2 Interrupt Control Registers 22-39
22.4.5 SSCG Address Map 22-40

23 Micro Second Channel (MSC) 23-1
23.1 MSC Kernel Description 23-3
23.1.1 Overview 23-3
23.1.2 Downstream Channel 23-5
23.1.2.1 Frame Formats and Definitions 23-6
23.1.2.2 Shift Register Operation 23-12
23.1.2.3 Transmission Modes 23-14
23.1.2.4 Downstream Counter and Enable Signals 23-19
23.1.2.5 Baud Rate 23-20
23.1.2.6 Abort of Frames 23-20
23.1.3 Upstream Channel 23-21
23.1.3.1 Data Frames 23-22
23.1.3.2 Parity Checking 23-22
23.1.3.3 Data Reception 23-23
23.1.3.4 Baud Rate 23-25
23.1.3.5 Spike Filter 23-26
23.1.4 I/O Control 23-27
23.1.4.1 Downstream Channel Output Control 23-27
23.1.4.2 Upstream Channel 23-30

23.1.5 MSC Interrupts . . . 23-31
23.1.5.1 Data Frame Interrupt . . . 23-32
23.1.5.2 Command Frame Interrupt . . . 23-32
23.1.5.3 Time Frame Finished Interrupt . . . 23-33
23.1.5.4 Receive Data Interrupt . . . 23-34
23.1.5.5 Interrupt Request Compressor . . . 23-35
23.2 MSC Kernel Registers . . . 23-36
23.2.1 Module Identification Register . . . 23-38
23.2.2 Status and Control Registers . . . 23-39
23.2.3 Data Registers . . . 23-59
23.3 MSC Module Implementation . . . 23-62
23.3.1 Interface Connections of the MSC Modules . . . 23-62
23.3.2 MSC0/MSC1 Module-Related External Registers . . . 23-64
23.3.3 Clock Control . . . 23-65
23.3.3.1 Clock Control Register . . . 23-67
23.3.3.2 Fractional Divider Register . . . 23-68
23.3.4 Port Control . . . 23-69
23.3.4.1 Input/Output Function Selection . . . 23-69
23.3.5 On-Chip Connections . . . 23-72
23.3.5.1 EMGSTOPMSC Signal (from SCU) . . . 23-72
23.3.5.2 ALTINH and ALTINL Connections . . . 23-72
23.3.5.3 DMA Controller Service Requests . . . 23-73
23.3.6 Interrupt Control Registers . . . 23-74
23.3.7 MSC0/MSC1 Address Map . . . 23-75

24 Controller Area Network Controller (MultiCAN) . . . 24-1
24.1 CAN Basics . . . 24-2
24.1.1 Addressing and Bus Arbitration . . . 24-2
24.1.2 CAN Frame Formats . . . 24-3
24.1.2.1 Data Frames . . . 24-3
24.1.2.2 Remote Frames . . . 24-5
24.1.2.3 Error Frames . . . 24-7
24.1.3 The Nominal Bit Time . . . 24-8
24.1.4 Error Detection and Error Handling . . . 24-9
24.2 TTCAN Basics . . . 24-11
24.2.1 Time Reference . . . 24-11
24.2.2 Basic Cycle . . . 24-11
24.2.3 Global System Time . . . 24-12
24.2.4 The System Matrix . . . 24-12
24.2.5 Generation of the Network Time Unit (NTU) . . . 24-13
24.2.6 Global Time Generation and Drift Correction . . . 24-13
24.3 Overview . . . 24-14
24.3.1 MultiCAN Module . . . 24-15

24.4 Time-Triggered Extension (TTCAN) 24-17
24.5 MultiCAN Kernel Functional Description 24-18
24.5.1 Module Structure 24-18
24.5.2 Clock Control 24-21
24.5.3 Port Input Control 24-23
24.5.4 Suspend Mode 24-23
24.5.5 CAN Node Control 24-25
24.5.5.1 Bit Timing Unit 24-26
24.5.5.2 Bitstream Processor 24-27
24.5.5.3 Error Handling Unit 24-28
24.5.5.4 CAN Frame Counter 24-29
24.5.5.5 CAN Node Interrupts 24-29
24.5.6 Message Object List Structure 24-31
24.5.6.1 Basics 24-31
24.5.6.2 List of Unallocated Elements 24-32
24.5.6.3 Connection to the CAN Nodes 24-32
24.5.6.4 List Command Panel 24-33
24.5.7 CAN Node Analysis Features 24-36
24.5.7.1 Analyze Mode 24-36
24.5.7.2 Loop-Back Mode 24-36
24.5.7.3 Bit Timing Analysis 24-37
24.5.8 Message Acceptance Filtering 24-39
24.5.8.1 Receive Acceptance Filtering 24-39
24.5.8.2 Transmit Acceptance Filtering 24-40
24.5.9 Message Postprocessing 24-42
24.5.9.1 Message Object Interrupts 24-42
24.5.9.2 Pending Messages 24-44
24.5.10 Message Object Data Handling 24-46
24.5.10.1 Frame Reception 24-46
24.5.10.2 Frame Transmission 24-49
24.5.11 Message Object Functionality 24-52
24.5.11.1 Standard Message Object 24-52
24.5.11.2 Single Data Transfer Mode 24-52
24.5.11.3 Single Transmit Trial 24-52
24.5.11.4 Message Object FIFO Structure 24-53
24.5.11.5 Receive FIFO 24-55
24.5.11.6 Transmit FIFO 24-56
24.5.11.7 Gateway Mode 24-57
24.5.11.8 Foreign Remote Requests 24-59
24.6 MultiCAN Kernel Registers 24-60
24.6.1 Global Module Registers 24-63
24.6.2 CAN Node Registers 24-76
24.6.3 Message Object Registers 24-94

24.7 Time-Triggered Extension (TTCAN Controller) 24-117
24.7.1 Generation of the Local Time 24-117
24.7.2 Automatic TUR Adjust 24-118
24.7.3 Cycle Time 24-118
24.7.3.1 Local Time and Synchronization Marks 24-118
24.7.3.2 Time Marks 24-119
24.7.3.3 Watch Trigger 24-120
24.7.4 Master Reference Mark (Level 2 only) 24-120
24.7.5 Transmit Enable Window 24-120
24.7.6 Local Offset and Global Time 24-121
24.7.7 Transmit Trigger 24-122
24.7.8 Reference Message 24-123
24.7.8.1 Differences to Normal CAN Messages 24-123
24.7.8.2 Transmit Trigger for a Reference Message 24-124
24.8 TTCAN Scheduler 24-126
24.8.1 Overview 24-126
24.8.2 Scheduler Memory 24-127
24.8.2.1 Scheduler Entry Types 24-128
24.8.2.2 Scheduler Entry Type Description 24-129
24.8.2.3 End of Scheduler Memory Entry 24-144
24.8.3 Setup of the Scheduler Entries 24-145
24.8.4 Reading the Scheduler Entries 24-145
24.8.4.1 Instructions During a Basic Cycle 24-145
24.8.4.2 Instructions at the End of a Basic Cycle 24-146
24.8.5 Scheduler Instruction Sequence 24-148
24.8.5.1 BCC and CSM 24-148
24.8.5.2 General Instruction Sequence Rules 24-149
24.8.5.3 Scheduler Sequence Example 24-150
24.9 TTCAN Operation 24-151
24.9.1 Configuration 24-151
24.9.2 Configuration Error 24-151
24.9.3 Synchronization Phase 24-152
24.9.4 Time Masters 24-152
24.9.4.1 State of a Time Master 24-152
24.9.4.2 Strictly Time-Triggered Behavior 24-152
24.9.5 Error Handling 24-153
24.9.6 Application Watchdog 24-153
24.9.7 MSC Handling 24-154
24.9.8 TTCAN Interrupt Control 24-155
24.10 TTCAN Registers 24-157
24.10.1 TTCAN Timing Registers 24-160
24.10.2 TTCAN Control / Status / Configuration Registers 24-172
24.10.3 Scheduler Registers 24-195

24.11 MultiCAN Module Implementation 24-202
24.11.1 Interfaces of the MultiCAN Module 24-202
24.11.2 MultiCAN Module External Registers 24-203
24.11.3 Module Clock Generation 24-204
24.11.3.1 CAN Clock Control Register 24-205
24.11.4 Port and I/O Line Control 24-208
24.11.4.1 Input/Output Function Selection in Ports 24-208
24.11.4.2 Node Receive Input Selection 24-208
24.11.4.3 External CAN Time Trigger Inputs 24-209
24.11.4.4 DMA Request Outputs 24-209
24.11.4.5 Connectons to GPTA0 Inputs 24-210
24.11.5 Interrupt Control 24-211
24.11.5.1 CAN Service Request Control Register 24-213
24.11.6 MultiCAN Module Register Address Map 24-214

25 Single Edge Nibble Transmission (SENT) 25-1
25.1 SENT Kernel Description 25-1
25.1.1 Overview 25-2
25.1.2 General Operation 25-4
25.1.2.1 Definitions 25-5
25.1.3 Standard SENT Operation 25-6
25.1.3.1 Frame Formats and Definitions 25-7
25.1.4 SPC Operation 25-12
25.1.4.1 Synchronous Transmission 25-12
25.1.4.2 Range Selection 25-12
25.1.4.3 ID Selection 25-13
25.1.4.4 Bidirectional Transmit Mode 25-14
25.1.4.5 SPC Timing 25-14
25.1.4.6 Abort of Frames 25-15
25.1.5 Baud Rate Generation 25-16
25.1.6 Error Detection Capabilities 25-18
25.1.7 Digital Glitch Filter. 25-19
25.1.8 Interrupts 25-20
25.1.9 Trigger Outputs 25-21
25.2 SENT Kernel Registers 25-22
25.2.1 Module Control 25-25
25.2.2 Channel Baud Rate Registers 25-29
25.2.3 Receiver Control and Status Registers 25-31
25.2.4 Input and Output Control 25-39
25.2.5 Receive Data Registers 25-42
25.2.6 SPC Control 25-45
25.2.7 Interrupt Control Registers 25-48
25.3 SENT Module Implementation 25-64

25.3.1 Interface Connections of the SENT Module 25-64
25.3.2 On-Chip Connections 25-65
25.3.2.1 Interrupt and DMA Controller Service Requests 25-65
25.3.2.2 Trigger Inputs 25-66
25.3.3 SENT Module-Related External Registers 25-67
25.3.3.1 Port Control 25-67
25.3.3.2 Service Request Control Registers 25-71
25.3.4 SENT Register Address Map 25-73
25.4 Revision History 25-74

26 FlexRay™ Protocol Controller (E-Ray) 26-1
26.1 E-Ray Kernel Description 26-1
26.2 Overview 26-2
26.3 Definitions 26-3
26.4 Block Diagram 26-3
26.5 Programmer's Model 26-6
26.5.1 Register Map 26-6
26.5.2 E-Ray Kernel Registers 26-8
26.5.2.1 Customer Registers 26-16
26.5.2.2 Special Registers 26-23
26.5.2.3 Service Request Registers 26-41
26.5.2.4 Communication Controller Control Registers 26-88
26.5.2.5 Communication Controller Status Registers 26-115
26.5.2.6 Message Buffer Control Registers 26-138
26.5.2.7 Message Buffer Status Registers 26-145
26.5.2.8 Identification Registers 26-166
26.5.2.9 Input Buffer 26-168
26.5.2.10 Output Buffer 26-179
26.6 Functional Description 26-196
26.6.1 Communication Cycle 26-196
26.6.1.1 Static Segment 26-196
26.6.1.2 Dynamic Segment 26-197
26.6.1.3 Symbol Window 26-197
26.6.1.4 Network Idle Time (NIT) 26-197
26.6.1.5 Configuration of Network Idle Time (NIT) Start and Offset Correction Start. 26-197
26.6.2 Communication Modes 26-199
26.6.3 Clock Synchronization 26-199
26.6.3.1 Global Time 26-199
26.6.3.2 Local Time 26-199
26.6.3.3 Synchronization Process 26-200
26.6.3.4 External Clock Synchronization 26-201
26.6.4 Error Handling 26-202

26.6.4.1 Clock Correction Failed Counter 26-202
26.6.4.2 Passive to Active Counter 26-203
26.6.4.3 HALT Command 26-203
26.6.4.4 FREEZE Command 26-203
26.6.5 Communication Controller States 26-205
26.6.5.1 Communication Controller State Diagram 26-205
26.6.5.2 DEFAULT_CONFIG State 26-207
26.6.5.3 MONITOR_MODE 26-208
26.6.5.4 READY State 26-209
26.6.5.5 WAKEUP State 26-209
26.6.5.6 STARTUP State 26-214
26.6.5.7 Startup Time-outs 26-217
26.6.5.8 Path of leading Coldstart Node (initiating coldstart) 26-218
26.6.5.9 NORMAL_ACTIVE State 26-220
26.6.5.10 NORMAL_PASSIVE State 26-220
26.6.5.11 HALT State 26-221
26.6.6 Network Management 26-222
26.6.7 Filtering and Masking 26-222
26.6.7.1 Frame ID Filtering 26-223
26.6.7.2 Channel ID Filtering 26-223
26.6.7.3 Cycle Counter Filtering 26-224
26.6.7.4 FIFO Filtering 26-225
26.6.8 Transmit Process 26-226
26.6.8.1 Static Segment 26-226
26.6.8.2 Dynamic Segment 26-226
26.6.8.3 Transmit Buffers 26-226
26.6.8.4 Frame Transmission 26-227
26.6.8.5 NULL Frame Transmission 26-228
26.6.9 Receive Process 26-229
26.6.9.1 Frame Reception 26-229
26.6.9.2 NULL Frame reception 26-230
26.6.10 FIFO Function 26-230
26.6.10.1 Description 26-230
26.6.10.2 Configuration of the FIFO 26-231
26.6.10.3 Access to the FIFO 26-232
26.6.11 Message Handling 26-232
26.6.11.1 Host access to Message RAM 26-232
26.6.11.2 Data Transfers between IBF / OBF and Message RAM 26-237
26.6.11.3 Minimum f_{CLC_ERAY} 26-243
26.6.11.4 FlexRay™ Protocol Controller access to Message RAM 26-247
26.6.12 Message RAM 26-248
26.6.12.1 Header Partition 26-250
26.6.12.2 Data Partition 26-253

26.6.12.3 ECC Check 26-254
26.6.13 Host Handling of Errors 26-257
26.6.13.1 Self-Healing 26-257
26.6.13.2 CLEAR_RAMS Command 26-257
26.6.13.3 Temporary Unlocking of Header Section 26-257
26.7 Module Service Request 26-259
26.8 Restrictions 26-262
26.8.1 Message Buffers with the same Frame ID 26-262
26.8.2 Data Transfers between IBF / OBF and Message RAM 26-262
26.9 E-Ray Module Implementation 26-263
26.9.1 Interconnections of the E-Ray Module 26-263
26.9.2 Port Control and Connections 26-264
26.9.2.1 Input/Output Function Selection 26-264
26.9.3 On-Chip Connections 26-266
26.9.3.1 E-Ray Connections with DMA 26-266
26.9.3.2 E-Ray Connections with the External Request Unit of SCU . . . 26-267
26.9.3.3 E-Ray Connections with the ECC Error Handling Unit of SCU . 26-267
26.9.3.4 E-Ray Connections with the External Clock Output of SCU . . . 26-267
26.9.4 Clock Control Register 26-268
26.9.5 Interrupt Registers 26-269

27 Micro Link Interface (MLI) 27-1
27.1 Functional Description 27-2
27.1.1 General Introduction 27-2
27.1.1.1 MLI Overview 27-2
27.1.1.2 Naming Conventions 27-4
27.1.1.3 MLI Communication Principles 27-6
27.1.2 MLI Frame Structure 27-10
27.1.2.1 General Frame Layout 27-11
27.1.2.2 Copy Base Address Frame 27-12
27.1.2.3 Write Offset and Data Frame 27-13
27.1.2.4 Optimized Write Frame 27-14
27.1.2.5 Discrete Read Frame 27-15
27.1.2.6 Optimized Read Frame 27-16
27.1.2.7 Command Frame 27-17
27.1.2.8 Answer Frame 27-18
27.1.3 Handshake Description 27-19
27.1.3.1 Handshake Signals 27-21
27.1.3.2 Error-free Handshake 27-21
27.1.3.3 Ready Delay Time 27-22
27.1.3.4 Non-Acknowledge Error 27-23
27.1.3.5 Signal Timing 27-24
27.1.4 Parity Generation 27-26

27.1.5 Address Prediction 27-26
27.2 Module Kernel Description 27-27
27.2.1 Frame Handling 27-27
27.2.1.1 Copy Base Address Frame 27-28
27.2.1.2 Write/Data Frames 27-30
27.2.1.3 Read Frames 27-34
27.2.1.4 Answer Frame 27-39
27.2.1.5 Command Frame 27-41
27.2.2 General MLI Features 27-44
27.2.2.1 Parity Check and Parity Error Indication 27-44
27.2.2.2 Non-Acknowledge Error 27-47
27.2.2.3 Address Prediction 27-47
27.2.2.4 Automatic Data Mode 27-48
27.2.2.5 Memory Access Protection 27-49
27.2.2.6 Triggered Command Transfers 27-49
27.2.2.7 Transmit Priority 27-50
27.2.2.8 Transmission Delay 27-50
27.2.3 Interface Description 27-51
27.2.3.1 Transmitter I/O Line Control 27-53
27.2.3.2 Receiver I/O Line Control 27-53
27.2.3.3 Connecting Several MLI Modules 27-55
27.2.4 MLI Service Request Generation 27-57
27.2.5 Transmitter Events 27-59
27.2.5.1 Parity/Time-out Error Event 27-60
27.2.5.2 Normal Frame Sent x Event 27-60
27.2.5.3 Command Frame Sent Events 27-61
27.2.6 Receiver Events 27-62
27.2.6.1 Discarded Read Answer Event 27-62
27.2.6.2 Memory Access Protection/Parity Error Event 27-63
27.2.6.3 Normal Frame Received/Move Engine Terminated Event 27-64
27.2.6.4 Interrupt Command Frame Event 27-65
27.2.6.5 Command Frame Received Event 27-66
27.2.7 Baud Rate Generation 27-67
27.2.8 Automatic Register Overwrite 27-68
27.3 Operating the MLI 27-69
27.3.1 Connection Setup 27-70
27.3.2 Local Transmitter and Pipe Setup 27-71
27.3.3 Remote Receiver Setup 27-71
27.3.4 Remote Transmitter and Local Receiver Setup 27-72
27.3.5 Delay Adjustment 27-73
27.3.6 Connection to DMA Mechanism 27-75
27.3.7 Connection of MLI to SPI 27-75
27.4 MLI Kernel Registers 27-77

27.4.1 General Module Registers 27-79
27.4.2 General Status/Control Registers 27-83
27.4.3 Access Protection Registers 27-90
27.4.4 Transmitter Control/Status Registers 27-92
27.4.5 Transmitter Pipe x Address Offset Register 27-103
27.4.6 Transmitter Interrupt Registers 27-107
27.4.7 Receiver Control/Status Registers 27-113
27.4.8 Receiver Address/Data Registers 27-117
27.4.9 Receiver Interrupt Registers 27-120
27.5 Implementation of the MLI0/MLI1 in TC1798 27-127
27.5.1 Interfaces of the MLI Modules 27-127
27.5.2 MLI Module External Registers 27-130
27.5.2.1 Automatic Register Overwrite 27-130
27.5.3 Module Clock Generation 27-131
27.5.4 Port Control and Connections 27-133
27.5.4.1 Input/Output Function Selection 27-133
27.5.5 On-Chip Connections 27-136
27.5.5.1 Service Request Output Connections 27-136
27.5.5.2 Break Signals 27-137
27.5.5.3 Trigger Input Signals 27-137
27.5.6 Access Protection 27-137
27.5.7 MLI0/MLI1 Transfer Window Address Maps 27-138
27.5.8 MLI0/MLI1 Address Map 27-139

28 General Purpose Timer Array (GPTA®v5) 28-1
28.1 What is new? 28-1
28.2 GPTA®v5 Overview 28-4
28.2.1 Functionality of GPTA0 and GPTA1 28-5
28.2.2 Functionality of LTCA2 28-7
28.3 GPTA0/GPTA1 Kernel Description 28-8
28.3.1 GTPA Units 28-9
28.3.2 Clock Generation Cells 28-10
28.3.2.1 Filter and Prescaler Cell (FPC) 28-12
28.3.2.2 Phase Discrimination Logic (PDL) 28-21
28.3.2.3 Duty Cycle Measurement Cell (DCM) 28-26
28.3.2.4 Digital Phase Locked Loop Cell (PLL) 28-30
28.3.2.5 Clock Distribution Cell (CDC) 28-35
28.3.3 Signal Generation Cells 28-38
28.3.3.1 Global Timers (GT) 28-38
28.3.3.2 Global Timer Cell (GTC) 28-55
28.3.3.3 Local Timer Cell (LTC00 to LTC62) 28-67
28.3.3.4 Local Timer Cell LTC63 28-79
28.3.3.5 Coherent Update 28-85

28.3.4 Input/Output Line Sharing Block (IOLS) 28-98
28.3.4.1 FPC Input Line Selection 28-102
28.3.4.2 GTC and LTC Output Multiplexer Selection 28-103
28.3.4.3 On-chip Trigger and Gating Output Multiplexer Selection 28-108
28.3.4.4 GTC Input Multiplexer Selection 28-111
28.3.4.5 LTC Input Multiplexer Selection 28-116
28.3.4.6 Multiplexer Register Array Programming 28-121
28.3.5 Interrupt Sharing Block (IS) 28-123
28.3.6 Pseudo Code Description of GPTA®v5 Kernel Functionality 28-126
28.3.6.1 FPC Algorithm 28-126
28.3.6.2 PDL-Algorithm 28-131
28.3.6.3 DCM-Algorithm 28-135
28.3.6.4 PLL-Algorithm 28-138
28.3.6.5 GT-Algorithm 28-140
28.3.6.6 GTC-Algorithm 28-141
28.3.6.7 LTC-Algorithm for Cells 0 to 62 28-146
28.3.6.8 LTC Algorithm for Cell 63 28-154
28.3.7 Programming of a GPTA®v5 Unit 28-158
28.4 GPTA0/1 Kernel Registers 28-160
28.4.1 GPTA®v5 Identification Register 28-166
28.4.2 FPC Registers 28-167
28.4.3 Phase Discriminator Registers 28-171
28.4.4 Duty Cycle Measurement Registers 28-173
28.4.5 Digital Phase Locked Loop Registers 28-177
28.4.6 Global Timer Registers 28-182
28.4.7 Clock Bus Register 28-185
28.4.8 Global Timer Cell Registers 28-187
28.4.9 Local Timer Cell Registers 28-192
28.4.10 Multiplexer Control Registers 28-207
28.4.11 Service Request Registers 28-223
28.5 LTCA Kernel Description 28-234
28.5.1 Local Timer Cell (LTC00 to LTC63) 28-235
28.5.2 Input/Output Line Sharing Block (IOLS) 28-235
28.5.2.1 Output Multiplexer 28-237
28.5.2.2 LTC Input Multiplexing Scheme 28-242
28.5.2.3 Multiplexer Register Array Programming 28-245
28.5.3 Interrupt Sharing Block (IS) 28-248
28.6 LTCA Kernel Registers 28-250
28.6.1 Bit Protection 28-251
28.6.2 Service Request Registers 28-252
28.6.3 Local Timer Cell Registers 28-252
28.6.4 I/O Sharing Block Registers 28-263
28.6.5 Multiplexer Control Registers 28-267

28.6.5.1 Output Multiplexer Control Registers 28-267
28.6.5.2 LTC Input Multiplexer Control Registers 28-270
28.7 GPTA®v5 Module Implementation 28-274
28.7.1 Interconnections of GPTA0/GPTA1/LTCA2 Units 28-274
28.7.2 GPTA®v5 Module External Registers 28-276
28.7.3 Port Control and Connections 28-276
28.7.3.1 I/O Port Line Assignment 28-276
28.7.3.2 Input/Output Function Selection 28-279
28.7.3.3 Emergency Control of GPTA®v5 Output Ports Lines 28-284
28.7.4 On-Chip Connections 28-286
28.7.4.1 Clock Bus Connections 28-286
28.7.4.2 MSC Controller Connections 28-287
28.7.4.3 Connections to SCU, MultiCAN, FADC, DMA, Ports 28-294
28.7.5 Module Clock Generation 28-296
28.7.5.1 Clock Control Registers 28-300
28.7.5.2 Fractional Divider Register 28-301
28.7.6 Limits of Cascading GTCs and LTCs 28-306
28.7.7 Interrupt Registers 28-307
28.7.8 GPTA Register Address Map 28-308
28.8 Revision History 28-311

29 Capture/Compare Unit 6 (CCU6) 29-1
29.1 Introduction 29-1
29.1.1 Feature Set Overview 29-2
29.1.2 Block Diagram 29-3
29.1.3 CCU6 Kernel Registers 29-4
29.2 Operating Timer T12 29-10
29.2.1 T12 Overview 29-11
29.2.2 T12 Counting Scheme 29-13
29.2.2.1 Clock Selection 29-13
29.2.2.2 Edge-Aligned / Center-Aligned Mode 29-14
29.2.2.3 Single-Shot Mode 29-16
29.2.3 T12 Compare Mode 29-17
29.2.3.1 Compare Channels 29-17
29.2.3.2 Channel State Bits 29-18
29.2.3.3 Hysteresis-Like Control Mode 29-23
29.2.4 Compare Mode Output Path 29-24
29.2.4.1 Dead-Time Generation 29-24
29.2.4.2 State Selection 29-26
29.2.4.3 Output Modulation and Level Selection 29-27
29.2.5 T12 Capture Modes 29-29
29.2.6 T12 Shadow Register Transfer 29-33
29.2.7 Timer T12 Operating Mode Selection 29-34

29.2.8 T12 related Registers 29-35
29.2.8.1 T12 Counter Register 29-35
29.2.8.2 Period Register 29-36
29.2.8.3 Capture/Compare Registers 29-37
29.2.8.4 Capture/Compare Shadow Registers 29-38
29.2.8.5 Dead-time Control Register 29-39
29.2.9 Capture/Compare Control Registers 29-41
29.2.9.1 Channel State Bits 29-41
29.2.9.2 T12 Mode Control Register 29-45
29.2.9.3 Timer Control Registers 29-46
29.3 Operating Timer T13 29-55
29.3.1 T13 Overview 29-55
29.3.2 T13 Counting Scheme 29-58
29.3.2.1 Clock Selection 29-58
29.3.2.2 T13 Counting 29-59
29.3.2.3 Single-Shot Mode 29-60
29.3.2.4 Synchronization to T12 29-61
29.3.3 T13 Compare Mode 29-63
29.3.4 Compare Mode Output Path 29-65
29.3.5 T13 Shadow Register Transfer 29-66
29.3.6 T13 related Registers 29-68
29.3.6.1 T13 Counter Register 29-68
29.3.6.2 Period Register 29-69
29.3.6.3 Compare Register 29-70
29.3.6.4 Compare Shadow Register 29-71
29.4 Synchronous Start Feature 29-72
29.5 Trap Handling 29-73
29.6 Multi-Channel Mode 29-75
29.7 Hall Sensor Mode 29-77
29.7.1 Hall Pattern Evaluation 29-78
29.7.2 Hall Pattern Compare Logic 29-80
29.7.3 Hall Mode Flags 29-81
29.7.4 Hall Mode for Brushless DC-Motor Control 29-83
29.8 Modulation Control Registers 29-85
29.8.1 Modulation Control 29-85
29.8.2 Trap Control Register 29-87
29.8.3 Passive State Level Register 29-90
29.8.4 Multi-Channel Mode Registers 29-91
29.9 Interrupt Handling 29-98
29.9.1 Interrupt Structure 29-98
29.9.2 Interrupt Registers 29-100
29.9.2.1 Interrupt Status Register 29-100
29.9.2.2 Interrupt Status Set Register 29-103

29.9.2.3 Status Reset Register 29-105
29.9.2.4 Interrupt Enable Register 29-107
29.9.2.5 Interrupt Node Pointer Register 29-109
29.9.3 Service Request Control Registers 29-112
29.10 General Module Operation 29-113
29.10.1 Mode Control 29-113
29.10.2 Input Selection 29-116
29.10.3 Input Monitoring 29-117
29.10.4 General Registers 29-118
29.10.4.1 ID Register 29-118
29.10.4.2 Port Input Select Registers 29-119
29.10.4.3 Kernel State Configuration Register 29-124
29.10.4.4 Kernel State Sensitivity Control Register 29-127
29.10.4.5 Module Configuration Register 29-128
29.10.4.6 Input Monitoring Register 29-130
29.10.4.7 Lost Indicator Register 29-133
29.11 Implementation 29-135
29.11.1 Address Map 29-135
29.11.1.1 Module Registers 29-136
29.11.2 Module Output Select 29-140
29.11.3 Synchronous Start 29-141
29.12 Digital Connections 29-142
29.12.1 Connections of CCU60 29-142
29.12.2 Connections of CCU61 29-146
29.12.3 Connections of CCU62 29-150
29.12.4 Connections of CCU63 29-154

30 The General Purpose Timer 12 (GPT12) 30-1
30.1 Timer Block GPT1 30-2
30.1.1 GPT1 Core Timer T3 Control 30-4
30.1.2 GPT1 Core Timer T3 Operating Modes 30-8
30.1.3 GPT1 Auxiliary Timers T2/T4 Control 30-15
30.1.4 GPT1 Auxiliary Timers T2/T4 Operating Modes 30-21
30.1.5 GPT1 Clock Signal Control 30-31
30.1.6 GPT1 Timer Registers 30-34
30.1.7 Interrupt Control for GPT1 Timers 30-35
30.2 Timer Block GPT2 30-37
30.2.1 GPT2 Core Timer T6 Control 30-39
30.2.2 GPT2 Core Timer T6 Operating Modes 30-42
30.2.3 GPT2 Auxiliary Timer T5 Control 30-46
30.2.4 GPT2 Auxiliary Timer T5 Operating Modes 30-50
30.2.5 GPT2 Register CAPREL Operating Modes 30-55
30.2.6 GPT2 Clock Signal Control 30-61

30.2.7 GPT2 Timer Registers 30-64
30.2.8 Interrupt Control for GPT2 Timers and CAPREL 30-66
30.3 Miscellaneous Registers 30-68
30.4 GPT12 Kernel Register Overview 30-72
30.5 Implementation of the GPT12 Modules 30-74
30.5.1 Address Map 30-74
30.5.2 Module Connections 30-74

31 Analog to Digital Converter (ADC) 31-1
31.1 Introduction 31-1
31.1.1 ADC Block Diagram 31-2
31.1.2 Feature Set 31-3
31.1.3 Abbreviations 31-4
31.1.4 ADC Kernel Overview 31-5
31.1.5 Conversion Request Unit 31-7
31.1.6 Conversion Result Unit 31-9
31.1.7 Interrupt Structure 31-10
31.1.8 Electrical Models 31-11
31.1.8.1 Input Signal Path 31-11
31.1.8.2 Reference Path 31-12
31.1.9 Transfer Characteristics and Error Definitions 31-14
31.2 Operating the ADC 31-15
31.2.1 Register Overview 31-16
31.2.2 Mode Control 31-21
31.2.3 Module Activation and Power Saving Modes 31-23
31.2.4 Clocking Scheme 31-24
31.2.5 ADC Module Registers 31-25
31.2.5.1 Clock Control Register 31-25
31.2.5.2 Kernel State Configuration Register 31-26
31.2.5.3 Service Request Control Registers 31-28
31.2.6 General ADC Kernel Registers 31-29
31.2.6.1 Request Source Input Registers 31-29
31.2.6.2 Module Identification Register 31-32
31.2.6.3 Interrupt Activation Register 31-33
31.2.6.4 Global Control 31-34
31.2.6.5 Global Configuration 31-37
31.2.6.6 Global Status 31-39
31.2.7 Request Source Arbiter 31-42
31.2.7.1 Request Source Priority 31-43
31.2.7.2 Conversion Start Modes 31-44
31.2.8 Arbiter Registers 31-47
31.2.8.1 Arbitration Slot Enable Register 31-47
31.2.8.2 Request Source Priority Register 31-48

31.2.9 Scan Request Source Handling 31-50
31.2.9.1 Overview 31-50
31.2.9.2 Scan Sequence Operation 31-51
31.2.9.3 Request Source Event and Interrupt 31-52
31.2.10 Scan Request Source Registers 31-54
31.2.10.1 Conversion Request Control Registers 31-54
31.2.10.2 Conversion Request Pending Registers 31-56
31.2.10.3 Conversion Request Mode Registers 31-57
31.2.11 Sequential Request Source Handling 31-60
31.2.11.1 Overview 31-61
31.2.11.2 Sequential Source Operation 31-62
31.2.11.3 Request Source Event and Interrupt 31-63
31.2.12 Sequential Source Registers 31-65
31.2.12.1 Queue Mode Registers 31-65
31.2.12.2 Queue Status Registers 31-68
31.2.12.3 Queue 0 Registers 31-70
31.2.12.4 Queue Backup Registers 31-72
31.2.12.5 Queue Input Registers 31-74
31.2.13 Channel-Related Functions 31-76
31.2.13.1 Input Classes 31-76
31.2.13.2 Reference Selection 31-77
31.2.13.3 Alias Feature 31-77
31.2.13.4 Limit Checking 31-78
31.2.13.5 Channel Event Interrupts 31-80
31.2.14 Channel-Related Registers 31-81
31.2.14.1 Channel Control Registers 31-81
31.2.14.2 Input Class Registers 31-83
31.2.14.3 Alias Register 31-84
31.2.14.4 Limit Check Boundary Registers 31-85
31.2.14.5 Channel Flag Register 31-86
31.2.14.6 Channel Flag Clear Register 31-87
31.2.14.7 Channel Event Node Pointer Registers 31-88
31.2.15 Conversion Result Handling 31-90
31.2.15.1 Storage of Conversion Results 31-90
31.2.15.2 Wait-for-Read Mode 31-92
31.2.15.3 Result Event Interrupts 31-93
31.2.15.4 Result FIFO Buffer 31-94
31.2.15.5 Data Reduction Filter 31-96
31.2.15.6 Result Data Filter 31-98
31.2.16 Conversion Result-Related Registers 31-100
31.2.16.1 Result Register 0 31-100
31.2.16.2 Result Registers 1 to 15 31-102
31.2.16.3 Valid Flag Register 31-104

31.2.16.4 Result Control Registers 31-105
31.2.16.5 Event Flag Register 31-107
31.2.16.6 Event Flag Clear Register 31-109
31.2.16.7 Event Node Pointer Registers 31-110
31.2.17 Multiplexer Test Support 31-113
31.2.18 External Multiplexer Control 31-114
31.2.19 Synchronized Conversions for Parallel Sampling 31-117
31.2.20 Equidistant Sampling 31-120
31.2.21 Access Protection 31-122
31.2.22 Broken Wire Detection 31-123
31.2.23 Additional Feature Registers 31-125
31.2.23.1 Access Protection Register 31-125
31.2.23.2 External Multiplexer Control 31-126
31.2.23.3 Synchronization Control Register 31-130
31.2.23.4 Broken Wire Detection Enable Register 31-132
31.2.23.5 Broken Wire Detection Configuration Register 31-133
31.3 Implementation 31-134
31.3.1 Request Sources in TC1798 31-134
31.3.2 Address Map 31-134
31.3.3 Result Data Filter 31-135
31.3.4 ADC Module Connections 31-136
31.3.4.1 ADC0 Connections 31-137
31.3.4.2 ADC1 Connections 31-143
31.3.4.3 ADC2 Connections 31-149
31.3.4.4 ADC3 Connections 31-155
31.3.4.5 Service Request Connections 31-161
31.3.4.6 Kernel Synchronization 31-162

32 Fast Analog to Digital Converter (FADC) 32-1
32.1 FADC Short Description 32-2
32.2 FADC Kernel Description 32-5
32.2.1 Analog Input Stage Configurations 32-5
32.2.2 Result Representation 32-7
32.2.3 Conversion Timing 32-7
32.2.4 Channel Triggers 32-8
32.2.5 Channel Timer 32-11
32.2.6 Conversion Control 32-12
32.2.6.1 Static Channel Priority 32-12
32.2.6.2 Dynamic Priority Assignment 32-12
32.2.6.3 Clock Generation 32-13
32.2.6.4 Suspend Mode Behavior 32-13
32.2.6.5 Alias Feature 32-14
32.2.7 Data Reduction Unit 32-15

32.2.7.1 Filter Block Structure 32-16
32.2.7.2 Filter Block Operation 32-16
32.2.7.3 Filter Concatenation 32-17
32.2.7.4 Width of Result Registers 32-19
32.2.8 Neighbor Channel Trigger 32-20
32.2.9 Calibration 32-21
32.2.9.1 Offset Calibration 32-22
32.2.10 Interrupt Generation 32-23
32.3 FADC Register Description 32-26
32.3.1 System Registers 32-30
32.3.1.1 Clock Control Register 32-30
32.3.1.2 Fractional Divider Register 32-31
32.3.1.3 Module Identification Register 32-33
32.3.1.4 Service Request Control Registers 32-34
32.3.2 Global Registers 32-35
32.3.2.1 Conversion Request Status Register 32-35
32.3.2.2 Flag Modification Register 32-37
32.3.2.3 Neighbor Channel Trigger Register 32-39
32.3.2.4 Global Control Register 32-42
32.3.2.5 Alias Register 32-46
32.3.3 Channel Registers 32-48
32.3.3.1 Channel Configuration Registers 32-48
32.3.3.2 Analog Control Registers 32-52
32.3.3.3 Conversion Result Registers 32-54
32.3.4 Filter Registers 32-55
32.3.4.1 Filter Control Registers 32-55
32.3.4.2 Current Result Registers 32-58
32.3.4.3 Intermediate Result Registers 32-60
32.3.4.4 Final Result Registers 32-62
32.4 Implementation of FADC 32-64
32.4.1 Register Overview 32-64
32.4.2 FADC Connections 32-65
32.4.3 Service Request Connections 32-66
32.4.4 Clock Control 32-67

1 Introduction

This User´s Manual describes the Infineon TC1798, a 32-bit microcontroller DSP, based on the Infineon TriCore Architecture.

1.1 About this Document

This document is designed to be read primarily by design engineers and software engineers who need a detailed description of the interactions of the TC1798 functional units, registers, instructions, and exceptions.

This TC1798 User´s Manual describes the features of the TC1798 with respect to the TriCore Architecture. Where the TC1798 directly implements TriCore architectural functions, this manual simply refers to those functions as features of the TC1798. In all cases where this manual describes a TC1798 feature without referring to the TriCore Architecture, this means that the TC1798 is a direct implementation of the TriCore Architecture.

Where the TC1798 implements a subset of TriCore architectural features, this manual describes the TC1798 implementation, and then describes how it differs from the TriCore Architecture. Such differences between the TC1798 and the TriCore Architecture are documented in the section covering each such subject.

1.1.1 Related Documentations

A complete description of the TriCore architecture is found in the document entitled “TriCore Architecture Manual”. The architecture of the TC1798 is described separately this way because of the configurable nature of the TriCore specification: Different versions of the architecture may contain a different mix of systems components. The TriCore architecture, however, remains constant across all derivative designs in order to preserve compatibility.

This User´s Manuals together with the “TriCore Architecture Manual” are required to understand the complete TC1798 micro controller functionality.

1.1.2 Text Conventions

This document uses the following text conventions for named components of the TC1798:

- Functional units of the TC1798 are given in plain UPPER CASE. For example: “The SSC supports full-duplex and half-duplex synchronous communication”.
- Pins using negative logic are indicated by an overline. For example: “The external reset pin, $\overline{\text{ESR0}}$, has a dual function.”.
- Bit fields and bits in registers are in general referenced as “Module_Register name.Bit field” or “Module_Register name.Bit”. For example: “The Current CPU Priority Number bit field CPU_ICR.CCPN is cleared”. Most of the

register names contain a module name prefix, separated by an underscore character "_" from the actual register name (for example, "ASC0_CON", where "ASC0" is the module name prefix, and "CON" is the kernel register name). In chapters describing the kernels of the peripheral modules, the registers are mainly referenced with their kernel register names. The peripheral module implementation sections mainly refer to the actual register names with module prefixes.

- Variables used to describe sets of processing units or registers appear in mixed upper and lower cases. For example, register name "MSGCFGn" refers to multiple "MSGCFG" registers with variable n. The bounds of the variables are always given where the register expression is first used (for example, "n = 0-31"), and are repeated as needed in the rest of the text.
- The default radix is decimal. Hexadecimal constants are suffixed with a subscript letter "H", as in 100_H. Binary constants are suffixed with a subscript letter "B", as in: 111_B.
- When the extent of register fields, groups register bits, or groups of pins are collectively named in the body of the document, they are represented as "NAME[A:B]", which defines a range for the named group from B to A. Individual bits, signals, or pins are given as "NAME[C]" where the range of the variable C is given in the text. For example: CFG[2:0] and SRPN[0].
- Units are abbreviated as follows:
  - **MHz** = Megahertz
  - **µs** = Microseconds
  - **kBaud, kbit** = 1000 characters/bits per second
  - **MBaud, Mbit** = 1,000,000 characters/bits per second
  - **Kbyte, KB** = 1024 bytes of memory
  - **Mbyte, MB**= 1048576 bytes of memory

  In general, the k prefix scales a unit by 1000 whereas the K prefix scales a unit by 1024. Hence, the Kbyte unit scales the expression preceding it by 1024. The kBaud unit scales the expression preceding it by 1000. The M prefix scales by 1,000,000 or 1048576, and µ scales by .000001. For example, 1 Kbyte is 1024 bytes, 1 Mbyte is 1024 × 1024 bytes, 1 kBaud/kbit are 1000 characters/bits per second, 1 MBaud/Mbit are 1000000 characters/bits per second, and 1 MHz is 1,000,000 Hz.
- Data format quantities are defined as follows:
  - **Byte** = 8-bit quantity
  - **Half-word** = 16-bit quantity
  - **Word** = 32-bit quantity
  - **Double-word** = 64-bit quantity

1.1.3 Reserved, Undefined, and Unimplemented Terminology

In tables where register bit fields are defined, the following conventions are used to indicate undefined and unimplemented function. Furthermore, types of bits and bit fields are defined using the abbreviations as shown in **Table 1-1**.

Table 1-1 Bit Function Terminology

Function of Bits	Description
Unimplemented, Reserved	Register bit fields named **0** indicate unimplemented functions with the following behavior. • Reading these bit fields returns 0. • These bit fields should be written with 0 if the bit field is defined as r or rh. • These bit fields have to be written with 0 if the bit field is defined as rw. These bit fields are reserved. The detailed description of these bit fields can be found in the register descriptions.
rw	The bit or bit field can be read and written.
rwh	As rw, but bit or bit field can be also set or reset by hardware.
r	The bit or bit field can only be read (read-only).
w	The bit or bit field can only be written (write-only). A read to this register will always give a default value back.
rh	This bit or bit field can be modified by hardware (read-hardware, typical example: status flags). A read of this bit or bit field give the actual status of this bit or bit field back. Writing to this bit or bit field has no effect to the setting of this bit or bit field.
s	Bits with this attribute are “sticky” in one direction. If their reset value is once overwritten by software, they can be switched again into their reset state only by a reset operation. Software cannot switch this type of bit into its reset state by writing the register. This attribute can be combined to “rws” or “rwhs”.
f	Bits with this attribute are readable only when they are accessed by an instruction fetch. Normal data read operations will return other values.

1.1.4 Register Access Modes

Read and write access to registers and memory locations are sometimes restricted. In memory and register access tables, the terms as defined in **Table 1-2** are used.

Table 1-2 Access Terms

Symbol	Description
U	Access Mode: Access permitted in User Mode 0 or 1.
	Reset Value: Value or bit is not changed by a reset operation.
SV	Access permitted in Supervisor Mode.
R	Read-only register.
32	Only 32-bit word accesses are permitted to this register/address range.
E	Endinit-protected register/address.
PW	Password-protected register/address.
NC	No change, indicated register is not changed.
BE	Indicates that an access to this address range generates a Bus Error.
nBE	Indicates that no Bus Error is generated when accessing this address range, even though it is either an access to an undefined address or the access does not follow the given rules.
nE	Indicates that no Error is generated when accessing this address or address range, even though the access is to an undefined address or address range. True for CPU accesses (MTCR/MFCR) to undefined addresses in the CSFR range.

1.1.5 Abbreviations and Acronyms

The following acronyms and terms are used in this document:

ADC	Analog-to-Digital Converter
AGPR	Address General Purpose Register
ALU	Arithmetic and Logic Unit
ASC	Asynchronous/Synchronous Serial Controller
BCU	Bus Control Unit
BMU	Bus Monitor Unit
BROM	Boot ROM & Test ROM
CAN	Controller Area Network
CMEM	PCP Code Memory
CISC	Complex Instruction Set Computing
CPS	CPU Slave Interface

CPU	Central Processing Unit
CRC	Cyclic Redundancy Code
CSA	Context Save Area
CSFR	Core Special Function Register
CCU6	Capture Compare Unit 6
DAP	Device Access Port
DAS	Device Access Server
DCACHE	Data Cache
DFLASH	Data Flash Memory
DGPR	Data General Purpose Register
DMA	Direct Memory Access
DMI	Data Memory Interface
DSPR	Data Scratch Pad RAM
EBU	External Bus Interface
ECC	Error Correction Code
EMI	Electro-Magnetic Interference
FADC	Fast Analog-to-Digital Converter
FAM	Flash Array Module
FCE	Flexible CRC Engine
FCS	Flash Command State Machine
FIM	Flash Interface and Control Module
FM-PLL	PLL with Frequency Modulation support
FPI	Flexible Peripheral Interconnect (Bus)
FPU	Floating Point Unit
GPIO	General Purpose Input/Output
GPR	General Purpose Register
GPT12	General Purpose Timer 12
GPTA	General Purpose Timer Array
ICACHE	Instruction Cache
I/O	Input / Output
JTAG	Joint Test Action Group = IEEE1149.1
LTC	Local Timer Cell

MCHK	Memory Checker module
MLI	Micro Link Interface
MMU	Memory Management Unit
MSB	Most Significant Bit
MSC	Micro Second Channel
NC	Not Connected
NMI	Non-Maskable Interrupt
OCDS	On-Chip Debug Support
OVRAM	Overlay Memory
PCP	Peripheral Control Processor
PLL	Phase Locked Loop
PFLASH	Program Flash Memory
PMI	Program Memory Interface
PMU	Program Memory Unit
PRAM	PCP Parameter RAM
PSPR	Program Scratch Pad RAM
RAM	Random Access Memory
RISC	Reduced Instruction Set Computing
SBCU	System Peripheral Bus Control Unit
SCU	System Control Unit
SENT	Single Edge Nibble Transmission
SHE	Secure Hardware Extension
SFR	Special Function Register
SPB	System Peripheral Bus
SRI	Shared Resource Interconnect
SRAM	Static Data Memory
SRN	Service Request Node
SSC	Synchronous Serial Controller
SSCG	Synchronous Serial Controller Guardian
STM	System Timer

WDT	Watchdog Timer
XBar, XBar_SRI	Cross Bar Interconnect, based on the Shared Resource Interconnect protocol

1.2 System Architecture of the TC1798

The TC1798 combines three powerful technologies within one silicon die, achieving new levels of power, speed, and economy for embedded applications:

- Reduced Instruction Set Computing (RISC) processor architecture
- Digital Signal Processing (DSP) operations and addressing modes
- On-chip memories and peripherals

DSP operations and addressing modes provide the computational power necessary to efficiently analyze complex real-world signals. The RISC load/store architecture provides high computational bandwidth with low system cost. On-chip memory and peripherals are designed to support even the most demanding high-bandwidth real-time embedded control-systems tasks.

Additional high-level features of the TC1798 include:

- Efficient memory organization: instruction and data scratch memories, caches
- Serial communication interfaces – flexible synchronous and asynchronous modes
- Peripheral Control Processor – standalone data operations and interrupt servicing
- DMA and SDMA Controller – DMA operations and interrupt servicing
- Secure Hardware Extension
- Flexible CRC Engine
- Bus Monitor Unit
- General-purpose timers
- High-performance on-chip buses
- On-chip debugging and emulation facilities
- Flexible interconnections to external components
- Flexible power-management

The TC1798 is a high-performance microcontroller with TriCore CPU, program and data memories, buses, bus arbitration, an interrupt controller, a peripheral control processor and a DMA controller and several on-chip peripherals. The TC1798 is designed to meet the needs of the most demanding embedded control systems applications where the competing issues of price/performance, real-time responsiveness, computational power, data bandwidth, and power consumption are key design elements.

The TC1798 offers several versatile on-chip peripheral units such as serial controllers, timer units, and Analog-to-Digital converters. Within the TC1798, all these peripheral units are connected to the TriCore CPU/system via the Flexible Peripheral Interconnect (FPI) Bus and the Local Memory Bus (SRI). Several I/O lines on the TC1798 ports are reserved for these peripheral units to communicate with the external world.

1.2.1 TC1798 Block Diagram

Figure 1-1 shows the block diagram of the TC1798. Pls. note that not all features that are shown in the block diagram are available in the other TC1798 package variants.

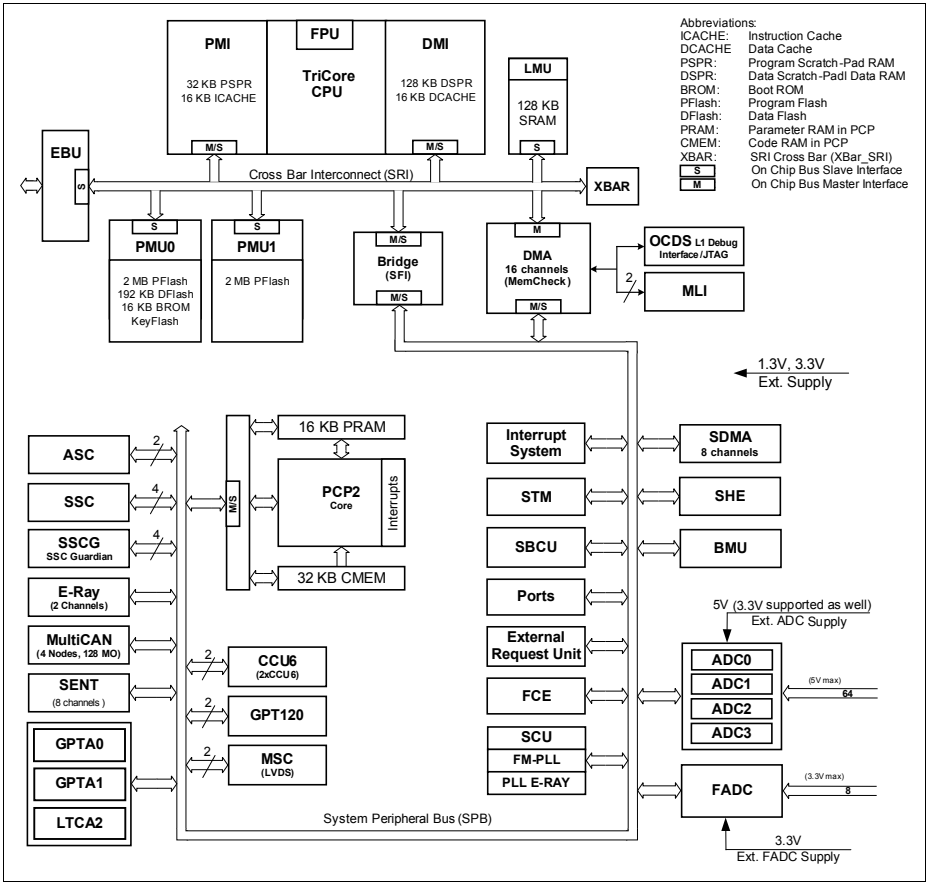


Figure 1-1 TC1798 Block Diagram

1.2.2 CPU Cores of the TC1798

The TC1798 includes a high Performance CPU and a Peripheral Control Processor.

1.2.2.1 High-performance 32-bit CPU

This chapter gives an overview of the TriCore 1.6 architecture.

TriCore (TC1.6) Architectural Highlights

- Unified RISC MCU/DSP
- 32-bit architecture with 4 Gbytes unified data, program, and I/O address space
- 32 general purpose registers with fast automatic context-switching
- Multiply-accumulate unit able to sustain 2 MAC operations per cycle.
- Fully pipelined Floating point unit
- Saturating integer arithmetic
- Bit handling
- Packed data operations
- Zero overhead loop
- Dedicated integer divide unit.
- Precise exceptions
- Flexible power management
- Flexible memory protection system

High-efficiency TriCore Instruction Set

- Powerful instruction set
- Freely mixable 16-bit and 32-bit instructions for reduced code size
- Data types include: Boolean, array of bits, character, signed and unsigned integer, integer with saturation, signed fraction, double-word integers, and IEEE-754 single-precision floating point
- Data formats include: Bit, 8-bit byte, 16-bit half-word, 32-bit word, and 64-bit double-word
- Flexible and efficient addressing mode for high performance and code density

Integrated CPU related On-Chip Memories

- Instruction memory:
  - 32 Kbyte Instruction Scratch-Pad RAM (PSPR)
  - 16 Kbyte Instruction Cache (ICACHE)
- Data memory:
  - 128 Kbyte Data Scratch-Pad RAM (DSPR)
  - 16 Kbyte Data Cache (DACHE)
- All memories are ECC protected

1.2.2.2 High-performance 32-bit Peripheral Control Processor

The PCP is a flexible Peripheral Control Processor optimized for interrupt handling and thus unloading the CPU.

Features

- Data move between any two memory or I/O locations
- Data move with predefined limit supported
- Read-Modify-Write capabilities
- Full computation capabilities including basic MUL/DIV
- Read/move data and accumulate it to previously read data
- Read two data values and perform arithmetic or logical operation and store result
- Bit-handling capabilities (testing, setting, clearing)
- Flow control instructions (conditional/unconditional jumps, breakpoint)
- Programmable write protection for Code Memory and Parameter Memory
- Programmable limit of FPI addresses than can be written by the PCP
- Dedicated Interrupt System
- PCP SRAMs with ECC protection
- High Integrity Operation support

Integrated PCP related On-Chip Memories

- 32 Kbyte Code Memory (CMEM)
- 16 Kbyte Parameter Memory (PRAM)

1.3 On-Chip System Units

The TC1798 microcontroller offers several versatile on-chip system peripheral units such as DMA controller modules (DMA, SDMA), embedded Flash modules (PMU0, PMU1), Flexible CRC Engine (FCE), System Timer Unit (STM), System Control Unit (SCU), Overlay Control Unit (OVC), Local Memory Unit (LMU), Bus Monitor Unit (BMU), Interrupt System and Ports modules.

1.3.1 Flexible Interrupt System

The TC1798 includes a programmable interrupt system with the following features:

1.3.1.1 Feature List

The interrupt system provides the following features:

- Fast interrupt response
- Hardware arbitration
- Independent interrupt systems for CPU and PCP
- Programmable service request nodes (SRNs)
- Each SRN can be mapped to the CPU or PCP interrupt system
- Flexible interrupt-prioritizing scheme with 255 interrupt priority levels per interrupt system

1.3.2 Direct Memory Access Controller (DMA)

The TC1798 includes a fast and flexible DMA controller with 16 independant DMA channels.

1.3.2.1 Feature List

The DMA controller provides the following features:

- 16 independent DMA channels
  - 2 DMA Sub-Blocks with (8 DMA channels per DMA Sub-Block)
  - DMA Sub-Blocks with support of parallel channel execution (1 channel per Sub-Block, both Sub-Blocks in parallel)
  - Up to 16 selectable request inputs per DMA channel
  - 2-level programmable priority of DMA channels within the DMA Sub-Block
  - Software and hardware DMA request
  - Hardware requests by selected on-chip peripherals and external inputs
- 3-level programmable priority of the DMA Sub-Blocks at the on chip bus interfaces
- Buffer capability for move actions on the buses (at least 1 move per bus is buffered)
- Individually programmable operation modes for each DMA channel
  - Single Mode: stops and disables DMA channel after a predefined number of DMA transfers

  - Continuous Mode: DMA channel remains enabled after a predefined number of DMA transfers; DMA transaction can be repeated
  - Programmable address modification
  - Two shadow register modes (with / w/o automatic re-set and direct write access).
- Full 32-bit addressing capability of each DMA channel
  - 4 Gbyte address range
  - Data block move supports > 32 Kbyte moves per DMA transaction
  - Circular buffer addressing mode with flexible circular buffer sizes
- Programmable data width of DMA transfer/transaction: 8-bit, 16-bit, or 32-bit
- Register set for each DMA channel
  - Source and destination address register
  - Channel control and status register
  - Transfer count register
- Flexible interrupt generation (the service request node logic for the MLI channels is also implemented in the DMA modules)
- DMA module is working on SPB frequency, SRI interface on CPU frequency.
- Dependant on the target/destination address, Read/write requests from the Move Engines are directed to the SPB, LMB, MLIs or to the the Cerberus.

1.3.3 Safe Direct Memory Access Controller

The TC1798 includes a fast and flexible Safe DMA controller with 8 independant DMA channels. Additionally to the normal DMA channels, the Safe DMA channels extended with CRC features for the read data, source and destination address.

1.3.3.1 Feature List

The SDMA provides the following features:

- 8 independent DMA channels
  - 8 DMA channels in the DMA Sub-Block
  - Up to 16 selectable request inputs per DMA channel
  - 2-level programmable priority of DMA channels within the DMA Sub-Block
  - Software and hardware DMA request
  - Hardware requests by selected on-chip peripherals and external inputs
-
- Upper and lower address boundary checking of the source and destination address.
- 3-level programmable priority of the DMA Sub-Block at the on chip bus interfaces
- Buffer capability for move actions on the buses (at least 1 move per bus is buffered)
- Individually programmable operation modes for each DMA channel
  - Single Mode: stops and disables DMA channel after a predefined number of DMA transfers
  - Continuous Mode: DMA channel remains enabled after a predefined number of DMA transfers; DMA transaction can be repeated

  - Programmable address modification
  - Two shadow register modes (with / w/o automatic re-set and direct write access).
- Full 32-bit addressing capability of each DMA channel
  - 4 Gbyte address range
  - Data block move supports > 32 Kbyte moves per DMA transaction
  - Circular buffer addressing mode with flexible circular buffer sizes
- Programmable data width of DMA transfer/transaction: 8-bit, 16-bit, or 32-bit
- Register set for each DMA channel
  - Source and destination address register
  - Channel control and status register
  - Transfer count register
- Generation of unique CRC checksums for source and destination addresses.
- Generation of in-line CRC checksum for read data.
- Flexible interrupt generation
- DMA module is working on SPB frequency.

1.3.4 Flexible CRC Engine (FCE)

The Flexible CRC Engine (FCE) module provides a parallel implementation of one or more Cyclic Redundancy Code (CRC) algorithms. The standard CRC polynomial implemented in the FCE module is the IEEE 802.3 ethernet CRC32. The FCE is meant to be used as an hardware acceleration engine for software applications or operating systems services (compatible with Autosar CRC “specification of CRC Routines”) using CRC signatures.

1.3.4.1 Feature List

The FCE provides the following features:

- Two CRC polynomials:
  - IEEE 802.3 CRC32 ethernet polynomial: 0x82608EDB (CRC kernel 0)
  - CRC32C Castagnoli: 0xD419CC15 (CRC kernel 1)
- Parallel CRC implementation (32-bits wide)
  - Data blocks to be computed by FCE shall be a multiple of 32-bits
  - Start address of Data blocks to be computed by FCE shall be at least 32-bits aligned
- Register Interface compliant with Autosar specification for CRC routines. Enables to support reentrant software routines via a software-based save/restore mechanism.
- Extended register interface to control reliability of FCE execution.
- Redundant implementation of critical control registers
- Error notification scheme via dedicated interrupt node
- Support of hardware configuration:

– Each CRC kernel supports as generic parameter the degree of the polynomial (POLY_DEGREE) directly controlling the width of the FCE data path. Only 32, 16 and 8 are allowed.
– FCE is designed as a multi - CRC kernel structure supporting concurrent operation of each CRC - kernel.

1.3.5 System Timer (STM)

The TC1798's STM is designed for global system timing applications requiring both high precision and long range.

1.3.5.1 Feature List

The System Timer provides the following features:

- Free-running 56-bit counter
- All 56 bits can be read synchronously
- Different 32-bit portions of the 56-bit counter can be read synchronously
- Flexible interrupt generation based on compare match with partial STM content
- Counting starts automatically after a reset operation
- STM registers are reset by an application reset if bit ARSTDIS.STMDIS is cleared. If bit ARSTDIS.STMDIS is set, the STM registers are not reset.[1)]
- STM can be halted in debug/suspend mode

Special STM register semantics provide synchronous views of the entire 56-bit counter, or 32-bit subsets at different levels of resolution.

The maximum clock period is $2^{56} \times f_{STM}$. At f_{STM} = 90 MHz, for example, the STM counts 25.39 years before overflowing. Thus, it is capable of continuously timing the entire expected product life time of a system without overflowing.

The STM can be optionally disabled for power-saving purposes, or suspended for debugging purposes via its clock control register. In suspend mode of the TC1798 (initiated by writing an appropriate value to STM_CLC register), the STM clock is stopped but all registers are still readable.

Due to the 56-bit width of the STM, it is not possible to read its entire content with one instruction. It needs to be read with two load instructions. Since the timer would continue to count between the two load operations, there is a chance that the two values read are not consistent (due to possible overflow from the low part of the timer to the high part between the two read operations). To enable a synchronous and consistent reading of the STM content, a capture register (STM_CAP) is implemented. It latches the content of the high part of the STM each time when one of the registers STM_TIM0 to STM_TIM5 is read. Thus, STM_CAP holds the upper value of the timer at exactly the same time

1) "STM registers" means all registers except STM_CLC, STM_SRC0, and STM_SRC1.

when the lower part is read. The second read operation would then read the content of the STM_CAP to get the complete timer value.

The content of the 56-bit System Timer can be compared against the content of two compare values stored in the STM_CMP0 and STM_CMP1 registers. Interrupts can be generated on a compare match of the STM with the STM_CMP0 or STM_CMP1 registers.

Figure 1-2 provides an overview on the STM module. It shows the options for reading parts of STM content.

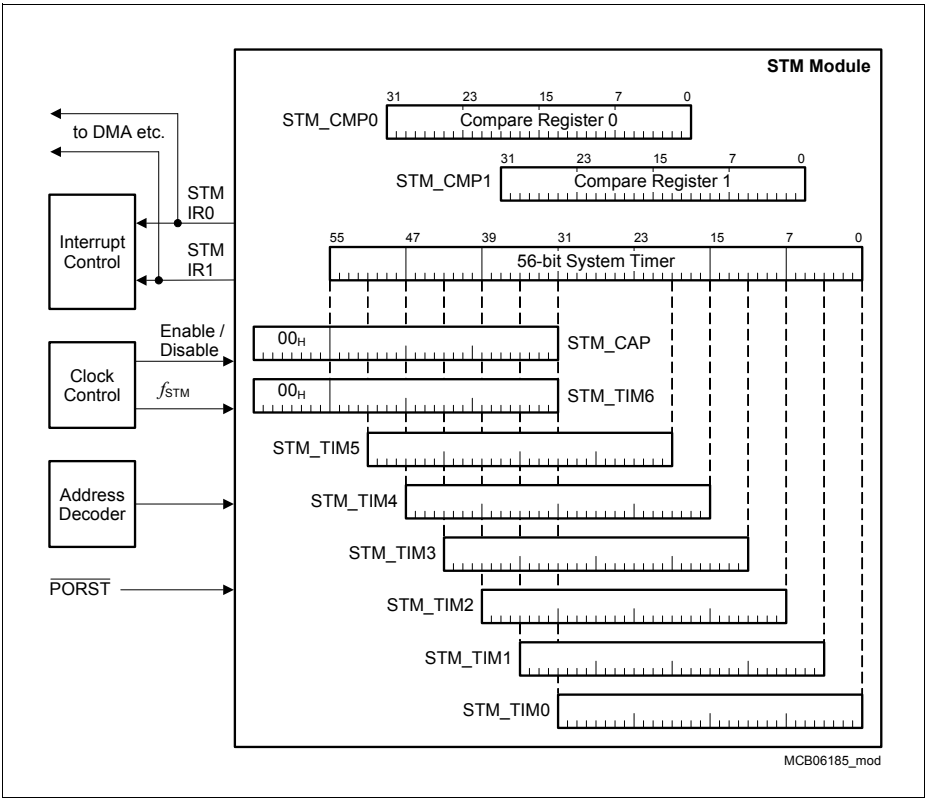


Figure 1-2 General Block Diagram of the STM Module Registers

1.3.6 System Control Unit (SCU)

The following SCU introduction gives an overview about the TC1798 System Control Unit (SCU).

The System Control Unit (SCU) of the TC1798 handles all system control tasks beside the debug related tasks which are controlled by the OCDS/Cerberus.

The SCU contains the following functional sub-blocks:

- Clock Control
- Reset Operation
- External Interface
- Power Management
- Software Boot Support
- SRAM ECC Control
- Die Temperature Measurement
- Watchdog Timer
- Emergency Stop Control
- NMI Trap Generation

1.3.6.1 Clock Generation Unit (CGU)

The Clock Generation Unit (CGU) allows a very flexible clock generation for the TC1798. During user program execution the frequency can be programmed for an optimal ratio between performance and power consumption.

1.3.6.2 Features of the Watchdog Timer (WDT)

The main features of the WDT are summarized here.

- 16-bit Watchdog counter
- Selectable input frequency: $f_{FPI}/256$ or $f_{FPI}/16384$
- 16-bit user-definable reload value for normal Watchdog operation, fixed reload value for Time-Out and Prewarning Modes
- Incorporation of the ENDINIT bit and monitoring of its modifications
- Sophisticated Password Access mechanism with fixed and user-definable password fields
- Access Error Detection: Invalid password (during first access) or invalid guard bits (during second access) trigger the Watchdog reset generation
- Overflow Error Detection: An overflow of the counter triggers the Watchdog reset generation
- Watchdog function can be disabled; access protection and ENDINIT monitor function remain enabled
- Double Reset Detection: If a Watchdog induced reset occurs twice, a severe system malfunction is assumed and the TC1798 is held in reset until a system / class 0 reset occurs. This prevents the device from being periodically reset if, for instance,

connection to the external memory has been lost such that even system initialization could not be performed

1.3.6.3 Reset Operation

The following reset request triggers are available:

- 1 External power-on hardware reset request trigger; $\overline{\text{PORST}}$, (cold reset)
- 2 External System Request reset triggers; $\overline{\text{ESR0}}$ and $\overline{\text{ESR1}}$ (cold/warm reset)
- Watchdog Timer (WDT) reset request trigger, (warm reset)
- Software reset (SW), (warm reset)
- Debug (OCDS) reset request trigger, (warm reset)
- JTAG reset (special reset)
- Resets via the JTAG interface

Note: The JTAG and OCDS resets are described in the OCDS chapter.

There are two basic types of reset request triggers:

- Trigger sources that do not depend on a clock, such as the $\overline{\text{PORST}}$. This trigger force the device into an asynchronous reset assertion independently of any clock. The activation of an asynchronous reset is asynchronous to the system clock, whereas its de-assertion is synchronized.
- Trigger sources that need a clock in order to be asserted, such as the input signals $\overline{\text{ESR0}}$, $\overline{\text{ESR1}}$, and $\overline{\text{ESR2}}$, the WDT trigger, the parity trigger, or the SW trigger.

1.3.6.4 External Interface (ESR, ERU)

The SCU provides interface pads for system purpose. Various functions are covered by these pins. Due to the different tasks some of the pads can not be shared with other functions but most of them can be shared with other functions. The following functions are covered by the SCU controlled pads:

- Reset request triggers
- Reset indication
- Trap request triggers
- Interrupt request triggers
- Non SCU module triggers

The first three points are covered by the ESR pads and the last two points by the ERU pads.

1.3.6.5 Die Temperature Measurement (DTS)

The Die Temperature Sensor (DTS) generates a measurement result that indicates directly the current temperature. The result of the measurement can be read via an DTS register.

1.3.7 General Purpose I/O Ports and Peripheral I/O Lines (Ports)

The TC1798 has port connections to interface with its peripherals and external devices. As an input port line, the digital signal from other parts of a circuit can be read. Alternatively, the port can act as output to control or signal to other peripherals or devices.

The TC1798 has a port structure where each port line has a number of control and data bits, enabling flexible usage of the line. If a peripheral unit uses a GPIO port line as a bi-directional I/O line, each port pin can be configured for input or output operation.

In input mode, it is possible to activate the internal weak pull-up, pull-down, or no input pull device. Input signals are connected directly to the various inputs of the peripheral units. Push-pull or open drain out put modes are available for selection. In addition, the pad output driver strength can be programmed individually for each port line. The pads are also capable to be configured for different pad levels.

When the port is in output mode, the digital level of the pin can be read by software through the input path or a peripheral can use the pin level as an input.The output multiplexer selects the signal source for the GPIO line when used as output. If the pin is used as general-purpose output, the multiplexer is switched to the Output Data Register Pn_OUT. The logic state of a port line can be set, cleared or toggled bit-wise.

When selected as general-purpose output line, the actual logic level at the pin can be examined and compared against the applied output level. This can be used to detect some electrical failures at the pin caused through external circuitry.

1.3.7.1 Feature List

The Port modules provide the following features:

- Digital General-Purpose Input/Output (GPIO) port lines
- Input/output functionality individually programmable for each port line
- Programmable input characteristics (pull-up, pull-down, no pull device)
- Pad output driver strength can be programmed individually for each port port line to minimize EMI (weak, medium, strong)
- Programmable output characteristics (push-pull, open drain)
- Programmable alternate output functions
- Output lines of each port can be updated port-wise or set/reset/toggled bit-wise

1.3.8 Program Memory Unit (PMU)

The Program Memory Unit “PMU” is part of the processor subsystem. The PMUs control the Flash memory and the Boot ROM.

The devices of the Audo-Max have at least one Program Memory Unit. This is named “PMU0”. With increasing Flash memory more PMUs are added which are named “PMU1”, and so on.

The TC1798 includes 2 PMUs (PMU0, PMU1). The exact configuration of each PMU is described in the PMU chapter in this document. Derived devices with a reduced set of memories may exist. Their configuration is contained in the data sheet.

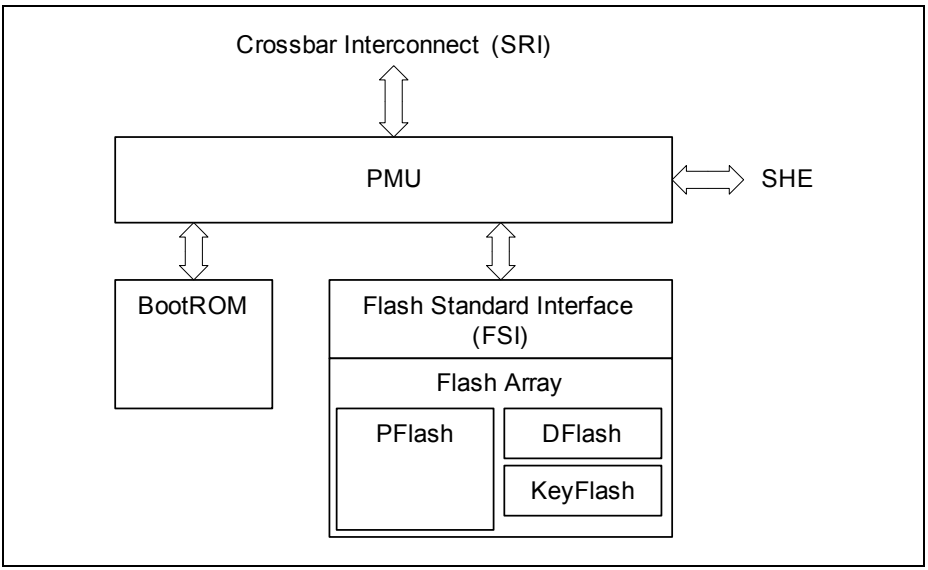


Figure 1-3 PMU Basic Block Diagram

1.3.8.1 Feature List

The PMU modules provides the following features:

- BootROM (“BROM”), only in PMU0.
- Program Flash (“PFlash”):
  - PMU0: 2 MByte.
  - PMU1: 2 MByte.
- Data Flash (“DFlash”):
  - PMU0: 192 KByte.
- Security Flash for SHE (“KeyFlash”).
- SRI slave interface for all assigned Flash memories and registers.

- Flash command control.
- Flash and BROM access control.
- Tuning Protection.
- Interface to security module SHE.

1.3.9 Secure Hardware Extension (SHE)

The SHE module realizes the functionality defined by HIS as “SHE” (Secure Hardware Extension). The storage of keys is done by the PMU0.

For further information please contact your Infineon representative.

1.3.10 Local Memory Unit (LMU)

The Local Memory Unit is an SRI peripheral providing access to volatile memory resources. It’s primary purpose is to provide 128 Kbytes of local memory for general purpose usage but it will also provide access to the separate block of emulation and debug memory (EMEM) provided in the Emulation Devices.

1.3.10.1 Feature List

An overview of the features implemented in the LMU follows:

- 128 Kbytes of SRAM
  - organised as 64 bit words
  - support for burst access
  - support of single data access (byte, half word, word accesses and double word)
  - ECC protection
- Interface to the EMEM of the ED device.
- OLDA region support.

1.3.11 Data Access Overlay (OVC)

The data overlay functionality provides the capability to redirect data accesses by the TriCore to program memory (internal Program Flash or external memory) to the SRAM in the Local Memory Unit (LMU), or to the Emulation Memory in Emulation Device ED, or to the external memory. This functionality makes it possible, for example, to modify the application's test and calibration parameters (which are typically stored in the program memory) during run time of a program. Note that read and write data accesses from/to program memory are redirected.

1.3.11.1 Feature List

The Data Access Overlay provides the following features:

- 16 overlay ranges ("blocks") configurable for Program Flash and external memory
- Supports usage of LMU SRAM (128 KB) as internal overlay memory
- Support of up to 512 Kbyte overlay/calibration memory in Emulation Device (EMEM)
- Support of up to 2 MB overlay memory in external memory (EBU space)
- Support of Online Data Acquisition into range of up to 32 KB and of its overlay
- Support of different overlay memory selections for every enabled overlay block
- Sizes of overlay blocks selectable from 16 byte to 512 Kbyte
- All configured overlay ranges can be enabled with only one register write access
- Programmable flush (invalidate) control for data cache in DMI

1.4 On-Chip Peripheral Units of the TC1798

The TC1798 microcontroller offers several versatile on-chip peripheral units such as serial controllers, timer units, and Analog-to-Digital converters. Several I/O lines on the TC1798 ports are reserved for these peripheral units to communicate with the external world.

On-Chip Peripheral Units

- Two Asynchronous/Synchronous Serial Channels (ASC) with baud-rate generator, parity, framing and overrun error detection
- Four Synchronous Serial Channels (SSC) with programmable data length and shift direction
- Four SSC Guardian modules (SSCG, one related to each SSC module)
- Two Micro Second Bus Interfaces (MSC) for serial communication
- One CAN Module with four CAN nodes (MultiCAN) for high-efficiency data handling via FIFO buffering and gateway data transfer
- Two Micro Link Serial Bus Interfaces (MLI) for serial multiprocessor communication
- Two General Purpose Timer Arrays (GPTA) with a powerful set of digital signal filtering and timer functionality to accomplish autonomous and complex Input/Output management. One additional Local Timer Cell Array (LCTA).
- Four CapCom 6 Unit modules (CCU6)
- Two General Purpose 12 Timer Units (GPT12)
- One SENT module (SENT) with support of 8 serial communication lines
- Four Analog-to-Digital Converter Units (ADC) with 8-bit, 10-bit, or 12-bit resolution.
- One fast Analog-to-Digital Converter Unit (FADC)
- One FlexRay™ module with 2 channels (E-Ray).
- One External Bus Interface (EBU)

1.4.1 Asynchronous/Synchronous Serial Interfaces (ASC)

The TC1798 includes two Asynchronous/Synchronous Serial Interfaces, ASC0 and ASC1. Both ASC modules have the same functionality.

Figure 1-5 shows a global view of the Asynchronous/Synchronous Serial Interface (ASC).

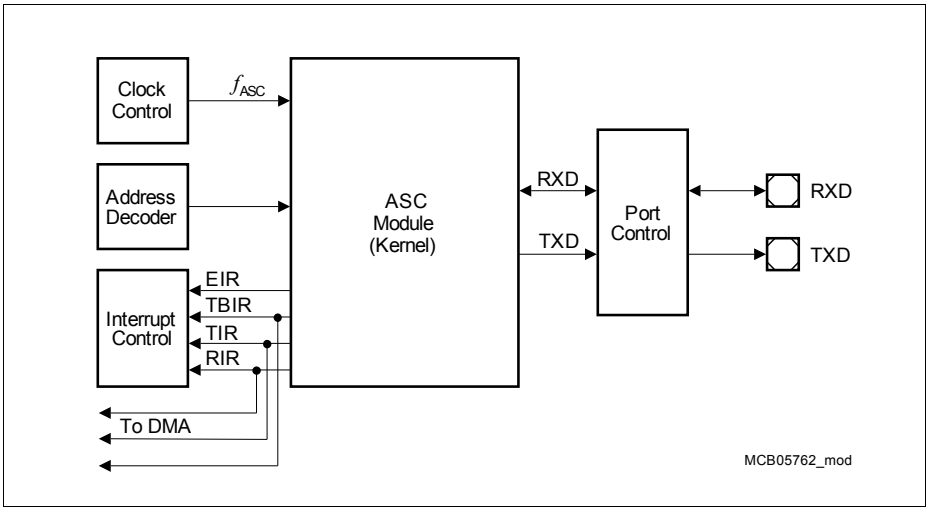


Figure 1-4 General Block Diagram of the ASC Interface

The ASC provides serial communication between the TC1798 and other microcontrollers, microprocessors, or external peripherals.

The ASC supports full-duplex asynchronous communication and half-duplex synchronous communication. In Synchronous Mode, data is transmitted or received synchronous to a shift clock that is generated by the ASC internally. In Asynchronous Mode, 8-bit or 9-bit data transfer, parity generation, and the number of stop bits can be selected. Parity, framing, and overrun error detection are provided to increase the reliability of data transfers. Transmission and reception of data is double-buffered. For multiprocessor communication, a mechanism is included to distinguish address bytes from data bytes. Testing is supported by a loop-back option. A 13-bit baud rate generator provides the ASC with a separate serial clock signal, which can be accurately adjusted by a prescaler implemented as fractional divider.

1.4.1.1 Feature List

The ASC module provides the following features:

- Full-duplex asynchronous operating modes
  - 8-bit or 9-bit data frames, LSB first
  - Parity-bit generation/checking
  - One or two stop bits
  - Baud rate from 6.875 Mbit/s to 1.64 bit/s (@ 110 MHz module clock)
  - Multiprocessor mode for automatic address/data byte detection
  - Loop-back capability

- Half-duplex 8-bit synchronous operating mode
  - Baud rate from 13.75 Mbit/s to 1119 bit/s (@ 110 MHz module clock)
- Double-buffered transmitter/receiver
- Interrupt generation
  - On a transmit buffer empty condition
  - On a transmit last bit of a frame condition
  - On a receive buffer full condition
  - On an error condition (frame, parity, overrun error)
- Implementation features
  - Connections to DMA Controller
  - Connections of receiver input to GPTA (LTC) for baud rate detection and LIN break signal measuring

1.4.2 High-Speed Synchronous Serial Interfaces (SSC)

The TC1798 includes four High-Speed Synchronous Serial Interfaces, SSC0, SSC1, SSC2 and SSC3. All SSC modules have the same functionality.

Figure 1-5 shows a global view of the of the Synchronous Serial interface (SSC).

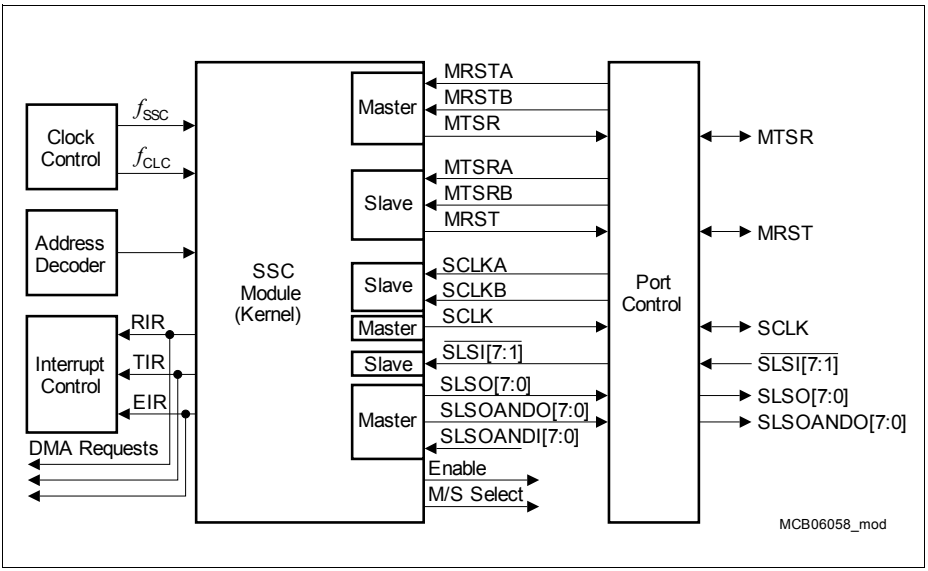


Figure 1-5 General Block Diagram of the SSC Interface

The SSC supports full-duplex and half-duplex serial synchronous communication up to 55.0 Mbit/s (@ 110.0 MHz module clock, Master Mode). The serial clock signal can be generated by the SSC itself (Master Mode) or can be received from an external master (Slave Mode). Data width, shift direction, clock polarity and phase are programmable. This allows communication with SPI-compatible devices. Transmission and reception of data is double-buffered. A shift clock generator provides the SSC with a separate serial clock signal. Seven slave select inputs are available for Slave Mode operation. Eight programmable slave select outputs (chip selects) are supported in Master Mode.

1.4.2.1 Feature List

The SSC module provides the following features:

- Master and Slave Mode operation
  - Full-duplex or half-duplex operation
  - Automatic pad control possible
- Flexible data format

  - Programmable number of data bits: 2 to 16 data bits (with parity: 1 to 15 data bits)
  - Programmable shift direction: LSB or MSB shift first
  - Programmable clock polarity: Idle low or idle high state for the shift clock
  - Programmable clock/data phase: Data shift with leading or trailing edge of the shift clock
- Baud rate generation
  - Master Mode: 55.0 Mbit/s to 839.3 bit/s (@ 110 MHz module clock)
  - Slave Mode: 27.5 Mbit/s to 839.3 bit/s (@ 110 MHz module clock)
- Interrupt generation
  - On a transmitter empty condition
  - On a receiver full condition
  - On an error condition (receive, phase, baud rate, transmit error, parity error)
- Queued SSC Mode supports control and data handling by the DMA controller
- Flexible SSC pin configuration
- Hardware supported parity mode
  - Individually selectable for transmit and receive frames
  - Even/odd parity selection
- Seven slave select inputs $\overline{\text{SLSI}}$[7:1] in Slave Mode
- Eight programmable slave select outputs SLSO[7:0] in Master Mode
  - Automatic SLSO generation with programmable timing
  - Programmable active level and enable control
  - Combinable with SLSO output signals from other SSC modules

1.4.3 Synchronous Serial Interface Guardian (SSCG)

Figure 1-6 shows a sub-system consisting of
- one SSC module SSC0
- one SSCG module SSCG0

This sub-system can be analyzed independently of the rest of the chip. One chip can contain one or more such subsystems. The SSCG module monitors the output signals of the corresponding SSC module and in case of a mismatch between the expected and the ongoing signals, it raises an error.

The TC1798 includes four High-Speed Synchronous Serial Interfaces, SSC0, SSC1, SSC2 and SSC3 and four guardians respectively. All SSCx/SSCGx subsistems provide the same functionality.

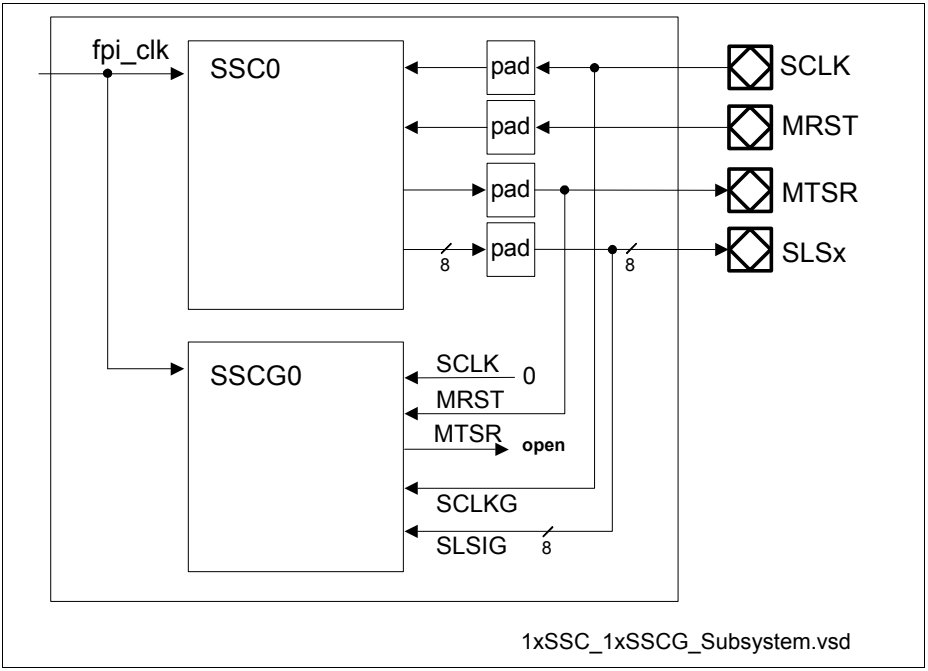


Figure 1-6 General Block Diagram of an SSC / SSCG Sub-System

1.4.3.1 Feature List

The SSCG module provides the following features:

- All output signals of the SSC monitored: data, clock and slave selects.
- Signals monitored after the output driver; it is included in the monitored loop

- Maximum monitored baud-rate of 4 MBaud .

1.4.4 Micro Second Channel Interface (MSC)

The TC1798 includes two Micro Second Channel interfaces, MSC0 and MSC1. Both MSC modules have the same functionality.

The Micro Second Channel (MSC) interface provides serial communication links typically used to connect power switches or other peripheral devices. The serial communication link includes a fast synchronous downstream channel and a slow asynchronous upstream channel. **Figure 1-7** shows a global view of the interface signals of an MSC interface.

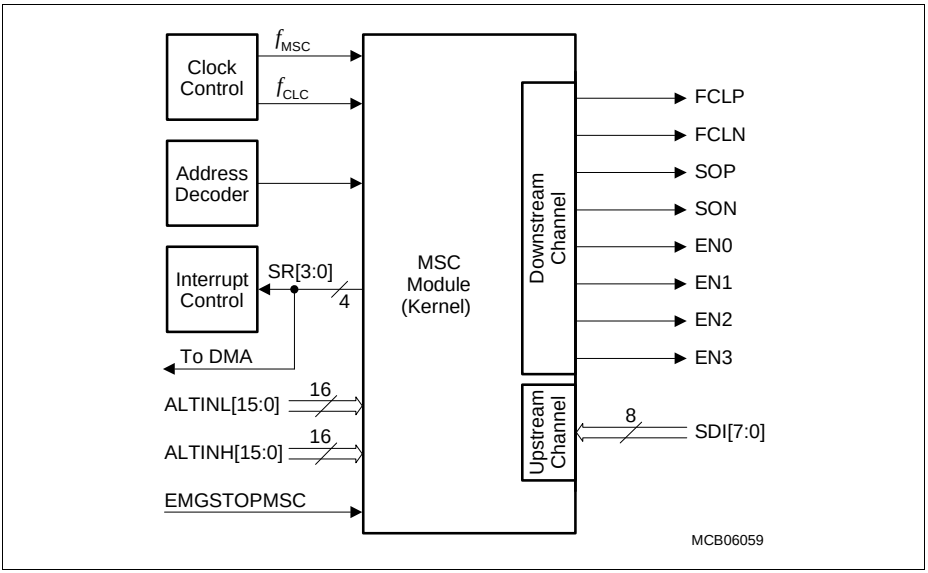


Figure 1-7 General Block Diagram of the MSC Interface

The downstream and upstream channels of the MSC module communicate with the external world via nine I/O lines. Eight output lines are required for the serial communication of the downstream channel (clock, data, and enable signals). One out of eight input lines SDI[7:0] is used as serial data input signal for the upstream channel. The source of the serial data to be transmitted by the downstream channel can be MSC register contents or data that is provided on the ALTINL/ALTINH input lines. These input lines are typically connected with other on-chip peripheral units (for example with a timer unit such as the GPTA). An emergency stop input signal makes it possible to set bits of the serial data stream to dedicated values in an emergency case.

Clock control, address decoding, and interrupt service request control are managed outside the MSC module kernel. Service request outputs are able to trigger an interrupt or a DMA request.

1.4.4.1 Feature List

The Micro Second Bus module provides the following features:

- Fast synchronous serial interface to connect power switches in particular, or other peripheral devices via serial buses
- High-speed synchronous serial transmission on downstream channel
  - Serial output clock frequency: $f_{FCL} = f_{MSC}/2$ (f_{MSCmax} = 110 MHz)
  - Fractional clock divider for precise frequency control of serial clock f_{MSC}
  - Command, data, and passive frame types
  - Start of serial frame: Software-controlled, timer-controlled, or free-running
  - Transmission with or without SEL bit
  - Flexible chip select generation indicates status during serial frame transmission
  - Emergency stop without CPU intervention
- Low-speed asynchronous serial reception on upstream channel
  - Baud rate: f_{MSC} divided by 4, 8, 16, 32, 64, 128, or 256 (f_{MSCmax} = 110 MHz)
  - Standard asynchronous serial frames
  - Programmable upstream data frame length (16 or 12 bits)
  - Parity error checker
  - 8-to-1 input multiplexer for SDI lines
  - Built-in spike filter on SDI lines
- Selectable pin types of downstream channel interface:
  four LVDS differential output drivers or four digital GPIO pins

1.4.5 FlexRay™ Protocol Controller (E-Ray)

The E-Ray IP-module performs communication according to the FlexRay™ [1] protocol specification v2.1. With maximum specified clock the bitrate can be programmed to values up to 10 Mbit/s. Additional bus driver (BD) hardware is required for connection to the physical layer.

1.4.5.1 E-Ray Kernel Description

Figure 1.4.5.1 shows a global view of the E-Ray interface.

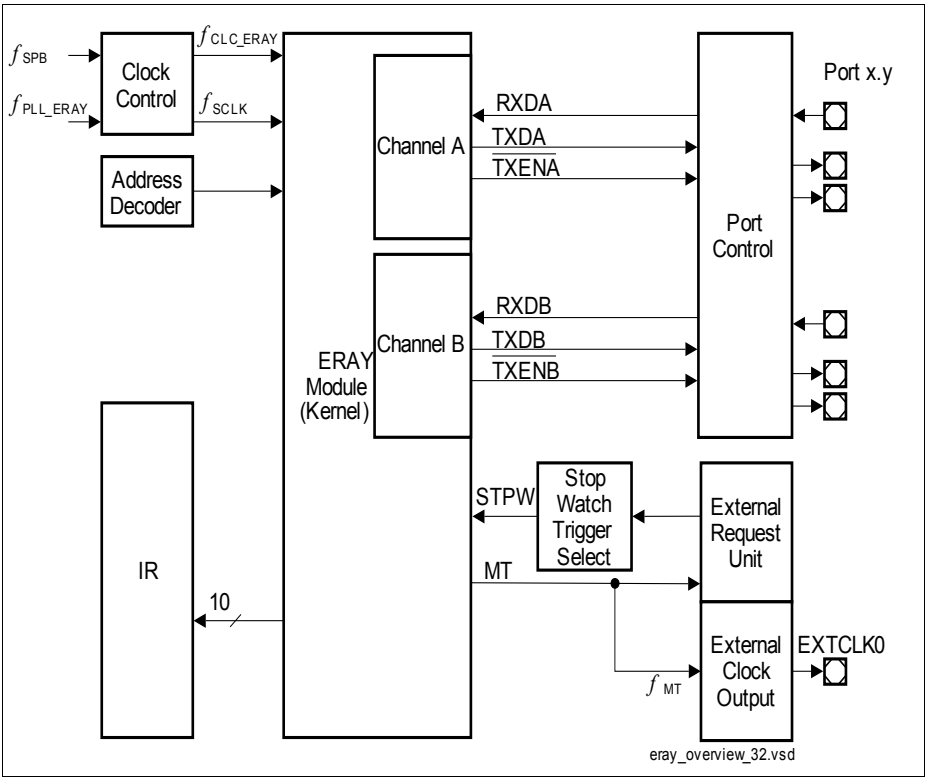


Figure 1-8 General Block Diagram of the E-Ray Interface

1) *Infineon®, Infineon Technologies®, are trademarks of Infineon Technologies AG. FlexRay™* is a trademark of FlexRay Consortium.

The E-Ray module communicates with the external world via three I/O lines each channel. The RXDAx and RXDBx lines are the receive data input signals, TXDA and TXDB lines are the transmit output signals, $\overline{\text{TXENA}}$ and $\overline{\text{TXENB}}$ the transmit enable signals.

Clock control, address decoding, and service request control are managed outside the E-Ray module kernel.

1.4.5.2 Overview

For communication on a FlexRay™ network, individual Message Buffers with up to 254 data byte are configurable. The message storage consists of a single-ported Message RAM that holds up to 128 Message Buffers. All functions concerning the handling of messages are implemented in the Message Handler. Those functions are the acceptance filtering, the transfer of messages between the two FlexRay™ Channel Protocol Controllers and the Message RAM, maintaining the transmission schedule as well as providing message status information.

The register set of the E-Ray IP-module can be accessed directly by an external Host via the module's Host interface. These registers are used to control/configure/monitor the FlexRay™ Channel Protocol Controllers, Message Handler, Global Time Unit, System Universal Control, Frame and Symbol Processing, Network Management, Service Request Control, and to access the Message RAM via Input / Output Buffer.

1.4.5.3 Features List

The E-Ray IP-module provides the following features:

- Conformance with FlexRay™ protocol specification v2.1
- Data rates of up to 10 Mbit/s on each channel
- Up to 128 Message Buffers configurable
- 8 Kbyte of Message RAM for storage of e.g. 128 Message Buffers with max. 48 byte data field or up to 30 Message Buffers with 254 byte Data Sections
- Configuration of Message Buffers with different payload lengths possible
- One configurable receive FIFO
- Each Message Buffer can be configured as receive buffer, as transmit buffer or as part of the receive FIFO
- Host access to Message Buffers via Input and Output Buffer.
  Input Buffer: Holds message to be transferred to the Message RAM
  Output Buffer: Holds message read from the Message RAM
- Filtering for slot counter, cycle counter, and channel
- Maskable module service requests
- Network Management supported
- Four service request lines

- Automatic delayed read access to Output Command Request Register (OBCR) if a data transfer from Message RAM to Output Shadow Buffer (initiated by a previous write access to the OBCR) is ongoing.
- Automatic delayed read access to Input Command Request Register (IBCR) if a data transfer from Input Shadow Buffer to Message RAM to (initiated by a previous write access to the IBCR) is ongoing.
- Four Input Buffer for building up transmission Frames in parallel.
- Flag indicating which Input Buffer is currently accessible by the host.

1.4.6 MultiCAN Controller

The MultiCAN module provides four independent CAN nodes, representing four serial communication interfaces. There is a TTCAN extension available on the node 0. The number of available message objects is 128.

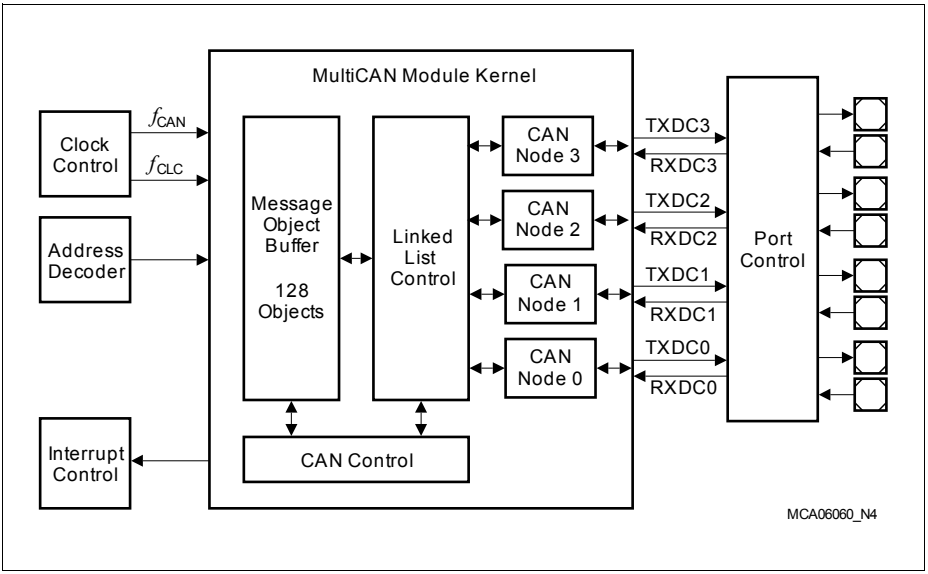


Figure 1-9 Overview of the MultiCAN Module

The MultiCAN module contains four independently operating CAN nodes with Full-CAN functionality that are able to exchange Data and Remote Frames via a gateway function. Transmission and reception of CAN frames is handled in accordance to CAN specification V2.0 B (active). Each CAN node can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers.

All four CAN nodes share a common set of message objects. Each message object can be individually allocated to one of the CAN nodes. Besides serving as a storage container for incoming and outgoing frames, message objects can be combined to build gateways between the CAN nodes or to set up a FIFO buffer.

The message objects are organized in double-chained linked lists, where each CAN node has its own list of message objects. A CAN node stores frames only into message objects that are allocated to the message object list of the CAN node, and it transmits only messages belonging to this message object list. A powerful, command-driven list controller performs all message object list operations.

The bit timings for the CAN nodes are derived from the module timer clock (f_{CAN}) and are programmable up to a data rate of 1 Mbit/s. External bus transceivers are connected to a CAN node via a pair of receive and transmit pins.

1.4.6.1 MultiCAN Feature List

The Mulitican module provides the following features:

- Compliant with ISO 11898
- CAN functionality according to CAN specification V2.0 B active
- Dedicated control registers for each CAN node
- Data transfer rates up to 1 Mbit/s
- Flexible and powerful message transfer control and error handling capabilities
- Advanced CAN bus bit timing analysis and baud rate detection for each CAN node via a frame counter
- Full-CAN functionality: A set of 128 message objects can be individually
  - Allocated (assigned) to any CAN node
  - Configured as transmit or receive object
  - Setup to handle frames with 11-bit or 29-bit identifier
  - Identified by a timestamp via a frame counter
  - Configured to remote monitoring mode
- Advanced Acceptance Filtering
  - Each message object provides an individual acceptance mask to filter incoming frames
  - A message object can be configured to accept standard or extended frames or to accept both standard and extended frames
  - Message objects can be grouped into four priority classes for transmission and reception
  - The selection of the message to be transmitted first can be based on frame identifier, IDE bit and RTR bit according to CAN arbitration rules, or on its order in the list
- Advanced message object functionality
  - Message objects can be combined to build FIFO message buffers of arbitrary size, limited only by the total number of message objects
  - Message objects can be linked to form a gateway that automatically transfers frames between 2 different CAN buses. A single gateway can link any two CAN nodes. An arbitrary number of gateways can be defined
- Advanced data management
  - The message objects are organized in double-chained lists
  - List reorganizations can be performed at any time, even during full operation of the CAN nodes
  - A powerful, command-driven list controller manages the organization of the list structure and ensures consistency of the list

  - Message FIFOs are based on the list structure and can easily be scaled in size during CAN operation
  - Static allocation commands offer compatibility with MultiCAN applications that are not list-based
- Advanced interrupt handling
  - Up to 16 interrupt output lines are available. Interrupt requests can be routed individually to one of the 16 interrupt output lines
  - Message post-processing notifications can be combined flexibly into a dedicated register field of 256 notification bits
- Module internal SRAM with ECC protection

1.4.6.2 TTCAN Feature List

The MultiCAN module provides the following TTCAN features

- Full support of basic cycle and system matrix functionality
- Support of reference messages level 1 and level 2
- Usable as time master
- Arbitration windows supported in time-triggered mode
- Global time information available
- CAN node 0 can be configured either for event-driven or time-triggered mode
- Built-in scheduler mechanism and a timing synchronization unit
- Write protection for scheduler timing data memory
- Timing-related interrupt functionality
- Parity protection for scheduler memory

1.4.7 Micro Link Serial Bus Interface (MLI)

This TC1798 contains two Micro Link Serial Bus Interfaces, MLI0 and MLI1.

The Micro Link Interface (MLI) is a fast synchronous serial interface to exchange data between microcontrollers or other devices, such as stand-alone peripheral components. **Figure 1-10** shows how two microcontrollers are typically connected together via their MLI interfaces.

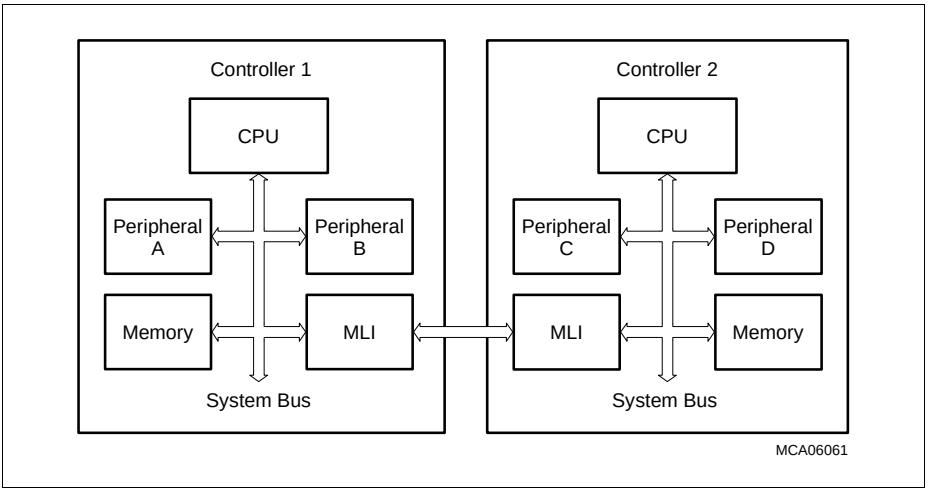


Figure 1-10 Typical Micro Link Interface Connection

1.4.7.1 MLI Feature List

The MLI module provides the following features:

- Synchronous serial communication between an MLI transmitter and an MLI receiver
- Different system clock speeds supported in MLI transmitter and MLI receiver due to full handshake protocol (4 lines between a transmitter and a receiver)
- Fully transparent read/write access supported (= remote programming)
- Complete address range of target device available
- Specific frame protocol to transfer commands, addresses and data
- Error detection by parity bit
- 32-bit, 16-bit, or 8-bit data transfers supported
- Programmable baud rate: $f_{MLI}/2$ (max. $f_{MLI} = f_{FPI}$)
- Address range protection scheme to block unauthorized accesses
- Multiple receiving devices supported

Figure 1-11 shows a general block diagram of the MLI module.

The MLI transmitter and MLI receiver communicate with other MLI receivers and MLI transmitters via a four-line serial connection each. Several I/O lines of these connections are available outside the MLI module kernel as a four-line output or input vector with index numbering A, B, C and D. The MLI module internal I/O control blocks define which signal of a vector is actually taken into account and also allow polarity inversions (to adapt to different physical interconnection means)

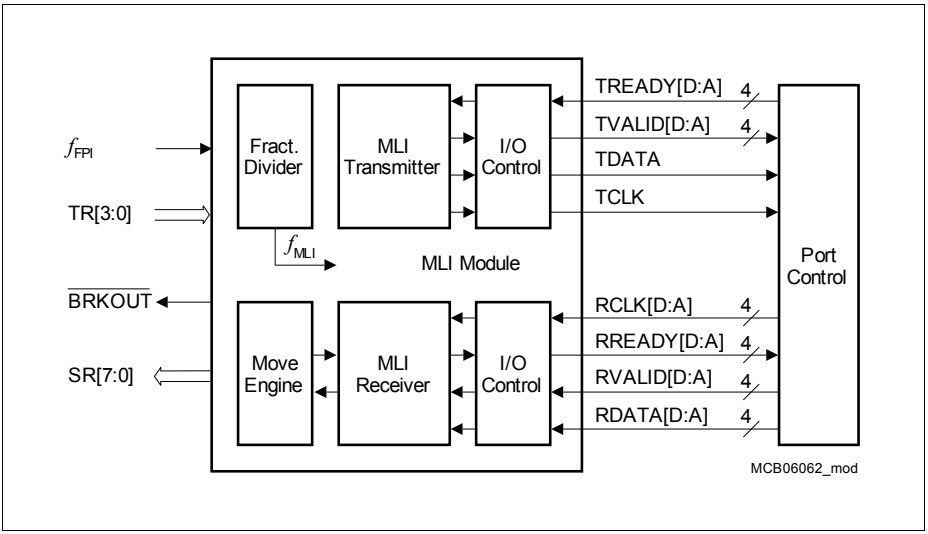


Figure 1-11 General Block Diagram of the MLI Modules

1.4.8 Single Edge Nibble Transmission (SENT)

This chapter describes the SENT Interface of the TC1798.

1.4.8.1 SENT Kernel Description

Figure 1-12 shows a global view of the SENT interface.

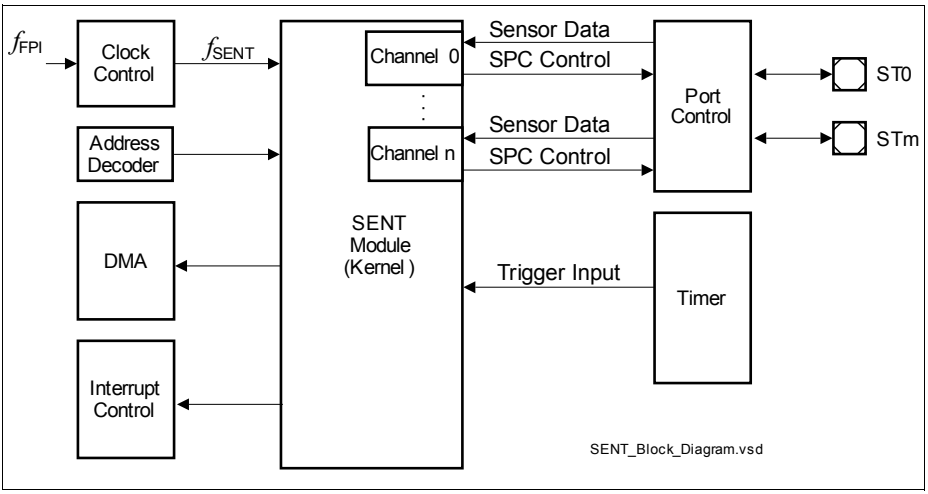


Figure 1-12 General Block Diagram of the SENT Interface

The SENT module communicates with the external world via one I/O line for each channel. The STx lines are the receive data input signals. They overlay ADC inputs. If the optional SPC mode is used, they can be used on a port configured with an open drain transistor. This way the optional SPC data can be transmitted and the line is used bidirectionally. In case of an external transceiver, receive and transmit path can be routed to two different ports.

1.4.9 SENT Feature Overview

The SENT interface provides a serial communication link typically used to connect sensors or other peripheral devices.

Clock control, address decoding, and service request control are managed by the SENT module kernel.

The SENT IP-module performs communication according to the SENT specification J2716 FEB2008.

While staying compliant to this standard, it is able to cover as well the Short PWM Code (SPC) protocol extensions. This enhances the standardized SENT protocol defined by J2716 FEB2008. SPC enables the use of enhanced protocol functionality like “synchronous”, “range selection” and “ID selection” protocol mode.

Receive data on a SENT channel can be set up according to the underlying application. In particular the number of nibbles forming one value is configurable.

The message storage consists of two 32-bit registers for each channel, representing a flexible double buffer system.

In SPC mode, maintaining the sample and transmission schedule as well as providing message status information is support.

The register set of the SENT module can be accessed directly by the CPU for configuration, data read out and status query.

The SENT IP-module supports the following features:

Feature List

The SENT module provides the following features:

- Conformance with SENT protocol specification J2716 FEB2008
- Data rates of up to 65,8 kbit/s at 3 µs tick length and 6 data nibbles on each channel
- Support of standard tick times (3 µs through 90 µs) and
- Message tick time programmable between 1 µs and 90 µs
- 8 SENT channels working independently in parallel
- Status nibble optionally included in the checksum (default not included)
- Sticky interrupt flags, error interrupt optional (default disabled)
- Configurable frame length (default is 24 bit), max data size is 32 bits
- Serial data processing optional (default: disabled)
- Option for bigger frame lengths (must still be fix for each application)
- transparent mode (nibble CRCs are written to the receive control register for SW processing)
- Support of SPC
- Support of trailing Pause Nibble of any length (even longer than 70 ticks)
- Indication of system status: STOP, INITIALIZED, RUNNING, SYNCHRONIZED

- The receiver module will monitor the message for the following error conditions:
  - Calibration pulse length deviates more than +/-25% from the nominal 56 ticks
  - Too many or too few nibbles between calibration pulses.
  - Checksum error.
  - Successive calibration pulse differ by more than 1.5625%
  - Any nibble data values measured as < 0 or >15.
- When any of those errors is detected, the receiver module shall declare that a message error has occurred and ignore the entire message.
- Any of those errors shall cause the receiver to begin searching for a valid calibration pulse to re synchronize.
- Option to enable/disable the check of the next calibration pulse before validation of received data
- Digital Glitch filter suppressing noise
- Buffer overrun detection
- Optional output inversion for use of external open drain transistor
- Optional input inversion for use of external open transistor for level shifting
- Interrupt on status nibble violation
- Programmable Nibble sorting to support LSN or HSN first and relief CPU

1.4.10 General Purpose Timer Array (GPTAv5)

The TC1798 contains the two General Purpose Timer Arrays (GPTA0 and GPTA1) with identical functionality, plus the additional Local Timer Cell Array (LTCA2).

The GPTA provides a set of timer, compare, and capture functionalities that can be flexibly combined to form signal measurement and signal generation units. They are optimized for tasks typical of engine, gearbox, and electrical motor control applications, but can also be used to generate simple and complex signal waveforms required for other industrial applications.

1.4.10.1 GPTA0 and GPTA1 Feature List

The General Purpose Timer Arrays (GPTA0 and GPTA1) each provides a set of hardware modules required for high-speed digital signal processing:

- Filter and Prescaler Cells (FPC) support input noise filtering and prescaler operation.
- Phase Discrimination Logic units (PDL) decode the direction information output by a rotation tracking system.
- Duty Cycle Measurement Cells (DCM) provide pulse-width measurement capabilities.
- A Digital Phase Locked Loop unit (PLL) generates a programmable number of GPTA module clock ticks during an input signal's period.
- Global Timer units (GT) driven by various clock sources are implemented to operate as a time base for the associated Global Timer Cells.
- Global Timer Cells (GTC) can be programmed to capture the contents of a Global Timer on an external or internal event. A GTC may also be used to control an external port pin depending on the result of an internal compare operation. GTCs can be logically concatenated to provide a common external port pin with a complex signal waveform.
- Local Timer Cells (LTC) operating in Timer, Capture, or Compare Mode may also be logically tied together to drive a common external port pin with a complex signal waveform. LTCs – enabled in Timer Mode or Capture Mode – can be clocked or triggered by various external or internal events.
- On-chip Trigger and Gating Signals (OTGS) can be configured to provide trigger or gating signals to integrated peripherals (GPTA0 only).

Input lines can be shared by an LTC and a GTC to trigger their programmed operation simultaneously.

The following list summarizes the specific features of the GPTA units.

Clock Generation Unit

- Filter and Prescaler Cell (FPC)
  – Six independent units

  - Three basic operating modes:
    Prescaler, Delayed Debounce Filter, Immediate Debounce Filter
  - Selectable input sources:
    Port lines, GPTA module clock, FPC output of preceding FPC cell
  - Selectable input clocks:
    GPTA module clock, prescaled GPTA module clock, DCM clock, compensated or uncompensated PLL clock.
  - f_{GPTA}/2 maximum input signal frequency in Filter Modes
- Phase Discriminator Logic (PDL)
  - Two independent units
  - Two operating modes (2- and 3- sensor signals)
  - f_{GPTA}/4 maximum input signal frequency in 2-sensor Mode, f_{GPTA}/6 maximum input signal frequency in 3-sensor Mode
- Duty Cycle Measurement (DCM)
  - Four independent units
  - 0 - 100% margin and time-out handling
  - f_{GPTA} maximum resolution
  - f_{GPTA}/2 maximum input signal frequency
- Digital Phase Locked Loop (PLL)
  - One unit
  - Arbitrary multiplication factor between 1 and 65535
  - f_{GPTA} maximum resolution
  - f_{GPTA}/2 maximum input signal frequency
- Clock Distribution Unit (CDU)
  - One unit
  - Provides nine clock output signals:
    f_{GPTA}, divided f_{GPTA} clocks, FPC1/FPC4 outputs, DCM clock, LTC prescaler clock

Signal Generation Unit

- Global Timers (GT)
  - Two independent units
  - Two operating modes (Free-Running Timer and Reload Timer)
  - 24-bit data width
  - f_{GPTA} maximum resolution
  - f_{GPTA}/2 maximum input signal frequency
- Global Timer Cell (GTC)
  - 32 units related to the Global Timers
  - Two operating modes (Capture, Compare and Capture after Compare)
  - 24-bit data width
  - f_{GPTA} maximum resolution
  - f_{GPTA}/2 maximum input signal frequency
- Local Timer Cell (LTC)

– 64 independent units
– Three basic operating modes (Timer, Capture and Compare) for 63 units
– Special compare modes for one unit
– 16-bit data width
– f_{GPTA} maximum resolution
– f_{GPTA}/2 maximum input signal frequency

Interrupt Sharing Unit

- 143 interrupt sources, generating up to 46 service requests

On-chip Trigger Unit

- 16 on-chip trigger signals

I/O Sharing Unit

- Interconnecting inputs and outputs from internal clocks, FPC, GTC, LTC, ports, and MSC interface

1.4.10.2 LTCA2 Feature List

The Local Timer Cell Array (LTCA2) provides a set of hardware modules required for high-speed digital signal processing:

- Local Timer Cells (LTC) operating in Timer, Capture, or Compare Mode may also be logically tied together to drive a common external port pin with a complex signal waveform. LTCs – enabled in Timer Mode or Capture Mode – can be clocked or triggered by various external or internal events.

The following list summarizes the specific features of the LTCA unit.

The Local Timer Arrays (LTCA2) provides a set of hardware modules required for high-speed digital signal processing:

Signal Generation Unit

- Local Timer Cell (LTC)
  – 64 independent units
  – Three basic operating modes (Timer, Capture and Compare)
  – Special compare modes for one unit
  – 16-bit data width
  – f_{GPTA} maximum resolution
  – f_{GPTA}/2 maximum input signal frequency

I/O Sharing Unit

- Interconnecting inputs and outputs from internal clocks, LTC, ports, and MSC interface

1.4.11 Capture/Compare Unit 6 (CCU6)

The CAPCOM6 provides two independent timers (T12, T13), which can be used for PWM generation, especially for AC-motor control. Additionally, special control modes for block commutation and multi-phase machines are supported.

CCU6061 module consists of CCU60 and CCU61 kernels while CCU6263 consists of CCU62 and CCU63 kernels.

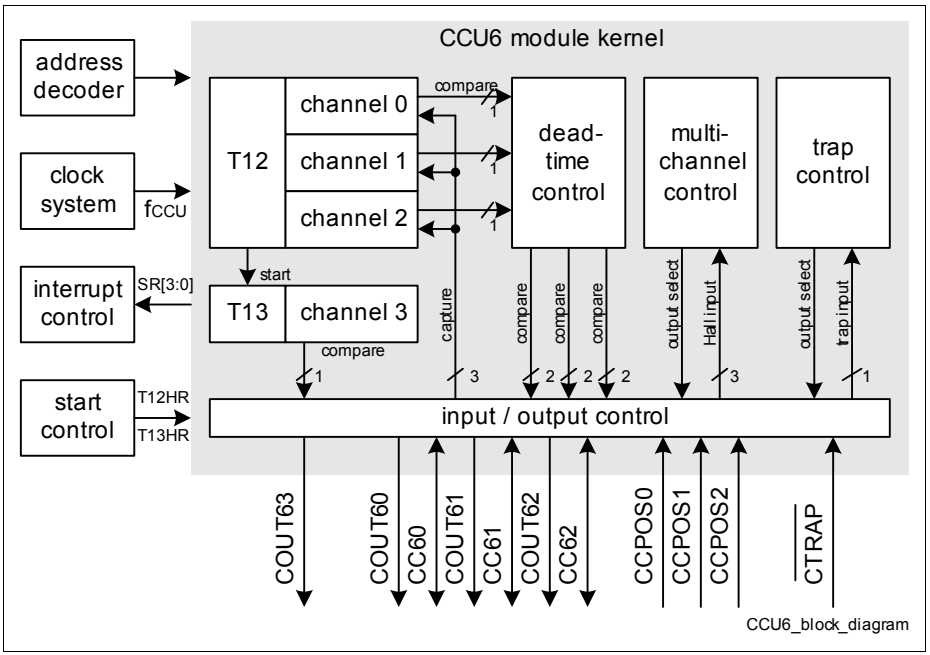


Figure 1-13 CCU6 Block Diagram

1.4.11.1 Feature List

The CCU6 module provides the following features:

Timer 12 Features

- Three capture/compare channels, each channel can be used either as capture or as compare channel.

- Generation of a three-phase PWM supported (six outputs, individual signals for highside and lowside switches)
- 16 bit resolution, maximum count frequency = peripheral input clock
- Dead-time control for each channel to avoid short-circuits in the power stage
- Concurrent update of the required T12/13 registers
- Center-aligned and edge-aligned PWM can be generated
- Single-shot mode supported
- Many interrupt request sources
- Hysteresis-like control mode
- Synchronized start supported (triggered by an external SCU signal through T12HR input for each CCU6 module)

Timer 13 Features

- One independent compare channel with one output
- 16 bit resolution, maximum count frequency = peripheral input clock
- Can be synchronized to T12
- Interrupt generation at period-match and compare-match
- Single-shot mode supported
- Synchronized start supported (triggered by an external SCU signal through T13HR input for each CCU6 module)

Additional Features

- Block commutation for Brushless DC-drives implemented
- Position detection via Hall-sensor pattern
- Automatic rotational speed measurement for block commutation
- Integrated error handling
- Fast emergency stop without CPU load via external signal ($\overline{\text{CTRAP}}$)
- Control modes for multi-channel AC-drives
- Output levels can be selected and adapted to the power stage

The timer T12 can work in capture and/or compare mode for its three channels. The modes can also be combined. The timer T13 can work in compare mode only. The multi-channel control unit generates output patterns which can be modulated by timer T12 and/or timer T13. The modulation sources can be selected and combined for the signal modulation.

1.4.12 General Purpose Timer (GPT12)

The GPT12E unit represents a very flexible multifunctional timer/counter structure which may be used for many different time related tasks such as event timing and counting, pulse width and duty cycle measurements, pulse generation, or pulse multiplication. Its functionality includes enhanced incremental interface modes and clock prescaler support.

1.4.12.1 Feature List

The GPT12E module provides the following features.

- Timer Block GPT1:
  - Maximum resolution peripheral input clock / 4
  - clock prescaler support
  - 3 independent timers/counters (T2, T3, T4).
  - Timers/counters can be concatenated.
  - 4 operating modes (timer, gated timer, counter, incremental).
  - enhanced incremental interface modes
  - Separate interrupt request lines.
- Timer Block GPT2:
  - Maximum resolution peripheral input clock / 2
  - clock prescaler support
  - 2 independent timers/counters (T5, T6).
  - Timers/counters can be concatenated.
  - 3 operating modes (timer, gated timer, counter).
  - Extended capture/reload functions via 16-bit Capture/Reload register CAPREL
  - Separate interrupt request lines.

1.4.13 External Bus Interface (EBU)

The External Bus Unit (EBU) of the TC1798 controls the accesses from the CPU and peripheral units to external memories.

1.4.13.1 Feature List

The EBU module provides the following features:

- 64-bit internal SRI interface
- 32-bit external bus interface
  - interface can be configured to support memory devices with 32 bit, 16 bit and 8 bit databus connections
  - Support for 3.3 V and 2.5 V memory devices
  - Limited support for 1.8 V memories
  - Flexibly programmable access parameters (e.g. control signal pulse width ,bus turnaround time, burst length for synchronous memories).
  - Different Device settings available for read and write accesses
  - Programmable address range for each chip select line.
- Support for multiple device access protocols
  - asynchronous memories e.g. SRAM, peripheral devices
  - synchronous devices e.g. burst NOR flash, PSRAM
  - DDR NOR flash e.g. LPDDR-NVM (Jedec 42.4), ONFI 2.0 (both at limited frequency using 1.8 V I/O supply).
- Scalable external bus timing
  - Derived from SRI frequency (f_{CPU}) by dividers internal to the EBU.
  - Can also be derived from the Flexray clock.
  - Maximum 75 MHz
- Data buffering supported
  - Read/write buffer

1.4.14 Analog-to-Digital Converters (ADC/FADC)

The TC1798 includes Analog to Digital Converter modules)ADC)and one Fast Analog to Digital Converter (FADC).

1.4.15 ADC Module

The analog to digital converter module (ADC) allows the conversion of analog input values into discrete digital values based on the successive approximation method.
This module contains 4 independent kernels (ADC0, ADC1, ADC2, ADC3) that can operate autonomously or can be synchronized to each other. An ADC kernel is a unit used to convert an analog input signal (done by an analog part) and provides means for triggering conversions, data handling and storage (done by a digital part).

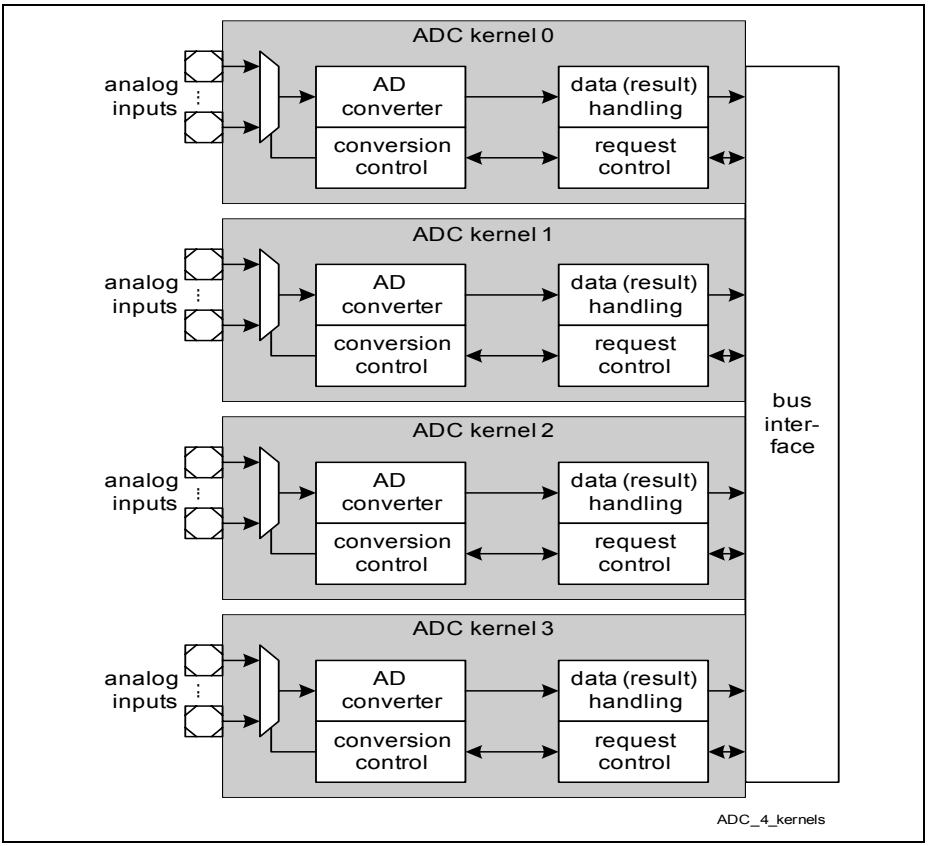


Figure 1-14 ADC Module with four ADC Kernels

1.4.15.1 Feature List

Each ADC kernel provides the following features:

- Analog supply voltage range from 3.3 V (minimum) to 5 V (nominal) for V_{DDM}
- Input voltage range from 0 V to analog supply voltage V_{DDM}
- Input multiplexer for a maximum of 16 possible analog input channels
- One standard reference input (V_{AREF}) and one alternative reference input (CH0) available
- Broken wire detection support for each input channel
- Multiplexer test support for input channels with odd channel numbers
- 5 conversion request sources for external or timer-driven events, auto-scan, programmable sequences, SW-driven conversions, etc.
- Synchronization of the ADC kernels for concurrent conversion starts and parallel sampling and measuring of analog input signals, e.g. for phase current measurements in AC drives
- Control capability for an external analog multiplexer, respecting the additional set up time
- Adjustable sampling times to accommodate output impedance of different analog signal sources (sensors, etc.)
- Possibility to cancel running conversions on demand with automatic restart
- Flexible interrupt generation (possibility of DMA support)
- Limit checking to reduce interrupt load (e.g. for temperature measurements or overload detection, only values exceeding a programmable level lead to an interrupt)
- Programmable data reduction filter, e.g. for digital anti-aliasing filtering, by adding a programmable number of conversion results
- Independent result registers (16 independent registers)
- Support of conversion result FIFO mechanism to allow a longer interrupt latency
- Programmable result data filter providing 3rd order FIR or 1st order IIR filter structure
- Support of suspend and power saving modes
- Individually programmable reference selection for each channel, e.g. to allow measurements of 3.3 V and 5 V signals in the full measurement range with the same ADC kernel (with exception of dedicated channels always referring to V_{AREF})

1.4.16 FADC Module

As shown in **Figure 1-15**, the main FADC functional blocks are:

- An Input Structure containing the differential inputs and impedance control.
- An A/D Converter Stage responsible for the analog-to-digital conversion including an input multiplexer to select between the channel amplifiers
- A Data Reduction Unit containing programmable anti-aliasing and data reduction filters
- A Channel Trigger Control block determining the trigger and gating conditions for the FADC channels

- A Channel Timer for each channel to independently trigger the conversions
- An A/D Control block responsible for the overall FADC functionality

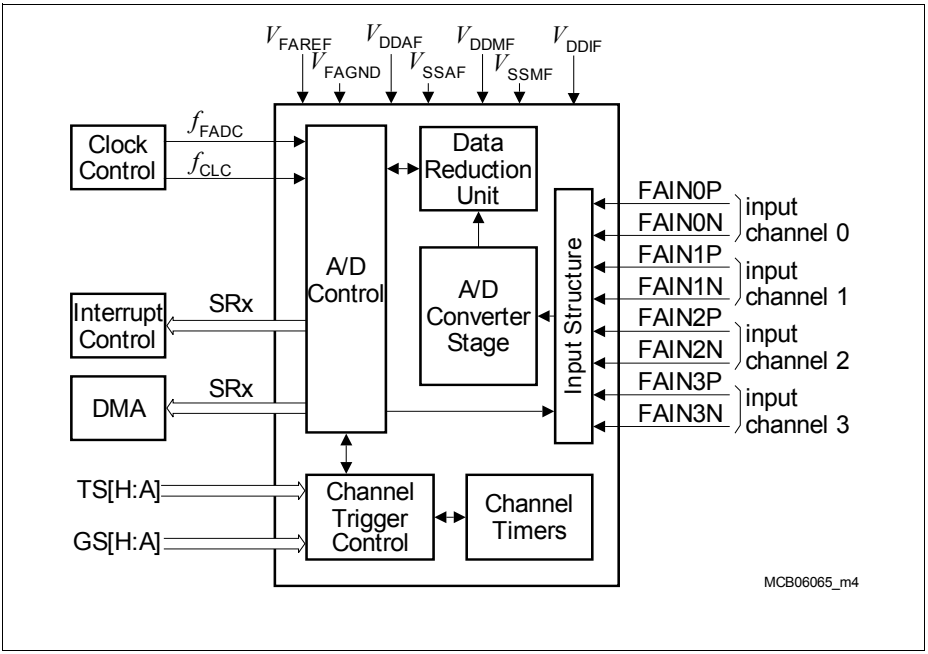


Figure 1-15 Block Diagram of the FADC Module with 4 Input Channels

FADC Power Supply and References

The FADC module is supplied by the following power supply and reference voltage lines:

- V_{DDMF} / V_{SSMF}: FADC Analog Channel Amplifier Power Supply (3.3 V)
- V_{DDIF} / V_{SSMF}: FADC Analog Input Stage Power Supply (3.3 - 5 V), the V_{DDIF} supply does not appear as supply pin, because it is internally connected to the V_{DDM} supply of the ADC that is sharing the FADC input pins.
- V_{DDAF} / V_{SSAF}: FADC Analog Part Power Supply (1.3 V), to be fed in externally
- V_{FAREF} / V_{FAGND}: FADC Reference Voltage (3.3 V max.) and FADC Reference Ground

Input Structure

The input structure of the FADC in the TC1798 contains:

- A differential analog input stage for each input channel to select the input impedance (differential or single-ended measurement) and to decouple the FADC input signal from the pins.
- All input channels are overlaid with ADC1 input signals (AN24 - AN31).

- A channel amplifier for each input channel with a settling time (about 5µs) when changing the characteristics of an input stage (changing between unused, differential, single-ended N, or single-ended P mode).

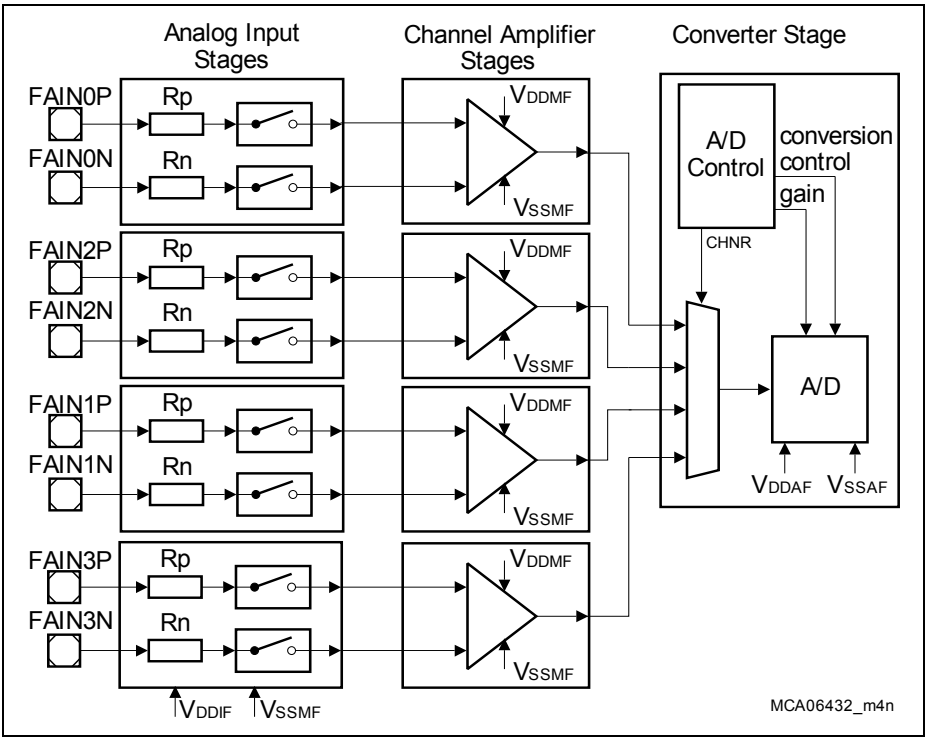


Figure 1-16 FADC Input Structure in TC1798

1.4.16.1 FADC Feature List

The FADC module provides the following features

- Extreme fast conversion, 21 cycles of f_{FADC} clock
- 10-bit A/D conversion (higher resolution can be achieved by averaging of consecutive conversions in digital data reduction filter)
- Successive approximation conversion method
- All differential input channels with impedance control
- All FADC inputs are overlaid with ADC1 inputs
- Each differential input channel can also be used as single-ended input
- Offset calibration support for each channel
- Programmable gain of 1, 2, 4, or 8 for each channel

- Free-running (Channel Timers) or triggered conversion modes
- Trigger and gating control for external signals
- Built-in Channel Timers for internal triggering
- Channel timer request periods independently selectable for each channel
- Selectable, programmable digital anti-aliasing and data reduction filter block with four independent filter units

1.5 On-Chip Debug Support (OCDS)

The TC1798 contains resources for different kinds of “debugging”, covering needs from software development to real-time-tuning. These resources are either embedded in specific modules (e.g. breakpoint logic of the TriCore) or part of a central peripheral (known as CERBERUS).

1.5.1 On-Chip Debug Support

The classic software debug approach (start/stop, single-stepping) is supported by several features labelled “OCDS Level 1”:

- Run/stop and single-step execution independently for TriCore and PCP.
- Means to request all kinds of reset without usage of sideband pins.
- Halt-after-Reset for repeatable debug sessions.
- Different Boot modes to use application software not yet programmed to the Flash.
- A total of eight hardware breakpoints for the TriCore based on instruction or data address.
- TriCore OCDS logic fully independent of the memory protection system.
- Unlimited number of software breakpoints (DEBUG instruction) for TriCore and PCP.
- Debug event generated by access to a specific address via the system peripheral bus or the SRI cross connect.
- Tool access to all SFRs and internal memories independent of the Cores.
- Two central Break Switches to collect debug events from all modules (TriCore, PCP, DMA, SRI, BCU, break input pins) and distribute them selectively to breakable modules (TriCore, PCP, break output pins).
- Central Suspend Switch to suspend parts of the system (TriCore, PCP, Peripherals) instead if breaking them as reaction to a debug event.
- Dedicated interrupt resources to handle debug events inside TriCore (breakpoint trap, software interrupt) and Cerberus (can trigger PCP), e.g. for implementing Monitor programs.
- Access to all OCDS Level 1 resources also for TriCore and PCP themselves for debug tools integrated into the application code.
- Triggered Transfer of data in response to a debug event; if target is programmed to be a device interface simple variable tracing can be done.

- In depth performance analysis and profiling support given by the Emulation Device through MCDS Event Counters driven by a variety of trigger signals (e.g. cache hit, wait state, interrupt accepted).

1.5.2 Real Time Trace

For detailed tracing of the system's behavior a pin-compatible Emulation Device will be available.[1)]

1.5.3 Calibration Support

Two main use cases are catered for by resources in addition the OCDS Level 1 infrastructure: Overlay of non-volatile on-chip memory and non-intrusive signaling:

- On-chip SRAM for Overlay (allocated from LMU RAM pool).
- Can be split into up to 16 blocks which can overlay independent memory regions during data reads (e.g. on-chip Flash).
- Changing the configuration is triggered by a single SFR access to maintain consistency.
- Overlay configuration switch does not require the TriCore to be stopped or suspended.
- Invalidation of the Data Cache (maintaining write-back data) can be done concurrently with the same SFR.
- 768 KB additional Overlay RAM on Emulation Device, shared with the trace functionality.
- A dedicated trigger SFR with 32 independent status bits is provided to centrally post requests from application code to the host computer.
- The host is notified automatically when the trigger SFR is updated by the TriCore or PCP. No polling via a system bus is required.

1.5.4 Tool Interfaces

Three options exist for the communication channel between Tools (e.g. Debugger, Calibration Tool) and TC1798:

- Two wire DAP (Device Access Port) protocol for long connections or noisy environments.
- Four (or five) wire JTAG (IEEE 1149.1) for standardized manufacturing tests.
- CAN (plus software linked into the application code) for low bandwidth deeply embedded purposes.
- DAP and JTAG are clocked by the tool.
- Bit clock up to 40 MHz for JTAG, up to 80 MHz for DAP.

1) The OCDS L2 interface of AudoNG is not available.

- Hot attach (i.e. physical disconnect/reconnect of the host connection without reset of the TC1798) for all interfaces.
- Infineon standard DAS (Device Access Server) implementation for seamless, transparent tool access over any supported interface.
- Lock mechanism to prevent unauthorized tool access to critical application code.

1.5.5 Self-Test Support

Some manufacturing tests can be invoked by the application (e.g. after power-on) if needed:

- Hardware-accelerated checksum calculation (e.g. for Flash content).
- RAM tests optimized for the implemented architecture.

1.5.6 FAR Support

To efficiently locate and identify faults after integration of a TC1798 into a system special functions are available:

- Boundary Scan (IEEE 1149.1) via JTAG and DAP.
- SSCM (Single Scan Chain Mode) for structural scan testing of the chip itself.
- SPD (Single Pin DAP) protocol via CAN0 pins.

2 CPU Subsystem

The TC1798 processor contains a TriCore 1.6 CPU. This chapter describes the implementation-specific options of the CPU, and should be read in conjunction with the TriCore Architecture Manual, which describes the complete TriCore Architecture including the register and instruction set.

2.1 TC1798 Processor Subsystem

The diagram below shows the block diagram of the processor subsystem.

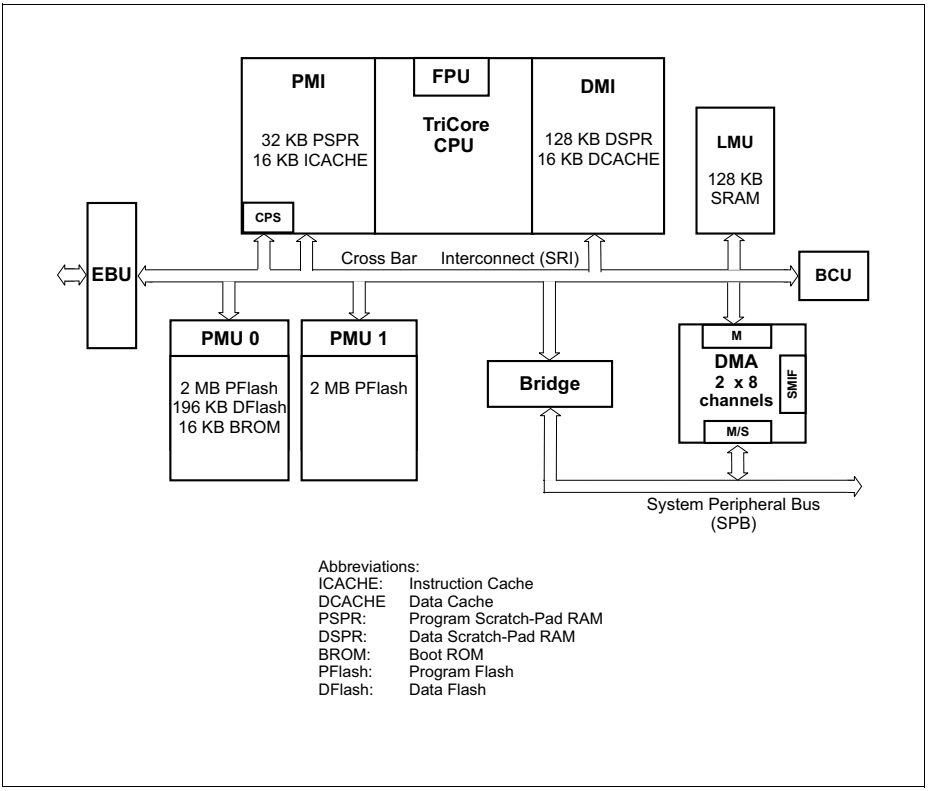


Figure 2-1 TC1798 Processor Subsystem Block Diagram

2.2 Central Processing Unit Features

The 330 MHz TriCore TC1798 CPU includes:

Architecture

- 32-bit load store architecture
- 4 Gbyte address range (2^{32})
- 16-bit and 32-bit instructions for reduced code size
- Data types:
  - Boolean, integer with saturation, bit array, signed fraction, character, double-word integers, signed integer, unsigned integer, IEEE-754 single-precision floating point
- Data formats:
  - Bit, byte (8-bits), half-word (16-bits), word (32-bits), double-word (64-bits)
- Byte and bit addressing
- Little-endian byte ordering for data, memory and CPU registers
- Multiply and Accumulate (MAC) instructions: Dual 16×16, 16×32, 32×32
- Saturation integer arithmetic
- Packed data
- Addressing modes:
  - Absolute, circular, bit reverse, long + short, base + offset with pre- and post-update
- Instruction types:
  - Arithmetic, address arithmetic, comparison, address comparison, logical, MAC, shift, coprocessor, bit logical, branch, bit field, load/store, packed data, system
- General Purpose Register Set (GPRS):
  - Sixteen 32-bit data registers
  - Sixteen 32-bit address registers
  - Three 32-bit status and program counter registers (PSW, PC, PCXI)
- Core Debug support (OCDS):
  - Level 1, supported in conjunction with the CPS block
  - Level 3, supported in conjunction with the MCDS block (Emulation Device only).
- Flexible memory protection system providing multiple protection sets with multiple protection ranges per set.
- Temporal protection system allowing time bounded real time operation.

Implementation

- Most instructions executed in 1 cycle
- Branch instructions in 1, 2 or 3 cycles (using branch prediction)
- Wide memory interface for fast context switch
- Automatic context save-on-entry and restore-on-exit for: subroutine, interrupt, trap
- Four memory protection register sets
- Dual instruction issuing (in parallel into Integer Pipeline and Load/Store Pipeline)
- Third pipeline for loop instruction only (zero overhead loop)

- Single precision Floating Point Unit
- Dedicated Integer divide unit

2.2.1 CPU Diagram

The Central Processing Unit (CPU) comprises of an Instruction Fetch Unit, an Execution Unit, a General Purpose Register File (GPR), a CPU Slave interface (CPS), and Floating Point Unit (FPU).

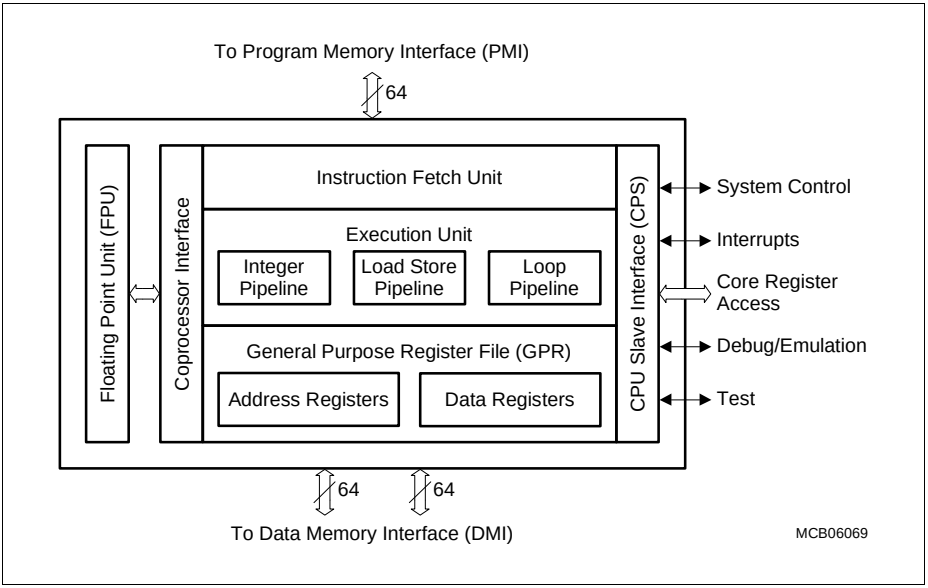


Figure 2-2 CPU Block Diagram

2.2.2 Instruction Fetch Unit

The Instruction Fetch Unit pre-fetches and aligns incoming instructions from the 64-bit wide Program Memory Interface (PMI). Instructions are placed in predicted program order in the Issue fifo. The Issue fifo buffers up to six instructions and directs the instruction to the appropriate execution pipeline.

The Instruction Protection Unit checks the validity of accesses to the PMI and the integrity of incoming instructions fetched from the PMI.

The branch unit examines the fetched instructions for branch conditions and predicts the most likely execution path based on previous branch behavior. The Program Counter Unit (PC) is responsible for updating the program counters.

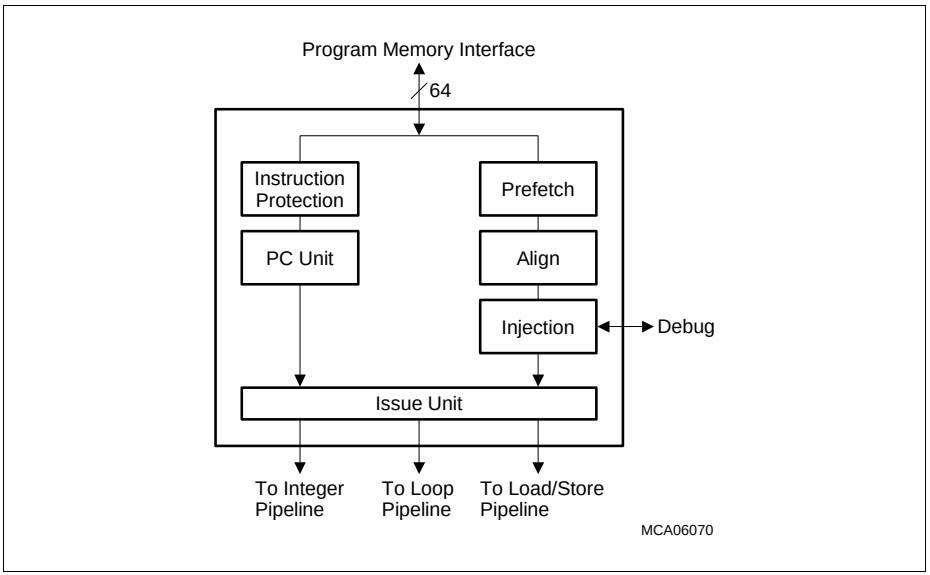


Figure 2-3 Instruction Fetch Unit

2.2.3 Execution Unit

The Execution Unit contains the Integer Pipeline, the Load/Store Pipeline and the Loop Pipeline. All three pipelines operate in parallel, permitting up to three instructions to be executed in one clock cycle. In the execution unit all instructions pass through a decode stage followed by two execute stages. Pipeline hazards (stalls) are minimised by the use of forwarding paths between pipeline stages allowing the results of one instruction to be used by a following instruction as soon as the result becomes available.

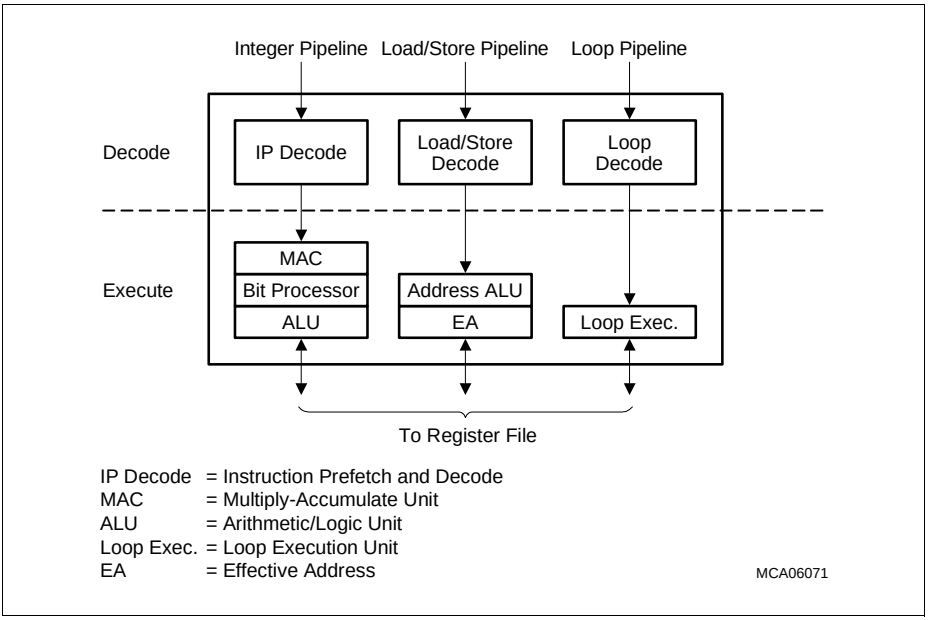


Figure 2-4 Execution Unit

2.2.4 General Purpose Register File

The CPU has a General Purpose Register (GPR) file, divided into an Address Register File (registers A0 through A15) and a Data Register File (registers D0 through D15).

The data flow for instructions issued to the Load/Store Pipeline is steered through the Address Register File.

The data flow for instructions issued to/from the Integer Pipeline and for data load/store instructions issued to the Load/Store Pipeline is steered through the Data Register File.

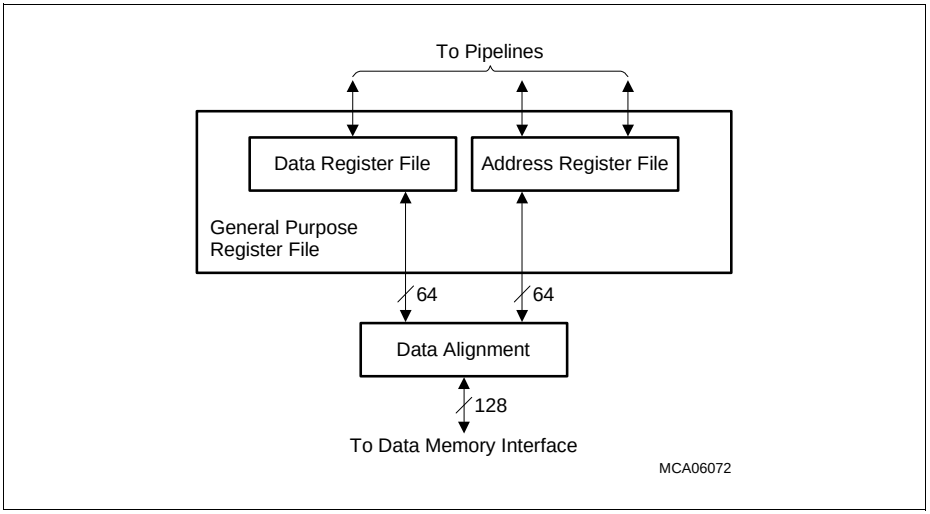


Figure 2-5 General Purpose Register File

2.3 Summary of functional changes from TC1.3.1

To achieve higher frequencies the TriCore1.6 pipeline is increased from 4 to 6 stages.

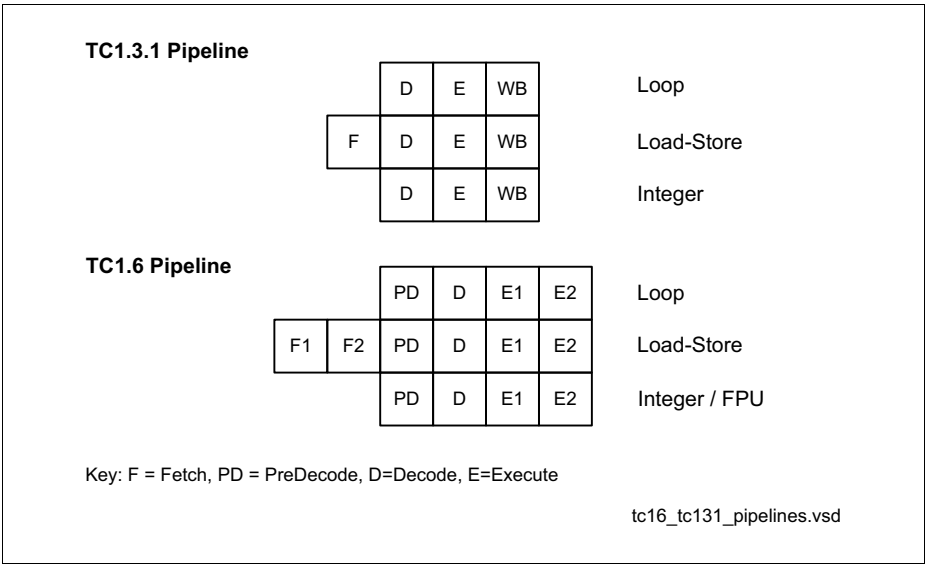


Figure 2-6 TC1.6 and TC1.3.1 Pipelines

To mitigate the effects on performance of the longer pipeline the following fetch and branch features are implemented.

- FIFO decoupled fetch and execute stages.
- Dynamic branch prediction using combined bimodal predictor table and branch target buffer.
- Loop aware branch prediction.

One effect of the longer pipeline is to increase the load-use penalty to 1 from 0. This necessitates re-scheduling of code to achieve optimum performance.

Other significant adaptations to the existing TC1.3.1 CPU are as follows:

- Fully Pipelined Floating Point Unit (FPU)
  – Most floating point instructions now have a repeat rate of 1
- Improved debug system - now decoupled from protection system.
  – 8 comparators proving up to 4 ranges, selectable for PC or load-store address
- Expanded and enhanced memory protection unit (MPU)
  – 16 data ranges and 8 code ranges shared between 4 protection sets.
- New Temporal protection system.

  - Guards against task runtime overrun.
- New Safe Interrupt mode.
  - Interrupt acknowledge decoupled from interrupt entry.
- New instructions for improved Interrupt and Data Cache manipulation support.
  - Disable, restore, CACHEI.I
- New instructions for Fast Integer Divide
  - DIV, DIV.U
- New Instructions for fast call and return with minimal saving of state.
  - FCALL, FCALLA, FCALLI, FRET
- Long offset addressing mode introduced for byte, half word and address accesses.
  - LD.BU, LD.B, LD.HU, LD.H, ST.B, ST.H, ST.A
- Extended range of 16 bit jumps
  - JEQ, JNE
- Increased flexibility in the system address map.
- Full SECDED ECC protection for all scratch, cache and tag memory structures.
- Cache and Scratch memory systems now entirely separated.
  - Cache memories may be mapped as additional scratch.

2.4 CPU Implementation-Specific Features

This section describes the implementation-specific features of the CPU. For a complete description of all registers, refer to the TriCore Architecture Manual.

2.4.1 Context Save Areas

Context Save Areas (CSA) may be placed in DSPR or external memory (cached or uncached).

The CPU uses a uniform context-switching method for function calls, interrupts and traps. In all cases the Upper Context of the task is automatically saved and restored by hardware. Saving and restoring of the Lower Context may be optionally performed by software.

CSA Placement in DSPR

The actual timing of context operations is dependent upon the placement of the Context Save Areas. Maximum performance is achieved when the Context Save Area is placed in DSPR. In this case all context save and restores operations take four cycles.

CSA Placement in Cached External Memory

In this case, the timing is also dependent on the state of the Data Cache. The best case Data Cache operation occurs when context saves do not incur a cache line writeback, and context restores hit in the data cache. In this case all context saves and restores take eight cycles.

2.4.2 Program Counter (PC) Register

The Program Counter (PC) holds the address of the instruction that is currently fetched and forwarded to the CPU pipelines. The CPU handles updates of the PC automatically.

Software can use the current value of the PC for various tasks, such as performing code address calculations. Reading the PC through software executed by the CPU must only be done with an MFCR instruction. Such a read will return the PC of the MFCR instruction itself. Explicit writes to the PC through an MTCR instruction must not be done due to possible unexpected behavior of the CPU.

The CPU must not perform Load/Store instructions to the mapped address of the PC in Segment 15. A MEM trap will be generated in such a case. Bit 0 of the PC register is read-only and hard-wired to 0.

2.4.3 Store Buffers

To increase performance the TC1.6 CPU implements store buffering to decouple memory write operations from CPU instruction execution. All stores from the CPU are placed in the store buffer prior to being written to local memory or transferred via the bus

system. Write data is taken from the store buffers and written to memory when the target memory or bus interface becomes available. In normal operation the CPU will prioritise memory load operations over store operations in order to improve performance unless:-

- The store buffer is full.
- The load is to peripheral space and a store to peripheral space exists in the store buffer. (In order peripheral space access).
- The load or store is part of an atomic operation.

Typically the operation of the store buffer is invisible to the end user. If there is a requirement that data is written to memory prior to execution of a subsequent instruction then a DSYNC instruction may be used to flush the store buffers.

To further improve performance consecutive byte writes to the same half word location are merged in the store buffer.

The TC1.6 CPU store buffer can hold the data for up to 6 stores.

Store buffer operation may be disabled be setting the SMACON.IODT bit. This should not be done in normal execution as it will severely limit performance.

2.4.4 Interrupt System

An interrupt request can be generated by the on-chip peripheral units, or it can be generated by external events. Requests can be targeted to either the CPU, or to the Peripheral Control Processor (PCP).

The interrupt system evaluates service requests for priority and to identify whether the CPU (or PCP) should receive the request. The highest-priority service request is then presented to the CPU (or PCP) by way of an interrupt.

The term “interrupt” is used generally to mean an event directed to the CPU, while the term “service request” describes an event that can be directed to either the CPU or the PCP.

2.4.4.1 Interrupt Acknowledge Decoupling for Safety Systems

In order to improve plausibility checks on Interrupt Service Routines (ISR) a modification to the Interrupt Controller (ICU) is introduced.

When an interrupt service request node (SRN) is arbitrated the ICU sends an acknowledge indicating which SRN is the winner. Upon reception of the information the winner SRN automatically clears the request flag. This happens before the ISR executes. Therefore the ISR can't directly double check if the node corresponding to it's interrupt level was active or not.

The TriCore1.6 implements a new mode where the feedback after an arbitration round is controlled by software, allowing an ISR to make consistency checks and then enabling the ICU to proceed with terminating the arbitration round and enabling further interrupts.

On Entering an interrupt the BIT SAFEINT.INT (0xFE30, bit-0) is set. The CPU holds off acknowledging the interrupt until this bit is cleared by a software write. Note that this delays re-arbitration and hence will impact interrupt performance.

Interrupt acknowledge decoupling is enabled by the COMPAT.INT bit. By default the standard, non-decoupled solution is selected.

2.4.5 Trap System

The following traps have implementation-specific properties.

UOPC - Unimplemented Opcode (TIN 2)

The UOPC trap is raised on optional MMU instructions, coprocessor two and coprocessor three instructions.

OPD - Invalid Operand (TIN 3)

The CPU raised OPD traps for instructions that take even-odd register pairs as an operand where if the operand specifier is odd.

DSE - Data Access Synchronous Error (TIN 2)

The Data Access Synchronous Bus Error (DSE) trap is generated by the DMI module when a load access from the CPU encounters certain error conditions, such as a Bus error, or an out-of-range access to DSPR. When a DSE trap is generated, the exact cause of the error can be determined by reading the Data Synchronous Trap Register, DSTR. For details of possible error conditions and the corresponding flag bits in DSTR, see **“DMI Trap Generation” on Page 2-90**.

DAE - Data Access Asynchronous Error (TIN 3)

The Data Access Asynchronous Error Trap (DAE) is generated by the DMI module when a store or cache management access from the CPU encounters certain error conditions, such as an Bus error. When a DAE trap is generated, the exact cause of the error can be determined by reading the Data Asynchronous Trap Register, DATR. For details of possible error conditions and the corresponding flag bits in DATR, see **“DMI Trap Generation” on Page 2-90**.

PIE Program Memory Integrity Error (TIN 5)

The PIE trap is raised whenever an uncorrectable memory integrity error is detected in an instruction fetch from a local memory. The trap is synchronous to the erroneous instruction. The trap is of Class-4 and has a TIN of 5.

Program memories are protected from memory integrity errors on a 64 bit basis. A PIE trap is raised when an attempt is made to execute an instruction from any 64bit fetch group containing a memory integrity error.

The PIEAR and PIETR registers may be interrogated to determine the source of any error more precisely.

DIE Data Memory Integrity Error (TIN 6)

The DIE trap is raised whenever an uncorrectable memory integrity error is detected in a data access to a local memory. The trap is of Class-4 and has a TIN of 6.

DIE traps are always asynchronous independent of the operation which encountered the error.

A DIE trap is raised if any memory half word accessed by a load/store operation contains an uncorrectable error. The DIEAR and DIETR registers may be interrogated to determine the source of any error more precisely.

2.4.6 Memory Integrity Error Handling

The TriCore 1.6 contains integrated support for the detection and handling of memory integrity errors. The handling of memory integrity errors for the various memory types in TriCore 1.6 is as follows:

2.4.6.1 Program Side Memories

The program side memories of the TriCore 1.6 core consist of two independent memory structures:- The Program Scratchpad RAM (PSPR) and Instruction Cache (ICACHE). Both memory structures are ECC protected from memory integrity errors on a 64bit basis with ECC calculated across both address and data. Any sub-64bit write access to the PSPR from the Bus interface is converted to a 64bit Read-Modify-Write sequence by the PMI module.

Program Scratchpad RAM (PSPR)

The Scratchpad RAM of TriCore 1.6 is protected from memory integrity errors on a 64bit basis with ECC calculated across address and data. Eight ECC bits are required per 64 bits stored.

Uncorrectable memory integrity error detection in the PSPR is enabled by setting MIECON.PSMIEE to one. When MIECON.PSMIEE is zero all uncorrectable memory integrity errors are ignored. Error correction is enabled by setting the MIECON2.PSMSECE to one. When the MIECON2.PSMSECE is zero all errors are treated as uncorrectable. If a correctable error is detected during a memory read and error correction is enabled via the MIECON2.PSMSECE then the read data will be corrected and the CCPIER.CCPIE_U counter incremented to record the fact the an unresolved correctable program integrity error has been detected. (The error is considered unresolved as the memory itself is not updated with the corrected value).

For instruction fetch requests from the TriCore CPU to PSPR, the ECC bits are read along with the data bits and are passed to the CPU along with their corresponding instructions. Whenever an attempt is made to issue an instruction containing an uncorrectable memory integrity error a synchronous PIE trap is raised. The trap handler is then responsible for correcting the memory entry and re-starting program execution.

For PSPR read operations from the Bus interface, either from the DMI module or another Bus master agent, an access that results in the detection of an uncorrectable memory integrity error in the requested data causes a bus error to be returned for the bus transaction. Since the TriCore CPU may not be involved in the transaction, a separate error is also flagged to the SCU module to optionally generate an NMI trap back to the core.

Writes to program scratchpad memory are only ever performed from the bus interface. For write operations of 64bit size or greater, the ECC bit values are pre-computed based on the 64-bit granularity and written to the scratch memory in parallel with the data. For sub 64bit write operations the memory transaction is transformed into a 64bit read-modify-write sequence inside the PMI module. As such, sub-64 bit write operations may result in the detection of uncorrectable memory integrity errors, which are handled as standard read operations.

Instruction Cache (ICACHE)

The Scratchpad RAM of TriCore 1.6 is protected from memory integrity errors on a 64bit basis with ECC calculated across address and data. The instruction cache stores eight ECC bits per 64 bits.

Uncorrectable memory integrity error detection in the ICache is enabled by setting MIECON.PCMIEE to one. When MIECON.PCMIEE is zero all uncorrectable memory integrity errors are ignored. Error correction is enabled by setting the MIECON2.PCMSECE to one. When the MIECON2.PCMSECE is zero all errors are treated as uncorrectable. If a correctable error is detected during a memory read and error correction is enabled via the MIECON2.PCMSECE then the read data will be corrected and the CCPIER.CCPIE_U counter incremented to record the fact the an unresolved correctable program integrity error has been detected. (The error is considered unresolved as the memory itself is not updated with the corrected value).

For instruction fetch requests from the TriCore CPU to ICACHE, the ECC bits are read along with the data bits of all cache ways, and an uncorrectable error signal generated for each 64 bits of each cache way. In the case of a tag hit, the uncorrectable error signals for the corresponding cache way are passed to the core along with their corresponding instructions. Whenever an attempt is made to issue an instruction containing an uncorrectable error a synchronous PIE trap is raised. The trap handler is then responsible for checking the source of the memory integrity error.

Program Tag (PTag)

The program tag stores a 21-bit tag field for each of the cache ways in a set. As such the program tag is written with 21-bit granularity and six ECC bits are associated with each 21-bit tag way.

Uncorrectable memory integrity error detection in the PTAG is enabled by setting MIECON.PTMIEE to one. When MIECON.PTMIEE is zero all uncorrectable memory integrity errors are ignored. Error correction is enabled by setting the MIECON2.PTMSECE to one. When the MIECON2.PTMSECE is zero all errors are treated as uncorrectable. If a correctable error is detected during a memory read and error correction is enabled via the MIECON2.PTMSECE then the read data will be corrected and the CCPIER.CCPIE_U counter incremented to record the fact the an unresolved correctable program integrity error has been detected. (The error is considered unresolved as the memory itself is not updated with the corrected value).

For instruction fetch requests from the TriCore CPU to ICACHE, the program tag ECC bits are read along with the data bits and an error flag is computed. A way hit is triggered only if the tag address comparison succeeds, the valid bit is set and no ECC error in the associated tag way is detected, any other result is considered a miss. In the normal case where no error is detected in either cache way then the cache line is filled/refilled as normal. In the case where an error is detected the cache controller replacement algorithm forces the way indicating an error to be replaced. Since such errors are

otherwise transparent to the TriCore CPU, the CCPIE_R counter is incremented to allow counting of such error corrections if required. In the case where one cache way flags a cache hit, and another cache way detects an uncorrectable ECC error, the error condition is masked and has no effect on the memory integrity error handling mechanisms.

2.4.6.2 Data Side Memories

The data side memories of the TriCore 1.6 core consist of two separate memory structures:- The Data Scratchpad RAM (DSPR) and Data Cache (DCache). Both memory structures are ECC protected from memory integrity errors on a per-half word basis. Any byte write access to either DSPR or DCache is converted to a halfword Read-Modify-Write sequence. The transformation of such byte accesses to atomic sequences is performed within the DMI rather than the CPU core itself. In normal operation isolated byte write transactions to the data memories result in no additional stall cycles.

Data Scratchpad Ram (DSPR)

The DSPR of TriCore 1.6 is protected from memory integrity errors on a per-halfword basis. The DSPR is ECC protected, six ECC bits are required per half-word stored.

Uncorrectable memory integrity error detection in the DSPR is enabled by setting MIECON.DSMIEE to one. When MIECON.DSMIEE is zero all uncorrectable memory integrity errors are ignored. Error correction is enabled by setting the MIECON2.DSMSECE to one. When the MIECON2.DSMSECE is zero all errors are treated as uncorrectable. If a correctable error is detected during a memory read and error correction is enabled via the MIECON2.DSMSECE then the read data will be corrected and the CCPIER.CCDIE_U counter incremented to record the fact the an unresolved correctable data integrity error has been detected. (The error is considered unresolved as the memory itself is not updated with the corrected value).

For data load requests from the TriCore CPU to DSPR, the ECC bits are read along with the data bits and an uncorrectable error signal is generated for each half-word. If an error is detected associated with any of the data half-words passed to the core an error is flagged to the core. If such an error condition is detected an asynchronous DIE trap is raised. The trap handler is then responsible for correcting the memory entry, or for taking alternative action (such as system soft reset) if correction of the data is not possible.

For DSPR read operations from the Bus interface, either from the PMI module or another Bus master agent, an access that results in the detection of an uncorrectable error in the requested data half-words causes a bus error to be returned for the bus transaction. Since the TriCore CPU may not be involved in the transaction, a separate error is also flagged to the SCU module to optionally generate an NMI trap back to the core.

For write operations to DSPR of half-word size or greater, the ECC bits are pre-calculated and written to the memory in parallel with the data bits. For byte write operations the memory transaction is transformed into a half-word read-modify-write

sequence inside the DMI module. As such, byte write operations may result in the detection of uncorrectable memory integrity errors, which are handled as per standard read operations.

Data Cache (DCache)

The data cache stores six ECC bits per half-word.

Uncorrectable memory integrity error detection in the DCache is enabled by setting MIECON.DCMIEE to one. When MIECON.DCMIEE is zero all uncorrectable memory integrity errors are ignored. Error correction is enabled by setting the MIECON2.DCMSECE to one. When the MIECON2.DCMSECE is zero all errors are treated as uncorrectable. If a correctable error is detected during a memory read and error correction is enabled via the MIECON2.DCMSECE then the read data will be corrected and the CCPIER.CCDIE_U counter incremented to record the fact the an unresolved correctable data integrity error has been detected. (The error is considered unresolved as the memory itself is not updated with the corrected value).

For data load requests from the TriCore CPU to DCache, the ECC bits are read along with the data bits of both cache ways, and an uncorrectable error flag computed for each half-word of each cache way. In the case where an error is detected with any of the requested data half-words in a cache way which has a corresponding tag hit, an error is flagged to the core. If such an error condition is detected an asynchronous DIE trap is raised. The trap handler is then responsible for correcting the memory entry, or for taking alternative action (such as system soft reset) if correction of the data is not possible.

For write operations of half-word size or greater, the check bits are pre-calculated and written to the memory in parallel with the data bits. For byte write operations the memory transaction is transformed into a half-word read-modify-write sequence inside the DMI module. As such, byte write operations may result in the detection of uncorrectable memory integrity errors as for read operations.

For cache line writeback, uncorrectable error detection is performed as dirty data is transferred to the store buffers. In all cases (normal cache line eviction, cachex.xx instruction) where an error condition is detected in a valid cache line a DIE trap is raised. The trap handler is then responsible for taking corrective action (such as system soft reset) since correction of the data is not possible.

Data Tag (DTag)

The data tag stores a 20-bit tag address for each cache way in a set. As such the data tags are written with 20-bit granularity and six ECC bits are associated with each 20-bit tag address.

Uncorrectable memory integrity error detection in the DTAG is enabled by setting MIECON.DTMIEE to one. When MIECON.DTMIEE is zero all uncorrectable memory integrity errors are ignored. Error correction is enabled by setting the

MIECON2.DTMSECE to one. When the MIECON2.DTMSECE is zero all errors are treated as uncorrectable. If a correctable error is detected during a memory read and error correction is enabled via the MIECON2.DTMSECE then the read data will be corrected and the CCPIER.CCDIE_U counter incremented to record the fact the an unresolved correctable data integrity error has been detected. (The error is considered unresolved as the memory itself is not updated with the corrected value).

For data load or store requests from the TriCore CPU to DCache, the data tag ECC bits are read along with the data bits and an uncorrectable error flag is computed. A way hit is triggered only if the tag address comparison succeeds, the tag location is valid and no uncorrectable error in the associated tag way is detected, any other result is considered a miss. In the normal case where no error is detected in either tag way then the cache line is filled/refilled as normal. In the case of a cache miss where an error is detected in one of the tag ways and the cache line does not contain dirty data the cache controller replacement algorithm forces the way indicating an error to be replaced when the refill operation returns. Since such errors are otherwise transparent to the TriCore CPU, the CCDIE_R counter is incremented to allow counting of such error corrections if required. In the case where one cache way flags a cache hit, and the another way detects an uncorrectable error, the error condition is masked and has no effect on the memory integrity error handling mechanisms. If a cache miss occurs, with an uncorrectable error detected on the associated data tag way and dirty data detected, then an asynchronous DIE trap is signalled to the core and any writeback / refill sequence aborted. The trap handler is responsible for invalidating the cache line and processing any associated dirty data if possible, or taking other corrective action. Similar action is taken for forced cache writeback using the cache manipulation instructions.

2.5 CPU Subsystem Registers

This section describes the implementation-specific features of the CPU Subsystem registers listed in **Table 2-1**. For complete descriptions of all registers refer to the TriCore Architecture Manual.

Table 2-1 CPU Subsystem Registers

Registers	Purpose	Description
CPU Core Special Function Registers (CSFRs)	Program state information, context and stack management, interrupt and trap control, system control	see **Page 2-20**
CPU General Purpose Registers (GPRs)	General Purpose Address and Data Registers	see **Page 2-30**
CPU Memory Protection Registers (CSFRs)	Memory protection control and mode selection	see **Page 2-33**
FPU Registers (CSFRs)	Support for the standard floating point instructions.	see **Page 2-38**
Memory Integrity Registers (CSFRs)	Integrity and Protection Core Special Function Registers.	see **Page 2-40**
CPU Slave Interface (CPS) Registers	Software break control and software service request control	see **Page 2-59**
Core Debug Registers (CSFRs)	Debug control	see **Page 2-62**
Implementation Specific Reset Values	Reset values for CPU registers not defined in this chapter	see **Page 2-65**
Program Memory Interface Registers (PMI CSFRs)	PMI instruction cache control, status and trap information	see **Page 2-82**
Data Memory Interface Registers (DMI CSFRs)	DMI data cache control, status and trap information	see **Page 2-93**

2.6 CPU Core Special Function Registers (CSFR)

Figure 2-7 shows the CSFR registers of the TC1798.

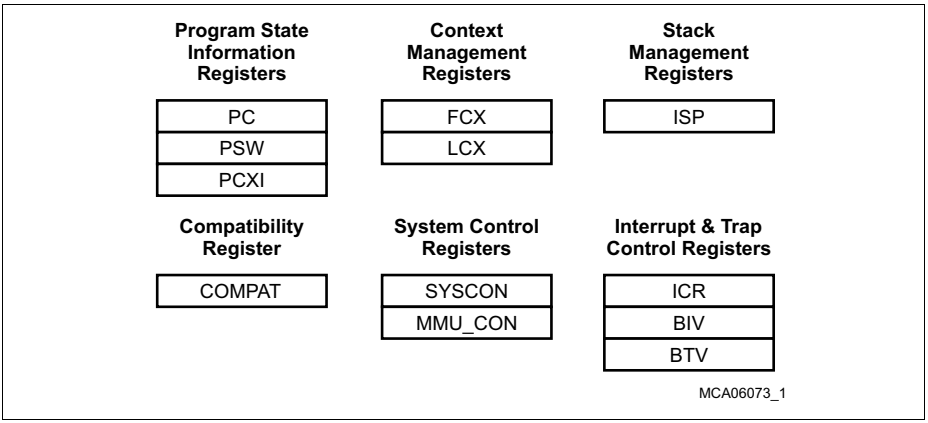


Figure 2-7 CSFR Registers

Table 2-2 Core Special Function Registers

Short Name	Description	Offset Address	Access Mode		Reset Value
			Read	Write	
MMU_CON	MMU Configuration Register	8000_H	U, SV, 32	SV, 32	Class 3 Reset 0000 8000_H
PCXI	Previous Context Information Register	$FE00_H$	U, SV, 32	SV, 32	Class 3 Reset 0000 0000_H
PSW	Program Status Word Register	$FE04_H$	U, SV, 32	SV, 32	Class 3 Reset 0000 $0B80_H$
PC	Program Counter Register	$FE08_H$	U, SV, 32	SV, 32	Class 3 Reset XXXX $XXXX_H$
SYSCON	System Configuration Register	$FE14_H$	U, SV, 32	SV, 32	Class 3 Reset 0000 0000_H
CPU_ID	CPU Identification Register	$FE18_H$	U, SV, 32	U, SV, 32, NC	Class 3 Reset 00C0 $C003_H$
BIV	Interrupt Vector Table Pointer Register	$FE20_H$	U, SV, 32	SV, E, 32	Class 3 Reset 0000 0000_H
BTV	Trap Vector Table Pointer Register	$FE24_H$	U, SV, 32	SV, E, 32	Class 3 Reset A000 0100_H

Table 2-2 Core Special Function Registers (cont'd)

Short Name	Description	Offset Address	Access Mode		Reset Value
			Read	Write	
ISP	Interrupt Stack Pointer Register	$FE28_H$	U, SV, 32	SV, E, 32	Class 3 Reset $0000\ 0100_H$
ICR	ICU Interrupt Control Register	$FE2C_H$	U, SV, 32	SV, 32	Class 3 Reset $0000\ 0000_H$
FCX	Free Context List Head Pointer Register	$FE38_H$	U, SV, 32	SV, 32	Class 3 Reset $0000\ 0000_H$
LCX	Free Context List Limit Pointer Register	$FE3C_H$	U, SV, 32	SV, 32	Class 3 Reset $0000\ 0000_H$
PMA0	Physical Memory Attributes	$801C_H$	U, SV, 32	SV, E, 32	Class 3 Reset $C000\ 03FF_H$
COMPAT	Compatibility Control Register	9400_H	U, SV, 32	SV, E, 32	Class 3 Reset $FFFF\ FFFF_H$

2.6.1 Registers

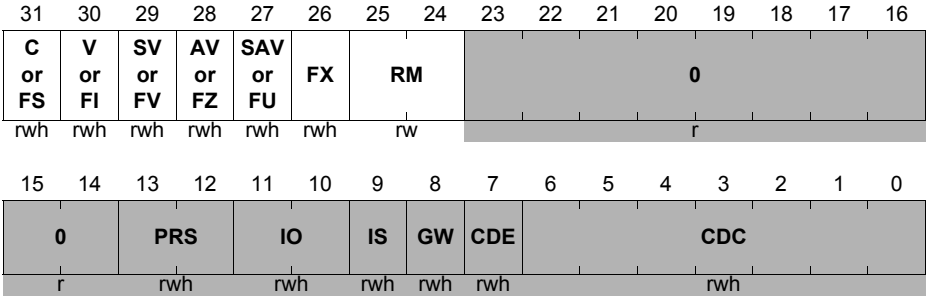
The implementation-specific Program Status Word Register (PSW) is an extension of the PSW description in the TriCore Architecture Manual. The status flags used for FPU operations overlay the status flags used for Arithmetic Logic Unit (ALU) operations.

Program Status Word Register

Note: The non-shaded areas in the register description define the implementation-specific bits/bit fields. The shaded areas are defined in the TriCore Architecture Manual.]

PSW

Program Status Word Register (F7E1 FE04$_H$) Reset Value: 0000 0B80$_H$



Field	Bits	Type	Description
RM	[25:24]	rw	**FPU Rounding Mode Selection**
FX	26	rwh	**FPU Inexact Flag**
SAV	27	rh	**Sticky Advance Overflow Flag**
FU		rwh	**FPU Underflow Flag**
AV	28	rwh	**Advance Overflow Flag**
FZ			**FPU Divide by Zero Flag**
SV	29	rwh	**Sticky Overflow Flag**
FV			**FPU Overflow Flag**
V	30	rwh	**Overflow Flag**
FI			**FPU Invalid Operation Flag**
C	31	rwh	**Carry Flag**
FS			**FPU Some Exception Flag**

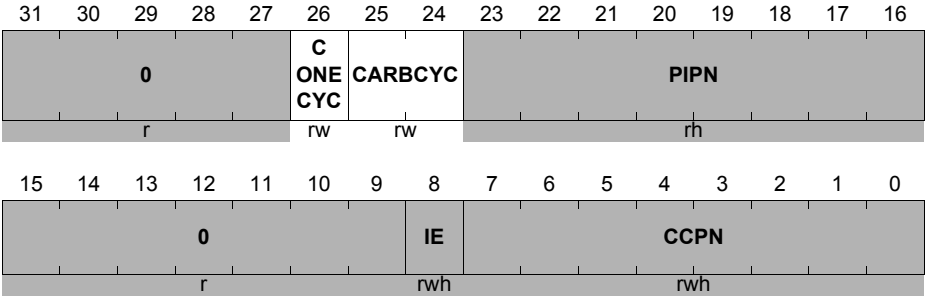
Interrupt Control Register

The Interrupt Control Register (ICR) is an implementation-specific CFSR. Its Arbitration Cycle Control implementation-specific details are defined in bits 24 to 26.

Note: The non-shaded areas in the register description define the implementation-specific bits/bit fields. The shaded areas are defined in the TriCore Architecture Manual.

ICR

Interrupt Control Register (F7E1 FE2C$_H$) Reset Value: 0000 0000$_H$



Field	Bits	Type	Description
CARBCYC	[25:24]	rw	**Number of Arbitration Cycles** CARBCYC controls the number of arbitration cycles used to determine the request with the highest priority. 00_B 4 arbitration cycles (default) 01_B 3 arbitration cycles 10_B 2 arbitration cycles 11_B 1 arbitration cycles
CONECYC	26	rw	**Number of Clocks per Arbitration Cycle Control** The CONECYC bit determines the number of system clocks per arbitration cycle. This bit should be set to 1 only for system designs utilizing low system clock frequencies. 0_B 2 clocks per arbitration cycle 1_B 1 clock per arbitration cycle

MMU Configuration Register

The MMU Configuration Register (MMU_CON) register indicates the non-availability of the TriCore Memory Management Unit (bit NOMMU is always set).

Note: To aid debug the TriCore 1.6 implements the MMU_ASI register.

Note: The non-shaded areas in the register description define the implementation-specific bits/bit fields. The shaded areas are defined in the TriCore Architecture Manual.

MMU_CON
MMU Configuration Register (F7E1 8000$_H$) Reset Value: 0000 8000$_H$

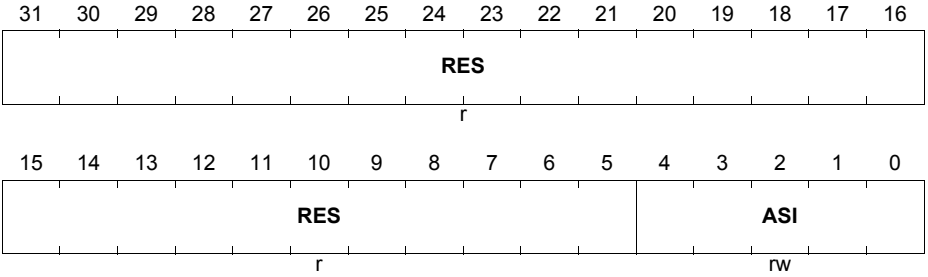
Field	Bits	Type	Description
NOMMU	15	r	**MMU Exists** 0_B MMU is available. 1_B MMU is not available. All other bits of MMU_CON are undefined. *Note:* The MMU is not available in TC1798.

Address Space Identifier Register (MMU_ASI)

The Memory Management Unit (MMU), Address Space Identifier (ASI) register description.

MMU_ASI
Address Space Identifier Register

(F7E1 8004$_H$) **Reset Value: 0000 001F$_H$**

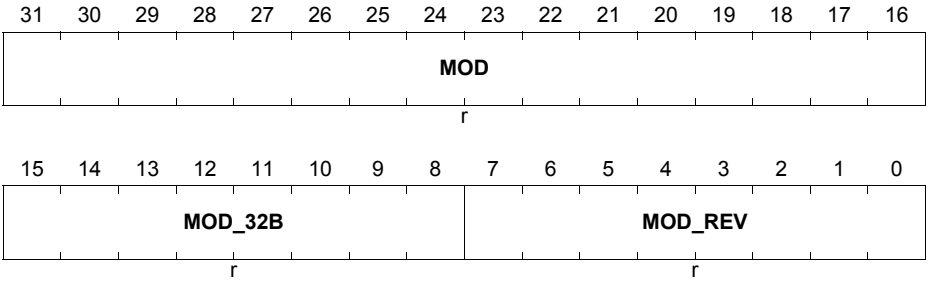


Field	Bits	Type	Description
RES	[31:5]	r	**Reserved**
ASI	[4:0]	rw	**Address Space Identifier** The ASI register contains the Address Space Identifier of the current process.

CPU Identification Register

CPU_ID
CPU Identification Register

(F7E1 FE18$_H$) **Reset Value: 00C0 C003$_H$**



Field	Bits	Type	Description
MOD_REV	[7:0]	r	**Revision Number** 03$_H$ Reset value
MOD_32B	[15:8]	r	**32-Bit Module Enable** C0$_H$ A value of C0$_H$ in this field indicates a 32-bit module with a 32-bit module ID register.
MOD	[31:16]	r	**Module Identification Number** 00C0$_H$ For module identification

Physical Memory Attributes Register

The Physical Memory Attributes PMA0 register defines the physical memory attribute for each segment in the physical address space. The register is ENDINIT protected and can be read with the MFCR instruction and written by the MTCR instruction. Note that when changing the value of the PMA0 register both the instruction and data caches should be invalidated, a dsync should be executed immediately prior to the MTCR with an ISYNC instruction executed immediately following. This is required to maintain coherency of the processors view of memory.

The physical memory attribute of a segment n in the physical address space, is defined by the bit field ATT[1:0][n]. For example, the segment F_H has the physical attributes defined by bit field ATT[1:0][F_H]. This refers to bit 15 of the ATT[1][n] bit field, and bit 15 of the ATT[0][n] bit field; i.e. a value of 10_B.

All segments are freely programmable with the following restrictions:-

- Segment-F is constrained to be Peripheral space
- Segment-D is constrained to be either cacheable or non-cacheable memory. Data fetches to the lower half segment and to the global address of the local data scratch memory are always non-cacheable irrespective of the programmed attributes.
- Segment-C is constrained to be either cacheable or non-cacheable memory. Code fetches to the lower half segment and to the global address of the local data scratch memory are always non-cacheable irrespective of the programmed attributes.
- Segment-A is constrained to be non-cacheable memory

Note: This register is ENDINIT protected.

PMA0
Physical Memory Attributes (F7E1 801C$_H$) Reset Value: C000 03FF

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ATT[1:0][15]	ATT[1:0][14]	ATT[1:0][13]	ATT[1:0][12]	ATT[1:0][11]	ATT[1:0][10]	ATT[1][n]									
r	rw	r	r	rw	r	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ATT[1:0][15]	ATT[1:0][14]	ATT[1:0][13]	ATT[1:0][12	ATT[1:0][11]	ATT[1:0][10]	ATT[0][n]									
r	rw	rw	rw	rw	r	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
ATT[1:0][15]	31, 15	r	Segment F_H physical memory attribute = 10_B. Segment F_H is constrained to always be peripheral space.

Field	Bits	Type	Description
ATT[1:0][14]	30, 14	rw	Segment E_H physical memory attribute.
ATT[1:0][13]	29, 13	rw	Segment D_H physical memory attribute = $0x_B$. Segment D_H is constrained to never be peripheral space
ATT[1:0][12]	28, 12	rw	Segment C_H physical memory attribute = $0x_B$. Segment C_H is constrained to never be peripheral space
ATT[1:0][11]	27, 11	rw	Segment B_H physical memory attribute.
ATT[1:0][10]	26, 10	r	Segment A_H physical memory attribute = 00_B. Segment A_H is constrained to be non-cached memory
ATT[1:0][9:0]	[25:16], [9:0]	rw	Segment 9_H - 0_H physical memory attributes.

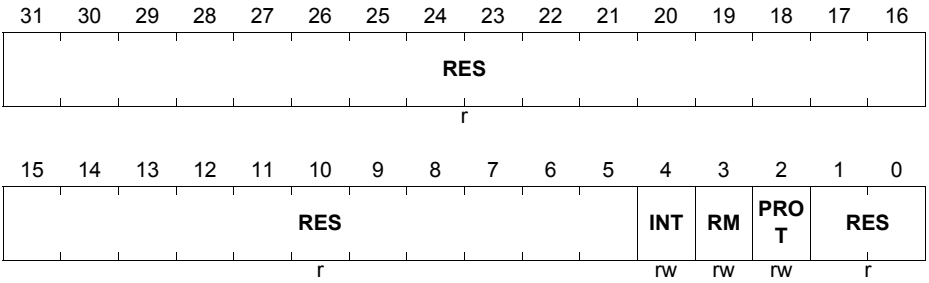
Table 2-3 ATT[1:0][n] Bit Field Encoding

ATT[1:0][n]	Segment Attributes
11	Reserved.
10	Peripheral Space.
01	Cacheable Memory.
00	Non-Cacheable Memory.

Compatibility Control Register

The Compatibility Control Register (COMPAT) is an implementation-specific CSFR which allows certain elements of backwards compatibility with TriCore 1.3.x behavior to be forced. The reset value of the COMPAT register ensures that backwards compatibility with TriCore 1.3 is enabled by default.

COMPAT
Compatibility Control Register (F7E1 9400$_H$) Reset Value: FFFF FFFF$_H$



Field	Bits	Type	Description
RES	[1:0]	r	**Reserved** Read as 1; should be written with 1.
PROT	2	rw	**Range Table to set mapping** 0_B Mapping enabled. 1_B Fixed mapping (TC1.3 behavior).
RM	3	rw	**Rounding mode compatibility** 0_B PSW.RM not restored by RET. 1_B PSW.RM restored by RET (TC1.3 behavior).
INT	4	r	**Interrupt Mode** 0_B Safe interrupt Operation, Software Acknowledge 1_B Standard Interrupt Operation, Hardware Acknowledge
RES	[31:5]	r	**Reserved** Read as 1; should be written with 1.

2.7 CPU General Purpose Registers

Figure 2-8 shows the General Purpose Registers (GPRs) of the TC1798.

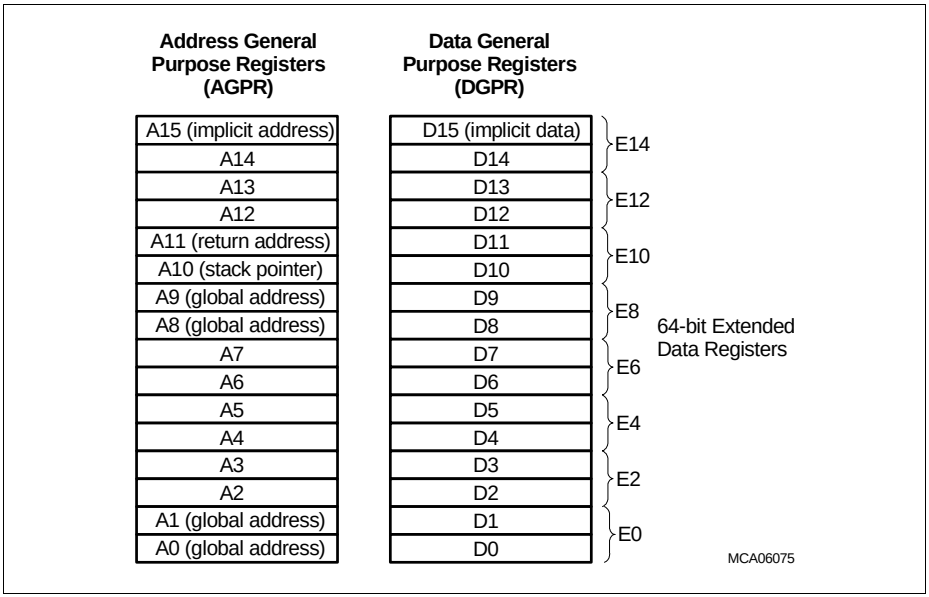


Figure 2-8 GPR Registers

Table 2-4 GPR Registers

Short Name	Description	Offset Address	Access Mode		Reset
			Read	Write	
D0	Data Register 0	$FF00_H$	U, SV, 32	SV, 32	Class 3 Reset XXXX XXXX$_H$
D1	Data Register 1	$FF04_H$	U, SV, 32	SV, 32	Class 3 Reset XXXX XXXX$_H$
D2	Data Register 2	$FF08_H$	U, SV, 32	SV, 32	Class 3 Reset XXXX XXXX$_H$
D3	Data Register 3	$FF0C_H$	U, SV, 32	SV, 32	Class 3 Reset XXXX XXXX$_H$
D4	Data Register 4	$FF10_H$	U, SV, 32	SV, 32	Class 3 Reset XXXX XXXX$_H$

Table 2-4 GPR Registers (cont'd)

Short Name	Description	Offset Address	Access Mode		Reset
			Read	Write	
D5	Data Register 5	$FF14_H$	U, SV, 32	SV, 32	Class 3 Reset $XXXX\ XXXX_H$
D6	Data Register 6	$FF18_H$	U, SV, 32	SV, 32	Class 3 Reset $XXXX\ XXXX_H$
D7	Data Register 7	$FF1C_H$	U, SV, 32	SV, 32	Class 3 Reset $XXXX\ XXXX_H$
D8	Data Register 8	$FF20_H$	U, SV, 32	SV, 32	Class 3 Reset $XXXX\ XXXX_H$
D9	Data Register 9	$FF24_H$	U, SV, 32	SV, 32	Class 3 Reset $XXXX\ XXXX_H$
D10	Data Register 10	$FF28_H$	U, SV, 32	SV, 32	Class 3 Reset $XXXX\ XXXX_H$
D11	Data Register 11	$FF2C_H$	U, SV, 32	SV, 32	Class 3 Reset $XXXX\ XXXX_H$
D12	Data Register 12	$FF30_H$	U, SV, 32	SV, 32	Class 3 Reset $XXXX\ XXXX_H$
D13	Data Register 13	$FF34_H$	U, SV, 32	SV, 32	Class 3 Reset $XXXX\ XXXX_H$
D14	Data Register 14	$FF38_H$	U, SV, 32	SV, 32	Class 3 Reset $XXXX\ XXXX_H$
D15	Data Register 15	$FF3C_H$	U, SV, 32	SV, 32	Class 3 Reset $XXXX\ XXXX_H$
A0	Address Register 0 (Global Address Register)	$FF80_H$	U, SV, 32	SV, 32	Class 3 Reset $XXXX\ XXXX_H$
A1	Address Register 1 (Global Address Register)	$FF84_H$	U, SV, 32	SV, 32	Class 3 Reset $XXXX\ XXXX_H$
A2	Address Register 2	$FF88_H$	U, SV, 32	SV, 32	Class 3 Reset $XXXX\ XXXX_H$
A3	Address Register 3	$FF8C_H$	U, SV, 32	SV, 32	Class 3 Reset $XXXX\ XXXX_H$
A4	Address Register 4	$FF90_H$	U, SV, 32	SV, 32	Class 3 Reset $XXXX\ XXXX_H$

Table 2-4 GPR Registers (cont'd)

Short Name	Description	Offset Address	Access Mode		Reset
			Read	Write	
A5	Address Register 5	$FF94_H$	U, SV, 32	SV, 32	Class 3 Reset XXXX XXXX$_H$
A6	Address Register 6	$FF98_H$	U, SV, 32	SV, 32	Class 3 Reset XXXX XXXX$_H$
A7	Address Register 7	$FF9C_H$	U, SV, 32	SV, 32	Class 3 Reset XXXX XXXX$_H$
A8	Address Register 8 (Global Address Register)	$FFA0_H$	U, SV, 32	SV, 32	Class 3 Reset XXXX XXXX$_H$
A9	Address Register 9 (Global Address Register)	$FFA4_H$	U, SV, 32	SV, 32	Class 3 Reset XXXX XXXX$_H$
A10	Address Register 10 (Stack Pointer)	$FFA8_H$	U, SV, 32	SV, 32	Class 3 Reset XXXX XXXX$_H$
A11	Address Register 11 (Return Address)	$FFAC_H$	U, SV, 32	SV, 32	Class 3 Reset XXXX XXXX$_H$
A12	Address Register 12	$FFB0_H$	U, SV, 32	SV, 32	Class 3 Reset XXXX XXXX$_H$
A13	Address Register 13	$FFB4_H$	U, SV, 32	SV, 32	Class 3 Reset XXXX XXXX$_H$
A14	Address Register 14	$FFB8_H$	U, SV, 32	SV, 32	Class 3 Reset XXXX XXXX$_H$
A15	Address Register 15	$FFBC_H$	U, SV, 32	SV, 32	Class 3 Reset XXXX XXXX$_H$

2.8 CPU Memory Protection Registers

There are four Memory Protection Register Sets in the TC1798. The sets specify memory protection ranges and permissions for code and data. The PSW.PRS bit field determines which of these sets is currently in use by the CPU. The TC1.6 implements 16 data and 8 code range comparators. These may be flexibly shared amongst the of protection sets to provide a maximum of 8 data ranges and four code ranges per set. The Memory Protection Registers are Core Special Function Registers, they are described in detail in the TriCore Architecture Manual.

Table 2-5 Memory Protection Registers

Short Name	Description	Offset Address	Access Mode		Reset
			Read	Write	
DPR0_0L	Data Protection Range 0.0, Lower Bound Register	$C000_H$	U, SV, 32	SV, 32	Class 3 Reset $0000\ 0000_H$
DPR0_0U	Data Protection Range 0.0, Upper Bound Register	$C004_H$	U, SV, 32	SV, 32	Class 3 Reset $0000\ 0000_H$
DPR0_1L	Data Protection Range 0.1, Lower Bound Register	$C400_H$	U, SV, 32	SV, 32	Class 3 Reset $0000\ 0000_H$
DPR0_1U	Data Protection Range 0.1, Upper Bound Register	$C404_H$	U, SV, 32	SV, 32	Class 3 Reset $0000\ 0000_H$
DPR1_0L	Data Protection Range 1.0, Lower Bound Register	$C800_H$	U, SV, 32	SV, 32	Class 3 Reset $0000\ 0000_H$
DPR1_0U	Data Protection Range 1.0, Upper Bound Register	$C804_H$	U, SV, 32	SV, 32	Class 3 Reset $0000\ 0000_H$
DPR1_1L	Data Protection Range 1.1, Lower Bound Register	$CC00_H$	U, SV, 32	SV, 32	Class 3 Reset $0000\ 0000_H$
DPR1_1U	Data Protection Range 1.1, Upper Bound Register	$CC04_H$	U, SV, 32	SV, 32	Class 3 Reset $0000\ 0000_H$
DPR2_0L	Data Protection Range 2.0, Lower Bound Register	$C008_H$	U, SV, 32	SV, 32	Class 3 Reset $0000\ 0000_H$
DPR2_0U	Data Protection Range 2.0, Upper Bound Register	$C00C_H$	U, SV, 32	SV, 32	Class 3 Reset $0000\ 0000_H$
DPR2_1L	Data Protection Range 2.1, Lower Bound Register	$C408_H$	U, SV, 32	SV, 32	Class 3 Reset $0000\ 0000_H$
DPR2_1U	Data Protection Range 2.1, Upper Bound Register	$C40C_H$	U, SV, 32	SV, 32	Class 3 Reset $0000\ 0000_H$

Table 2-5 Memory Protection Registers (cont'd)

Short Name	Description	Offset Address	Access Mode		Reset
			Read	Write	
DPR3_0L	Data Protection Range 3.0, Lower Bound Register	$C808_H$	U, SV, 32	SV, 32	Class 3 Reset $0000\ 0000_H$
DPR3_0U	Data Protection Range 3.0, Upper Bound Register	$C80C_H$	U, SV, 32	SV, 32	Class 3 Reset $0000\ 0000_H$
DPR3_1L	Data Protection Range 3.1, Lower Bound Register	$CC08_H$	U, SV, 32	SV, 32	Class 3 Reset $0000\ 0000_H$
DPR3_1U	Data Protection Range 3.1, Upper Bound Register	$CC0C_H$	U, SV, 32	SV, 32	Class 3 Reset $0000\ 0000_H$
DPR4_0L	Data Protection Range 4.0, Lower Bound Register	$C010_H$	U, SV, 32	SV, 32	Class 3 Reset $0000\ 0000_H$
DPR4_0U	Data Protection Range 4.0, Upper Bound Register	$C014_H$	U, SV, 32	SV, 32	Class 3 Reset $0000\ 0000_H$
DPR4_1L	Data Protection Range 4.1, Lower Bound Register	$C410_H$	U, SV, 32	SV, 32	Class 3 Reset $0000\ 0000_H$
DPR4_1U	Data Protection Range 4.1, Upper Bound Register	$C414_H$	U, SV, 32	SV, 32	Class 3 Reset $0000\ 0000_H$
DPR5_0L	Data Protection Range 5.0, Lower Bound Register	$C810_H$	U, SV, 32	SV, 32	Class 3 Reset $0000\ 0000_H$
DPR5_0U	Data Protection Range 5.0, Upper Bound Register	$C814_H$	U, SV, 32	SV, 32	Class 3 Reset $0000\ 0000_H$
DPR5_1L	Data Protection Range 5.1, Lower Bound Register	$CC10_H$	U, SV, 32	SV, 32	Class 3 Reset $0000\ 0000_H$
DPR5_1U	Data Protection Range 5.1, Upper Bound Register	$CC14_H$	U, SV, 32	SV, 32	Class 3 Reset $0000\ 0000_H$
DPR6_0L	Data Protection Range 6.0, Lower Bound Register	$C018_H$	U, SV, 32	SV, 32	Class 3 Reset $0000\ 0000_H$
DPR6_0U	Data Protection Range 6.0, Upper Bound Register	$C01C_H$	U, SV, 32	SV, 32	Class 3 Reset $0000\ 0000_H$
DPR6_1L	Data Protection Range 6.1, Lower Bound Register	$C418_H$	U, SV, 32	SV, 32	Class 3 Reset $0000\ 0000_H$
DPR6_1U	Data Protection Range 6.1, Upper Bound Register	$C41C_H$	U, SV, 32	SV, 32	Class 3 Reset $0000\ 0000_H$

Table 2-5 Memory Protection Registers (cont'd)

Short Name	Description	Offset Address	Access Mode		Reset
			Read	Write	
DPR7_0L	Data Protection Range 7.0, Lower Bound Register	$C818_H$	U, SV, 32	SV, 32	Class 3 Reset $0000\ 0000_H$
DPR7_0U	Data Protection Range 7.0, Upper Bound Register	$C81C_H$	U, SV, 32	SV, 32	Class 3 Reset $0000\ 0000_H$
DPR7_1L	Data Protection Range 7.1, Lower Bound Register	$CC18_H$	U, SV, 32	SV, 32	Class 3 Reset $0000\ 0000_H$
DPR7_1U	Data Protection Range 7.1, Upper Bound Register	$CC1C_H$	U, SV, 32	SV, 32	Class 3 Reset $0000\ 0000_H$
CPR0_0L	Code Protection Range 0.0, Lower Bound Register	$D000_H$	U, SV, 32	SV, 32	Class 3 Reset $0000\ 0000_H$
CPR0_0U	Code Protection Range 0.0, Upper Bound Register	$D004_H$	U, SV, 32	SV, 32	Class 3 Reset $0000\ 0000_H$
CPR0_1L	Code Protection Range 0.1, Lower Bound Register	$D400_H$	U, SV, 32	SV, 32	Class 3 Reset $0000\ 0000_H$
CPR0_1U	Code Protection Range 0.1, Upper Bound Register	$D404_H$	U, SV, 32	SV, 32	Class 3 Reset $0000\ 0000_H$
CPR1_0L	Code Protection Range 1.0, Lower Bound Register	D800	U, SV, 32	SV, 32	Class 3 Reset $0000\ 0000_H$
CPR1_0U	Code Protection Range 1.0, Upper Bound Register	$D804_H$	U, SV, 32	SV, 32	Class 3 Reset $0000\ 0000_H$
CPR1_1L	Code Protection Range 1.1, Lower Bound Register	$DC00_H$	U, SV, 32	SV, 32	Class 3 Reset $0000\ 0000_H$
CPR1_1U	Code Protection Range 1.1, Upper Bound Register	DC04	U, SV, 32	SV, 32	Class 3 Reset $0000\ 0000_H$
CPR2_0L	Code Protection Range 2.0, Lower Bound Register	$D008_H$	U, SV, 32	SV, 32	Class 3 Reset $0000\ 0000_H$
CPR2_0U	Code Protection Range 2.0, Upper Bound Register	$D00C_H$	U, SV, 32	SV, 32	Class 3 Reset $0000\ 0000_H$
CPR2_1L	Code Protection Range 2.1, Lower Bound Register	$D408_H$	U, SV, 32	SV, 32	Class 3 Reset $0000\ 0000_H$
CPR2_1U	Code Protection Range 2.1, Upper Bound Register	$D40C_H$	U, SV, 32	SV, 32	Class 3 Reset $0000\ 0000_H$

Table 2-5 Memory Protection Registers (cont'd)

Short Name	Description	Offset Address	Access Mode		Reset
			Read	Write	
CPR3_0L	Code Protection Range 3.0, Lower Bound Register	$D808_H$	U, SV, 32	SV, 32	Class 3 Reset $0000\ 0000_H$
CPR3_0U	Code Protection Range 3.0, Upper Bound Register	D80C	U, SV, 32	SV, 32	Class 3 Reset $0000\ 0000_H$
CPR3_1L	Code Protection Range 3.1, Lower Bound Register	$DC08_H$	U, SV, 32	SV, 32	Class 3 Reset $0000\ 0000_H$
CPR3_1U	Code Protection Range 3.1, Upper Bound Register	$DC0C_H$	U, SV, 32	SV, 32	Class 3 Reset $0000\ 0000_H$
DPS0	Data Protection Set Configuration Register 0	$E000_H$	U, SV, 32	SV, 32	Class 3 Reset $0000\ 0000_H$
DPS1	Data Protection Set Configuration Register 1	$E080_H$	U, SV, 32	SV, 32	Class 3 Reset $0000\ 0000_H$
DPS2	Data Protection Set Configuration Register 2	$E100_H$	U, SV, 32	SV, 32	Class 3 Reset $0000\ 0000_H$
DPS3	Data Protection Set Configuration Register 3	$E180_H$	U, SV, 32	SV, 32	Class 3 Reset $0000\ 0000_H$
CPS0	Code Protection Set Configuration Register 0	$E200_H$	U, SV, 32	SV, 32	Class 3 Reset $0000\ 0000_H$
CPS1	Code Protection Set Configuration Register 1	$E280_H$	U, SV, 32	SV, 32	Class 3 Reset $0000\ 0000_H$
CPS2	Code Protection Set Configuration Register 2	$E300_H$	U, SV, 32	SV, 32	Class 3 Reset $0000\ 0000_H$
CPS3	Code Protection Set Configuration Register 3	$E380_H$	U, SV, 32	SV, 32	Class 3 Reset $0000\ 0000_H$

2.9 Temporal Protection Registers

To Guard against task runtime overrun the TriCore1.6 implements a temporal protection system. This system consists of two independent decrementing counters arranged to generate a Temporal Asynchronous Error trap (TAE - Class-4, Tin-7) on decrement to zero. The Temporal Protection Registers are Core Special Function Registers, they are described in detail in the TriCore Architecture Manual.

Table 2-6 Temporal Protection System Registers

Short Name	Description	Offset Address	Access Mode		Reset
			Read	Write	
TPS_CON	TPS Control Register	$E400_H$	U, SV, 32	SV, 32	Class 3 Reset $0000\ 0000_H$
TPS_TIMER0	TPS Timer 0 Register	$E404_H$	U, SV, 32	SV, 32	Class 3 Reset $0000\ 0000_H$
TPS_TIMER1	TPS Timer 1 Register	$E408_H$	U, SV, 32	SV, 32	Class 3 Reset $0000\ 0000_H$

2.10 FPU Registers

A number of FPU Special Function Registers (CSFRs) have been introduced to the TriCore 1.6 architecture in order to fully support functional enhancements.

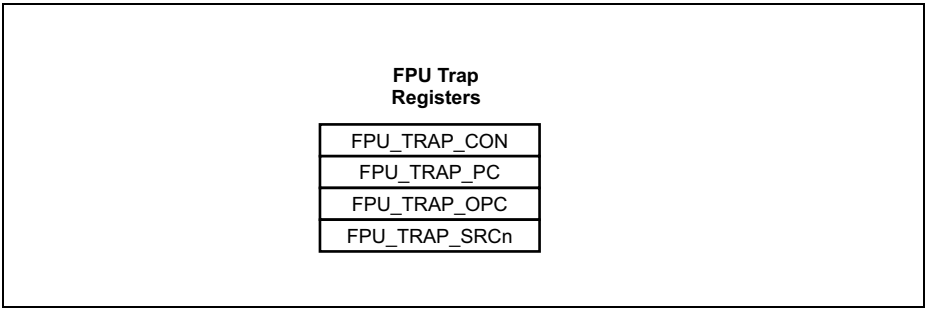


Figure 2-9 TriCore 1.6 CSFR Registers

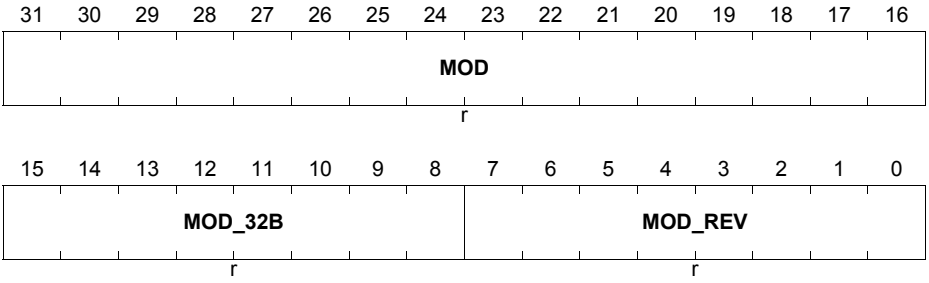
Table 2-7 Floating Point Special Function Registers

Short Name	Description	Offset Address	Access Mode		Reset
			Read	Write	
FPU_TRAP_CON	Trap Control Register	$A000_H$	U, SV, 32	SV, 32	Class 3 Reset $0000\ 0000_H$
FPU_TRAP_PC	Trapping Instruction Program Counter Register	$A004_H$	U, SV, 32	SV, 32	Class 3 Reset $0000\ 0000_H$
FPU_TRAP_OPC	Trapping Instruction Opcode Register	$A008_H$	U, SV, 32	SV, 32	Class 3 Reset $0000\ 0000_H$
FPU_TRAP_SRC1	Trapping Instruction Operand Register	$A010_H$	U, SV, 32	SV, 32	Class 3 Reset $0000\ 0000_H$
FPU_TRAP_SRC2	Trapping Instruction Operand Register	$A014_H$	U, SV, 32	SV, 32	Class 3 Reset $0000\ 0000_H$
FPU_TRAP_SRC3	Trapping Instruction Operand Register	$A018_H$	U, SV, 32	SV, 32	Class 3 Reset $0000\ 0000_H$
FPU_ID	Trapping Identification Register	$A020_H$	U, SV, 32	SV, 32	Class 3 Reset $00C2\ C003_H$

2.10.1 Registers

FPU Identification Register

FPU_ID
Trapping Identification Register (F7E1 A020$_H$) **Reset Value: 00C2 C003$_H$**



Field	Bits	Type	Description
MOD_REV	[7:0]	r	**Revision Number** 03_H Reset value
MOD_32B	[15:8]	r	**32-Bit Module Enable** $C0_H$ A value of $C0_H$ in this field indicates a 32-bit module with a 32-bit module ID register.
MOD	[31:16]	r	**Module Identification Number** $00C2_H$ For module identification.

2.11 Memory Integrity Registers

To monitor and debug the integrity of the memory subsystems the following registers are introduced.

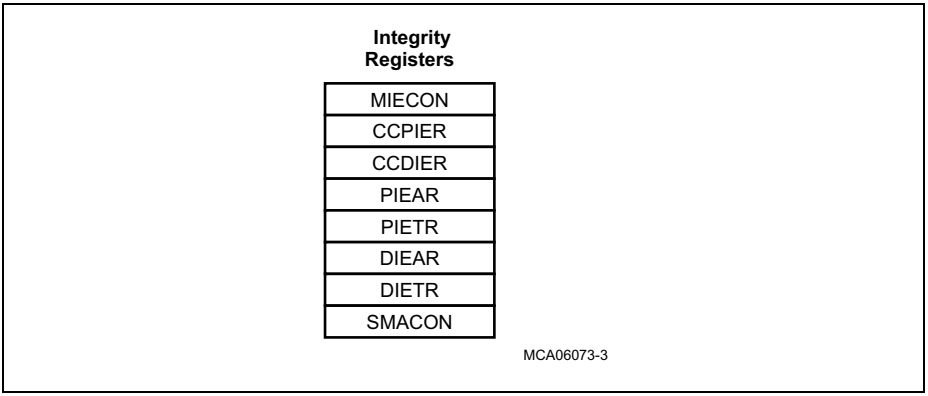


Figure 2-10 TriCore 1.6 CSFR Registers

Table 2-8 Memory Integrity Registers

Short Name	Description	Offset Address	Access Mode		Reset
			Read	Write	
MIECON	Memory Integrity Error Control Register	9044_H	U, SV, 32	SV, E, 32	Class 3 Reset $0000\ 0000_H$
MIECON2	Memory Integrity Error Control Register 2	9048_H	U, SV, 32	SV, E, 32	Class 3 Reset $0000\ 0000_H$
CCPIER	Count of Corrected Program Integrity Errors Register	9218_H	U, SV, 32	SV, 32	Class 3 Reset $0000\ 0000_H$
CCDIER	Count of Corrected Data Integrity Errors Register	9028_H	U, SV, 32	SV, 32	Class 3 Reset $0000\ 0000_H$
PIEAR	Program Integrity Error Address Register	9210_H	U, SV, 32	SV, 32	Class 3 Reset $0000\ 0000_H$
PIETR	Program Integrity Error Trap Register	9214_H	U, SV, 32	SV, 32	Class 3 Reset $0000\ 0000_H$
DIEAR	Data Integrity Error Address Register	9020_H	U, SV, 32	SV, 32	Class 3 Reset $0000\ 0000_H$

Table 2-8 Memory (cont'd) **Integrity Registers**

Short Name	Description	Offset Address	Access Mode		Reset
			Read	Write	
DIETR	Data Integrity Error Trap Register	9024_H	U, SV, 32	SV, 32	Class 3 Reset $0000\ 0000_H$
SMACON	SIST Mode Access Control Register	$900C_H$	U, SV, 32	SV, E, 32	Class 3 Reset $0000\ 0000_H$

2.11.1 Register Descriptions

Memory Integrity Error Control Register

The Memory Integrity Error Control Register (MIECON) allows software to control the handling of uncorrectable memory integrity errors.

MIECON
Memory Integrity Error Control Register
(F7E1 9044$_H$) **Reset Value: 0000 0000$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES													PTIEE	RES	DTIEE
r													rw	r	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES					PBMIEE	PCMIEE	PSMIEE	RES						DCMIEE	DSMIEE
r					rw	rw	rw	r						rw	rw

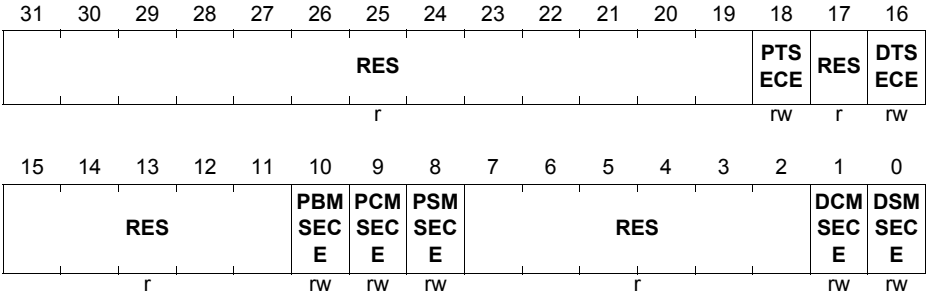
Field	Bits	Type	Description
DSMIEE	0	rw	**Data Scratch Memory Integrity Error Enable** Enables handling of uncorrectable integrity errors for the DSPR Memories. 0_B Uncorrectable integrity error handling disabled - all memory accesses interpreted as error free. 1_B Uncorrectable integrity error handling enabled.
DCMIEE	1	rw	**Data Cache Memory Integrity Error Enable** Enables handling of uncorrectable integrity errors for the Data Cache Memories. 0_B Uncorrectable integrity error handling disabled - all memory accesses interpreted as error free. 1_B Uncorrectable integrity error handling enabled.
RES	[7:2]	r	**Reserved**

Field	Bits	Type	Description
PSMIEE	8	rw	**Program Scratch Memory Integrity Error Enable** Enables handling of uncorrectable integrity errors for the Program Scratch Memories. 0_B Uncorrectable integrity error handling disabled - all memory accesses interpreted as error free. 1_B Uncorrectable integrity error handling enabled.
PCMIEE	9	rw	**Program Cache Memory Integrity Error Enable** Enables handling of uncorrectable integrity errors for the Program Cache Memories. 0_B Uncorrectable integrity error handling disabled - all memory accesses interpreted as error free. 1_B Uncorrectable integrity error handling enabled.
PBMIEE	10	rw	**Program Bus Memory Integrity Error Enable** Enables handling of uncorrectable integrity errors for Instructions fetched directly from the bus system. 0_B Uncorrectable integrity error handling disabled - all memory accesses interpreted as error free. 1_B Uncorrectable integrity error handling enabled.
RES	[15:11]	r	**Reserved**
DTIEE	16	rw	**Data Tag Integrity Error Enable** Enables handling of uncorrectable integrity errors for the Data Tag. 0_B Uncorrectable integrity error handling disabled - all memory accesses interpreted as error free. 1_B Uncorrectable integrity error handling enabled.
RES	17	r	**Reserved**
PTIEE	18	rw	**Program Tag Integrity Error Enable** Enables handling of uncorrectable integrity errors for the Program Tag. 0_B Uncorrectable integrity error handling disabled - all memory accesses interpreted as error free. 1_B Uncorrectable integrity error handling enabled.
RES	[31:19]	r	**Reserved** Read as 0; should be written with 0.

Memory Integrity Error Control Register 2

The Memory Integrity Error Control Register 2 (MIECON2) allows software to control the handling of correctable memory integrity errors.

MIECON2
Memory Integrity Error Control Register 2
(F7E1 9048$_H$) **Reset Value: 0000 0000$_H$**



Field	Bits	Type	Description
DSMSECE	0	rw	**Data Scratch Memory Single Error Correction Enable** Enables single bit error correction for the DSPR Memories.
DCMSECE	1	rw	**Data Cache Memory Single Error Correction Enable** Enables single bit error correction for the Data Cache Memories.
RES	[7:2]	r	**Reserved**
PSMSECE	8	rw	**Program Scratch Memory Single Error Correction Enable** Enables single bit error correction for the Program Memories.
PCMSECE	9	rw	**Program Cache Memory Single Error Correction Enable** Enables single bit error correction for the Program Memories.

Field	Bits	Type	Description
PBMSECE	10	rw	**Program Bus Memory Single Error Correction Enable** Enables single bit error correction for the instructions fetched directly from the bus system.
RES	[15:11]	r	**Reserved**
DTSECE	16	rw	**Data Tag Single Error Correction Enable** Enables single bit error correction for the Data Tag
RES	17	r	**Reserved**
PTSECE	18	rw	**Program Tag Single Error Correction Enable** Enables single bit error correction for the Program Tag.
RES	[31:19]	r	**Reserved** Read as 0; should be written with 0.

Function

Although the xxIEE and xxSECE bits for a given memory type exist in different registers (MIECON and MIECON2 respectively) due to different protection requirements for these CSFR bits, the bits interact to perform the following general functions.

Table 2-9 Functions

xxSECE	xxIEE	Description
0	0	**No Memory Integrity Handling** All single and double-bit memory integrity errors ignored.
0	1	**Error Detection Mode** Single and double-bit errors treated as uncorrectable errors.
1	0	**SEC Only Mode** Single-bit errors corrected by ECC, double-bit errors ignored
1	1	**SECDED Mode** Single-bit errors corrected by ECC, double-bit errors treated as uncorrectable errors.

Program Integrity Error Information Registers

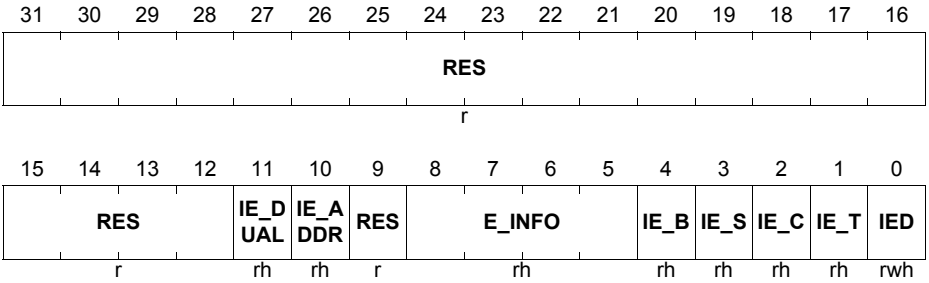
Two architecturally visible registers (PIETR, PIEAR) allow software to localise the source of the last detected uncorrectable program memory integrity error. These registers are updated when an uncorrectable program integrity error condition is detected and the PIETR.IED bit is zero. On update the PIETR.IED bit is set to one and remains set until cleared by software. Whilst PIETR.IED is set further hardware updates of PIETR and PIEAR are inhibited.

PIETR and PIEAR are updated on any uncorrectable program memory integrity error condition detected, either during a bus access or a CPU instruction pre-fetch. Since instruction pre-fetches are speculative, the PIETR and PIEAR registers may be updated without a corresponding PIE trap.

The Program Integrity Error Trap Register (PIETR) contains flags to support software in localising the source of the last detected uncorrectable program memory integrity error. Where an uncorrectable integrity error condition is detected during an instruction pre-fetch, the IE_S, IE_C and IE_T bits are updated to denote in which memory structure the error was detected, whilst BUS_ID and IE_B are cleared. Where the error is detected during an external bus access to a core memory, IE_B is set and BUS_ID updated to denote the master tag ID of the initiating bus master, whilst IE_S, IE_C and IE_T are cleared. If the error detected in the address the IE_ADDR bit is set. If the error detected is a dual bit error the IE_DUAL bit is set.

Program Integrity Error Trap Register (PIETR)

PIETR
Program Integrity Error Trap Register
(F7E1 9214$_H$) **Reset Value: 0000 0000$_H$**



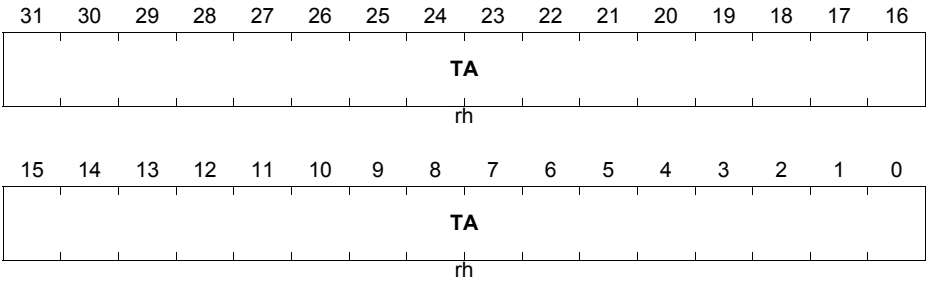
Field	Bits	Type	Description
IED	0	rwh	**Integrity Error Detected** Read Operation: 0_B No program integrity error condition occurred. 1_B Program integrity error condition detected. PIETR and PIEAR contents valid, further PIETR and PIEAR updates disabled. Write Operation: 0_B Clear IED bit, re-enable PIETR and PIEAR updates. 1_B No effect.
IE_T	1	rh	**Integrity Error - Tag Memory**
IE_C	2	rh	**Integrity Error - Cache Memory**
IE_S	3	rh	**Integrity Error - Scratchpad Memory**
IE_B	4	rh	**Integrity Error - Bus Access**
E_INFO	[8:5]	rh	**Error Information** If IE_B = 1 : Bus Master Tag ID of requesting master If IE_C = 1 : Cache way.
RES	9	r	**Reserved** Read as 0; should be written with 0.
IE_ADDR	10	r	**Integrity Error - Address Error Detected**
IE_DUAL	11	r	**Integrity Error - Dual Error Detected**

Field	Bits	Type	Description
RES	[31:12]	r	**Reserved** Read as 0; should be written with 0.

Program Integrity Error Address Register

This register contains the physical address accessed by the operation that encountered a uncorrectable program memory integrity error. This register is only updated if PIETR.IED is zero.

PIEAR
Program Integrity Error Address Register
(F7E1 9210$_H$) **Reset Value: 0000 0000$_H$**



Field	Bits	Type	Description
TA	[31:0]	rh	**Transaction Address** Physical address being accessed by operation that encountered program integrity error.

Data Integrity Error Information Registers

Two architecturally visible registers (DIETR, DIEAR) allow software to localise the source of the last detected uncorrectable data memory integrity error. These registers are updated when an uncorrectable data integrity error condition is detected and the DIETR.IED bit is zero. On update the DIETR.IED bit is set to one and remains set until cleared by software. Whilst DIETR.IED is set further hardware updates of DIETR and DIEAR are inhibited.

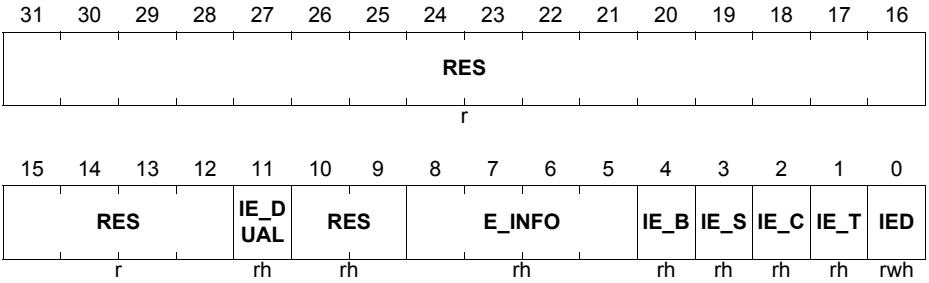
The Data Integrity Error Trap Register (DIETR) contains flags to support software in localising the source of the last detected uncorrectable data memory integrity error. Where an uncorrectable data memory integrity error condition is detected during a CPU Load/Store access, the IE_S, IE_C, IE_T and E_INFO fields are updated to denote where the error was detected and the nature of the DIE trap. whilst BUS_ID and IE_B are cleared. Where the error is detected during an external bus access to a core memory the IE_B is set and E_INFO updated to denote the master tag ID of the initiating bus master, whilst IE_S, IE_C, IE_T are cleared.

Whether a single or dual error is detected is indicated by the IE_DUAL bit. When a data integrity error is detected which causes an update of the DIE information registers and results in an asynchronous DIE trap the IED bit is set and further asynchronous DIE traps are disabled until DIETR.IED is cleared by software.

Data Integrity Error Trap Register (DIETR)

DIETR
Data Integrity Error Trap Register

(F7E1 9024$_H$) **Reset Value: 0000 0000$_H$**



Field	Bits	Type	Description
IED	0	rwh	**Integrity Error Detected** Read Operation: 0_B No data integrity error condition occurred. 1_B Data integrity error condition detected. DIETR and DIEAR contents valid, further DIETR and DIEAR updates disabled. Write Operation: 0_B Clear IED bit, re-enable DIETR and DIEAR update. 1_B No effect.
IE_T	1	rh	**Integrity Error - Tag Memory**
IE_C	2	rh	**Integrity Error - Cache Memory**
IE_S	3	rh	**Integrity Error - Scratchpad Memory**
IE_B	4	rh	**Integrity Error - Bus Access**
E_INFO	[8:5]	rh	**Error Information** If IE_B = 1 : Bus Master Tag ID of requesting master If IE_C = 1 : Cache way.
RES	[10:9]	r	**Reserved** Read as 0; should be written with 0.
IE_DUAL	11	rh	**IE_DUAL** Dual bit error detected.

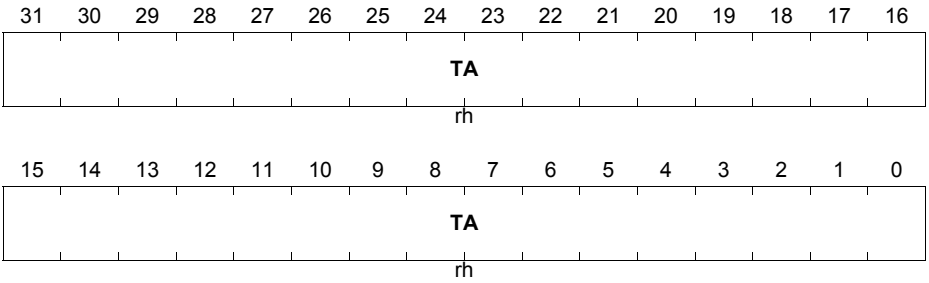
Field	Bits	Type	Description
RES	[31:12]	r	**Reserved** Read as 0; should be written with 0.

Data Integrity Error Address Register

This register contains the physical address accessed by the operation that encountered a uncorrectable data memory integrity error. This register is only updated if DIETR.IED is zero.

DIEAR
Data Integrity Error Address Register

(F7E1 9020$_H$) **Reset Value: 0000 0000$_H$**



Field	Bits	Type	Description
TA	[31:0]	rh	**Transaction Address** Physical address being accessed by operation that encountered data integrity error.

SIST (Software In-System) Test Support

The TriCore 1.6 core protects against memory integrity errors by ECC protection of the on-core memories. This has the side-effect of requiring memory blocks wider than the normal data access path to the memory. The additional ECC storage bits are not easily accessible via the existing data paths, causing problems where SIST based testing of the memories is required. The TriCore 1.6 core also includes embedded memory arrays, such as the tag memories, which are not ordinarily accessible by the usual CPU datapaths. In order to address this problem, the TriCore 1.6 core includes improved SIST support, allowing all on-core memory arrays to be accessed, both as a backup for MBIST based memory test and to allow the test and debug of the new fault tolerant memory systems.

The mapping of embedded memory arrays into the TriCore address space and the enabling of other SIST related features is controlled by the setting of bits within the SIST Mode Access Control Register (SMACON).

The embedded memory arrays are mapped into the program and data scratch areas (Segments C_H and D_H) of the address map by setting bits in the SMACON register. Program side embedded memories are mapped into the PSPR area and located in the address range $C01C0000_H$ - $C01FFFFF_H$.Data side embedded memories are mapped into the DSPR area and located in the address range $D01C0000_H$ - $D01FFFFF_H$. A memory that has been mapped into the scratch memory area using the SMACON register may not be accessed in its normal operational mode.

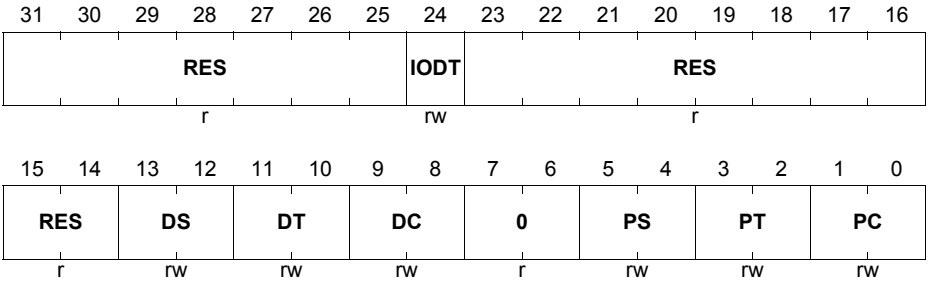
In general no bits of the SMACON register should be set during normal operation. The only exception to this is the mapping of cache to SRAM in hard real time systems in which cache operation is not desired. In such systems the cache memories may be mapped to SRAM for normal operation by setting the SMACON.PC and/or the SMACON.DC bits to “11”.

Note: When the Flash Read Protection (OTP protection) mechanism is active, the value of SMACON.PC is overridden and treated as 00_B 'normal operating mode'; however the field can still be read and written normally.

SIST Mode Access Control Register

SMACON
SIST Mode Access Control Register

(F7E1 900C$_H$) Reset Value: 0000 0000$_H$



Field	Bits	Type	Description
PC	[1:0]	rw	**Instruction Cache Memory SIST mode access control** *Note: When the Flash Read Protection mechanism is active, the value of SMACON.PC is overridden and treated as 00_B 'normal operating mode'; however the field can still be read and written normally.* 00_B Normal Operation, No Mapping. 01_B Data Array Mapping, no error detection/correction. 10_B Check Array Mapping, no error detection/correction. 11_B Data Array Mapping, error detection/correction enabled.
PT	[3:2]	rw	**Program Tag Memory SIST mode access control** 00_B Normal Operation, No Mapping. 01_B Data Array Mapping, no error detection/correction. 10_B Check Array Mapping, no error detection/correction. 11_B Reserved.

Field	Bits	Type	Description
PS	[5:4]	rw	**Program Scratch Memory SIST mode access control** 00_B Normal Operation, No Mapping. 01_B Data Array Mapping, no error detection/correction. 10_B Check Array Mapping, no error detection/correction. 11_B Data Array Mapping, error detection/correction enabled.
RES	[7:6]	r	**Reserved** Read as 0; should be written with 0.
DC	[9:8]	rw	**Data Cache Memory SIST mode access control** 00_B Normal Operation, No Mapping. 01_B Data Array Mapping, no error detection/correction. 10_B Check Array Mapping, no error detection/correction. 11_B Data Array Mapping, error detection/correction enabled.
DT	[11:10]	rw	**Data Tag Memory SIST mode access control** 00_B Normal Operation, No Mapping. 01_B Data Array Mapping, no error detection/correction. 10_B Check Array Mapping, no error detection/correction. 11_B Reserved.
DS	[13:12]	rw	**Data Scratch Memory SIST mode access control** 00_B Normal Operation, No Mapping, Performance Optimised. 01_B Data Array Mapping, no error detection/correction. 10_B Check Array Mapping, no error detection/correction. 11_B Data Array Mapping, error detection/correction enabled.
RES	[23:14]	r	**Reserved** Read as 0; should be written with 0.

Field	Bits	Type	Description
IODT	24	rw	**In-Order Data Transactions** 0_B Normal operation, Non-dependent loads bypass stores. 1_B In-order operation, Loads always flush preceding stores, processor store buffer disabled.
RES	[31:25]	r	**Reserved** Read as 0; should be written with 0.

Control Fields

The control fields within the SMACON register allow individual control of the local memories. Each memory may be mapped to operate in a number of different modes.

Normal operation, No Mapping

No mapping of the memories is performed and normal operation is possible. Embedded memories not usually directly addressable are not accessible in the system address map. Performance optimisations are enabled such that loads may read from the physical memory or associated write buffers.

Data Array Mapping, no error detection/correction

The data array (only) of the memory is made visible in the address map. Writes to the memory will not affect the check bits. Error correction/detection for the memory is disabled. Performance optimisations are disabled such that memory accesses are guaranteed to be performed to the actual memory.

Check Array Mapping, no error detection/correction

The check bit array (only) of the memory is made visible in the address map. Writes to the memory will not affect the data bits. Error correction/detection for the memory is disabled. Performance optimisations are disabled such that memory accesses are guaranteed to be performed to the actual memory.

Data Array Mapping, error detection/correction enabled

The data array of the memory is made visible in the address map. Writes to the memory will update the check bits as per normal operation. Error correction/detection for the memory is enabled. Performance optimisations are disabled such that memory accesses are guaranteed to be performed to the actual memory.

2.12 CPU Slave Interface (CPS) Registers

The CPU Slave Interface (CPS) of the TriCore CPU directly accesses the interrupt service request registers in the CPU from the System Peripheral Bus. The CPS registers are described in detail in the TriCore Architecture Manual.

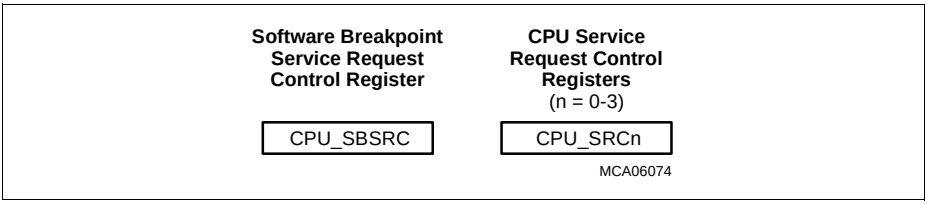


Figure 2-11 CPS Registers

Table 2-10 CPS Registers

Short Name	Description	Offset Address	Access Mode		Reset
			Read	Write	
CPU_SBSRC	CPU Software Breakpoint Service Request Control Register	$FFBC_H$	U, SV, 32	SV, 32	Class 3 Reset $0000\ 0000_H$
CPU_SRC3	CPU Service Request Control 3 Register	$FFF0_H$	U, SV, 32	SV, 32	Class 3 Reset $0000\ 0000_H$
CPU_SRC2	CPU Service Request Control 2 Register	$FFF4_H$	U, SV, 32	SV, 32	Class 3 Reset $0000\ 0000_H$
CPU_SRC1	CPU Service Request Control 1 Register	$FFF8_H$	U, SV, 32	SV, 32	Class 3 Reset $0000\ 0000_H$
CPU_SRC0	CPU Service Request Control 0 Register	$FFFC_H$	U, SV, 32	SV, 32	Class 3 Reset $0000\ 0000_H$

Note: The registers CPU_SBSRC and CPU_SRC[3:0] are not bit-addressable.

2.12.1 Register Descriptions

This registers have a specific implementation detail, the Type of Service Control (TOS) bit/bit field.

CPU Service Request Control Register

Note: The non-shaded areas in the register description define the implementation-specific bits/bit fields. The shaded areas are defined in the TriCore Architecture Manual.

CPU_SRCn (n = 0-3)
CPU Service Request Control Register n

(F7E0 FFFC$_H$-n*4) **Reset Value: 0000 0000$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SETR	CLRR	SRR	SRE	RES	TOS	0		SRPN							
w	w	rh	rw	r	rw	r		rw							

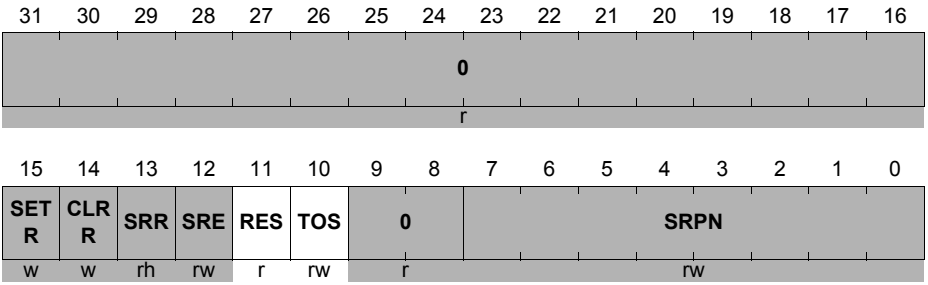
Field	Bits	Type	Description
TOS	10	rw	**Type of Service Control** 0_B Service Provider = CPU 1_B Service Provider = PCP2
RES	11	r	**Reserved** Read as 0; should be written with 0.

CPU Software Breakpoint Service Request Control Register

Note: The non-shaded areas in the register description define the implementation-specific bits/bit fields. The shaded areas are defined in the TriCore Architecture Manual.

CPU_SBSRC
CPU Software Breakpoint Service Request Control Register

(F7E0 FFBC$_H$) **Reset Value: 0000 0000$_H$**



Field	Bits	Type	Description
TOS	10	rw	**Type of Service Control** 0_B Service Provider = CPU 1_B Reserved
RES	11	r	**Reserved** Read as 0; should be written with 0.

2.13 Core Debug and Performance Counter Registers

The Core Debug and performance counter registers are available for debug purposes. For a complete description of all registers, refer to the TriCore Architecture Manual.

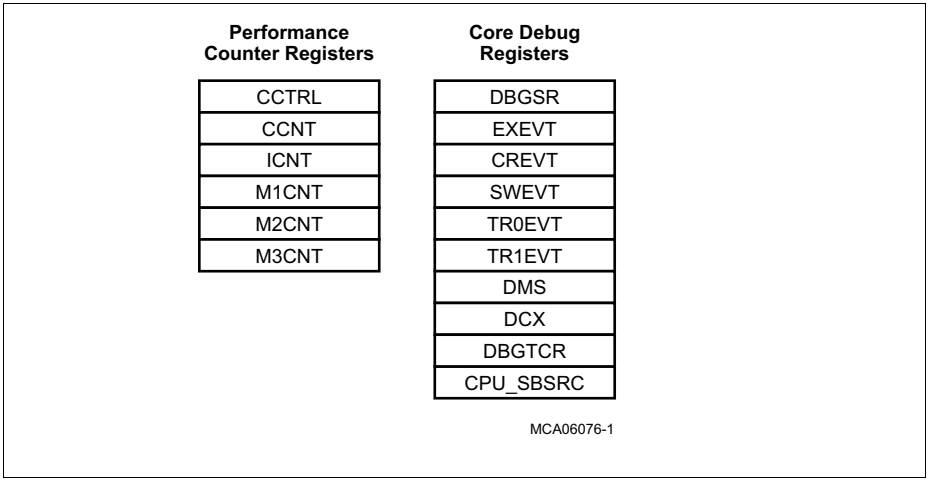


Figure 2-12 Core Debug Registers

Table 2-11 Core Debug and Performance Counter Registers

Short Name	Description	Offset Address	Access Mode		Reset
			Read	Write	
CCTRL	Counter Control Register	$FC00_H$	U, SV, 32	SV, 32	Class 1 Reset 0000 0000_H
CCNT	CPU Clock Count Register	$FC04_H$	U, SV, 32	SV, 32	Class 1 Reset 0000 0000_H
ICNT	Instruction Count Register	$FC08_H$	U, SV, 32	SV, 32	Class 1 Reset 0000 0000_H
M1CNT	Multi-Count Register 1	$FC0C_H$	U, SV, 32	SV, 32	Class 1 Reset 0000 0000_H
M2CNT	Multi-Count Register 2	$FC10_H$	U, SV, 32	SV, 32	Class 1 Reset 0000 0000_H
M3CNT	Multi-Count Register 3	$FC14_H$	U, SV, 32	SV, 32	Class 1 Reset 0000 0000_H
DBGSR	Debug Status Register	$FD00_H$	U, SV, 32	SV, 32	Debug Reset 0000 0000_H

Table 2-11 Core Debug and Performance Counter Registers (cont'd)

Short Name	Description	Offset Address	Access Mode		Reset
			Read	Write	
EXEVT	External Event Register	$FD08_H$	U, SV, 32	SV, 32	Debug Reset 0000 0000$_H$
CREVT	Core Register Access Event Register	$FD0C_H$	U, SV, 32	SV, 32	Debug Reset 0000 0000$_H$
SWEVT	Software Debug Event Register	$FD10_H$	U, SV, 32	SV, 32	Debug Reset 0000 0000$_H$
DMS	Debug Monitor Start Address Register	$FD40_H$	U, SV, 32	SV, 32	Debug Reset A000 0200$_H$
DCX	Debug Context Save Area Pointer Register	$FD44_H$	U, SV, 32	SV, 32	Debug Reset A000 0400$_H$
CPU_SBSRC0	Central Processing Unit Software Breakpoint Service Request Control 0 Register	$FFBC_H$	U, SV, 32	SV, 32	Debug Reset 0000 0000$_H$
TR0EVT	Trigger Event 0 Configuration Register	$F000_H$	U, SV, 32	SV, 32	Debug Reset 0000 0000$_H$
TR0ADR	Trigger Event 0 Address Register	$F004_H$	U, SV, 32	SV, 32	Debug Reset 0000 0000$_H$
TR1EVT	Trigger Event 1 Configuration Register	$F008_H$	U, SV, 32	SV, 32	Debug Reset 0000 0000$_H$
TR1ADR	Trigger Event 1 Address Register	$F00C_H$	U, SV, 32	SV, 32	Debug Reset 0000 0000$_H$
TR2EVT	Trigger Event 2 Configuration Register	$F010_H$	U, SV, 32	SV, 32	Debug Reset 0000 0000$_H$
TR2ADR	Trigger Event 2 Address Register	$F014_H$	U, SV, 32	SV, 32	Debug Reset 0000 0000$_H$
TR3EVT	Trigger Event 3 Configuration Register	$F018_H$	U, SV, 32	SV, 32	Debug Reset 0000 0000$_H$
TR3ADR	Trigger Event 3 Address Register	$F01C_H$	U, SV, 32	SV, 32	Debug Reset 0000 0000$_H$
TR4EVT	Trigger Event 4 Configuration Register	$F020_H$	U, SV, 32	SV, 32	Debug Reset 0000 0000$_H$
TR4ADR	Trigger Event 4 Address Register	$F024_H$	U, SV, 32	SV, 32	Debug Reset 0000 0000$_H$

Table 2-11 Core Debug and Performance Counter Registers (cont'd)

Short Name	Description	Offset Address	Access Mode		Reset
			Read	Write	
TR5EVT	Trigger Event 5 Configuration Register	$F028_H$	U, SV, 32	SV, 32	Debug Reset 0000 0000_H
TR5ADR	Trigger Event 5 Address Register	$F02C_H$	U, SV, 32	SV, 32	Debug Reset 0000 0000_H
TR6EVT	Trigger Event 6 Configuration Register	$F030_H$	U, SV, 32	SV, 32	Debug Reset 0000 0000_H
TR6ADR	Trigger Event 6 Address Register	$F034_H$	U, SV, 32	SV, 32	Debug Reset 0000 0000_H
TR7EVT	Trigger Event 7 Configuration Register	$F038_H$	U, SV, 32	SV, 32	Debug Reset 0000 0000_H
TR7ADR	Trigger Event 7 Address Register	$F03C_H$	U, SV, 32	SV, 32	Debug Reset 0000 0000_H

2.14 Implementation Specific Reset Values

This section summarizes the implementation specific reset values of the CPU registers not defined in this chapter.

Table 2-12 Implementation Specific Reset Values

Register	Address	Reset Value
PCXI	$F7E1\ FE00_H$	$0000\ 0000_H$
CPU_ID	$F7E1\ FE18_H$	$00C0\ C003_H$
FCX	$F7E1\ FE38_H$	$0000\ 0000_H$
LCX	$F7E1\ FE3C_H$	$0000\ 0000_H$
COMPAT	$F7E1\ 9400_H$	$FFFF\ FFFF_H$
ISP	$F7E1\ FE28_H$	$0000\ 0100_H$
BIV	$F7E1\ FE20_H$	$0000\ 0000_H$
BTV	$F7E1\ FE24_H$	$A000\ 0100_H$
FPU_ID	$F7E1\ A020_H$	$00C2\ C003_H$

2.15 CPU Instruction Timing

This section gives information on CPU instruction timing by execution unit. The Integer Pipeline and Load/Store Pipeline are always present, and the Floating Point Unit (FPU) is optional. The Load/Store unit implements the optional TLB instructions.

Definition of Terms:

- **Repeat Rate**

Assuming the same instruction is being issued sequentially, repeat is the minimum number of clock cycles between two consecutive issues. There may be additional delays described elsewhere due to internal pipeline effects when issuing a different subsequent instruction.

- **Result Latency**

The number of clock cycles from the cycle when the instruction is issued to the cycle when the result value is available to be used as an operand to a subsequent instruction or written into a GPR. Result latency is not meaningful for instructions that do not write a value into a GPR.

- **Address Latency**

The number of clocks cycles from the cycle when the instruction is issued to the cycle when the addressing mode updated value is available as an operand to a subsequent instruction or written into an Address Register.

- **Flow Latency**

The number of clock cycles from the cycle when the instruction is issued to the cycle when the next instruction (located at the target location or the next sequential instruction if the control change is conditional) is issued.

2.15.1 Integer-Pipeline Instructions

These are the Integer-Pipeline instruction timings for each instruction.

2.15.1.1 Simple Arithmetic Instruction Timings

Each instruction is single issued.

Table 2-13 Simple Arithmetic Instruction Timing

Instruction	Result Latency	Repeat Rate	Instruction	Result Latency	Repeat Rate
Integer Pipeline Arithmetic Instructions					
ABS	1	1	**MAX.H**	1	1
ABS.B	1	1	**MAX.HU**	1	1
ABS.H	1	1	**MAX.U**	1	1
ABSDIF	1	1	**MIN**	1	1
ABSDIF.B	1	1	**MIN.B**	1	1
ABSDIF.H	1	1	**MIN.BU**	1	1
ABSDIFS	2	1	**MIN.H**	1	1
ABSDIFS.H	2	1	**MIN.HU**	1	1
ABSS	2	1	**MIN.U**	1	1
ABSS.H	2	1	**RSUB**	1	1
ADD	1	1	**RSUBS**	2	1
ADD.B	1	1	**RSUBS.U**	2	1
ADD.H	1	1	**SAT.B**	1	1
ADDC	1	1	**SAT.BU**	1	1
ADDI	1	1	**SAT.H**	1	1
ADDIH	1	1	**SAT.HU**	1	1
ADDS	2	1	**SEL**	1	1
ADDS.H	2	1	**SELN**	1	1
ADDS.HU	2	1	**SUB**	1	1
ADDS.U	2	1	**SUB.B**	1	1
ADDX	1	1	**SUB.H**	1	1
CADD	1	1	**SUBC**	1	1
CADDN	1	1	**SUBS**	2	1

Table 2-13 Simple Arithmetic Instruction Timing (cont'd)

Instruction	Result Latency	Repeat Rate	Instruction	Result Latency	Repeat Rate
CSUB	1	1	**SUBS.H**	2	1
CSUBN	1	1	**SUBS.HU**	2	1
MAX	1	1	**SUBS.U**	2	1
MAX.B	1	1	**SUBX**	1	1
MAX.BU	1	1			
Compare Instructions					
EQ	1	1	**LT.B**	1	1
EQ.B	1	1	**LT.BU**	1	1
EQ.H	1	1	**LT.H**	1	1
EQ.W	1	1	**LT.HU**	1	1
EQANY.B	1	1	**LT.U**	1	1
EQANY.H	1	1	**LT.W**	1	1
GE	1	1	**LT.WU**	1	1
GE.U	1	1	**NE**	1	1
LT	1	1			
Count Instructions					
CLO	1	1	**CLS.H**	1	1
CLO.H	1	1	**CLZ**	1	1
CLS	1	1	**CLZ.H**	1	1
Extract Instructions					
DEXTR	2	1	**INS.T**	1	1
EXTR	2	1	**INSN.T**	1	1
EXTR.U	2	1	**INSERT**	2	1
IMASK	2	1			
Logical Instructions					
AND	1	1	**OR.EQ**	1	1
AND.AND.T	1	1	**OR.GE**	1	1
AND.ANDN.T	1	1	**OR.GE.U**	1	1
AND.EQ	1	1	**OR.LT**	1	1
AND.GE	1	1	**OR.LT.U**	1	1

Table 2-13 Simple Arithmetic Instruction Timing (cont'd)

Instruction	Result Latency	Repeat Rate	Instruction	Result Latency	Repeat Rate
AND.GE.U	1	1	**OR.NE**	1	1
AND.LT	1	1	**OR.NOR.T**	1	1
AND.LT.U	1	1	**OR.OR.T**	1	1
AND.NE	1	1	**OR.T**	1	1
AND.NOR.T	1	1	**ORN**	1	1
AND.OR.T	1	1	**ORN.T**	1	1
AND.T	1	1	**XNOR**	1	1
ANDN	1	1	**XNOR.T**	1	1
ANDN.T	1	1	**XOR**	1	1
NAND	1	1	**XOR.EQ**	1	1
NAND.T	1	1	**XOR.GE**	1	1
NOR	1	1	**XOR.GE.U**	1	1
NOR.T	1	1	**XOR.LT**	1	1
OR	1	1	**XOR.LT.U**	1	1
OR.AND.T	1	1	**XOR.NE**	1	1
OR.ANDN.T	1	1	**XOR.T**	1	1
Move Instructions					
CMOV	1	1	**MOV.U**	1	1
CMOVN	1	1	**MOVH**	1	1
MOV	1	1			
Shift Instructions					
SH	1	1	**SH.NE**	1	1
SH.AND.T	1	1	**SH.NOR.T**	1	1
SH.ANDN.T	1	1	**SH.OR.T**	1	1
SH.EQ	1	1	**SH.ORN.T**	1	1
SH.GE	1	1	**SH.XNOR.T**	1	1
SH.GE.U	1	1	**SH.XOR.T**	1	1
SH.H	1	1	**SHA**	1	1
SH.LT	1	1	**SHA.H**	1	1
SH.LT.U	1	1	**SHAS**	2	1

Table 2-13 Simple Arithmetic Instruction Timing (cont'd)

Instruction	Result Latency	Repeat Rate	Instruction	Result Latency	Repeat Rate
SH.NAND.T	1	1			
Coprocessor 0 Instructions					
BMERGE	2	1	**IXMIN**	2	1
BSPLIT	2	1	**UNPACK**	2	1
PARITY	2	1	**IXMAX**	2	1
PACK	2	1	**IXMAX.U**	2	1
IXMIN.U	2	1			
Integer Divide Instructions					
DVADJ	2	1	**DVSTEP**	6	4
DVINIT	2	1	**DVSTEP.U**	6	4
DVINIT.U	2	1	**DIV**	4-11	3-9
DVINIT.B	2	1	**DIV.U**	4-11	3-9
DVINIT.H	2	1			
DVINIT.BU	2	1			
DVINIT.HU	2	1			

The latency and repeat rate values listed for the DIV and DIV.U instructions are the minimum and maximum values.The algorithm used allows for early termination of the instruction once the full result is available.

2.15.1.2 Multiply Instruction Timings

Each instruction is single issued.

Table 2-14 Multiply Instruction Timing

Instruction	Result Latency	Repeat Rate	Instruction	Result Latency	Repeat Rate
MUL	2	1	**MUL.Q**	3	1
MUL.U	2	1	**MULM.H**	3	1
MULS	3	1	**MULR.H**	3	1
MULS.U	3	1	**MULR.Q**	3	1
MUL.H	3	1			

2.15.1.3 Multiply Accumulate (MAC) Instruction Timing

Each instruction is single issued.

Table 2-15 Multiply Accumulate Instruction Timing

Instruction	Result Latency	Repeat Rate	Instruction	Result Latency	Repeat Rate
MADD	3	1	**MSUB**	3	1
MADD.U	3	1	**MSUB.U**	3	1
MADDS	3	1	**MSUBS**	3	1
MADDS.U	3	1	**MSUBS.U**	3	1
MADD.H	3	1	**MSUB.H**	3	1
MADD.Q	3	1	**MSUB.Q**	3	1
MADDM.H	3	1	**MSUBM.H**	3	1
MADDMS.H	3	1	**MSUBMS.H**	3	1
MADDR.H	3	1	**MSUBR.H**	3	1
MADDR.Q	3	1	**MSUBR.Q**	3	1
MADDRS.H	3	1	**MSUBRS.H**	3	1
MADDRS.Q	3	1	**MSUBRS.Q**	3	1
MADDS.H	3	1	**MSUBS.H**	3	1
MADDS.Q	3	1	**MSUBS.Q**	3	1
MADDSU.H	3	1	**MSUBAD.H**	3	1
MADDSUM.H	3	1	**MSUBADM.H**	3	1
MADDSUMS.H	3	1	**MSUBADMS.H**	3	1
MADDSUR.H	3	1	**MSUBADR.H**	3	1
MADDSURS.H	3	1	**MSUBADRS.H**	3	1
MADDSUS.H	3	1	**MSUBADS.H**	3	1

For All MADD, MSUB and MUL type instructions the result latency is reduced to 1 for accumulator forwarding between similar instructions.

For MADD.Q, MADDS.Q, MSUB.Q, MSUBS.Q Instructions:

MADD.Q, MADDS.Q, MSUB.Q, MSUBS.Q	Result Latency	Repeat Rate
16 × 16	3	1
16 × 32	3	1
32 × 32	3	1

2.15.1.4 Control Flow Instruction Timing

Control flow instruction timing for TriCore1.6 is complicated by the use of branch target buffers and fetch FIFOs.

- Incorrectly predicted LS instructions incur a three cycle branch recovery penalty.
- Incorrectly predicted IP instructions incur a four cycle branch recovery penalty.
- Correctly predicted not taken breaches incur no penalty
- Correctly predicted taken branch incur a penalty of up to two cycles depending on the state of the fetch FIFOs and the branch target buffer.
- Loop instructions incur the same penalty as an LS conditional jump instruction.

Assumptions

- All target locations yield a full instruction in one access (i.e. not 16-bits of a 32-bit instruction).
- All code fetches take a single cycle.
- Timing is best case; no cache misses for context operations, no pending stores.

Table 2-16 Control flow timing

Prediction-Result	Flow Latency (LS, LP)	Repeat rate (LS,LP)	Flow Latency (IP)	Repeat Rate (IP)
Correct Not-Taken	1	1	1	1
Correct Taken	1-2	1-2	1-2	1-2
Incorrect Not-Taken	3	4	3	4
Incorrect Taken	3	4	3	4

2.15.2 Load-Store Pipeline Instructions

This section summarizes the Load-Store Pipeline instructions.

2.15.2.1 Address Arithmetic Timing

Each instruction is single issued.

Table 2-17 Address Arithmetic Instruction Timing

Instruction	Result Latency	Repeat Rate	Instruction	Result Latency	Repeat Rate
Load Store Arithmetic Instructions					
ADD.A	1	1	**GE.A**	1	1
ADDIH.A	1	1	**LT.A**	1	1
ADDSC.A	2	1	**NE.A**	1	1
ADDSC.AT	2	1	**NEZ.A**	1	1
EQ.A	1	1	**SUB.A**	1	1
EQZ.A	1	1	**NOP**	1	1
Trap and Interrupt Instructions					
DEBUG	–	1	**TRAPSV**[1)]	–	1
DISABLE	–	1	**TRAPV**[1)]	–	1
ENABLE	–	1	**RSTV**	–	1
RESTORE	–	1			
Move Instructions					
MFCR	2	1	**MOV.A**	1	1
MTCR	1	1	**MOV.AA**	1	1
MOVH.A	1	1	**MOV.D**	1	1
Sync Instructions					
DSYNC[2)]	–	1	**ISYNC**[3)]	–	1

1) Execution cycles when no TRAP is taken. The execution timing in the case of raising these TRAPs is the same as other TRAPs such as SYSCALL.

2) Repeat rate assumes that no shadow register writeback is pending, otherwise the repeat rate will depend upon the time for all delayed memory operation to occur.

3) Repeat rate assumes that code refetch takes a single cycle.

2.15.2.2 CSA Control Flow Instruction Timing

This section summarizes the timing of CSA Control Flow instructions.

- All targets yield a full instruction in one access (not 16-bits of a 32-bit instruction).
- All code fetches take a single cycle. Timing is best case; no cache misses for context operations, no pending stores.

Table 2-18 CSA Control Flow Instruction Timing

Instruction	Flow Latency	Repeat Rate	Instruction	Flow Latency	Repeat Rate
CALL	4-8	4-8	**SYSCALL**	4-8	4-8
CALLA	4-8	4-8	**SVLCX**	4-8	4-8
CALLI	4-8	4-8	**RSLCX**	4-8	4-8
RET	4-8	4-8	**RFE**	4-8	4-8
BISR	4-8	4-8	**RFM**	4-8	4-8
FCALL	1	1	**FCALLA**	1	1
FCALLI	1	1	**FRET**	1	1

Access to DSPR require 4 cycles, accesses to cached external memory require 8 cycles.

2.15.2.3 Load Instruction Timing

Load instructions can produce two results if they use the pre-increment, post-increment, circular or bit-reverse addressing modes. Hence, in those cases there are two latencies that must be specified, the result latency for the value loaded from memory and the address latency for using the updated address register result.

- Each instruction is single issued.
- The memory references is naturally aligned.
- The memory accessed takes a single cycle to return a data item.
- Timing is best case; no cache misses, no pending stores.

Table 2-19 Load Instruction Timing

Instruction	Address Latency	Result Latency	Repeat Rate	Instruction	Address Latency	Result Latency	Repeat Rate
Load Instructions							
LD.A	1	3	1	**LD.Q**	1	2	1
LD.B	1	2	1	**LD.W**	1	2	1
LD.BU	1	2	1	**LDLCX**	4-8	4-8	4

Table 2-19 Load Instruction Timing (cont'd)

Instruction	Address Latency	Result Latency	Repeat Rate	Instruction	Address Latency	Result Latency	Repeat Rate
LD.D	1	2	1	**LDUCX**	4-8	4-8	4
LD.DA	1	3	1	**SWAP.W**	2	3	2
LD.H	1	2	1	**LEA**[1)]	–	1	1
LD.HU	1	2	1				

1) The addressing mode returning an updated address is not relevant for this instruction.

2.15.2.4 Store Instruction Timing

Cache and Store instructions similar to Load instructions will have a result for the pre-increment, post-increment, circular or bit-reverse addressing modes, but do not produce a ‘memory’ result.

- Each instruction is single issued.
- The memory references is naturally aligned.
- The memory accessed takes a single cycle to accept a data item.
- Timing is best case; no cache misses, no pending stores.

Table 2-20 Cache and Store Instruction Timing

Instruction	Address Latency	Repeat Rate	Instruction	Address Latency	Repeat Rate
Cache Instructions					
CACHEA.I	1	1	**CACHEA.WI**[1)]	1	1
CACHEA.W[1)]	1	1	**CACHEI.W**	1	1
CACHEI.WI	1	1	**CACHEI.I**	1	1
Store Instructions					
ST.A	1	1	**ST.T**	1	2
ST.B	1	1	**ST.W**	1	1
ST.D	1	1	**STLCX**	1	4-8
ST.DA	1	1	**STUCX**	1	4-8
ST.H	1	1	**LDMST**	1	2
ST.Q	1	1			

1) Repeat rate assumes that no memory writeback operation occurs. Otherwise the repeat rate will depend upon the time for the castout buffers to clear.

2.15.3 Floating Point Pipeline Timing

These instructions are only valid if the optional Floating Point Unit is implemented.

Each instruction is single issued.

Table 2-21 Floating Point Instruction Timing

Instruction	Result Latency	Repeat Rate	Instruction	Result Latency	Repeat Rate
Floating Point Instructions					
ADDF	2	1	**ITOF**	2	1
CMP.F	1	1	**MADD.F**	3	1
DIV.F	8	6	**MSUB.F**	3	1
FTOI	2	1	**MUL.F**	2	1
FTOIZ	2	1	**Q31TOF**	2	1
FTOQ31	2	1	**QSEED.F**	1	1
FTOQ31Z	2	1	**SUB.F**	2	1
FTOU	2	1	**UPDFL**	–	1
FTOUZ	2	1	**UTOF**	2	1

2.16 Program Memory Interface (PMI)

Figure 2-13 shows the block diagram of the Program Memory Interface (PMI) of the TC1798.

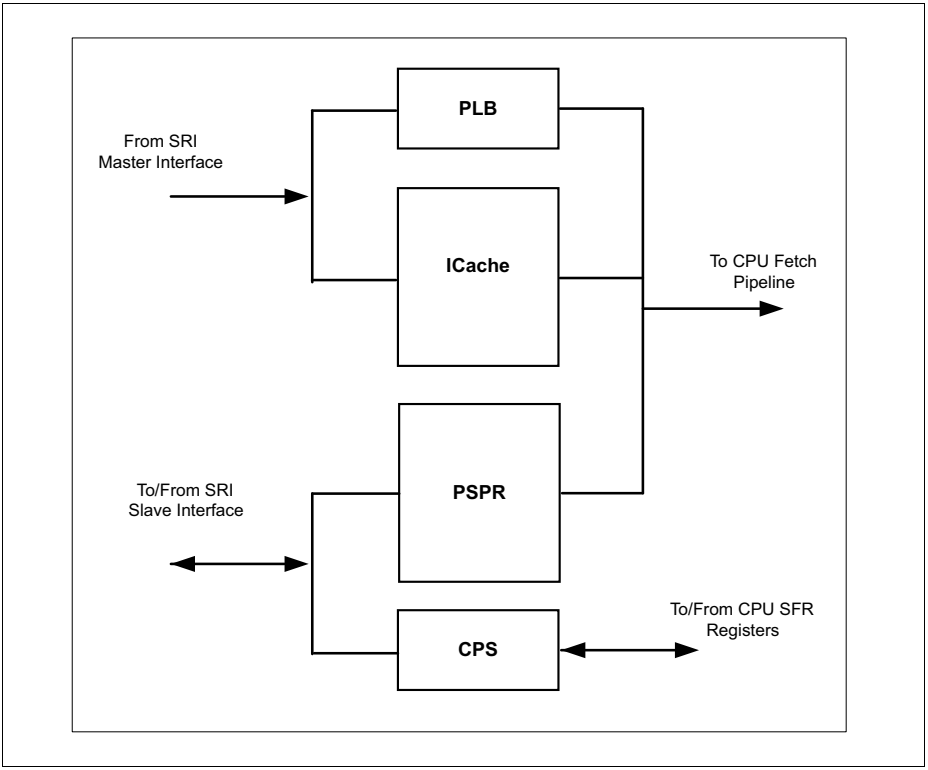


Figure 2-13 PMI Block Diagram

2.16.1 PMI Features

The Program Memory Interface (PMI) has the following features:

- 16 Kbyte Program Cache (ICACHE)
  - Four-way set associative cache
  - PLRU (Pseudo Least-Recently Used) replacement algorithm
  - Cache line size: 256 bits (4 double-words)
  - Validity granularity: One valid bit per cache line
  - ICACHE can be globally invalidated to provide support for software cache coherency (to be handled by the programmer)

  - ICACHE can be bypassed to provide a direct fetch from the CPU to on-chip and off-chip resources
  - ICACHE refill mechanism:
    Critical word first, line wrap around, streaming to CPU
- 32 Kbyte Program Scratchpad memory (PSPR)
- CPU interface
  - Supporting 64bit aligned fetches.
- CPU Slave interface (CPS)
- Shared Resource Interconnect Bus (SRI) Master Interface
- Shared Resource Interconnect Bus (SRI) Slave Interface to scratchpad RAM and CPS.
- All PMI SRAMs (PSPR, ICACHE, and cache tag SRAM) are ECC protected
  - ECC is calculated on address and data for the PSPR and ICACHE

2.16.2 Scratchpad RAM

The TC1798 contains 32 Kbyte of Program scratchpad RAM. Scratchpad RAM provides a fast, deterministic program fetch access from the CPU for use by performance critical code sequences.

- CPU program fetch accesses to scratchpad RAM are never cached in the instruction cache and are always directly targeted to the scratchpad RAM.

The CPU fetch interface will generate aligned accesses (64-bit), which will result in 64-bits of instruction being returned to the CPU.

Note that the CPU Fetch Unit can only read from the scratchpad RAM and can never write to it.

The scratchpad RAM may also be accessed from the SRI Slave interface by another bus master, such as the Data Memory Interface (DMI). The scratchpad RAM may be both read and written from the SRI. In the TC1798, the SRI Slave interface supports all SRI transaction types.

The scratchpad RAM is ECC protected across both address and data.

2.16.3 Instruction Cache

The TC1798 contains up to 16 Kbyte of Instruction Cache (ICACHE). The ICACHE is a four-way set-associative cache with a Pseudo Least-Recently-Used (PLRU) replacement algorithm. Each ICACHE line contains 256 bits of instruction along with a single associated valid bit and associated ECC bits.

CPU program fetch accesses which target a cacheable memory segment (and where the ICACHE is not bypassed) target the ICACHE. If the requested address and its associated instruction are found in the cache (Cache Hit), the instruction is passed to the CPU Fetch Unit without incurring any wait states. If the address is not found in the cache (Cache Miss), the PMI cache controller issues a cache refill sequence and wait states

are incurred whilst the cache line is refilled. The fetch request always returns an aligned 64bit packet to the CPU.

The Instruction cache is ECC protected on both address and data. The Instruction TAG Ram is ECC protected on data.

Instruction Cache Refill Sequence

Instruction Cache refills are performed using a critical double-word first strategy with cache line wrapping such that the refill size is always 4 double-words. ICACHE refills are always performed in 64-bit quantities. A refill sequence will always affect only one cache line. There is no prefetching of the next cache line.

ICACHE refills are therefore implemented using an SRI Burst Transfer 4 (BTR4) transfers. The Instruction Cache supports instruction streaming, meaning that it can deliver available instruction half-words to the CPU Fetch Unit whilst the refill operation is ongoing.

Instruction Cache Bypass

The Instruction Cache may be bypassed, under control of PCON0.PCBYP, to provide a direct instruction fetch path for the CPU Fetch Unit. The default value of PCON0.PCBYP is such that the ICACHE is bypassed after reset. ICACHE bypass should be disabled during initialization to enable the ICACHE.

Whilst ICACHE bypass is enabled, a fetch request by the CPU to a cacheable address will result in a forced cache miss, such that the cache controller issues a standard refill sequence and supplies instruction half-words to the CPU using instruction streaming, without updating the cache contents. Any valid cache lines within the ICACHE will remain valid and unchanged whilst the ICACHE is bypassed. As such, instruction fetch requests to cacheable addresses with ICACHE bypass enabled behave identically to instruction fetch requests to non-cacheable addresses.

Instruction Cache Invalidation

The PMI does not have automatic cache coherency support. Changes to the contents of memory areas external to the PMI that may have already been cached in the ICACHE are not detected. Software must provide the cache coherency in such a case. The PMI supports this via the cache invalidation function. The ICACHE contents may be globally invalidated by writing a ‘1’ to PCON1.PCINV. The ICACHE invalidation is performed over 128 cycles by a hardware state machine which cycles through the ICACHE entries marking each as invalid. During an invalidate sequence the CPU may continue to fetch instructions from non-cacheable memory. Any attempt to fetch instructions from a cacheable memory location during an invalidation sequence will result in the CPU stalling until the sequence completes. The status of the ICACHE invalidation sequence may be determined by reading the PCON1.PCINV bit.

2.16.4 Program Line Buffer

The PMI module contains a 256-bit Program Line Buffer (PLB). Program fetch requests to non-cacheable addresses (or to cacheable addresses with the cache in bypass) utilize the PLB as a single line cache. A single valid bit is associated with the PLB, denoting that the PLB contents are valid. As such all fetch requests resulting in an update of the PLB, whether to a cacheable address or not, are implemented as SRI Burst Transfer 4 (BTR4) transactions, with the critical double-word of the PLB line being fetched first size. The PLB may be invalidated by writing PCON1.PBINV.

The PLB is ECC protected on both address and data.

2.16.5 CPU Slave Interface (CPS)

The CPU Slave Interface provides access from the SRI bus to the core CSFR and SFR registers.

2.16.6 PMI Registers

Three control registers are control the operation of the Program Memory Interface. These registers and their bits are described in this section.

Table 2-22 PMI Registers

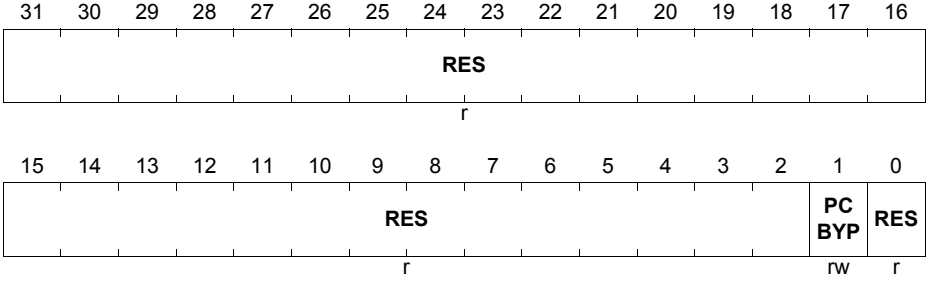
Short Name	Description	Offset Address	Access Mode		Reset
			Read	Write	
PCON0	PMI Control Register 0	$920C_H$	U, SV, 32	SV, 32	Class 3 Reset $0000\ 0002_H$
PCON1	PMI Control Register 1	9204_H	U, SV, 32	SV, 32	Class 3 Reset $0000\ 0000_H$
PCON2	PMI Control Register 2	9208_H	U, SV, 32	SV, E, 32	Class 3 Reset $0020\ 0010_H$
PMI_STR	PMI Synchronous Trap Register	9200_H	U, SV, 32	SV, 32	Class 3 Reset $0000\ 0000_H$

2.16.6.1 PMI Register Descriptions

PMI Control Register 0

PCON0
Program Memory Control Register 0

(F7E1 920C$_H$) **Reset Value: 0000 0002$_H$**

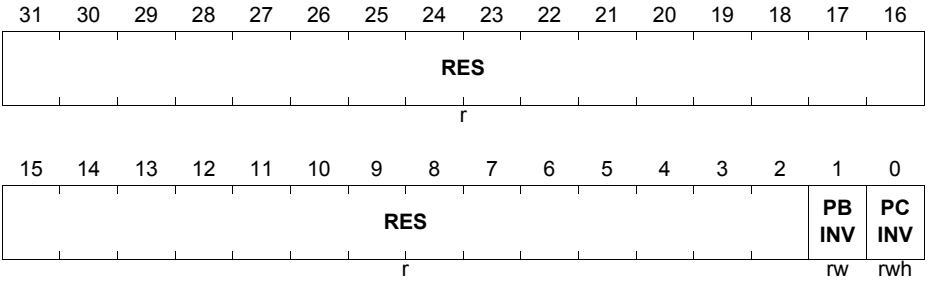


Field	Bits	Type	Description
RES	0	r	**Reserved** Read as 0; should be written with 0.
PCBYP	1	rw	**Instruction Cache Bypass** 0_B Cache enabled 1_B Cache bypassed (disabled)
RES	[31:2]	r	**Reserved** Read as 0; should be written with 0.

PMI Control Register 1

PCON1

Program Memory Control Register 1 (F7E1 9204$_H$) **Reset Value: 0000 0000$_H$**



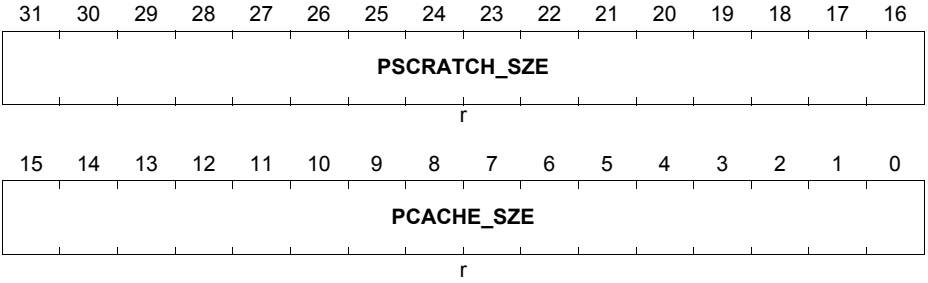
Field	Bits	Type	Description
PCINV	0	rwh	**Instruction Cache Invalidate** Write Operation: 0_B No effect. Normal instruction cache operation. 1_B Initiate invalidation of entire instruction cache. Read Operation: 0_B Normal operation. Instruction cache available. 1_B Instruction cache invalidation in progress. Instruction cache unavailable.
PBINV	1	rw	**Program Buffer Invalidate** Write Operation: 0_B No effect. Normal program line buffer operation. 1_B Invalidate the program line buffer. This field returns 0 when read.
RES	[31:2]	r	**Reserved** Read as 0; should be written with 0.

PMI Control Register 2

PCON2 contains size information for the Program memory system.

PCON2
Program Memory Control Register 2

(F7E1 9208$_H$) **Reset Value: 0020 0010$_H$**



Field	Bits	Type	Description
PCACHE_SZE	[15:0]	r	**Program Cache (ICACHE) Size** In KBytes
PSCRATCH_SZE	[31:16]	r	**Program Scratch Size** In KBytes

Program Memory Interface Synchronous Trap Register (PSTR)

PSTR contains synchronous trap information for the program memory system. The register is updated with trap information for PSE traps to aid the localisation of faults.

The register is only set whenever a trap is detected and the register has no bits already set. It is cleared by a CSFR write (independent of data value).

PSTR
Program Synchronous Trap Register
(F7E1 9200$_H$) **Reset Value: 0000 0000$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RES	FME	RES	FPE	RES									FBE	FGAE	FRE
r	rwh	r	rwh	r									rwh	rwh	rwh

Field	Bits	Type	Description
FRE	0	rwh	**Fetch Range Error**
FGAE	1	rwh	**Fetch Global Address Error**
FBE	2	rwh	**Fetch Bus Error**
RES	[11:3]	r	**Reserved**
FPE	12	rwh	**Fetch Peripheral Error**
RES	13	r	**Reserved**
FME	14	rwh	**Fetch MSIST Error**
RES	[31:15]	r	**Reserved**

Fetch Range Error

A Fetch Range Error occurs whenever an access to the Program Scratch is outside the range of the SRAM.

Fetch Global Address Error

A Fetch Global Address Error occurs whenever an there is access to an address that cannot be translated to a valid global address.This will occur for accesses in the range D1000000 to D7FFFFFF

Fetch Bus Error

A Fetch bus error will be set whenever the SRI flags an error due a fetch from external memory. This will be set for both direct fetches from the bus and for cache refills.

Fetch Peripheral Error

A Fetch peripheral error will be flagged whenever a fetch is attempted to peripheral space.

Fetch MSIST Error

During SIST mode, a fetch from the PTAG will cause a PSE trap to occur.

2.17 Data Memory Interface (DMI)

This figure shows the block diagram of the Data Memory Interface (DMI) of the TC1798.

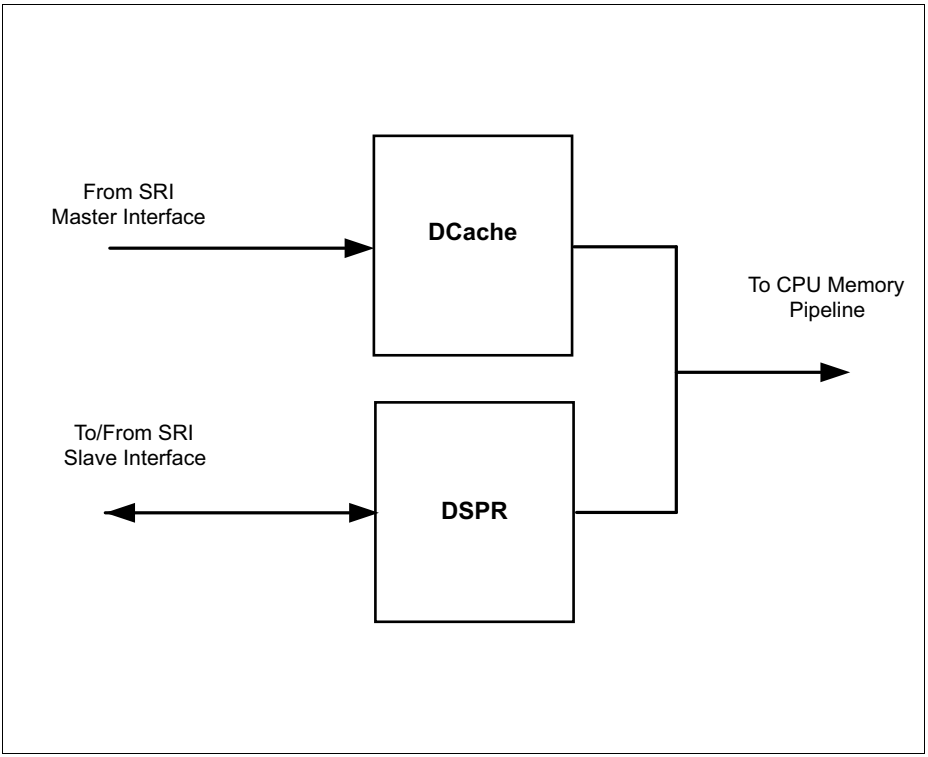


Figure 2-14 DMI Block Diagram

2.17.1 DMI Features

The Data Memory Interface (DMI) has the following features:

- 128 Kbyte Data Scratchpad Ram (DSPR)
  - Supporting unaligned access (16-bit aligned) with no penalty.
- 16 Kbyte Data Memory (DCACHE):
  - Four-way set associative cache, Pseudo least recently used (PLRU) replacement algorithm
  - Cache line size: 256 bits
  - Validity granularity: One valid bit per cache line
  - Write-back Cache: Writeback granularity: 256 bits
  - Refill mechanism: full cache line refill

- CPU interface
- Shared Resource Interface Bus (SRI) Master interface
- Shared Resource Interface (SRI) Slave interface to DSPR
-
- All DMI SRAMs (DSPR, DCACHE, and cache tag SRAM) are ECC protected

2.17.2 Data Scratchpad RAM (DSPR)

The TC1798 contains 128 Kbyte of DSPR. DSPR provides fast, deterministic data access to the CPU for use by performance critical code sequences.

The DSPR is organised as multiple memory “towers”. This organisation allow the CPU to access 64bits of data from any 16bit aligned address

The DSPR may also be accessed from the SRI Slave interface by another bus master, with both read and write transactions supported. The DSPR may be accessed by the SRI Slave interface using any SRI transaction type, including burst transfers. In accordance with the SRI protocol, accesses to the SRI Slave interface must be naturally aligned.

2.17.3 Data Cache

The TC1798 contains 16 KByte of Data Cache (DCache). The DCache is a four-way set-associative cache with a Pseudo Least-Recently-Used (PLRU) replacement algorithm. Each line contains 256 bits of data along with ECC bits. A single valid bit and a single dirty bit are associated with each line.

CPU data accesses to a cacheable memory segment target the DCache. If the requested address and its associated data are found in the cache (Cache Hit), the data is passed to/from the CPU Load-Store Unit without incurring any wait states. If the address is not found in the cache (Cache Miss), the DMI cache controller issues a cache refill sequence and wait states are incurred whilst the cache line is refilled. The CPU load-store interface will generate unaligned accesses (16-bit aligned), which will result in up to 64-bits of data being transferred to or from the CPU (for non-context operations). If the data access is made within a DCache line, no matter the alignment, and a cache hit is detected then the requested data is returned to the CPU in a single cycle. If the data access is made to the end of a DCache line, such that the requested data would span two DCache lines, a single wait cycle is incurred (if both cache lines are present in the cache, otherwise a refill sequence is required for the missing cache line(s)).

The TC1798 data cache is of the writeback type. When the CPU writes to a cacheable location the data is merged with the corresponding cache line and not written to main memory immediately. Associated with each cache line is a single ‘dirty’ bit, to denote that the data in the cache line has been modified. Whenever a CPU load-store access results in a cache miss, and each of the potential cache ways that could hold the requested cache line are valid, one of the cache lines is chosen for eviction based upon the PLRU replacement algorithm. The line selected for eviction is then checked to determine if it

has been modified using its dirty bit. If the line has not been modified the line is discarded and the refill sequence started immediately. If the line has been modified then the dirty data is first written back to main memory before the refill is initiated. Due to the single dirty bit per cache line, 256 bits of data will always be written back, resulting in a SRI Burst-4 Transfer (BTR4) transactions.

Data Cache refills always result in the full cache line being refilled, with the critical double-word of the DCache line being fetched first. A refill sequence will always affect only one cache line. There is no prefetching of the next cache line. Due to the uniform size of DCache refill sequences, such refills are always implemented using SRI Burst Transfer 4 (BTR4) transactions.

2.17.4 DMI Trap Generation

CPU data accesses to the DMI may encounter one of a number of potential error conditions, which result in one of the following trap conditions being reported by the DMI.

ALN Trap

An ALN trap is raised for the following conditions:

- An access whose effective address does not conform to the alignment rules
- An access where the length, size or index of a circular buffer is incorrect

Whenever an ALN trap occurs, the DSTR (Data Synchronous Trap Register) and the DEADD (Data Error Address Register) CSFRs are updated.

MEM Trap

A MEM trap is raised for the following conditions:

- An access whose effective address has a different segment to that of the base address (Segment Difference Error)
- An access whose effective address causes the data to span two segments (Segment Crossing Error)
- A memory address is used to access a CSFR area (CSFR Access Error)

Whenever a MEM trap occurs, the DSTR (Data Synchronous Trap Register) and the DEADD (Data Error Address Register) CSFRs are updated.

DSE Trap

A DSE trap is raised for the following conditions:

- An access outside the range of the DSPR (Scratch Range Error)
- An access to the lower half of segment C which cannot be translated into a global address, i.e. from C1000000 to C7FFFFFF (Global Address Error)
- An error on the bus for an external accesses due to a load (Load Bus Error)
- An error from the bus during a cache refill (Cache Refill Error)

- An error during a load whilst in SIST mode (Load MSIST Error)
- An error generated by the overlay system during a load.

Whenever a DSE trap occurs, the DSTR (Data Synchronous Trap Register) and the DEADD (Data Error Address Register) CSFRs are updated.

DAE Trap

A DAE trap is raised for the following conditions:

- An error on the bus for an external accesses due to a store (Store Bus Error)
- An error on the bus due to a cache writeback (Cache writeback Error)
- An error from the bus due to a cache flush (Cache Flush Error)
- An error due to a store whilst in SIST mode (Store MSIST Error)
- An error generated by the overlay system during a store.

Whenever a DAE trap occurs, the DATR (Data Synchronous Trap Register) and the DEADD (Data Error Address Register) CSFRs are updated.

Data Memory Protection Traps

Data memory protection traps (MPW, MPR, MPP, MPN) are raised by the memory protection system when a protection violation occurs. Whenever a data memory protection trap occurs the DSTR (Data synchronous trap register) and the DEADD (Data Error Address Register) are updated.

2.18 Memory Configuration

The TC1.6 memories are configured as follows:-

Table 2-23 Memory Configuration

Processor	Program Cache	Program Scratchpad	Data Cache	Data Scratchpad
TC1.6	16K Bytes	32 KBytes	16 KBytes	128 KBytes

The cache and tag memories may be mapped into the CPUs address space using the SMACON register. When mapped the locations of these memories is as follows.

The CACHEI.* instructions require a way and index value to be supplied in a valid address. The location of these bits in the 32bit address is as follows.

Table 2-24 Way and Index Location

Function	Address Bits
Way	[1:0]
Index	[11:5]

2.18.1 DMI Registers

Two control registers and three trap flag registers control the operation of the DMI. These registers and their bits are described in this section.

Table 2-25 DMI Registers

Short Name	Description	Offset Address	Access Mode		Reset
			Read	Write	
DCON0	DMI Control Register 0	9040_H	U, SV, 32	SV, E, 32	Class 3 Reset $0000\ 0002_H$
DCON2	DMI Control Register 2	9000_H	U, SV, 32	SV, E, 32	Class 3 Reset $0800\ 0010_H$
DSTR	DMI Synchronous Trap Flag Register	9010_H	U, SV, 32[1)]	SV, 32	Class 3 Reset $0000\ 0000_H$
DATR	DMI Asynchronous Trap Flag Register	9018_H	U, SV, 32[1)]	SV, 32	Class 3 Reset $0000\ 0000_H$
DEADD	DMI Data Error Address Register	$901C_H$	U, SV, 32	SV, 32	Class 3 Reset $0000\ 0000_H$

1) Writing these registers clears the contents independent of the data value.

.

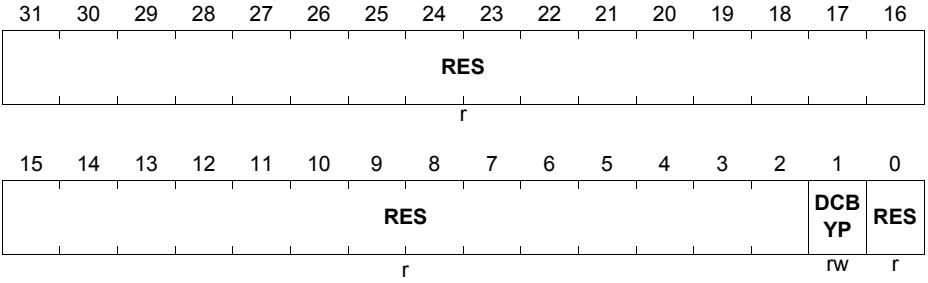
2.18.1.1 DMI Register Descriptions

Note: There is no DCON1 register in this implementation.

Data Memory Control Register 0 (DCON0)

The DCON0 register allows the Data cache to be bypassed.

DCON0
Data Memory Control Register (F7E1 9040$_H$) Reset Value: 0000 0002$_H$

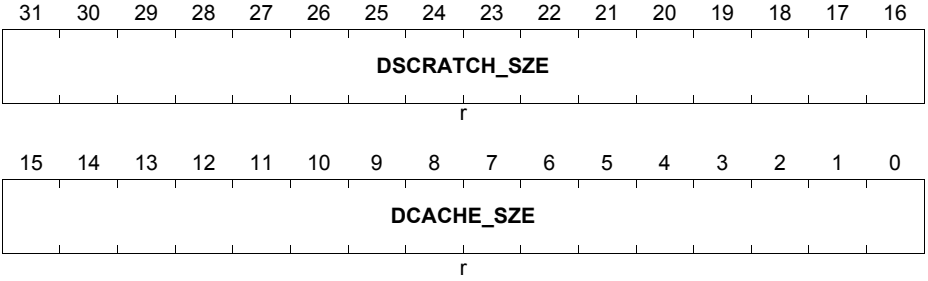


Field	Bits	Type	Description
RES	0	-	**Reserved**
DCBYP	1	rw	**Data Cache Bypass** 0_B Cache enabled 1_B Cache Bypass (disabled)
RES	[31:2]	-	**Reserved**

Data Control Register 2 (DCON2)

DCON2 contains size information for the Data memory system.

DCON2
Data Control Register 2 **(F7E1 9000$_H$)** **Reset Value: 0080 0010$_H$**



Field	Bits	Type	Description
DCACHE_SZE	[15:0]	r	**Data Cache Size** In KBytes
DSCRATCH_SZE	[31:16]	r	**Data Scratch Size** In KBytes

DMI Synchronous Trap Flag Register

The DSTR contains synchronous trap information for the data memory system. The register is updated with trap source information to aid the localisation of faults.

The register is updated whenever a valid trap is detected and the register has no bits already set. It is cleared by a write (independent of data value).

DSTR

Data Synchronous Trap Register (F7E1 9010$_H$) **Reset Value: 0000 0000$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES							ALN	RES					CAC	SCE	SDE
r							rwh	r					rwh	rwh	rwh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LOE	DTME	RES							CRE	RES			LBE	GAE	SRE
rwh	rwh	r							rwh	r			rwh		rwh

Field	Bits	Type	Description
SRE	0	rwh	**Scratch Range Error**
GAE	1	rwh	**Global Address Error**
LBE	2	rwh	**Load Bus Error**
RES	[5:3]	r	**Reserved**
CRE	6	rwh	**Cache Refill Error**
RES	[13:7]	r	**Reserved**
DTME	14	rwh	**DTAG MSIST Error**
LOE	15	rwh	**Load Overlay Error**
SDE	16	rwh	**Segment Difference Error**
SCE	17	rwh	**Segment Crossing Error**
CAC	18	rwh	**CSFR Access Error**
RES	[23:19]	r	**Reserved**
ALN	24	rwh	**Alignment Error**
RES	[31:25]	r	**Reserved**

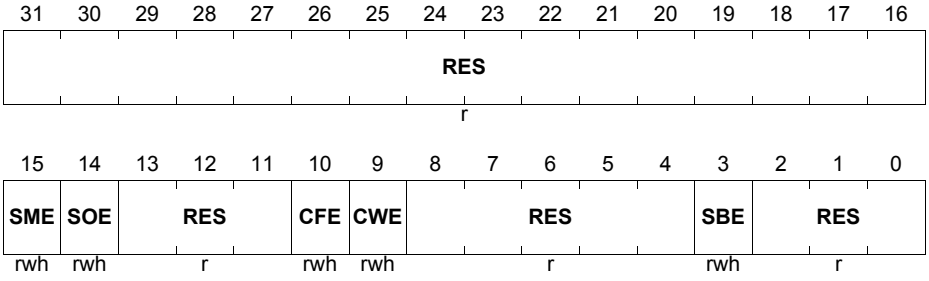
DMI Asynchronous Trap Flag Register

The DATR contains asynchronous trap information for the data memory system. The register is updated with trap information for DAE traps to aid the localisation of faults.

The register is updated whenever a valid trap is detected and the register has no bits already set. It is cleared by a write (independent of data value).

DATR

Data Asynchronous Trap Register(F7E1 9018$_H$) **Reset Value: 0000 0000$_H$**



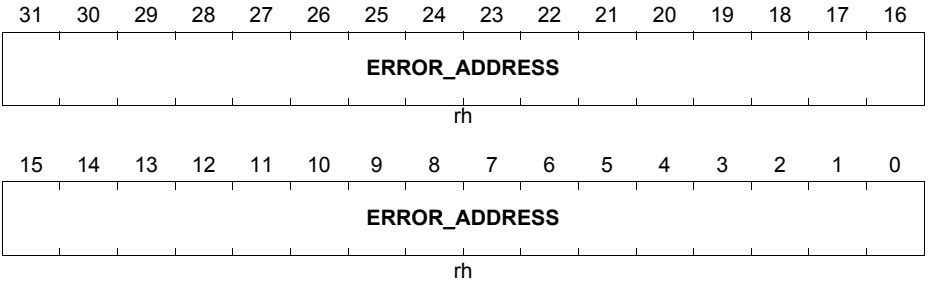
Field	Bits	Type	Description
RES	[2:0]	r	**Reserved**
SBE	3	rwh	**Store Bus Error**
RES	[8:4]	r	**Reserved**
CWSE	9	rwh	**Cache Writeback Error**
CFSE	10	rwh	**Cache Flush Error**
RES	[14:11]	r	**Reserved**
SOE	[14]	rwh	**Store Overlay Error**
SME	15	rwh	**Store MIST Error**
RES	[31:16]	r	**Reserved**

Data Error Address Register

DEADD contains trap address information for the Data memory system. The register is updated with trap information for MEM, ALN, DSE or DAE traps to aid the localisation of faults.

The register is only set whenever a trap is detected and either the DATR or DSTR registers have no bits already set.

DEADD
Data Error Address Register (F7E1 901C$_H$) Reset Value: 0000 0000$_H$



Field	Bits	Type	Description
ERROR_ADDRESS	[31:0]	rh	**Error Address**

2.19 Safety Features

The TC1798 implements a number of safety concepts. As part of this the TriCore1.6 core implements the following features:-

- SRI Address Phase Error Injection
- SRI Data Phase Error Capture
- Safety Interrupt Acknowledge Decoupling

2.19.1 SRI Address Phase Error Injection

To allow the SRI address phase error detection system to be tested it is necessary to inject errors during the read phase of an SRI address transaction. This is done by selectively inverting individual bits of the SRI read or write phase ECC packet and is controlled using the SFAGEN register. The SFAGEN register contains two fields:- an enable (AE) and a bit flip (ADFLIP) field. When enabled the address ECC bits indicated by the flip field are inverted for the next SRI data read or write bus transaction performed by the DMI. Following the transaction the enable bit is cleared by hardware. This mechanism allows selected bits of the SRI address ECC to be corrupted for a single transaction.

2.19.2 SRI Data Phase Error Capture

Error information detected during the SRI read data phase as the result of a PMI fetch is captured in the SFERR0 and SFERR1 registers. Such an error will typically result in a PIE trap. On detection of an error the error information is captured and the SFERR0.E_VAL bit is set. No further error information is captured until this bit is cleared by software.

2.19.3 Safety Interrupt Acknowledge Decoupling

In standard operation a successfully requesting interrupt node is automatically acknowledged and cleared down by hardware. This is done as part of the interrupt entry sequence performed by the TriCore and before the start of the Interrupt Service Routine (ISR). An ISR is therefore unable to verify that the interrupt node corresponding to its level is active.

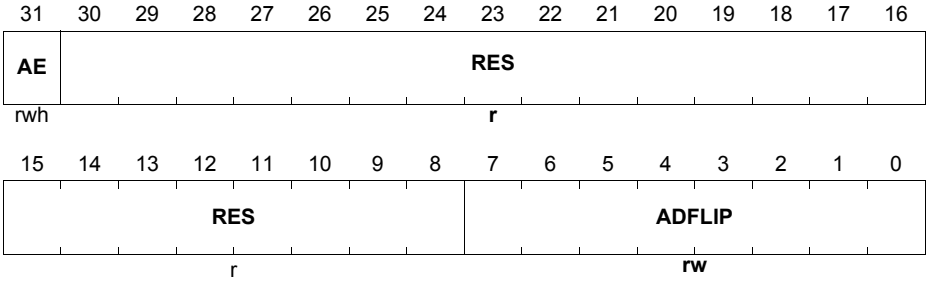
In safety systems such verification is desirable. The Tricore1.6 may be operated in a “Safe Interrupt” mode in which the acknowledgment and clearing of the requesting node is decoupled from the Interrupt entry sequence hence allowing an ISR to inspect the requesting node to verify correct operation. This mode is enabled by clearing the COMPAT.INT bit. The ISR is responsible for acknowledging and clearing down the interrupt node by clearing the SAFEINT.INT bit

2.19.4 Registers Implementing Safety Features

Safe Fetch Address Error Generation Register

The SFAGEN register controls the injection of SRI address phase errors from the DMI.

SFAGEN
Safe Fetch Address Error Generation Register ($F7E1\ 1030_H$) **Reset Value: $0000\ 000_H$**



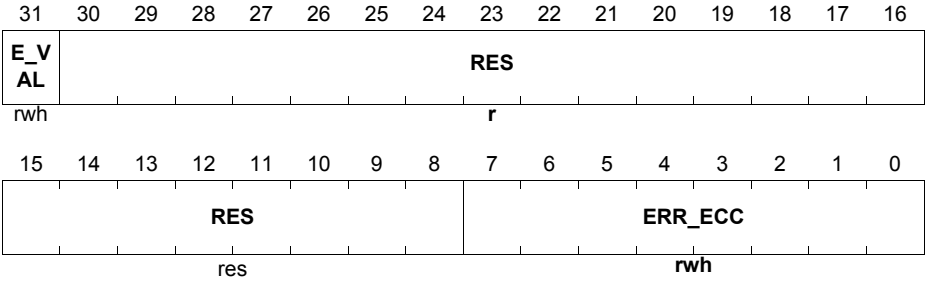
Field	Bits	Type	Description
ADFLIP	[7:0]	rw	**Address ECC bit flip** SRI address ECC Bits to be flipped on the next read or write transaction from the DMI when enabled by AE. 0_B No Flip 1_B Flip
RES	[30:8]	r	**Reserved**
AE	31	rwh	**Address Error Enable** Enabled the selective inverting of SRI address phase ECC packet bits defined by ADFLIP. This bit will be cleared by hardware after the next SRI read or write transaction from the DMI. 0_B Not Enabled 1_B Enabled

Safe Fetch Error Register 0

The SFERR0 register captures read data phase error information on safe fetch errors from the PMI.

SFERR0

Safe Fetch Error Register 0 **(F7E1 1000$_H$)** **Reset Value: 0000 000$_H$**

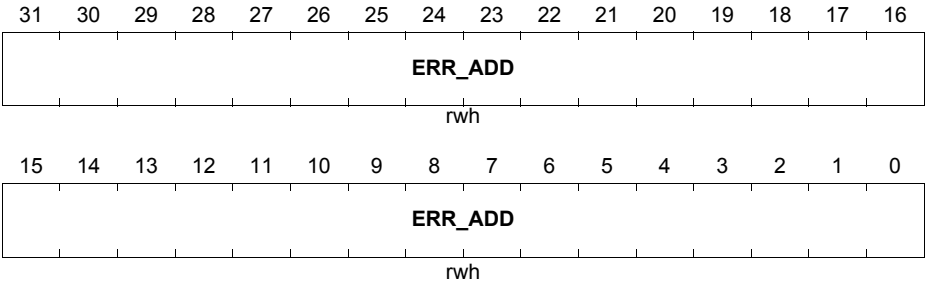


Field	Bits	Type	Description
ERR_ECC	[7:0]	rwh	**Error ECC** The ERR information of the erroneous SRI packet
RES	[30:8]	-	**Reserved**
E_VAL	31	rwh	**Error Valid** An error has been detected since the register was last cleared

Safe Fetch Error Register 1

SFERR1

Safe Fetch Error Register 1 **(F7E1 1004$_H$)** **Reset Value: 0000 000$_H$**

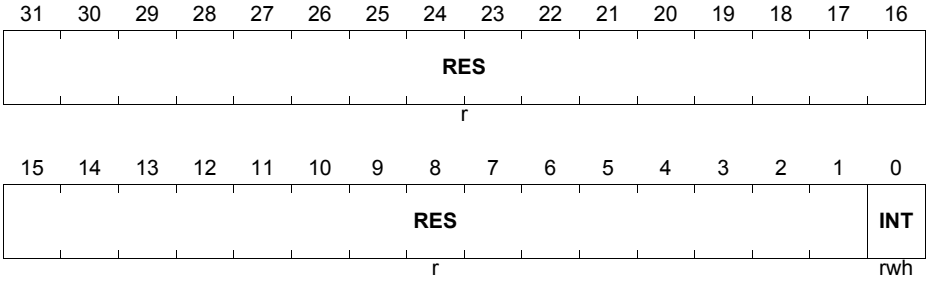


Field	Bits	Type	Description
ERR_ECC	[31:0]	rwh	**ERR_ADD** The Address of the erroneous SRI packet

Safe Interrupt register

In order to improve plausibility checks on Interrupt Service Routines (ISR) The acknowledgement of interrupts may be decoupled from interrupt entry. When interrupt entry occurs the SAFEINT.INT bit is set. The interrupt acknowledge is delayed until the register is written to zero.

SAFEINT
Safe Interrupt Register **(0xFe30)** **Reset value: 0000 0000$_H$**



Field	Bits	Type	Description
INT	0	rwh	**Interrupt Active** Read: 0 = Interrupt Inactive Read: 1 = Interrupt Active Write: 0 = Clear Safe Interrupt Write: 1 = No effect
RES	[31:1]	r	**Reserved**

3 System Control Unit (SCU)

The System Control Unit (SCU) of the TC1798 handles all system control tasks beside the debug related tasks which are controlled by the OCDS/Cerberus.

The SCU contains the following functional sub-blocks:

- Clock Control (see **Section 3.1**)
- Reset Operation (see **Section 3.2**)
- External Interface (see **Section 3.3**)
- Power Management (see **Section 3.4**)
- Software Boot Support (see **Section 3.5**)
- SRAM ECC Control (see **Section 3.6**)
- Die Temperature Measurement (see **Section 3.7**)
- Watchdog Timer (see **Section 3.8**)
- Emergency Stop Control (see **Section 3.9**)
- Interrupt Generation (see **Section 3.10**)
- NMI Trap Generation (see **Section 3.11**)
- SCU registers and Address map (see **Section 3.12**)
- SCU register overview table (see **Table 3-22**)

3.1 Clock System Overview

This section describes the TC1798 clock system. Topics covered include clock generation and the operation of clock circuitry.

The TC1798 clock system provides the following functions:

- Acquires and buffers incoming clock signals to create a master clock frequency
- Distributes in-phase synchronized clock signals throughout the TC1798's entire clock tree
- Divides the master clock frequency into lower frequencies required by the different modules for operation
- Reduces electromagnetic interference (EMI) by switching off unused modules

Figure 3-1 shows the structure of the TC1798 clock system. The master clock f_{PLL} is generated by the oscillator circuit and the PLL (phase-locked loop) unit (see **Section 3-2**).

The functionality of the control blocks shown in **Figure 3-1** varies depending on the functional unit being controlled. Some functional units such as the watchdog timer, are directly driven by the system clock. The implemented clock control register options are described for each module in the module chapter itself.

All clock control registers CLC and the fractional divider registers FDR are Endinit-protected.

Features of the TC1798 Clock System

- PLL operation for multiplying clock source by different factors
- Direct drive capability for direct clocking
- Comfortable state machine for secure switching between Freerunning Mode / Normal Mode and Prescaler Mode

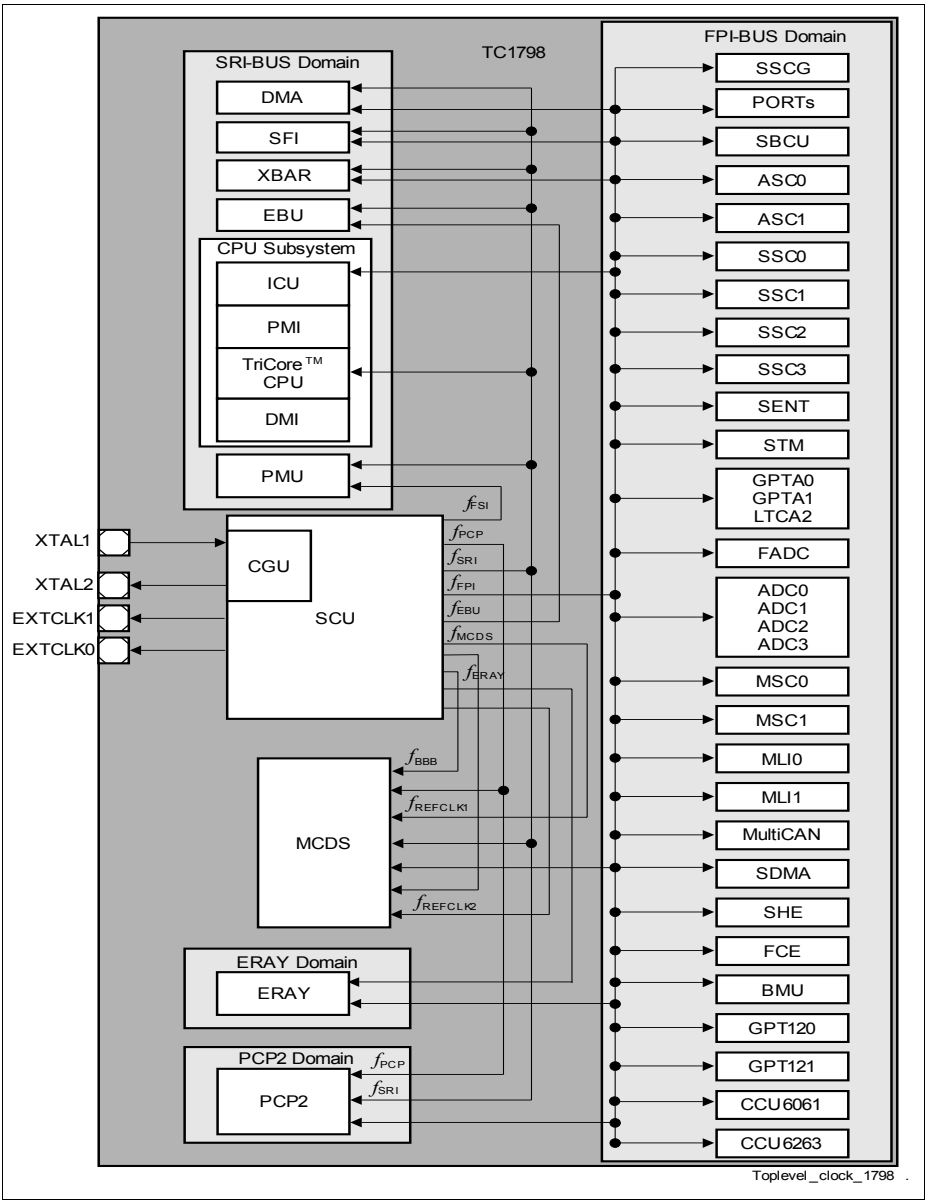


Figure 3-1 TC1798 Clocking System

3.1.1 Clock Generation Unit

The Clock Generation Unit (CGU) allows a very flexible clock generation for the TC1798. During user program execution the frequency can be programmed for an optimal ratio between performance and power consumption.

3.1.1.1 Overview

The CGU in the TC1798 consists of one oscillator circuit (OSC), two Phase-Locked Loop modules (PLL and PLL_ERAY) and a Clock Control Unit (CCU). The CGU can convert a low-frequency external clock signal to a high-speed internal clock.

The CGU provides clock signals for the different parts of the device that can be configured depending on the application needs within certain limits.

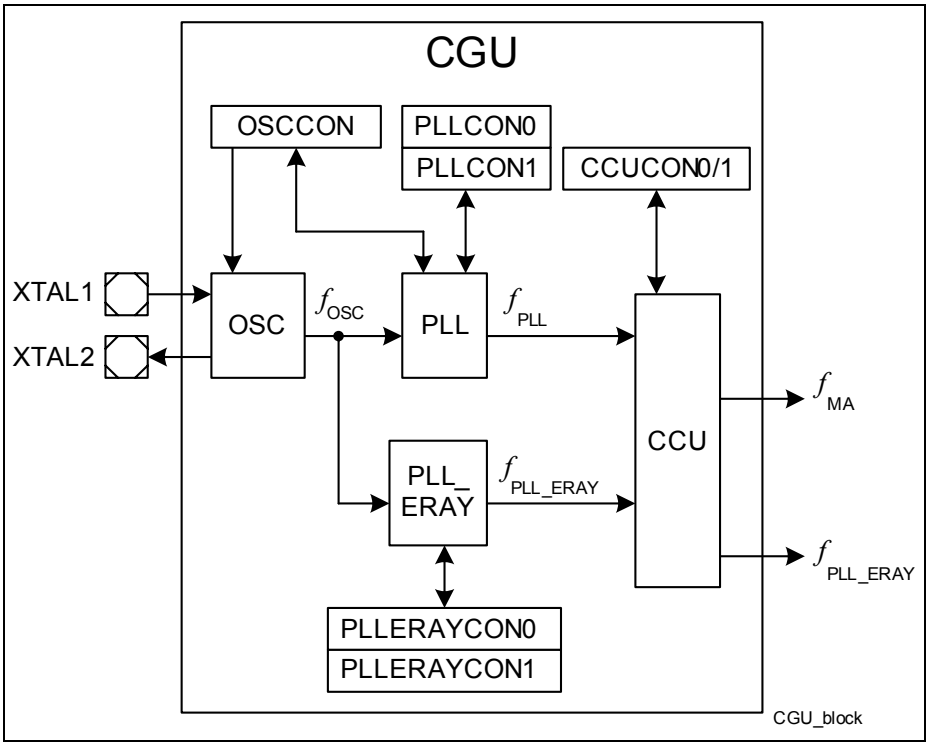


Figure 3-2 Clock Generation Unit Block Diagram

The following sections describe the different parts of the CGU.

3.1.1.2 Oscillator Circuit (OSC)

The oscillator circuit, a Pierce oscillator, is designed to work with both an external crystal / resonator or an external stable clock source, consists of an inverting amplifier with XTAL1 as input, and XTAL2 as output with an integrated feedback resistor.

External Input Clock Mode

When supplying the clock signal directly, not using an external crystal / ceramic resonator and bypassing the oscillator, the input frequency needs to be equal or greater than PLL VCO input frequency (the value is listed in the Data Sheet).

When using an external clock signal it must be connected to XTAL1. XTAL2 is left open (unconnected).

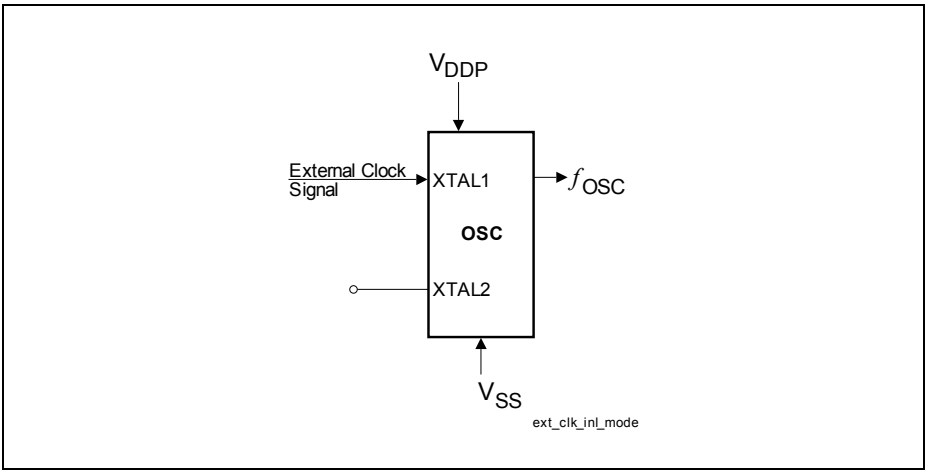


Figure 3-3 TC1798 Direct Clock Input

External Crystal / Ceramic Resonator Mode

Figure 3-4 shows the recommended external circuitries for both operating modes, External Crystal / Ceramic Resonator Mode with and without external components.

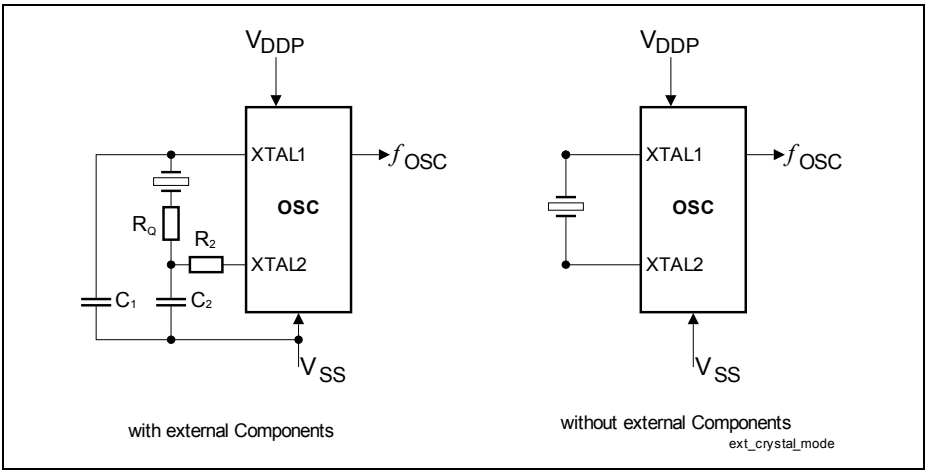


Figure 3-4 External Circuitry for Crystal / Ceramic Resonator operation

When using an external crystal / ceramic resonator, its frequency can be within the allowed range (the values are listed in the Data Sheet). An external oscillator load circuitry must be used, connected to both pins, XTAL1 and XTAL2. Additionally are necessary, two load capacitances C_1 and C_2, and depending on the crystal / ceramic resonator type, a series resistor R_2 to limit the current. A test resistor R_Q may be temporarily inserted to measure the oscillation allowance (negative resistance) of the oscillator circuitry. R_Q values are typically specified by the crystal / ceramic resonator vendor. The C_1 and C_2 values shown in the Data Sheet can be used as starting points for the negative resistance evaluation and for non-productive systems. The exact values and related operating range are dependent on the crystal / ceramic resonator frequency and have to be determined and optimized together with the crystal / ceramic resonator vendor using the negative resistance method. Oscillation measurement with the final target system is strongly recommended to verify the input amplitude at XTAL1 and to determine the actual oscillation allowance (margin negative resistance) for the oscillator-crystal / ceramic resonator system.

The oscillator can also be used in combination with a ceramic resonator. The final circuitry must be also verified by the resonator vendor.

Oscillator Run Detection

See .

3.1.1.3 Phase-Locked Loop (PLL) Module

The PLL can convert a low-frequency external clock signal to a high-speed internal clock for maximum performance. The PLL also has fail-safe logic that detects degenerate external clock behavior such as abnormal frequency deviations or a total loss of the external clock. It can execute emergency actions if it loses its lock on the external clock.

This module is a phase locked loop for integer frequency synthesis. It allows the use of input and output frequencies of a wide range by varying the different divider factors.

Features

- VCO lock detection
- 4-bit input divider **P:** (divide by PDIV+1)
- 7-bit feedback divider **N**: (multiply by NDIV+1)
- 7-bit output divider **K1 or K2:** (divide by either by K1DIV+1 or K2DIV+1)
- Oscillator Watchdog
  - Detecting too low input frequencies
  - Detecting too high input frequencies
  - Spike detection for the OSC input frequency
- Different operating modes
  - Prescaler Mode
  - Freerunning Mode
  - Normal Mode
- VCO Power Down
- Glitchless switching between both K-Dividers
- Glitchless switching between Normal Mode and Prescaler Mode
- Frequency Modulation
- Jitter reduction for modulation jitter

PLL Functional Description

The PLL consists of a Voltage Controlled Oscillator (VCO) with a feedback path. A divider in the feedback path (N-Divider) divides the VCO frequency down. The resulting frequency is then compared with the externally provided and divided frequency (P-Divider). The phase detection logic determines the difference between the two clocks and accordingly controls the frequency of the VCO (f_{VCO}). A PLL lock detection unit monitors and signals this condition. The phase detection logic continues to monitor the two clocks and adjusts the VCO clock if required. The PLL output clock f_{PLL} is derived from the VCO clock by the K2-Divider or from the oscillator clock and the K1-Divider.

The following figure shows the PLL block structure.

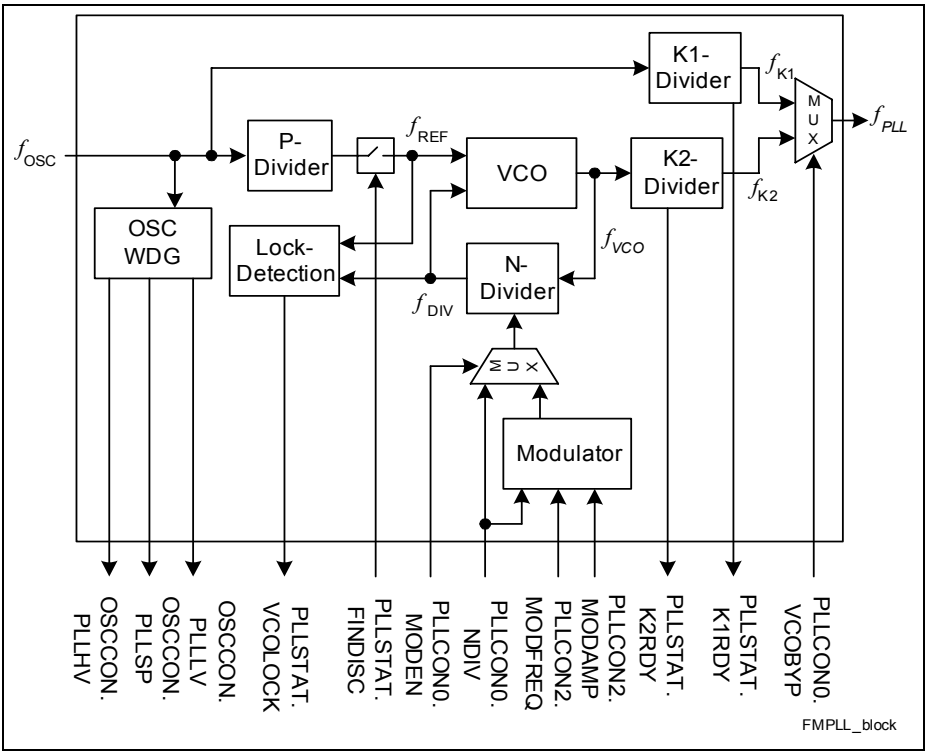


Figure 3-5 PLL Block Diagram

Clock Source Control

The PLL clock f_{PLL} is generated from f_{OSC} in one of three software selectable modes:

- Normal Mode
- Prescaler Mode
- Freerunning Mode

Normal Mode

In Normal Mode the input frequency f_{OSC} is divided down by a factor P, multiplied by a factor N and then divided down by a factor K2.

The output frequency is given by

(3.1)

$$f_{PLL} = \frac{N}{P \cdot K2} \cdot f_{OSC}$$

Prescaler Mode

In Prescaler Mode the reference frequency f_{OSC} is only divided down by a factor K1.

The output frequency is given by

$$f_{PLL} = \frac{f_{OSC}}{K1} \quad (3.2)$$

Freerunning Mode

In Freerunning Mode the base frequency output of the Voltage Controlled Oscillator (VCO) $f_{VCObase}$ is only divided down by a factor K2.

The output frequency is given by

$$f_{PLL} = \frac{f_{VCObase}}{K2} \quad (3.3)$$

Oscillator Watchdog (OSC_WDT)

The oscillator watchdog monitors the incoming clock frequency f_{OSC} from OSC. A stable and defined input frequency is a mandatory requirement for operation in both Prescaler Mode and Normal Mode. For operation in Freerunning Mode no f_{OSC} input frequency is required. Therefore this mode is selected automatically after each System Reset. In addition for the Normal Mode it is required that the input frequency f_{OSC} is in a certain frequency range to obtain a stabile master clock from the VCO part.

The expected input frequency is selected via the bit field OSCCON.OSCVAL. The OSC_WDT checks for too low frequencies and for too high frequencies.

The frequency that is monitored is f_{OSCREF} which is derived for f_{OSC}.

$$f_{OSCREF} = \frac{f_{OSC}}{OSCVAL + 1} \quad (3.4)$$

The divider value OSCCON.OSCVAL has to be selected in a way that f_{OSCREF} is 2.5 MHz.

Note: f_{OSCREF} has to be within the range of 2 MHz to 3 MHz and should be as close as possible to 2.5 MHz.

Before configuring the OSC_WDT function all the trap options should be disabled in order to avoid unintended traps. Thereafter the value of OSCCON.OSCVAL can be changed. Then the OSC_WDT should be reset by setting OSCCON.OSCRES. This requests the start of OSC_WDT monitoring with the new configuration. When the

expected positive monitoring results of OSCCON.PLLLV and / or OSCCON.PLLHV are set the input frequency is within the expected range. As setting OSCCON.OSCRES clears all three bits OSCCON.PLLSP, OSCCON.PLLLV, and OSCCON.PLLHV all three trap status flags will be set. Therefore all three flags should be cleared before the trap generation is enabled again. The trap disabling-clearing-enabling sequence should also be used if only bit OSCCON.OSCRES is set without any modification of OSCCON.OSCVAL.

Configuration and Operation of the Freerunning Mode

In Freerunning Mode, the PLL is running at its VCO base frequency and f_{PLL} is derived from f_{VCO} only by the K2-Divider.

The Freerunning Mode is entered after each System Reset.

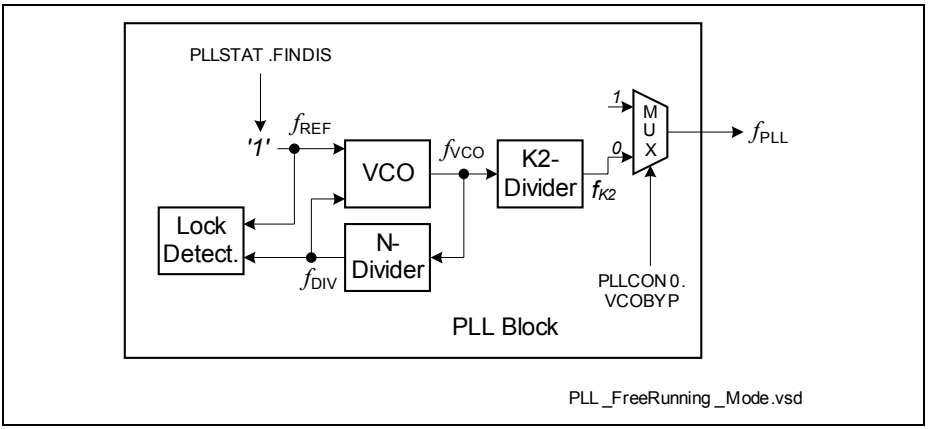


Figure 3-6 PLL Free-Running Mode Diagram

The output frequency is given by

$$f_{PLL} = \frac{f_{VCObase}}{K2} \quad (3.5)$$

The Freerunning Mode is selected by the following settings

- PLLCON0.VCOBYP = 0
- PLLCON0.SETFINDIS = 1

The Freerunning Mode is entered when

- PLLSTAT.FINDIS = 1
- AND
- PLLSTAT.VCOBYST = 0

Operation on the Freerunning Mode does not require an input clock frequency of f_{OSC}. The Freerunning Mode is automatically entered on a PLL VCO Loss-of-Lock event if bit PLLCON0.OSCDISCDIS is cleared. This mechanism allows a fail-safe operation of the PLL as in emergency cases still a clock is available.

The frequency of the Freerunning Mode $f_{VCObase}$ is listed in the Data Sheet.

Note: Changing the system operation frequency by changing the value of the K2-Divider has a direct coupling to the power consumption of the device. Therefore this has to be done carefully.

Depending on the selected divider value of the K2-Divider the duty cycle of the clock is selected. This can have an impact for the operation with an external communication interface. The duty cycles values for the different K2-divider values are defined in the Data Sheet.

Configuration and Operation of the Prescaler Mode

In Prescaler Mode, the PLL is running at the external frequency f_{OSC} and f_{PLL} is derived from f_{OSC} only by the K1-Divider.

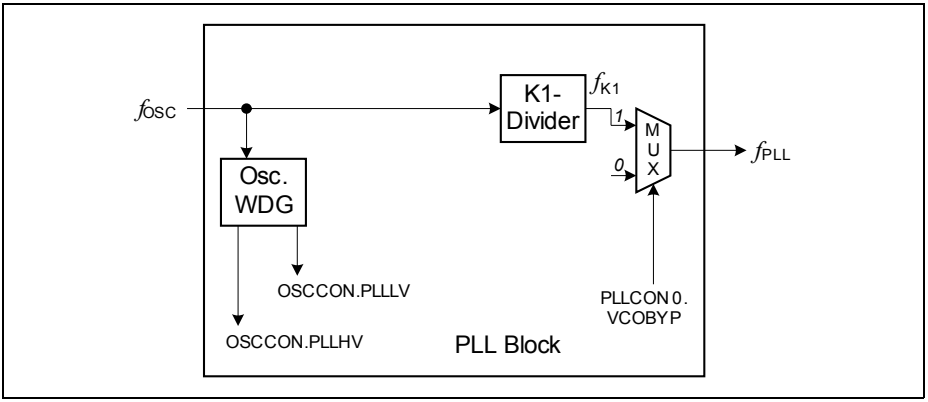


Figure 3-7 PLL Prescaler Mode Diagram

The output frequency is given by:

$$f_{PLL} = \frac{f_{OSC}}{K1} \quad (3.6)$$

The Prescaler Mode is selected by the following settings

- PLLCON0.VCOBYP = 1

The Prescaler Mode is entered when the following requirements are all together valid:

- PLLSTAT.VCOBYST = 1
- OSCCON.PLLLV = 1

Operation on the Prescaler Mode does require an input clock frequency of f_{OSC}. Therefore it is recommended to check and monitor if an input frequency f_{OSC} is available at all by checking OSCCON.PLLLV. For a better monitoring also the upper frequency can be monitored via OSCCON.PLLHV.

For the Prescaler Mode there are no requirements regarding the frequency of f_{OSC}.

The system operation frequency is controlled in the Prescaler Mode by the value of the K1-Divider. When the value of PLLCON1.K1DIV was changed the next update of this value should not be done before bit PLLSTAT.K1RDY is set.

Note: Changing the system operation frequency by changing the value of the K1-Divider has a direct coupling to the power consumption of the device. Therefore this has to be done carefully.

Depending on the selected divider value of the K1-Divider the duty cycle of the clock is selected. This can have an impact for the operation with an external communication interface. The duty cycles values for the different K1-divider values are defined in the Data Sheet.

The Prescaler Mode is requested from the Freerunning or Normal Mode by setting bit PLLCON.VCOBYP. The Prescaler Mode is entered when the status bit PLLSTAT.VCOBYST is set. Before the Prescaler Mode is requested the K1-Divider should be configured with a value generating a PLL output frequency f_{PLL} that matches the one generated by the Freerunning or Normal Mode as much as possible. In this way the frequency change resulting out of the mode change is reduced to a minimum.

The Prescaler Mode is requested to be left by clearing bit PLLCON.VCOBYP. The Prescaler Mode is left when the status bit PLLSTAT.VCOBYST is cleared.

Configuration and Operation of the Normal Mode

In Normal Mode, the PLL is running at the external frequency f_{OSC} and f_{PLL} is divided down by a factor P, multiplied by a factor N and then divided down by a factor K2.

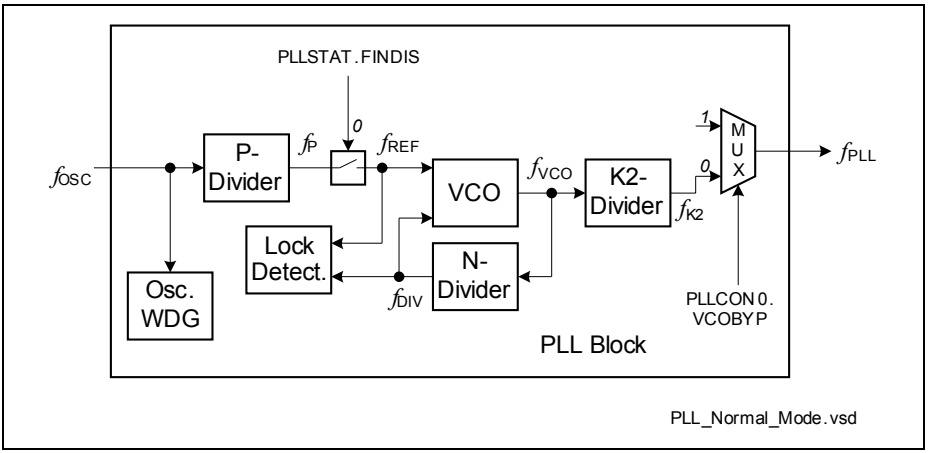


Figure 3-8 PLL Normal Mode Diagram

The output frequency is given by:

(3.7)

$$f_{PLL} = \frac{N}{P \cdot K2} \cdot f_{OSC}$$

The Normal Mode is selected by the following settings

- PLLCON0.VCOBYP = 0
- PLLCON0.CLRFINDIS = 1

The Normal Mode is entered when the following requirements are all together valid:

- PLLSTAT.FINDIS = 0
- PLLSTAT.VCOBYST = 0
- PLLSTAT.VCOLOCK = 1
- OSCCON.PLLLV = 1
- OSCCON.PLLHV = 1

For the Nomal Mode operation it is recommanded to clear bit PLLCON0.OSCDISCDIS.

Operation on the Normal Mode does require an input clock frequency of f_{OSC}. Therefore it is recommended to check and monitor if an input frequency f_{OSC} is available at all by checking OSCCON.PLLLV. For a better monitoring also the upper frequency can be monitored via OSCCON.PLLHV.

The system operation frequency is controlled in the Normal Mode by the values of the three dividers: P, N, and K2. A modification of the two dividers P and N has a direct influence to the VCO frequency and lead to a loss of the VCO Lock status. A modification

of the K2-divider has no impact on the VCO Lock status but still changes the PLL output frequency.

Note: Changing the system operation frequency by changing the value of the K2-Divider has a direct coupling to the power consumption of the device. Therefore this has to be done carefully.

When the frequency of the Normal Mode should be modified or entered the following sequence should be followed:

First the Prescaler Mode should be configured and entered. For more details see the Prescaler Mode.

The NMI trap generation for the VCO Lock should be disabled.

While the Prescaler Mode is used the Normal Mode can be configured and checked for a positive VCO Lock status. The first target frequency of the Normal Mode should be selected in a way that it matches or is only slightly higher as the one used in the Prescaler Mode. This avoids big changes in the system operation frequency and therefore power consumption when switching later from Prescaler Mode to Normal Mode. The P and N divider should be selected in the following way:

- Selecting P and N in a way that f_{VCO} is in the lower area of its allowed values leads to a slightly reduced power consumption but to a slightly increased jitter
- Selecting P and N in a way that f_{VCO} is in the upper area of its allowed values leads to a slightly increased power consumption but to a slightly reduced jitter

After the P, N, and K2 dividers are updated for the first configuration the indication of the VCO Lock status should be await (PLLSTAT.VCOLOCK = 1).

Note: It is recommended to reset the VCO Lock detection (PLLCON0.RESLD = 1) after the new values of the dividers are configured to get a defined VCO lock check time.

When this happens the switch from Prescaler Mode to Normal Mode can be done. Normal Mode is requested by clearing PLLCON.VCOBYP. The Normal Mode is entered when the status bit PLLSTAT.VCOBYST is cleared.

Now the Normal Mode is entered. The NMI status flag for the VCO Lock trap should be cleared and then enabled again. The intended PLL output target frequency can now be configured by changing only the K2-Divider.

Depending on the selected divider value of the K2-Divider the duty cycle of the clock is selected. This can have an impact for the operation with an external communication interface. The duty cycles values for the different K2-divider values are defined in the Data Sheet. This can result in multiple changes of the K2-Divider to avoid to big frequency changes. Between the update of two K2-Divider values 6 cycles of f_{PLL} should be waited.

PLL VCO Lock Detection

The PLL has a lock detection that supervises the VCO part of the PLL in order to differentiate between stable and instable VCO circuit behavior. The lock detector marks the VCO circuit and therefore the output f_{VCO} of the VCO as instable if the two inputs f_{REF} and f_{DIV} differ too much. Changes in one or both input frequencies below a level are not marked by a loss of lock because the VCO can handle such small changes without any problem for the system.

PLL VCO Loss-of-Lock Event

The PLL may become unlocked, caused by a break of the crystal or the external clock line. In such a case, an NMI trap is generated if the according NMI trap is enabled. Additionally, the OSC clock input f_{OSC} is disconnected from the PLL VCO to avoid unstable operation due to noise or sporadic clock pulses coming from the oscillator circuit. Without a clock input f_{OSC}, the PLL gradually slows down to its VCO base frequency and remains there. This automatic feature can be disabled by setting bit PLLCON0.OSCDISCDIS. If this bit is set the OSC clock remains connected to the VCO.

VCO Power Down Mode

The PLL offers a VCO Power Down Mode. This mode can be entered to save power within the PLL. The VCO Power Down Mode is entered by setting bit PLLCON0.VCOPWD. While the PLL is in VCO Power Down Mode only the Prescaler Mode is operable. Please note that selecting the VCO Power Down Mode does not automatically switch to the Prescaler Mode. So before the VCO Power Down Mode is entered the Prescaler Mode must be active.

PLL Power Down Mode

The PLL offers a Power Down Mode. This mode can be entered to save power if the PLL is not needed at all. The Power Down Mode is entered by setting bit PLLCON0.PLLPWD. While the PLL is in Power Down Mode no PLL output frequency is generated.

Frequency Modulation

If the PLL operates in Normal Mode the output frequency f_{PLL} can additionally be modified by a low-frequency modulation. A triangle waveform is generated and fed to a noiseshaper. The noiseshaper generate a stream of values for the N-divider that are used there to modify (modulate) the N-divider value. Due to the low pass function of the PLL (VCO part) non integer frequencies can be generated by switching fast enough between different values of the N-divider.

The modulation is enabled via bit PLLCON0.MODEN. The modulation itself is a triangle-shaped function with an amplitude that can be configured via bit field PLLCON2.MODAMP. Setting bit field MODAMP to zero disables the modulation synchronously. The modulation frequency itself is configurable by bit field PLLCON2.MODFREQ.

3.1.1.4 ERAY Phase-Locked Loop (PLL_ERAY) Module

The PLL_ERAY can convert a low-frequency external clock signal to a high-speed internal clock for maximum performance. The PLL_ERAY also has fail-safe logic that detects degenerate external clock behavior such as abnormal frequency deviations or a total loss of the external clock. It can execute emergency actions if it loses its lock on the external clock.

This module is a phase locked loop for integer frequency synthesis. It allows the use of input and output frequencies of a wide range by varying the different divider factors.

Features

- VCO lock detection
- 6-bit feedback divider **N**: (multiply by NDIV+1)
- 5-bit output divider **K1 or K2:** (divide by either by K1DIV+1 or K2DIV+1)
- Different operating modes
  - Prescaler Mode
  - Freerunning Mode
  - Normal Mode
- VCO Power Down (Sleep Mode)
- Glitchless switching between both K-Dividers
- Glitchless switching between Normal Mode and Prescaler Mode

PLL_ERAY Functional Description

The PLL_ERAY consists of a Voltage Controlled Oscillator (VCO) with a feedback path. A divider in the feedback path (N-Divider) divides the VCO frequency down. The resulting frequency is then compared with the externally provided frequency. The phase detection logic determines the difference between the two clocks and accordingly controls the frequency of the VCO (f_{VCO}). A PLL_ERAY lock detection unit monitors and signals this condition. The phase detection logic continues to monitor the two clocks and adjusts the VCO clock if required. The PLL_ERAY output clock f_{PLL_ERAY} is derived from the VCO clock by the K2-Divider or from the oscillator clock and the K1-Divider.

The following figure shows the PLL_ERAY block structure.

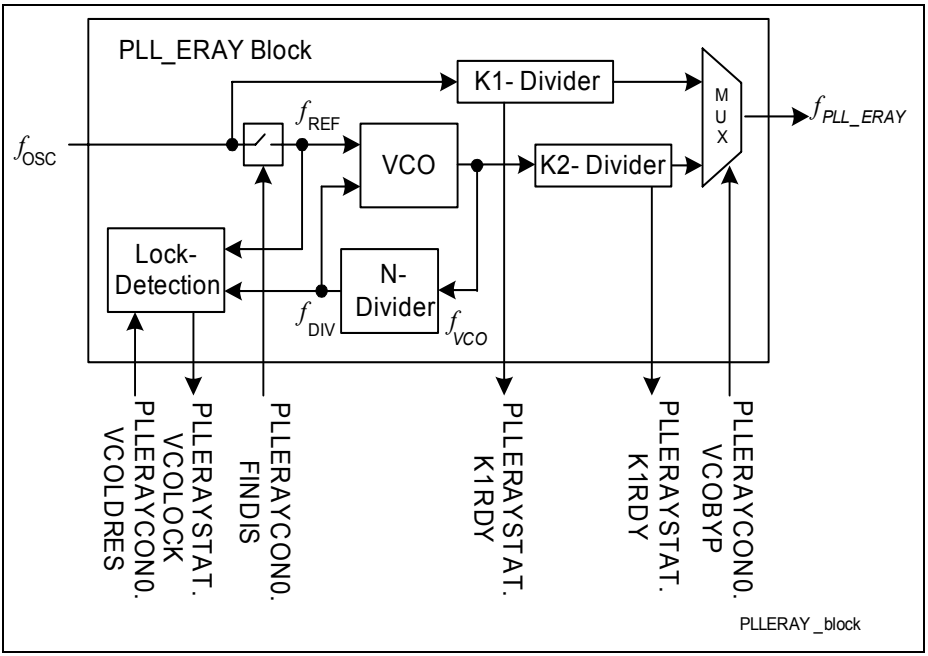


Figure 3-9 PLL_ERAY Block Diagram

Clock Source Control

The PLL_ERAY clock f_{PLL_ERAY} is generated from f_{OSC} in one of three software selectable modes:

- Bypassing N and both K dividers; this defines the Bypass Mode
- Normal Mode
- Prescaler Mode
- Freerunning Mode

Normal Mode

In Normal Mode the input frequency f_{OSC} is multiplied by a factor N and then divided down by a factor K2.

The output frequency is given by

(3.8)

$$f_{PLL} = \frac{N}{K2} \cdot f_{OSC}$$

Prescaler Mode

In Prescaler Mode the reference frequency f_{OSC} is only divided down by a factor K1.

The output frequency is given by

$$f_{PLL} = \frac{f_{OSC}}{K1} \quad (3.9)$$

Freerunning Mode

In Freerunning Mode the base frequency output of the Voltage Controlled Oscillator (VCO) $f_{VCObase}$ is only divided down by a factor K2.

The output frequency is given by

$$f_{PLL} = \frac{f_{VCObase}}{K2} \quad (3.10)$$

Configuration and Operation of the Freerunning Mode

In Freerunning Mode, the PLL_ERAY is running at its VCO base frequency and f_{PLL_ERAY} is derived from f_{VCO} only by the K2-Divider.

The Freerunning Mode is entered after each System Reset.

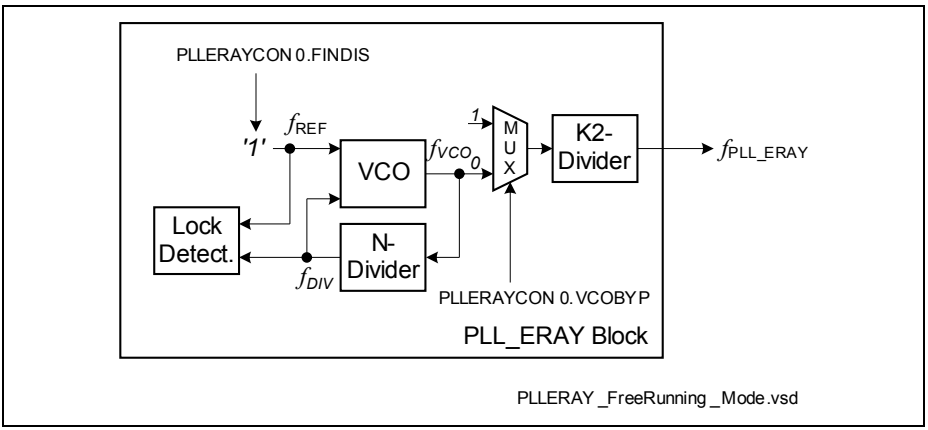


Figure 3-10 PLL_ERAY Free-Running Mode Diagram

The output frequency is given by

$$f_{PLL} = \frac{f_{VCObase}}{K2} \quad (3.11)$$

The Freerunning Mode is selected by the following settings

- PLLERAYCON0.VCOBYP = 0
- PLLERAYCON0.SETFINDIS = 1

The Freerunning Mode is entered when

- PLLERAYSTAT.FINDIS = 1
- AND
- PLLERAYSTAT.VCOBYST = 0

Operation on the Freerunning Mode does not require an input clock frequency of f_{OSC}. The Freerunning Mode is automatically entered on a PLL_ERAY VCO Loss-of-Lock event if bit PLLERAYCON0.OSCDISCDIS is cleared. This mechanism allows a fail-safe operation of the PLL_ERAY as in emergency cases still a clock is available.

The frequency of the Freerunning Mode $f_{VCObase}$ is listed in the Data Sheet.

Depending on the selected divider value of the K2-Divider the duty cycle of the clock is selected. This can have an impact for the operation with an external communication interface. The duty cycles values for the different K2-divider values are defined in the Data Sheet.

Configuration and Operation of the Prescaler Mode

In Prescaler Mode, the PLL_ERAY is running at the external frequency f_{OSC} and f_{PLL_ERAY} is derived from f_{OSC} only by the K1-Divider.

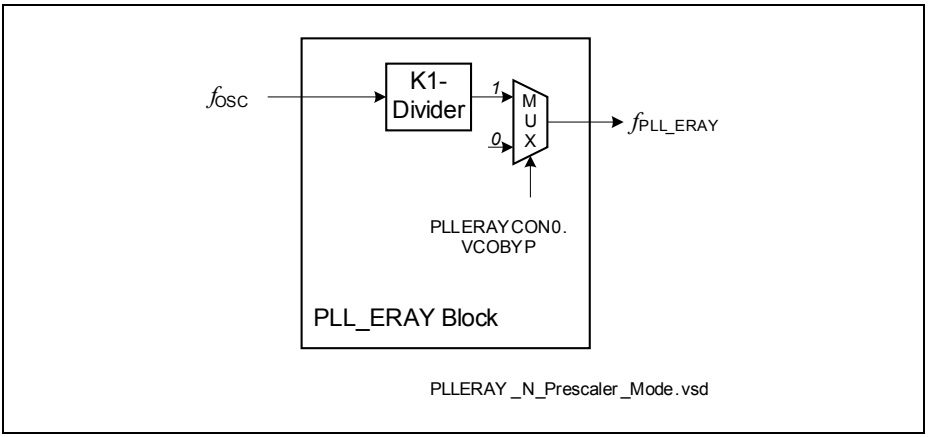


Figure 3-11 PLL_ERAY Prescaler Mode Diagram

The output frequency is given by:

(3.12)

$$f_{PLL} = \frac{f_{OSC}}{K1}$$

The Prescaler Mode is selected by the following settings

- PLLERAYCON0.VCOBYP = 1

The Prescaler Mode is entered when the following requirements are all together valid:

- PLLERAYSTAT.VCOBYST = 1
- OSCCON.PLLLV = 1

Operation on the Prescaler Mode does require an input clock frequency of f_{OSC}. Therefore it is recommended to check and monitor if an input frequency f_{OSC} is available at all by checking OSCCON.PLLLV. For a better monitoring also the upper frequency can be monitored via OSCCON.PLLHV.

For the Prescaler Mode there are no requirements regarding the frequency of f_{OSC}.

The system operation frequency is controlled in the Prescaler Mode by the value of the K1-Divider. When the value of PLLERAYCON1.K1DIV was changed the next update of this value should not be done before bit PLLERAYSTAT.K1RDY is set.

Depending on the selected divider value of the K1-Divider the duty cycle of the clock is selected. This can have an impact for the operation with an external communication interface. The duty cycles values for the different K1-divider values are defined in the Data Sheet.

The Prescaler Mode is requested from the Freerunning or Normal Mode by setting bit PLLERAYCON.VCOBYP. The Prescaler Mode is entered when the status bit PLLERAYSTAT.VCOBYST is set. Before the Prescaler Mode is requested the K1-Divider should be configured with a value generating a PLL_ERAY output frequency f_{PLL_ERAY} that matches the one generated by the Freerunning or Normal Mode as much as possible. In this way the frequency change resulting out of the mode change is reduced to a minimum.

The Prescaler Mode is requested to be left by clearing bit PLLERAYCON.VCOBYP. The Prescaler Mode is left when the status bit PLLERAYSTAT.VCOBYST is cleared.

Configuration and Operation of the Normal Mode

In Normal Mode, the PLL_ERAY is running at the external frequency f_{OSC} and f_{PLL_ERAY} is multiplied by a factor N and then divided down by a factor K2.

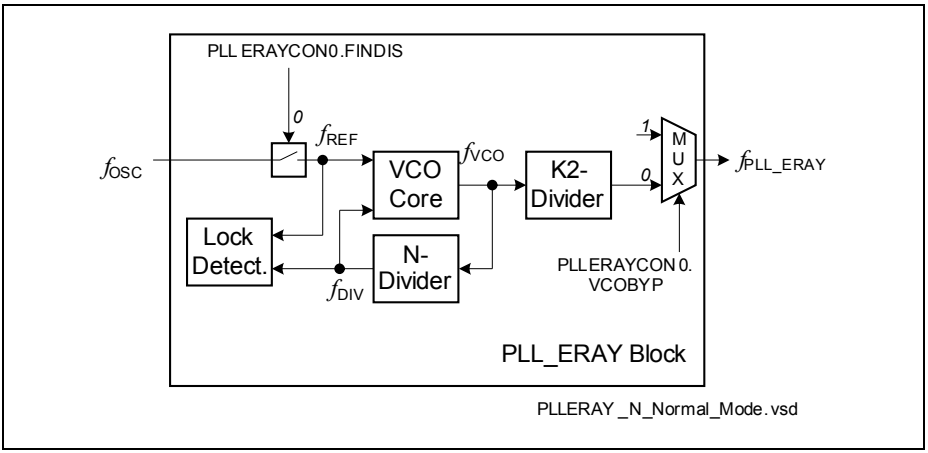


Figure 3-12 PLL_ERAY Normal Mode Diagram

The output frequency is given by:

(3.13)

$$f_{PLL} = \frac{N}{K2} \cdot f_{OSC}$$

The Normal Mode is selected by the following settings

- PLLERAYCON0.VCOBYP = 0
- PLLERAYCON0.CLRFINDIS = 1

The Normal Mode is entered when the following two requirements are all together valid:

- PLLERAYSTAT.FINDIS = 0

- PLLERAYSTAT.VCOBYST = 0
- PLLERAYSTAT.VCOLOCK = 1
- OSCCON.PLLLV = 1
- OSCCON.PLLHV = 1

Operation on the Normal Mode does require an input clock frequency of f_{OSC}. Therefore it is recommended to check and monitor if an input frequency f_{OSC} is available at all by checking OSCCON.PLLLV. For a better monitoring also the upper frequency can be monitored via OSCCON.PLLHV.

The system operation frequency is controlled in the Normal Mode by the values of the two dividers: N and K2. A modification of the divider N has a direct influence to the VCO frequency and lead to a loss of the VCO Lock status. A modification of the K2-divider has no impact on the VCO Lock status but still changes the PLL_ERAY output frequency.

When the frequency of the Normal Mode should be modified or entered the following sequence should be followed:

First the Prescaler Mode should be configured and entered. For more details see the Prescaler Mode.

The NMI trap generation for the VCO Lock should be disabled.

While the Prescaler Mode is used the Normal Mode can be configured and checked for a positive VCO Lock status. The first target frequency of the Normal Mode should be selected in a way that it matches or is only slightly higher as the one used in the Prescaler Mode. This avoids big changes in the system operation frequency and therefore power consumption when switching later from Prescaler Mode to Normal Mode. The N divider should be selected in the following way:

- Selecting N in a way that f_{VCO} is in the lower area of its allowed values leads to a slightly reduced power consumption but to a slightly increased jitter
- Selecting N in a way that f_{VCO} is in the upper area of its allowed values leads to a slightly increased power consumption but to a slightly reduced jitter

After the N and K2 dividers are updated for the first configuration the indication of the VCO Lock status should be await (PLLERAYSTAT.VCOLOCK = 1).

*Note: It is recommended to reset the VCO Lock detection (PLL*ERAY*CON0.RESLD = 1) after the new values of the dividers are configured to get a defined VCO lock check time.*

When this happens the switch from Prescaler Mode to Normal Mode can be done. Normal Mode is requested by clearing PLLERAYCON.VCOBYP. The Normal Mode is entered when the status bit PLLERAYSTAT.VCOBYST is cleared.

Now the Normal Mode is entered. The NMI status flag for the VCO Lock trap should be cleared and then enabled again. The intended PLL_ERAY output target frequency can not be configured by changing only the K2-Divider.

Depending on the selected divider value of the K2-Divider the duty cycle of the clock is selected. This can have an impact for the operation with an external communication interface. The duty cycles values for the different K2-divider values are defined in the Data Sheet. This can result in multiple changes of the K2-Divider to avoid to big frequency changes. Between the update of two K2-Divider values 6 cycles of f_{PLL_ERAY} should be waited.

PLL_ERAY VCO Lock Detection

The PLL_ERAY has a lock detection that supervises the VCO part of the PLL_ERAY in order to differentiate between stable and instable VCO circuit behavior. The lock detector marks the VCO circuit and therefore the output f_{VCO} of the VCO as instable if the two inputs f_{REF} and f_{DIV} differ too much. Changes in one or both input frequencies below a level are not marked by a loss of lock because the VCO can handle such small changes without any problem for the system.

PLL_ERAY VCO Loss-of-Lock Event

The PLL_ERAY may become unlocked, caused by a break of the crystal or the external clock line. In such a case, an NMI trap is generated if the according NMI trap is enabled. Additionally, the OSC clock input f_{OSC} is disconnected from the PLL_ERAY VCO to avoid unstable operation due to noise or sporadic clock pulses coming from the oscillator circuit. Without a clock input f_{OSC}, the PLL_ERAY gradually slows down to its VCO base frequency and remains there. This automatic feature can be disabled by setting bit PLLERAYCON0.OSCDISCDIS. If this bit is cleared the OSC clock remains connected to the VCO.

VCO Power Down Mode

The PLL_ERAY offers a VCO Power Down Mode. This mode can be entered to save power within the PLL_ERAY. The VCO Power Down Mode is entered by setting bit PLLCON0.VCOPWD. While the PLL_ERAY is in VCO Power Down Mode only the Prescaler Mode is operable. Please note that selecting the VCO Power Down Mode does not automatically switch to the Prescaler Mode. So before the VCO Power Down Mode is enter the Prescaler Mode must be active.

PLL_ERAY Power Down Mode

The PLL_ERAY offers a Power Down Mode. This mode can be entered to save power if the PLL_ERAY is not needed at all. The Power Down Mode is entered by setting bit PLLCON0.PLLPWD. While the PLL_ERAY is in Power Down Mode no PLL_ERAY output frequency is generated.

3.1.1.5 Clock Control Unit

The Clock Control Unit (CCU) receives the clock that is created by the two PLLs f_{PLL} and f_{PLL_ERAY}.

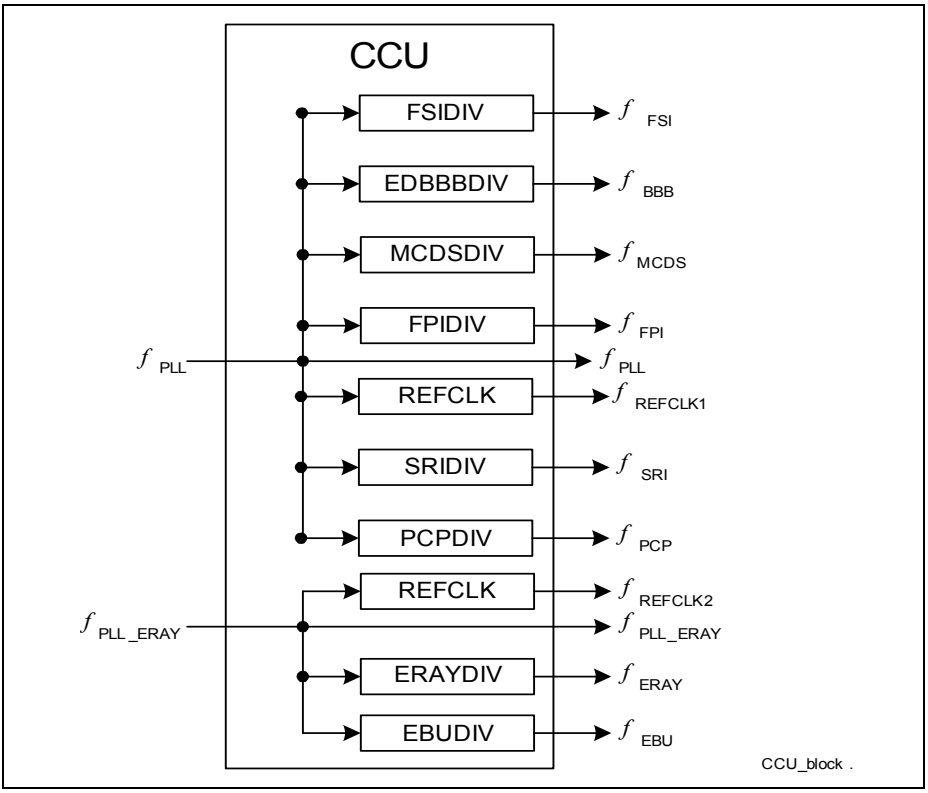


Figure 3-13 Clock Control Unit

The clocking system of the TC1798 consists of the Clock Control Unit (CCU) and the Clock Generation Unit.

There is also a fix reference clock REFCLK1 for the MCDS block which divides the master clock f_{PLL} by 24. This allows the MCDS to generate time stamps independent of the selected SRI-Bus and FPI-Bus clock speeds.

Clock Divider Limitations

The following table defines the allowed clock ratios for the application relevant clocks. The values given in the table define values for the bit fields of register CCUCON0.

Table 3-1 Allowed Clock Ratios

Register Name	Option 1	Option 2	Option 3	Option 4
SRIDIV	0	0	1	0
FSIDIV	0	1	3	1
PCPDIV	0	0	2	1
FPIDIV	0	1	5	3

Note: CCUCON1.EDBBBDIV and CCUCON1.MCDSDIV should always be set to SRI / CPU speed divided by two.

For changing the clock frequencies it is recommanded to follow the sequence described in **Figure 3-14**.

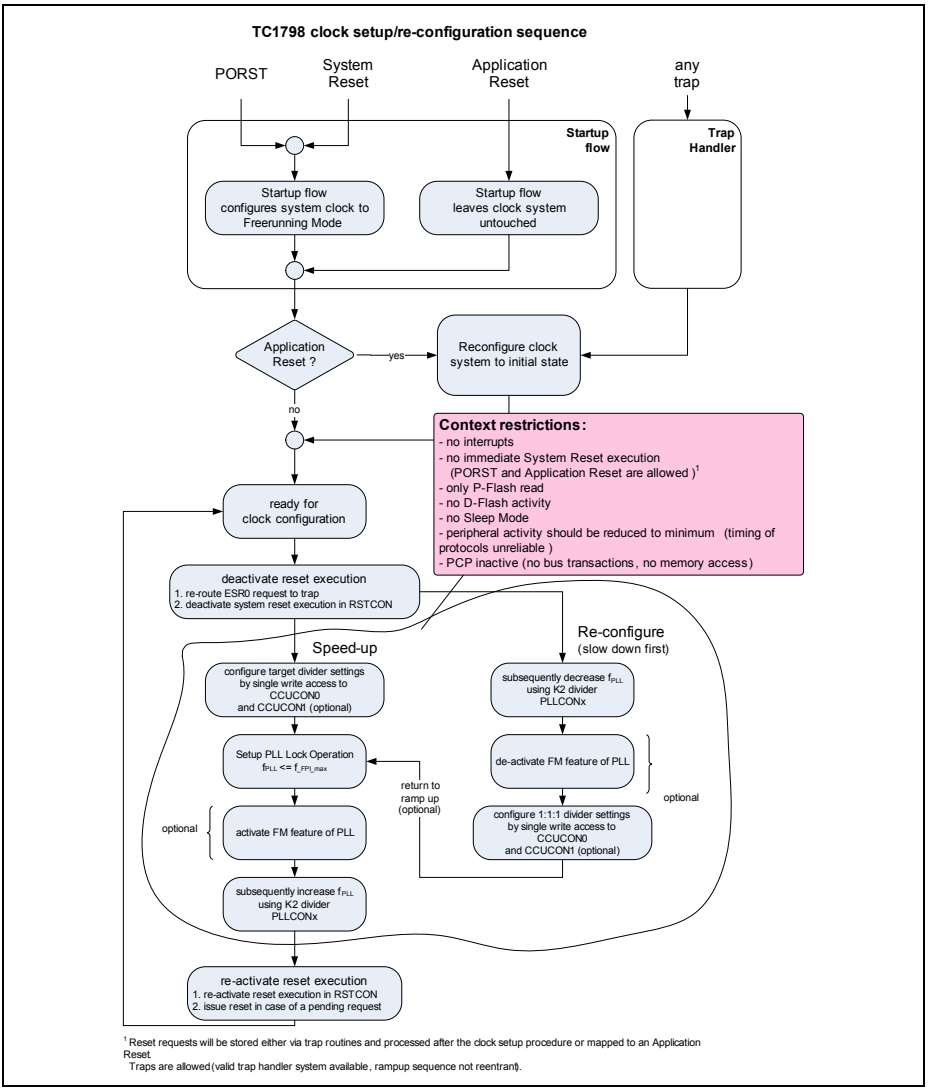


Figure 3-14 Clock changing Sequence

3.1.1.6 External Clock Output

Two external clock outputs are provided via pins EXTCLK0 and EXTCLK1. These external clocks can be enabled/disabled via bits EXTCON.EN0 for EXTCLK0 and

EXTCON.EN1 for EXTCLK1. Each of the clocks that defines a clock domain can individually be selected to be seen at pins EXTCLK0 or EXTCLK1, this is configured via bit field EXTCON.SEL0/1. Changing the content of bit field EXTCON.SEL0/1 can lead to spikes at pins EXTCLK0/1.

Note: Only the burst flash clock of the EBU is not included as the EBU provides a separate pin here.

Additionally a connection to the GPTA module is implemented to support the start-up control of an external crystal for the device clock generation. The first time before the master clock is generated based on a external crystal 1000 cycles of the crystal clock f_{OSC} should be waited before the clock control system is changed to External Crystal Mode. The 1000 cycles can be counted with the GPTA using f_{OSC} as count input for the counter.

Programmable Frequency Output for EXTCLK0

This section describes the external clock generation using the Fractional Divider.

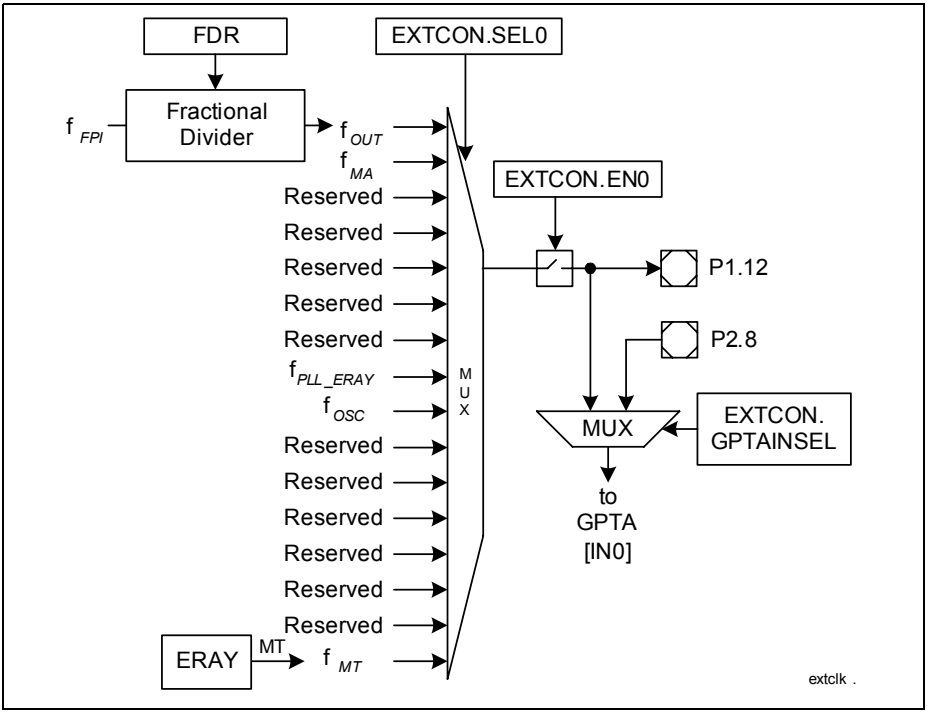


Figure 3-15 EXTCLK0 Generation

Overview

The fractional divider makes it possible to generate a external clock from the FPI-Bus clock using a programmable divider. The fractional divider divides the input clock f_{FPI} either by the factor 1/n or by a fraction of n/1024 for any value of n from 0 to 1023. This clock is thereafter divider additionally by a factor of two to guarantee a 50% duty cycle and outputs the clock, f_{OUT}. The fractional divider is controlled by the FDR register. **Figure 3-16** shows the fractional divider block diagram.

The adder logic of the fractional divider can be configured for two operating modes:

- Reload counter (addition of +1), generating an output clock pulse on counter overflow
- Adder that adds a STEP value to the RESULT value and generates an output clock pulse on counter overflow

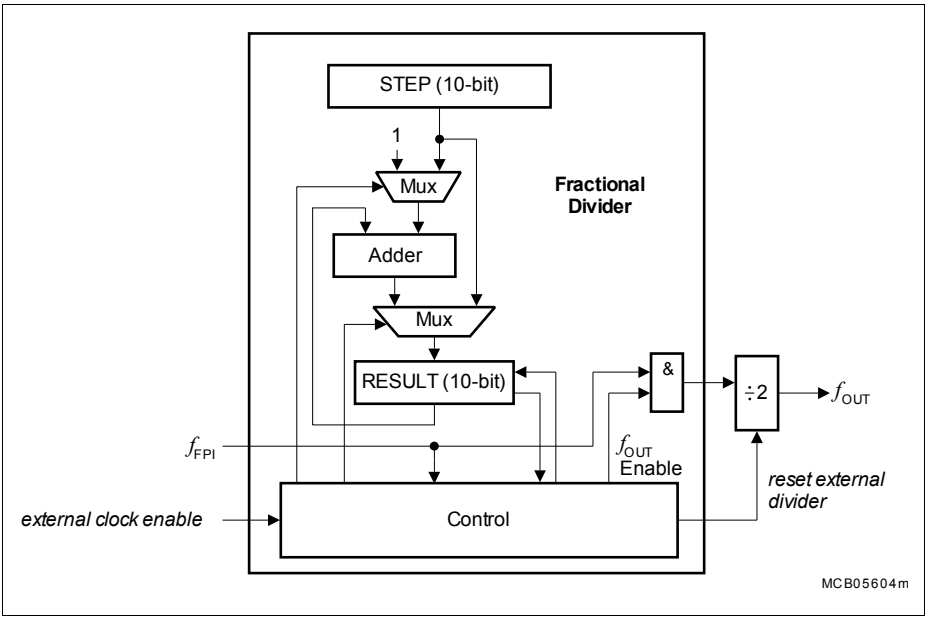


Figure 3-16 Fractional Divider Block Diagram

The adder logic of the fractional divider can be configured for two operating modes:

- **Normal Mode:** Reload counter (RESULT = RESULT + 1), generating an output clock pulse on counter overflow.
- **Fractional Divider Mode:** Adder that adds a STEP value to the RESULT value and generates an output clock pulse on counter overflow.

Fractional Divider Operating Modes

The fractional divider has two operating modes:

- Normal Divider Mode
- Fractional Divider Mode

Normal Divider Mode

In Normal Divider Mode (FDR.DM = 01_B), the fractional divider behaves as a reload counter (addition of +1) that generates an output clock pulse on the transition from $3FF_H$ to 000_H. FDR.RESULT represents the counter value and FDR.STEP determines the reload value.

The output frequencies in Normal Divider Mode are defined according to the following formulas:

$$f_{OUT} = \frac{f_{FPI} \times \frac{1}{n}}{2}, \text{ with n = 1024 - STEP} \quad (3.14)$$

In order to get $f_{OUT} = f_{FPI}/2$ STEP must be programmed with $3FF_H$.

Fractional Divider Mode

When the Fractional Divider Mode is selected (FDR.DM = 10_B), the output is derived from the input clock f_{FPI} by division of a fraction of n/1024 for any value of n from 0 to 1023 followed by the division of two. In general, the Fractional Divider Mode makes it possible to program the average output clock frequency with a higher accuracy than in Normal Divider Mode.

In Fractional Divider Mode, a pulse is generated depending on the result of the addition FDR.RESULT + FDR.STEP. If the addition leads to an overflow over $3FF_H$, a pulse is generated for the divider by two. Note that in Fractional Divider Mode the clock f_{OUT} can have a maximum period jitter of one f_{FPI} clock period.

The output frequencies in Fractional Divider Mode are defined according to the following formulas:

$$f_{OUT} = \frac{f_{FPI} \times \frac{n}{1024}}{2}, \text{ with n = 0-1023} \quad (3.15)$$

External Clock Enable

When the external clock generation with the fractional divider has been disabled by software (setting FDR.DISCLK = 1), the disable state can be exited (hardware controlled) when the External Clock Enable input = 1.

Programmable Frequency Output for EXTCLK1

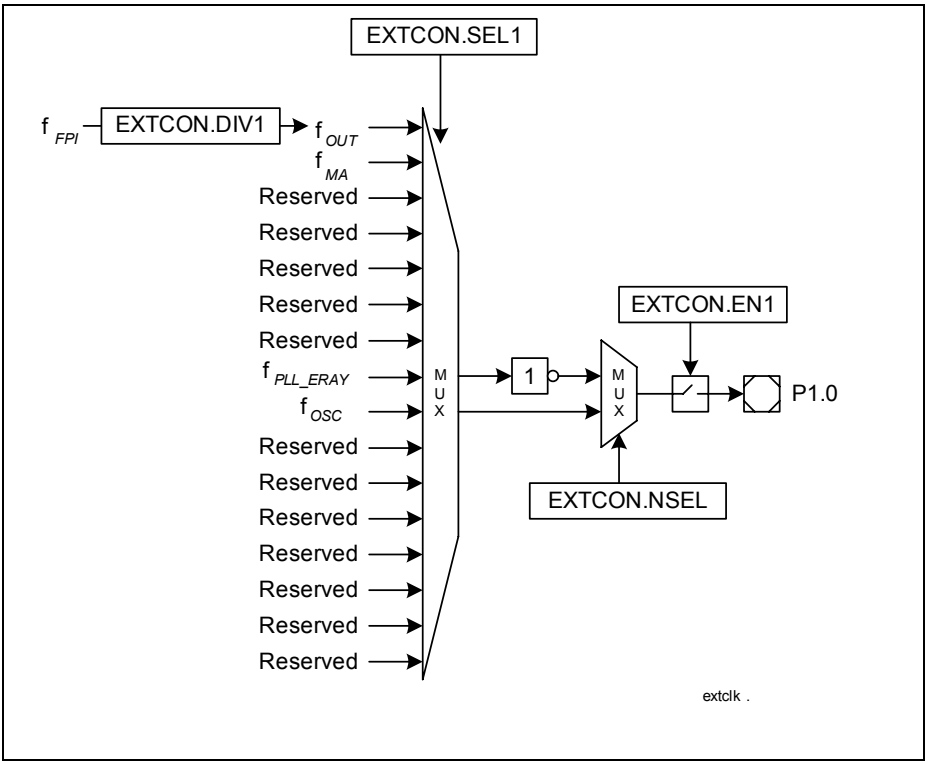


Figure 3-17 EXTCLK1 Generation

Clock f_{OUT} is generated via a counter, so the output frequency can be selected in small steps.

f_{OUT} always provides complete output periods.

Register EXTCON provides control over the output generation (frequency, activation).

3.1.1.7 CGU Registers

System Oscillator Register

This register controls the settings of OSC.

OSCCON
OSC Control Register **(010_H)** **Reset Value: 0000 021A$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0											OSCVAL				
r											rw				

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0				X1D EN	X1D	PLL SP	PLL HV	0	MODE		GAINSEL		OSC RES	PLL LV	0
r				rw	rh	rh	rh	rw	rw		rh		w	rh	

Field	Bits	Type	Description
PLLLV	1	rh	**Oscillator for PLL Valid Low Status Bit** This bit indicates if the frequency output of OSC is usable for the VCO part of the PLL. This is checked by the Oscillator Watchdog of the PLL. 0_B The OSC frequency is not usable. Frequency f_{REF} is too low. 1_B The OSC frequency is usable
OSCRES	2	w	**Oscillator Watchdog Reset** 0_B The Oscillator Watchdog of the PLL is not cleared and remains active 1_B The Oscillator Watchdog of the PLL is cleared and restarted
GAINSEL	[4:3]	rw	**Oscillator Gain Selection** 00_B Reserved, do not use this combination 01_B The gain control is configured for frequencies from 8 MHz to 16 MHz 10_B The gain control is configured for frequencies from 8 MHz to 20 MHz 11_B The gain control is configured for frequencies from 8 MHz to 25 MHz

Field	Bits	Type	Description
MODE	[6:5]	rw	**Oscillator Mode** This bit field defines which mode can be used and if the oscillator entered the Power-Saving Mode or not. 00_B External Crystal Mode and External Input Clock Mode. The oscillator Power-Saving Mode is not entered. 01_B OSC is disabled. The oscillator Power-Saving Mode is not entered. 10_B External Input Clock Mode and the oscillator Power-Saving Mode is entered 11_B OSC is disabled. The oscillator Power-Saving Mode is entered.
PLLHV	8	rh	**Oscillator for PLL Valid High Status Bit** This bit indicates if the frequency output of OSC is usable for the VCO part of the PLL. This is checked by the Oscillator Watchdog of the PLL. 0_B The OSC frequency is not usable. Frequency f_{OSC} is too high. 1_B The OSC frequency is usable
PLLSP	9	rh	**Oscillator for PLL Valid Spike Status Bit** This bit indicates if the frequency output of OSC is usable for the VCO part of the PLL. This is checked by the Oscillator Watchdog of the PLL. 0_B The OSC frequency is not usable. Spikes are detected that disturb a locked operation 1_B The OSC frequency is usable
X1D	10	rh	**XTAL1 Data Value** This bit monitors the value (level) of pin XTAL1. If XTAL1 is not used as clock input it can be used as GPI pin. This bit is only updated if X1DEN is set.
X1DEN	11	rw	**XTAL1 Data Enable** 0_B Bit X1D is not updated 1_B Bit X1D can be updated

Field	Bits	Type	Description
OSCVAL	[20:16]	rw	**OSC Frequency Value** This bit field defines the divider value that generates the reference clock that is supervised by the oscillator watchdog. f_{OSC} is divided by OSCVAL + 1 in order to generate f_{OSCREF}.
0	7	rw	**Reserved** Should be written with 0.
0	0, [15:12], [31:21]	r	**Reserved** Read as 0; should be written with 0.

PLL Registers

These registers control the setting of the PLL.

PLLSTAT
PLL Status Register **(014_H)** **Reset Value: $0000\ 0038_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0								**MODRUN**	**0**	**K2RDY**	**K1RDY**	**FINDIS**	**VCOLOCK**	**PWDSTAT**	**VCOBYST**
r								rh	r	rh	rh	rh	rh	rh	rh

Field	Bits	Type	Description
VCOBYST	0	rh	**VCO Bypass Status** 0_B Freerunning / Normal Mode is entered 1_B Prescaler Mode is entered
PWDSTAT	1	rh	**PLL Power-saving Mode Status** 0_B PLL Power-saving Mode was not entered 1_B PLL Power-saving Mode was entered

Field	Bits	Type	Description
VCOLOCK	2	rh	**PLL VCO Lock Status** 0_B The frequency difference of f_{REF} and f_{DIV} is greater than allowed. The VCO part of the PLL can not lock on a target frequency. 1_B The frequency difference of f_{REF} and f_{DIV} is small enough to enable a stable VCO operation. *Note: In case of a loss of VCO lock the f_{VCO} goes to the upper boundary of the VCO frequency if the reference clock input is greater than expected.* *Note: In case of a loss of VCO lock the f_{VCO} goes to the lower boundary of the VCO frequency if the reference clock input is lower than expected.*
FINDIS	3	rh	**Input Clock Disconnect Select Status** 0_B The input clock from the oscillator is connected to the VCO part 1_B The input clock from the oscillator is disconnected from the VCO part *Note: This bit can be set by setting bit PLLCON0.SETFINDIS.* *Note: This bit can be cleared by setting bit PLLCON0.CLRFINDIS.*
K1RDY	4	rh	**K1 Divider Ready Status** This bit indicates if the K1-divider operates on the configured value or not. this is of interest if the values is changed. 0_B K1-Divider is not ready to operate with the new value 1_B K1-Divider is ready to operate with the new value

Field	Bits	Type	Description
K2RDY	5	rh	**K2 Divider Ready Status** This bit indicates if the K2-divider operates on the configured value or not. this is of interest if the values is changed. 0_B K2-Divider is not ready to operate with the new value 1_B K2-Divider is ready to operate with the new value
MODRUN	7	rh	**Modulation Run** This bit indicates if the frequency modulation of the PLL is activated or not. 0_B Frequency modulation is not active 1_B Frequency modulation is active
0	6, [31:8]	r	**Reserved** Read as 0; should be written with 0.

PLLCON0
PLL Configuration 0 Register **(018_H)** **Reset Value: 0001 C600$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0				PDIV				0					RES LD	0	1
rw				rw				r					w	r	rw

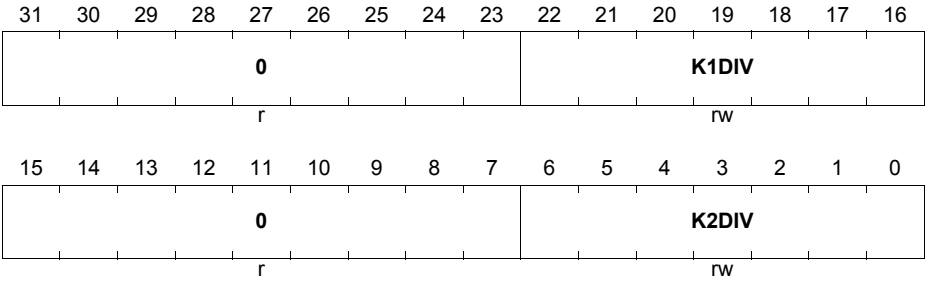
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NDIV							0	0	OSC DISC DIS	CLR FIN DIS	SET FIN DIS	0	MOD EN	VCO PWD	VCO BYP
rw							rw	r	rw	w	w	rw	rw	rw	rw

Field	Bits	Type	Description
VCOBYP	0	rw	**VCO Bypass** 0_B Normal operation, VCO is not bypassed 1_B Prescaler Mode; VCO is bypassed

Field	Bits	Type	Description
VCOPWD	1	rw	**VCO Power Saving Mode** 0_B Normal behavior 1_B The VCO is put into a Power Saving Mode and can no longer be used. Only Prescaler Mode are active if previously selected.
MODEN	2	rw	**Modulation Enable** This bit controls the activation of the frequency modulation of the PLL. 0_B Frequency modulation is not activated 1_B Frequency modulation is activated
SETFINDIS	4	w	**Set Status Bit PLLSTAT.FINDIS** 0_B Bit PLLSTAT.FINDIS is left unchanged 1_B Bit PLLSTAT.FINDIS is set. The input clock from the oscillator is disconnected from the VCO part.
CLRFINDIS	5	w	**Clear Status Bit PLLSTAT.FINDIS** 0_B Bit PLLSTAT.FINDIS is left unchanged 1_B Bit PLLSTAT.FINDIS is cleared. The input clock from the oscillator is connected to the VCO part.
OSCDISCDIS	6	rw	**Oscillator Disconnect Disable** This bit is used to disable the control PLLSTAT.FINDIS in a PLL loss-of-lock case. 0_B In case of a PLL loss-of-lock bit PLLSTAT.FINDIS is set 1_B In case of a PLL loss-of-lock bit PLLSTAT.FINDIS is cleared
NDIV	[15:9]	rw	**N-Divider Value** The value the N-Divider operates is NDIV+1.
RESLD	18	w	**Restart VCO Lock Detection** Setting this bit will clear bit PLLSTAT.VCOLOCK and restart the VCO lock detection. Reading this bit returns always a zero.
PDIV	[27:24]	rw	**P-Divider Value** The value the P-Divider operates is PDIV+1.
0	3, 8, [31:28]	rw	**Reserved** Have to be written with 0.

Field	Bits	Type	Description
1	16	rw	**Reserved** Should be written with 1.
0	7, 17, [23:19]	r	**Reserved** Read as 0; should be written with 0.

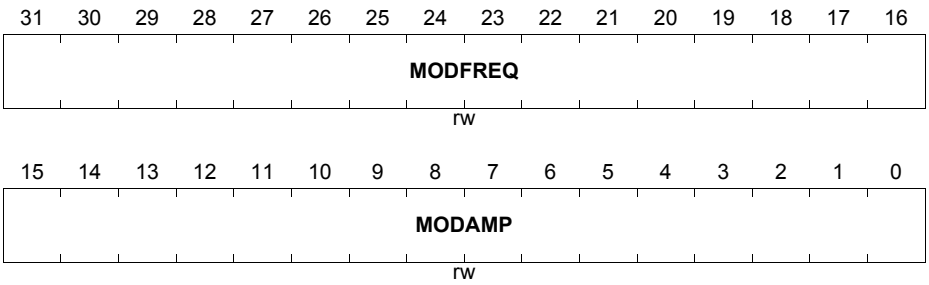
PLLCON1
PLL Configuration 1 Register **($01C_H$)** **Reset Value: 0002 000F$_H$**



Field	Bits	Type	Description
K2DIV	[6:0]	rw	**K2-Divider Value** The value the K2-Divider operates is K2DIV+1.
K1DIV	[22:16]	rw	**K1-Divider Value** The value the K1-Divider operates is K1DIV+1.
0	[15:7], [31:23]	r	**Reserved** Read as 0; should be written with 0.

PLLCON2

PLL Configuration 2 Register **(020_H)** **Reset Value: 0000 0000$_H$**



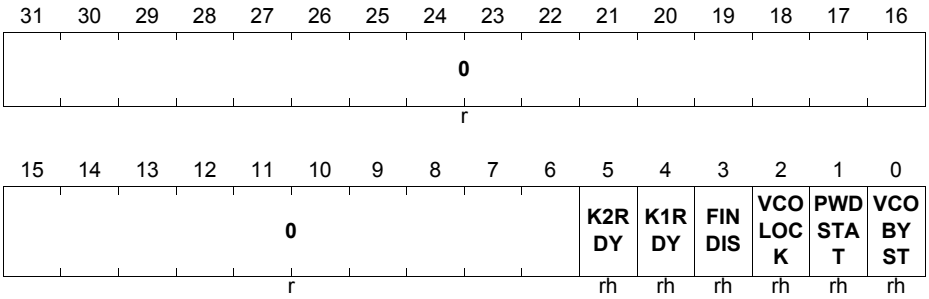
Field	Bits	Type	Description
MODAMP	[15:0]	rw	**Modulation Amplitude** This bit field defines the amplitude of the modulation.
MODFREQ	[31:16]	rw	**Modulation Frequency** This bit field defines the modulation frequency.

PLL_ERAY Registers

These registers controls the setting of the PLL_ERAY.

PLLERAYSTAT

PLL_ERAY Status Register **(024_H)** **Reset Value: 0000 0038$_H$**



Field	Bits	Type	Description
VCOBYST	0	rh	**VCO Bypass Status** 0_B Freerunning / Normal Mode is entered 1_B Prescaler Mode is entered
PWDSTAT	1	rh	**PLL_ERAY Power-saving Mode Status** 0_B PLL_ERAY Power-saving Mode was not entered 1_B PLL_ERAY Power-saving Mode was entered
VCOLOCK	2	rh	**PLL VCO Lock Status** 0_B The frequency difference of f_{REF} and f_{DIV} is greater than allowed. The VCO part of the PLL_ERAY can not lock on a target frequency. 1_B The frequency difference of f_{REF} and f_{DIV} is small enough to enable a stable VCO operation. *Note: In case of a loss of VCO lock the f_{VCO} goes to the upper boundary of the VCO frequency if the reference clock input is greater than expected.* *Note: In case of a loss of VCO lock the f_{VCO} goes to the lower boundary of the VCO frequency if the reference clock input is lower than expected.*
FINDIS	3	rh	**Input Clock Disconnect Select Status** 0_B The input clock from the oscillator is connected to the VCO part 1_B The input clock from the oscillator is disconnected from the VCO part *Note: This bit can be set by setting bit PLLERAYCON0.SETFINDIS.* *Note: This bit can be cleared by setting bit PLLERAYCON0.CLRFINDIS.*

Field	Bits	Type	Description
K1RDY	4	rh	**K1 Divider Ready Status** This bit indicates if the K1-divider operates on the configured value or not. this is of interest if the values is changed. 0_B K1-Divider is not ready to operate with the new value 1_B K1-Divider is ready to operate with the new value
K2RDY	5	rh	**K2 Divider Ready Status** This bit indicates if the K2-divider operates on the configured value or not. this is of interest if the values is changed. 0_B K2-Divider is not ready to operate with the new value 1_B K2-Divider is ready to operate with the new value
0	[31:6]	r	**Reserved** Read as 0; should be written with 0.

PLLERAYCON0
PLL_ERAY Configuration 0 Register (028_H) **Reset Value: 0001 2E00$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0													RESLD	0	1
r													w	r	rw

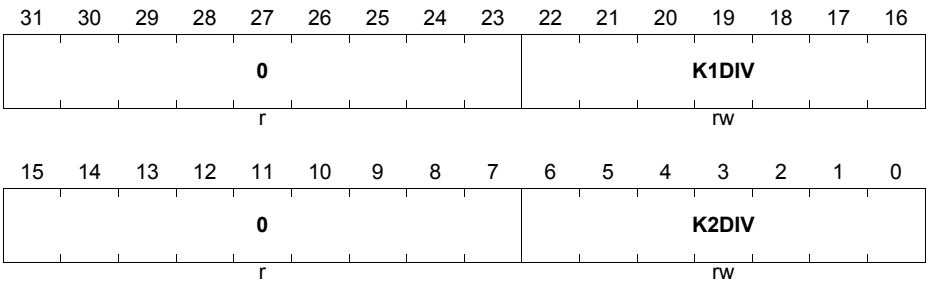
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	NDIV					0		OSCDISCDIS	CLRFINDIS	SETFINDIS	0		VCOPWD	VCOBYP
r	rw	rw					r		rw	w	w	r		rw	rw

Field	Bits	Type	Description
VCOBYP	0	rw	**VCO Bypass** 0_B Normal operation, VCO is not bypassed 1_B Prescaler Mode; VCO is bypassed

Field	Bits	Type	Description
VCOPWD	1	rw	**VCO Power Saving Mode** 0_B Normal behavior 1_B The VCO is put into a Power Saving Mode and can no longer be used.
SETFINDIS	4	w	**Set Status Bit PLLERAYSTAT.FINDIS** 0_B Bit PLLERAYSTAT.FINDIS is left unchanged 1_B Bit PLLERAYSTAT.FINDIS is set. The input clock from the oscillator is disconnected from the VCO part.
CLRFINDIS	5	w	**Clear Status Bit PLLERAYSTAT.FINDIS** 0_B Bit PLLERAYSTAT.FINDIS is left unchanged 1_B Bit PLLERAYSTAT.FINDIS is cleared. The input clock from the oscillator is connected to the VCO part.
OSCDISCDIS	6	rw	**Oscillator Disconnect Disable** This bit is used to disable the control PLLERAYSTAT.FINDIS in a PLL_ERAY loss-of-lock case. 0_B In case of a PLL loss-of-lock bit PLLERAYSTAT.FINDIS is set 1_B In case of a PLL loss-of-lock bit PLLERAYSTAT.FINDIS is cleared
NDIV	[13:9]	rw	**N-Divider Value** The value the N-Divider operates is (NDIV+1).
RESLD	18	w	**Restart VCO Lock Detection** Setting this bit will clear bit PLLERAYSTAT.VCOLOCK and restart the VCO lock detection. Reading this bit returns always a zero.
0	14	rw	**Reserved** Should be written with 0.
1	16	rw	**Reserved** Should be written with 1.
0	[3:2], [8:7], 15, 17, [31:19]	r	**Reserved** Read as 0; should be written with 0.

PLLERAYCON1

PLL_ERAY Configuration 1 Register (02C$_H$) **Reset Value: 000F 000F$_H$**

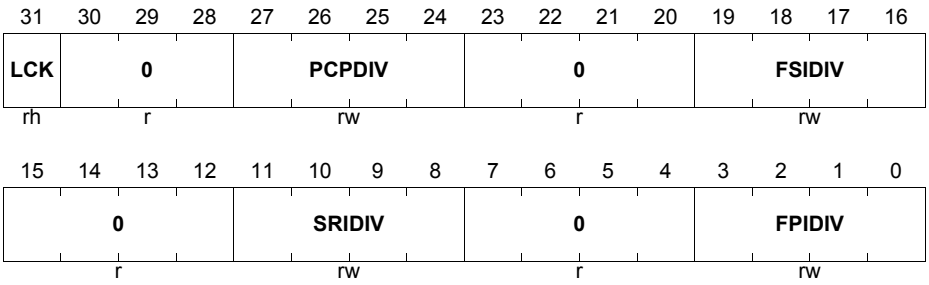


Field	Bits	Type	Description
K2DIV	[6:0]	rw	**K2-Divider Value** The value the K2-Divider operates is K2DIV+1.
K1DIV	[22:16]	rw	**K1-Divider Value** The value the K1-Divider operates is K1DIV+1.
0	[15:7], [31:23]	r	**Reserved** Read as 0; should be written with 0.

CCU Control Registers

CCUCON0

CCU Clock Control Register 0 (030$_H$) **Reset Value: 0000 0000$_H$**



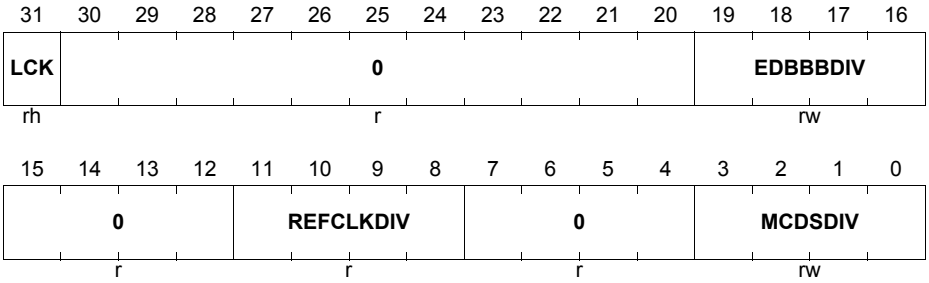
Field	Bits	Type	Function
FPIDIV	[3:0]	rw	**FPI-Bus Divider Reload Value** 0000_B $f_{FPI} = f_{PLL}$ 0001_B $f_{FPI} = f_{PLL}/2$ 0010_B $f_{FPI} = f_{PLL}/3$ 0011_B $f_{FPI} = f_{PLL}/4$ 0100_B $f_{FPI} = f_{PLL}/5$ 0101_B $f_{FPI} = f_{PLL}/6$ 0110_B $f_{FPI} = f_{PLL}/7$ 0111_B $f_{FPI} = f_{PLL}/8$ 1000_B $f_{FPI} = f_{PLL}/9$ 1001_B $f_{FPI} = f_{PLL}/10$ 1010_B $f_{FPI} = f_{PLL}/11$ 1011_B $f_{FPI} = f_{PLL}/12$ 1100_B $f_{FPI} = f_{PLL}/13$ 1101_B $f_{FPI} = f_{PLL}/14$ 1110_B $f_{FPI} = f_{PLL}/15$ 1111_B $f_{FPI} = f_{PLL}/16$
SRIDIV	[11:8]	rw	**SRI-Bus Divider Reload Value** 0000_B $f_{SRI} = f_{PLL}$ 0001_B $f_{SRI} = f_{PLL}/2$ 0010_B $f_{SRI} = f_{PLL}/3$ 0011_B $f_{SRI} = f_{PLL}/4$ 0100_B $f_{SRI} = f_{PLL}/5$ 0101_B $f_{SRI} = f_{PLL}/6$ 0110_B $f_{SRI} = f_{PLL}/7$ 0111_B $f_{SRI} = f_{PLL}/8$ 1000_B $f_{SRI} = f_{PLL}/9$ 1001_B $f_{SRI} = f_{PLL}/10$ 1010_B $f_{SRI} = f_{PLL}/11$ 1011_B $f_{SRI} = f_{PLL}/12$ 1100_B $f_{SRI} = f_{PLL}/13$ 1101_B $f_{SRI} = f_{PLL}/14$ 1110_B $f_{SRI} = f_{PLL}/15$ 1111_B $f_{SRI} = f_{PLL}/16$

Field	Bits	Type	Function
FSIDIV	[19:16]	rw	**FSI Divider Reload Value** 0000_B $f_{FSI} = f_{PLL}$ 0001_B $f_{FSI} = f_{PLL}/2$ 0010_B $f_{FSI} = f_{PLL}/3$ 0011_B $f_{FSI} = f_{PLL}/4$ 0100_B $f_{FSI} = f_{PLL}/5$ 0101_B $f_{FSI} = f_{PLL}/6$ 0110_B $f_{FSI} = f_{PLL}/7$ 0111_B $f_{FSI} = f_{PLL}/8$ 1000_B $f_{FSI} = f_{PLL}/9$ 1001_B $f_{FSI} = f_{PLL}/10$ 1010_B $f_{FSI} = f_{PLL}/11$ 1011_B $f_{FSI} = f_{PLL}/12$ 1100_B $f_{FSI} = f_{PLL}/13$ 1101_B $f_{FSI} = f_{PLL}/14$ 1110_B $f_{FSI} = f_{PLL}/15$ 1111_B $f_{FSI} = f_{PLL}/16$
PCPDIV	[27:24]	rw	**PCP Divider Reload Value** 0000_B $f_{PCP} = f_{PLL}$ 0001_B $f_{PCP} = f_{PLL}/2$ 0010_B $f_{PCP} = f_{PLL}/3$ 0011_B $f_{PCP} = f_{PLL}/4$ 0100_B $f_{PCP} = f_{PLL}/5$ 0101_B $f_{PCP} = f_{PLL}/6$ 0110_B $f_{PCP} = f_{PLL}/7$ 0111_B $f_{PCP} = f_{PLL}/8$ 1000_B $f_{PCP} = f_{PLL}/9$ 1001_B $f_{PCP} = f_{PLL}/10$ 1010_B $f_{PCP} = f_{PLL}/11$ 1011_B $f_{PCP} = f_{PLL}/12$ 1100_B $f_{PCP} = f_{PLL}/13$ 1101_B $f_{PCP} = f_{PLL}/14$ 1110_B $f_{PCP} = f_{PLL}/15$ 1111_B $f_{PCP} = f_{PLL}/16$
LCK	31	rh	**Lock Status** This bit indicates if the register can be updated with a new value or if the register is locked and a write action from the bus side has no effect. 0_B The register is unlocked and can be updated 1_B The register is locked and can not be updated

Field	Bits	Type	Function
0	[7:4], [15:12], [23:20], [30:28]	r	**Reserved** Read as 0; should be written with 0.

CCUCON1
CCU Clock Control Register 1

(034$_H$) **Reset Value: 0005 0B03$_H$**



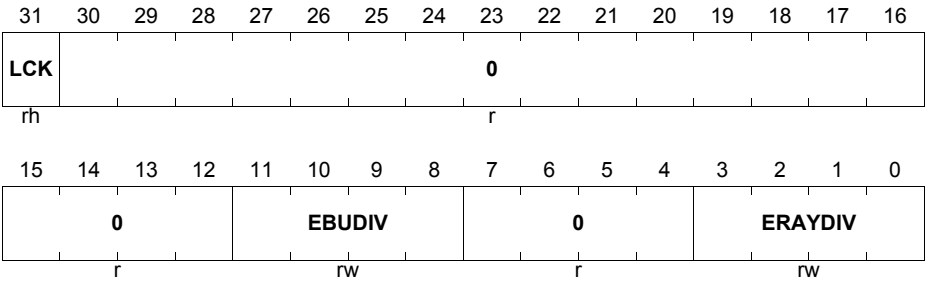
Field	Bits	Type	Function
MCDSDIV	[3:0]	rw	**MCDS Divider Reload Value** 0000_B.f_{MCDS} = f_{PLL} 0001_B.f_{MCDS} = f_{PLL}/2 0010_B.f_{MCDS} = f_{PLL}/3 0011_B.f_{MCDS} = f_{PLL}/4 0100_B.f_{MCDS} = f_{PLL}/5 0101_B.f_{MCDS} = f_{PLL}/6 0110_B.f_{MCDS} = f_{PLL}/7 0111_B.f_{MCDS} = f_{PLL}/8 1000_B.f_{MCDS} = f_{PLL}/9 1001_B.f_{MCDS} = f_{PLL}/10 1010_B.f_{MCDS} = f_{PLL}/11 1011_B.f_{MCDS} = f_{PLL}/12 1100_B.f_{MCDS} = f_{PLL}/13 1101_B.f_{MCDS} = f_{PLL}/14 1110_B.f_{MCDS} = f_{PLL}/15 1111_B.f_{MCDS} = f_{PLL}/16

Field	Bits	Type	Function
REFCLKDIV	[11:8]	r	**Reference Clock for MCDS Divider Reload Value** 0000_B.$f_{REFCLK2} = f_{PLL\_ERAY}/2$ and $f_{REFCLK1} = f_{PLL}/2$ 0001_B.$f_{REFCLK2} = f_{PLL\_ERAY}/4$ and $f_{REFCLK1} = f_{PLL}/4$ 0010_B.$f_{REFCLK2} = f_{PLL\_ERAY}/6$ and $f_{REFCLK1} = f_{PLL}/6$ 0011_B.$f_{REFCLK2} = f_{PLL\_ERAY}/8$ and $f_{REFCLK1} = f_{PLL}/8$ 0100_B.$f_{REFCLK2} = f_{PLL\_ERAY}/10$ and $f_{REFCLK1} = f_{PLL}/10$ 0101_B.$f_{REFCLK2} = f_{PLL\_ERAY}/12$ and $f_{REFCLK1} = f_{PLL}/12$ 0110_B.$f_{REFCLK2} = f_{PLL\_ERAY}/14$ and $f_{REFCLK1} = f_{PLL}/14$ 0111_B.$f_{REFCLK2} = f_{PLL\_ERAY}/16$ and $f_{REFCLK1} = f_{PLL}/16$ 1000_B.$f_{REFCLK2} = f_{PLL\_ERAY}/18$ and $f_{REFCLK1} = f_{PLL}/18$ 1001_B.$f_{REFCLK2} = f_{PLL\_ERAY}/20$ and $f_{REFCLK1} = f_{PLL}/20$ 1010_B.$f_{REFCLK2} = f_{PLL\_ERAY}/22$ and $f_{REFCLK1} = f_{PLL}/22$ 1011_B.$f_{REFCLK2} = f_{PLL\_ERAY}/24$ and $f_{REFCLK1} = f_{PLL}/24$ 1100_B.$f_{REFCLK2} = f_{PLL\_ERAY}/26$ and $f_{REFCLK1} = f_{PLL}/26$ 1101_B.$f_{REFCLK2} = f_{PLL\_ERAY}/28$ and $f_{REFCLK1} = f_{PLL}/28$ 1110_B.$f_{REFCLK2} = f_{PLL\_ERAY}/30$ and $f_{REFCLK1} = f_{PLL}/30$ 1111_B.$f_{REFCLK2} = f_{PLL\_ERAY}/32$ and $f_{REFCLK1} = f_{PLL}/32$
EDBBBDIV	[19:16]	rw	**ED part Backbone Bus Divider Reload Value** 0000_B.$f_{BBB} = f_{PLL}$ 0001_B.$f_{BBB} = f_{PLL}/2$ 0010_B.$f_{BBB} = f_{PLL}/3$ 0011_B.$f_{BBB} = f_{PLL}/4$ 0100_B.$f_{BBB} = f_{PLL}/5$ 0101_B.$f_{BBB} = f_{PLL}/6$ 0110_B.$f_{BBB} = f_{PLL}/7$ 0111_B.$f_{BBB} = f_{PLL}/8$ 1000_B.$f_{BBB} = f_{PLL}/9$ 1001_B.$f_{BBB} = f_{PLL}/10$ 1010_B.$f_{BBB} = f_{PLL}/11$ 1011_B.$f_{BBB} = f_{PLL}/12$ 1100_B.$f_{BBB} = f_{PLL}/13$ 1101_B.$f_{BBB} = f_{PLL}/14$ 1110_B.$f_{BBB} = f_{PLL}/15$ 1111_B.$f_{BBB} = f_{PLL}/16$
LCK	31	rh	**Lock Status** This bit indicates if the register can be updated with a new value or if the register is locked and a write action from the bus side has no effect. 0_B The register is unlocked and can be updated 1_B The register is locked and can not be updated

Field	Bits	Type	Function
0	[7:4], [15:12], [30:20]	r	**Reserved** Read as 0; should be written with 0.

CCUCON2

CCU Clock Control Register 2 **(044_H)** **Reset Value: 0000 0001$_H$**



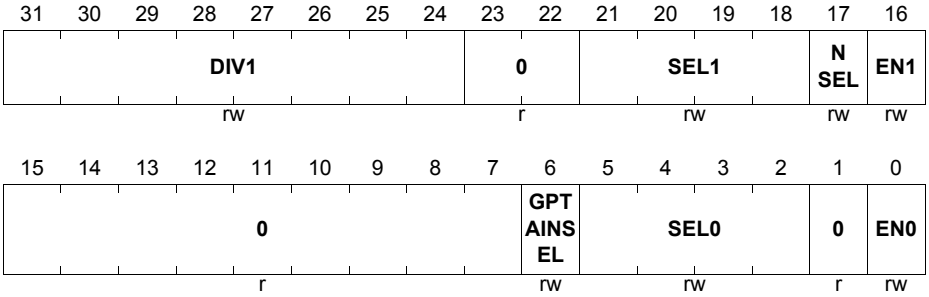
Field	Bits	Type	Function
ERAYDIV	[3:0]	rw	**ERAY-Bus Divider Reload Value** 0000_B $f_{ERAY} = f_{PLL\_ERAY}$ 0001_B $f_{ERAY} = f_{PLL\_ERAY}/2$ 0010_B $f_{ERAY} = f_{PLL\_ERAY}/3$ 0011_B $f_{ERAY} = f_{PLL\_ERAY}/4$ 0100_B $f_{ERAY} = f_{PLL\_ERAY}/5$ 0101_B $f_{ERAY} = f_{PLL\_ERAY}/6$ 0110_B $f_{ERAY} = f_{PLL\_ERAY}/7$ 0111_B $f_{ERAY} = f_{PLL\_ERAY}/8$ 1000_B $f_{ERAY} = f_{PLL\_ERAY}/9$ 1001_B $f_{ERAY} = f_{PLL\_ERAY}/10$ 1010_B $f_{ERAY} = f_{PLL\_ERAY}/11$ 1011_B $f_{ERAY} = f_{PLL\_ERAY}/12$ 1100_B $f_{ERAY} = f_{PLL\_ERAY}/13$ 1101_B $f_{ERAY} = f_{PLL\_ERAY}/14$ 1110_B $f_{ERAY} = f_{PLL\_ERAY}/15$ 1111_B $f_{ERAY} = f_{PLL\_ERAY}/16$

Field	Bits	Type	Function
EBUDIV	[11:8]	rw	**EBU-Bus Divider Reload Value** 0000_B $f_{EBU} = f_{PLL\_ERAY}$ 0001_B $f_{EBU} = f_{PLL\_ERAY}/2$ 0010_B $f_{EBU} = f_{PLL\_ERAY}/3$ 0011_B $f_{EBU} = f_{PLL\_ERAY}/4$ 0100_B $f_{EBU} = f_{PLL\_ERAY}/5$ 0101_B $f_{EBU} = f_{PLL\_ERAY}/6$ 0110_B $f_{EBU} = f_{PLL\_ERAY}/7$ 0111_B $f_{EBU} = f_{PLL\_ERAY}/8$ 1000_B $f_{EBU} = f_{PLL\_ERAY}/9$ 1001_B $f_{EBU} = f_{PLL\_ERAY}/10$ 1010_B $f_{EBU} = f_{PLL\_ERAY}/11$ 1011_B $f_{EBU} = f_{PLL\_ERAY}/12$ 1100_B $f_{EBU} = f_{PLL\_ERAY}/13$ 1101_B $f_{EBU} = f_{PLL\_ERAY}/14$ 1110_B $f_{EBU} = f_{PLL\_ERAY}/15$ 1111_B $f_{EBU} = f_{PLL\_ERAY}/16$
LCK	31	rh	**Lock Status** This bit indicates if the register can be updated with a new value or if the register is locked and a write action from the bus side has no effect. 0_B The register is unlocked and can be updated 1_B The register is locked and can not be updated
0	[7:4], [30:12]	r	**Reserved** Read as 0; should be written with 0.

Clock Output Control Register

This register controls the setting of external clock for pin 1.0 and 1.12 (EXTCLK0 and EXTCLK1).

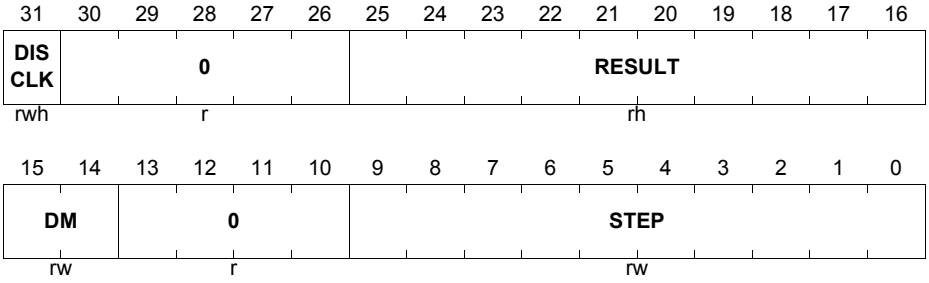
EXTCON
External Clock Control Register ($03C_H$) Reset Value: $0000\ 0000_H$



Field	Bits	Type	Description
EN0	0	rw	**External Clock Enable for EXTCLK0** 0_B No external clock is provided 1_B The configured external clock is provided
SEL0	[5:2]	rw	**External Clock Select for EXTCLK0** This bit field defines the clock source that is selected as output for pin EXTCLK0. 0000_B.f_{OUT} is selected for the external clock 0001_B.f_{PLL} is selected for the external clock 0010_B Reserved, do not use this combination ... 0110_B Reserved, do not use this combination 0111_B.f_{PLL_ERAY} is selected for the external clock signal 1000_B.f_{OSC} is selected for the external clock signal 1001_B Reserved, do not use this combination ... 1110_B Reserved, do not use this combination 1111_B.f_{MT} from the ERAY module is selected for the external clock

Field	Bits	Type	Description
GPTAINSEL	6	rw	**GPTA Input Select** This value defines if either the input from P2.8 or the configured output frequency for EXTCLK0 is used as input for IN0 of the GPTA module. 0_B P2.8 is selected as input for IN0 of the GPTA 1_B EXTCLK0 output is selected as input for IN0 of the GPTA
EN1	16	rw	**External Clock Enable for EXTCLK1** 0_B No external clock is provided 1_B The configured external clock is provided
NSEL	17	rw	**Negation Selection** 0_B The external clock is inverted 1_B The external clock is not inverted
SEL1	[21:18]	rw	**External Clock Select for EXTCLK1** This bit field defines the clock source that is selected as output for pin EXTCLK1. 0000_B f_{OUT} is selected for the external clock 0001_B f_{PLL} is selected for the external clock 0010_B Reserved, do not use this combination ... 0110_B Reserved, do not use this combination 0111_B f_{PLL_ERAY} is selected for the external clock signal 1000_B f_{OSC} is selected for the external clock signal 1001_B Reserved, do not use this combination ... 1111_B Reserved, do not use this combination
DIV1	[31:24]	rw	**External Clock Divider for EXTCLK1** This value defines the reload value of the divider that generates f_{OUT} out of f_{FPI} ($f_{OUT} = f_{FPI}/(DIV1+1)$). The divider itself is cleared each time bit EN1 is cleared.
0	1, [15:7], [23:22]	r	**Reserved** Read as 0; should be written with 0.

FDR
Fractional Divider Register **(038_H)** **Reset Value: 0000 0000_H**



Field	Bits	Type	Description
STEP	[9:0]	rw	**Step Value** In Normal Divider Mode, STEP contains the reload value for RESULT. In Fractional Divider Mode, this bit field determines the 10-bit value that is added to RESULT with each input clock cycle.
DM	[15:14]	rw	**Divider Mode** This bit fields determines the functionality of the fractional divider block. 00_B Fractional divider is switched off; no output clock is generated. The Reset External Divider signal is 1. RESULT is not updated (default after System Reset). 01_B Normal Divider Mode selected. 10_B Fractional Divider Mode selected. 11_B Fractional divider is switched off; no output clock is generated. RESULT is not updated.
RESULT	[25:16]	rh	**Result Value** In Normal Divider Mode, RESULT acts as reload counter (addition +1). In Fractional Divider Mode, this bit field contains the result of the addition RESULT + STEP. If DM is written with 01_B or 10_B, RESULT is loaded with $3FF_H$.

Field	Bits	Type	Description
DISCLK	31	rwh	**Disable Clock** 0_B Clock generation of f_{OUT} is enabled according to the setting of bit field DM. 1_B Fractional divider is stopped. No change except when writing bit field DM. This bit is cleared when external clock enable input is asserted. In case of a conflict between hardware clear and software set of DISCLK, the software set wins. Any write or read-modify-write action leads to the described behavior. As a result, read-modify-write operations should be avoided.
0	[13:10], [30:26]	r	**Reserved** Read as 0; should be written with 0.

3.1.2 Module Clock Generation

The TC1798 on-chip modules have two registers for clock control:

- Clock Control Register CLC
- Fractional Divider Register FDR

The following sections describes the general functionality of CLC and FDR. The module-specific implementation details are described in the corresponding module chapters.

3.1.2.1 Clock Control Register CLC

All CLC registers have basically the same bit and bit field layout. However, not all CLC register functions are implemented for each peripheral module. **Table 3-2** defines in detail which bits and bit fields of the CLC registers are implemented for each clock control register.

The CLC register controls the generation of the peripheral module clock which is derived from the system clock. The following functions for the module are associated with the CLC register:

- Peripheral clock static on/off control
- Module clock behavior in Sleep Mode
- Operation during Suspend Mode
- Fast Shut-off Mode control

Module Enable/Disable Control

If a module is not used at all by an application, it can be completely shut off by setting bit DISR in its CLC register. For peripheral modules with a run mode clock divider field RMC, a second option to completely switch off the module is to set bit field RMC to 00_H. This also disables the module's operation.

The status bit DISS always indicates whether a module is currently switched off (DISS = 1) or switched on (DISS = 0).

Write operations to the non CLC registers of disabled modules are not allowed. However, the CLC of a disabled module can be written. An attempt to write to any of the other writable registers of a disabled module except CLC will cause the corresponding Bus Control Unit (BCU) to generate a bus error.

A read operation of registers of a disabled module is allowed and does not generate a bus error.

When a disabled module is switched on by writing an appropriate value to its MOD_CLC register (DISR = 0 and RMC (if implemented) > 0), status bit DISS changes from 1 to 0. During the phase in which the module becomes active, any write access to corresponding module registers (when DISS is still set) will generate a bus error. Therefore, when enabling a disabled module, application software should check after activation of the module once (read back of the CLC register) to find out whether DISS is already cleared, before a module register (including the CLC register) will be written to.

Sleep Mode Control

The EDIS bit in the CLC register controls whether or not a module is stopped during Sleep Mode. If EDIS is 0, a Sleep Mode request can be recognized by the module and, when received, its clock is shut off.

If EDIS is set to 1, a Sleep Mode request is disregarded by the module and the module continues its operation.

Suspend Mode Control

During emulation and debugging of TC1798 applications, the execution of an application program can be suspended. When an application is suspended, normal operation of the application's program is halted, and the TC1798 begins (or resumes) executing a special debug monitor program. If bit SPEN is set, the operation of the peripheral module is stopped when the Suspend Mode request is generated. If SPEN is cleared, the module does not react to the Suspend Mode request and continues its normal operation. This feature allows each peripheral module to be adapted to the unique requirements of the application being debugged. Setting SPEN bits is usually performed by a debugger.

This feature is necessary because application requirements typically determine whether on-chip modules should be stopped or left running when an application is suspended for debugging. For example, a peripheral unit that is controlling the motion of an external device through motors in most cases must not be stopped so as to prevent damage of the external device due to the loss of control through the peripheral. On the other hand, it makes sense to stop the system timer while the debugger is actively controlling the chip because it should only count the time when the user's application is running.

Note that it is never appropriate for application software to set the SPEN bit. The Suspend Mode should only be set by a debug software. To guard against application software accidently setting SPEN, bit SPEN is specially protected by the mask bit SBWE. The SPEN bit can only be written if, during the same write operation, SBWE is set, too. Application software should never set SBWE. In this way, user software can not accidentally alter the value of the SPEN bit that has been set by a debugger.

Entering Disabled Mode

Software can request that a peripheral unit be put into Disabled Mode by setting DISR. A module will also be put into Disabled Mode if the Sleep Mode is requested and the module is configured to allow Sleep Mode.

In Secure Shut-off Mode, a module first finishes any operation in progress, then proceeds with an orderly shut down. When all sub-components of the module are ready to be shut down, the module signals its clock control unit, that turns off the clock to this peripheral unit, that it is now ready for shut down. The status bit DISS is updated by the peripheral unit accordingly.

During emulation and debugging, it may be necessary to monitor the instantaneous state of the machine – including all or most of its modules – at the moment a software breakpoint is reached. In such cases, it may not be desired that the kernel of a module finish whatever transaction is in progress before stopping, because that might cause important states in this module to be lost. Fast Shut-off Mode, controlled by bit FSOE, is available for this situation.

If FSOE = 0, modules are stopped as described above. This is called Secure Shut-off Mode. The module is allowed to finish whatever operation is in progress. If Fast Shut-off Mode is selected (FSOE = 1), clock generation to the unit is stopped as soon as any outstanding bus operation is finished. The clock control unit does not wait until the module has finished its transaction. This option stops the unit's clock as fast as possible, and the state of the unit will be the closest possible to the time of the occurrence of the software breakpoint.

Note: In all TC1798 modules except MultiCAN and DMA, the only shut down operating mode that is available is the Fast Shut-off ModeTC1798, regardless of the state of the FSOE bit.

Whether Secure Shut-off Mode or Fast Shut-off Mode is required depends on the application, the needs of the debugger, and the type of unit. For example, the analog-to-digital converter might allow the converter to finish a running analog conversion before it can be suspended. Otherwise the conversion might be corrupted and a wrong value could be produced when Suspend Mode is exited and the unit is enabled again. This would affect further emulation and debugging of the application's program.

On the other hand, if a problem is observed to relate to the operation of the external analog-to-digital converter itself, it might be necessary to stop the unit as fast as possible in order to monitor its current instantaneous state. To do this, the Fast Shut-off Mode option would be selected. Although proper continuation of the application's program might not be possible after such a step, this would most likely not matter in such a case.

Note that it is never appropriate for application software to set the FSOE bit. Fast Shut-off Mode should only be set by debug software. To guard against application software accidently setting FSOE, bit FSOE is specially protected by the mask bit SBWE. The SPEN bit can only be written if, during the same write operation, SBWE is set, too. Application software should never set SBWE. In this way, user software can not accidentally alter the value of the FSOE bit. Note that this is the same guard mechanism used for the SPEN bit.

Module Clock Divider Control

Peripheral modules of the TC1798 can have a RMC control bit field in their CLC registers. This Run Mode Clock control bit field makes it possible to slow down the CLC clock via a programmable clock divider circuit.

A value of 00_H in RMC disables the clock signals to these modules (CLC clock is switched off). If RMC is not equal to 00_H, the clock for a module register (f_{CLC}) accesses is generated as

(3.16)

$$f_{CLC} = \frac{f_{FPI}}{RMC}$$

where RMC is the content of its CLC register RMC field with a range of 1 to 255. If RMC is not available in a CLC register, the CLC clock frequency f_{CLC} is always equal to the frequency of f_{FPI}.

Note: The number of module clock cycles (wait states) that are required for a "destructive read" access (means: flags/bits are set/cleared by a read access) to a module register of a peripheral unit depends on the selected CLC clock frequency.
Therefore, a slower CLC clock (selected via bit field RMC in the CLC register) may result in a longer read cycle access time on the FPI-Bus for peripheral units with "destructive read" access (e.g. the ASC).

Module Clock Register Implementations

Table 3-2 shows which of the CLC register bits/bit fields are implemented for each peripheral module in the TC1798 and which modules are equipped with a fractional divider.

Table 3-2 Clock Generation Implementation of the TC1798 Peripheral Modules

Module	DISR Bit 0	DISS Bit 1	SPEN Bit 2	EDIS Bit 3	SBWE Bit 4	FSOE Bit 5	RMC	Fract. Divider [1]
ADC0 ADC1 ADC2 ADC3	✔	✔	✔	✔	✔	✔	–	–
FADC	✔	✔	✔	✔	✔	✔	–	✔
ASC0 and ASC1	✔	✔	✔	✔	✔	✔	8-bit	–
SSC0	✔	✔	✔	✔	✔	✔	–	✔
SSC1	✔	✔	✔	✔	✔	✔	–	✔
SSC2	✔	✔	✔	✔	✔	✔	–	✔
SSC3	✔	✔	✔	✔	✔	✔	–	✔
GPT120	✔	✔	✔	✔	✔	✔	–	–
GPT121	✔	✔	✔	✔	✔	✔	–	–
MultiCAN	✔	✔	✔	✔	✔	✔	–	✔
DMA	✔	✔	✔	✔	✔	✔	–	–
SDMA	✔	✔	✔	✔	✔	✔	–	–

Table 3-2 Clock Generation Implementation of the TC1798 Peripheral Modules

Module	DISR Bit 0	DISS Bit 1	SPEN Bit 2	EDIS Bit 3	SBWE Bit 4	FSOE Bit 5	RMC	Fract. Divider 1)
GPTA0 GPTA1 LTCA2	✔	✔	✔	✔	✔	✔	–	✔
MLI0	not implemented, MLI is connected to DMA_CLC							✔
MLI1	not implemented, MLI is connected to DMA_CLC							✔
MSC0	✔	✔	✔	✔	✔	✔	–	✔
MSC1	✔	✔	✔	✔	✔	✔	–	✔
PCP2	different bit definitions2)							
STM	✔	✔	✔	✔	✔	✔	3-bit	–
ERAY	✔	✔	✔	✔	✔	✔	3-bit	–
SHE	✔	✔	✔	✔	✔	✔	–	–
BMU	✔	✔	✔	✔	✔	✔	–	–
FCE	✔	✔	–	–	–	–	–	–
LMU	✔	✔	–	–	–	–	–	–

1) Further info on FDR implementations see **Table 3-4**.

2) Automatic clock switch-off capability if PCP is idle.

Fractional Divider Operation

The fractional divider divides the input clock f_{CLC} either by the factor 1/n or by a fraction of n/1024 for any value of n from 0 to 1023, and outputs the clock signal, f_{MOD}. The fractional divider is controlled by the MOD_FDR register.

The fractional divider can be configured for two operating modes:

- **Normal Divider Mode:** Reload counter (RESULT = RESULT + 1), generating an output clock pulse on counter overflow.
- **Fractional Divider Mode:** Add a STEP value to the RESULT value and generates an output clock pulse on counter overflow.

Normal Divider Mode

In Normal Divider Mode (MOD_FDR.DM = 01_B), the fractional divider behaves as a reload counter (addition of +1) that generates an output clock pulse at f_{MOD} on the transition from $3FF_H$ to 000_H. MOD_FDR.RESULT represents the counter value and MOD_FDR.STEP determines the reload value.

The output frequencies in Normal Divider Mode are defined according to the following formulas:

$$f_{MOD} = f_{CLC} \times \frac{1}{n} \quad \text{, with n = 1024 - STEP} \tag{3.17}$$

Note: Each write to register FDR with bit field DM = 01_B or 10_B sets bit field RESULT to $3FF_H$.

In order to get $f_{MOD} = f_{CLC}$ MOD_FDR.STEP must be programmed with $3FF_H$. **Figure 3-18** shows the operation of the Normal Divider Mode with a reload value of MOD_FDR.STEP = $3FD_H$.

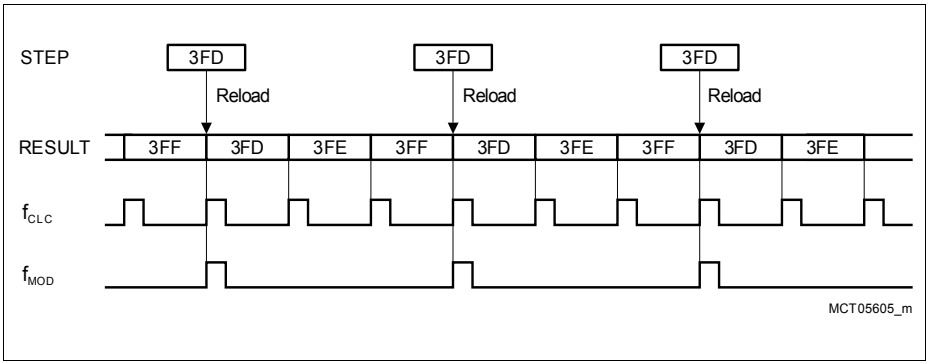


Figure 3-18 Normal Divider Mode

Fractional divider Mode

When the Fractional Divider Mode is selected (MOD_FDR.DM = 10_B), the module clock f_{MOD} is derived from the bus clock f_{CLC} by division of a fraction of n/1024 for any value of n from 0 to 1023. In general, the Fractional Divider Mode makes it possible to program the average module clock frequency with a higher accuracy than in Normal Divider Mode.

In Fractional Divider Mode, an clock pulse at f_{MOD} is generated depending on the result of the addition MOD_FDR.RESULT + MOD_FDR.STEP. If the addition leads to an overflow over $3FF_H$, a pulse is generated at f_{MOD}. Note that in Fractional Divider Mode the clock f_{MOD} can have a maximum period jitter of one f_{CLC} clock period.

The frequencies in Fractional Divider Mode are defined according to the following formula:

$$f_{MOD} = f_{CLC} \times \frac{n}{1024} \quad \text{, with n = 0-1023} \tag{3.18}$$

Note: Each write to register FDR with bit field DM = 01_B or 10_B sets bit field RESULT to $3FF_H$.

Suspend Mode

The operation of the fractional divider can be controlled by the Suspend Mode Request input. This input is activated in Suspend Mode by the on-chip debug control logic. In Suspend Mode, module registers are accessible for read and write actions, but other module internal functions are frozen.

The state of the Suspend Mode Request and Suspend Mode Acknowledge is latched in two status flags of register MOD_FDR, SUSREQ and SUSACK. Suspend Mode Request and (Suspend Mode Acknowledge or bit SM) must remain set both to maintain the Suspend Mode.

The Kernel Disable Request becomes always active when the Module Disable Request signal is activated, independently of the Suspend Mode settings in the fractional divider.

External Clock Enable

When the module clock generation has been disabled by software (setting MOD_FDR.DISCLK = 1), the disable state can be exited when the External Clock Enable input = 1. This feature is enabled when MOD_FDR.ENHW = 1.

Table 3-3 Fractional Divider Function Table

Mode	SC	DM	Result	f_{MOD}	Operation of Fractional Divider
Normal Mode	–	00_B	unchanged	inactive	switched off
		01_B	continuously updated	active	Normal Divider Mode
		10_B			Fractional Divider Mode
		11_B	unchanged	inactive	switched off
Suspend Mode	00_B	00_B	unchanged	inactive	switched off
		01_B	continuously updated	active	Normal Divider Mode
		10_B			Fractional Divider Mode
		11_B	unchanged	inactive	switched off
	01_B	00_B	unchanged		switched off
		01_B	loaded with $3FF_H$		halted
		10_B			
		11_B	unchanged	inactive	switched off
	10_B	00_B	loaded with $3FF_H$	inactive	switched off
		01_B			halted
		10_B			
		11_B			switched off
	11_B	–	loaded with $3FF_H$	inactive	switched off

Fractional Divider Register Implementations

Table 3-4 shows the implementations specific differences of the fractional divider functionality.

Table 3-4 FDR Register Implementations

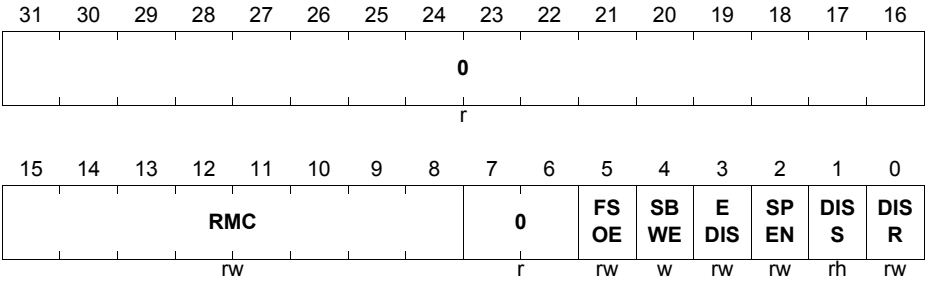
FDR Register	Suspend Mode Acknowledge Operation[1]	ENHW[2]
CAN_FDR	Acknowledge depends on module state	–
FADC_FDR	Acknowledge depends on module state	–
GPTA0_FDR	Always immediately acknowledged; independently from module states	from MultiCAN
MLI0_FDR	Acknowledge depends on module state	–
MLI1_FDR	Acknowledge depends on module state	–
MSC0_FDR	Acknowledge depends on module state	from MultiCAN
MSC1_FDR	Acknowledge depends on module state	from MultiCAN
SSC0_FDR	Always immediately acknowledged; independently from module state	from MultiCAN
SSC1_FDR	Always immediately acknowledged; independently from module state	from MultiCAN
SSC2_FDR	Always immediately acknowledged; independently from module state	from MultiCAN
SSC3_FDR	Always immediately acknowledged; independently from module state	from MultiCAN
SENT_FDR	Always immediately acknowledged; independently from module state	from MultiCAN
SSCG0_FDR SSCG1_FDR SSCG2_FDR SSCG3_FDR	Always immediately acknowledged; independently from module state	from MultiCAN

1) This column shows whether a suspend acknowledge from a FDR controlled module depends on the module's state or not. If a suspend acknowledge depends from the module state, typically module operations such as serial transmissions are terminated before a suspend request is acknowledged back to the fractional divider. Note that bit FDR.SM must be cleared (granted suspend mode selected) when using the suspend mode acknowledge/grant functionality. If immediate suspend mode is selected (FDR.SM = 1), Suspend Mode is entered at once (if FDR.SC not equal 00_B) independently from the suspend acknowledge answer from the module.

2) This column shows whether the External Clock Enable input of a fractional divider is controlled by on-chip hardware (source module see comment) or not ("–").

Module CLC Register

MOD_CLC
Clock Control Register **(00_H)** **Reset Value: Module-specific**



Field	Bits	Type	Description
DISR	0	rw	**Module Disable Request Bit** Used for enable/disable control of the module. 0_B Module disable is not requested 1_B Module disable is requested
DISS	1	rh	**Module Disable Status Bit** Bit indicates the current status of the module 0_B Module is enabled 1_B Module is disabled If the RMC field is implemented and if it is 0, DISS is set automatically.
SPEN	2	rw	**Module Suspend Enable** Used for enabling the Suspend Mode. 0_B Module cannot be suspended (suspend is disabled) 1_B Module can be suspended (suspend is enabled) This bit can be written only if SBWE is set during the same write operation.
EDIS	3	rw	**Sleep Mode Enable Control** Used for module Sleep Mode control. 0_B Sleep Mode request is regarded. Module is enabled to go into Sleep Mode. 1_B Sleep Mode request is disregarded: Sleep Mode cannot be entered on a request.

Field	Bits	Type	Description
SBWE	4	w	**Module Suspend Bit Write Enable for OCDS** Determines whether SPEN and FSOE are write-protected. 0_B Bits SPEN and FSOE are write-protected 1_B Bits SPEN and FSOE are overwritten by respective value of SPEN or FSOE Reading this bit returns always 0.
FSOE	5	rw	**Fast Switch Off Enable** Used for fast clock switch-off in Suspend Mode. 0_B Clock switch-off in Suspend Mode via Disable Control Feature (Secure Clock Switch Off) selected 1_B Fast clock switch off in Suspend Mode selected This bit can be written only if SBWE is set during the same write operation.
RMC	[15:8]	rw	**8-Bit Clock Divider Value in RUN Mode** This is a maximum 8-bit divider value for clock f_{FPI}. If RMC is set to 0 the module is disabled.
0	7, 6, [31:16]	r	**Reserved** Read as 0; should be written with 0.

MOD_FDR
Fractional Divider Register **Reset Value: 0000 0000$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DISCLK	**ENHW**	**SUSREQ**	**SUSACK**	**0**		**RESULT**									
rwh	rw	rh	rh	r		rh									

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DM		**SC**		**SM**	**FDIS**	**STEP**									
rw		rw		rw	rw	rw									

Field	Bits	Type	Description
STEP	[9:0]	rw	**Step Value** In Normal Divider Mode, STEP contains the reload value for RESULT. In Fractional Divider Mode, this bit field determines the 10-bit value that is added to RESULT with each input clock cycle.
FDIS	10	rw	**Freeze Disable** This bit controls the freeze function for this module. 0_B Module operates on corrected clock, with reduced modulation jitter 1_B Module operates on uncorrected clock with full modulation jitter
SM	11	rw	**Suspend Mode** SM selects between granted or immediate Suspend Mode. 0_B Granted Suspend Mode selected 1_B Immediate Suspend Mode selected
SC	[13:12]	rw	**Suspend Control** This bit field determines the behavior of the fractional divider in Suspend Mode (bit SUSREQ and SUSACK set). 00_B Clock generation continues. 01_B Clock generation is stopped and the clock output signal is not generated. RESULT is not changed except when writing bit field DM with 01_B or 10_B. 10_B Clock generation is stopped and the clock output signal is not generated. RESULT is loaded with $3FF_H$. 11_B Same as SC = 10_B but signal Reset External Divider is 1 (independently of bit field DM).

Field	Bits	Type	Description
DM	[15:14]	rw	**Divider Mode** This bit fields determines the functionality of the fractional divider block. 00_B Fractional divider is switched off; no output clock is generated. The Reset External Divider signal is 1. RESULT is not updated. 01_B Normal Divider Mode selected. 10_B Fractional Divider Mode selected. 11_B Fractional divider is switched off; no output clock is generated. RESULT is not updated.
RESULT	[25:16]	rh	**Result Value** In Normal Divider Mode, RESULT acts as reload counter (addition +1). In Fractional Divider Mode, this bit field contains the result of the addition RESULT + STEP. If DM is written with 01_B or 10_B, RESULT is loaded with $3FF_H$.
SUSACK	28	rh	**Suspend Mode Acknowledge** 0_B Suspend Mode is not acknowledged. 1_B Suspend Mode is acknowledged. Suspend Mode is entered when SUSACK and SUSREQ are set.
SUSREQ	29	rh	**Suspend Mode Request** 0_B Suspend Mode is not requested. 1_B Suspend Mode is requested. Suspend Mode is entered when SUSREQ and SUSACK are set.
ENHW	30	rw	**Enable Hardware Clock Control** 0_B Bit DISCLK cannot be cleared by a high level of the External Clock Enable input 1_B Bit DISCLK is cleared while the External Clock Enable input is at high level.
DISCLK	31	rwh	**Disable Clock** 0_B Clock generation of f_{MOD} is enabled according to the setting of bit field DM. 1_B Fractional divider is stopped. Signal f_{MOD} becomes inactive. No change except when writing bit field DM.

Field	Bits	Type	Description
0	[27:26]	r	**Reserved** Read as 0; should be written with 0.

3.2 Reset Operation

This section describes the conditions under which the TC1798 will be reset and the reset operation configuration and control.

3.2.1 Overview

The following reset request triggers are available:

- 1 External power-on hardware reset request trigger; $\overline{\text{PORST}}$, (cold reset)
- 2 External System Request reset triggers; $\overline{\text{ESR0}}$, and $\overline{\text{ESR1}}$,(warm reset)
- Watchdog Timer (WDT) reset request trigger, (warm reset)
- Software reset (SW), (warm reset)
- Debug (OCDS) reset request trigger, (warm reset)
- Resets via the JTAG interface
- Flash Tuning Protection (TP) (warm reset)
- JTAG reset (special reset)

Note: The JTAG and OCDS resets are described in the OCDS chapter.

There are two basic types of reset request triggers:

- Trigger sources that do not depend on a clock, such as the $\overline{\text{PORST}}$. This trigger force the device into an asynchronous reset assertion independently of any clock. The activation of an asynchronous reset is asynchronous to the system clock, whereas its de-assertion is synchronized.
- Trigger sources that need a clock in order to be asserted, such as the input signals $\overline{\text{ESR0}}$,$\overline{\text{ESR1}}$, the WDT trigger, TP trigger, or the SW trigger.

Note: A $\overline{\text{PORST}}$ reset should only triggered for power related issue and not for pure functional purpose.

3.2.2 Reset Types

The following summary shows the different reset types.

- Power-on Reset:
  This reset leads to a initialization into a defined state of the complete system. This reset should only be requested on a real power-on event and can not by any non power related event.
  A Power-on Reset also generates a System Reset and an Application Reset.
- System Reset:
  This reset leads to a initialization into a defined state of the complete system without the following parts: reset control, power control.
  A System Reset also generates an Application Reset.
- Debug Reset:
  This reset leads to a initialization into a defined state of the complete debug system.

- Application Reset:
  This reset leads to a initialization into a defined state of the complete application system with the following parts: all peripherals, the CPU and partially the SCU and the flash memory.

3.2.3 Reset Sources Overview

The connection of the reset sources and the activated reset signals/domains are shown in Table 3-5.

Table 3-5 Effects of Resets for Reset Signal Activation

Reset Request Trigger	Application Reset	Debug Reset	System Reset
$\overline{\text{PORST}}$	Activated	Activated	Activated
$\overline{\text{ESR0}}$	Configurable	Not Activated	Configurable
$\overline{\text{ESR1}}$	Configurable	Not Activated	Configurable
WDT	Configurable	Not Activated	Configurable
SW	Configurable	Not Activated	Configurable
OCDS Reset	Not Activated	Activated	Not Activated
CBS_OJCONF.RSTCL0	Activated	Not Activated	Activated
CBS_OJCONF.RSTCL1	Not Activated	Activated	Not Activated
CBS_OJCONF.RSTCL3	Activated	Not Activated	Not Activated

3.2.4 Module Reset Behavior

Table 3-6 lists how the various functions of the TC1798 are affected through a reset depending on the reset type. A “X” means that this block has at least some register/bits that are affected by this reset.

Table 3-6 Effect of Reset on Device Functions

Module / Function	Application Reset	Debug Reset	System Reset	Power-on Reset
CPU Core	X	X	X	X
Peripherals (except SCU)	X	X	X	X
SCU	X	Not affected	X	X

Table 3-6 Effect of Reset on Device Functions (cont'd)

Module / Function		Application Reset	Debug Reset	System Reset	Power-on Reset
On-chip Static RAMs[1]	**OVRAM**	Not affected, reliable	Not affected, reliable	Affected, un-reliable	Affected, un-reliable
	DSPR	Not affected, reliable	Not affected, reliable	Affected, un-reliable	Affected, un-reliable
	DCACHE	Not affected, reliable	Not affected, reliable	Affected, un-reliable	Affected, un-reliable
	PSPR	Not affected, reliable	Not affected, reliable	Affected, un-reliable	Affected, un-reliable
	PRAM	Not affected, reliable	Not affected, reliable	Affected, un-reliable	Affected, un-reliable
	CMEM	Not affected, reliable	Not affected, reliable	Affected, un-reliable	Affected, un-reliable
	ICACHE	Not affected, reliable	Not affected, reliable	Affected, un-reliable	Affected, un-reliable
	LMU	Not affected, reliable	Not affected, reliable	Affected, un-reliable	Affected, un-reliable
Flash Memory		X [2]	Not affected, reliable	X	X
JTAG Interface		Not affected	Not affected	Not affected	Affected
OCDS		Not affected	X	Not affected	X
MCDS		Not affected	X	Not affected	X
Oscillators, PLL		Not affected	Not affected	X	X
Port Pins		X	Not affected	X	X
Pins ESRx		Not affected	Not affected	X	X

1) Reliable here means that also the redundancy is not affected by the reset.

2) Parts of the flash memory block are only reset by a class 0 reset. For more detail see the flash chapter.

3.2.5 General Reset Operation

A reset is generated if an enabled reset request trigger is asserted. Most reset request trigger can configured for the reset type that should initiated by it. No action (disabled) is one possible configuration and can be selected for a reset request trigger by setting the adequate bit field in a Reset Configuration Register to 00_B. The Debug Reset can only

be requested by dedicated reset request triggers and can not be selected via a Reset Configuration Register. For more information see also register RSTCON.

The duration of a reset is defined by two independent counters. One counter for the Power-on, System, and Application Reset types and one separate counter for the Debug Reset. A separate counter for the Debug Reset was implemented to allow a non-intrusive adaptation of the reset length to the debugger needs without modification of the application setting.

3.2.6 Reset State Machine

There is one central Reset State Machine (RSM) controlling the reset generation for the complete device beside the JTAG reset domain.

Note: The JTAG reset domain is controlled by the $\overline{TRST}$ pin.

The RSM is composed of a control block responsible for the operation flow, two counters with a reload register, and a distribution logic that controls the generation of the three dedicated resets.

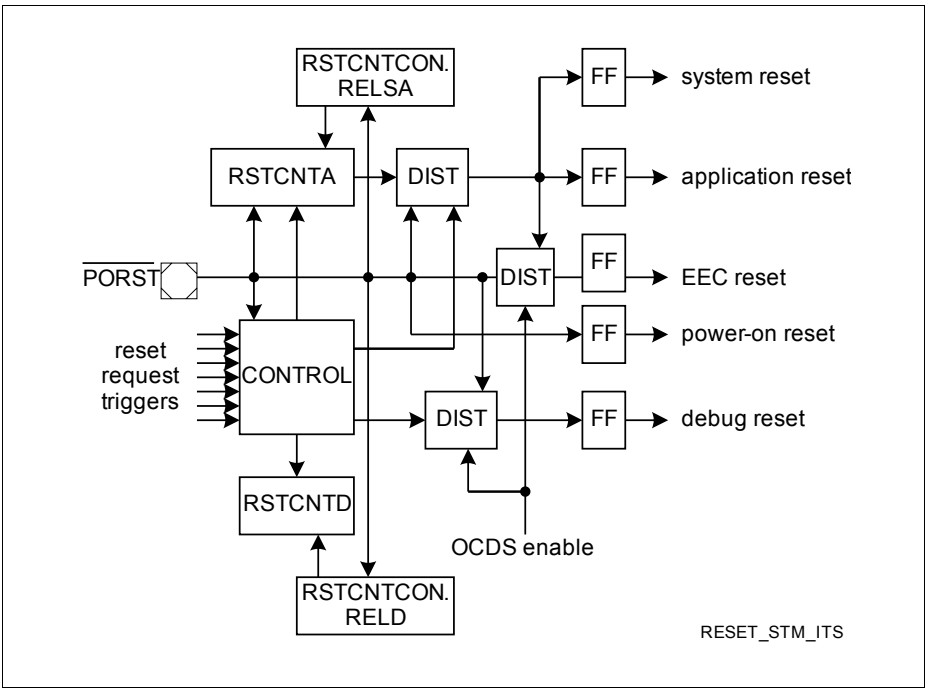


Figure 3-19 Reset State Machine Block Diagram

3.2.7 Reset Counters (RSTCNTA and RSTCNTD)

There are two reset counters implemented. RSTCNTA is the reset counter that controls the reset length for all non debug relevant resets (System Reset and Application Reset). RSTCNTD is the reset counter that controls the reset length for the Debug Reset.

The reset counters can be used for the following purposes:

- First to control the length of the internal resets.
- Second to configure the reset length in a way that the reset outputs via the ESRx pins match with the reset input requirements of external blocks connected with the reset outputs.

A reset counter RSTCNT is an 16-bit counter counting down from the reload value defined by RSTCNTCON.RELx (x = SA or D). The counter is started by the control block as soon as a reset request trigger condition becomes active (for more information see **Table 3-7** and **Table 3-8**). Whether the counter has to be started or not depends on the reset request trigger and whether the counter is already active or not. In case that the counter is inactive, not counting down, it is always started. While the counter is already active it depends on the reset of the new reset request trigger that was asserted anew if the counter is restarted or not. This behavior is summarized in **Table 3-7** and **Table 3-8**.

Table 3-7 Restart of RSTCNTA

Reset Active	New Reset Request			
	Power-on	System	Debug	Application
Power-on Reset	Restart	No Restart	No Restart	No Restart
System	Restart	No Restart	No Restart	No Restart
Application	Restart	Restart	No Restart	No Restart

Table 3-8 Restart of RSTCNTD

Reset Active	New Reset / Reset Type Request			
	Power-on	System	Debug	Application
Debug	Restart	No Restart	No Restart	No Restart

RSTCNTx ensures that a reset request trigger generates a reset of a minimum length which is configurable. But if a reset request trigger is asserted continuously longer than the counter needs for the complete count-down process the reset cannot be deasserted before the reset request trigger is also deasserted. Anyway the counter is not started again, instead the control block informs the distribution logic (DIST) that the reset still has to be asserted until the reset request trigger is deasserted.

The reset state of the control block is implemented such that the RSTCNTA is started and two reset types (System and Application) have to be asserted by the distribution logic.

The reset state of the control block is implemented such that the RSTCNTD is started and the Debug Reset has to be asserted by the distribution logic.

Note: The reset counter should not be configured with a value lower than 20_H due to the implementation.

3.2.8 De-assertion of a Reset

The reset is de-asserted when all of the following conditions are fulfilled.

- The reset counter has expired (reached zero)
- No reset request trigger that is configured to generate the same reset is currently asserted

3.2.8.1 Example1:

Reset request trigger A is asserted and leads to an Application Reset. If the reset request trigger is de-asserted before RSTCNTA reached zero the Application Reset is de-asserted when RSTCNTA reaches zero. If the reset request trigger is de-asserted after RSTCNTA reached zero the Application Reset is de-asserted when the reset request trigger is de-asserted.

3.2.8.2 Example2:

Reset request trigger A is asserted and leads to an Application Reset. Reset request trigger A is de-asserted before RSTCNTA reached zero. Reset request trigger B is asserted after reset request trigger A but before RSTCNTA reaches zero. Reset request trigger B is also configured to result in an Application Reset. If the reset request trigger B is de-asserted before RSTCNTA reached zero the Application Reset is de-asserted when RSTCNTA reaches zero. If the reset request trigger B is de-asserted after RSTCNTA reached zero the Application Reset is de-asserted when the reset request trigger B is de-asserted.

3.2.8.3 Example3:

Reset request trigger A is asserted and leads to a System Reset. Reset request trigger A is de-asserted before RSTCNTA reached zero. Reset request trigger B is asserted after reset request trigger A but before RSTCNTA reaches zero. Reset request trigger B is configured to result in an Application Reset. If the reset request trigger B is de-asserted before RSTCNTA reached zero the System and Application Resets are de-asserted when RSTCNTA reaches zero. If the reset request trigger B is de-asserted after

RSTCNTA reached zero the Application Reset is de-asserted when the reset request trigger B is de-asserted.

3.2.9 Reset Triggers

There are two types of reset triggers for the reset control logic:

- Triggers that lead to a specific reset
- Triggers that lead to a configurable reset

3.2.9.1 Specific Reset Triggers

These triggers lead to a predefined reset if the trigger is asserted. Additionally these triggers can not be enabled / disabled. All specific reset are listed in **Table 3-9**.

Table 3-9 Specific Reset Triggers

Reset Trigger	Reset Type Request
Debug (OCDS from Cerberus)	Debug Reset
Cerberus 0 (CB0)	System Reset
Cerberus 1 (CB1)	Debug Reset
Cerberus 3 (CB3)	Application Reset

3.2.9.2 Configurable Reset Triggers

These triggers lead to a selectable reset if the trigger is asserted. Additionally these triggers can be enabled / disabled. The behavior of the reset triggers action is defined by the configuration of the dedicated bit field for this trigger in register RSTCON.

3.2.10 Debug Specific Behavior

For safety reasons it is required by the debugger that if the OCDS system is disabled a Debug Reset is also asserted every time an Application Reset is asserted.

3.2.11 EEC Reset Specific Behavior

The complete EEC part is reset with the Power-on Reset. For safety reasons it is required by the debugger that if the OCDS system is disabled a EEC reset is also asserted every time an Application Reset is asserted.

3.2.12 Reset Controller Registers

3.2.12.1 Status Registers

After a reset has been executed, the Reset Status registers provide information on the source of the last reset(s). The reset status registers are updated upon each reset cycle. A reset cycle is finished when all resets are de-asserted. Within a reset cycle the status flags are used as sticky flags.

RSTSTAT
Reset Status Register

(050_H) **Reset Value: 0001 0001_H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0										TP	CB3	CB1	CB0	OCDS	PORST
r										rh	rh	rh	rh	rh	rh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0											SW	WDT	0	ESR1	ESR0
r											rh	rh	r	rh	rh

Field	Bits	Type	Description
ESR0	0	rh	**Reset Request Trigger Reset Status for ESR0** 0_B The last reset was not requested by this reset trigger 1_B The last reset was requested by this reset trigger *Note: This bit is set if the ESR0 pin is configured as open drain for output characteristics (IOCR.PC0 = 1101_H or 1110_H) and ESR0 is configured to generate a Reset (RSTCON.ESR0 = 01_B or 10_B) AND a reset is signaled by the ESR0 pin to the outside. That this bit is set under this condition can be avoided by either setting IOCR.PC0 = 1001_H or 1010_H or RSTCON.ESR0 = 00_B.*

Field	Bits	Type	Description
ESR1	1	rh	**Reset Request Trigger Reset Status for ESR1** 0_B The last reset was not requested by this reset trigger 1_B The last reset was requested by this reset trigger *Note: This bit is set if the ESR1 pin is configured as open drain for output characteristics (IOCR.PC1 = 1101_H or 1110_H) and ESR1 is configured to generate a Reset (RSTCON.ESR1 = 01_B or 10_B) AND a reset is signaled by the ESR1 pin to the outside. That this bit is set under this condition can be avoided by either setting IOCR.PC1 = 1001_H or 1010_H or RSTCON.ESR1 = 00_B.*
WDT	3	rh	**Reset Request Trigger Reset Status for WDT** 0_B The last reset was not requested by this reset trigger 1_B The last reset was requested by this reset trigger
SW	4	rh	**Reset Request Trigger Reset Status for SW** 0_B The last reset was not requested by this reset trigger 1_B The last reset was requested by this reset trigger
PORST	16	rh	**Reset Request Trigger Reset Status for PORST** 0_B The last reset was not requested by this reset trigger 1_B The last reset was requested by this reset trigger This bit is also set if the bits CB0, CB1, and CB3 are set in parallel.
OCDS	17	rh	**Reset Request Trigger Reset Status for OCDS** 0_B The last reset was not requested by this reset trigger 1_B The last reset was requested by this reset trigger

Field	Bits	Type	Description
CB0	18	rh	**Reset Request Trigger Reset Status for Cerberus System Reset** 0_B The last reset was not requested by this reset trigger 1_B The last reset was requested by this reset trigger
CB1	19	rh	**Reset Request Trigger Reset Status for Cerberus Debug Reset** 0_B The last reset was not requested by this reset trigger 1_B The last reset was requested by this reset trigger
CB3	20	rh	**Reset Request Trigger Reset Status for Cerberus Application Reset** 0_B The last reset was not requested by this reset trigger 1_B The last reset was requested by this reset trigger
TP	21	rh	**Reset Request Trigger Reset Status for TP** 0_B The last reset was not requested by this reset trigger 1_B The last reset was requested by this reset trigger
0	2, [15:5], [31:22]	r	**Reserved** Read as 0; should be written with 0.

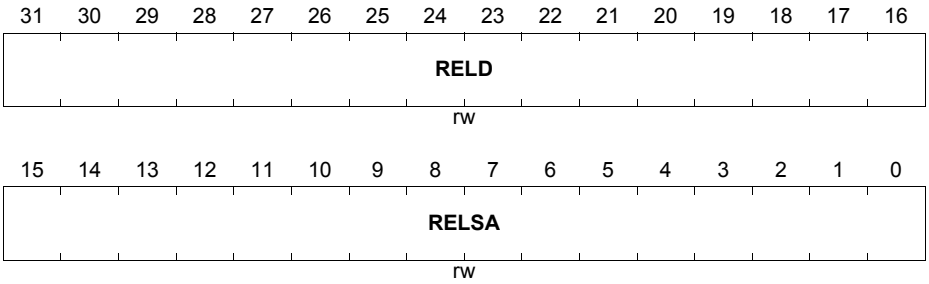
3.2.12.2 Configuration Registers

Reset Counter Control Register

This register controls the reset length settings for the three resets.

RSTCNTCON
Reset Counter Control Register

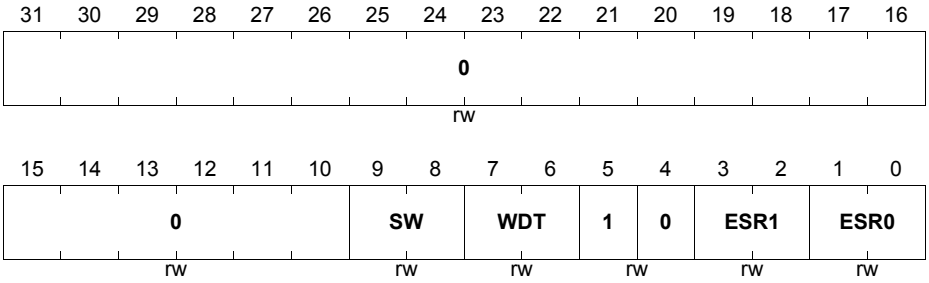
(054$_H$) Reset Value: 05BE 05BE$_H$



Field	Bits	Type	Description
RELSA	[15:0]	rw	**System Application Reset Counter Reload Value** This bit field defines the reload value of RSTCNTA. This value is always used when counter RSTCNTA is started.
RELD	[31:16]	rw	**Debug 1 Reset Counter Reload Value** This bit field defines the reload value of RSTCNTD. This value is always used when counter RSTCNTD is started.

RSTCON
Reset Configuration Register

(058$_H$) Reset Value: 0000 02A2$_H$

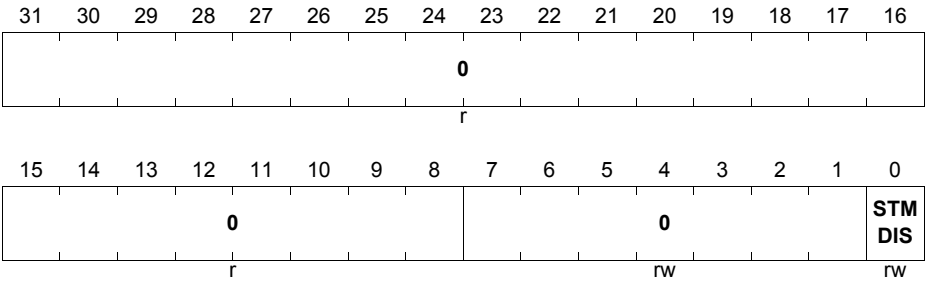


Field	Bits	Type	Description
ESR0	[1:0]	rw	**ESR0 Reset Request Trigger Reset Configuration** This bit field defines which reset is generated by a reset request trigger from ESR0 reset. 00_B No reset is generated for a trigger of ESR0 01_B A System Reset is generated for a trigger of ESR0 reset 10_B An Application Reset is generated for a trigger of ESR0 reset 11_B Reserved, do not use this combination
ESR1	[3:2]	rw	**ESR1 Reset Request Trigger Reset Configuration** This bit field defines which reset is generated by a reset request trigger from ESR1 reset. 00_B No reset is generated for a trigger of ESR1 01_B A System Reset is generated for a trigger of ESR1 reset 10_B An Application Reset is generated for a trigger of ESR1 reset 11_B Reserved, do not use this combination
WDT	[7:6]	rw	**WDT Reset Request Trigger Reset Configuration** This bit field defines which reset is generated by a reset request trigger from WDT reset. 00_B No reset is generated for a trigger of WDT 01_B A System Reset is generated for a trigger of WDT reset 10_B An Application Reset is generated for a trigger of WDT reset 11_B Reserved, do not use this combination
SW	[9:8]	rw	**SW Reset Request Trigger Reset Configuration** This bit field defines which reset is generated by a reset request trigger from software reset. 00_B No reset is generated for a trigger of software reset 01_B A System Reset is generated for a trigger of Software reset 10_B An Application Reset is generated for a trigger of Software reset 11_B Reserved, do not use this combination

Field	Bits	Type	Description
1	5	rw	**Reserved** Should be written with 1.
0	4, [31:10]	rw	**Reserved** Should be written with 0.

ARSTDIS
Application Reset Disable Register

(05C$_H$) **Reset Value: 0000 0000$_H$**



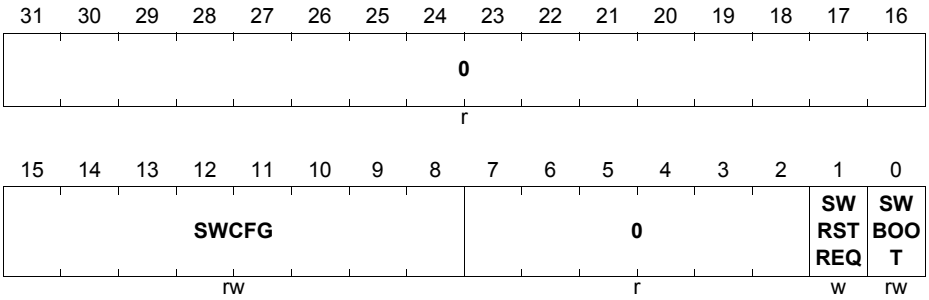
Field	Bits	Type	Description
STMDIS	0	rw	**STM Disable Reset** This bit field defines if an Application Reset leads to an reset for the STM. 0_B An Application Reset resets the STM 1_B An Application Reset has no effect for the STM
0	[7:1]	rw	**Reserved** Should be written with 0.
0	[31:8]	r	**Reserved** Read as 0; should be written with 0.

SW Reset Configuration Register

This register controls the SW Reset operation.

SWRSTCON
Software Reset Configuration Register

(060$_H$) Reset Value: 0000 0000$_H$



Field	Bits	Type	Description
SWBOOT	0	rw	**Software Boot Configuration Selection** 0_B Bit field STSTAT.HWCFG is not updated with the content of SWCFG upon an Application Reset 1_B Bit field STSTAT.HWCFG is updated with the content of SWCFG upon an Application Reset
SWRSTREQ	1	w	**Software Reset Request** 0_B No SW Reset is requested 1_B A SW Reset request trigger is generated This bit is automatically cleared and read always as zero.
SWCFG	[15:8]	rw	**Software Boot Configuration** A software boot configuration different from the external applied hardware configuration can be specified with these bits. The configuration encoding is equal to the HWCFG encoding in register STSTAT.
0	[7:2], [31:16]	r	**Reserved** Read as 0; should be written with 0.

3.3 External Interface

The SCU provides interface pads for system purpose. Various functions are covered by these pins. Due to the different tasks some of the pads can not be shared with other functions but most of them can. The following functions are covered by the SCU controlled pads:

- Reset request triggers
- Reset indication
- Trap request triggers
- Interrupt request triggers
- Non SCU module triggers

The first three points are covered by the ESR pads and the last two points by the ERU pads.

3.3.1 External Service Requests ($\overline{\text{ESRx}}$)

The ESR pins can be used to trigger either a reset, a trap (NMI), as reset output, or as data pin.

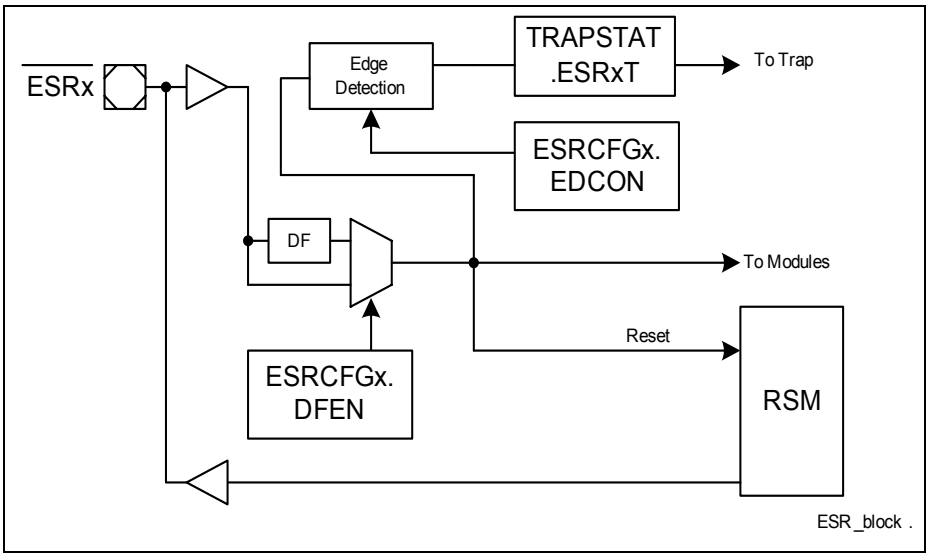


Figure 3-20 ESR Operation

3.3.1.1 $\overline{\text{ESRx}}$ as Reset Request Trigger

An $\overline{\text{ESR0}}$/$\overline{\text{ESR1}}$ reset request trigger leads to a System or Application Reset. The type of the reset can be configured via RSTCON.ESRx.

In order to be safely recognized $\overline{\text{ESR0}}$/$\overline{\text{ESR1}}$ has to be active for a minimum of 2 f_{FPI} clock cycles.

The input signal $\overline{\text{ESR0}}$/$\overline{\text{ESR1}}$ have digital filters (3-stage median filters), that can be disabled.

A 3-stage median filter samples with f_{FPI} three consecutive clock cycles and the output is defined by the majority of the three sampled values.

The behavior of all three $\overline{\text{ESR0}}$/$\overline{\text{ESR1}}$ pins can be configured by programming the registers ESRCFGn. The pad control functionality can be configured independently for each pin, comprising:

- A selection of the driver type (open-drain or push-pull)
- An enable function for the output driver (input and/or output capability)
- An enable function for the pull-up/down resistance

3.3.1.2 $\overline{\text{ESRx}}$ as Reset Output

The external pins $\overline{\text{ESR0}}$/$\overline{\text{ESR1}}$ can serve as an reset output (open drain) for the Application Reset.

Note: The reset output is only asserted for the duration the reset counter RSTCNTA is active. During a possible reset extension the reset output is not longer asserted.

If the pin $\overline{\text{ESR0}}$/$\overline{\text{ESR1}}$ is enabled as reset output and the input level is low while the output stage is disabled (indicating that it is still driven low externally), the reset circuitry holds the chip in reset until a high level is detected on $\overline{\text{ESR0}}$/$\overline{\text{ESR1}}$. The internal output stage drives a low level during reset only while RSTCNTA is active. It deactivates the output stage when the time defined by RSTCNTCON.RELSA has passed.

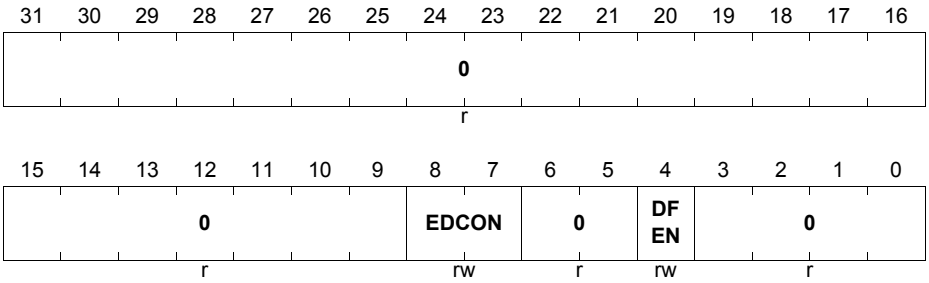
3.3.1.3 ESR Registers

ESRCFG0
ESR0 Configuration Register

(070_H) **Reset Value: $0000\ 0110_H$**

ESRCFG1
ESR1 Configuration Register

(074_H) **Reset Value: $0000\ 0090_H$**



Field	Bits	Type	Description
DFEN	4	rw	**Digital Filter Enable** This bit defines if the 3-stage median filter of the ESR0 is used or bypassed. 0_B The filter is bypassed 1_B The filter is used
EDCON	[8:7]	rw	**Edge Detection Control** This bit field defines the edges that lead to an ESR0 trigger of the synchronous path. 00_B No trigger is generated 01_B A trigger is generated upon a rising edge 10_B A trigger is generated upon a falling edge 11_B A trigger is generated upon a rising OR falling edge
0	[3:0], [6:5], [31:9]	r	**Reserved** Read as 0; should be written with 0.

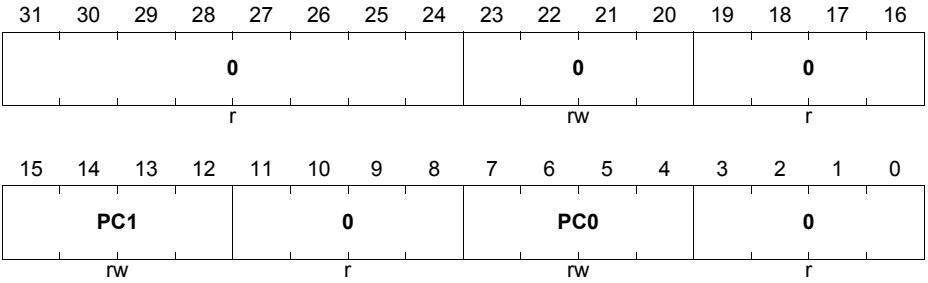
Input/Output Control Registers

The input/output control registers select the digital output and input driver functionality and characteristics of the pin. Direction (input or output), pull-up or pull-down devices for

inputs, and push-pull or open-drain functionality for outputs can be selected by the corresponding bit fields PCx (x = 0-1).

IOCR

Input/Output Control Register ($0A0_H$) Reset Value: $0020\ 10E0_H$



Field	Bits	Type	Description
PC0	[7:4]	rw	**Control for $\overline{\text{ESR0}}$ Pin** This bit field defines the $\overline{\text{ESR0}}$ pin functionality according to the coding table (see **Table 3-10**).
PC1	[15:12]	rw	**Control for $\overline{\text{ESR1}}$ Pin** This bit field defines the $\overline{\text{ESR1}}$ pin functionality according to the coding table (see **Table 3-11**).
0	[23:20]	rw	**Reserved** Have to be written with 0010_B.
0	[3:0], [11:8], [19:16], [31:24]	r	**Reserved** Read as 0; should be written with 0.

Pad Control Coding

Table 3-10 describes the coding of the PC0 bit field that determine the port line functionality.

Table 3-10 PC0 Coding

PC0[3:0]	I/O	Output Characteristics	Selected Pull-up/Pull-down/ Selected Output Function
$0X00_B$	Input is active and not inverted; Output is inactive		No input pull device connected
$0X01_B$			Input pull-down device connected
$0X10_B$			Input pull-up device connected
$0X11_B$			No input pull device connected
1000_B	Input is active and not inverted; Output is active	Push-pull	General-purpose Output
1001_B			Output drives a 0 for System Resets, a weak pull-up is active otherwise
1010_B			Output drives a 0 for Application Resets, a weak pull-up is active otherwise
1011_B			Reserved, do not use this combination
1100_B	the input is active and not inverted; Output is active	Open-drain	General-purpose Output
1101_B			Output drives a 0 for System Resets, a weak pull-up is active otherwise
1110_B			Output drives a 0 for Application Resets, a weak pull-up is active otherwise
1111_B			Reserved, do not use this combination

Pad Control Coding

Table 3-11 describes the coding of the PC1 bit field that determine the port line functionality.

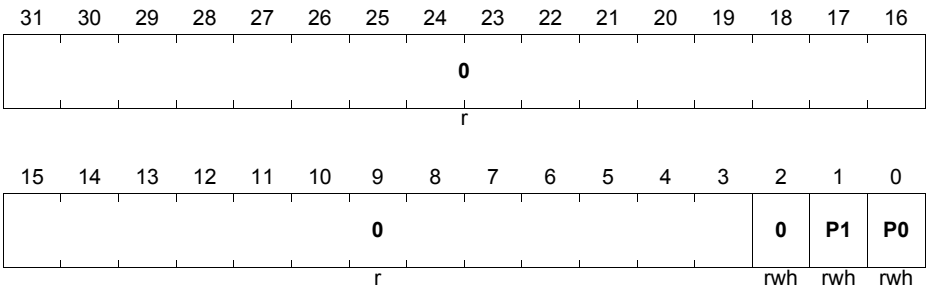
Table 3-11 PC1 Coding

PC1[3:0]	I/O	Output Characteristics	Selected Pull-up/Pull-down/ Selected Output Function
$0X00_B$	Input is active and not inverted; Output is inactive		No input pull device connected
$0X01_B$			Input pull-down device connected
$0X10_B$			Input pull-up device connected
$0X11_B$			No input pull device connected
1000_B	Input is active and not inverted; Output is active	Push-pull	General-purpose Output
1001_B			Output drives a 0 for System Resets, a 'Z' otherwise
1010_B			Output drives a 0 for Application Resets, a 'Z' otherwise
1011_B			Reserved, do not use this combination
1100_B	the input is active and not inverted; Output is active	Open-drain	General-purpose Output
1101_B			Output drives a 0 for System Resets, a 'Z' otherwise
1110_B			Output drives a 0 for Application Resets, a 'Z' otherwise
1111_B			Reserved, do not use this combination

Output Register

The output register determines the value of a GPIO pin when it is selected by IOCR as output. Writing a 0 to a OUT.Px (x = 0-1) bit position delivers a low level at the corresponding output pin. A high level is output when the corresponding bit is written with a 1. Note that each single bit or group of bits of OUT.Px can be set/cleared by writing appropriate values into the output modification register OMR.

OUT
Output Register **($0A4_H$)** **Reset Value: $0000\ 0000_H$**

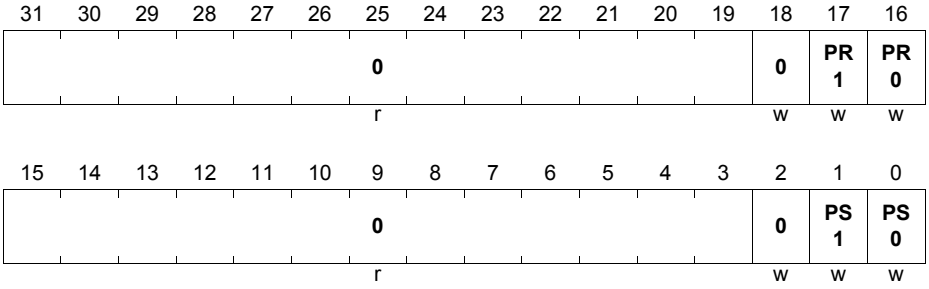


Field	Bits	Type	Description
Px **(x = 0-1)**	x	rwh	**Output Bit x** This bit determines the level at the output pin $\overline{ESR}$x if the output is selected as GPIO output. 0_B The output level of $\overline{ESR}$x is 0 1_B The output level of $\overline{ESR}$x is 1 Px can also be set/cleared by control bits of the OMR register.
0	2	rwh	**Reserved** Have to be written with 0.
0	[31:3]	r	**Reserved** Read as 0; should be written with 0.

Output Modification Register

The output modification register contains control bits that make it possible to individually set, clear, or toggle the logic state of a single pad by manipulating the output register.

OMR
Output Modification Register **($0A8_H$)** **Reset Value: $0000\ 0000_H$**



Field	Bits	Type	Description
PSx (x = 0-1)	x	w	**Set Bit x** Setting this bit will set or toggle the corresponding bit in the output register OUT. The function of this bit is shown in **Table 3-12**.
PRx (x = 0-1)	x + 16	w	**Clear Bit x** Setting this bit will clear or toggle the corresponding bit in the port output register OUT. The function of this bit is shown in **Table 3-12**.
0	2, 18	w	**Reserved** Read as 0; have to be written with 0.
0	[15:3], [31:19]	r	**Reserved** Read as 0; should be written with 0.

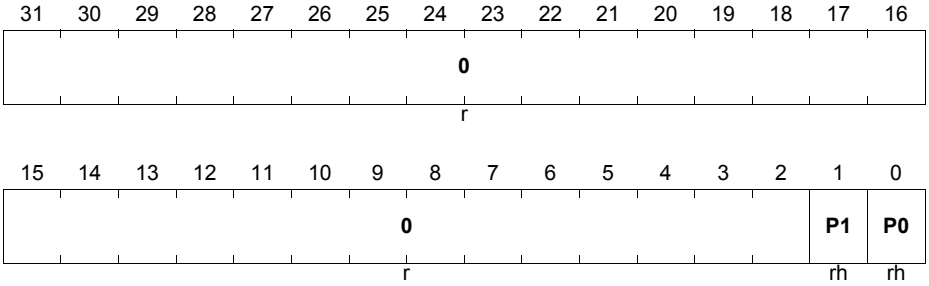
Table 3-12 Function of the Bits PRx and PSx

PRx	PSx	Function
0	0	Bit OUT.Px is not changed
0	1	Bit OUT.Px is set
1	0	Bit OUT.Px is cleared
1	1	Bit OUT.Px is toggled

Input Register

The logic level of a GPIO pin can be read via the read-only port input register IN. Reading the IN register always returns the current logical value at the GPIO pin independently whether the pin is selected as input or output.

IN
Input Register **($0AC_H$)** **Reset Value: $0000\ 000X_H$**



Field	Bits	Type	Description
Px **(x = 0-1)**	x	rh	**Input Bit x** This bit indicates the level at the input pin $\overline{ESR}$x. 0_B The input level of $\overline{ESR}$x is 0 1_B The input level of $\overline{ESR}$x is 1
0	[31:2]	r	**Reserved** Read as 0.

3.3.2 External Request Unit (ERU)

The External Request Unit (ERU) is a versatile event and pattern detection unit. Its major task is the **generation of interrupts based on selectable trigger events at different inputs**, e.g. to generate external interrupt requests if an edge occurs at an input pin. The detected events can also be used by other modules to trigger or to gate module-specific actions.

3.3.2.1 Introduction

The ERU of the TC1798 can be split in three main functional parts:

- 4 independent **Input Channels x** for input selection and conditioning of trigger or gating functions
- Event distribution: A **Connecting Matrix** defines the events of the Input Channel x that lead to a reaction of an Output Channel y.
- 4 independent **Output Channels y** for combination of events, definition of their effects and distribution to the system (interrupt generation, ...)

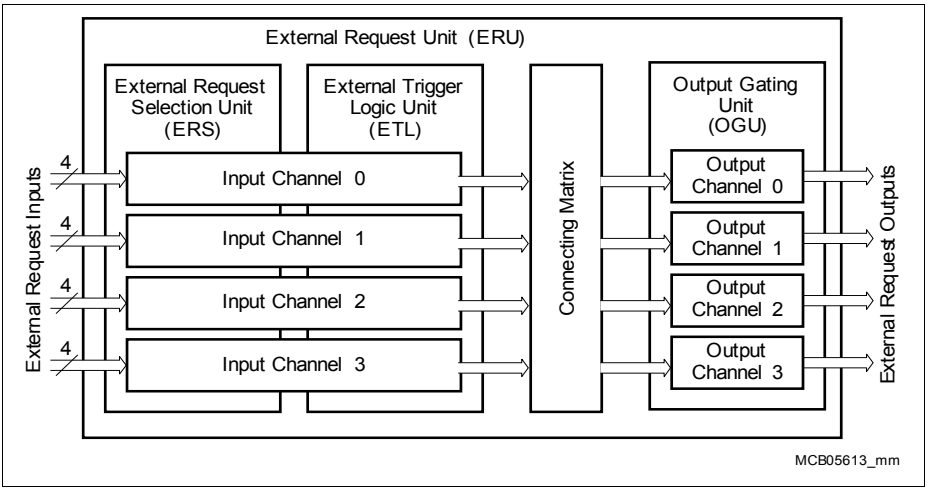


Figure 3-21 External Request Unit Overview

These tasks are handled by the following building blocks:

- An **External Request Select Unit (ERSx)** per Input Channel allows the selection of one input vector out of the 4 possible inputs available.
- An **Event Trigger Logic (ETLx)** per Input Channel allows the definition of the transition (edge selection, or by software) that lead to a trigger event and can also store this status. Here, the input levels of the selected signals are translated into

events (event detected = event flag becomes set, independent of the polarity of the original input signals).

- The **Connecting Matrix** distributes the events and status flags generated by the Input Channels to the Output Channels.
- An **Output Gating Unit (OGUy)** per Output Channel that combines the available trigger events and status information from the Input Channels. An event of one Input Channel can lead to reactions of several Output Channels, or also events of several Input Channels can be combined to a reaction of one Output Channel (pattern detection).
  Different types of reactions are possible, e.g. interrupt generation (based on signals ERU_IOUTy).

3.3.2.2 ERU Pin Connections

Figure 3-22 shows the ERU input connections.

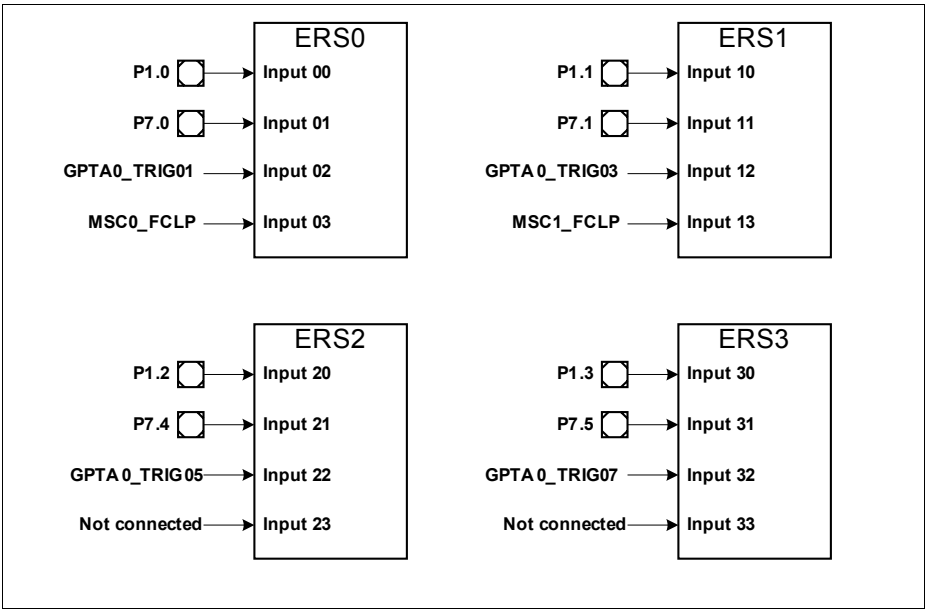


Figure 3-22 ERU Inputs Overview

The inputs to the ERU can be selected from a large number of input signals. While some of the inputs come directly from a pin, other inputs use signals from various peripheral modules.
Usually, such signals would be selected for an ERU function when the input function to the other module is not used otherwise, or the module is not used at all. However, it is also possible to select a input which is actually needed in the other module, and to use it also in the ERU to provide for certain trigger functions, eventually combined with other signals (e.g. to generate an interrupt trigger in case a start of frame is detected at a selected communication).

3.3.2.3 External Request Select Unit (ERS)

Each ERS combines four inputs to the one input signal of the respective input channel. Figure 3-23 shows the structure of this block.

In addition to the direct choice of either input Ax or Bx or their inverted values, the possible logical combinations for two selected inputs are a logical AND or a logical OR.

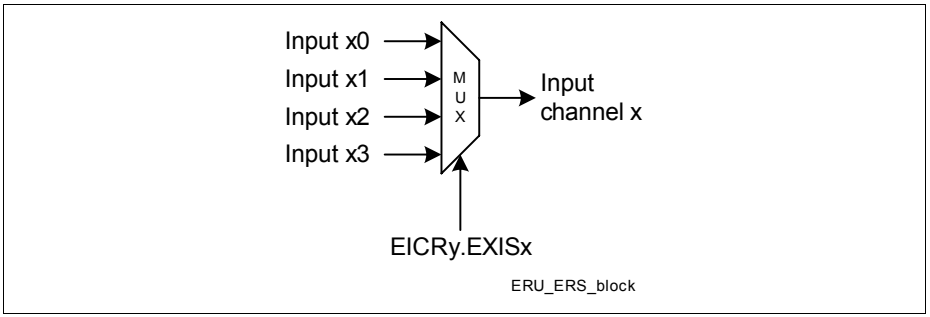


Figure 3-23 External Request Select Unit Overview

The ERS unit for channel x is controlled via bit field ERCIy.EXISx.

3.3.2.4 Event Trigger Logic (ETL)

For each Input Channel x, an event trigger logic ETLx derives a trigger event and a status from the input channel x delivered by the associated ERSx unit. Each ETLx is based on an edge detection block, where the detection of a rising or a falling edge can be individually enabled. Both edges lead to a trigger event if both enable bits are set (e.g. to handle a toggling input).
Each pair of the four ETL units has an associated EICRy register, that controls all options of an ETL (the register also holds control bits for the associated ERS unit pair, e.g. EICR0 to control ESR0 and ESR1 plus and ETL0 and ETL1).

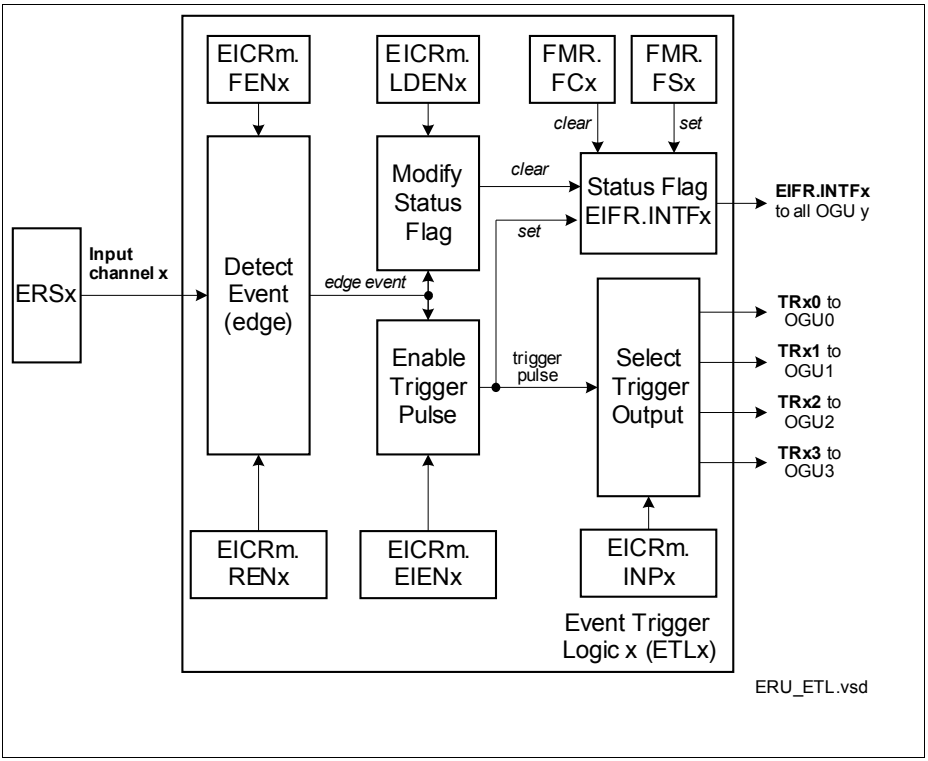


Figure 3-24 Event Trigger Logic Overview

When the selected event (edge) is detected, the status flag EIFR.INTFx becomes set. the status flag is cleared automatically if the “opposite” event is detected if enabled so via bit EICRy.LDENx = 1. For example, if only the falling edge detection is enabled to set the status flag, it is cleared when the rising edge is detected. In this mode, it can be used for pattern detection where the actual status of the input is important (enabling both edge detections is not useful in this mode).
The output of the status flag is connected to all following Output Gating Units (OGUz) in parallel (see **Figure 3-25**) to provide **pattern detection capability of all OGUz** units based on different or the same status flags.

In addition to the modification of the status flag, a trigger pulse output TRxz of ETLx can be enabled (by bit EICRy.EIENx) and selected to **trigger actions in one of the OGUz** units. The target OGUz for the trigger is selected by bit field EICRy.INPx.
The trigger becomes active when the selected edge event is detected, independently from the status flag EIFR.INTFx.

3.3.2.5 Connecting Matrix

The connecting matrix distributes the trigger signals (TRxy) and status signals (EIFR.INPFx) from the different ETLx units between the OGUy units. **Figure 3-25** provides a complete overview of the connections between the ETLx and the OGUz units.

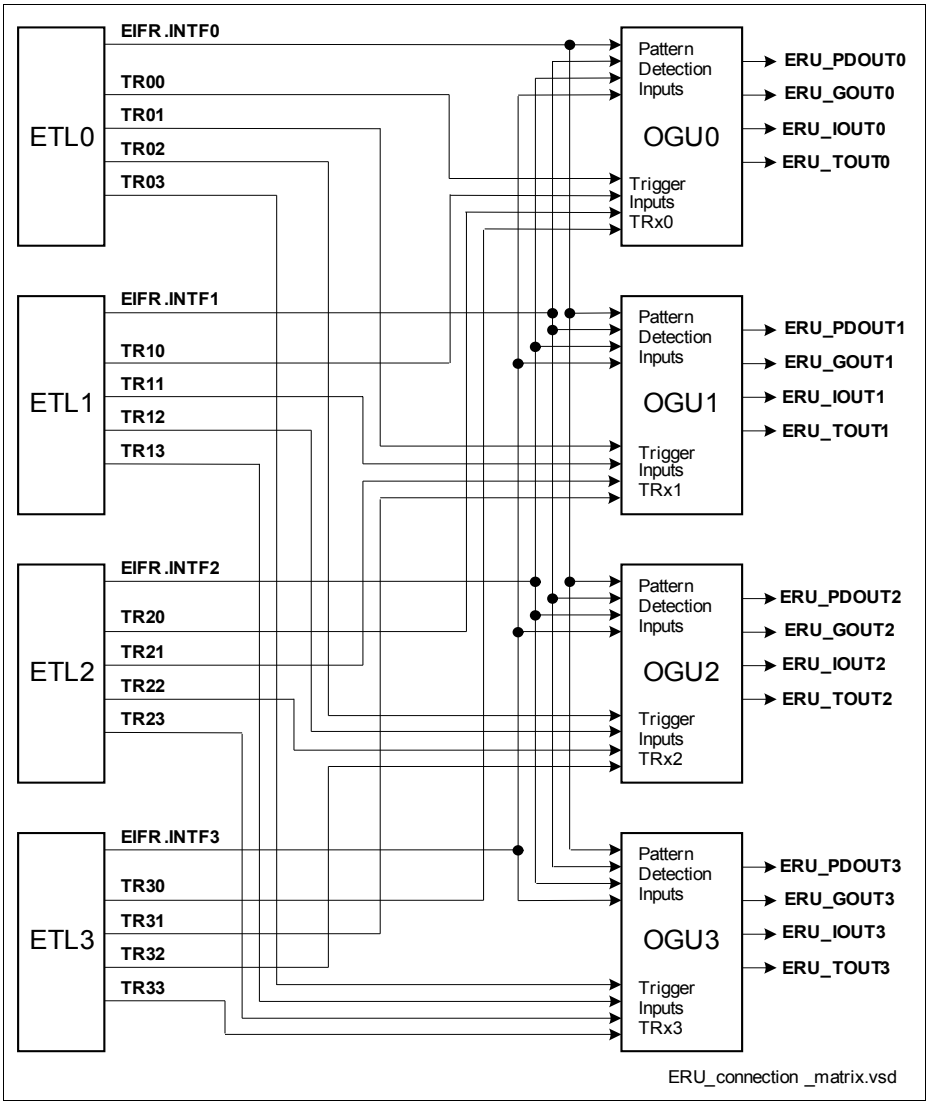


Figure 3-25 Connecting Matrix between ETLx and OGUy

3.3.2.6 Output Gating Unit (OGU)

Each OGUy unit combines the available trigger events and status flags from the Input Channels and distributes the results to the system. **Figure 3-26** illustrates the logic blocks within an OGUy unit. All functions of an OGUy unit are controlled by the associated IGCRm registers, one for each pair of output channels e.g. IGCR1 for OGU2 and OGU3. The function of an OGUy unit can be split into two parts:

- **Trigger combination**:
  All trigger signals TRxy from the Input Channels that are enabled and directed to OGUy and a pattern change event (if enabled) are logically OR-combined.
- **Pattern detection**:
  The status flags EIFR.INTFx of the Input Channels can be enabled to take part in the pattern detection. A pattern match is detected while all enabled status flags are set.

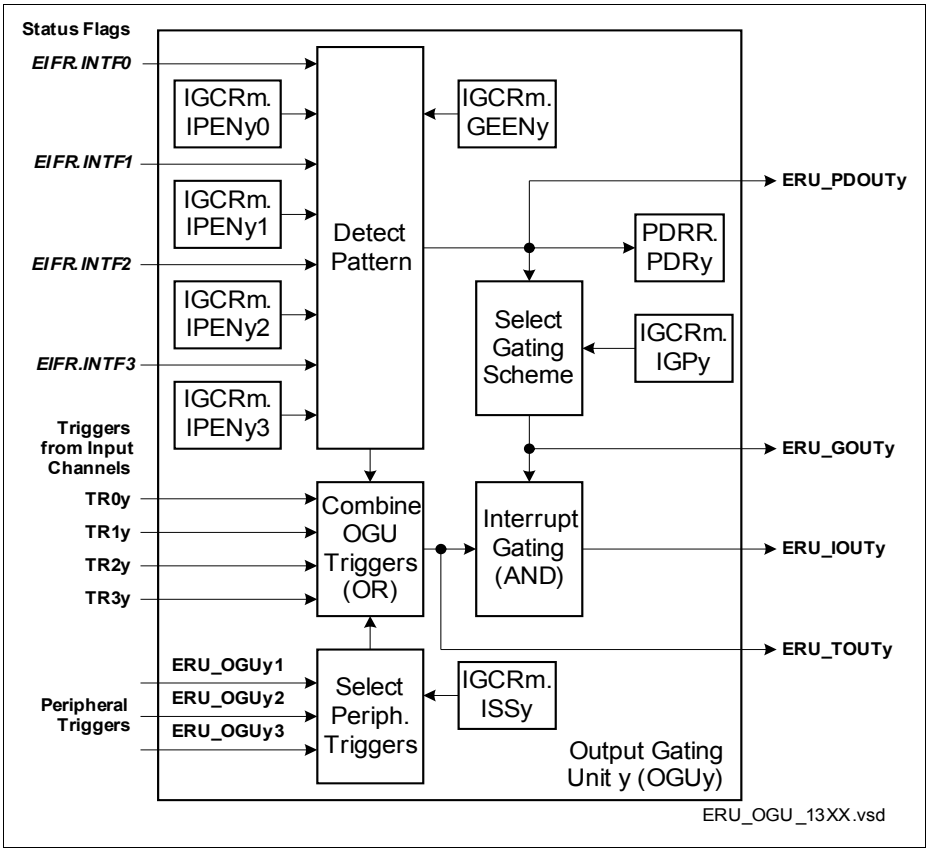


Figure 3-26 Output Gating Unit for Output Channel y

Each OGUy units generates 4 output signals that are distributed to the system.

- **ERU_PDOUTy** to directly output the pattern match information for gating purposes in other modules (pattern match = 1).
- **ERU_GOUTy** to output the pattern match or pattern miss information (inverted pattern match), or a permanent 0 or 1 under software control for gating purposes in other modules.
- **ERU_TOUTy** as combination of a peripheral trigger, a pattern detection result change event, or the ETLx trigger outputs TRxy to trigger actions in other modules.
- **ERU_IOUTy** as gated trigger output (ERU_GOUTy logical AND-combined with ERU_TOUTy) to trigger interrupts (e.g. the interrupt generation can be gated to allow interrupt activation during a certain time window).

Trigger Combination

The trigger combination logically OR-combines different trigger inputs to form a common trigger ERU_TOUTy. Possible trigger inputs are:

- In each ETLx unit of the **Input Channels**, the trigger output TRxy can be enabled and the trigger event can be directed to one of the OGUy units.
- One out of three **peripheral trigger** signals per OGUy can be selected as additional trigger source. These peripheral triggers are generated by on-chip peripheral modules, such as capture/compare or timer units. The selection is done by bit field EXOCONy.ISS.
- In the case that at least one **pattern detection** input is enabled (IGCRm.IPENxy) and a change of the pattern detection result from pattern match to pattern miss (or vice-versa) is detected, a trigger event is generated to indicate a pattern detection result event (if enabled by IGCRm.GEENy).

The trigger combination offers the possibility to program different trigger criteria for several input signals (independently for each Input Channel) or peripheral signals, and to combine their effects to a single output, e.g. to generate an interrupt or to start e.g. an ADC conversion. This combination capability allows the generation of an interrupt per OGU that can be triggered by several inputs (multitude of request sources -> one reaction).

The following table describes the peripheral trigger connections for the OGUy stages. The selection is defined by the bit fields ISS in registers **IGCR0** (for OGU0 and OGU1) and **IGCR1** (for OGU2 and OGU3).

Table 3-13 OGUy Peripheral Trigger Connections in TC1798

Input	from/to Module	I/O to OGUy	Can be used to/as
OGU0 Inputs			
ERU_ OGU01	CCU60_SR1	I	peripheral triggers for OGU0
ERU_ OGU02	Reserved	I	
ERU_ OGU03	Reserved	I	
OGU1 Inputs			

Table 3-13 OGUy Peripheral Trigger Connections in TC1798 (cont'd)

Input	from/to Module	I/O to OGUy	Can be used to/as
ERU_ OGU11	CCU61_SR1	I	peripheral triggers for OGU1
ERU_ OGU12	Reserved	I	
ERU_ OGU13	Reserved	I	
OGU2 Inputs			
ERU_ OGU21	CCU62_SR1	I	peripheral triggers for OGU2
ERU_ OGU22	Reserved	I	
ERU_ OGU23	Reserved	I	
OGU3 Inputs			
ERU_ OGU31	CCU63_SR1	I	peripheral triggers for OGU3
ERU_ OGU32	Reserved	I	
ERU_ OGU33	Reserved	I	

Pattern Detection

The pattern detection logic allows the combination of the status flags of all ETLx units. Each status flag can be individually included or excluded from the pattern detection for each OGUy, via control bits IGCRm.IPENxy. The pattern detection block outputs the following pattern detection results:

- **Pattern match** (PDRR.PDRy = 1 and ERU_PDOUTy = 1):
  A pattern match is indicated while all status flags that are included in the pattern detection are 1.
- **Pattern miss** (PDRR.PDRy = 0 and ERU_PDOUTy = 0):
  A pattern miss is indicated while at least one of the status flags that are included in the pattern detection is 0.

In addition, the pattern detection can deliver a trigger event if the pattern detection result changes from match to miss or vice-versa (if enabled by IGCRm.GEENy = 1). The pattern result change event is logically OR-combined with the other enabled trigger events to support interrupt generation or to trigger other module functions (e.g. in an ADC). The event is indicated when the pattern detection result changes and PDRR.PDRy becomes updated.

The interrupt generation in the OGUy is based on the trigger ERU_TOUTy that can be gated (masked) with the pattern detection result ERU_PDOUTy. This allows an automatic and reproducible generation of interrupts during a certain time window, where the request event is elaborated by the trigger combination block and the time window information (gating) is given by the pattern detection. For example, interrupts can be issued on a regular time base while a combination of input signals occurs (pattern detection based on ETLx status bits).

A programmable gating scheme introduces flexibility to adapt to application requirements and allows the generation of interrupt requests ERU_IOUTy under different conditions:

- **Pattern match** (IGCRm.IGPy = 10_B):
  An interrupt request is issued when a trigger event occurs while the pattern detection shows a pattern match.
- **Pattern miss** (IGCRm.IGPy = 11_B):
  An interrupt request is issued when the trigger event occurs while the pattern detection shows a pattern miss.
- **Independent** of pattern detection (IGCRm.IGPy = 01_B):
  In this mode, each occurring trigger event leads to an interrupt request. The pattern detection output can be used independently from the trigger combination for gating purposes of other peripherals (independent use of ERU_TOUTy and ERU_PDOUTy with interrupt requests on trigger events).
- **No interrupts** (IGCRm.IGPy = 00_B, default setting)
  In this mode, an occurring trigger event does not lead to an interrupt request. The pattern detection output can be used independently from the trigger combination for gating purposes of other peripherals (independent use of ERU_TOUTy and ERU_PDOUTy without interrupt requests on trigger events).

3.3.2.7 ERU Output Connections

This section describes the connections of the ERU output signals for gating or triggering other module functions, as well as the connections to the interrupt control registers.

Table 3-14 ERU Output Connections in TC1798

Output	from/to Module	I/O to OGUy	Can be used to/as
OGU0 Outputs			
ERU_ PDOUT0	ERAY input STPW0	O	pattern detection output
ERU_ GOUT0	not connected	O	gated pattern detection output
ERU_ TOUT0	not connected	O	trigger output
ERU_ IOUT0	**Interrupt Generation** DMA channel 00 DMA channel 04	O	interrupt output
OGU1 Outputs			
ERU_ PDOUT1	ERAY input STPW1	O	pattern detection output
ERU_ GOUT1	not connected	O	gated pattern detection output
ERU_ TOUT1	not connected	O	trigger output
ERU_ IOUT1	**Interrupt Generation** DMA channel 01 DMA channel 05 GPTA0 input INT1 GPTA1 input INT1 LTCA2 input INT1	O	interrupt output
OGU2 Outputs			
ERU_ PDOUT2	ERAY input STPW2 ADC gating input FADC input FADC_GSC	O	pattern detection output
ERU_ GOUT2	not connected	O	gated pattern detection output
ERU_ TOUT2	not connected	O	trigger output

Table 3-14 ERU Output Connections in TC1798 (cont'd)

Output	from/to Module	I/O to OGUy	Can be used to/as
ERU_ IOUT2	**Interrupt Generation** DMA channel 02 DMA channel 06 ADC trigger input FADC input FADC_TSC GPTA0 input INT2 GPTA1 input INT2 LTCA2 input INT2	O	interrupt output
OGU3 Outputs			
ERU_ PDOUT3	ERAY input STPW3 ADC gating input FADC input FADC_GSD	O	pattern detection output
ERU_ GOUT3	not connected	O	gated pattern detection output
ERU_ TOUT3	not connected	O	trigger output
ERU_ IOUT3	**Interrupt Generation** DMA channel 03 DMA channel 07 ADC trigger input FADC input FADC_TSD GPTA0 input INT3 GPTA1 input INT3 LTCA2 input INT3	O	interrupt output

3.3.2.8 External Request Unit Registers

The External Input Channel Register EICR0 and EICR1 for the external input channels 0 to 3 contain bits to configure the external request selection ERS and the event trigger logic ETL.

EICR0

External Input Channel Register 0 (080_H) **Reset Value: $0000\ 0000_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0		**INP1**		**EI EN1**	**LD EN1**	**R EN1**	**F EN1**	**0**		**EXIS1**		**0**			
r		rw		rw	rw	rw	rw	r		rw		r			

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0		**INP0**		**EI EN0**	**LD EN0**	**R EN0**	**F EN0**	**0**		**EXIS0**		**0**			
r		rw		rw	rw	rw	rw	r		rw		r			

Field	Bits	Type	Description
EXIS0	[5:4]	rw	**External Input Selection 0** This bit field determines which input line is selected for Input Channel 0. 00_B Input 00 is selected 01_B Input 01 is selected 10_B Input 02 is selected 11_B Input 03 is selected
FEN0	8	rw	**Falling Edge Enable 0** This bit determines if the falling edge of Input Channel 0 is used to set bit INTF0. 0_B The falling edge is not used 1_B The detection of a falling edge of Input Channel 0 generates a trigger event (INTF0 becomes set)
REN0	9	rw	**Rising Edge Enable 0** This bit determines if the rising edge of Input Channel 0 is used to set bit INTF0. 0_B The rising edge is not used 1_B The detection of a rising edge of Input Channel 0 generates a trigger event (INTF0 becomes set)

Field	Bits	Type	Description
LDEN0	10	rw	**Level Detection Enable 0** This bit determines if bit INTF0 is cleared automatically if an edge of the input Input Channel 0 is detected, which has not been selected (rising edge with REN0 = 0 or falling edge with FEN0 = 0). 0_B Bit INTF0 will not be cleared 1_B Bit INTF0 will be cleared
EIEN0	11	rw	**External Input Enable 0** This bit enables the generation of a trigger event for request channel 0 (e.g. for interrupt generation) when a selected edge is detected. 0_B The trigger event is disabled 1_B The trigger event is enabled
INP0	[14:12]	rw	**Input Node Pointer** This bit field determines the destination (output channel) for trigger event 0 (if enabled by EIEN0). 000_B The event of input channel 0 triggers output channel 0 (signal INT00) 001_B The event of input channel 0 triggers output channel 1 (signal INT01) 010_B The event of input channel 0 triggers output channel 2 (signal INT02) 011_B The event of input channel 0 triggers output channel 3 (signal INT03) 100_B Reserved, do not use this combination 101_B Reserved, do not use this combination 110_B Reserved, do not use this combination 111_B Reserved, do not use this combination
EXIS1	[21:20]	rw	**External Input Selection 1** This bit field determines which input line is selected for Input Channel 1. 00_B Input 10 is selected 01_B Input 11 is selected 10_B Input 12 is selected 11_B Input 13 is selected

Field	Bits	Type	Description
FEN1	24	rw	**Falling Edge Enable 1** This bit determines if the falling edge of Input Channel 1 is used to set bit INTF1. 0_B The falling edge is not used 1_B The detection of a falling edge of Input Channel 1 generates a trigger event (INTF1 becomes set)
REN1	25	rw	**Rising Edge Enable 1** This bit determines if the rising edge of Input Channel 1 is used to set bit INTF1. 0_B The rising edge is not used 1_B The detection of a rising edge of Input Channel 1 generates a trigger event (INTF1 becomes set)
LDEN1	26	rw	**Level Detection Enable 1** This bit determines if bit INTF1 is cleared automatically if an edge of the input Input Channel 1 is detected, which has not been selected (rising edge with REN1 = 0 or falling edge with FEN1 = 0). 0_B Bit INTF1 will not be cleared 1_B Bit INTF1 will be cleared
EIEN1	27	rw	**External Input Enable 1** This bit enables the generation of a trigger event for request channel 1 (e.g. for interrupt generation) when a selected edge is detected. 0_B The trigger event is disabled 1_B The trigger event is enabled

Field	Bits	Type	Description
INP1	[30:28]	rw	**Input Node Pointer** This bit field determines the destination (output channel) for trigger event 1 (if enabled by EIEN1). 000_B The event of input channel 1 triggers output channel 0 (signal INT10) 001_B The event of input channel 1 triggers output channel 1 (signal INT11) 010_B The event of input channel 1 triggers output channel 2 (signal INT12) 011_B The event of input channel 1 triggers output channel 3 (signal INT13) 100_B Reserved, do not use this combination 101_B Reserved, do not use this combination 110_B Reserved, do not use this combination 111_B Reserved, do not use this combination
0	[3:0], [7:6], [19:15], [23:22], 31	r	**Reserved** Read as 0; should be written with 0.

EICR1

External Input Channel Register 1 (084_H) Reset Value: 0000 0000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0		**INP3**		**EI EN3**	**LD EN3**	**R EN3**	**F EN3**	**0**		**EXIS3**		**0**			
r		rw		rw	rw	rw	rw	r		rw		r			

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0		**INP2**		**EI EN2**	**LD EN2**	**R EN2**	**F EN2**	**0**		**EXIS2**		**0**			
r		rw		rw	rw	rw	rw	r		rw		r			

Field	Bits	Type	Description
EXIS2	[5:4]	rw	**External Input Selection 2** This bit field determines which input line is selected for Input Channel 2. 00_B Input 20 is selected 01_B Input 21 is selected 10_B Input 22 is selected 11_B Input 23 is selected
FEN2	8	rw	**Falling Edge Enable 2** This bit determines if the falling edge of Input Channel 2 is used to set bit INTF2. 0_B The falling edge is not used 1_B The detection of a falling edge of Input Channel 2 generates a trigger event (INTF3 becomes set)
REN2	9	rw	**Rising Edge Enable 2** This bit determines if the rising edge of signal Input Channel 2 is used to set bit INTF2. 0_B The rising edge is not used 1_B The detection of a rising edge of Input Channel 2 generates a trigger event (INTF2 becomes set)
LDEN2	10	rw	**Level Detection Enable 2** This bit determines if bit INTF2 is cleared automatically if an edge of the input Input Channel 2 is detected, which has not been selected (rising edge with REN2 = 0 or falling edge with FEN2 = 0). 0_B Bit INTF2 will not be cleared 1_B Bit INTF2 will be cleared
EIEN2	11	rw	**External Input Enable 2** This bit enables the generation of a trigger event for request channel 2 (e.g. for interrupt generation) when a selected edge is detected. 0_B The trigger event is disabled 1_B The trigger event is enabled

Field	Bits	Type	Description
INP2	[14:12]	rw	**Input Node Pointer** This bit field determines the destination (output channel) for trigger event 2 (if enabled by EIEN2). 000_B The event of input channel 2 triggers output channel 0 (signal INT20) 001_B The event of input channel 2 triggers output channel 1 (signal INT21) 010_B The event of input channel 2 triggers output channel 2 (signal INT22) 011_B The event of input channel 2 triggers output channel 3 (signal INT23) 100_B Reserved, do not use this combination 101_B Reserved, do not use this combination 110_B Reserved, do not use this combination 111_B Reserved, do not use this combination
EXIS3	[21:20]	rw	**External Input Selection 3** This bit field determines which input line is selected for Input Channel 3. 00_B Input 30 is selected 01_B Input 31 is selected 10_B Input 32 is selected 11_B Input 33 is selected
FEN3	24	rw	**Falling Edge Enable 3** This bit determines if the falling edge of Input Channel 3 is used to set bit INTF3. 0_B The falling edge is not used 1_B The detection of a falling edge of Input Channel 3 generates a trigger event (INTF3 becomes set)
REN3	25	rw	**Rising Edge Enable 3** This bit determines if the rising edge of signal Input Channel 3 is used to set bit INTF3. 0_B The rising edge is not used 1_B The detection of a rising edge of Input Channel 3 generates a trigger event (INTF3 becomes set)

Field	Bits	Type	Description
LDEN3	26	rw	**Level Detection Enable 3** This bit determines if bit INTF3 is cleared automatically if an edge of the input Input Channel 3 is detected, which has not been selected (rising edge with REN3 = 0 or falling edge with FEN3 = 0). 0_B Bit INTF3 will not be cleared 1_B Bit INTF3 will be cleared
EIEN3	27	rw	**External Interrupt Enable 3** This bit enables the generation of a trigger event for request channel 3 (e.g. for interrupt generation) when a selected edge is detected. 0_B The trigger event is disabled 1_B The trigger event is enabled
INP3	[30:28]	rw	**Interrupt Node Pointer** This bit field determines the destination (output channel) for trigger event 3 (if enabled by EIEN3). 000_B The event of input channel 3 triggers output channel 0 (signal INT30) 001_B The event of input channel 3 triggers output channel 1 (signal INT31) 010_B The event of input channel 3 triggers output channel 2 (signal INT32) 011_B The event of input channel 3 triggers output channel 3 (signal INT33) 100_B Reserved, do not use this combination 101_B Reserved, do not use this combination 110_B Reserved, do not use this combination 111_B Reserved, do not use this combination
0	[3:0], [7:6], [19:15], [23:22], 31	r	**Reserved** Read as 0; should be written with 0.

The External Input Flag Register EIFR contains all status flags for the external input channels. The bits in this register can be cleared by software by setting FMR.FCx, and set by setting FMR.FSx.

EIFR
External Input Flag Register **(088_H)** **Reset Value: $0000\ 0000_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0												INTF3	INTF2	INTF1	INTF0
r												rh	rh	rh	rh

Field	Bits	Type	Description
INTFx (x = 0-3)	x	rh	**External Interrupt Flag of Channel x** This bit monitors the status flag of the event trigger condition for the input channel x. This bit is automatically cleared when the selected condition (see RENx, FENx) is no longer met (if LDENx = 1) or remains set until it is cleared by software (if LDENx = 0).
0	[31:4]	r	**Reserved** Read as 0; should be written with 0.

FMR
Flag Modification Register **($08C_H$)** **Reset Value: $0000\ 0000_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0												FC3	FC2	FC1	FC0
r												w	w	w	w

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0												FS3	FS2	FS1	FS0
r												w	w	w	w

Field	Bits	Type	Description
FSx (x = 0-3)	x	w	**Set Flag INTFx for Channel x** Setting this bit will set the corresponding bit INTFx in register EIFR. Reading this bit always delivers a 0. 0_B The bit x in register EIFR is not modified 1_B The bit x in register EIFR is set
FCx (x = 0-3)	16 + x	w	**Clear Flag INTFx for Channel x** Setting this bit will clear the corresponding bit INTFx in register EIFR. Reading this bit always delivers a 0. 0_B The bit x in register EIFR is not modified 1_B The bit x in register EIFR is cleared
0	[15:4], [31:20]	r	**Reserved** Read as 0; should be written with 0.

The Pattern Detection Result Register monitors the combinatorial output status of the pattern detection units.

PDRR
Pattern Detection Result Register (090_H) Reset Value: 0000 000F$_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0												PDR 3	PDR 2	PDR 1	PDR 0
r												rh	rh	rh	rh

Field	Bits	Type	Description
PDRy (y = 0-3)	y	rh	**Pattern Detection Result of Channel y** This bit monitors the output status of the pattern detection for the output channel y.
0	[31:4]	r	**Reserved** Read as 0; should be written with 0.

The Interrupt Gating Control Registers IGCR0 and IGCR1 contain bits to enable the pattern detection and to control the gating for output channel 0 to 3.

IGCR0
Interrupt Gating Register 0 (094_H) Reset Value: 0000 0000$_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
IGP1		GEEN1	0			ISS1		0				IPEN13	IPEN12	IPEN11	IPEN10
rw		rw	r			rw		r				rw	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IGP0		GEEN0	0			ISS0		0				IPEN03	IPEN02	IPEN01	IPEN00
rw		rw	r			rw		r				rw	rw	rw	rw

Field	Bits	Type	Description
IPEN0x (x = 0-3)	x	rw	**Interrupt Pattern Enable for Channel 0** Bit IPEN0x determines if the flag INTFx of channel x takes part in the pattern detection for the gating of the requests for the output signals GOUTy and IOUTy. 0_B The bit INTFx does not take part in the pattern detection 1_B The bit INTFx is taken into consideration for the pattern detection
ISS0	[9:8]	rw	**Internal Trigger Source Selection** This bit field defines which input is selected as peripheral trigger input for OGU0. The possible input signals are given in **Table 3-13**. 00_B The peripheral trigger function is disabled 01_B Input ERU_OGU01 is selected 10_B Input ERU_OGU02 is selected 11_B Input ERU_OGU03 is selected

Field	Bits	Type	Description
GEEN0	13	rw	**Generate Event Enable 0** Bit GEEN0 enables the generation of a trigger event for output channel 0 when the result of the pattern detection changes. When using this feature, a trigger (e.g. for an interrupt) is generated during the first clock cycle when a pattern is detected or when it is no longer detected. 0_B The trigger generation at a change of the pattern detection result is disabled 1_B The trigger generation at a change of the pattern detection result is enabled
ISS1	[25:24]	rw	**Internal Trigger Source Selection** This bit field defines which input is selected as peripheral trigger input for OGU1. The possible input signals are given in **Table 3-13**. 00_B The peripheral trigger function is disabled 01_B Input ERU_OGU11 is selected 10_B Input ERU_OGU12 is selected 11_B Input ERU_OGU13 is selected
IGP0	[15:14]	rw	**Interrupt Gating Pattern 0** Bit field IGP0 determines how the pattern detection influences the output lines GOUT0 and IOUT0. 00_B The detected pattern is not taken into account. An activation of IOUT0 is always possible due to a trigger event. 01_B The detected pattern is not taken into account. An activation of IOUT0 is not possible. 10_B The detected pattern is taken into account. An activation of IOUT0 is only possible due to a trigger event while the pattern is detected. 11_B The detected pattern is taken into account. An activation of IOUT0 is only possible due to a trigger event while the pattern is not detected.

Field	Bits	Type	Description
IPEN1x (x = 0-3)	16+x	rw	**Interrupt Pattern Enable for Channel 1** Bit IPEN1x determines if the flag INTFx of channel x takes part in the pattern detection for the gating of the requests for the output signals GOUTy and IOUTy. 0_B The bit INTFx does not take part in the pattern detection 1_B The bit INTFx is taken into consideration for the pattern detection
GEEN1	29	rw	**Generate Event Enable 1** Bit GEEN1 enables the generation of a trigger event for output channel 1 when the result of the pattern detection changes. When using this feature, a trigger (e.g. for an interrupt) is generated during the first clock cycle when a pattern is detected, or when it is no longer detected. 0_B The trigger generation at a change of the pattern detection result is disabled 1_B The trigger generation at a change of the pattern detection result is enabled
IGP1	[31:30]	rw	**Interrupt Gating Pattern 1** Bit field IGP1 determines how the pattern detection influences the output lines GOUT1 and IOUT1. 00_B The detected pattern is not taken into account. An activation of IOUT1 is always possible due to a trigger event. 01_B The detected pattern is not taken into account. An activation of IOUT1 is not possible. 10_B The detected pattern is taken into account. An activation of IOUT1 is only possible due to a trigger event while the pattern is detected. 11_B The detected pattern is taken into account. An activation of IOUT1 is only possible due to a trigger event while the pattern is not detected.
0	[7:4], [12:10], [23:20],[28:26]	r	**Reserved** Read as 0; should be written with 0.

IGCR1
Interrupt Gating Register 1 **(098_H)** **Reset Value: 0000 0000$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
IGP3		GEEN3	0			ISS3		0				IPEN33	IPEN32	IPEN31	IPEN30
rw		rw	r			rw		r				rw	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IGP2		GEEN2	0			ISS2		0				IPEN23	IPEN22	IPEN21	IPEN20
rw		rw	r			rw		r				rw	rw	rw	rw

Field	Bits	Type	Description
IPEN2x (x = 0-3)	x	rw	**Interrupt Pattern Enable for Channel 2** Bit IPEN2x determines if the flag INTFx of channel x takes part in the pattern detection for the gating of the requests for the output signals GOUTy and IOUTy. 0_B The bit INTFx does not take part in the pattern detection 1_B The bit INTFx is taken into consideration for the pattern detection
ISS2	[9:8]	rw	**Internal Trigger Source Selection** This bit field defines which input is selected as peripheral trigger input for OGU2. The possible input signals are given in **Table 3-13**. 00_B The peripheral trigger function is disabled 01_B Input ERU_OGU21 is selected 10_B Input ERU_OGU22 is selected 11_B Input ERU_OGU23 is selected

Field	Bits	Type	Description
GEEN2	13	rw	**Generate Event Enable 2** Bit GEEN2 enables the generation of a trigger event for output channel 2 when the result of the pattern detection changes. When using this feature, a trigger (e.g. for an interrupt) is generated during the first clock cycle when a pattern is detected, or when it is no longer detected. 0_B The trigger generation at a change of the pattern detection result is disabled 1_B The trigger generation at a change of the pattern detection result is enabled
IGP2	[15:14]	rw	**Interrupt Gating Pattern 2** Bit field IGP2 determines how the pattern detection influences the output lines GOUT2 and IOUT2. 00_B The detected pattern is not taken into account. An activation of IOUT2 is always possible due to a trigger event. 01_B The detected pattern is not taken into account. An activation of IOUT2 is not possible. 10_B The detected pattern is taken into account. An activation of IOUT2 is only possible due to a trigger event while the pattern is detected. 11_B The detected pattern is taken into account. An activation of IOUT2 is only possible due to a trigger event while the pattern is not detected.
IPEN3x (x = 0-3)	16+x	rw	**Interrupt Pattern Enable for Channel 3** Bit IPEN3x determines if the flag INTFx of channel x takes part in the pattern detection for the gating of the requests for the output signals GOUTy and IOUTy. 0_B The bit INTFx does not take part in the pattern detection 1_B The bit INTFx is taken into consideration for the pattern detection

Field	Bits	Type	Description
ISS3	[25:24]	rw	**Internal Trigger Source Selection** This bit field defines which input is selected as peripheral trigger input for OGU13. The possible input signals are given in **Table 3-13**. 00_B The peripheral trigger function is disabled 01_B Input ERU_OGU31 is selected 10_B Input ERU_OGU32 is selected 11_B Input ERU_OGU33 is selected
GEEN3	29	rw	**Generate Event Enable 3** Bit GEEN3 enables the generation of a trigger event for output channel 3 when the result of the pattern detection changes. When using this feature, a trigger (e.g. for an interrupt) is generated during the first clock cycle when a pattern is detected, or when it is no longer detected. 0_B The trigger generation at a change of the pattern detection result is disabled 1_B The trigger generation at a change of the pattern detection result is enabled
IGP3	[31:30]	rw	**Interrupt Gating Pattern 3** Bit field IGP3 determines how the pattern detection influences the output lines GOUT3 and IOUT3. 00_B The detected pattern is not taken into account. An activation of IOUT3 is always possible due to a trigger event. 01_B The detected pattern is not taken into account. An activation of IOUT3 is not possible. 10_B The detected pattern is taken into account. An activation of IOUT3 is only possible due to a trigger event while the pattern is detected. 11_B The detected pattern is taken into account. An activation of IOUT3 is only possible due to a trigger event while the pattern is not detected.
0	[7:4], [12:10], [23:20], [28:26]	r	**Reserved** Read as 0; should be written with 0.

3.4 Power Management

This section describes the power management system of the TC1798. Topics covered here include the internal system interfaces, external interfaces, and the operations of the CPU and peripherals.

3.4.1 Power Management Overview

The TC1798 power-management system allows software to configure the various processing units so that they automatically adjust to draw the minimum necessary power for the application.

As shown in **Table 3-15**, there are three power management modes available:

- Run Mode
- Idle Mode
- Sleep Mode

Table 3-15 Power Management Mode Summary

Mode	Description
Run Mode	The system is fully operational. CPU and peripherals are enabled, as determined by software.
Idle Mode	The CPU is disabled, waiting for a condition to return it to Run Mode. Idle Mode can be entered by software when the processor has no active tasks to perform. Processor memory is accessible to peripherals. An Application Reset, Watchdog Timer event, an NMI trap, or any interrupt for the CPU will return the system to Run Mode.
Sleep Mode	Only those peripherals programmed to operate in Sleep Mode are active. The other peripheral module will be shut down. Interrupts for the CPU, a Watchdog Timer event, an NMI trap, or an Application Reset will return the system to Run Mode. Entering this state requires an orderly shut-down controlled by the Power Management State Machine.

The power-management modes provide flexible reduction of power consumption through a combination of techniques, including:

- Stopping the CPU
- Stopping other system components individually
- Clock-speed reduction of some peripheral components individually

The Power Management controls the power mode of all system components during Run Mode, Idle Mode, and Sleep Mode. This flexibility in power management provides minimum power consumption for any application.

In typical operation, Idle Mode and Sleep Mode may be entered and exited frequently during the run time of an application. For example, system software will typically cause

the CPU to enter Idle Mode each time it has to wait for an interrupt before continuing its tasks. In Sleep Mode and Idle Mode, wake-up is performed automatically when any interrupt is detected or if an NMI trap is activated.

3.4.2 Power Management Modes

This section describes in more detail the power management modes, their operations, and how power management modes are entered and exited. It also describes the behavior of TC1798 system components in all power management modes.

3.4.2.1 Idle Mode

The Idle Mode is requested by software when writing to register PMCSR.REQSLP = 01_B. The CPU finishes its current operation, sends an acknowledge to the Power Management, and then enters an inactive state in which the CPU and the DMI and PMI memory units are shut off.

Other system components that are able to write to register PMCSR can also request the Idle Mode. For example, the PCPDMA controller can request Idle Mode by writing to the PMCSR register.

During Idle Mode, memory accesses to the DMI and PMI cause these units to awaken automatically to handle the transactions. When memory transactions are complete, the DMI and PMI return to Idle Mode again.

The system will return to Run Mode through the occurrence of any of the following conditions:

- An interrupt is received from an interrupt source of the CPU
- An NMI trap request is received
- An Application Reset is generated

If any of these conditions arise, the TC1798 immediately awakens and returns to Run Mode. If it is awakened by a reset, the TC1798 system begins its reset sequence. If it is awakened by a Watchdog Timer overflow event, it executes the instruction following the one that was last executed before Idle Mode was entered. If it is awakened by an NMI or interrupt, the CPU will immediately vector to the appropriate handler.

3.4.2.2 Sleep Mode

The Sleep Mode is requested by software when writing to register PMCSR.REQSLP = 10_B.

Entering Sleep Mode

Sleep Mode is entered in two steps:

1. The CPU is put into Idle Mode as described in the previous section. When the Power Management receives the Idle acknowledge back from the CPU, it proceeds with the second step.
2. Each FPI Bus unit is requested to enter the Sleep Mode. The response of each FPI Bus unit to the sleep request is determined by its clock control register. These clock control registers must have been previously configured by software.

TC1798 State During Sleep Mode

Sleep Mode is disabled for a unit if MOD_CLC.EDIS is set. The sleep request is ignored in this case and the corresponding unit continues normal operation. If MOD_CLC.EDIS is cleared, Sleep Mode is enabled for this unit and the unit enters Sleep Mode. Two actions then occur:

- The unit finishes whatever bus transaction was in progress when the signal was received
- The unit functions are suspended

Depending on bit MOD_CLC.FSOE, the module is either immediately stopped (MOD_CLC.FSOE = 1), or the unit is allowed to finish ongoing operations (MOD_CLC.FSOE = 0) before the Sleep Mode is entered. For example, setting MOD_CLC.FSOE to 1 for a serial port will stop all actions in the serial port immediately when the sleep request is received. Ongoing transmissions or receptions will be aborted. If MOD_CLC.FSOE is cleared, ongoing transmissions or receptions will be completed, before Sleep Mode is entered. The purpose of setting MOD_CLC.FSOE = 1 is to allow a debugger to observe the internal state of a peripheral unit immediately.

Exiting Sleep Mode

The system will be returned to Run Mode by the same events that exit Idle Mode. The response of the CPU to being awakened is also the same as for Idle Mode. Peripheral units that have entered Sleep Mode will switch back to their selected Run Mode operation.

3.4.3 Power Management Control and Status Register, PMCSR

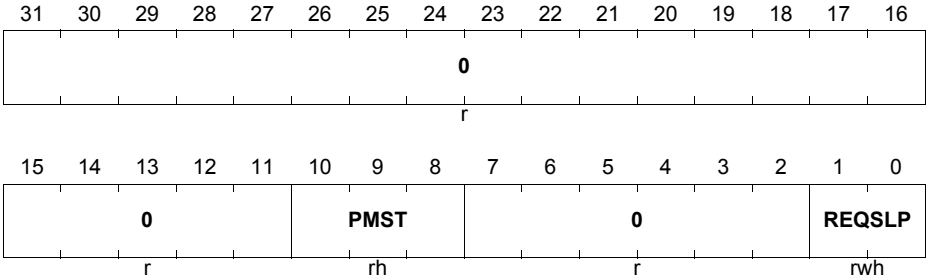
The set of registers used for power management is divided between central TC1798 components and peripheral components. The PMCSR register provides software control

and status information for the central part. There are individual clock control registers for peripheral components because the Sleep Mode behavior of each peripheral component is programmable. When entering Idle Mode and Sleep Mode, the Power Management directly controls TC1798 components such as the CPU, but indirectly controls peripheral components through their clock control registers.

PMCSR

Power Management Control and Status Register

($0B0_H$) **Reset Value: $0000\ 0100_H$**



Field	Bits	Type	Function
REQSLP	[1:0]	rwh	**Idle Mode and Sleep Mode Request** 00_B Normal Run Mode 01_B Request Idle Mode 10_B Request Sleep Mode 11_B Reserved; do not use this combination In Idle Mode or Sleep Mode, these bits are cleared in response to an interrupt for the CPU, or when bit 15 of the Watchdog Timer count register (the WDT_SR.TIM[15] bit) changes from 0 to 1.
PMST	[10:8]	rh	**Power Management Status** 000_B Waiting for PLL lock condition 001_B Normal Run Mode 010_B Idle Mode requested 011_B Idle Mode acknowledged 100_B Sleep Mode 101_B Reserved, do not use this combination 110_B Reserved, do not use this combination 111_B Reserved, do not use this combination

Field	Bits	Type	Function
0	[7:2], [31:11]	r	**Reserved** Read as 0; should be written with 0.

3.5 Software Boot Support

In order to determine the correct starting point of operation for the software a minimum of hardware support is required. As much as possible is done via software. Some decisions have to be done in hardware because they must be known before any software is operational.

For a startup operation there are two general cases that have to be handled:

- Differentiation between Test Mode and Normal Mode for each Power-on Reset event (see **Section 3.5.1**)
- Configuration of the boot option for each Application Reset event (see **Section 3.5.2**)

3.5.1 Configuration done with Start-up

With the device power-on some basic operating mode selection has to be made. The first decision that has to be made is if the device should operate in Test Mode or in Normal (Customer) Mode. The Test Mode is only for Infineon internal usage not for any customer and has nothing to do with debugging.

If the Normal Mode was selected the next decision is which debug interface type issued for debugging for this session (until the next power-on event).

Table 3-16 Normal Mode / Test Mode Input Selection

Field	Description
$\overline{\text{TEST}}$L	**Latched $\overline{\text{TEST}}$ Signal** 0 A Test Mode can be selected 1 Normal Mode is selected
$\overline{\text{TRST}}$L	**Latched $\overline{\text{TRST}}$ Signal** 0 The JTAG interface is active 1 The DAP interface is active

After these two decisions were made the detailed decision has to be made to define the real startup configuration. Most is made via the software and can be supported by some hardware selections depending on the startup configuration that should be selected.

3.5.2 Start-up Configuration Options

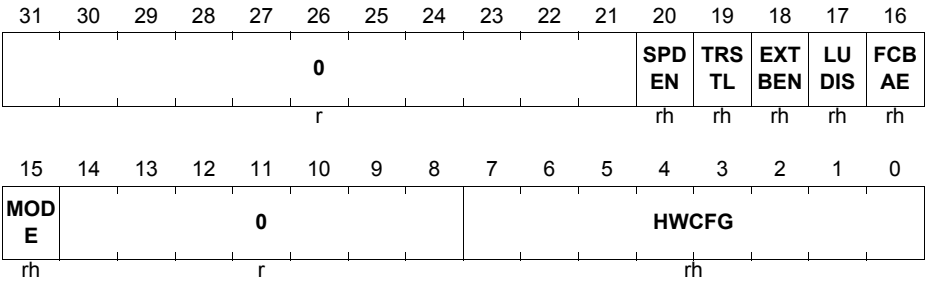
For the support of the start-up pins P0.0 to P0.7 are latched with the rising edge of the Application Reset and stored in register STSTAT.HWCFG. The update of bit field STSTAT.HWCFG with the latched value is only done if bit STSTAT.LUDIS is cleared. If bit STSTAT.LUDIS is set the value of STSTAT.HWCFG is not updated.

3.5.3 Start-up Registers

3.5.3.1 Start-up Status Register

Register STSTAT contains the information required by the boot software to identify the different start-up settings that can be selected.

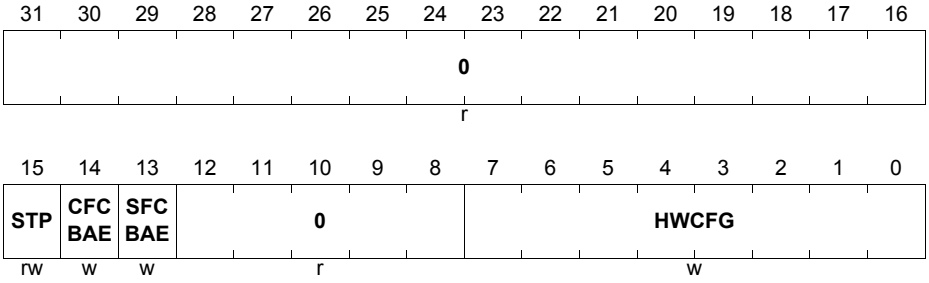
STSTAT
Start-up Status Register **($0C0_H$)** **Reset Value: 0008 80XX$_H$**



Field	Bits	Type	Description
HWCFG	[7:0]	rh	**Hardware Configuration Setting** This bit field contains the value that is used by the boot software. This bit field is updated in case of an Application Reset with the content by register SWRSTCON.SWCFG if bit SWRSTCON.SWBOOT AND RSTSTAT.SW are set. This bit field is updated in case of an Application Reset with the content of the latches of P0.0 to P.0.7 if bit SWRSTCON.SWBOOT OR RSTSTAT.SW are cleared and bit STSTAT.LUDIS is cleared. This bit field is left unchanged in case of an Application Reset and is not updated with the content of the latches of P0.0 to P.0.7 if bit SWRSTCON.SWBOOT OR RSTSTAT.SW are cleared and bit STSTAT.LUDIS is set. This bit field is updated with the value written to bit field STCON.HWCFG on a software write action.

Field	Bits	Type	Description
Mode	15	rh	**Mode** This bit indicates if the Test Mode is entered or not. 0_B A Test Mode can be selected 1_B Normal Mode is selected
FCBAE	16	rh	**Flash Config. Sector Access Enable** 0_B Flash config sector is not accessible. Instead the flash memory area is accessed. 1_B Flash config sector is accessible. The flash memory area can not be accessed. This bit can be cleared by setting bit STCON.CFCBAE. This bit can be set by setting bit STCON.SFCBAE.
LUDIS	17	rh	**Latch Update Disable** 0_B Bit field STSTAT.HWCFG is automatically updated with the latched value of pins P0.0 to P0.7 1_B Bit field STSTAT.HWCFG is not updated with the latched value of pins P0.0 to P0.7 This bit can be set by setting bit SYSCON.SETLUDIS.
EXTBEN	18	rh	**External Boot Enable** 0_B No Boot Configuration Value is fetched by the EBU 1_B A Boot Configuration Value is fetched by the EBU This bit can be set by setting bit SYSCON.SETEXTBEN.
TRSTL	19	rh	**TRSTL Status** This bit simply displays the value of TRSTL.
SPDEN	20	rh	**Single Pin DAP Mode Enable** 0_B Single Pin DAP Mode is disabled 1_B Single Pin DAP Mode is enabled
0	[14:8], [31:21]	r	**Reserved** Read as 0; should be written with 0.

STCON
Start-up Configuration Register (0C4$_H$) Reset Value: 0000 8000$_H$



Field	Bits	Type	Description
HWCFG	[7:0]	w	**Hardware Configuration Setting** Writing to this bit field updates bit field STSTAT.HWCFG. Reading this bit field returns zero.
SFCBAE	13	w	**Set Flash Config. Sector Access Enable** Setting this bit sets bit STSTAT.FCBAE. Reading this bit returns always a zero. *Note: This bit may not be set in parallel with bit CFCBAE.*
CFCBAE	14	w	**Clear Flash Config. Sector Access Enable** Setting this bit clears bit STCON.FCBAE. Reading this bit returns always a zero. *Note: This bit may not be set in parallel with bit SFCBAE.*
STP	15	rw	**Start-up Protection Setting** 0_B Start-up code is executed. Start-up protection is disabled. 1_B Start-up code protection is active This bit is also cleared by an Application Reset.
0	[12:8], [31:16]	r	**Reserved** Read as 0; should be written with 0.

3.6 ECC Error Handling

The on-chip RAM and flash modules check ECC information during read accesses and in case of an error a signal is generated. These signals are combined and trigger a trap.

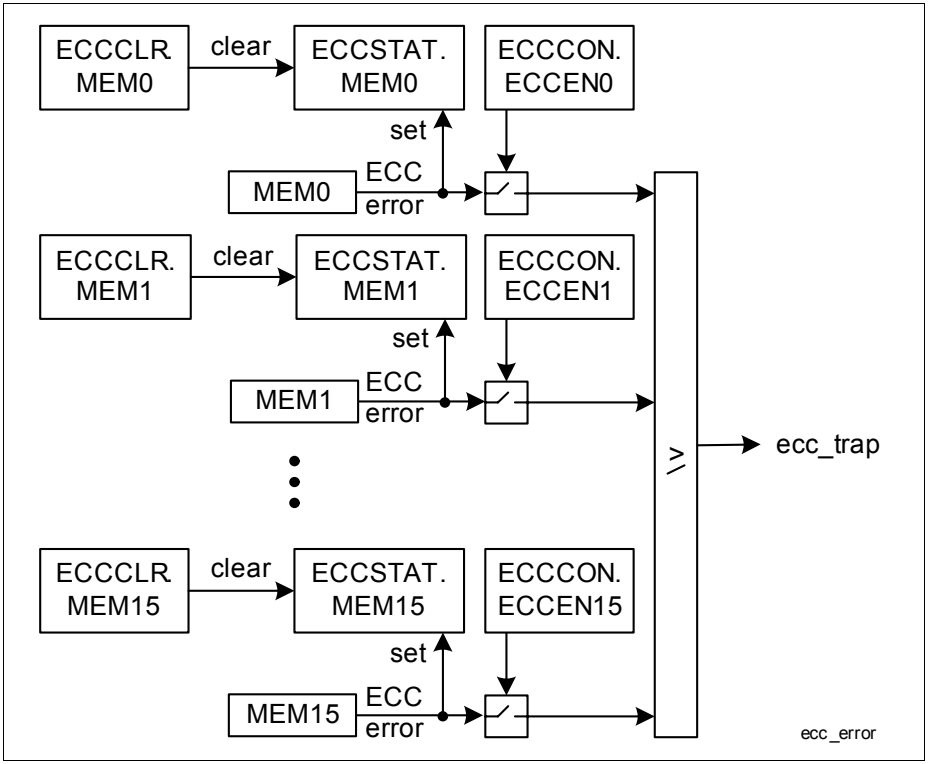


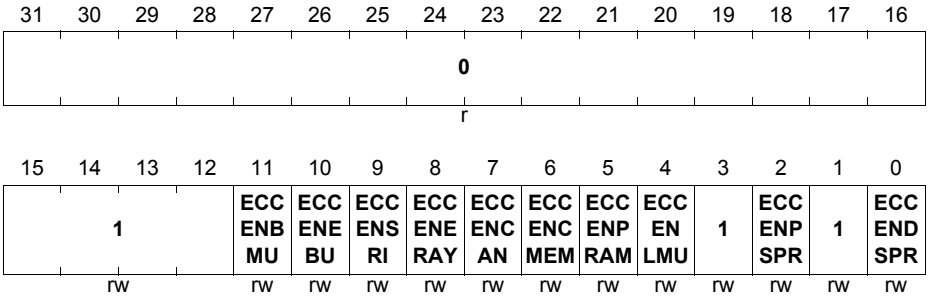
Figure 3-27 ECC Error Control Logic

3.6.1 ECC Software Testing Support

This can be done for each module individually by simply disabling the ECC protection in the module change the content of a memory address enable ECC again and read the memory address again. For more information see the different module chapters.

3.6.2 ECC Registers

ECCCON
ECC Control Register **($0D0_H$)** **Reset Value: 0000 FFFF$_H$**



Field	Bits	Type	Description
ECCENDSPR	0	rw	**ECC Error Trap Enable for DSPR and DCACHE Memory** This bit determine whether a trap is requested if an uncorrected ECC error is detected in the DSPR / DCACHE memory. 0_B No ECC error trap trigger is requested 1_B A ECC error trap trigger is requested
ECCENPSPR	2	rw	**ECC Error Trap Enable for PDPR and ICACHE Memory** This bit determine whether a trap is requested if an uncorrected ECC error is detected in the PSPR / ICACHE memory. 0_B No ECC error trap trigger is requested 1_B A ECC error trap trigger is requested
ECCENLMU	4	rw	**ECC Error Trap Enable for LMU Memory** This bit determine whether a trap is requested if an uncorrected ECC error is detected in the LMU memory. 0_B No ECC error trap trigger is requested 1_B A ECC error trap trigger is requested

Field	Bits	Type	Description
ECCENPRAM	5	rw	**ECC Error Trap Enable for PCP PRAM** This bit determine whether a trap is requested if an uncorrected ECC error is detected in the PCP PRAM memory. 0_B No ECC error trap trigger is requested 1_B A ECC error trap trigger is requested
ECCENCMEM	6	rw	**ECC Error Trap Enable for PCP CMEM** This bit determine whether a trap is requested if an uncorrected ECC error is detected in the PCP CMEM memory. 0_B No ECC error trap trigger is requested 1_B A ECC error trap trigger is requested
ECCENCAN	7	rw	**ECC Error Trap Enable for CAN Memory** This bit determine whether a trap is requested if an uncorrected ECC error is detected in the CAN memory. 0_B No ECC error trap trigger is requested 1_B A ECC error trap trigger is requested
ECCENERAY	8	rw	**ECC Error Trap Enable for ERAY Memory** This bit determine whether a trap is requested if an uncorrected ECC error is detected in the ERAY memories. 0_B No ECC error trap trigger is requested 1_B A ECC error trap trigger is requested
ECCENSRI	9	rw	**ECC Error Trap Enable for SRI-Bus** This bit determine whether a trap is requested if an uncorrected ECC error is detected by the SRI-Bus protocol. 0_B No ECC error trap trigger is requested 1_B A ECC error trap trigger is requested
ECCENEBU	10	rw	**ECC Error Trap Enable for EBU** This bit determine whether a trap is requested if an uncorrected ECC error is detected by the EBU. 0_B No ECC error trap trigger is requested 1_B A ECC error trap trigger is requested

Field	Bits	Type	Description
ECCENBMU	11	rw	**ECC Error Trap Enable for BMU** This bit determine whether a trap is requested if an uncorrected ECC error is detected by the BMU. 0_B No ECC error trap trigger is requested 1_B A ECC error trap trigger is requested
1	1, 3, [15:12]	rw	**Reserved** Should be written with 1.
0	[31:16]	r	**Reserved** Read as 0; should be written with 0.

Note: Register ECCCON is Endinit-protected for write operations.

ECCSTAT
ECC Status Register **($0D4_H$)** **Reset Value: $0000\ 0000_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0				BMU	EBU	SRI	ERAY	CAN	CMEM	PRAM	LMU	0	PSPR	0	DSPR
r				rh	rh	rh	rh	rh	rh	rh	rh	r	rh	r	rh

Field	Bits	Type	Description
DSPR	0	rh	**ECC Error Flag for DSPR and DCACHE Memory** This bit indicate whether an ECC error has been detected in the DSPR / DCACHE memory. 0_B No ECC error detected 1_B ECC error is detected
PSPR	2	rh	**ECC Error Flag for PSPR and ICACHE Memory** This bit indicate whether an ECC error has been detected in the PSPR / ICACHE memory. 0_B No ECC error detected 1_B ECC error is detected

Field	Bits	Type	Description
LMU	4	rh	**ECC Error Flag for LMU Memory** This bit indicate whether an ECC error has been detected in the LMU memory. 0_B No ECC error detected 1_B ECC error is detected
PRAM	5	rh	**ECC Error Flag for Parameter RAM Memory** This bit indicate whether an ECC error has been detected in the Parameter RAM memory. 0_B No ECC error detected 1_B ECC error is detected
CMEM	6	rh	**ECC Error Flag for Code Memory** This bit indicate whether an ECC error has been detected in the code memory. 0_B No ECC error detected 1_B ECC error is detected
CAN	7	rh	**ECC Error Flag for CAN Memory** This bit indicate whether an ECC error has been detected in the CAN memory. 0_B No ECC error detected 1_B ECC error is detected
ERAY	8	rh	**ECC Error Flag for ERAY Memory** This bit indicate whether an ECC error has been detected in the ERAY memory. 0_B No ECC error detected 1_B ECC error is detected
SRI	9	rh	**ECC Error Flag for SRI-Bus** This bit indicate whether an ECC error has been detected by the SRI-Bus. 0_B No ECC error detected 1_B ECC error is detected
EBU	10	rh	**ECC Error Flag for EBU** This bit indicate whether an ECC error has been detected in the EBU. 0_B No ECC error detected 1_B ECC error is detected

Field	Bits	Type	Description
BMU	11	rh	**ECC Error Flag for BMU** This bit indicate whether an ECC error has been detected in the BMU. 0_B No ECC error detected 1_B ECC error is detected
0	1,3, [31:12]	r	**Reserved** Read as 0; should be written with 0.

ECCCLR
ECC Clear Register **($0D8_H$)** **Reset Value: $0000\ 0000_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0				BMU	EBU	SRI	ERAY	CAN	CMEM	PRAM	LMU	0	PSPR	0	DSPR
r				w	w	w	w	w	w	w	w	r	w	r	w

Field	Bits	Type	Description
DSPR	0	w	**Clear DSPR and DCACHE EEC Error Status** 0_B No action 1_B Setting this bit clears bit EECSTAT.DSPR This bit always read as 0.
PSPR	2	w	**Clear PSPR and PCACHE EEC Error Status** 0_B No action 1_B Setting this bit clears bit EECSTAT.PSPR This bit always read as 0.
LMU	4	w	**Clear LMU Memory EEC Error Status** 0_B No action 1_B Setting this bit clears bit EECSTAT.LMU This bit always read as 0.

Field	Bits	Type	Description
PRAM	5	w	**Clear Parameter RAM Memory EEC Error Status** 0_B No action 1_B Setting this bit clears bit EECSTAT.PRAM This bit always read as 0.
CMEM	6	w	**Clear Parameter Code Memory EEC Error Status** 0_B No action 1_B Setting this bit clears bit EECSTAT.CMEM This bit always read as 0.
CAN	7	w	**Clear CAN Memory EEC Error Status** 0_B No action 1_B Setting this bit clears bit EECSTAT.CAN This bit always read as 0.
ERAY	8	w	**Clear ERAY Memory EEC Error Status** 0_B No action 1_B Setting this bit clears bit EECSTAT.ERAY This bit always read as 0.
SRI	9	w	**Clear SRI-Bus EEC Error Status** 0_B No action 1_B Setting this bit clears bit EECSTAT.SRI This bit always read as 0.
EBU	10	w	**Clear EBU EEC Error Status** 0_B No action 1_B Setting this bit clears bit EECSTAT.EBU This bit always read as 0.
BMU	11	w	**Clear BMU EEC Error Status** 0_B No action 1_B Setting this bit clears bit EECSTAT.BMU This bit always read as 0.
0	1, 3, [31:12]	r	**Reserved** Read as 0; should be written with 0.

3.7 Die Temperature Measurement

The Die Temperature Sensor (DTS) generates a measurement result that indicates directly the current temperature. The result of the measurement is displayed via bit field DTSSTAT.RESULT. In order to start one measurement bit DTSCON.START needs to be set.

The DTS has to be enabled before it can be used via bit DTSCON.PWD. When the DTS is powered after the start-up time of the DTS (defined in the Data Sheet) a temperature measurement can be started.

Note: If bit field DTSSTAT.RESULT is read before the first measurement was finished it will return 0x000.

When a measurement is started the result is available after the measurement time passed. If the DTS is ready to start a measurement can be checked via bit DTSSTAT.RDY. If a started measurement is finished or still in progress is indicated via the status bit DTSSTAT.BUSY. The measurement time is also defined in the Data Sheet.

In order to adjust production variations bit field DTSCON.CAL should be programmed with a predefined value. The value is located at address 0xD0000018 for the complete register DTSCON with bit DTSCON.PWD cleared.

Note: The first measurement after the DTS was powered delivers a result without calibration adjustment and should be ignored therefore.

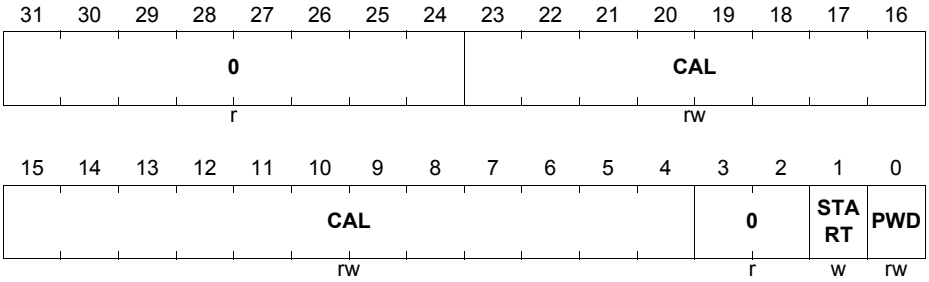
The formula to calculate the die temperature is defined in the Data Sheet.

Note: The maximum resolution is only achieved for a measurement that is part of multiple continuos measurements.

3.7.1 Die Temperature Sensor Register

DTSCON

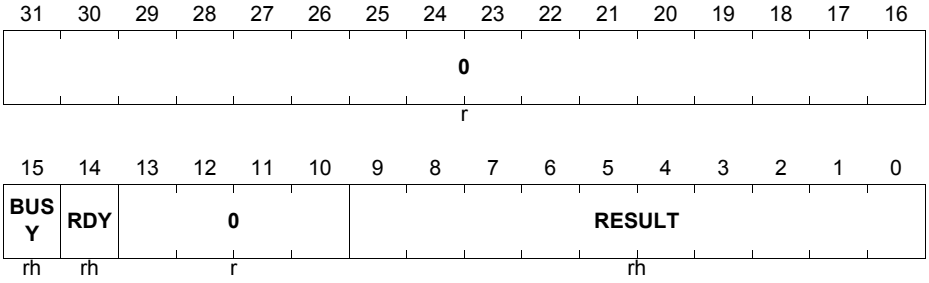
Die Temperature Sensor Control Register($0E4_H$) **Reset Value: $0000\ 0001_H$**



Field	Bits	Type	Description
PWD	0	rw	**Sensor Power Down** This bit defines the DTS power state. 0_B The DTS is powered 1_B The DTS is not powered
START	1	w	**Sensor Measurement Start** This bit starts a measurement of the DTS. 0_B No DTS measurement is started 1_B A DTS measurement is started If set this bit is automatically cleared. This bit always reads as zero.
CAL	[23:4]	rw	**Calibration Value** This bit field interfaces the calibration values to the DTS.
0	[3:2], [31:24]	r	**Reserved** Read as 0; should be written with 0.

DTSSTAT

Die Temperature Sensor Status Register($0E0_H$) **Reset Value: $0000\ 0000_H$**



Field	Bits	Type	Description
RESULT	[9:0]	rh	**Result of the DTS Measurement** This bit field shows the result of the DTS measurement. The value given is directly related to the die temperature. Only the bit [9:2] have to be evaluated. The formula for mapping the result to a temperature will follow later.
RDY	14	rh	**Sensor Ready Status** This bit indicate the DTS is ready or not. 0_B The DTS is not ready 1_B The DTS is ready
BUSY	15	rh	**Sensor Busy Status** This bit indicate the DTS is currently busy or not. If the sensor is busy currently a measurement is running and the result should not be used. 0_B The DTS is not busy 1_B The DTS is busy *Note: This bit is updated 2 cycles after bit DTSCON.START is set.*
0	[13:10], [31:16]	r	**Reserved** Read as 0; should be written with 0.

3.8 Watchdog Timer

This section describes the TC1798 Watchdog Timer (WDT). Topics include an overview of the WDT function and descriptions of the registers, the password-protection scheme, accessing registers, modes, and initialization.

3.8.1 Watchdog Timer Overview

The WDT provides a highly reliable and secure way to detect and recover from software or hardware failure. The WDT helps to abort an accidental malfunction of the TC1798 in a user-specified time period. When enabled, the WDT can cause the TC1798 system to be reset if the WDT is not serviced within a user-programmable time period. The CPU must service the WDT within this time interval to prevent the WDT from causing a TC1798 System or Application Reset. Hence, routine service of the WDT confirms that the system is functioning properly.

In addition to this standard “Watchdog” function, the WDT incorporates the End-of-Initialization (Endinit) feature and monitors its modifications.

Because servicing the Watchdog and modifications of the ENDINIT bit are critical functions that must not be allowed in case of a system malfunction, a sophisticated scheme is implemented that requires a password and guard bits during accesses to the WDT control register. Any write access that does not deliver the correct password or the correct value for the guard bits is regarded as a malfunction of the system, and a Watchdog reset is requested. In addition, even after a valid access has been performed and the ENDINIT bit has been cleared to provide access to the critical registers, the Watchdog imposes a time limit for this access window. If bit ENDINIT has not been properly set again before this limit expires, the system is assumed to have malfunctioned, and a Watchdog reset is requested. These stringent requirements, although not guaranteed, nonetheless provide a high degree of assurance of the robustness of system operation.

A further enhancement in the TC1798’s WDT is its reset prewarning operation. Instead of immediately resetting the device on the detection of an error (the way that standard Watchdogs do), the WDT first issues a Non-Maskable Interrupt (NMI) to the CPU before finally resetting the device at a specified time period later.

3.8.2 Features of the Watchdog Timer

The main features of the WDT are summarized here.

- 16-bit Watchdog counter
- Selectable input frequency: $f_{FPI}/256$ or $f_{FPI}/16384$
- 16-bit user-definable reload value for normal Watchdog operation, fixed reload value for Time-Out and Prewarning Modes
- Incorporation of the ENDINIT bit and monitoring of its modifications

- Sophisticated Password Access mechanism with fixed and user-definable password fields
- Access Error Detection: Invalid password (during first access) or invalid guard bits (during second access) trigger the Watchdog reset generation
- Overflow Error Detection: An overflow of the counter triggers the Watchdog reset generation
- Watchdog function can be disabled; access protection and ENDINIT bit monitor function remain enabled
- Double Reset Detection

3.8.3 The Endinit Function

It is a prerequisite to understand the ENDINIT bit and its function for better understanding of the descriptions in the following sections. Hence, its function is explained first.

There are a number of registers in the TC1798 that are usually programmed only once during the initialization sequence of the application. Modification of such registers during normal application run can have a severe impact on the overall operation of modules or the entire system.

While the Supervisor Mode, that allows writes to registers only when it is active, provides a certain level of protection against unintentional modifications, it may not provide enough security for system-critical registers.

The TC1798 provides one more level of protection for such registers via the Endinit feature. This is a highly secure write-protection scheme that makes unintentional modifications of registers protected by this feature nearly impossible.

The Endinit feature consists of an ENDINIT bit incorporated in the WDT control register, WDT_CON0. Registers protected via Endinit determine whether or not writes are enabled. Writes are only enabled if bit ENDINIT = 0 AND Supervisor Mode is active. Write attempts if this condition is not true will be discarded and the register contents will not be modified in this case. The BCU controls the further operation following a discarded write access.

To get the highest level of security, this bit is incorporated in the highly secure access protection scheme implemented in the WDT. This is a complex procedure, that makes it nearly impossible for the ENDINIT bit to be modified unintentionally. In addition, the WDT monitors ENDINIT bit modifications by starting a time-out sequence each time software opens access to the critical registers through clearing bit ENDINIT. If the time out period ends before bit ENDINIT is set again, a malfunction of the software is assumed and a reset request is generated.

The access-protection scheme and the Endinit time-out operation of the WDT is described in the following sections. **Table 3-17** lists the registers that are protected via the Endinit feature in the TC1798.

Note: The clearing of the ENDINIT bit takes some time. Accesses to Endinit-protected registers after the clearing of the ENDINT bit must only be done when bit ENDINIT is really cleared. As a solution, WDT_CON0 (the register with the ENDINIT bit) should be read back once before Endinit-protected registers are accessed the first time after bit ENDINIT has been cleared.

Table 3-17 TC1798 Registers Protected via the Endinit Feature

Register Name	Description
mod_CLC	All clock control registers of the individual peripheral modules are Endinit-protected
mod_FDR	All clock fractional divider registers of the individual peripheral modules are Endinit-protected
BTV, BIV, ISP	Trap and interrupt vector table pointer as well as the interrupt stack pointer are Endinit-protected
MIECON **SMACON** **COMPAT**	CPU Control Registers
FLASH0_FCON **FLASH1_FCON** **FLASH0_RDWCFG0** **FLASH0_RDWCFG1** **FLASH0_RDWCFG2** **FLASH1_RDWCFG0** **FLASH1_RDWCFG1** **FLASH1_RDWCFG2** **FLASH0_MARP** **FLASH1_MARP** **FLASH0_ECCW** **FLASH1_ECCW** **FLASH0_ECCR** **FLASH1_ECCR**	Flash configuration registers
WDT_CON1	The Watchdog Timer Control Register 1, which controls the disabling and the input frequency of the Watchdog Timer, is Endinit-protected. In addition, its bits will only have an effect on the WDT when ENDINIT is properly set to 1 again.

Table 3-17 TC1798 Registers Protected via the Endinit Feature (cont'd)

Register Name	Description
SCU_OSCCON **SCU_PLLCON0** **SCU_PLLCON1** **SCU_CCUCON0** **FDR** **SCU_CCUCON1**	All clock control registers are protected
SCU_RSTCNTCON **SCU_RSTCON** **SCU_ARSTDIS** **SCU_SWRSTCON**	All reset control registers are protected
SCU_ESRCFG0 **SCU_ESRCFG1**	All ESR control registers are protected
SCU_EMSR	The emergency stop register
SCU_TRAPSET **SCU_TRAPDIS**	The trap set and disable register
SHE_MPRTS **SHE_MPRTE**	SHE memory protection
P17_PDISC **Px_ESR** **Px_PDR**	Port Control Registers
DMA_MExARR **DMA_MExAENR** **DMA_OCDSR** **DMA_SUSPMR**	DMA Control Registers
PCP_CS	PCP Control Registers
DMI_CON	DMI Control Registers

3.8.3.1 Password Access to WDT_CON0

A correct password must be written to register WDT_CON0 in order to unlock it for modifications. Software must either know the correct password in advance or compute it at runtime. The password required to unlock the register is formed by a combination of bits in registers WDT_CON0 and WDT_CON1, plus a number of guard bits. **Table 3-18** summarizes the requirements for the password.

Table 3-18 Password Access Bit Pattern Requirements

Bit Position	Required Value
0	Current state of bit WDT_CON0.ENDINIT
1	Fixed; must be written with 0
2	Current state of bit WDT_CON1.IR
3	Current state of bit WDT_CON1.DR
[7:4]	Fixed; must be written to 1111_B
[15:8]	Current value of user.definable password field WDT_CON0.PW
[31:16]	Current value of user-definable reload value, WDT_CON0REL

The password is designed such that it is not possible to just read the contents of a register and use this as the password. The password is never identical to the contents of WDT_CON0 or WDT_CON1, it is always required to modify the read value (at least bits 1 and [7:4]) to get the correct password. This prevents a malfunction from accidentally reading a WDT register's contents and writing it to WDT_CON0 as an unlocking password.

If the password matches the requirements, WDT_CON0 will be unlocked as soon as the Password Access is completed. The unlocked condition will be indicated by WDT_CON0.LCK = 0.

If an improper password value is written to WDT_CON0 during the Password Access, a Watchdog Access Error condition exists. Bit WDT_SR.AE is set and the Prewarning Mode is entered.

The user-definable password, WDT_CON0.PW, provides additional options for adjusting the password requirements to the application's needs. It can be used, for instance, to detect unexpected software loops, or to monitor the execution sequence of routines.

3.8.3.2 Modify Access to WDT_CON0

If WDT_CON0 is successfully unlocked, the following write access to WDT_CON0 can modify it. However, this access must also meet certain requirements in order to be accepted and regarded as valid. **Table 3-19** lists the required bit patterns. If the access does not follow these rules, a Watchdog Access Error condition is detected, bit WDT_SR.AE is set, and the Prewarning Mode is entered.

Table 3-19 Modify Access Bit Pattern Requirements

Bit Position	Value
0	User-definable; desired value for bit WDT_CON0.ENDINIT.
1	Fixed; must be written with 1.
2	Fixed; must be written with 0.
3	Fixed; must be written with 0.
[7:4]	Fixed; must be written with 1111_B.
[15:8]	User-definable; desired value of user-definable password field, WDT_CON0.PW.
[31:16]	User-definable; desired value of user-definable reload value, WDT_CON0.REL.

After the Modify Access has completed, WDT_CON0.LCK is set again, automatically re-locking WDT_CON0. Before the register can be modified again, a valid Password Access must be executed again.

3.8.3.3 Access to Endinit-Protected Registers

If some or all of the system's Endinit-protected registers must be changed during run time of an application, access can be re-opened. To do this, WDT_CON0 must first be unlocked with a Valid Password Access. In the subsequent Valid Modify Access, ENDINIT can be cleared. Access to Endinit-protected registers is now open again. However, when WDT_CON0 is unlocked, the WDT is automatically switched to Time-Out Mode. Thus, the access window is time-limited. Time-Out Mode is only terminated after ENDINIT has been set again, requiring another Valid Password and Valid Modify Access to WDT_CON0.

If the WDT is not used in an application and is therefore disabled (WDT_SR.DS = 1), the above described case is the only occasion when WDT_CON0 must be accessed again after the system is initialized. If there are no further changes to critical system registers needed, no further accesses to WDT_CON0, WDT_CON1, or WDT_SR are necessary. However, it is recommended that the WDT be used in an application for safety reasons.

For debugging support the Cerberus module can override the ENDINIT control to ease the debug flow. If bit CBS_OSTATE.ENIDIS is set the ENDINIT protection is disabled independent of the current status configured by the WDT. If CBS_OSTATE.ENIDIS is cleared the complete control is within the WDT.

3.8.4 Timer Operation

The timer is automatically active after an Application Reset. The 16-bit counter implementing the timer functionality is either triggered with f_{FPI} / 256 or f_{FPI} / 16384. The two possible counting rates are controlled via bit WDT_CON1.IR.

Determining WDT Periods

The WDT uses the FPI-Bus clock f_{FPI}. A clock divider in front of the WDT provides two output frequencies, f_{FPI} / 256 and f_{FPI} / 16384.

The general formula to calculate a Watchdog period is:

$$\text{period} = \frac{(2^{16} - \text{startvalue}) \cdot 256 \cdot 2^{(1-\text{IR}) \cdot 6}}{f_{FPI}} \quad (3.19)$$

The parameter start value represents the fixed value $FFFC_H$ for the calculation of the Time-Out Period, and the user-programmable reload value WDT_CON0.REL for the calculation of the Normal Period.

3.8.4.1 Timer Modes

The Watchdog Timer can operate in one of four different operating modes:

- Time-Out Mode
- Normal Mode
- Disable Mode
- Prewarning Mode

The following overview describes these modes and how the WDT changes from one mode to the other.

Time-Out Mode

The Time-Out Mode is entered after an Application Reset or when a valid Password Access to register WDT_CON0 is performed (see **Section 3.8.3.1**). The Time-Out Mode is indicated by bit WDT_SR.TO = 1. The timer is set to $FFFC_H$ and starts counting upwards. Time-Out Mode can only be exited properly by setting ENDINIT = 1 with a correct access sequence. If an improper access to the WDT is performed, or if the timer overflows before ENDINIT is set, a WDT_NMI is requested, and Prewarning Mode is entered.

A proper exit from Time-Out Mode can either be to the Normal or the Disable Mode, depending on the state of the disable request bit WDT_CON1.DR.

Normal Mode

In Normal Mode (DR = 0), the WDT operates in a standard Watchdog fashion. The timer is set to WDT_CON0.REL, and begins counting up. It has to be serviced before the counter overflows. Servicing is performed through a proper access sequence to the control register WDT_CON0. This enters the Time-Out Mode.

If the WDT is not serviced before the timer overflows, a system malfunction is assumed. Normal Mode is terminated, a WDT_NMI is requested, and Prewarning Mode is entered.

Disable Mode

Disable Mode is provided for applications which truly do not require the WDT function. It can be requested from Time-Out Mode when the disable request bit WDT_CON1.DR is set. The Disable Mode is entered when was requested AND bit WDT_CON0.ENDINIT is set. The timer is stopped in this mode. However, disabling the WDT only stops it from performing the standard Watchdog function, eliminating the need for timely service of the WDT. It does not disable Time-Out and Prewarning Mode. If an access to register WDT_CON0 is performed in Disable Mode, Time-Out Mode is entered if the access was valid, and Prewarning Mode is entered if the access was invalid. Thus, the ENDINIT monitor function as well as (a part of) the system malfunction detection will still be active.

Prewarning Mode

Prewarning Mode is entered always when a Watchdog error is detected. This can be due to an overflow of the timer in Normal or Time-Out Mode, or an invalid access to register WDT_CON0. Instead of immediately requesting a reset of the device, the WDT enables the system to enter a secure state by a prewarning before the reset occurs.

In Prewarning Mode, after having generated the NMI request, the WDT counts up from $FFFC_H$, and then generates a Watchdog reset request on the overflow. This reset request cannot be avoided in this mode; the WDT does not react anymore to accesses to its registers, nor will it change its state unless reset by an Application Reset. This is to prevent a malfunction from falsely terminating this mode, disabling the reset, and letting the device to continue to function improperly. Register WDT_CON0 can still be accessed by a valid Password Access.

Note: In Prewarning Mode, it is not required for the part to wait for the end of this mode and the reset. After having saved required state in the NMI routine, software can execute an Application Reset to shorten the time.

Note: The Prewarning Mode is only left by an application Reset and not only on the reset request. Therefore if bit field RSTCON.WDT is set to 00_B the Prewarning Mode is not left.

3.8.4.2 WDT Reset Behavior

WDT reset requests are generated for three cases:

- Invalid password access to register WDT_CON0
- Not finishing a password access before a timer overflow occurs in the Time-Out Mode
- Not serving the WDT before a timer overflow occurs in the Normal Mode

If a reset is generated on a WDT reset request and the kind of the reset can be configured via bit field RSTCON.WDT.

Note: The WDT itself is reset by any Application Reset.

Before a reset is requested the Prewarning Mode is entered, for more details see **Section 3.8.4.1**.

Double WDT Reset

If the Watchdog induced reset occurs twice, a severe system malfunction is assumed and the TC1798 is held in reset until a System Reset occurs. This prevents the device from being periodically reset if, for instance, connection to the external memory has been lost such that even system initialization could not be performed.

If the WDT is configured to request an Application Reset the second reset request will be permanently asserted resulting (without any change in the reset configuration) resulting in a permanent Application Reset. The information about the first WDT reset request is stored in an internal flag which is reset with the System Reset. This flag is set when the Prewarning Mode is finished and the reset request is generated. If a new reset is requested and the internal flag is already set a double reset event has occurred and a permanent request is generated. This internal flag is cleared by any System Reset or when bit WDT_CON1.CLRIRF is set AND bit WDT_CON0.ENDINIT is set too. Please note that a correct service of the WDT does not clear this internal flag. Bit WDT_CON1.CLRIRF can only be set when bit WDT_CON0.ENDINIT is cleared.

Note: It does not matter whether a reset was generated on a WDT reset request or if the reset configuration was changed between the two reset requests.

Note: If for any reason random code is executed bit field RSTCON.WDT can be updated unintentional. This can result that a WDT error does not lead to an reset. To avoid this after the SSW is finished this bit field should be checked and the ENDINIT protection enabled.

Servicing the Watchdog Timer

If the WDT is used in an application and is enabled (WDT_SR.DS = 0), it must be regularly serviced to prevent it from overflowing.

Service is performed in two steps. a Valid Password Access followed by a Valid Modify Access. The Valid Password Access to WDT_CON0 automatically switches the WDT to Time-Out Mode. Thus, the Modify Access must be performed before the Time-out expires or a System Reset will result.

During the next Modify Access, the strict requirement is that WDT_CON0.ENDINIT as well as bit 1 and bits [7:4] are written with 1, while bits [3:2] are written with 0.

Note: ENDINIT must be written with 1 to perform a proper service, even if it is already set to 1.

Changes to the reload value WDT_CON0.REL, or the user-definable password WDT_CON0.PW, are not required. However, changing WDT_CON0.PW is recommended so that software can monitor WDT service operations throughout the duration of an application program (see next section).

When WDT service is properly executed, Time-Out Mode is terminated, and the WDT switches back to its former mode of operation, and WDT service is complete.

3.8.4.3 WDT Operation During Power-Saving Modes

If the CPU is in Idle Mode or Sleep Mode, it cannot service the WDT because no software is running. Excluding the case where the system is running normally, a strategy for managing the WDT is needed while the CPU is in Idle or Sleep Mode. There are two ways to manage the WDT in these cases. First, the Watchdog can be disabled before idling the CPU. The disadvantage of this is that the system will no longer be monitored during the idle period.

A better approach to this problem relies upon a wake-up feature of the WDT. Whenever the CPU is put in Idle or Sleep Mode and the WDT is not disabled, it causes the CPU to be awakened at regular intervals. When the WDT changes its count value (WDT_SR.TIM) from $7FFF_H$ to 8000_H, the CPU is awakened and continues to execute the instruction following the instruction that was last executed before entering the Idle or Sleep Mode.

Note: Before switching into a non-running power-management mode, software should perform a Watchdog service sequence. At the Modify Access, the Watchdog reload value, WDT_CON0.REL, should be programmed such that the wake-up occurs after a period which best meets application requirements. The maximum period between two CPU wake-ups is one-half of the maximum WDT period.

3.8.4.4 Suspend Mode Support

In an enabled and active debug session the Watchdog functionality can lead to unintended resets. Therefore to avoid these resets the OCDS can control if the WDT is enabled or disabled (default after Application Reset) via bit CBS_OSTATE.WDTSUS if it is not already stopped.

Table 3-20 OCDS Behavior of WDT

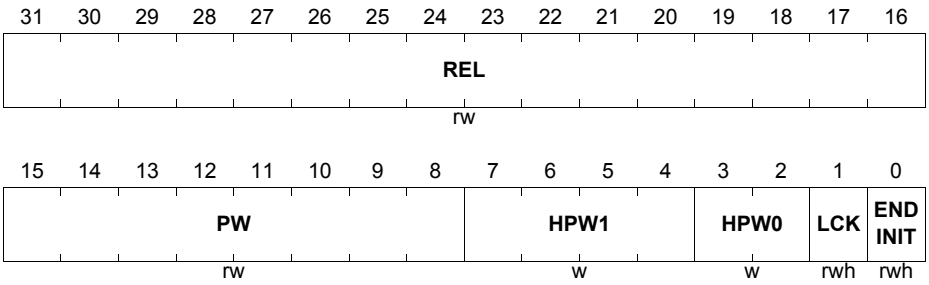
STCON.STP	WDT_SR.DS	CBS_OSTATE.OEN	CBS_OSTATE.SUS	CBS_MCDSSG.SOS	WDT Action
0	X	X	X	X	Stopped
1	1	X	X	X	Stopped
1	0	0	X	X	Running
1	0	1	0	X	Stopped
1	0	1	1	0	Running
1	0	1	1	1	Stopped

3.8.5 Watchdog Timer Registers

3.8.5.1 Watchdog Timer Control Register 0

Register WDT_CON0 manages Password Access to the Watchdog Timer. It also stores the timer reload value, a user-definable password field, a lock bit, and the End-of-Initialization (ENDINIT) control bit.

WDT_CON0
WDT Control Register 0 (F000 05F0$_H$) Reset Value: FFFC 0002$_H$



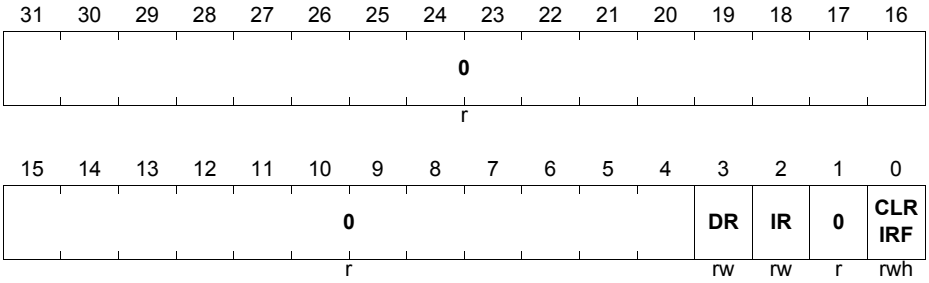
Field	Bits	Type	Description
ENDINIT	0	rwh	**End-of-Initialization Control Bit** 0_B Access to Endinit-protected registers is permitted (default after Application Reset) 1_B Access to Endinit-protected registers is not permitted

Field	Bits	Type	Description
LCK	1	rwh	**Lock Bit to Control Access to WDT_CON0** 0_B Register WDT_CON0 is unlocked 1_B Register WDT_CON0 is locked (default after Application Reset) The actual value of LCK is controlled by hardware. It is cleared after a valid Password Access to WDT_CON0, and automatically set again after a valid Modify Access to WDT_CON0. During a write to WDT_CON0, the value written to this bit is only used for the password-protection mechanism and is not stored. This bit must be cleared during a Password Access to WDT_CON0, and set during a Modify Access to WDT_CON0. That is, the inverted value read from LCK always must be written to itself.
HPW0	[3:2]	w	**Hardware Password 0** This bit field must be written with the value of the bits WDT_CON1.DR and WDT_CON1.IR during a Password Access. This bit field must be written with 0s during a Modify Access to WDT_CON0. When read, these bits always return 0.
HPW1	[7:4]	w	**Hardware Password 1** This bit field must be written with 1111_B during both Password Access and Modify Access to WDT_CON0. When read, these bits always return 0.
PW	[15:8]	rw	**User-Definable Password Field for Access to WDT_CON0** This bit field must be written with its current contents during a Password Access. It can be changed during a Modify Access to WDT_CON0.
REL	[31:16]	rw	**Reload Value for the WDT** If the Watchdog Timer is enabled and in Normal Timer Mode, it will start counting from this value after a correct Watchdog service. This bit field must be written with its current contents during a Password Access. It can be changed during a Modify Access to WDT_CON0 ($FFFC_H$ = default after Application Reset).

3.8.5.2 Watchdog Timer Control Register 1

WDT_CON1 manages operation of the WDT. It includes the disable request and frequency selection bits. It is ENDINIT-protected.

WDT_CON1
WDT Control Register 1 **(F000 05F4$_H$)** **Reset Value: 0000 0000$_H$**



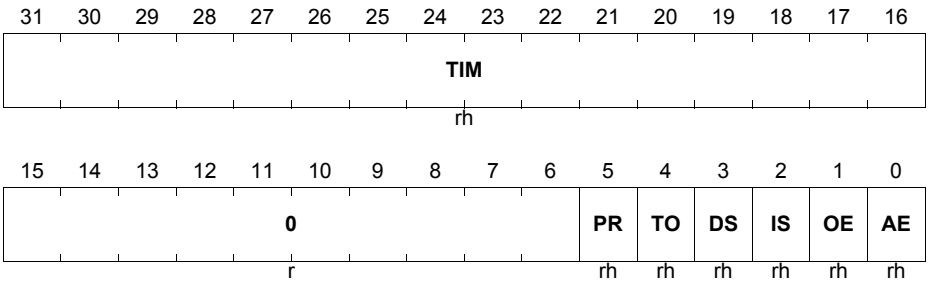
Field	Bits	Type	Description
CLRIRF	0	rwh	**Clear Internal Reset Flag** This bit is used to request a clear of the internal flag storing the information about the first WDT reset request. 0_B No action 1_B Request to clear the internal flag This bit can only be modified if WDT_CON0.ENDINIT is cleared. The internal flag is cleared when ENDINIT is set again. As long as ENDINIT is cleared, the internal flag is unchanged and controls the current past error status of the WDT. When ENDINIT is set again with a Valid Modify Access, the internal flag is cleared together with this bit.

Field	Bits	Type	Description
IR	2	rw	**Input Frequency Request Control Bit** 0_B Request to set input frequency to $f_{FPI}/16384$. 1_B Request to set input frequency to $f_{FPI}/256$. This bit can only be modified if WDT_CON0.ENDINIT is cleared. WDT_SR.IS is updated by this bit only when ENDINIT is set again. As long as ENDINIT is cleared, WDT_SR.IS controls the current input frequency of the Watchdog Timer. When ENDINIT is set again, WDT_SR.IS is updated with the state of IR.
DR	3	rw	**Disable Request Control Bit** 0_B Request to enable the WDT 1_B Request to disable the WDT This bit can only be modified if WDT_CON0.ENDINIT is cleared. WDT_SR.DS is updated when ENDINIT is set again. As long as ENDINIT is cleared, bit WDT_SR.DS controls the current enable/disable status of the WDT. When ENDINIT is set again with a Valid Modify Access, WDT_SR.DS is updated with the state of DR.
0	1, [31:4]	r	**Reserved** Read as 0; should be written with 0.

3.8.5.3 Watchdog Timer Status Register

Register WDT_SR shows the current state of the WDT. Status include bits indicating reset prewarning, Time-Out, enable/disable status, input clock status, and access error status.

WDT_SR
WDT Status Register **(F000 05F8$_H$)** **Reset Value: FFFC 0010$_H$**



Field	Bits	Type	Description
AE	0	rh	**Watchdog Access Error Status Flag** 0_B No Watchdog access error 1_B A Watchdog access error has occurred This bit is set when an illegal Password Access or Modify Access to register WDT_CON0 was attempted. This bit is only cleared when WDT_CON0.ENDINIT is set during a Valid Modify Access However, it is not possible to clear this bit if the WDT is in Prewarning Mode.
OE	1	rh	**Watchdog Overflow Error Status Flag** 0_B No Watchdog overflow error 1_B A Watchdog overflow error has occurred This bit is set when the WDT overflows from $FFFF_H$ to 0000_H. This bit is only cleared when WDT_CON0.ENDINIT is set to 1 during a Valid Modify Access. However, it is not possible to clear this bit if the WDT is in Prewarning Mode.
IS	2	rh	**Watchdog Input Clock Status Flag** 0_B The timer operation clock is f_{FPI}/16384 (default after Application Reset) 1_B The timer operation clock is f_{FPI}/256 This bit is updated with the state of bit WDT_CON1.IR after WDT_CON0.ENDINIT is written with 1 during a Valid Modify Access to register WDT_CON0.
DS	3	rh	**Watchdog Enable/Disable Status Flag** 0_B WDT is enabled (default after Application Reset) 1_B WDT is disabled This bit is updated with the state of bit WDT_CON1.DR after WDT_CON0.ENDINIT is set during a Valid Modify Access to register WDT_CON0.

Field	Bits	Type	Description
TO	4	rh	**Watchdog Time-Out Mode Flag** 0_B The Watchdog is not operating in Time-Out Mode 1_B The Watchdog is operating in Time-Out Mode (default after Application Reset) This bit is set when Time-Out Mode is entered. It is automatically cleared when Time-Out Mode is left.
PR	5	rh	**Watchdog Prewarning Mode Flag** 0_B The Watchdog is not operating in Prewarning Mode 1_B The Watchdog is operating in Prewarning Mode This bit is set when a Watchdog error is detected. The WDT has issued a trap trigger and is in Prewarning Mode. A reset of the chip occurs after the prewarning period has expired if it is enabled in bit field RSTCON.WDT.
TIM	[31:16]	rh	**Timer Value** Reflects the current content of the WDT.
0	[15:6]	r	**Reserved** Read as 0.

3.9 Emergency Stop Output Control

The emergency stop feature of the TC1798 allows for a fast emergency reaction on an external event without the intervention of software. In an emergency case, the outputs can be selectively put immediately to a well-defined logic state (for more information see the port chapter).

The emergency case is indicated by an emergency input signal with selectable polarity that has to be connected to input P9.10.

Figure 3-28 shows a diagram of the emergency stop input logic. This logic is controlled by the SCU Emergency Stop Register EMSR.

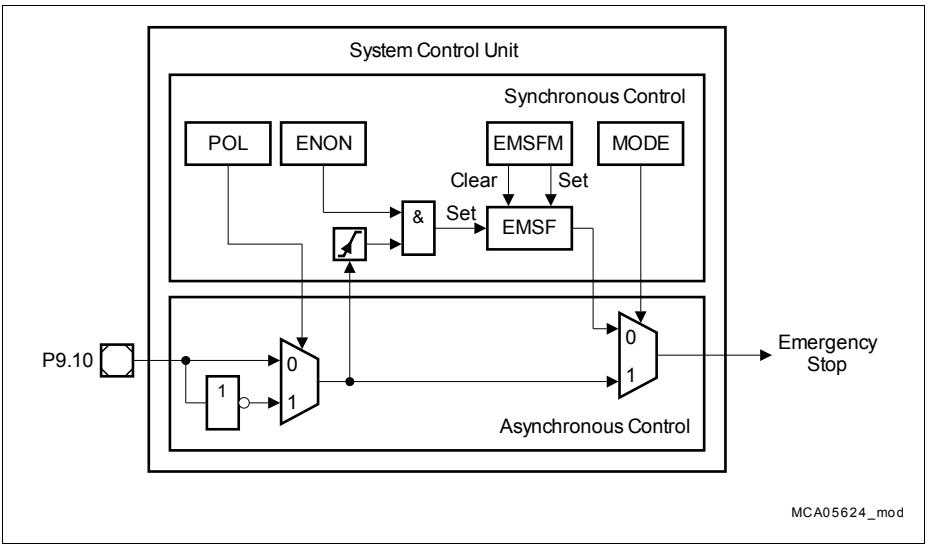


Figure 3-28 Emergency Stop Input Control

The emergency stop control logic for the ports can basically operate in two modes:

- Synchronous Mode (default after reset):
  Emergency case is activated by hardware and released by software.
- Asynchronous Mode:
  Emergency case is activated and released by hardware.

In Synchronous Mode (selected by EMSR.MODE = 0), the port signal is sampled for a inactive-to-active level transition, and an emergency stop flag EMSR.EMSF is set if the transition is detected. The setting of EMSR.EMSF activates the emergency stop signal. An emergency case can only be terminated by clearing EMSR.EMSF via software. The synchronous control logic is clocked by the system bus clock f_{FPI}. This results in a small delay between the port signal and emergency stop signal generation.

In Asynchronous Mode (selected by EMSR.MODE = 1), the occurrence of an active level at the port input immediately activates the emergency stop signal. Of course, a valid-to-invalid transition of the port input (emergency case is released) also immediately deactivates the emergency stop signal.

The EMSR.POL bit determines the active level of the input signal. The EMSR.MODE bit selects Synchronous or Asynchronous Mode for emergency stop signal generation.

3.9.1 Emergency Stop Register

The Emergency Stop Register EMSR contains control and status bits/flags of the emergency stop input logic.

EMSR
Emergency Stop Register **(100_H)** **Reset Value: 0000 0000$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0						EMSFM		0							EMSF
r						w		r							rh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0													ENON	MODE	POL
r													rw	rw	rw

Field	Bits	Type	Description
POL	0	rw	**Input Polarity** This bit determines the polarity of the input line. 0_B Input is high active 1_B Input is low active
MODE	1	rw	**Mode Selection** This bit determines the operating mode of the emergency stop signal. 0_B Synchronous Mode selected; emergency stop is derived from the state of flag EMSF 1_B Asynchronous Mode selected; emergency stop is directly derived from the state of the input signal
ENON	2	rw	**Enable ON** This bit enables the setting of flag EMSF by an inactive-to-active level transition of input signal. 0_B Setting of EMSF is disabled 1_B Setting of EMSF is enabled

Field	Bits	Type	Description
EMSF	16	rh	**Emergency Stop Flag** This bit indicates if an emergency stop condition has occurred. 0_B An emergency stop has not occurred 1_B An emergency stop has occurred and signal emergency stop becomes active (if MODE = 0)
EMSFM	[25:24]	w	**Emergency Stop Flag Modification** This bit field set or clear flag EMSF via software. 00_B EMSF remains unchanged 01_B EMSF becomes set 10_B EMSF becomes cleared 11_B EMSF remains unchanged EMSFM is always read as 00_B.
0	[15:3], [23:17], [31:26]	r	**Reserved** Read as 0; should be written with 0.

3.10 Interrupt Generation

The interrupt structure is shown in **Figure 3-29**. The interrupt request or the corresponding interrupt set bit (in register INTSET) can trigger the interrupt generation at the selected interrupt node x. The service request pulse is generated independently from the interrupt flag in register INTSTAT. The interrupt flag can be cleared by software by writing to the corresponding bit in register INTCLR.
If more than one interrupt source is connected to the same interrupt node pointer (in register INTNP), the requests are combined to one common line.

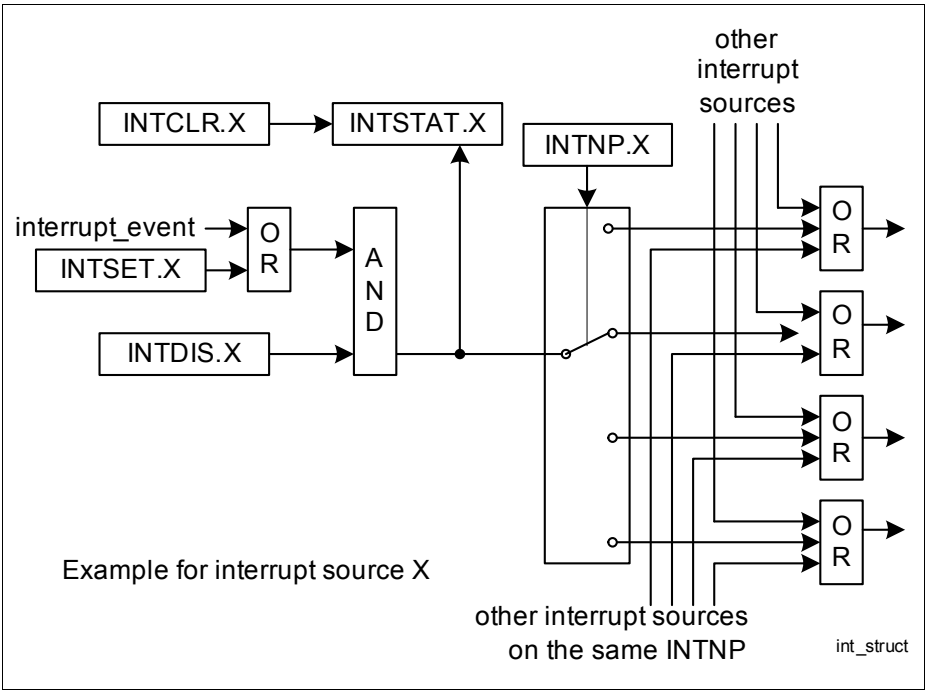
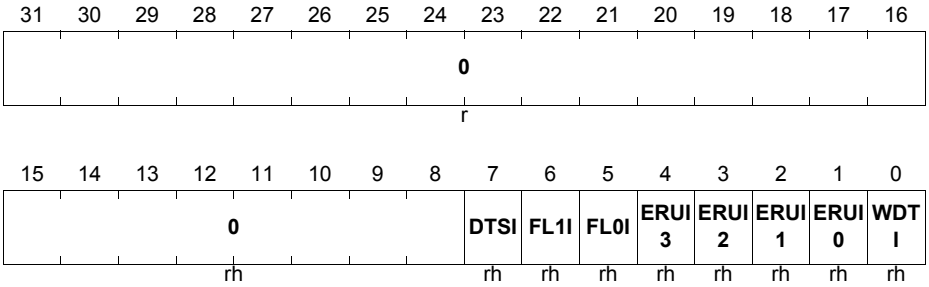


Figure 3-29 Interrupt Generation

3.10.1 Interrupt Control Registers

INTSTAT
Interrupt Status Register **(110_H)** **Reset Value: 0000 0000$_H$**



Field	Bits	Type	Description
WDTI	0	rh	**Watchdog Timer Interrupt Request Flag** This bit is set if the WDT Prewarning Mode is entered and bit is INTDIS.WDTI = 0. 0_B No interrupt was requested since this bit was cleared the last time 1_B An interrupt was requested since this bit was cleared the last time This bit can be cleared by bit INTCLR.WDTI. This bit can be set by bit INTSET.WDTI.
ERUI0	1	rh	**ERU Channel 0 Interrupt Request Flag** This bit is set if the ERU channel 0 is active and bit is INTDIS.ERUI0 = 0. 0_B No interrupt was requested since this bit was cleared the last time 1_B An interrupt was requested since this bit was cleared the last time This bit can be cleared by bit INTCLR.ERUI0. This bit can be set by bit INTSET.ERUI0.

Field	Bits	Type	Description
ERUI1	2	rh	**ERU Channel 1 Interrupt Request Flag** This bit is set if the ERU channel 1 is active and bit is INTDIS.ERUI1 = 0. 0_B No interrupt was requested since this bit was cleared the last time 1_B An interrupt was requested since this bit was cleared the last time This bit can be cleared by bit INTCLR.ERUI1. This bit can be set by bit INTSET.ERUI1.
ERUI2	3	rh	**ERU Channel 2 Interrupt Request Flag** This bit is set if the ERU channel 2 is active and bit is INTDIS.ERUI2 = 0. 0_B No interrupt was requested since this bit was cleared the last time 1_B An interrupt was requested since this bit was cleared the last time This bit can be cleared by bit INTCLR.ERUI2. This bit can be set by bit INTSET.ERUI2.
ERUI3	4	rh	**ERU Channel 3 Interrupt Request Flag** This bit is set if the ERU channel 3 is active and bit is INTDIS.ERUI3 = 0. 0_B No interrupt was requested since this bit was cleared the last time 1_B An interrupt was requested since this bit was cleared the last time This bit can be cleared by bit INTCLR.ERUI3. This bit can be set by bit INTSET.ERUI3.
FL0I	5	rh	**Flash 0 Interrupt Request Flag** This bit is set if the Flash interrupt trigger is active and bit is INTDIS.FL0I = 0. 0_B No interrupt was requested since this bit was cleared the last time 1_B An interrupt was requested since this bit was cleared the last time This bit can be cleared by bit INTCLR.FL0I. This bit can be set by bit INTSET.FL0I.

Field	Bits	Type	Description
FL1I	6	rh	**Flash 1 Interrupt Request Flag** This bit is set if the Flash interrupt trigger is active and bit is INTDIS.FL1I = 0. 0_B No interrupt was requested since this bit was cleared the last time 1_B An interrupt was requested since this bit was cleared the last time This bit can be cleared by bit INTCLR.FL1I. This bit can be set by bit INTSET.FL1I.
DTSI	7	rh	**DTS Interrupt Request Flag** This bit is set if the DTS busy indication changes from 1_B to 0_B and bit is INTDIS.DTSI = 0. 0_B No interrupt was requested since this bit was cleared the last time 1_B An interrupt was requested since this bit was cleared the last time This bit can be cleared by bit INTCLR.DTSI. This bit can be set by bit INTSET.DTSI.
0	[15:8]	rh	**Reserved** Read as 0. This bit can be cleared by bit INTCLR.[x]. This bit can be set by bit INTSET.[x]. *Note: x = 6, [13:8], 15.*
0	[31:16]	r	**Reserved** Read as 0; should be written with 0.

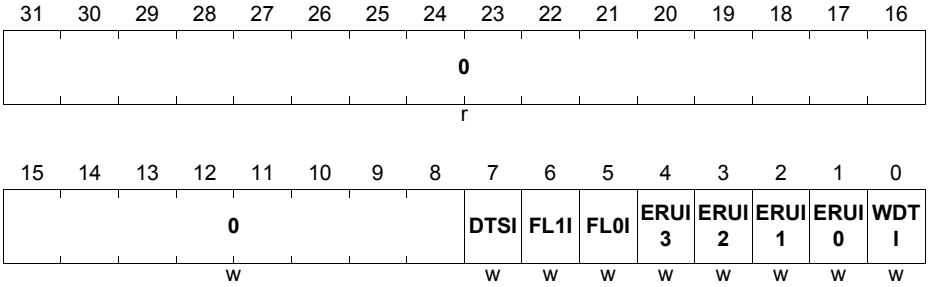
INTSET
Interrupt Set Register **(114_H)** **Reset Value: $0000\ 0000_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0								DTSI	FL1I	FL0I	ERUI3	ERUI2	ERUI1	ERUI0	WDTI
w								w	w	w	w	w	w	w	w

Field	Bits	Type	Description
WDTI	0	w	**Set Interrupt Request Flag WDTI** Setting this bit set bit INTSTAT.WDTI. Clearing this bit has no effect. Reading this bit returns always zero.
ERUI0	1	w	**Set Interrupt Request Flag ERUI0** Setting this bit set bit INTSTAT.ERUI0. Clearing this bit has no effect. Reading this bit returns always zero.
ERUI1	2	w	**Set Interrupt Request Flag ERUI1** Setting this bit set bit INTSTAT.ERUI1. Clearing this bit has no effect. Reading this bit returns always zero.
ERUI2	3	w	**Set Interrupt Request Flag ERUI2** Setting this bit set bit INTSTAT.ERUI2. Clearing this bit has no effect. Reading this bit returns always zero.
ERUI3	4	w	**Set Interrupt Request Flag ERUI3** Setting this bit set bit INTSTAT.ERUI3. Clearing this bit has no effect. Reading this bit returns always zero.
FL0I	5	w	**Set Interrupt Request Flag FL0I** Setting this bit set bit INTSTAT.FL0I. Clearing this bit has no effect. Reading this bit returns always zero.
FL1I	6	w	**Set Interrupt Request Flag FL1I** Setting this bit set bit INTSTAT.FL1I. Clearing this bit has no effect. Reading this bit returns always zero.
DTSI	7	w	**Set Interrupt Request Flag DTSI** Setting this bit set bit INTSTAT.DTSI. Clearing this bit has no effect. Reading this bit returns always zero.
0	[15:8]	w	**Reserved** Read as 0; have to be written with 0.
0	[31:16]	r	**Reserved** Read as 0; should be written with 0.

INTCLR
Interrupt Clear Register **(118_H)** **Reset Value: 0000 0000$_H$**



Field	Bits	Type	Description
WDTI	0	w	**Clear Interrupt Request Flag WDTI** Setting this bit clears bit INTSTAT.WDTI. Clearing this bit has no effect. Reading this bit returns always zero.
ERUI0	1	w	**Clear Interrupt Request Flag ERUI0** Setting this bit clears bit INTSTAT.ERUI0. Clearing this bit has no effect. Reading this bit returns always zero.
ERUI1	2	w	**Clear Interrupt Request Flag ERUI1** Setting this bit clears bit INTSTAT.ERUI1. Clearing this bit has no effect. Reading this bit returns always zero.
ERUI2	3	w	**Clear Interrupt Request Flag ERUI2** Setting this bit clears bit INTSTAT.ERUI2. Clearing this bit has no effect. Reading this bit returns always zero.
ERUI3	4	w	**Clear Interrupt Request Flag ERUI3** Setting this bit clears bit INTSTAT.ERUI3. Clearing this bit has no effect. Reading this bit returns always zero.
FL0I	5	w	**Clear Interrupt Request Flag FL0I** Setting this bit clears bit INTSTAT.FL0I. Clearing this bit has no effect. Reading this bit returns always zero.

Field	Bits	Type	Description
FL1I	6	w	**Clear Interrupt Request Flag FL1I** Setting this bit clears bit INTSTAT.FL1I. Clearing this bit has no effect. Reading this bit returns always zero.
DTSI	7	w	**Clear Interrupt Request Flag DTSI** Setting this bit clears bit INTSTAT.DTSI. Clearing this bit has no effect. Reading this bit returns always zero.
0	[15:8]	w	**Reserved** Read as 0; have to be written with 1.
0	[31:16]	r	**Reserved** Read as 0; should be written with 0.

INTDIS
Interrupt Disable Register **($11C_H$)** **Reset Value: $0000\ 0000_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

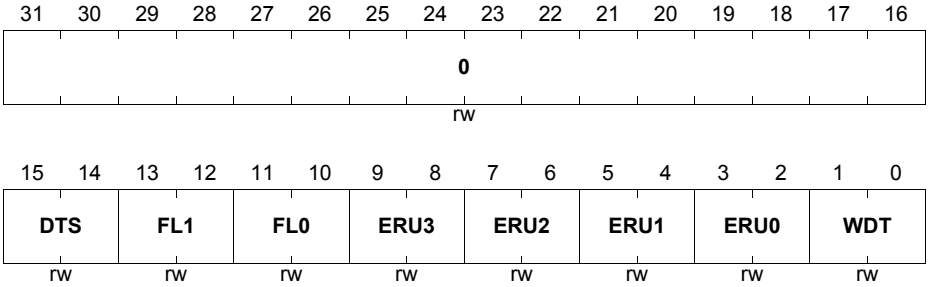
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0								DTSI	FL1I	FL0I	ERUI3	ERUTI2	ERUI1	ERUI0	WDTI
rw								rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
WDTI	0	rw	**Disable Interrupt Request WDT** 0_B An interrupt request can be generated for this source 1_B No interrupt request can be generated for this source
ERUI0	1	rw	**Disable Interrupt Request ERU0** 0_B An interrupt request can be generated for this source 1_B No interrupt request can be generated for this source

Field	Bits	Type	Description
ERUI1	2	rw	**Disable Interrupt Request ERU1** 0_B An interrupt request can be generated for this source 1_B No interrupt request can be generated for this source
ERUI2	3	rw	**Disable Interrupt Request ERU2** 0_B An interrupt request can be generated for this source 1_B No interrupt request can be generated for this source
ERUI3	4	rw	**Disable Interrupt Request ERU3** 0_B An interrupt request can be generated for this source 1_B No interrupt request can be generated for this source
FL0I	5	rw	**Disable Interrupt Request Flash 0** 0_B An interrupt request can be generated for this source 1_B No interrupt request can be generated for this source
FL1I	6	rw	**Disable Interrupt Request Flash 1** 0_B An interrupt request can be generated for this source 1_B No interrupt request can be generated for this source
DTSI	7	rw	**Disable Interrupt Request DTS** 0_B An interrupt request can be generated for this source 1_B No interrupt request can be generated for this source
0	[15:8]	rw	**Reserved** Have to be written with 1.
0	[31:16]	r	**Reserved** Read as 0; should be written with 0.

INTNP

Interrupt Node Pointer Register (120_H) Reset Value: $0000\ 0000_H$

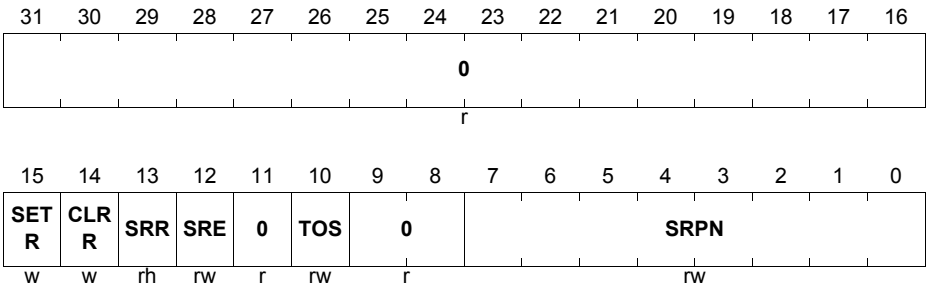


Field	Bits	Type	Description
WDT	[1:0]	rw	**Interrupt Node Pointer for Interrupt WDT** This bit field defines the interrupt node, that is requested due to the set condition for bit INTSTAT.WDTI (if enabled by bit INTDIS.WDTI). 00_B Interrupt node 0 is selected 01_B Interrupt node 1 is selected 10_B Interrupt node 2 is selected 11_B Interrupt node 3 is selected
ERU0	[3:2]	rw	**Interrupt Node Pointer for Interrupt ERU0** This bit field defines the interrupt node, that is requested due to the set condition for bit INTSTAT.ERUI0 (if enabled by bit INTDIS.ERUI0). 00_B Interrupt node 0 is selected 01_B Interrupt node 1 is selected 10_B Interrupt node 2 is selected 11_B Interrupt node 3 is selected
ERU1	[5:4]	rw	**Interrupt Node Pointer for Interrupt ERU1** This bit field defines the interrupt node, that is requested due to the set condition for bit INTSTAT.ERUI1 (if enabled by bit INTDIS.ERUI1). 00_B Interrupt node 0 is selected 01_B Interrupt node 1 is selected 10_B Interrupt node 2 is selected 11_B Interrupt node 3 is selected

Field	Bits	Type	Description
ERU2	[7:6]	rw	**Interrupt Node Pointer for Interrupt ERU2** This bit field defines the interrupt node, that is requested due to the set condition for bit INTSTAT.ERUI2 (if enabled by bit INTDIS.ERUI2). 00_B Interrupt node 0 is selected 01_B Interrupt node 1 is selected 10_B Interrupt node 2 is selected 11_B Interrupt node 3 is selected
ERU3	[9:8]	rw	**Interrupt Node Pointer for Interrupt ERU3** This bit field defines the interrupt node, that is requested due to the set condition for bit INTSTAT.ERUI3 (if enabled by bit INTDIS.ERUI3). 00_B Interrupt node 0 is selected 01_B Interrupt node 1 is selected 10_B Interrupt node 2 is selected 11_B Interrupt node 3 is selected
FL0	[11:10]	rw	**Interrupt Node Pointer for Interrupt FL0** This bit field defines the interrupt node, that is requested due to the set condition for bit INTSTAT.FL0I (if enabled by bit INTDIS.FL0I). 00_B Interrupt node 0 is selected 01_B Interrupt node 1 is selected 10_B Interrupt node 2 is selected 11_B Interrupt node 3 is selected
FL1	[13:12]	rw	**Interrupt Node Pointer for Interrupt FL1** This bit field defines the interrupt node, that is requested due to the set condition for bit INTSTAT.FL1I (if enabled by bit INTDIS.FL1I). 00_B Interrupt node 0 is selected 01_B Interrupt node 1 is selected 10_B Interrupt node 2 is selected 11_B Interrupt node 3 is selected
DTS	[15:14]	rw	**Interrupt Node Pointer for Interrupt DTS** This bit field defines the interrupt node, that is requested due to the set condition for bit INTSTAT.DTSI (if enabled by bit INTDIS.DTSI). 00_B Interrupt node 0 is selected 01_B Interrupt node 1 is selected 10_B Interrupt node 2 is selected 11_B Interrupt node 3 is selected

Field	Bits	Type	Description
0	[31:16]	rw	**Reserved** Should be written with 0.

SRC0
Service Request Control 0 Register (1FC$_H$) Reset Value: 0000 0000$_H$
SRC1
Service Request Control 1 Register (1F8$_H$) Reset Value: 0000 0000$_H$
SRC2
Service Request Control 2 Register (1F4$_H$) Reset Value: 0000 0000$_H$
SRC3
Service Request Control 3 Register (1F0$_H$) Reset Value: 0000 0000$_H$



Field	Bits	Type	Description
SRPN	[7:0]	rw	**Service Request Priority Number** 00_H Service request is never serviced 01_H Service request is on lowest priority ... FF_H Service request is on highest priority
TOS	10	rw	**Type of Service Control** 0_B CPU service is initiated 1_B PCP request is initiated
SRE	12	rw	**Service Request Enable** 0_B Service request is disabled 1_B Service request is enabled
SRR	13	rh	**Service Request Flag** 0_B No service request is pending 1_B A service request is pending

Field	Bits	Type	Description
CLRR	14	w	**Request Clear Bit** CLRR is required to clear SRR. 0_B No action 1_B Clear SRR; bit value is not stored; read always returns 0; no action if SETR is set also.
SETR	15	w	**Request Set Bit** SETR is required to set SRR. 0_B No action 1_B Set SRR; bit value is not stored; read always returns 0; no action if CLRR is set also.
0	[9:8], 11, [31:16]	r	**Reserved** Read as 0; should be written with 0.

3.11 NMI Trap Generation

The NMI trap structure is shown in **Figure 3-30**. The trap request trigger or the corresponding trap set bit (in register TRAPSET) can trigger the NMI trap generation. The trap flag can be cleared by software by writing to the corresponding bit in register TRAPCLR. A NMI request is only generated if the trap source was not disabled. Otherwise only the trap status flag is set but no NMI request is generated.

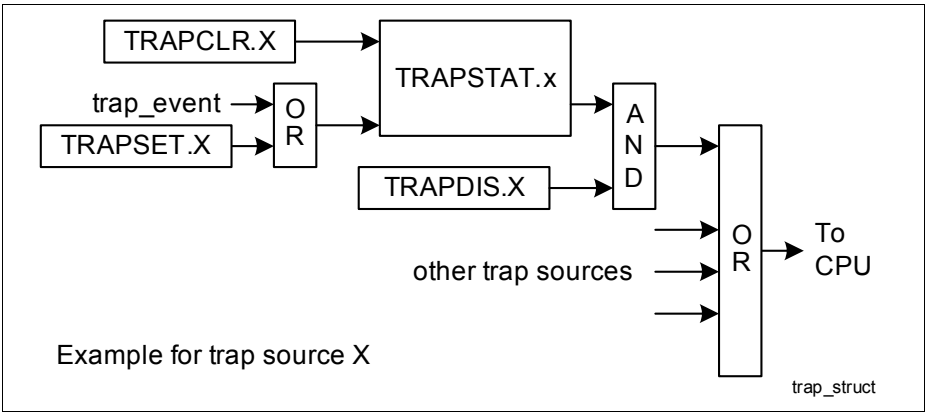


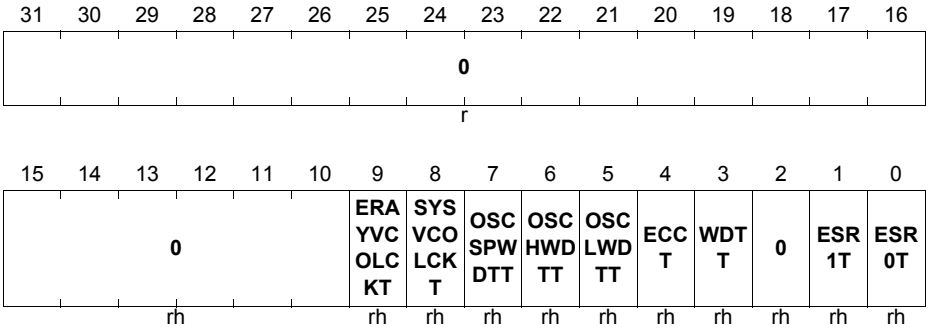
Figure 3-30 NMI Trap Generation

Handling NMI Traps

As an NMI trap is generated while the trap source is enable AND the trap status flag is set it is recommended to clear the trap status flag before the trap source is enabled. The trap status flag can be set before the trap source is enabled and simply enabling the trap source can result in unintended NMI traps. At the end of a NMI trap handing routine the trap status flag should be cleared.

3.11.1 Trap Control Registers

TRAPSTAT
Trap Status Register **(124_H)** **Reset Value: $0000\ 0100_H$**



Field	Bits	Type	Description
ESR0T	0	rh	**ESR0 Trap Request Flag** This bit is set if an ESR0 event is triggered and bit is TRAPDIS.ESR0T is cleared. 0_B No trap was requested since this bit was cleared the last time 1_B A trap was requested since this bit was cleared the last time This bit can be cleared by setting bit TRAPCLR.ESR0T. This bit can be set by setting bit TRAPSET.ESR0T.
ESR1T	1	rh	**ESR1 Trap Request Flag** This bit is set if an ESR1 event is triggered and bit is TRAPDIS.ESR1T is cleared. 0_B No trap was requested since this bit was cleared the last time 1_B A trap was requested since this bit was cleared the last time This bit can be cleared by setting bit TRAPCLR.ESR1T. This bit can be set by setting bit TRAPSET.ESR1T.

Field	Bits	Type	Description
WDTT	3	rh	**WDT Trap Request Flag** This bit is set if a WDT trap is indicated and bit is TRAPDIS.WDTT is cleared. 0_B No trap was requested since this bit was cleared the last time 1_B A trap was requested since this bit was cleared the last time This bit can be cleared by setting bit TRAPCLR.WDTT. This bit can be set by setting bit TRAPSET.WDTT.
ECCT	4	rh	**ECC Error Trap Request Flag** This bit is set if a memory ECC error is indicated and bit is TRAPDIS.ECCT is cleared. 0_B No trap was requested since this bit was cleared the last time 1_B A trap was requested since this bit was cleared the last time This bit can be cleared by setting bit TRAPCLR.ECCT. This bit can be set by setting bit TRAPSET.ECCT.
OSCLWDTT	5	rh	**OSCWDT Low Trap Request Flag** This bit is set if a oscillator WDT of the PLL detects a low event and bit is TRAPDIS.OSCLWDTT cleared. 0_B No trap was requested since this bit was cleared the last time 1_B A trap was requested since this bit was cleared the last time This bit can be cleared by setting bit TRAPCLR.OSCLWDTT. This bit can be set by setting bit TRAPSET.OSCLWDTT.

Field	Bits	Type	Description
OSCHWDTT	6	rh	**OSCWDT High Trap Request Flag** This bit is set if a oscillator WDT of the PLL detects a high event and bit is TRAPDIS.OSCHWDTT cleared. 0_B No trap was requested since this bit was cleared the last time 1_B A trap was requested since this bit was cleared the last time This bit can be cleared by setting bit TRAPCLR.OSCHWDTT. This bit can be set by setting bit TRAPSET.OSCHWDTT.
OSCSPWDTT	7	rh	**OSCWDT Spike Trap Request Flag** This bit is set if a oscillator WDT of the PLL detects a spike event and bit is TRAPDIS.OSCSPWDTT cleared. 0_B No trap was requested since this bit was cleared the last time 1_B A trap was requested since this bit was cleared the last time This bit can be cleared by setting bit TRAPCLR.OSCSPWDTT. This bit can be set by setting bit TRAPSET.OSCSPWDTT.
SYSVCOLCKT	8	rh	**SYSVCOWDT Trap Request Flag** This bit is set if a PLL VCO Loss-of-Lock event is triggered and bit is TRAPDIS.SYSVCOLCKT cleared. 0_B No trap was requested since this bit was cleared the last time 1_B A trap was requested since this bit was cleared the last time This bit can be cleared by setting bit TRAPCLR.SYSVCOLCKT. This bit can be set by setting bit TRAPSET.SYSVCOLCKT.

Field	Bits	Type	Description
ERAYVCOLCKT	9	rh	**ERAYVCOWDT Trap Request Flag** This bit is set if a PLL_ERAY VCO Loss-of Oscillator Lock event is triggered and bit is TRAPDIS.ERAYXVCOLCKT cleared. 0_B No trap was requested since this bit was cleared the last time 1_B A trap was requested since this bit was cleared the last time This bit can be cleared by setting bit TRAPCLR.ERAYVCOLCKT. This bit can be set by setting bit TRAPSET.ERAYVCOLCKT.
0	2, [15:10]	rh	**Reserved** Read as 0. This bit can be cleared by bit TRAPCLR.[x]. This bit can be set by bit TRAPSET.[x]. *Note: x = 2, [15:10].*
0	[31:16]	r	**Reserved** Read as 0.

TRAPSET
Trap Set Register **(128_H)** **Reset Value: 0000 0000$_H$**

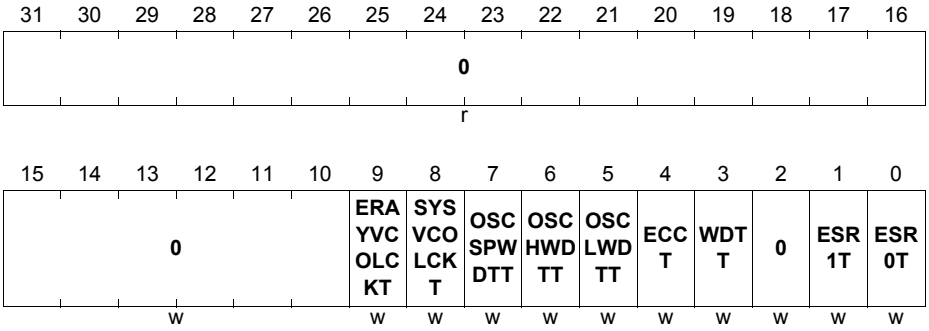
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0						ERAYVCOLCKT	SYSVCOLCKT	OSCSPWDTT	OSCHWDTT	OSCLWDTT	ECCT	WDTT	0	ESR1T	ESR0T
w						w	w	w	w	w	w	w	w	w	w

Field	Bits	Type	Description
ESR0T	0	w	**Set Trap Request Flag ESR0T** Setting this bit set bit TRAPSTAT.ESR0T. Clearing this bit has no effect. Reading this bit returns always zero.
ESR1T	1	w	**Set Trap Request Flag ESR1T** Setting this bit set bit TRAPSTAT.ESR1T. Clearing this bit has no effect. Reading this bit returns always zero.
WDTT	3	w	**Set Trap Request Flag WDTT** Setting this bit set bit TRAPSTAT.WDTT. Clearing this bit has no effect. Reading this bit returns always zero.
ECCT	4	w	**Set Trap Request Flag ECCT** Setting this bit set bit TRAPSTAT.ECCT. Clearing this bit has no effect. Reading this bit returns always zero.
OSCLWDTT	5	w	**Set Trap Request Flag OSCLWDTT** Setting this bit set bit TRAPSTAT.OSCLWDTT. Clearing this bit has no effect. Reading this bit returns always zero.
OSCHWDTT	6	w	**Set Trap Request Flag OSCHWDTT** Setting this bit set bit TRAPSTAT.OSCHWDTT. Clearing this bit has no effect. Reading this bit returns always zero.
OSCSPWDTT	7	w	**Set Trap Request Flag OSCSPWDTT** Setting this bit set bit TRAPSTAT.OSCSPWDTT. Clearing this bit has no effect. Reading this bit returns always zero.
SYSVCOLCKT	8	w	**Set Trap Request Flag SYSVCOLCKT** Setting this bit set bit TRAPSTAT.SYSVCOLCKT. Clearing this bit has no effect. Reading this bit returns always zero.
ERAYVCOLCKT	9	w	**Set Trap Request Flag ERAYVCOLCKT** Setting this bit set bit TRAPSTAT.ERAYVCOLCKT. Clearing this bit has no effect. Reading this bit returns always zero.

Field	Bits	Type	Description
0	2, [15:10]	w	**Reserved** Read as 0; have to be written with 0.
0	[31:16]	r	**Reserved** Read as 0; should be written with 0.

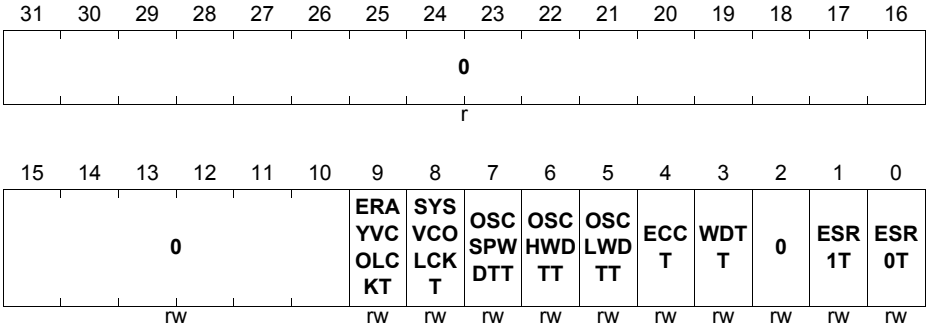
TRAPCLR
Trap Clear Register **($12C_H$)** **Reset Value: 0000 0000$_H$**



Field	Bits	Type	Description
ESR0T	0	w	**Clear Trap Request Flag ESR0T** Setting this bit clears bit TRAPSTAT.ESR0T. Clearing this bit has no effect. Reading this bit returns always zero.
ESR1T	1	w	**Clear Trap Request Flag ESR1T** Setting this bit clears bit TRAPSTAT.ESR1T. Clearing this bit has no effect. Reading this bit returns always zero.
WDTT	3	w	**Clear Trap Request Flag WDTT** Setting this bit clears bit TRAPSTAT.WDTT. Clearing this bit has no effect. Reading this bit returns always zero.
ECCT	4	w	**Clear Trap Request Flag ECCT** Setting this bit clears bit TRAPSTAT.ECCT. Clearing this bit has no effect. Reading this bit returns always zero.

Field	Bits	Type	Description
OSCLWDTT	5	w	**Clear Trap Request Flag OSCLWDTT** Setting this bit clears bit TRAPSTAT.OSCLWDTT. Clearing this bit has no effect. Reading this bit returns always zero.
OSCHWDTT	6	w	**Clear Trap Request Flag OSCHWDTT** Setting this bit clears bit TRAPSTAT.OSCHWDTT. Clearing this bit has no effect. Reading this bit returns always zero.
OSCSPWDTT	7	w	**Clear Trap Request Flag OSCSPWDTT** Setting this bit clears bit TRAPSTAT.OSCSPWDTT. Clearing this bit has no effect. Reading this bit returns always zero.
SYSVCOLCKT	8	w	**Clear Trap Request Flag SYSVCOLCKT** Setting this bit clears bit TRAPSTAT.SYSVCOLCKT. Clearing this bit has no effect. Reading this bit returns always zero.
ERAYVCOLCKT	9	w	**Clear Trap Request Flag ERAYVCOLCKT** Setting this bit clears bit TRAPSTAT.ERAYVCOLCKT. Clearing this bit has no effect. Reading this bit returns always zero.
0	2, [15:10]	w	**Reserved** Read as 0; should be written with 0.
0	[31:16]	r	**Reserved** Read as 0; should be written with 0.

TRAPDIS
Trap Disable Register **(130_H)** **Reset Value: 0000 FFFF$_H$**



Field	Bits	Type	Description
ESR0T	0	rw	**Disable Trap Request ESR0T** 0_B A trap request can be generated for this source 1_B No trap request can be generated for this source
ESR1T	1	rw	**Disable Trap Request ESR1T** 0_B A trap request can be generated for this source 1_B No trap request can be generated for this source
WDTT	3	rw	**Disable Trap Request WDTT** 0_B A trap request can be generated for this source 1_B No trap request can be generated for this source
ECCT	4	rw	**Disable Trap Request ECCT** 0_B A trap request can be generated for this source 1_B No trap request can be generated for this source
OSCLWDTT	5	rw	**Disable Trap Request OSCLWDTT** 0_B A trap request can be generated for this source 1_B No trap request can be generated for this source

Field	Bits	Type	Description
OSCHWDTT	6	rw	**Disable Trap Request OSCHWDTT** 0_B A trap request can be generated for this source 1_B No trap request can be generated for this source
OSCSPWDTT	7	rw	**Disable Trap Request OSCSPWDTT** 0_B A trap request can be generated for this source 1_B No trap request can be generated for this source
SYSVCOLCKT	8	rw	**Disable Trap Request SYSVCOLCKT** 0_B A trap request can be generated for this source 1_B No trap request can be generated for this source
ERAYVCOLCKT	9	rw	**Disable Trap Request ERAYVCOLCKT** 0_B A trap request can be generated for this source 1_B No trap request can be generated for this source
0	2, [15:10]	rw	**Reserved** Have to be written with 1.
0	[31:16]	r	**Reserved** Read as 0; should be written with 0.

3.12 Miscellaneous System Control Register

This section collects different register that serve various system aspects.

3.12.1 GPTA Input IN1 Control

In the TC1798, the input line IN1 of the GPTA module can be used to measure the baud rate of an ASC0 or ASC1 receiver input signal with GPTA. This feature is controlled by SYSCON.GPTAIS.

Table 3-21 GPTA0/GPTA1/LTCA2 Input Line IN1 Connections

SYSCON.GPTAIS	GPTA0/GPTA1/LTCA2 Input IN1 Connected to
00_B	P2.9 / IN1 (default after Application Reset)
01_B	P5.0 / RXD0A
10_B	P6.8 / RXD0B
11_B	P6.10 / RXD1B

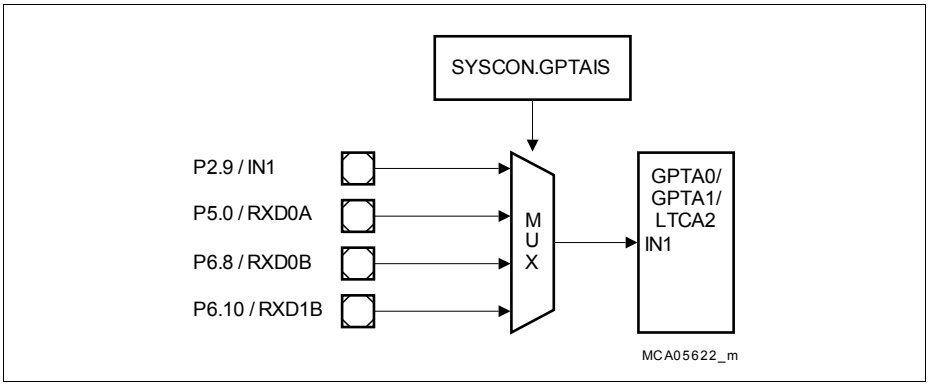
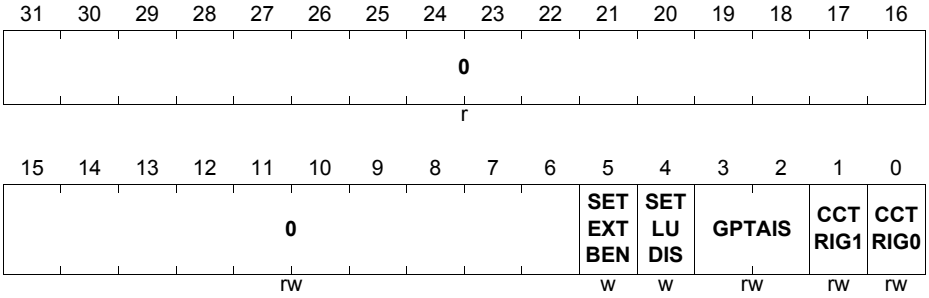


Figure 3-31 GPTA0/GPTA1/LTCA2 Input IN1 Control

3.12.2 System Control Register

This register controls various functionality used by the SCU but that are located outside of the module. Additionally some functions for other modules are included.

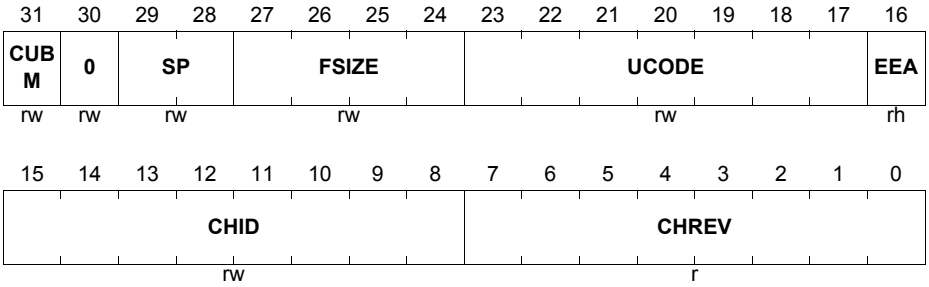
SYSCON
System Control Register **(040_H)** **Reset Value: 0000 0000_H**



Field	Bits	Type	Description
CCTRIGx (x = 0-1)	x	rw	**Capture Compare Trigger x** This bit is used to trigger the Synchronous Start feature of the CAPCOMs in the system.
GPTAIS	[3:2]	rw	**GPTA Input Select** This bit field selects the input that is used for IN1 of the GPTA module. For more information see either Section 3.12.1 or the GPTA chapter. 00_B IN0 is selected 01_B IN1 is selected 10_B IN2 is selected 11_B IN3 is selected
SETLUDIS	4	w	**Set Latch Update Disable** Setting this bit sets bit STSTAT.LUDIS. Clearing this bit has no effect. This bit reads always as zero.
SETEXTBEN	5	w	**Set External Boot Enable** Setting this bit sets bit STSTAT.EXTBEN. Clearing this bit has no effect. This bit reads always as zero.
0	[15:6]	rw	**Reserved** Should be written with 0.
0	[31:16]	r	**Reserved** Read as 0; should be written with 0.

3.12.3 Identification Registers

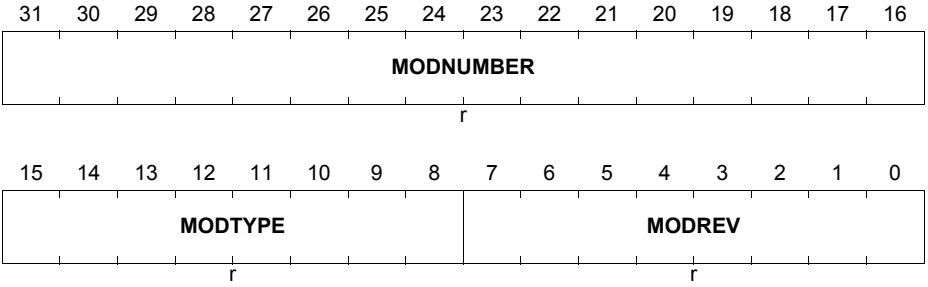
CHIPID
Chip Identification Register **(140_H)** **Reset Value: XXXX XXXX$_H$**



Field	Bits	Type	Description
CHREV	[7:0]	r	**Chip Revision Number** This bit field indicates the revision number of the TC1798 device. The value of this bit field is defined in the TC1798 Data Sheet.
CHID	[15:8]	rw	**Chip Identification Number** This bit field defines the product by a unique number. 98_H = 1798
EEA	16	rh	**Emulation Extension Available** Indicates if the emulation extension is available or not. 0_B EEC is not available 1_B EEC is available
UCODE	[23:17]	rw	**µCode Version** This bit field displays the Version x.y of the flash µCode.
FSIZE	[27:24]	rw	**Program Flash Size** this bit field indicates available program flash size for this device. Detailed information is shown in the Data Sheet.
SP	[29:28]	rw	**Speed** This bit field indicates the maximum allowed speed for the CPU of this device. Detailed information is shown in the Data Sheet.

Field	Bits	Type	Description
CUBM	31	rw	**Copper Bond Material** This bit indicates if copper was used for the bond wires. 0_B No copper was used 1_B Copper was used
0	30	rw	**Reserved** Have not to be written at all.

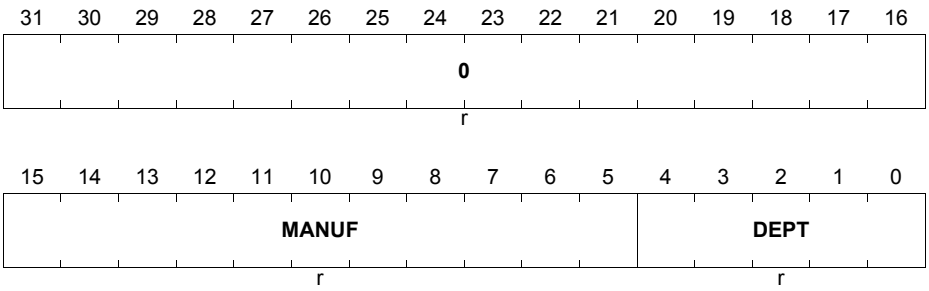
ID
Identification Register **(008_H)** **Reset Value: 0052 C0XX$_H$**



Field	Bits	Type	Description
MODREV	[7:0]	r	**Module Revision Number** This bit field indicates the revision number of the TC1798 module (01_H = first revision).
MODTYPE	[15:8]	r	**Module Type** This bit field is $C0_H$. It defines a 32-bit module
MODNUMBER	[31:16]	r	**Module Number** This bit field defines the module identification number.

MANID

Manufacturer Identification Register (144_H) **Reset Value: 0000 1820$_H$**



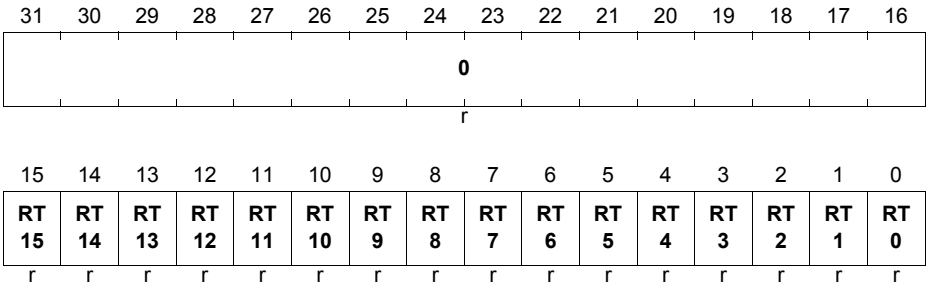
Field	Bits	Type	Description
DEPT	[4:0]	r	**Department Identification Number** = 00_H: indicates the Automotive & Industrial microcontroller department within Infineon Technologies.
MANUF	[15:5]	r	**Manufacturer Identification Number** This is a JEDEC normalized manufacturer code. MANUF = $C1_H$ stands for Infineon Technologies.
0	[31:16]	r	**Reserved** Read as 0.

The Redesign Tracing Register RTID provides a means of signalling minor redesigns that are not reflected in the CHIPID.CHREV bit field.

RTID

Redesign Tracing Identification Register

(148_H) **Reset Value: 0000 XXXX$_H$**



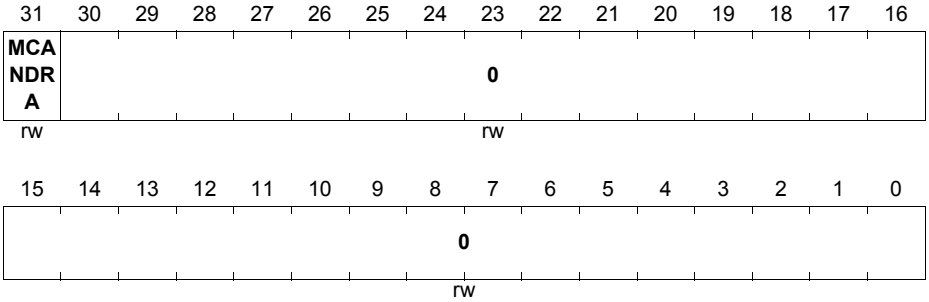
Field	Bits	Type	Description
RTx (x = 0-15)	x	r	**Redesign Trace Bit x** 0_B No change indicated 1_B A change has been made (without changing bit field CHIPID.CHREV). RTx can be used, e.g., for minor redesign stepping identification purposes.
0	[31:16]	r	**Reserved** Read as 0

Note: The RTID reset value for a major design step (without modifications) is 0000_H.

3.12.4 Memory Test Register

3.12.4.1 Register MEMTEST

MEMTEST
Memory Test Register **(160_H)** **Reset Value: $0000\ 0000_H$**



Field	Bits	Type	Description
MCANDRA	31	rw	**MCAN Direct RAM Access** 0_B Direct RAM access for the MCAN is not possible 1_B Direct RAM access for the MCAN is possible
0	[30:0]	r	**Reserved** Has to be written with 0.

3.12.5 SCU Kernel Registers

This section describes the kernel registers of the 32-bit SCU module. Most of 32-bit SCU kernel register names described in this section will be referenced in other parts of the TC1798 User´s Manual by the module name prefix “SCU_”.

SCU Kernel Register Overview

Table 3-22 Register Overview of SCU

Short Name	Long Name	Offset Addr.[1)]	Access Mode		Reset	Description See
			Read	Write		
–	Reserved	000_H - $00C_H$	BE	BE	–	–
OSCCON	OSC Control Register	010_H	U, SV	SV, E	System Reset	Page 3-31
PLLSTAT	PLL Status Register	014_H	U, SV	BE	System Reset	Page 3-33
PLLCON0	PLL Configuration 0 Register	018_H	U, SV	SV, E	System Reset	Page 3-35
PLLCON1	PLL Configuration 1 Register	$01C_H$	U, SV	SV, E	System Reset	Page 3-37
–	Reserved	020_H	BE	BE	–	–
PLLERAY STAT	PLL_ERAY Status Register	024_H	U, SV	BE	System Reset	Page 3-38
PLLERAY CON0	PLL_ERAY Configuration 0 Register	028_H	U, SV	SV, E	System Reset	Page 3-40
PLLERAY CON1	PLL_ERAY Configuration 1 Register	$02C_H$	U, SV	SV, E	System Reset	Page 3-42
CCUCON0	CCU Control Register 0	030_H	U, SV	SV, E	System Reset	Page 3-42
CCUCON1	CCU Control Register 1	034_H	U, SV	SV, E	System Reset	Page 3-45
FDR	Fractional Divider Register	038_H	U, SV	SV, E	System Reset	Page 3-51
EXTCON	External Clock Control Register	$03C_H$	U, SV	U, SV	System Reset	Page 3-49
SYSCON	System Control Register	040_H	U, SV	U, SV	System Reset	Page 3-182
CCUCON2	CCU Control Register 2	044_H	U, SV	SV, E	System Reset	Page 3-47

Table 3-22 Register Overview of SCU (cont'd)

Short Name	Long Name	Offset Addr.[1)]	Access Mode		Reset	Description See
			Read	Write		
–	Reserved	048_H - $04C_H$	BE	BE	–	–
RSTSTAT	Reset Status Register	050_H	U, SV	BE	Power-on Reset	Page 3-75
RSTCNTCON	Reset Counter Control Register	054_H	U, SV	SV, E	Power-on Reset	Page 3-78
RSTCON	Reset CON Register	058_H	U, SV	SV, E	Power-on Reset	Page 3-78
ARSTDIS	Application Reset Disable Register	$05C_H$	U, SV	SV, E	Power-on Reset	Page 3-80
SWRSTCON	Software Reset Configuration Register	060_H	U, SV	SV, E	Power-on Reset	Page 3-81
–	Reserved	064_H - 068_H	BE	BE	–	–
ESRCFG0	ESR0 Configuration Register	070_H	U, SV	SV, E	System Reset	Page 3-84
ESRCFG1	ESR1 Configuration Register	074_H	U, SV	SV, E	System Reset	Page 3-84
–	Reserved	078_H - $07C_H$	BE	BE	–	–
EICR0	External Input Channel Register 0	080_H	U, SV	U, SV	Application Reset	Page 3-105
EICR1	External Input Channel Register 1	084_H	U, SV	U, SV	Application Reset	Page 3-108
EIFR	External Input Flag Register	088_H	U, SV	U, SV	Application Reset	Page 3-112
FMR	Flag Modification Register	$08C_H$	U, SV	U, SV	Application Reset	Page 3-112
PDRR	Pattern Detection Result Register	090_H	U, SV	U, SV	Application Reset	Page 3-113

Table 3-22 Register Overview of SCU (cont'd)

Short Name	Long Name	Offset Addr.[1]	Access Mode		Reset	Description See
			Read	Write		
IGCR0	Interrupt Gating Register 0	094_H	U, SV	U, SV	Application Reset	Page 3-114
IGCR1	Interrupt Gating Register 1	098_H	U, SV	U, SV	Application Reset	Page 3-117
–	Reserved	$09C_H$	BE	BE	–	–
IOCR	Input/Output Control Register	$0A0_H$	U, SV	U, SV	System Reset	Page 3-85
OUT	Output Register	$0A4_H$	U, SV	U, SV	System Reset	Page 3-88
OMR	Output Modification Register	$0A8_H$	U, SV	U, SV	System Reset	Page 3-89
IN	Input Register	$0AC_H$	U, SV	BE	System Reset	Page 3-90
PMCSR	Power Management Control and Status Register	$0B0_H$	U, SV	U, SV	Application Reset	Page 3-123
–	Reserved	$0B4_H$ - $0BC_H$	BE	BE	–	–
STSTAT	Start-up Status Register	$0C0_H$	U, SV	BE	Power-on Reset	Page 3-126
STCON	Start-up Configuration Register	$0C4_H$	U, SV	ST	Power-on Reset	Page 3-128
–	Reserved	$0C8_H$ - $0CC_H$	BE	BE	–	–
ECCCON	ECC Control Register	$0D0_H$	U, SV	SV, E	Application Reset	Page 3-130
ECCSTAT	ECC Status Register	$0D4_H$	U, SV	BE	Application Reset	Page 3-132
ECCCLR	ECC Clear Register	$0D8_H$	U, SV	U, SV	Application Reset	Page 3-134

Table 3-22 Register Overview of SCU (cont'd)

Short Name	Long Name	Offset Addr.[1]	Access Mode		Reset	Description See
			Read	Write		
DTSSTAT	Die Temperature Sensor Status Register	$0E0_H$	U, SV	BE	Application Reset	Page 3-138
DTSCON	Die Temperature Sensor Control Register	$0E4_H$	U, SV	U, SV	Application Reset	Page 3-137
–	Reserved	$0E8_H$ - $0EC_H$	BE	BE	–	–
WDT_CON0	WDT Control Register 0	$0F0_H$	U, SV	U, SV	Application Reset	Page 3-149
WDT_CON1	WDT Control Register 1	$0F4_H$	U, SV	SV, E	Application Reset	Page 3-151
WDT_SR	WDT Status Register	$0F8_H$	U, SV	BE	Application Reset	Page 3-152
–	Reserved	$0FC_H$	BE	BE	–	–
EMSR	Emergency Stop Register	100_H	U, SV	SV, E	Application Reset	Page 3-157
–	Reserved	104_H - $10F_H$	BE	BE	–	–
INTSTAT	Interrupt Status Register	110_H	U, SV	BE	Application Reset	Page 3-160
INTSET	Interrupt Set Register	114_H	U, SV	U, SV	Application Reset	Page 3-162
INTCLR	Interrupt Clear Register	118_H	U, SV	U, SV	Application Reset	Page 3-164
INTDIS	Interrupt Disable Register	$11C_H$	U, SV	U, SV	Application Reset	Page 3-165
INTNP	Interrupt Node Pointer Register	120_H	U, SV	U, SV	Application Reset	Page 3-167
TRAPSTAT	Trap Status Register	124_H	U, SV	BE	System Reset	Page 3-172
TRAPSET	Trap Set Register	128_H	U, SV	SV, E	System Reset	Page 3-175

Table 3-22 Register Overview of SCU (cont'd)

Short Name	Long Name	Offset Addr.[1]	Access Mode		Reset	Description See
			Read	Write		
TRAPCLR	Trap Clear Register	$12C_H$	U, SV	U, SV	System Reset	Page 3-177
TRAPDIS	Trap Disable Register	130_H	U, SV	SV, E	Application Reset	Page 3-179
–	Reserved	134_H - $13F_H$	BE	BE	–	–
CHIPID	Chip Identification Register	140_H	U, SV	ST	System Reset	Page 3-183
MANID	Manufacture Identification Register	144_H	U, SV	BE	System Reset	Page 3-185
RTID	Redesign Trace Identification Register	148_H	U, SV	BE	System Reset	Page 3-185
–	Reserved	$14C_H$ - $15F_H$	BE	BE	–	–
MEMTEST	Memory Test Register	160_H	U, SV	SV, E	System Reset	Page 3-187
–	Reserved	164_H - $1EF_H$	BE	BE	–	–
SRC3	Service Request Control Register 3	$1F0_H$	U, SV	SV	Application Reset	Page 3-169
SRC2	Service Request Control Register 2	$1F4_H$	U, SV	SV	Application Reset	Page 3-169
SRC1	Service Request Control Register 1	$1F8_H$	U, SV	SV	Application Reset	Page 3-169
SRC0	Service Request Control Register 0	$1FC_H$	U, SV	SV	Application Reset	Page 3-169

1) The absolute register address is calculated as follows:
Module Base Address + Offset Address (shown in this column)

3.12.6 SCU Address Area

Table 3-23 Registers Address Space - SCU Kernel Registers

Module	Base Address	End Address	Note
SCU	$F000\ 0500_H$	$F000\ 06FF_H$	-

4 On-Chip System Buses and Bus Bridges

The TC1798 has two independent on-chip buses:

- Shared Resource Interconnect (SRI)
- System Peripheral Bus (SPB)

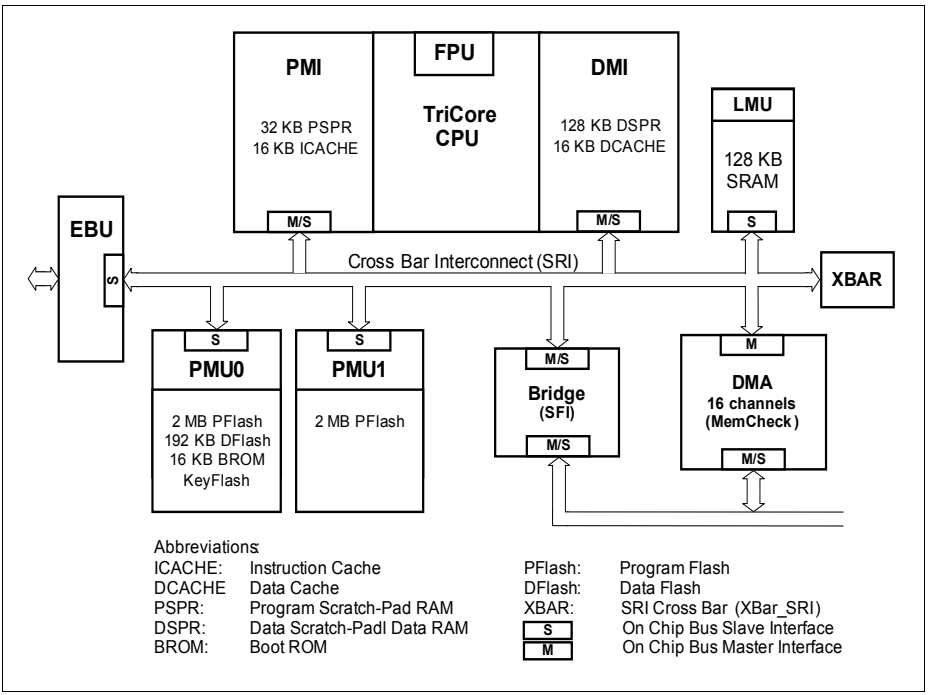


Figure 4-1 On Chip Buses in TC1798 Processor Subsystem

The SRI connects the TriCore CPU to its local resources for instruction fetches and data accesses.

The SPB is accessible by the CPU via the SRI to FPI Bridge (SFI).

4.1 What is new

Major differences of the TC1798 On Chip Bus System architecture compared to AudoF/AudoS and other TC1.3.x based products:

- The TC1798 is based on two on chip busses (SRI, SPB). The Local Memory Bus (LMB) was replaced by an Shared Resource Interconnect (SRI / SRI Crossbar, **Chapter 4.2**)
- The LBCU functionality is now covered by the SRI Crossbar (XBar_SRI)

- The LMB to FPI Bridge (LFI) was replaced by the SRI to FPI Bridge (SFI, **Chapter 4.3**)
- The SFI is fully transparent regarding address and master TAG ID
- The on chip bus architecture was adapted to the TC1.6 (CPS registers are now accessed via PMI SRI slave, additional LMU peripheral connected to SRI)
- The table On Chip Bus Master TAG Assignments was adapted (SDMA TAG added, LFI TAGs removed, **Page 4-103**)

4.2 SRI Crossbar (XBar_SRI)

4.2.1 Introduction

The Shared Resource Interconnection (SRI) is the new high speed system bus for TriCore1.6 CPU. The central module of the interconnect is the XBar_SRI which connects all components in one SRI system. The XBar_SRI handles, arbitrates and forwards the communication between all connected SRI-Master and SRI-Slave peripherals.

The XBar_SRI supports parallel transaction between different SRI-Master and SRI-Slave peripherals. It supports also pipelined requests from the SRI-Master interfaces and pipelined address phases to the connected SRI-Slave interfaces.

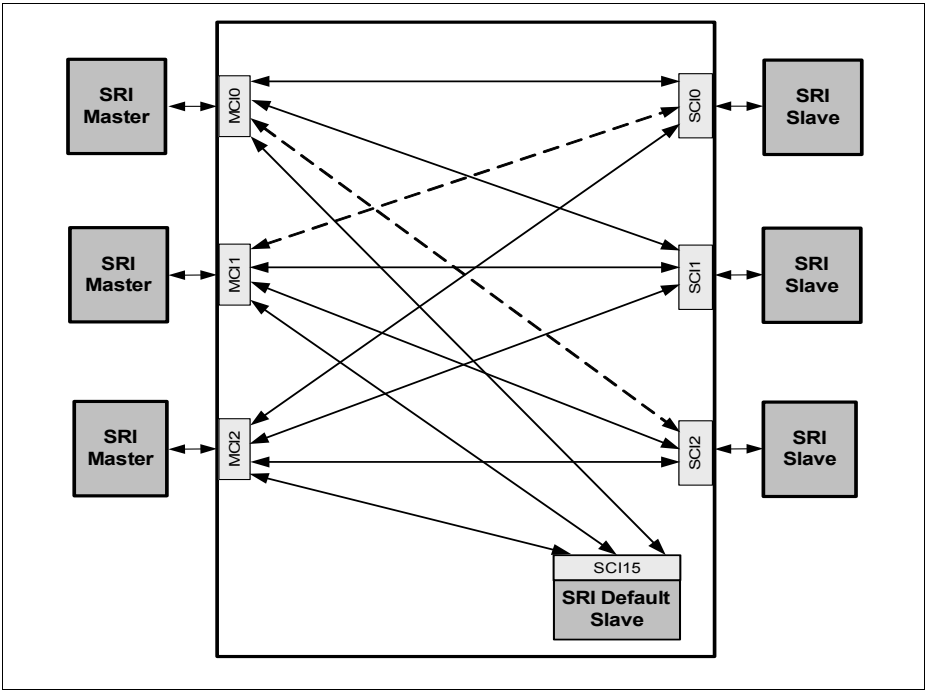


Figure 4-2 XBAR_SRI point to point connection scheme

The XBar_SRI provides SRI Slave Interfaces (SCIx) to connect SRI Slave modules and SRI Master Interfaces (MCIx) to connect SRI Master models to the XBar_SRI. The XBar_SRI includes an Default SRI Slave that provides access to the XBar_SRI control registers and that takes over all SRI transactions to address outside the connected SRI

Slave address ranges. The XBar_SRI includes also one Arbiter module per connected SRI slave module and the infrastructure for the enabled read/write data paths. Each connected SRI slave module as well as the default slave have an related arbiter module within the XBar_SRI.

Please note that only these SRI-Master <-> SRI-Slave connections are implemented that are required for the system functionality (example: connection between PMI Master and PMI Slave is not implemented, see also **Table 4-8**).

For performance optimization the XBar_SRI includes arbitration schemes that allows to configure SRI master priorities for each SRI slave individually (arbiter functionality). For debug support on system level the XBar_SRI includes debug support for SRI-Error and SRI-Transaction ID errors (local SRI slave module support in the related arbiter, global control in the Default Slave) .

Table 4-1 SRI Bus Terms

Term	Description
Agent	An SRI agent is any master or slave device which is connected to the SRI Bus.
Master	An SRI master device is an SRI agent which is able to initiate transactions on the SRI.
Slave	An SRI slave device is an SRI agent which is not able to initiate transactions on the SRI. It is only able to handle operations that are dedicated to it by SRI CrossBar (XBar_SRI).
XBar_SRI	The SRI CrossBar (XBar_SRI) provides the interconnects between connected Master and Slaves. The XBar_SRI includes arbitration mechanisms and debug capabilities. The XBar_SRI has 16 Master Connection Interfaces (MCI0 - MCI15) to connect SRI master devices to it and 15 Slave Connection Interfaces (SCI0 - SCI14) to connect SRI slave devices to it.
MCI	Each Master is connected via one Master Connection Interface (MCI x, x = 0 ...15). The XBar_SRI control registers include control and debug informations related to the Master Connection Interfaces MCI x (x = 0 ... 15).
SCI	Each Slave is connected via one Slave Connection Interface (SCI x, x = 0 ...14). The XBar_SRI control registers include control and debug informations related to the Slave Connection Interfaces SCI x (x = 0 ... 14). The XBar_SRI default slave is connected to SCI 15.

4.2.1.1 XBar_SRI Features

XBar_SRI feature overview:

- Single/Block Data Read Transaction Support (8/16/32/64 Bit)
- Single/Block Data Write Transactions Support (8/16/32/64 Bit)
- Read Modify Write Support
- Supports pipelined requests from SRI master peripherals
- Supports pipelined address phases to SRI slave peripherals
- Single arbiter module for each connected Slave device
- Arbitration priority scheme can be configured for each Slave device individually
- Flexible arbitration schemes (priority, two round robin groups, starvation prevention)
- Breakpoint signal generation based on SRI transactions (OCDS Level 1)
- Configurable MCDS trace interface
- Information integrity support for SRI address phase and read data path through the SRI interconnect.

4.2.2 SRI Transactions

Each SRI transaction consists of:

- one request phase
- one or multiple data phases if not finished with error acknowledge

Due to the point to point nature master/slave connections of the XBar a master that is requesting for access to one SIR slave peripheral is providing all transaction information in parallel with the request. This means that there are no separate on chip bus request and on chip bus address phases. An SRI request/address phase consists of:

- request signal
- lock signal (indicating a read modify write transaction)
- 32-bit address
- 4-bit SRI Op-Code (kind of single data or burst transaction)
- read/write signal (read, write or read modify transaction)
- supervisor mode signal
- Transaction ID (consists of a unique 6-bit Master TAG ID and a 2 bit running number increased for each new transaction of this master)
- 8-bit address phase ECC (covering all address phase signals with the exception of request and grant)
- one or multiple data phases if not finished with error acknowledge

After the request for a slave access was granted by the related XBar_SRI arbiter module, the transaction can be either finished with error acknowledge or with the read/write data phases as defined during the request/address phase.

Each data phase ends with the transmission of data phase informations including:

- Read or Write Transaction ID (must be equal to the related Transaction ID otherwise the address phase is invalid)

- 8-bit read/write data ECC (covering the 64-bit read/write data and the bits [23:3] of the related address.
- 64 bit read or write data. In case of an 8-bit, 16-bit or 32-bit read/write transaction the unused bits are filled with ´don't care´ data. The read/write data ECC covers the 64 data bits as transferred (incl. the possible don't care data).

4.2.3 SRI Op-Codes

The SRI Op-Code defines for a SRI transaction the number of data phases, the addressing mode in case of a multi beat transaction and valid bytes in case of a single data transaction.

Table 4-2 Operation Code Encoding

sri_opc[3:0]	Identifier	Description
0000	SDTB	Single Data Transfer Byte (8 bit)
0001	SDTH	Single Data Transfer Half-Word (16 bit)
0010	SDTW	Single Data Transfer Word (32 bit)
0011	SDTD	Single Data Transfer Double-Word (64 bit)
0100	-	Reserved
0101	-	Reserved
0110	-	Reserved
0111	-	Reserved
1000	BTR2	Block Transfer Request (2 transfers) Wrap Around Address Mode is used.
1001	BTR4	Block Transfer Request (4 transfers) Wrap Around Mode is used.
1010	BTRL2[1)]	Block Transfer Request (2 transfers) Linear Address Mode is used.
1011	BTRL4[1)]	Block Transfer Request (4 transfers) Linear Address Mode is used.
1100	-	Reserved
1101	-	Reserved
1110	-	Reserved
1111	-	Reserved

1) The SRI implementation in the TC1798 does not support bursts with linear addressing modes.

4.2.4 SRI Error Conditions

The sri_err_n signal is used by the slave during a transaction to signal the corresponding master that an error has happened which results in an immediate termination of the current transaction. Errors during transaction are tracked by the XBar_SRI and are signalled to via an interrupt and directly to the SMU.

Only the following error conditions are supported and recognized by SRI slaves:

- access level is incorrect (user/supervisor)
- unmapped address access from an SRI master[1)]
- unsupported op-code
- reserved op-code

An SRI error can be generated by the application SW e.g. with an access to a reserved address (see chapter Memory Map):

4.2.5 SRI Transaction ID Error Conditions

Transaction ID is an identifier connected to all phases of a transaction in order to make the transaction unique in the SRI system during the transactions live time.

The transaction ID is used by SRI masters and slaves to identify problems in the SRI system that results in data packets received by a master or slave that do not match the corresponding arbitration/address phase. If the read/write transaction identifier doesn't match with the previous send transaction identifier in the address phase, this is identified as a transaction ID error and tracked by the XBar_SRI.

In situations where at the data source side (master for write transactions, slave for read transactions) a data phase has to be invalidated (e.g. detection of an not correctable SRAM ECC error) and invalid transaction ID is send in order to invalidate the data phase.

An SRI Transaction ID error condition can be generated by injecting an non correctable error into one of the SRAMs (e.g. CPU Instruction Scratch Pad SRAM) and than reading the corrupted data by a CPU.

1) The accesses to unmapped slaves is checked by a default slave.

4.2.6 Operational Overview

This chapter describes the functionality of the XBar_SRI module in order to enable the user to configure the XBar_SRI control registers and to use the XBar_SRI debug resources.

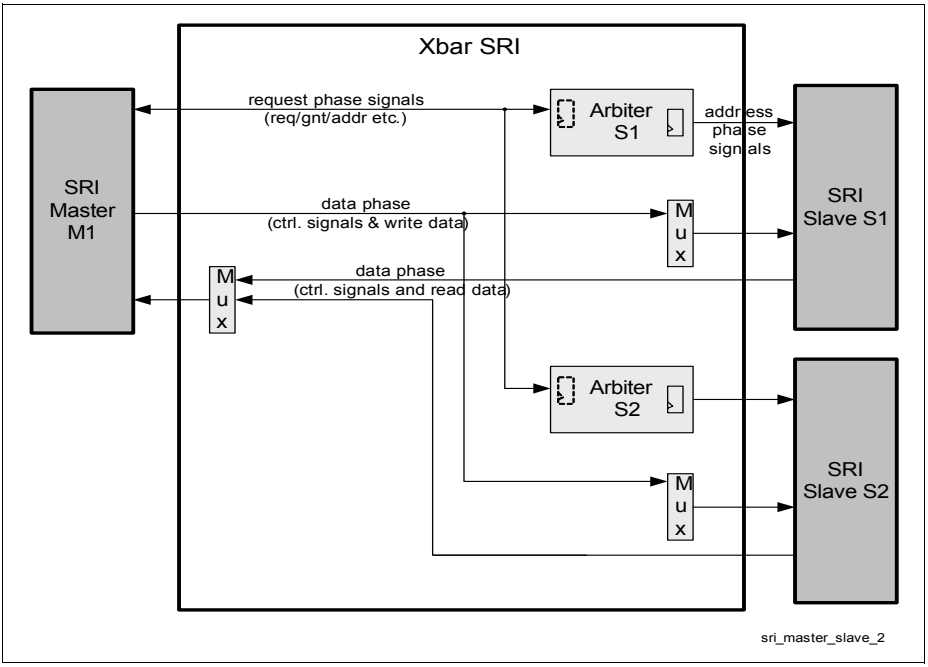


Figure 4-3 XBAR_SRI connections between SRI Master and SRI Slaves

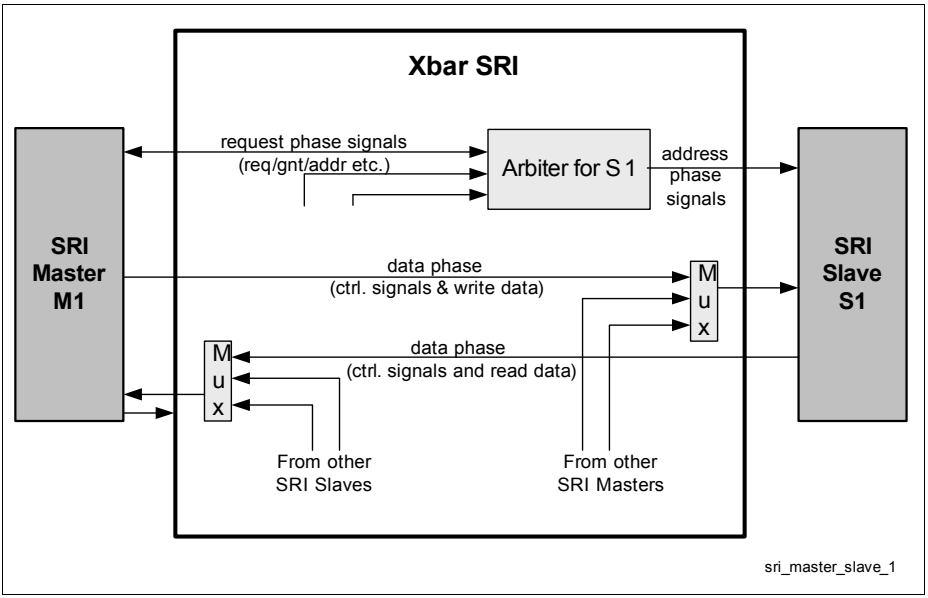


Figure 4-4 XBAR_SRI connections between SRI Slave and SRI Master modules

4.2.6.1 Functional Blocks

The XBar_SRI represents the highest level of the hierarchical SRI-Bus system. Since, it is closest to the TC1.6 core, peripherals critical to CPU performance can be attached to it.

The XBar_SRI module is partitioned into blocks for arbitration and data path control which are necessary for each XBar_SRI master- or slave interface and one block that covers the default slave - and debug functionality.

The XBar_SRI module can handle and process several transaction of different master in parallel if the masters requests different slaves.

XBar_SRI Master Connection Interface (MCI)

Each SRI master module in the system is mapped to one or more XBar_SRI Master Connection Interfaces (MCI). Each MCI is related within the XBAR_SRI module to a default arbitration priority and to register control bits and register control bit fields. So each SRI master in the system is mapped to an XBar_SRI internal default arbitration priority and to master related control register bits and bit fields via its MCI number (see also see also **Table 4-4** and **Table 4-6**).

XBar_SRI Slave Connection Interface (SCI)

Each SRI slave module in the system is mapped to one XBar_SRI Slave Connection Interfaces (SCIx). Each SCI is related within the XBAR_SRI module to one arbiter module with its arbiter module control register and to register control bits and register control bit fields related to this SCIx. So each SRI slave module in the system is mapped to an XBar_SRI internal arbiter module and to slave related control register bits and bit fields via its SCI number (see also see also **Table 4-7**).

XBar_SRI Arbiter

Each XBar_SRI slave connection interface is mapped to exactly one dedicated instantiation of the slave arbiter module in the XBar_SRI. This module includes all required functionality for the following tasks:

- Arbitration: the module includes all required functionality for the arbitration. This includes SRI address decoding, SRI request arbitration, SRI request starvation algorithm, SRI address phase generation and control registers for the priority of the connected master connection interfaces and an FSM to detect the end of the current SRI transaction.
- Debugging: the module tracks the SRI transactions to the dedicated slave connection interface for SRI errors. The transaction information of the first transaction where the SRI protocol error is captured in arbiter internal control registers.
  The module tracks the requests from all masters to detect starvation of masters in the arbitration rounds.
- Error signalling: The first SRI error or starvation error is signalled to the default slave module via two sideband signals.
- XBar_SRI control bus interface: the module has a slave interface to the XBar_SRI control bus. The slave arbiter decodes the address of each new control bus transaction and, if addressed, processes the read/write transaction to the module internal control registers.

Default Slave

The XBar_SRI default slave module is a XBar_SRI internal SRI slave module with its own, dedicated arbiter module inside the XBar_SRI. For accesses to the XBar_SRI control registers only SRI single data transactions of word size are supported. Any other op-code that is SRI protocol legal is not supported by the default slave module. Such transactions are acknowledged with an error by the default slave to the SIF_SRI. The default slave module includes all required functionality for the following tasks:

- As a SRI default slave, it deals with all transactions that are directed to a nonexisting slave in the SRI system as it is described in the SRI protocol. The purpose of the SRI default slave in that situation is to guarantee a defined behavior by terminating these SRI transactions with an error.

- The XBar_SRI default slave module is the SRI interface to all XBar_SRI internal diagnostic- and control registers.
- The XBar_SRI default slave module samples the mci_id_err_n and sci_id_err_n signals from all XBar_SRI master and slave connection interface modules. If the default slave module detects mci_id_err_n and sci_id_err_n pulses it generates an interrupt to the system. The sampling of each mci_id_err_n and sci_id_err_n signal from an arbiter can be disabled via the default slave interrupt control register IDINTEN.
- The XBar_SRI default slave module includes the interrupt node control structure and the corresponding control register.

4.2.7 Functional Overview

4.2.7.1 Arbitration Block

The arbiter has access to all arbitration-/address phase signals from the master connector interfaces he is enabled for, therefore he sees requests from all master connector interfaces in parallel.

In order to check if a master request is addressed to 'its' slave connector interface for the next transaction the arbiter checks if the address transmitted together with the request from the master matches with the allocated address area of this slave via address decoding. Due to the fact that a master can access any slave for a transaction all arbiters of the XBar_SRI are checking the requested address from a requesting master in parallel.

Due to the fact that multiple masters can request for one slave in parallel, each slave has to decode the addresses from all the master connector interfaces it is enabled for in parallel.

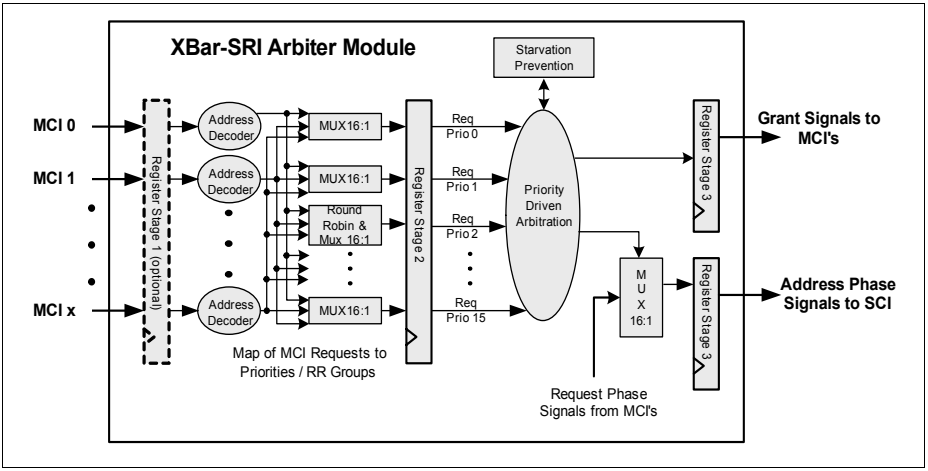


Figure 4-5 XBAR_SRI arbiter scheme

Address Map Checking

The arbiter performs the address comparison for all pending requests from the connected SRI master modules to its slave module in parallel.

Arbitration

A transaction request from a master that matches the address area of a slave connection interface takes part in the next arbitration cycle.

The arbitration is divided into two levels:

- priority driven arbitration
- arbitration within round robing groups (priority 2 and 8)

After reset each enabled master connector interface has a unique priority for the arbiters by default see (also see also **Table 4-4**). The priorities and the priority algorithm of the master connection interfaces can be programmed for each arbiter individually. The programming of the master priorities can be done by SRI read/write transaction via the default slave module.

The highest priority for an arbiter is 0 and the lowest is 15.

According to the transaction rules described in the SRI protocol specification the arbiter asserts the sri_gnt_x signal to grant the slave to this winning master.

In parallel - or after granting the master, the arbiter sends the address phase for the next transaction to the slave by propagating all necessary informations via the slave connection interface to the slave. The arbiter sends the address phase in parallel with the grant or delayed depending on the address phase pipeline status of the corresponding SRI slave.

For debug purposes, the arbiter samples all necessary transaction informations and provides them to the XBar_SRI default slave module if an SRI error happened and the protocol error feature was enabled.

Arbitration Algorithms

The arbiter related to a slave connection interface (SCI) can be connected to all master connection interfaces (MCI), see also **Chapter 4.2.8.3**. The priority of each MCI can be controlled via the arbiter priority registers (PRIOx). The priority of a master is defined by 4 bit field in the PRIOL / PRIOH register that is related to this master / its MCI number. This can be configured individually for each arbiter so the same master can be handled with different priorities for accesses to different slaves. After reset, each priority register has a default value, which means that each MCI has a unique default priority.

Please Note:

It must be ensured that two enabled masters don’t have the same priority, with the exception of priority 2 and priority 8 (round robin group priorities).

For changing the priorities during runtime (switching the priorities), all master connection interfaces that should be remapped have to be mapped to the round robin group priorities (2 / 8) before mapping them to their new priorities can be done. This will prevent situations where two masters have the same priority but not a round robin one.

Priority Driven Arbitration

The general arbitration algorithm is priority driven where priority 0 is the highest priority and 15 the lowest one. If multiple masters are requesting for one slave, the master with the highest priority will win the next arbitration round (see also 'starvation prevention').

Round Robin Groups

The arbiter arbitrates in general priority driven, where Priority 2 and priority 8 contain a second 'arbitration' layer. Both priorities can be used as round robin priorities for a group of max. 8 MCI's each. If only one master is mapped to a round robin group priority, the master's request will be treated as normal master request with the priority of the round robin group. If more than one master is mapped to the priority of a round robin group, the requests of the mapped masters will be handled by the round robin algorithm, the winning request of the round robin group arbitration has the priority of the round robin group within the priority driven arbitration.

After the winner of a round robin group is granted, the round robin group starts with a new arbitration round which means the requesting MCI's of the round robin group with the next highest MCI ID number will win the next round robin arbitration round. If there is no requesting MCI with a higher ID number in the round robin group, the algorithm will start with the MCI with the lowest MCI ID number that is mapped to the group, going to the next higher MCI ID number and so on.

Request Latency

If no other request is pending, a request from an MCI has a latency of 1 clock cycle, starting with the detection of the SRI master request on the bus, ending with the SRI grant to the requesting MCI and the SRI address phase to the addressed SCI.

Usually address decoding, round robin arbitration, priority driven arbitration and starvation prevention will be done in one clock cycle.

Table 4-3 XBar_SRI Request Latency

Clock Cycle Nr.:	Task(s)
0 (Default Slave)	sri_req_n is sampled at XBar_SRI MCI (Only valid for access to the XBar_SRI control registers)
1	address decoding, mapping of MCI's to priorities / round robin groups and starvation prevention. Round robin arbitrations, priority driven arbitration, mux request phase signals to the address phase registers masking sri_req_n from MCIx after granting the MCIx
2	sri_gnt_n to the requesting MCI, SRI address phase to SCI.

Grant -> New Request Latency (Request Dead Time)

After an MCI was granted, it takes 2 clock cycles before a new request from the same MCI will participate in a new arbitration round even when the SRI master has requested permanently. This request dead time is a result of the synchronous sri_req_n de-assertion and the XBar_SRI request latency.

Default MCI x Priorities after Reset

After Reset each Master has a default priority which is equal to the number of the Master Connection Interface (MCI x, x = 0 ... 15) it is connected to. MCI0 is configured with the highest priority and MCI15 with the lowest priority. **Table 4-4** shows the default priority of the MCI with the related coding in the **XBAR_PRIOLx (x = 3-6)** registers. After reset, the priority scheme of the MCIs can be re-configured via the **XBAR_PRIOLx (x = 3-6)** registers, for each SCI (accesses to the Slave connected to an SCI) individually.

Table 4-4 Default MCI Priority in the XBar_SRI Arbiters

Priority	Coding	Round Robin Group	Default Mapping:	Comments
0	0000	-	MCI 0	
1	0001	-	MCI 1	
2	0010	Yes, max 8 master	MCI 2	Maximal 8 MCI can be mapped to the priority 1 e.g. can have the prio ’0001’.
3	0011	-	MCI 3	
4	0100	-	MCI 4	
5	0101	-	MCI 5	
6	0110	-	MCI 6	
7	0111	-	MCI 7	
8	1000	Yes, max. 8 master	MCI 8	Maximal 8 MCI can be mapped to the priority 8 e.g. can have the prio ’1000’.
9	1001	-	MCI 9	
10	1010	-	MCI 10	
11	1011	-	MCI 11	
12	1100	-	MCI 12	
13	1101	-	MCI 13	
14	1110	-	MCI 14	
15	1111	-	MCI 15	

Starvation Prevention

Starvation can occur when masters with high priority continuously request a dedicated slave, preventing other masters with lower priority from getting access to this slave. To prevent such a situation, a starvation counter has been implemented in each arbiter. This mechanism allows the promotion of weak masters.

Each time the starvation counter in a slave module has and underflow, all pending requests to this arbiter will be entered in the arbiters request list. This even applies to all masters mapped to a round robin group.

Next time when the starvation counter has an underflow, the masters of this request list will be entered in the arbiters request promotion list if:

- The request was not granted during the last starvation period

The masters in that request promotion list will be the next to be granted independent of their priorities. The masters in the request promotion list will be granted one after the other, starting with the master which has the lowest MCI number in this list if there are more than one. The master promotion list has the highest priority within the arbiters main arbitration algorithm, therefore all masters in the promotion list will be granted before the arbiter switches back to its 'normal' arbitration. A master is removed from both lists when it is granted.

If several masters are mapped to a round robin priority, all masters of that round robin arbitration round will be entered in the request list/request promotion list when not granted.

The value controlling the counter period is programmable. After reset the starvation counter is disabled and has a value of zero. On a starvation counter underflow it is reloaded with the content of the arbiter control register ARBCON.SPC. An underflow occurs in the clock cycle when the counter tries to count down from zero.

The number of arbitration cycles a master must wait for the slave varies. But it's guaranteed to be no more than 2 $\times$ ARBCON.SPC until the master is promoted to the request promotion list.

Each time there is an underflow it is checked if there are any masters in the request promotion list that were not granted since the last underflow. This can happen if there are to many/to long transactions to be promoted compared to ARBCON.SPC value. In this case an error is generated via the xcb_sc_err_n signal to the default slave if the feature was enabled (bit ARBCONx.SCERREN set).

If currently a RMW transaction is processed the starvation counter is stopped before the next overflow. The starvation counter is released again after the address phase of the write part is generated or an error for the RMW transaction was received.

If currently a Read-Modify-Write (RMW) transaction is processed by the slave the starvation protection counter is stopped until this RMW is finished.

4.2.7.2 Default Slave

The default slave serves three features in the XBar_SRI implementation:

Control and Configuration Registers Interface

The XBar_SRI default slave module handles all read and write transactions to the debug- and control registers of the XBar_SRI. For this purpose, the default slave module has its own address space which must be mapped into the system address space by an address decoder, provided by the customer.

For a detailed description of the registers see **Chapter 4.2.9**.

Non Existing Addresses

The XBar_SRI internal default slave module has its own arbiter module.

If an SRI master sends a request with a non existing address[1)] to the XBar_SRI, the transaction will be directed to the default slave. The default slave finishes the transaction with error following the SRI protocol rules, which activates the error tracking mechanism of the arbiter. As a result of the error, the default slave module signals this incorrect behavior to the system by generating an interrupt.

A write from an SRI master to a non existing address on the System Peripheral Bus (SPB) will be handled by the Bus Control Unit on the SPB only. A read from an SRI master to a non existing address on the SPB will be handled by the by the Bus Control Unit on the SPB and also captured by the XBar_SRI arbiter as it will see the transaction as read transaction finished with Error Acknowledge.

Error Handling

If an arbiter detects an SRI protocol error during a transaction with a corresponding slave the involved arbiter samples all relevant information of the transaction in the arbiter internal diagnostic registers (ERRADDRx and ERRx) and signals this event via xcb_sri_err_n or xcb_sri_err_d_n sideband signal to the default slave module.

Note: The two error registers ERRx and ERRADDRx in each arbiter are updated with the content of the currently processed transaction in the data phase. The registers are only updated if they are not locked due to a pending protocol error and sri_ready_n was asserted in parallel with sri_err_n deasserted.

The error capture registers in the arbiter can't be changed until the interrupt was acknowledged to the slave arbiter module (set the ARBCON.INTACK) via the default slave.

1) non existing address = all Reserved address ranges described in the Memory Map chapter

The stored informations can be read from the default slave module with SRI single data read transactions, the acknowledge can be sent to the default slave via a write to a specific address.

This can result in a loss of interrupt data information of the same source beyond the first until the write was processed but as all SRI errors must be analyzed and fixed before the product will work, these kind of errors can be analyzed one after the other.

In case that a master or a slave signals an ID error to the XBar_SRI the default slave marks the source of the ID error by setting the according bit in register IDINTSAT if this feature was enabled for that specific master and/or slave interface.

As a result, the default slave generates an interrupt to the system.

Note: While a status bit for a error source is set in either the INTSAT or IDINTSAT register a new error from this particular source doesn't generate a new interrupt.

1. *Each participant in the SRI-Bus system has three interrupt sources; protocol errors, ID errors and time-out due to starvation. All error from the SRI-Bus components are combined in the single SRN of the XBar_SRI.*

Each arbiter has two 32 bit registers containing the error information. This registers are accessed as all other registers, via the default slave module.

The default slave module has one service request node (SRN) to start interrupts for detected SRI errors. Protocol errors, starvation errors as well as ID errors are handled together by this node.

4.2.7.3 SRI ECC Error Handling

The SRI protocol provides ECC protection for the:

- Address phase of an SRI transaction
- Read Data transmitted during read data phases

If an SRI slave detects an SRI address phase ECC error it finishes the transaction with SRI error acknowledge and does not further process it (see also **Chapter 4.2.7.4**).

It can happen that a data during a transaction shows an ECC error inside the data source peripheral (master during write, slave during read). Example: A burst read transaction from a memory slave peripheral where the second, third or forth data taken from the SRAM shows inside the slave/master an ECC error. In this situation a slave can finish a read transaction with error acknowledge (if the error is detected before the first data phase) or a slave / master can invalidate the related data phase with an invalid read / write transaction ID error (see also **Chapter 4.2.7.4**).

A master that detects an SRI read data ECC error is free to decide how it handles the situation:

- PMI and DMI: a bus error trap will be generated but only if and when a received 64 bit read data is really used by the CPU. This as PMI / DMI can read complete cache

lines (4x64 bit) where the critical 64 bit is used, the other 3 x 64 bit are speculative reads and might not be used by the CPU later.
- DMA: the DMA ignores read data ECC in this product. Background is that the SRI ECC was introduced for the safe instruction fetch path.
- SFI: the SFI SRI master ignores the read data ECC. Background is that the SRI ECC was introduced for the safe instruction fetch path.

Most of the SRI peripherals are signalling detected SRI ECC errors also to the SCU:

- PMI and DMI: detected SRI ECC errors are signalled to the SCU via the still available ECC error signals (to the SCU). More details (SRI Address Phase ECC Error or SRI ECC Read Data Error) can be found in the PMI / DMI control registers.
- EBU: signals detected SRI Address Phase ECC Errors to the SCU.
- LMU: signals detected SRI Address Phase ECC Errors to the SCU. More details (SRI Address Phase ECC Error or SRAM ECC Error) can be found in the LMU control registers.
- PMU and SFI SRI slave: no signalling of detected SRI Address Phase ECC Errors to the SCU.

4.2.7.4 Error Tracking Capability

The XBar_SRI tracks all SRI transactions for SRI protocol errors. Additionally it tracks informations about starvation errors and SRI transaction ID errors. This is done by all arbiters and the default slave in parallel as the XBar_SRI supports the processing of multiple transactions from master and slaves in parallel which can result in parallel events at different slave connector interfaces.

For this purpose, each arbiter has two error/debug registers where it samples the transaction informations of the transaction where the first protocol error happened.

Note: Protocol errors and debug trigger events can lock the error/debug registers. Only the first event of both sources can lock the registers. All other events are not captured with this two error/debug registers unless the lock was released in the meantime.

Further protocol errors will be ignored by an arbiter that has detected an protocol error until the tracking mechanism is re-activated via the arbiter internal control register. A detected protocol error or starvation error is signalled by the arbiter to the default slave module via two separate sideband signals for SRI- and starvation error. The default slave samples the sideband signals pulses in an error status register INTSAT. As each slave has its own sideband signals, the default slave has the information which arbiter has detected an SRI protocol or starvation error. Each error signal can be masked individually by control registers in the arbiter modules. All debug registers are accessible via the SRI-Bus interface of the default slave.

For transaction ID errors of write transactions the SCI propagates the sci_id_err_n signal via the sri_wr_tr_id_err signal from the slave to the default slave module. The default slave sets the assigned bit in register IDINTSAT.

For transaction ID error of read transactions the MCIs propagate the sri_id_err_n signal via the sri_rd_tr_id_err signal from the master to the default slave module. The default slave sets the assigned bit in register IDINTSAT.

Once an error was signalled from an arbiter or an MCI/SCI to the default slave, the default slave module sends an interrupt request to the system. The system can read out the error status registers in the default slave module to find out which arbiter(s) or master/slave have detected an error, then the system can start with more detailed diagnostics by reading out the error/debug registers in the arbiter for a protocol error. The error informations captured for an SRI protocol error allows the identification of the master via the sampled master tag ID and the final destination via the sampled target address. Additionally the arbiter samples the op-code and the sri_rd_n, sri_wr_n and sri_svm control signals of the transaction.

In addition to the SRI transaction information, the XBar_SRI captures sideband signal informations (**XBAR_ERRx (x = 0-6)**.MCI_SBS and **XBAR_ERRD**.MCI_SBS). In the TC1798 these sideband signals are used by the DMA SRI master interface to provide informations about the requestor of a transaction, in parallel to the SRI request phase. **Table 4-5** shows the encoding of the MCI_SBS bit field for the encoding of the TC1798.

Table 4-5 Encoding of ERRx.MCI_SBS in the TC1798

MCI_SBS[7:0]	Bit field encoding
MCI_SBS[2:0]	000_B DMA Channel 0 001_B DMA Channel 1 . . . 110_B DMA Channel 6 111_B DMA Channel 7 This bit field is only valid if MCI_SBS[7:3] shows the Move Engine 0 or Move Engine 1 encoding.
MCI_SBS[7:3]	00000_B Reserved 00001_B Move Engine 0 00010_B Move Engine 1 00011_B MLI 0 00100_B MLI 1 00101_B Cerberus Others -> Reserved

After reading all relevant error informations, the error/debug tracking mechanism can be reactivated.

4.2.7.5 Debug Trigger Event Generation (OCDS Level 1)

The goal is to generate breakpoints on selectable and configurable events in the SRI-Bus traffic. Inside the TriCore breakpoints are generated by the Cerberus module based in debug trigger event signals created by the several decentralized debug blocks in system.

The XBar_SRI module uses the xbar_brk_out_n signal for this purpose.

The generation of any debug trigger event signal has to be enabled by an asserted input signal ocds_enable. If this signal is deasserted no arbiter generate a debug trigger event independent of the selected configurations. The xbar_brk_out_n is driven with the default value in this case.

To enable the user to gain advantage of this feature in the needed way the debug event trigger selection and configuration is done via the three debug registers DBCON, DBADD and DBMADD and the three status registers DBSAT, ERR and ERRADDR.

All DBXXX registers reset only with the ocds_rst_n signal.

The register DBSAT collects all debug trigger events from all arbiters in the XBar_SRI module. When an arbiter generates a debug trigger event the according bit in register DBSAT is set. An arbiter signals a debug trigger event to the default slave via the xcb_db_evt_n signal.

The DBCON register defines the debug trigger event conditions for each arbiter individually. Several individual break conditions can be combined by enabling them in parallel. Possible break conditions are:

- Write transactions
  - If bit DBCON.WREN is set only transactions with an asserted sri_wr_n signal can generate a debug event.

Note: Only if DBCON.WREN and DBCON.RDEN are set together a RMW transaction generate a debug trigger event.

- Read transactions
  - If bit DBCON.RDEN is set only transactions with an asserted sri_rd_n signal can generate a debug event.

Note: Only if DBCON.WREN and DBCON.RDEN are set together a RMW transaction generate a debug trigger event.

- Supervisor mode transactions
  - If bit DBCON.SVMEN is set only transactions with an asserted sri_svm signal can generate a debug event.
- Transactions from a dedicated master
  - If bit DBCON.MASEN is set only transactions initiated by master DBCON.MASTER can generate a debug event.
- Transactions accessing a defined address area

– If bit DBCON.ADDEN is set only transactions accessing an address in the selected address area can generate a debug event. The selected address area is defined by the registers DBADD and DBMADD. Register DBADD defines one global 32-bit address that is compared with sri_addr[31:0] for all bits where DBMADDR is set to ’1’.

All enabled debug trigger conditions are combined by a logical AND.

Example: If DBCON.WREN and DBCON.SVMEN are set and all other enables are cleared a debug trigger event is only generated for a write transaction operating in the supervisor mode.

Additionally a debug trigger event is generated if DBCON.ERREN is set and an error occurs. Please note that an error occurs only when the generation for this source is enabled in the linked registers ARBCON or IDINTEN.

The result of the logical AND of the first five debug trigger event options is combined with the result of the error debug trigger event by a logical OR.

A debug event is signaled to the default slave. The default slave combines all XBar arbiter debug event signals with its own and generates the debug event signal that is sent to the Cerberus module.

The minimum length of debug event signal that is send out to the Cerberus module is adapted to the frequency of the Cerberus module. The debug event signal to the Cerberus will be asserted for as long as one at least one condition inside an XBar master module or the XBar default slave module is met at least.

Debug Trigger events inside the XBar_SRI are sampled in the register DBSAT. Additionally an interrupt can be generated for debug trigger events by the XBar_SRI.

When debug condition is reached in one of the XBar_SRI arbiter modules, informations of the transaction that matched to the debug condition is captured in the two error/debug capture registers ERRx and ERRADDRx. If the two registers are already locked due to an earlier action the capturing is not performed.

Writing to DBCON.REARM will rearm the feature, this also sets DBCON.ARM.

4.2.7.6 Interrupt and Debug Events of the XBar_SRI Module

There are some interactions between interrupt them self and debug events. In general due to the nature of the crossbar concept several interrupts from the same or a different source (arbiter, MCI or SCI) can occur. One interrupt could occur several times before a service request routine is initiate. Additionally can all interrupts occur in parallel to one or more debug trigger events.

All following examples assume a time interval without any acknowledge either from a service routine or a debug routine and all consecutive interrupts/events come from the same source.

Two Consecutive Protocol Errors

The first protocol error is captured as normal together with a generation of an interrupt to the system. The second protocol error is not captured as the two registers ERR and ERRADD are already locked and no interrupt is generated.

Two Consecutive Starvation Errors

The first starvation error generate an interrupt to the system. The second starvation error will not generate an interrupt to the system.

Two Consecutive Transaction ID Errors

The first transaction ID error generate an interrupt to the system. The second transaction ID error will not generate an interrupt to the system.

Two Consecutive Debug Trigger Events

The first debug trigger event is captured as normal together with a generation of debug trigger event signal to the system. The second debug trigger event is not captured as the two registers ERR and ERRADD are already locked and a debug trigger event signal is generated.

Protocol Error followed by a Debug Trigger Event

The first protocol error is captured as normal together with a generation of an interrupt to the system. The later debug trigger event is not captured as the two registers ERR and ERRADD are already locked and a debug trigger event signal is generated to the system.

Debug Trigger Event followed by a Protocol Error

The first debug trigger event is captured as normal together with a generation of debug trigger event signal to the system. The later protocol error is not captured as the two registers ERR and ERRADD are already locked and no interrupt is generated.

Starvation/Transaction ID Error followed by a Debug Trigger Event

The first starvation/transaction ID error generate an interrupt to the system. The later debug trigger event is captured to the two registers ERR and ERRADD and a debug trigger event signal is generated to the system.

Debug Trigger Event followed by a Starvation/Transaction ID Error

The first debug trigger event is captured as normal together with a generation of debug trigger event signal to the system. The later starvation/transaction ID error generates an interrupt to the system.

Releasing the Lock from registers ERR and ERRADD

If the ERR and ERRADD registers are locked only from one even only (protocol error or debug trigger event) the lock can be releasing by:

- Writing a one to ARBCONx.INTACK when the registers are locked by a protocol error
- Writing a one to DBCONx.REARM when the registers are locked by a debug trigger event

If both, a protocol error and a debug trigger event occurred since the lock was released the last time both locks have to be released

- Writing a one to DBCONx.REARM AND Writing and to ARBCONx.INTACK when the registers are locked by a debug trigger event AND a protocol error

4.2.8 Implementation of the Cross Bar (XBar_SRI) in the TC1798

This chapter describes the SRI Interconnect implementation in the TC1798. The knowledge of the specific implementation (e.g. the connection of the SRI master / slave devices to the Interconnect) is necessary in order to:

- map error informations to the connected slave devices
- define the arbitration scheme for accesses to the connected slave devices
- map XBar_SRI (arbiter) control registers to connected slave devices

This chapter includes three tables that are describing: the relationship (mapping) of

- the relationship (mapping) of TC1798 SRI master devices to the XBar_SRI Master Connection Interfaces MCI 0 - MCI 15 (**Table 4-6**)
- the relationship (mapping) of TC1798 SRI slave devices to the XBar_SRI Slave Connection Interfaces SCI 0 - SCI 15 (**Table 4-7**)
- the point to point connections between TC1798 SRI master and slave devices (**Table 4-8**)

4.2.8.1 Mapping of SRI Master Modules to XBar_SRI Master Interfaces

Table 4-6 shows the mapping of master devices to the XBar_SRI Master Interfaces (MCI 0 - MCI 15). Most of the XBar_SRI control registers are related to the XBar_SRI Slave Interfaces (SCI 0 - SCI 15) or the XBar_SRI Master Interfaces. Therefore it is important to know which TC1798 SRI master device relates to which XBar_SRI Slave Interface.

Example 1:

The XBar_SRI includes error registers where each MCI is represented with 1 bit, showing if during the transfers requested by the master devices connected to the MCI´s an error situation occurred (e.g. **XBAR_IDINTSAT**).

Example 2:

The XBar_SRI includes one arbiter module per connected SRI slave device. Each arbiter module includes a four bit field where the priority requests from connected MCI can be

defined. If the access priority of the DMI SRI master to one SRI slave device has to be changed, this can be done via the bit field related to MCI 4 in the arbiter control register related to this SRI slave (**XBAR_PRIOLx (x = 3-6)**, **XBAR_PRIOLD**).

Table 4-6 Mapping of TC1798 SRI master devices to MCI

XBar_SRI Master Connection Interface	Priority after Reset	Connected SRI master device
MCI 0	0	DMA SRI master interface, high priority
MCI 1	1	DMA SRI master interface, medium priority
MCI 2	2	DMA SRI master interface, low priority
MCI 3	3	SFI (PCP / SDMA access to SRI)
MCI 4	4	DMI
MCI 5	5	PMI
MCI 6 - MCI 15	6	-

4.2.8.2 Mapping of SRI Slave modules to XBar_SRI Slave Interfaces

Table 4-7 shows the mapping of slave modules to the XBar_SRI Slave Interfaces (SCI 0 - SCI 15). Most of the XBar_SRI control registers are related to the XBar_SRI Slave Interfaces (SCI 0 - SCI 15) or the XBar_SRI Master Interfaces. Therefore it is important to know which TC1798 SRI slave device relates to which XBar_SRI Slave Interface or arbiter module.

Example 1:

The XBar_SRI includes error registers where each SCI is represented with 1 bit, showing if during the transfers requested by the master devices connected to the MCI´s an error situation occurred (e.g. **XBAR_DBSAT**, **XBAR_IDINTSAT**, **XBAR_IDINTEN**).

Example 2:

The XBar_SRI includes one arbiter module per connected SRI slave device. Each arbiter module includes error capturing resources and breakpoint capabilities. These can be used e.g. to analyze accesses to the connected slave device that where answered with error acknowledge by the slave device (e.g. **XBAR_ERRx (x = 0-6)**, **XBAR_ERRADDRD**).

Table 4-7 Mapping of TC1798 SRI slave devices to SCI

XBar_SRI Slave Connection Interface (SCI)	Connected SRI master device
SCI 0	PMI (PSPR, PCache RAM)
SCI 1	DMI (DSPR, DCache RAM)
SCI 2	SFI (DMI access to devices on SPB)
SCI 3	PMU0
SCI 4	PMU1
SCI 5	LMU
SCI 6	EBU
SCI 7 - SCI 14	-
SCI 15	XBar_SRI Default Slave

4.2.8.3 TC1798 SRI Master / Slave Interconnection Matrix

Table 4-8 shows the SRI master to SRI Slave interconnects that are implemented in the TC1798. The not implemented SRI Master / Slave connections are redundant as they would not be used by the device and does therefore not restrict the functionality.

Table 4-8 TC1798 SRI Master / Slave Interconnection Matrix

XBar_SRI Master Connection Interface	DMA (MCI 0-2)	SFI (MCI 3)	DMI (MCI 4)	PMI (MCI 5)
PMI (SCI 0)	Yes	Yes	Yes	-
DMI (SCI 1)	Yes	Yes	-	Yes
SFI (SCI 2)	-	-	Yes	-
PMU0 (SCI 3)	Yes	Yes	Yes	Yes
PMU1 (SCI 4)	Yes	Yes	Yes	Yes
LMU (SCI 5)	Yes	Yes	Yes	Yes
EBU (SCI 6)	Yes	Yes	Yes	Yes
XBar_SRI (SCI 15)	Yes	Yes	Yes	Yes

4.2.8.4 Connection Master-Slave in XBar_SRI

As the SRI-Bus protocol is a point to point based bus implementation multiplexer inside the data paths in front of the MCIs and arbiter/SCIs are required (see **Figure 4-3** and **Figure 4-4**).

The write data path multiplexer in front of the SCIs are controlled by the related arbiter modules. The read data path multiplexers in front of the MCIs are controlled by all arbiters.

Master - and Slave side MUX

During an SRI transaction, the corresponding arbiter has to establish the data path connection from his slave connection interface to the corresponding master connection interface in order to enable the master to receive the SCI control signals , if it is a read transaction the read data, send by the slave.

4.2.9 SRI Crossbar Registers

Figure 4-6 and Table 4-9 are showing the address maps with all registers of the SRI Crossbar (XBar_SRI) module.

XBar_SRI Unit Register Overview

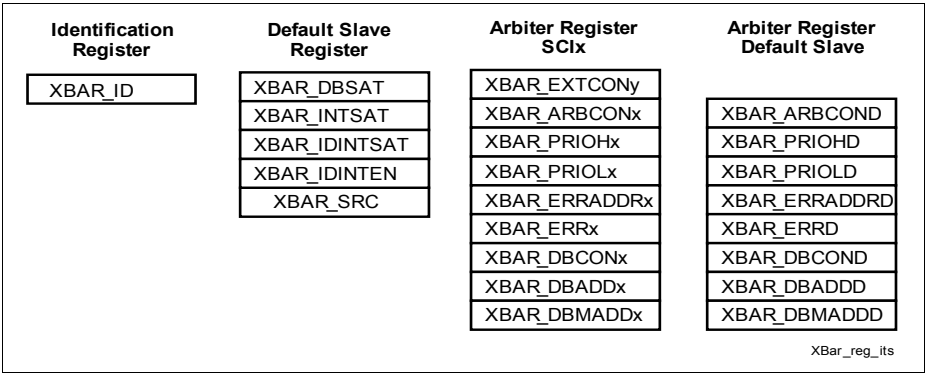


Figure 4-6 TC1798 Control Registers (x = 0 ... 6, y = 2)

Note: Addresses listed in column "Offset Address" of Table 4-9 are word (32-bit) addresses.

Note: XBar_SRI registers can be accessed only with SDTW (32 bit) transactions. 8, 16 bit and RMW transactions are not supported.

Table 4-9 Registers Address Space - XBar_SRI Register Address Space

Module	Base Address	End Address	Note
XBAR	$F870\ 0000_H$	$F870\ 04FF_H$	

Table 4-10 Registers Overview - XBAR Module Control Registers

Short Name	Description	Offset Addr.[1]	Access Mode		Reset Class	Description See
			Read	Write		
-	Reserved	400_H - 404_H	BE	BE	-	-
ID	Identification Register[2]	408_H	U, SV	BE	-	Page 4-34
DBSAT	Debug Trigger Event Status Register[2]	$40C_H$	U, SV	U, SV	1	Page 4-35

Table 4-10 Registers Overview - XBAR Module Control Registers (cont'd)

Short Name	Description	Offset Addr.[1]	Access Mode		Reset Class	Description See
			Read	Write		
INTSAT	Arbiter Interrupt Status Register[2]	410_H	U, SV	U, SV	3	Page 4-36
IDINTSAT	ID Interrupt Status Register[2]	414_H	U, SV	U, SV	3	Page 4-37
IDINTEN	ID Interrupt Enable Register [2]	418_H	U, SV	U, SV	3	Page 4-39
-	Reserved	$41C_H$ - $4F8_H$	BE	BE	-	-
SRC	XBar_SRI Service Request Control Register[2]	$4FC_H$	U, SV	SV	3	Page 4-63
-	Reserved	$01C_H$ - 020_H	BE	BE	-	-
-	Reserved	000_H	BE	BE	-	-
ARBCOND	Arbiter Control Register Default Slave	004_H	U, SV	U, SV	3	Page 4-42
-	Reserved	008_H	U, SV	U, SV	-	-
PRIOLD	Arbiter Priority Register Low Default Slave	$00C_H$	U, SV	U, SV	3	Page 4-44
ERRADDRD	Arbiter Address Error/Debug Capture Register Default Slave	010_H	U, SV	U, SV	3	Page 4-50
ERRD	Arbiter Error/Debug Capture Register Default Slave	014_H	U, SV	U, SV	3	Page 4-51
DBCON	Arbiter x Debug Control Register	018_H	U, SV	U, SV	3	Page 4-52
DBADD	Arbiter x Debug Address Register	$01C_H$	U, SV	U, SV	3	Page 4-55
DBMADD	Arbiter x Debug Mask Address Register	020_H	U, SV	U, SV	3	Page 4-59
-	Reserved	024_H - 040_H	BE	BE	-	-

Table 4-10 Registers Overview - XBAR Module Control Registers (cont'd)

Short Name	Description	Offset Addr.[1)]	Access Mode		Reset Class	Description See
			Read	Write		
ARBCON0	Arbiter 0 Control Register	044_H	U, SV	U, SV	3	Page 4-42
-	Reserved	048_H	U, SV	U, SV	-	-
PRIOL0	Arbiter 0 Priority Register Low	$04C_H$	U, SV	U, SV	3	Page 4-44
ERRADDR0	Arbiter 0 Address Error/Debug Capture Register	050_H	U, SV	U, SV	3	Page 4-50
ERR0	Arbiter 0 Error/Debug Capture Register	054_H	U, SV	U, SV	3	Page 4-51
DBCON0	Arbiter 0 Debug Control Register	058_H	U, SV	U, SV	3	Page 4-52
DBADD0	Arbiter 0 Debug Address Register	$05C_H$	U, SV	U, SV	3	Page 4-55
DBMADD0	Arbiter 0 Debug Mask Address Register	060_H	U, SV	U, SV	3	Page 4-59
-	Reserved	064_H - 080_H	BE	BE	-	-
ARBCON1	Arbiter 1 Control Register	084_H	U, SV	U, SV	3	Page 4-42
-	Reserved	088_H	U, SV	U, SV	-	-
PRIOL1	Arbiter 1 Priority Register Low	$08C_H$	U, SV	U, SV	3	Page 4-44
ERRADDR1	Arbiter 1 Address Error/Debug Capture Register	090_H	U, SV	U, SV	3	Page 4-50
ERR1	Arbiter 1 Error/Debug Capture Register	094_H	U, SV	U, SV	3	Page 4-51
DBCON1	Arbiter 1 Debug Control Register	098_H	U, SV	U, SV	3	Page 4-52
DBADD1	Arbiter 1 Debug Address Register	$09C_H$	U, SV	U, SV	3	Page 4-60

Table 4-10 Registers Overview - XBAR Module Control Registers (cont'd)

Short Name	Description	Offset Addr.[1)]	Access Mode		Reset Class	Description See
			Read	Write		
DBMADD1	Arbiter 1 Debug Mask Address Register	$0A0_H$	U, SV	U, SV	3	Page 4-60
-	Reserved	$0A4_H$ - $0BF_H$	BE	BE	-	-
EXTCON2	External Slave 2 Control (SFI control registers)	$0C0_H$	U, SV	U, SV	3	Page 4-40
ARBCON2	Arbiter 2 Control Register	$0C4_H$	U, SV	U, SV	3	Page 4-42
-	Reserved	$0C8_H$	U, SV	U, SV	-	-
PRIOL2	Arbiter 2 Priority Register Low	$0CC_H$	U, SV	U, SV	3	Page 4-44
ERRADDR2	Arbiter 2 Address Error/Debug Capture Register	$0D0_H$	U, SV	U, SV	3	Page 4-50
ERR2	Arbiter 2 Error/Debug Capture Register	$0D4_H$	U, SV	U, SV	3	Page 4-51
DBCON2	Arbiter 2 Debug Control Register	$0D8_H$	U, SV	U, SV	3	Page 4-52
DBADD2	Arbiter 2 Debug Address Register	$0DC_H$	U, SV	U, SV	3	Page 4-55
DBMADD2	Arbiter 2 Debug Mask Address Register	$0E0_H$	U, SV	U, SV	3	Page 4-59
-	Reserved	$0E4_H$ - 100_H	BE	BE	-	-
ARBCON3	Arbiter 3 Control Register	104_H	U, SV	U, SV	3	Page 4-42
-	Reserved	108_H	U, SV	U, SV	-	-
PRIOL3	Arbiter 3 Priority Register Low	$10C_H$	U, SV	U, SV	3	Page 4-44
ERRADDR3	Arbiter 3 Address Error/Debug Capture Register	110_H	U, SV	U, SV	3	Page 4-50

Table 4-10 Registers Overview - XBAR Module Control Registers (cont'd)

Short Name	Description	Offset Addr.[1)]	Access Mode		Reset Class	Description See
			Read	Write		
ERR3	Arbiter 3 Error/Debug Capture Register	114_H	U, SV	U, SV	3	Page 4-51
DBCON3	Arbiter 3 Debug Control Register	118_H	U, SV	U, SV	3	Page 4-52
DBADD3	Arbiter 3 Debug Address Register	$11C_H$	U, SV	U, SV	3	Page 4-55
DBMADD3	Arbiter 3 Debug Mask Address Register	120_H	U, SV	U, SV	3	Page 4-59
-	Reserved	124_H - 140_H	BE	BE	-	-
ARBCON4	Arbiter 4 Control Register	144_H	U, SV	U, SV	3	Page 4-42
-	Reserved	148_H	U, SV	U, SV	-	-
PRIOL4	Arbiter 4 Priority Register Low	$14C_H$	U, SV	U, SV	3	Page 4-44
ERRADDR4	Arbiter 4 Address Error/Debug Capture Register	150_H	U, SV	U, SV	3	Page 4-50
ERR4	Arbiter 4 Error/Debug Capture Register	154_H	U, SV	U, SV	3	Page 4-51
DBCON4	Arbiter 4 Debug Control Register	158_H	U, SV	U, SV	3	Page 4-52
DBADD4	Arbiter 4 Debug Address Register	$15C_H$	U, SV	U, SV	3	Page 4-55
DBMADD4	Arbiter 4 Debug Mask Address Register	160_H	U, SV	U, SV	3	Page 4-59
-	Reserved	164_H - 180_H	BE	BE	-	-
ARBCON5	Arbiter 5 Control Register	184_H	U, SV	U, SV	3	Page 4-42
-	Reserved	188_H	U, SV	U, SV	-	-
PRIOL5	Arbiter 5 Priority Register Low	$18C_H$	U, SV	U, SV	3	Page 4-44

Table 4-10 Registers Overview - XBAR Module Control Registers (cont'd)

Short Name	Description	Offset Addr.[1]	Access Mode		Reset Class	Description See
			Read	Write		
ERRADDR5	Arbiter 5 Address Error/Debug Capture Register	190_H	U, SV	U, SV	3	Page 4-50
ERR5	Arbiter 5 Error/Debug Capture Register	194_H	U, SV	U, SV	3	Page 4-51
DBCON5	Arbiter 5 Debug Control Register	198_H	U, SV	U, SV	3	Page 4-52
DBADD5	Arbiter 5 Debug Address Register	$19C_H$	U, SV	U, SV	3	Page 4-55
DBMADD5	Arbiter 5 Debug Mask Address Register	$1A0_H$	U, SV	U, SV	3	Page 4-59
-	Reserved	$1A4_H$ - $1C0_H$	BE	BE	-	-
ARBCON6	Arbiter 6 Control Register	$1C4_H$	U, SV	U, SV	3	Page 4-42
-	Reserved	$1C8_H$	U, SV	U, SV	-	-
PRIOL6	Arbiter 6 Priority Register Low	$1CC_H$	U, SV	U, SV	3	Page 4-44
ERRADDR6	Arbiter 6 Address Error/Debug Capture Register	$1D0_H$	U, SV	U, SV	3	Page 4-50
ERR6	Arbiter 6 Error/Debug Capture Register	$1D4_H$	U, SV	U, SV	3	Page 4-51
DBCON6	Arbiter 6 Debug Control Register	$1D8_H$	U, SV	U, SV	3	Page 4-52
DBADD6	Arbiter 6 Debug Address Register	$1DC_H$	U, SV	U, SV	3	Page 4-55
DBMADD6	Arbiter 6 Debug Mask Address Register	$1E0_H$	U, SV	U, SV	3	Page 4-59
-	Reserved	$1E4_H$ - $3FF_H$	BE	BE	-	-

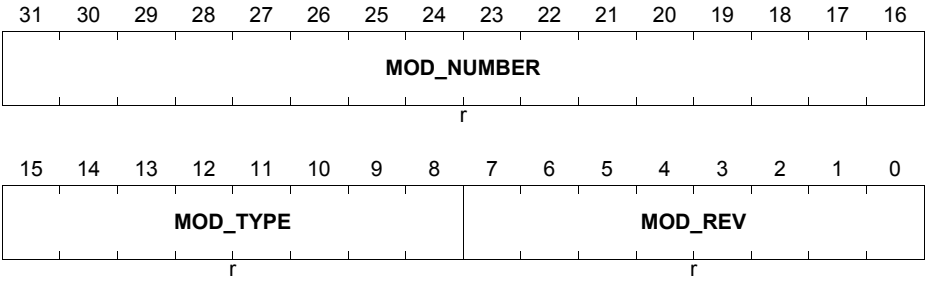
1) The absolute register address is calculated as follows:
Module Base Address (Table 4-10) + Offset Address (shown in this column)

2) This register is located inside the default slave

4.2.9.1 TC1798 Control Registers

The identification register allows the programmer version-tracking of the module. The table below shows the identification register which is implemented in the LBCU module.

XBAR_ID
Module Identification Register **(408_H)** **Reset Value: 0004 D0XX$_H$**



Field	Bits	Type	Description
MOD_REV	[7:0]	r	**Module Revision Number** This bit field defines the module revision number. The value of a module revision starts with 01_H (first revision).
MOD_TYPE	[15:8]	r	**Module Type** The bit field is set to $C0_H$ which defines the module as a 32-bit module.
MOD_NUMBER	[31:16]	r	**Module Number Value** This bit field defines a module identification number. The value for the LBCU module is $000F_H$.

XBAR_DBSAT

Debug Trigger Event Status Register ($40C_H$) **Reset Value: $0000\ 0000_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SCID	0								SCI 6	SCI 5	SCI 4	SCI 3	SCI 2	SCI 1	SCI 0
rwh	rw								rwh	rwh	rwh	rwh	rwh	rwh	rwh

Field	Bits	Type	Description
SCIn (n = 0-6)	n	rwh	**SCI Debug Trigger Event Status** 0_B No Debug Trigger Event was detected for SCIn by its arbiter. 1_B A Debug Trigger Event was detected for SCIn by its arbiter. Writing a '1' to this bit clears the bit.
SCID	15	rwh	**Default Slave Debug Trigger Event Status** 0_B No Debug Trigger Event was detected for the default slave by its arbiter. 1_B A Debug Trigger Event was detected for the default slave by its arbiter. Writing a '1' to this bit clears the bit.
0	[14:7]	rw	**Reserved** Read as 0; must be written with 0.
0	[31:16]	r	**Reserved** Read as 0; should be written with 0.

Note: This register is not reset with the normal system reset as all other registers in the XBar_SRI. This register is only reset with the special debug reset.

XBAR_INTSAT

Arbiter Interrupt Status Register (410_H) Reset Value: 0000 0000$_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PRSCID				0					PRSCI6	PRSCI5	PRSCI4	PRSCI3	PRSCI2	PRSCI1	PRSCI0
rwh				r					rwh	rwh	rwh	rwh	rwh	rwh	rwh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SCSCID				0					SCSCI6	SCSCI5	SCSCI4	SCSCI3	SCSCI2	SCSCI1	SCSCI0
rwh				r					rwh	rwh	rwh	rwh	rwh	rwh	rwh

Field	Bits	Type	Description
SCSCIn (n = 0-6)	n	rwh	**Starvation Error from SCIn Status** 0_B No starvation error is pending from SCIn 1_B A starvation error is pending from SCIn Writing a zero to the bit leaves the content unchanged. Writing a one to the bit clears it. In case of a parallel clearing via software and an error from the hardware the bit remains set and is not cleared.
SCSCID	15	rwh	**Starvation Error from Default Slave Status** 0_B No starvation error is pending from default slave 1_B A starvation error is pending from default slave Writing a zero to the bit leaves the content unchanged. Writing a one to the bit clears it. In case of a parallel clearing via software and an error from the hardware the bit remains set and is not cleared.

Field	Bits	Type	Description
PRSCIn (n = 16-22)	n	rwh	**Protocol Error from SCIn Status** 0_B No protocol error is pending from SCIn 1_B A protocol error is pending from SCIn Writing a zero to the bit leaves the content unchanged. Writing a one to the bit clears it. In case of a parallel clearing via software and an error from the hardware the bit remains set and is not cleared.
PRSCID	31	rwh	**Protocol Error from Default Slave Status** 0_B No protocol error is pending from default slave 1_B A protocol error is pending from default slave Writing a zero to the bit leaves the content unchanged. Writing a one to the bit clears it. In case of a parallel clearing via software and an error from the hardware the bit remains set and is not cleared.
0	[30:23], [14:7]	r	**Reserved** Read as 0; should be written with 0.

Note: Only the bits assigned to configured SCIs are implemented. Not implemented bits treated as reserved bits, read as ´0´, should be written with ´0´.

XBAR_IDINTSAT

Transaction ID Interrupt Status Register(414_H) **Reset Value: $0000\ 0000_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0										IDMCI5	IDMCI4	IDMCI3	IDMCI2	IDMCI1	IDMCI0
r										rwh	rwh	rwh	rwh	rwh	rwh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IDSCID	0								IDSCI6	IDSCI5	IDSCI4	IDSCI3	IDSCI2	IDSCI1	IDSCI0
rwh	r								rwh	rwh	rwh	rwh	rwh	rwh	rwh

Field	Bits	Type	Description
IDSCIn (n = 0-6)	n	rwh	**Transaction ID Error from SCIn Status** 0_B No transaction ID error is pending from SCIn 1_B A transaction ID error is pending from SCIn Writing a zero to the bit leaves the content unchanged. Writing a one to the bit clears it. *Note: In case of a parallel clearing via software and an error from the hardware the bit remains set and is not cleared.*
IDSCID	15	rwh	**Transaction ID Error from Default Slave Status** 0_B No transaction ID error is pending from default slave 1_B A transaction ID error is pending from default slave Writing a zero to the bit leaves the content unchanged. Writing a one to the bit clears it. In case of a parallel clearing via software and an error from the hardware the bit remains set and is not cleared.
IDMCIn (n = 16-21)	n	rwh	**Transaction ID Error from MCIn Status** 0_B No transaction ID error is pending from MCIn 1_B A transaction ID error is pending from MCIn Writing a zero to the bit leaves the content unchanged. Writing a one to the bit clears it. *Note: In case of a parallel clearing via software and an error from the hardware the bit remains set and is not cleared.*
0	[31:22], [14:7]	r	**Reserved** Read as 0; should be written with 0.

Note: Only the bits assigned to configured SCIs are implemented. Not implemented bits treated as reserved bits, read as ´0´, should be written with ´0´.

XBAR_IDINTEN

Transaction ID Interrupt Enable Register(418_H) **Reset Value: 003F 807F$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0										ENMCI5	ENMCI4	ENMCI3	ENMCI2	ENMCI1	ENMCI0
r										rw	rw	rw	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ENSCID	0								ENSCI6	ENSCI5	ENSCI4	ENSCI3	ENSCI2	ENSCI1	ENSCI0
rw	r								rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
ENSCIn (n = 0-6)	n	rw	**Enable ID Error from SCIn** 0_B No transaction ID error from SCIn are sampled 1_B A transaction ID error from SCIn are sampled
ENSCID	15	rw	**Enable ID Error from Default Slave** 0_B No transaction ID error from the default slave is sampled 1_B A transaction ID error from the default slave is sampled
ENMCIn (n = 16-21)	n	rw	**Enable ID Error from MCIn** 0_B No transaction ID error from MCIn are sampled 1_B A transaction ID error from MCIn are sampled
0	[31:22], [14:7]	r	**Reserved** Read as 0; should be written with 0.

Note: Only the bits assigned to configured SCIs are implemented. Not implemented bits treated as reserved bits, read as ´0´, should be written with ´0´.

Note: Reset values for bits/bitfields coupled to masters or slaves that are not configured or enabled are zero.

XBAR_EXTCON2
External Control Register 2 **($0C0_H$)** **Reset Value: $0000\ 0000_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0							NOP DIS	RETRY_CNT				0			
rw							rw	rw				rw			

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MAXWS				0	NO RMW	NO DEL TR	0		FRE QDIS F	0	FRE QDIS S	WF WD	0		
rw				rw	rw	rw	rw		rw	rw	rw	rw	rw		

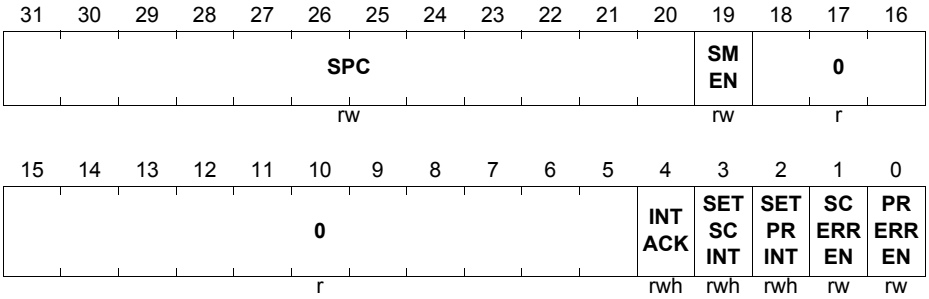
Field	Bits	Type	Description
WFWD	3	rw	**Wait for FPI Write Data** For FPI-Bus block write transfers the transaction request can be delayed until all write data arrived from the FPI-Bus in the SFI. As on thew FPI-Bus side very slow masters can resident SRI-Bus slaves can blocked for many SRI-Bus cycles if the write transaction is started with the first write data 0_B Write transactions on the SRI-Bus are requested with the first received write data from the FPI-Bus (default) 1_B Write transactions on the SRI-Bus are requested with the last received write data from the FPI-Bus
FREQDISS	4	rw	**Disable Fast Request Feature for SRI to FPI Transactions** 0_B Fast request feature is enabled (default) 1_B Fast request feature is disabled
FFREQS	5	rw	**Disable Fast Request Feature for SRI to FPI Transactions** 0_B Fast request feature is used normally (default) 1_B or all transaction automatically the fast request feature is used This bit is not used in TC1798 and is not connected to the SFI. Writing is possible and will change the bit nomal but has no impact to the SFI configuration

Field	Bits	Type	Description
FREQDISF	6	rw	**Disable Fast Request Feature for FPI to SRI Transactions** 0_B Fast request feature is enabled (default) 1_B Fast request feature is disabled
NODELTR	9	rw	**Control Signal for deferred transactions** 0_B Deferred Tranactions are generated (default) 1_B Deferred Tranactions are not generated
NORMW	10	rw	**Control Signal for deferred transactions** 0_B Deferred Tranactions are generated for RMW (default) 1_B Deferred Tranactions are not generated for RMW
MAX_WS	[19:13]	rw	**FPI-Bus Waitstait Retry Ratio** SIF-FPI retry after the programed value delayed transactions from the FPI-Bus. The value should be greater than 32, otherwise all transactions will be retired
RETRY_CNT	[23:20]	rw	**MIF_FPI Retry Idle Count** Number of clock cycles before MIF2_FPI repeats a transaction after a retry
NOPDIS	24	rw	**NOP-Inclusion Disable** 0_B NOP inclusion is used by SIF_FPI (default) 1_B NOP inclusion is disabled for SIF_FPI
0	[31:25], [19:16], 11, [8:7], 5, [2:0]	rw	**Reserved** Read as 0; should be written with 0.

Note: Only the bits assigned to configured SCIs are implemented. Not implemented bits treated as reserved bits, read as ´0´, should be written with ´0´.

Note: Reset values for bits/bitfields coupled to masters or slaves that are not configured or enabled are zero.

XBAR_ARBCONx (x = 0-6)
Arbiter Control Register x **(044_H+x*40_H)** **Reset Value: 0000 0003_H**
XBAR_ARBCOND
Arbiter Control Register D **(004_H)** **Reset Value: 0000 0003_H**



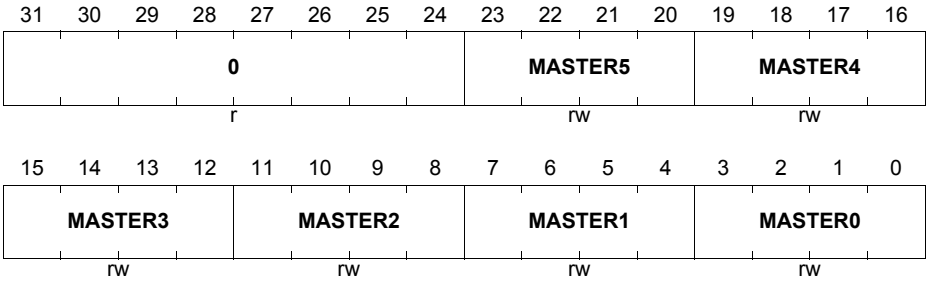
Field	Bits	Type	Description
PRERREN	0	rw	**SRI Protocol Error Enable** 0_B Protocol errors are not recognized and no information is captured. 1_B Protocol errors are recognized and information is captured.
SCERREN	1	rw	**SRI Starvation Error Enable** 0_B Starvation based errors are not recognized and no information is captured. 1_B Starvation based errors are recognized and information is captured.
SETPRINT	2	rwh	**Set SRI Protocol Interrupt** 0_B No protocol interrupt is generated 1_B A protocol interrupt is generated After the interrupt is generated by set the bit it's automatically cleared by the hardware
SETSCINT	3	rwh	**Set SRI Starvation Interrupt** 0_B No starvation interrupt is generated 1_B A starvation interrupt is generated After the interrupt is generated by set the bit it's automatically cleared by the hardware

Field	Bits	Type	Description
INTACK	4	rwh	**Interrupt Acknowledge** 0_B Default value 1_B An Error for this arbiter is pending. The ERRADDR and ERR registers are not updated for new errors. Writing a one to this bitfield while it's set have the following results: The error lock of registers ERRADDR and ERR are released and the register could be updated with the next interrupt request detected (see **Chapter 4.2.7.4**). In the cycle after the write action the hardware automatically clears the bit.
SMEN	19	rw	**Starvation Mode Enable** 0_B Starvation mode is disabled 1_B Starvation mode is enabled
SPC	[31:20]	rw	**Starvation Protection Counter Reload Value** The reload value defines the period for the starvation protection.
0	[18:5]	r	**Reserved** Read as 0; should be written with 0.

Note: Only the bits assigned to configured SCIs are implemented. Bits for non configured SCIs are treated as reserved bits.

Note: The ´D´ at ARBCOND stands for Default Slave.

XBAR_PRIOLx (x = 3-6)
Arbiter Priority Register x **($04C_H$+x*40_H)** **Reset Value: $0054\ 3210_H$**
XBAR_PRIOLD
Arbiter Priority Register D **($00C_H$)** **Reset Value: $0054\ 3210_H$**



Field	Bits	Type	Description
MASTER0	[3:0]	rw	**Master 0 Priority** (Priority of DMA High Priority access) This bitfield contains the master priority for the arbitration used by the arbiter of slave x. For each master a unique number for this slave has to be used. A lower number has a higher priority in the arbitration round than a higher one.
MASTER1	[7:4]	rw	**Master 1 Priority** (Priority of DMA Medium Priority access) This bitfield contains the master priority for the arbitration used by the arbiter of slave x. For each master a unique number for this slave has to be used. A lower number has a higher priority in the arbitration round than a higher one.
MASTER2	[11:8]	rw	**Master 2 Priority** (Priority of DMA Low Priority access) This bitfield contains the master priority for the arbitration used by the arbiter of slave x. For each master a unique number for this slave has to be used. A lower number has a higher priority in the arbitration round than a higher one.

Field	Bits	Type	Description
MASTER3	[15:12]	rw	**Master 3 Priority** (Priority of SFI access) This bitfield contains the master priority for the arbitration used by the arbiter of slave x. For each master a unique number for this slave has to be used. A lower number has a higher priority in the arbitration round than a higher one.
MASTER4	[19:16]	rw	**Master 4 Priority** (Priority of DMI access) This bitfield contains the master priority for the arbitration used by the arbiter of slave x. For each master a unique number for this slave has to be used. A lower number has a higher priority in the arbitration round than a higher one.
MASTER5	[23:20]	rw	**Master 5 Priority** (Priority of PMI access) This bitfield contains the master priority for the arbitration used by the arbiter of slave x. For each master a unique number for this slave has to be used. A lower number has a higher priority in the arbitration round than a higher one.
0	[31:24]	r	**Reserved** Read as 0; should be written with 0.

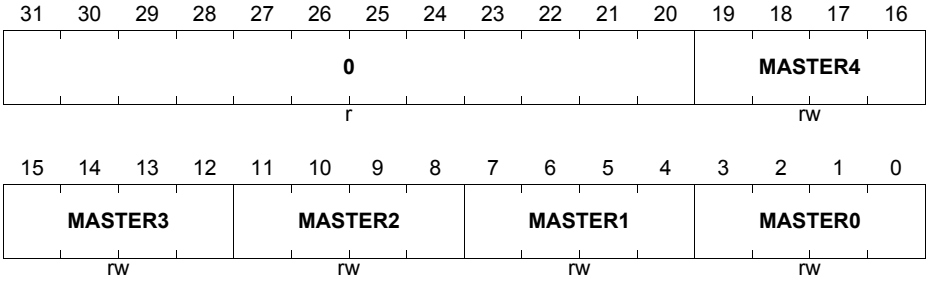
Note: Only the bits assigned to configured MCIs are implemented. Bits for non configured SCIs are treated as reserved bits.

Note: The ´D´ at XBAR_PRIOLD stands for Default Slave.

Note: Reset values for bits/bitfields coupled to masters or slaves that are not configured or enabled are zero.

XBAR_PRIOL0

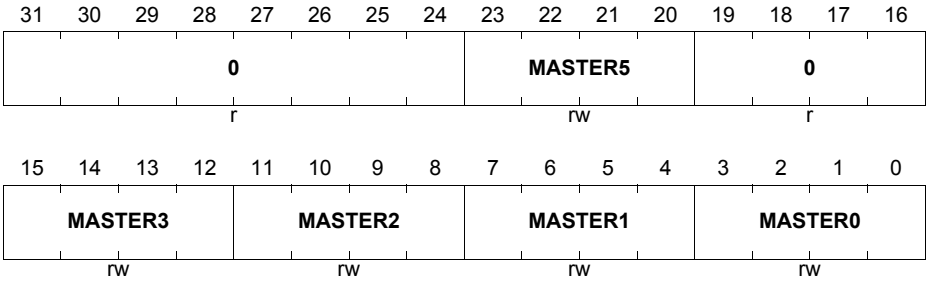
Arbiter Priority Register 0 **($04C_H$)** **Reset Value: $0004\ 3210_H$**



Field	Bits	Type	Description
MASTER0	[3:0]	rw	**Master 0 Priority** (Priority of DMA High Priority access) This bitfield contains the master priority for the arbitration used by the arbiter of slave x. For each master a unique number for this slave has to be used. A lower number has a higher priority in the arbitration round than a higher one.
MASTER1	[7:4]	rw	**Master 1 Priority** (Priority of DMA Medium Priority access) This bitfield contains the master priority for the arbitration used by the arbiter of slave x. For each master a unique number for this slave has to be used. A lower number has a higher priority in the arbitration round than a higher one.
MASTER2	[11:8]	rw	**Master 2 Priority** (Priority of DMA Low Priority access) This bitfield contains the master priority for the arbitration used by the arbiter of slave x. For each master a unique number for this slave has to be used. A lower number has a higher priority in the arbitration round than a higher one.

Field	Bits	Type	Description
MASTER3	[15:12]	rw	**Master 3 Priority** (Priority of SFI access) This bitfield contains the master priority for the arbitration used by the arbiter of slave x. For each master a unique number for this slave has to be used. A lower number has a higher priority in the arbitration round than a higher one.
MASTER4	[19:16]	rw	**Master 4 Priority** (Priority of DMI access) This bitfield contains the master priority for the arbitration used by the arbiter of slave x. For each master a unique number for this slave has to be used. A lower number has a higher priority in the arbitration round than a higher one.
0	[31:20]	r	**Reserved** Read as 0; should be written with 0.

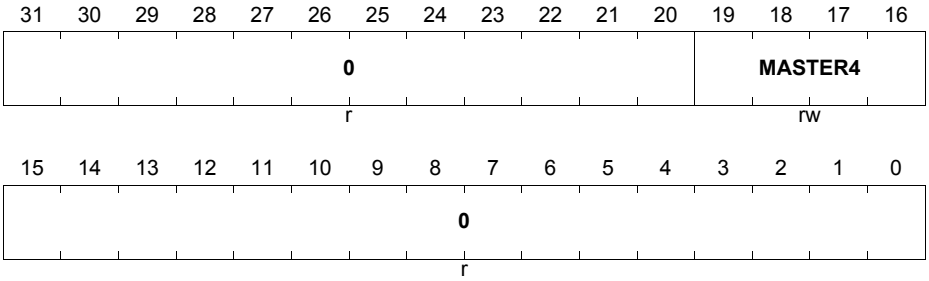
XBAR_PRIOL1
Arbiter Priority Register 1 **($08C_H$)** **Reset Value: $0050\ 3210_H$**



Field	Bits	Type	Description
MASTER0	[3:0]	rw	**Master 0 Priority** (Priority of DMA High Priority access) This bitfield contains the master priority for the arbitration used by the arbiter of slave x. For each master a unique number for this slave has to be used. A lower number has a higher priority in the arbitration round than a higher one.
MASTER1	[7:4]	rw	**Master 1 Priority** (Priority of DMA Medium Priority access) This bitfield contains the master priority for the arbitration used by the arbiter of slave x. For each master a unique number for this slave has to be used. A lower number has a higher priority in the arbitration round than a higher one.
MASTER2	[11:8]	rw	**Master 2 Priority** (Priority of DMA Low Priority access) This bitfield contains the master priority for the arbitration used by the arbiter of slave x. For each master a unique number for this slave has to be used. A lower number has a higher priority in the arbitration round than a higher one.
MASTER3	[15:12]	rw	**Master 3 Priority** (Priority of SFI access) This bitfield contains the master priority for the arbitration used by the arbiter of slave x. For each master a unique number for this slave has to be used. A lower number has a higher priority in the arbitration round than a higher one.

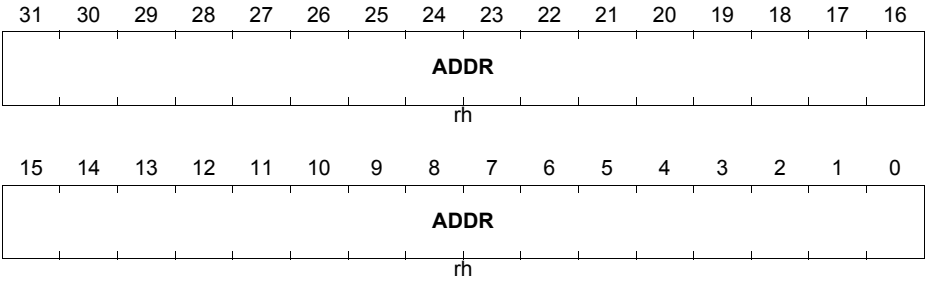
Field	Bits	Type	Description
MASTER5	[23:20]	rw	**Master 5 Priority** (Priority of PMI access) This bitfield contains the master priority for the arbitration used by the arbiter of slave x. For each master a unique number for this slave has to be used. A lower number has a higher priority in the arbitration round than a higher one.
0	[31:24], [19:16]	r	**Reserved** Read as 0; should be written with 0.

XBAR_PRIOL2
Arbiter Priority Register 2 **(0CC$_H$)** **Reset Value: 0004 0000$_H$**



Field	Bits	Type	Description
MASTER4	[19:16]	rw	**Master 4 Priority** (Priority of DMI access) This bitfield contains the master priority for the arbitration used by the arbiter of slave x. For each master a unique number for this slave has to be used. A lower number has a higher priority in the arbitration round than a higher one.
0	[31:20], [15:0]	r	**Reserved** Read as 0; should be written with 0.

XBAR_ERRADDRD
Error/Debug Address Capture Register D(010_H) **Reset Value: $0000\ 0000_H$**
XBAR_ERRADDR0
Error/Debug Address Capture Register 0(050_H) **Reset Value: $C000\ 0000_H$**
XBAR_ERRADDR1
Error/Debug Address Capture Register 1(090_H) **Reset Value: $D000\ 0000_H$**
XBAR_ERRADDR2
Error/Debug Address Capture Register 2($0D0_H$) **Reset Value: $F000\ 0000_H$**
XBAR_ERRADDRx (x = 3-6)
Error/Debug Address Capture Register x(050_H+x*40_H) **Reset Value: $8000\ 0000_H$**

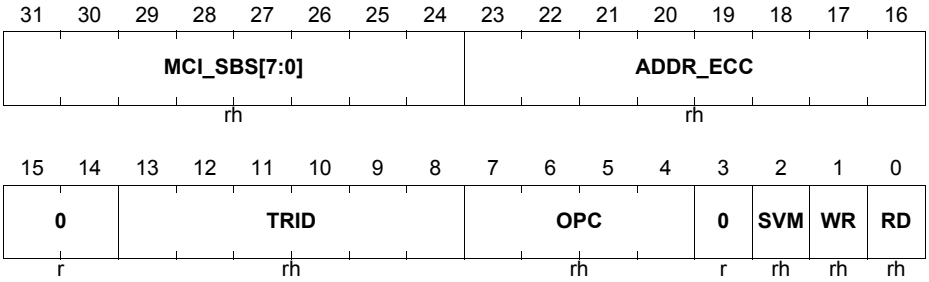


Field	Bits	Type	Description
ADDR	[31:0]	rh	**Transaction Address** This biffield contains the address of the erroneous transaction from the address phase

Note: The default value can differ from the one shown here because a constant can be used to reduce the number of compared bits in the arbitration if a slave occupies only a limited address area. For more details see the design specification of the XBar_SRI.

Note: The ´D´ at XBAR_ERRADDRD stands for Default Slave.

XBAR_ERRx (x = 0-6)
Error/Debug Capture Register x **(054_H+x*40_H)** **Reset Value: 0000 0000_H**
XBAR_ERRD
Error/Debug Capture Register D **(014_H)** **Reset Value: 0000 0000_H**



Field	Bits	Type	Description
RD	0	rh	**Read Indication Status** 0_B The read indication SRI-Bus signal line was asserted 1_B The read indication SRI-Bus signal line was deasserted
WR	1	rh	**Write Indication Status** 0_B The write indication SRI-Bus signal line was asserted 1_B The write indication SRI-Bus signal line was deasserted
SVM	2	rh	**Supervisor Mode Indication Status** 0_B The supervisor mode indication SRI-Bus signal line was deasserted 1_B The supervisor mode indication SRI-Bus signal line was asserted
OPC	[7:4]	rh	**Operation Code** This bitfield contains the op-code of the erroneous transaction.

Field	Bits	Type	Description
TR_ID	[13:8]	rh	**Transaction ID** This bitfield contains the transaction ID of the erroneous transaction from the address phase. The Transaction ID is build out of an 4 bit unique TAG ID TR_ID[3:0] and a 2 bit running number TR_ID[5:4] (see also **Chapter 4.6**).
ADDR_ECC	[23:16]	rh	**SRI Address Phase Error Detection Information** This bitfield contains the Address Phase Error Detection Information of the erroneous transaction
MCI_SBS	[31:24]	rh	**MCI Sideband Signals [7:0]** This bitfield contains the MCI Sideband Signals [7:0] that are related to the address phase informations captured by the ERRD/ERRADDR registers. In the TC1798 the sideband signals are used by the DMA SRI master interface to provide information about the DMA requestor of a DMA transaction (for the encoding see **Table 4-5**).
0	[15:14], 3	r	**Reserved** Read as 0; should be written with 0

Note: The ´D´ at XBAR_ERRD stands for Default Slave.

XBAR_DBCONx (x = 0-6)
Debug Control Register x **(058_H+x*40_H)** **Reset Value: 0000 0000_H**
XBAR_DBCOND
Debug Control Register D **(018_H)** **Reset Value: 0000 0000_H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0				MASTER				MAS EN	0		ERR EN	ADD EN	SVM EN	WR EN	RD EN
r				rw				rw	r		rw	rw	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0												SET DB EVT	RE ARM	DB SAT	DB EN
r												w	w	rh	r

Field	Bits	Type	Description
DBEN	0	r	**Status of OCDS Enable Signal** Displays the value of the OCDS enable signal from Cerberus.
DBSAT	1	rh	**Debug (OCDS) Trigger Status** 0_B The debug (OCDS) trigger was used and has to be rearmed 1_B The debug (OCDS) trigger is armed
REARM	2	w	**Rearm Debug (OCDS) Trigger** 0_B Read back value 1_B Writing a one to this bit arms sets bit DBCON.DBSAT. Writing a one to this bitfield while it's set have the following results: The debug lock of registers ERRADDR and ERR are released and the register could be updated with the next debug event request detected (see **Chapter 4.2.7.4**). In the cycle after the write action the hardware automatically clears the bit. *Note: This bit is automatically reset by the hardware after DBCON.DBSAT was set.*
SETDBEVT	3	w	**Set Debug Event** 0_B Default value 1_B A debug trigger event will be generated by this arbiter if the debug feature is enabled (DBCON.ENST is set). The registers ERR and ERRADD capture the status if not locked already. *Note: This bit is automatically reset by the hardware.*
RDEN	16	rw	**Read Trigger Enable** 0_B Read Transaction are not used to trigger the debug trigger event (OCDS) 1_B Read Transaction are used to trigger the debug trigger event (OCDS)

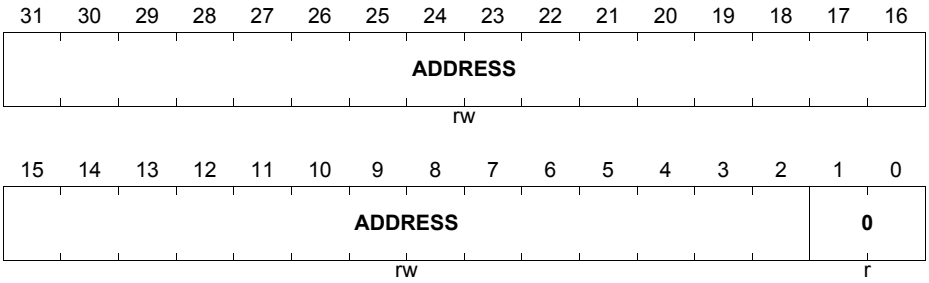
Field	Bits	Type	Description
WREN	17	rw	**Write Trigger Enable** 0_B Write Transaction are not used to trigger the debug trigger event (OCDS) 1_B Write Transaction are used to trigger the debug trigger event (OCDS)
SVMEN	18	rw	**SVM Trigger Enable** 0_B SVM Transaction are not used to trigger the debug trigger event (OCDS) 1_B SVM Transaction are used to trigger the debug trigger event (OCDS)
ADDEN	19	rw	**Address Trigger Enable** 0_B Transaction addresses are not used to trigger the debug trigger event (OCDS) 1_B Transaction address defined by the registers DBADD and DBMADD are used to trigger the debug trigger event (OCDS)
ERREN	20	rw	**Error Trigger Enable** 0_B Errored Transaction are not used to trigger the debug trigger event (OCDS) 1_B Errored Transaction are used to trigger the debug trigger event (OCDS) Reading this bit return always zero. *Note: Protocol errors, starvation errors and transaction ID errors can be used where, but have to enabled before as usual in registers ARBCON or IDINTEN depending on the error type.*
MASEN	23	rw	**Master Trigger Enable** 0_B The Master TAG ID as defined in the bitfield MASTER is not used to trigger the debug trigger event (OCDS) 1_B The Master TAG ID as defined in the bitfield MASTER is used to trigger the debug trigger event (OCDS)

Field	Bits	Type	Description
MASTER	[27:24]	rw	**Master TAG ID Trigger Selector** The value of this bitfield define the Master TAG ID within the address phase of an SRI transaction to the related SRI slave module that triggers the debug trigger event (OCDS). The Master TAG IDs are defined here: **Table 4-17**.
0	[31:28], [22:21], [15:4]	r	**Reserved** Read as 0; should be written with 0.

Note: This register is not reset with the normal system reset as all other registers in the XBar_SRI. This register is only reset with the special debug reset.

Note: The ´D´ at XBAR_DBCOND stands for Default Slave.

XBAR_DBADDD
Debug Address Register D **(01C$_H$)** **Reset Value: 0000 0000$_H$**



Field	Bits	Type	Description
UPPER	[31:2]	rw	**Debug Address Boundary**
0	[1:0]	r	**Reserved** Read as 0; should be written with 0.

Note: This register is reset with the debug reset (Class 1 reset).

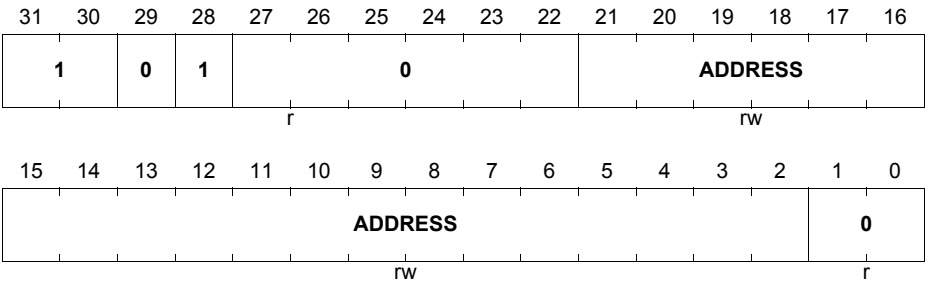
Note: The last ´D´ at XBAR_DBADDD stands for Default Slave.

XBAR_DBADD0
Debug Mask Address Register 0 ($05C_H$) Reset Value: $C000\ 0000_H$

Field	Bits	Type	Description
ADDRESS	[29:2]	rw	**Debug Address Boundary**
ONE	[31:30]	r	**Reserved** Read as 1; should be written with 0.
0	[1:0]	r	**Reserved** Read as 0; should be written with 0.

Note: This register is reset with the debug reset (Class 1 reset).

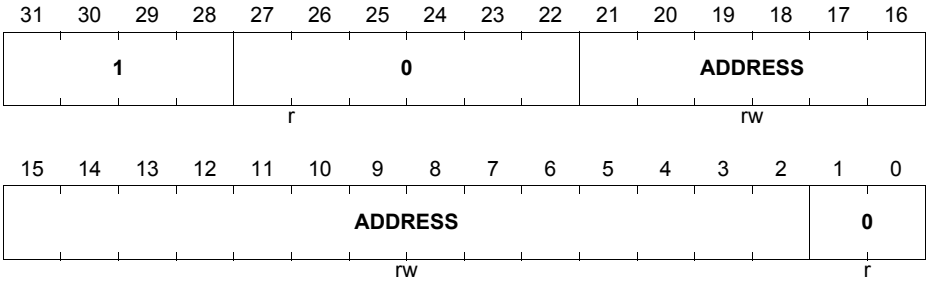
XBAR_DBADD1
Debug Mask Address Register 1 ($09C_H$) Reset Value: $D000\ 0000_H$



Field	Bits	Type	Description
ADDRESS	[21:2]	rw	**Debug Address Boundary**
ONE	[31:30], 28	r	**Reserved** Read as 1; should be written with 0.
0	29, [27:22], [1:0]	r	**Reserved** Read as 0; should be written with 0.

Note: This register is reset with the debug reset (Class 1 reset).

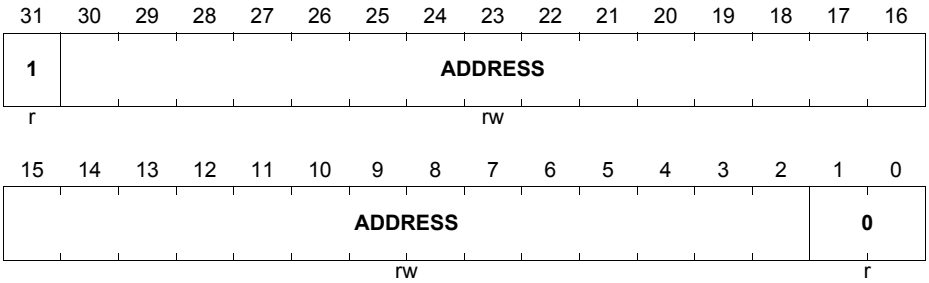
XBAR_DBADD2
Debug Mask Address Register 2 ($0DC_H$) Reset Value: $F000\ 0000_H$



Field	Bits	Type	Description
ADDRESS	[21:2]	rw	**Debug Address Boundary**
ONE	[31:28]	r	**Reserved** Read as 1; should be written with 0.
0	[27:22], [1:0]	r	**Reserved** Read as 0; should be written with 0.

Note: This register is reset with the debug reset (Class 1 reset).

XBAR_DBADD3
Debug Mask Address Register 3 ($11C_H$) Reset Value: $8000\ 0000_H$
XBAR_DBADD4
Debug Mask Address Register 4 ($15C_H$) Reset Value: $8000\ 0000_H$
XBAR_DBADD6
Debug Mask Address Register 6 ($1DC_H$) Reset Value: $8000\ 0000_H$



Field	Bits	Type	Description
ADDRESS	[30:2]	rw	**Debug Address Boundary**
ONE	31	r	**Reserved** Read as 1; should be written with 0.
0	[1:0]	r	**Reserved** Read as 0; should be written with 0.

Note: This register is reset with the debug reset (Class 1 reset).

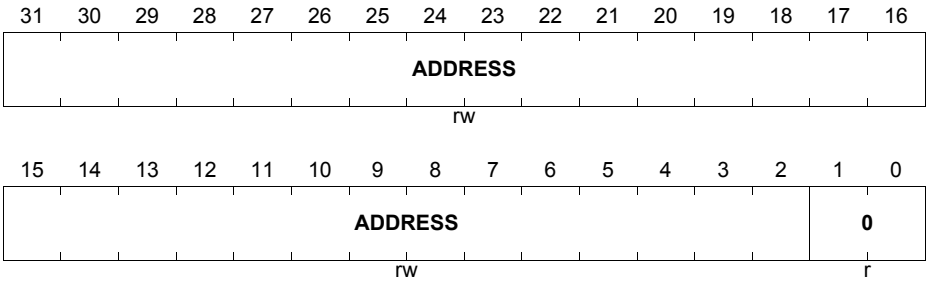
XBAR_DBADD5
Debug Mask Address Register 5 ($19C_H$) Reset Value: $8000\ 0000_H$

Field	Bits	Type	Description
ADDRESS	[29:2]	rw	**Debug Address Boundary**
ONE	31	r	**Reserved** Read as 1; should be written with 0.
0	30, [1:0]	r	**Reserved** Read as 0; should be written with 0.

Note: This register is reset with the debug reset (Class 1 reset).

XBAR_DBMADDD

Debug Mask Address Register D (020_H) Reset Value: 0000 0000$_H$

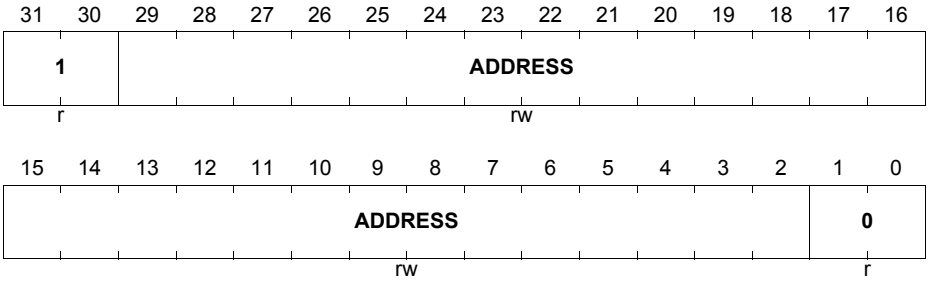


Field	Bits	Type	Description
ADDRESS	[31:2]	rw	**Debug Address Boundary**
0	[1:0]	r	**Reserved** Read as 0; should be written with 0.

Note: This register is reset with the debug reset (Class 1 reset).

Note: The last ´D´ at XBAR_DBMADDD stands for Default Slave.

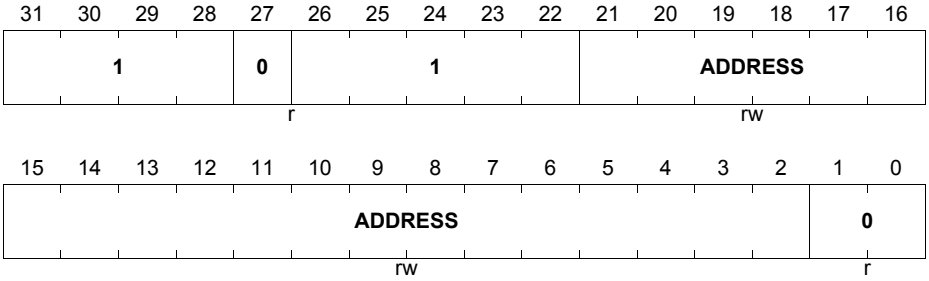
XBAR_DBMADD0
Debug Mask Address Register 0 (060_H) Reset Value: C000 0000$_H$
XBAR_DBMADD5
Debug Mask Address Register 5 ($1A0_H$) Reset Value: C000 0000$_H$



Field	Bits	Type	Description
ADDRESS	[29:2]	rw	**Debug Address Boundary**
ONE	[31:30]	r	**Reserved** Read as 1; should be written with 0.
0	[1:0]	r	**Reserved** Read as 0; should be written with 0.

Note: This register is reset with the debug reset (Class 1 reset).

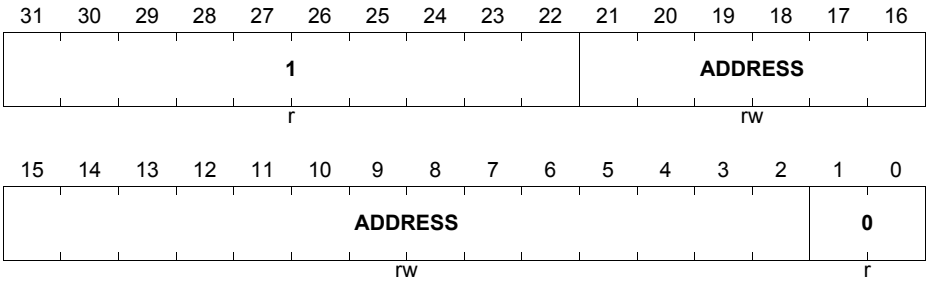
XBAR_DBMADD1
Debug Mask Address Register 1 ($0A0_H$) Reset Value: F7C0 0000$_H$



Field	Bits	Type	Description
ADDRESS	[21:2]	rw	**Debug Address Boundary**
ONE	[31:28], [26:22]	r	**Reserved** Read as 1; should be written with 0.
0	27, [1:0]	r	**Reserved** Read as 0; should be written with 0.

Note: This register is reset with the debug reset (Class 1 reset).

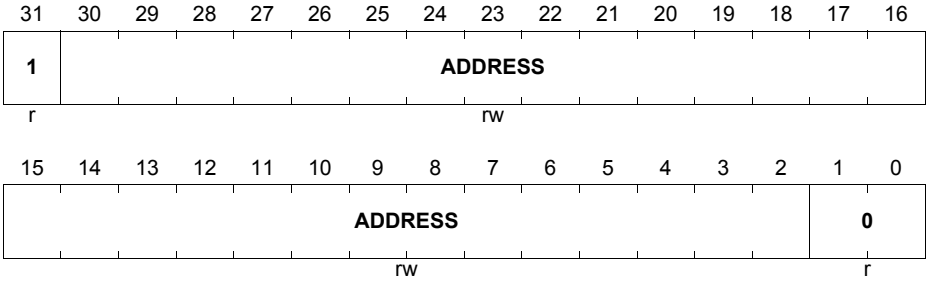
XBAR_DBMADD2
Debug Mask Address Register 2 ($0E0_H$) Reset Value: $FFC0\ 0000_H$



Field	Bits	Type	Description
ADDRESS	[21:2]	rw	**Debug Address Boundary**
ONE	[31:22]	r	**Reserved** Read as 1; should be written with 0.
0	[1:0]	r	**Reserved** Read as 0; should be written with 0.

Note: This register is reset with the debug reset (Class 1 reset).

XBAR_DBMADD3
Debug Mask Address Register 3 (120_H) Reset Value: $8000\ 0000_H$
XBAR_DBMADD4
Debug Mask Address Register 4 (160_H) Reset Value: $8000\ 0000_H$
XBAR_DBMADD6
Debug Mask Address Register 6 ($1E0_H$) Reset Value: $8000\ 0000_H$



Field	Bits	Type	Description
ADDRESS	[30:2]	rw	**Debug Address Boundary**
ONE	31	r	**Reserved** Read as 1; should be written with 0.
0	[1:0]	r	**Reserved** Read as 0; should be written with 0.

Note: This register is reset with the debug reset (Class 1 reset).

XBAR_SRC
XBar_SRI Service Request Control Register
($4FC_H$) **Reset Value: $0000\ 0000_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SETR	CLRR	SRR	SRE	TOS		0		SRPN							
w	w	rh	rw	rw		r		rw							

Field	Bits	Type	Description
SRPN	[7:0]	rw	**Service Request Priority Number**
TOS	[11:10]	rw	**Type-of-Service State** If written, register must be set to 00_B. This means type-of-service is associated with interrupt bus 0 (CPU interrupt arbitration bus).
SRE	12	rw	**Service Request Enable**
SRR	13	rh	**Service Request Flag**
CLRR	14	w	**Request Flag Clear Bit**
SETR	15	w	**Request Flag Set Bit**
0	[9:8], [31:16]	r	**Reserved** Read as 0; should be written with 0.

4.3 Shared Resource Interconnect to FPI Bus Interface (SFI Bridge)

This section describes the basic functionality of the SFI Bridge.

4.3.1 Functional Overview

The SFI Bridge is a bi-directional bus bridge between the SRI Interconnect and the System Peripheral FPI Bus (SPB). The bridge supports all transactions types of both the SRI Bus and FPI Bus.

The bridge is transparent, this means that the address of a transaction and the master TAG of a bus master is forwarded to the other side of the bridge. Addresses are only changed by the bridge where it is required by the transaction conversion from the 64 bit SRI Interconnect to the 32 bit SPB.

In order to avoid deadlocks, priority is given to transactions initiated by the DMA on SPB or the PCP.

Bus Errors at Writes via the SFI Bridge

Write transactions are handled as posted writes. The SFI is able to buffer multiple posted writes. This means that a write operation from the SPB through the SFI Bridge to the SRI Interconnect can be finished on SPB and than generated on the SRI autonomously by the SFI. If this write operation results in a bus error on the SRI the Error information is not passed back to the SPB bus. This is also valid for transactions from SRI to SPB via SFI bridge. The bus error is detected by the on chip bus control logic of the target on chip bus system (BCU_FPI on the SPB, XBar_SRI on the SRI) which can generate an interrupt.

Note that this behavior occurs only at write operations via the SFI Bridge. It can also be triggered by an erroneous write cycle of a read-modify-write bus transaction.

4.4 System Peripheral Bus

The TC1798 has one on-chip FPI Bus:

- System Peripheral Bus (SPB)
  - System bus for on-chip peripherals

This section gives an overview of the on-chip FPI Bus. It describes its bus control units, the bus characteristics, bus arbitration, scheduling, prioritizing, error conditions, and debugging support.

4.4.1 Overview

The FPI Bus interconnects the on-chip peripheral functional units with the TC1798 processor subsystem.

The FPI Bus is designed to be quick to be acquired by on-chip functional units, and quick to transfer data. The low setup overhead of the FPI Bus access protocol guarantees fast FPI Bus acquisition, which is required for time-critical applications.

The FPI Bus is designed to sustain high transfer rates. For example, a peak transfer rate of up to 320 Mbyte/s can be achieved with the 32-bit data bus at 80 MHz bus clock. Multiple data transfers per bus arbitration cycle allow the FPI Bus to operate close to its peak bandwidth.

Additional features of the FPI Bus include:

- Optimized for high speed and high performance
- Support of multiple bus masters and pipelined transactions
- 32-bit wide address and data buses
- 8-, 16-, and 32-bit data transfers
- 64-, 128-, and 256-bit block transfers
- Central simple per-cycle arbitration
- Slave-controlled wait state insertion
- Support of atomic operations LDMST, ST.T and SWAP.W

The functional units of the TC1798 are connected to the FPI Bus via FPI Bus interfaces. An FPI Bus interfaces acts as bus agents, requesting bus transactions on behalf of their functional unit, or responding to bus transaction requests.

There are two types of bus agents:

- FPI Bus master agents can initiate FPI Bus transactions and can also act as slaves.
- Slave agents can only react and respond to FPI Bus transaction requests in order to read or write internal registers of slave modules as for example memories.

When an FPI Bus master attempts to initiate a transfer on the FPI Bus, it first signals a request for bus ownership to the bus control unit (SBCU). When bus ownership is granted by the SBCU, an FPI Bus read or write transaction is initiated. The unit targeted by the transaction becomes the FPI Bus slave, and responds with the requested action.

Some functional units operate only as slaves, while others can operate as either masters or slaves on the FPI Bus. In the TC1798, DMI and PMI (via the SFI Bridge), PCP, DMA (including Cerberus and MLI´s) and SDMA operate as FPI Bus masters. On-chip peripheral units are typically FPI Bus slaves.

FPI Bus arbitration is performed by the Bus Control Unit (SBCU) of the FPI Bus. In case of bus errors, the SBCU generates an interrupt request to the CPU and provides debugging information about the actual bus error to the CPU.

4.4.2 Bus Transaction Types

This section describes the SPB transaction types.

Single Transfers

Single transfers are byte, half-word, and word transactions that target any slave connected to SPB. Note that the SFI Bridge operates as an SPB master.

Block Transfers

Block transfers operate in principle in the same way as single transfers do, but one address phase is followed by multiple data phases. Block transfers can be composed of 2 word, 4 word, or 8 word transfers.

Note: In general, block transfers (2 word, 4 word, or 8 word) cannot be executed in the TC1798 with peripheral units that operate as FPI Bus slaves during an FPI Bus transaction.

Block transfers are initiated by the following CPU instructions: LD.D, LD.DA, MOV.D, ST.D and ST.DA. The BCOPY instruction of the PCP also initiates a block transfer transaction on the FPI Bus.

Atomic Transfers

Atomic transfers are generated by LDMST, ST.T and SWAP.W instructions that require two single transfers. The read and write transfer of an atomic transfer are always locked and cannot be interrupted by another bus masters. Atomic transfers are also referenced as read-modify-write transfers.

*Note: See also **Table 4-13** for available FPI Bus transfer types.*

4.4.3 Reaction of a Busy Slave

If an FPI Bus slave is busy at an incoming FPI Bus transaction request, it can delay the execution of the FPI Bus transaction. The requesting FPI Bus master releases the FPI Bus for one cycle after the FPI Bus transaction request, in order to allow the FPI Bus slave to indicate if it is ready to handle the requested FPI Bus transaction. This sequence is repeated as long as the slave indicates that it is busy.

Note: For the FPI Bus default master, the one cycle gap does not result in a performance loss because it is granted the FPI Bus in this cycle as default master if no other master requests the FPI Bus for some other reasons.

4.4.4 Address Alignment Rules

FPI Bus address generation is compliant with the following rules:

- Half-word transactions must have a half-word aligned address (A0 = 0). Half-word accesses on byte lanes 1 and 2 addresses are illegal.
- Word transactions must always have word-aligned addresses (A[1:0] = 00_B).
- Block transactions must always have block-type aligned addresses.

4.4.5 FPI Bus Basic Operations

This section describes some basic transactions on the FPI Bus.

The example in **Figure 4-7** shows the three cycles of an FPI Bus operation:

1. **Request/Grant Cycle:** The FPI Bus master attempts to perform a read or write transfer and requests for the FPI Bus. If the FPI Bus is available, it is granted in the same cycle by the FPI Bus controller.
2. **Address Cycle:** After the request/grant cycle, the master puts the address on the FPI Bus, and all FPI Bus slave devices check whether they are addressed for the following data cycle.
3. **Data Cycle:** In the data cycle, either the master puts write data on the FPI Bus which is read by the FPI Bus slave (write cycle) or vice versa (read cycle).

Transfers 2 and 3 show the conflict when two master try to use the FPI Bus and how the conflict is resolved. In the example, the FPI Bus master of transfer 2 has a higher priority than the FPI Bus master of transfer 3.

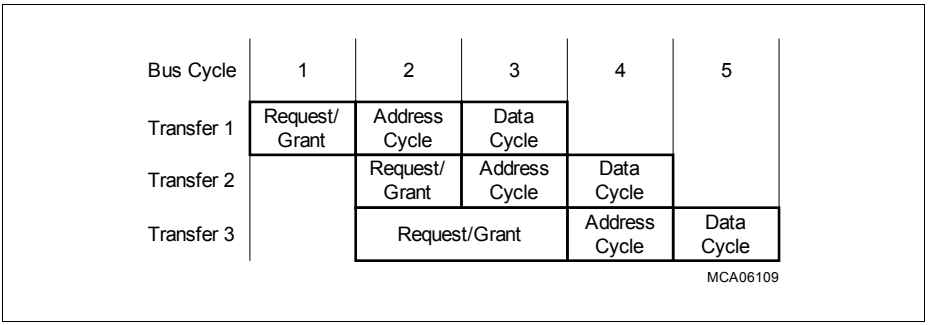


Figure 4-7 Basic FPI Bus Transactions

At a block transfer, the address cycle of a second transfer is extended until the data cycles of the block transfer are finished. In the example of **Figure 4-8**, transfer 1 is a block transfer, while transfer 2 is a single transfer.

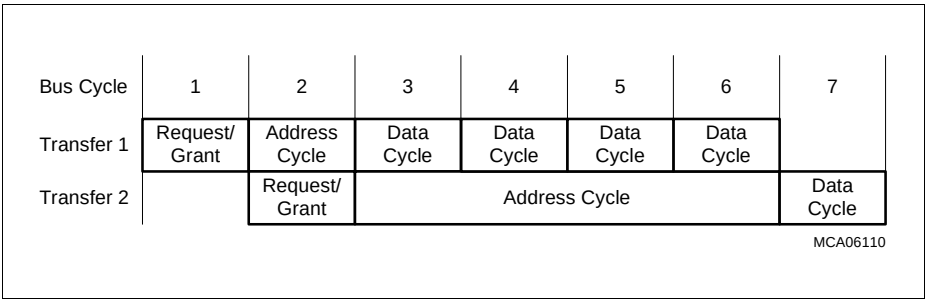


Figure 4-8 FPI Bus Block Transactions

4.5 FPI Bus Control Unit (SBCU)

The TC1798 incorporates one BCU for the SPB, called SBCU.

4.5.1 FPI Bus Arbitration

The arbitration unit of the BCU determines whether it is necessary to arbitrate for FPI Bus ownership, and, if so, which available bus requestor gets the FPI Bus for the next data transfer. During arbitration, the bus is granted to the requesting agent with the highest priority. If no request is pending, the bus is granted to a default master. If no bus master takes the bus, the BCU itself will drive the FPI Bus to prevent it from floating electrically.

4.5.1.1 Arbitration on the System Peripheral Bus

The TC1798 SPB has four bus agents that can become a SPB bus master (DMA, SFI, PCP, SDMA). Each agent is supplied an arbitration priority as shown in **Table 4-11**. DMA controller agent can be assigned to low, medium or high priority by software (via DMA Channel and OCDS control registers).

Table 4-11 Priority of TC1798 SPB Bus Agents

Priority	Agent	Comment
highest	Any bus requestor meeting the starvation protection criteria is assigned this priority	Highest priority, used only for starvation protection
	DMA, high priority	DMA requests from module: - OCDS high priority[1)] - DMA channel with high priority[2)]
	SDMA	
	Peripheral Control Processor (PCP)	Default master 0
	DMA, medium priority	DMA requests from module: - DMA channels with med. priority
	SFI Bridge	Default master 1
lowest	DMA, low priority	DMA requests from modules: - Cerberus low priority[1)] - DMA channels low priority[2)] - MLI

1) Priority of Cerberus transaction at the On Chip Busses is defined by the register bit IOCONF.FPI_PRIO. The register is defined in the OCDS chapter.

2) Priority of a DMA channel is defined by the corresponding CHCRmn.DMAPRIO bits. The registers are defined in the DMA chapter.

If there is no request from an SPB bus master, the SPB is granted to a default master (SFI Bridge or PCP) which has been at last the active master.

4.5.1.2 Starvation Prevention

Starvation prevention is a feature of the SBCU that can take care that even requesting low priority master agents will be granted after a period, where the period length can be controlled by SBCU control registers. Because the priority assignment of the SPB agents is fixed, it is possible that a lower-priority bus requestor may never be granted the bus if a higher-priority bus requestor continuously asks for, and receives, bus ownership. To protect against bus starvation of lower-priority masters, the starvation prevention mechanism of the SBCU will detect such cases and momentarily raise the priority of the lower-priority requestor to the highest priority (above all other priorities), thereby guaranteeing it access.

Starvation protection employs a counter that is decremented each time an arbitration is performed on the connected FPI bus. The counter is re-loaded with the starvation period value in the SBCU_CON.SPC bit field as long it is enabled SBCU_CON.SPE. When this counter is counted down to zero, for each active bus request a request flag is stored in the BCU. This flag is cleared automatically when a master is granted the bus.

When the next period is finished, an active request of a master from which the request flag was set, a starvation event happened. This master will now be set to the highest priority and will be granted service. If there are several masters to which this starvation condition applies, they are served in the order of their hard-wired priority ranking.

If a master that is processing its transaction under starvation condition is retried, its corresponding request flag is automatically again.

Starvation protection can be enabled and disabled through bit SBCU_CON.SPE. The sample period of the counter is programmed through bit field SBCU_CON.SPC. SPC should be set to a value at least greater than or equal to the number of masters. Its reset value is 40_H.

4.5.2 FPI Bus Error Handling

When an error occurs on an FPI Bus, its BCU captures and stores data about the erroneous condition and generates a service request if enabled to do so. The error conditions that force an error-capture are:

- Error Acknowledge: An FPI Bus slave responds with an error to a transaction.
- Un-implemented Address: No FPI Bus slave responds to a transaction request.
- Time-out: A slave does not respond to a transaction request within a certain time window. The number of bus clock cycles that can elapse until a bus time-out is generated is defined by bit field SBCU_CON.TOUT.

When a transaction causes an error, the address and data phase signals of the transaction causing the error are captured and stored in registers.

- The Error Address Capture Register (SBCU_EADD) stores the 32-bit FPI Bus address that has been captured during the erroneous FPI Bus transaction.

- The Error Data Capture Registers (SBCU_EDAT) stores the 32-bit FPI Bus data bus information that has been captured during the erroneous FPI Bus transaction.
- The Error Control Capture Register (SBCU_ECON) stores status information of the bus error event.

If more than one FPI Bus transaction generates a bus error, only the first bus error is captured. After a bus error has been captured, the capture mechanism must be released again by software.

If a write transaction from TriCore causes an error on the SPB, the originating master is not informed about this error as it is not an SPB master agent. With each bus error-capture event, a service request is generated, and an interrupt can be generated if enabled and configured in the corresponding service request register.

Interpreting the BCU Control Register Error Information

Although the address and data values captured in registers SBCU_EADD and SBCU_EDAT, respectively, are self-explanatory, the captured FPI Bus control information needs some more explanation.

Register SBCU_ECON captures the state of the read (RDN), write (WRN), Supervisor Mode (SVM), acknowledge (ACK), ready (RDY), abort (ABT), time-out (TOUT), bus master identification lines (TAG) and transaction operation code (OPC) lines of the FPI Bus.

The SVM signal is set to 1 for an access in Supervisor Mode and set to 0 for an access in User Mode. The time-out signal indicates if there was no response on the bus to an access, and the programmed time (via SBCU_TOUT) has elapsed. TOUT is set to 1 in this case. An acknowledge code has to be driven by the selected slave during each data cycle of an access. These codes are listed in **Table 4-12**.

Table 4-12 FPI Bus Acknowledge Codes

Code (ACK)	Description
00_B	NSC: No Special Condition.
01_B	SPT: Split Transaction (not used in the TC1798).
10_B	RTY: Retry. Slave can currently not respond to the access. Master needs to repeat the access later.
11_B	ERR: Bus Error, last data cycle is aborted.

Transactions on the FPI Bus are classified via a 4-bit operation code (see **Table 4-13**). Note that split transactions (OPC = 1000_B to 1110_B) are not used in the TC1798.

Table 4-13 FPI Bus Operation Codes (OPC)

OPC	Description
0000_B	Single Byte Transfer (8-bit)
0001_B	Single Half-Word Transfer (16-bit)
0010_B	Single Word Transfer (32-bit)
0100_B	2-Word Block Transfer
0101_B	4-Word Block Transfer
0110_B	8-Word Block Transfer
1111	No operation
0011_B, 0111_B, 1000_B - 1110_B	Reserved

4.5.3 BCU Debug Support

For debugging purposes, the BCU has the capability for breakpoint generation support. This OCDS debug capability is controlled by the Cerberus module and must be enabled by it (indicated by bit SBCU_DBCNTL.EO).

When BCU debug support has been enabled (EO = 1), any breakpoint request generated by the BCU to the Cerberus disarms the BCU breakpoint logic for further breakpoint requests. In order to rearm the BCU breakpoint logic again for the next breakpoint request generation, bit SBCU_DBCNTL.RA must be set. The status of the BCU breakpoint logic (armed or disarmed) is indicated by bit SBCU_DBCNTL.OA.

There are three types of trigger events:

- Address triggers
- Signal triggers
- Grant triggers

4.5.3.1 Address Triggers

The address debug trigger event conditions are defined by the contents of the SBCU_DBADR1, SBCU_DBADR2, and SBCU_DBCNTL registers. A wide range of possibilities arise for the creation of debug trigger events based on addresses. The following debug trigger events can be selected:

- Match on one signal address
- Match on one of two signal addresses
- Match on one address area
- Mismatch on one address area

Each pair of DBADRx registers and DBCNTL.ONAx bits determine one possible debug trigger event. The combination of these two possible debug trigger events defined by DBCNTL.CONCOM1 determine the address debug trigger event condition.

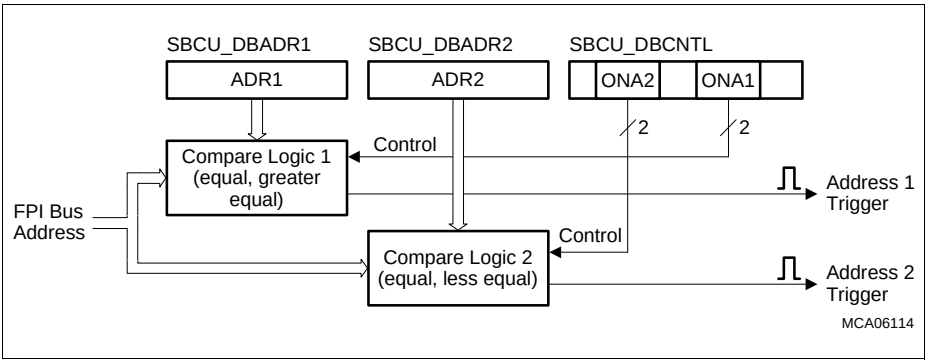


Figure 4-9 Address Trigger Generation

4.5.3.2 Signal Status Triggers

The signal status debug trigger event conditions are defined by the contents of the SBCU_DBBOS and SBCU_DBCNTL registers. Depending on the selected configuration a wide range of possibilities arise for the creation of a debug trigger event based on FPI Bus status signals. Possible combinations are:

- Match on a single signal status
- Match on a multiple signal status

With the multiple signal match conditions, all single signal match conditions are combined with a logical **AND** to the signal status debug trigger event signal. The selection whether or not a single match condition is selected can be enabled/disabled selectively for each condition via the SBCU_DBCNTL.ONBOSx bits.

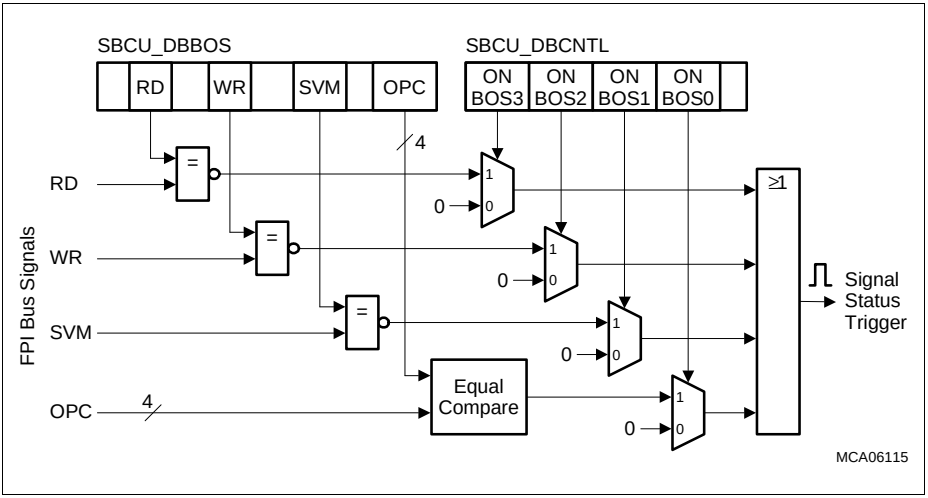


Figure 4-10 Signal Status Trigger Generation

4.5.3.3 Combination of Triggers

The combination of the four debug trigger signals to the single BCU breakpoint trigger event is defined via the bits CONCOM[2:0] of register SBCU_DBCNTL (see **Figure 4-11**). The two address triggers are combined to one address trigger that is further combined with signal status and grant trigger signals. A logical AND or OR combination can be selected for the BCU breakpoint trigger generation.

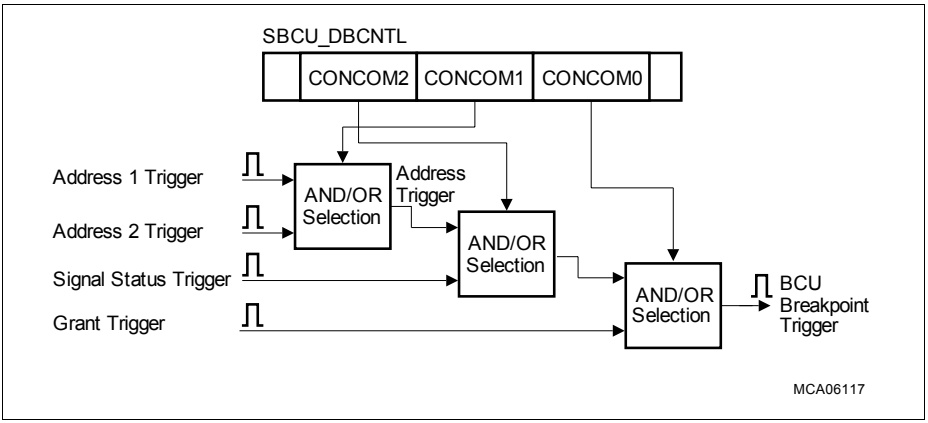


Figure 4-11 BCU Breakpoint Trigger Combination Logic

4.5.3.4 BCU Breakpoint Generation Examples

This section gives three examples of how BCU debug trigger events are programmed.

OCDS Debug Example 1

- Task: Generation of a BCU debug trigger event on any SPB write access to address 00002004_H or $000020A0_H$ by SPB master of the SFI Bridge or the PCP.

For this task, the following programming settings for the BCU breakpoint logic must be executed:

1. Writing SBCU_DBADR1 = 0000 2004_H
2. Writing SBCU_DBADR2 = 0000 $20A0_H$
3. Writing SBCU_DBCNTL = $C1115010_H$:
   a) ONBOS[3:0] = 1100_B means that no signal status trigger is generated (disabled) for a read signal match AND write signal match condition according to the settings of bits RD and WR in register SBCU_DBBOS. Debug trigger event generation for Supervisor Mode signal match and opcode signal match condition is disabled.
   b) ONA2 = 01_B means that the equal match condition for debug address 2 register is selected.

c) ONA1 = 01_B means that the equal match condition for debug address 1 register is selected.
d) ONG = 1 means that the grant debug trigger is enabled.
e) CONCOM[2:0] = 101_B means that the address trigger is created by address trigger 1 OR address trigger 2 (CONCOM1 = 0), and that the grant trigger is ANDed with the address trigger (CONCOM0 = 1), and that the signal status trigger is ANDed with the address trigger (CONCOM2 = 1).
f) RA = 1 means that the BCU breakpoint logic is rearmed.

4. Writing SBCU_DBGRNT = $FFFFFFD7_H$:
means that the grant trigger for the SPB master of the PCP and SFI Bridge is enabled.
5. Writing SBCU_DBBOS = 00001000_H:
means that the signal status trigger is generated on a write transfer and not on a read transfer.

OCDS Debug Example 2

- Task: generation of a BCU debug trigger event on any half-word access in User Mode to address area $01FFFFFF_H$ to $02FFFFFF_H$ by any master.

For this task, the following programming settings for the BCU breakpoint logic must be executed:

1. Writing SBCU_DBADR1 = $01FFFFFF_H$
2. Writing SBCU_DBADR2 = $02FFFFFF_H$
3. Writing SBCU_DBCNTL = 32206010_H:
a) ONBOS[3:0] = 0011_B means that the signal status trigger is disabled for a read or for write signal status match but enabled for Supervisor Mode match AND opcode match conditions according to the settings of bit SVM and bit field OPC in register SBCU_DBBOS.
b) ONA2 = 10_B means that the address 2 trigger is generated if the FPI Bus address is greater or equal to SBCU_DBADR2.
c) ONA1 = 10_B means that the address 1 trigger is generated if the FPI Bus address is greater or equal to SBCU_DBADR1.
d) ONG = 0 means that the grant debug trigger is disabled.
e) CONCOM[2:0] = 110_B means that the address trigger is created by address trigger 1 AND address trigger 2 (CONCOM1 = 1), and that the grant trigger is OR-ed with the address trigger (CONCOM0 = 0), and that the signal status trigger is AND-ed with the address trigger (CONCOM2 = 1).
f) RA = 1 means that the BCU breakpoint logic is rearmed.
4. Writing SBCU_DBGRNT = $FFFFFFFF_H$:
means that no grant trigger for SPB masters is selected (“don’t care” because also disabled by ONG = 0).

5. Writing SBCU_DBBOS = 00000001_H:
   means that the signal status trigger is generated for read (RD = 0) and write (WR = 0) half-word transfers (OPC = 0001_B) in User Mode (SVM = 0).

OCDS Debug Example 3

- Task: Generation of a BCU debug trigger event on any access into address area $01FFFFFF_H$ to $FFFFFFFF_H$ by the PCP.

For this task the following programming settings for the BCU breakpoint logic must be executed:

1. Writing SBCU_DBADR1 = $01FFFFFF_H$
2. Writing SBCU_DBADR2 = don't care
3. Writing SBCU_DBCNTL = 00215010_H:
   a) ONBOS[3:0] = 0000_B means that a signal status trigger is generated for all FPI Bus opcodes not equal to a "no operation" opcode.
   b) ONA2 = 00_B means that no address 2 trigger is generated.
   c) ONA1 = 10_B means that the address 1 trigger is generated if the FPI Bus address is greater or equal to SBCU_DBADR1.
   d) ONG = 1 means that the grant debug trigger is enabled.
   e) CONCOM[2:0] = 101_B means that the address trigger is created by address trigger 1 OR address trigger 2 (CONCOM1 = 0), and that the grant trigger is AND-ed with the address trigger (CONCOM0 = 1), and that the signal status trigger is ANDed with the address trigger (CONCOM2 = 1).
   f) RA = 1 means that the BCU breakpoint logic is rearmed.
4. Writing SBCU_DBGRNT = $FFFFFFF7_H$:
   means that the grant trigger for the SPB bus master of the PCP is enabled.
5. Writing SBCU_DBBOS is "don't care". No signal trigger for SVM, WR, or RD is generated.

4.5.4 System Bus Control Unit Registers

Figure 4-12 and Table 4-15 are showing the address maps with all registers of the System Bus Control Unit (SBCU) module.

SBCU Control Registers Overview

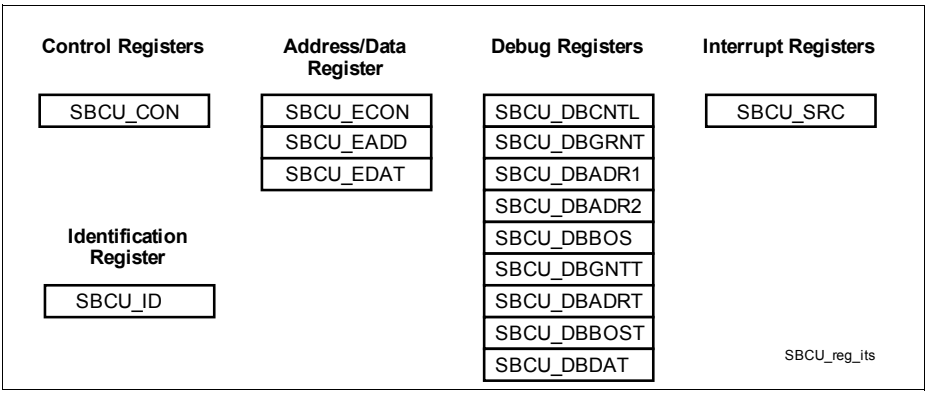


Figure 4-12 SBCU Registers

Table 4-14 Registers Address Space - SBCU Address Space

Module	Base Address	End Address	Note
SBCU	$F000\ 0100_H$	$F000\ 01FF_H$	

Table 4-15 Registers Overview - SBCU Control Registers

Short Name	Description	Offset Addr.[1]	Access Mode		Reset Class	Description See
			Read	Write		
–	Reserved	000_H - 004_H	BE	BE	-	-
SBCU_ID	SBCU Module Identification Register	008_H	U, SV	BE	-	Page 4-82
–	Reserved	$00C_H$	BE	BE	-	-
SBCU_ CON	SBCU Control Register	010_H	U, SV	SV	3	Page 4-83
–	Reserved	014_H - $01C_H$	BE	BE	3	-

Table 4-15 Registers Overview - SBCU Control Registers (cont'd)

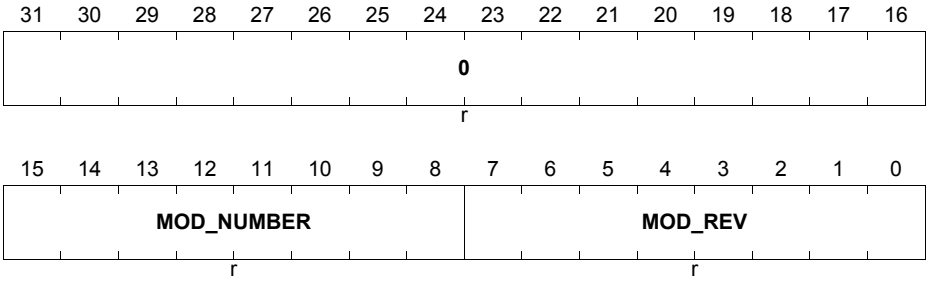
Short Name	Description	Offset Addr.[1]	Access Mode		Reset Class	Description See
			Read	Write		
SBCU_ ECON	SBCU Error Control Capture Register	020_H	U, SV	SV	3	Page 4-84
SBCU_ EADD	SBCU Error Address Capture Register	024_H	U, SV	SV	3	Page 4-86
SBCU_ EDAT	SBCU Error Data Capture Register	028_H	U, SV	SV	3	Page 4-87
–	Reserved	$02C_H$	BE	BE	-	-
SBCU_ DBCNTL	SBCU Debug Control Register	030_H	U, SV	SV	1	Page 4-88
SBCU_ DBGRNT	SBCU Debug Grant Mask Register	034_H	U, SV	SV	1	Page 4-91
SBCU_ DBADR1	SBCU Debug Address Register 1	038_H	U, SV	SV	1	Page 4-93
SBCU_ DBADR2	SBCU Debug Address Register 2	$03C_H$	U, SV	SV	1	Page 4-93
SBCU_ DBBOS	SBCU Debug Bus Operation Signals Register	040_H	U, SV	SV	1	Page 4-94
SBCU_ DBGNTT	SBCU Debug Trapped Master Register	044_H	U, SV	BE	1	Page 4-95
SBCU_ DBADRT	SBCU Debug Trapped Address Register	048_H	U, SV	BE	1	Page 4-97
SBCU_ DBBOST	SBCU Debug Trapped Bus Operation Signals Register	$04C_H$	U, SV	BE	1	Page 4-98
SBCU_ DBDAT	SBCU Debug Data Status Register	050_H	U, SV	BE	1	Page 4-100
–	Reserved	054_H - $0F8_H$	BE	BE	-	-
SBCU_ SRC	SBCU Service Request Control Register	$0FC_H$	U, SV	SV	3	Page 4-102

1) The absolute register address is calculated as follows:
Module Base Address (Table 4-14) + Offset Address (shown in this column)

4.5.4.1 SBCU ID Register Description

The identification register allows the programmer version-tracking of the module. The table below shows the identification register which is implemented in the SBCU module.

SBCU_ID
Module Identification Register **(008_H)** **Reset Value: 0000 6AXX$_H$**

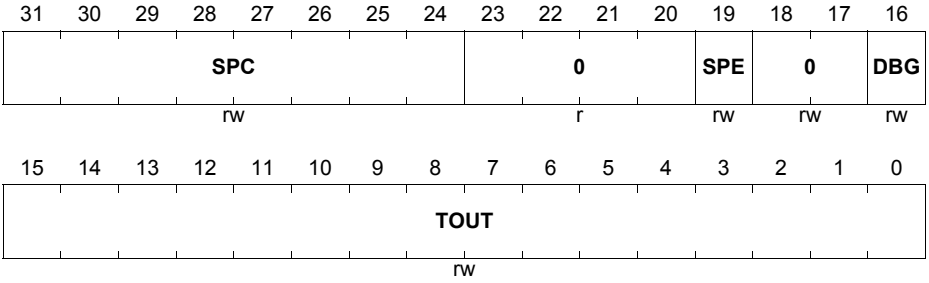


Field	Bits	Type	Description
MOD_REV	[7:0]	r	**Module Revision Number** This bit field defines the module revision number. The value of a module revision starts with 01_H (first revision).
MOD_NUMBER	[15:8]	r	**Module Number Value** This bit field defines a module identification number. The value for the LBCU module is 006AH.
0	[31:16]	r	**Reserved** Read as 0; should be written with 0.

4.5.4.2 SBCU Control Registers Descriptions

The SBCU Control Register controls the overall operation of the SBCU, including setting the starvation sample period, the bus time-out period, enabling starvation-protection mode, and error handling.

SBCU_CON
SBCU Control Register **(010_H)** **Reset Value: $4009\ FFFF_H$**



Field	Bits	Type	Description
TOUT	[15:0]	rw	**SBCU Bus Time-Out Value** The bit field determines the number of System Peripheral Bus time-out cycles. Default after reset is $FFFF_H$ (= 65536 bus cycles). Pls. Note: TOUT value must be >= 5.
DBG	16	rw	**SBCU Debug Trace Enable** 0_B SBCU debug trace disabled 1_B SBCU debug trace enabled (default after reset)
SPE	19	rw	**SBCU Starvation Protection Enable** 0_B SBCU starvation protection disabled 1_B SBCU starvation protection enabled (default after reset)
SPC	[31:24]	rw	**Starvation Period Control** Determines the sample period for the starvation counter. Must be larger than the number of masters. The reset value is 40_H.
0	[18:17], [23:20]	r	**Reserved** Read as 0; should be written with 0.

4.5.4.3 SBCU Error Registers Descriptions

The capture of bus error conditions is enabled by setting SBCU_CON.DBG to 1. In case of a bus error, information about the condition will then be stored in the SBCU error capture registers. The SBCU error capture registers can then be examined by software to determine the cause of the FPI Bus error.

If enabled and an FPI Bus error occurs, the SBCU_ECON register holds the captured FPI Bus control information and an error count of the number of bus errors. The SBCU_EADD register stores the captured FPI Bus address. The SBCU_EDAT register stores the captured FPI Bus data.

If the capture of FPI Bus error conditions is disabled (SBCU_CON.DBG = 0), the SBCU error capture registers remain untouched.

Note: The SBCU error capture registers store only the parameters of the first error. In case of multiple bus errors, an error counter SBCU_ECON.ERRCNT shows the number of bus errors since the first error occurred. An application reset clears this bit field to zero, but the counter can be set to any value through software. This counter is prevented from overflowing, so a value of 2^{16} - 1 indicates that at least this many errors have occurred, but there may have been more. After SBCU_ECON has been read, the SBCU_ECON, SBCU_EADD and SBCU_EDAT registers are re-enabled to trace FPI Bus error conditions.

SBCU_ECON
SBCU Error Control Capture Register (020_H) **Reset Value: $0000\ 0000_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
OPC				TAG				RDN	WRN	SVM	ACK		ABT	RDY	T OUT
rwh				rwh				rwh	rwh	rwh	rwh		rwh	rwh	rwh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ERRCNT															
rwh															

Field	Bits	Type	Description
ERRCNT	[15:0]	rwh	**FPI Bus Error Counter** ERRCNT is incremented on every occurrence of an FPI Bus error. ERRCNT is reset to 0000_H after the SBCU_ECON register is read.[1)]
TOUT	16	rwh	**State of FPI Bus Time-Out Signal** This bit indicates the state of the time-out signal at an FBI Bus error. 0_B No time-out occurred 1_B Time-out has occurred
RDY	17	rwh	**State of FPI Bus Ready Signal** This bit indicates the state of the ready signal at an FBI Bus error. 0_B Wait state(s) have been inserted. Ready signal was active 1_B Ready signal was inactive
ABT	18	rwh	**State of FPI Bus Abort Signal** This bit indicates the state of the abort signal at an FBI Bus error. 0_B Master has aborted an FPI Bus transfer. Abort signal was active 1_B Abort signal was inactive
ACK	[20:19]	rwh	**State of FPI Bus Acknowledge Signals** This bit field indicates the acknowledge code that has been output by the selected slave at an FPI Bus error. Coding see **Table 4-12**.
SVM	21	rwh	**State of FPI Bus Supervisor Mode Signal** This bit indicates whether the FPI Bus error occurred in Supervisor Mode or in User Mode. 0_B Transfer was initiated in User Mode 1_B Transfer was initiated in Supervisor Mode
WRN	22	rwh	**State of FPI Bus Write Signal** This bit indicates whether the FPI Bus error occurred at a write cycle (see**Table 4-16**).
RDN	23	rwh	**State of FPI Bus Read Signal** This bit indicates whether the FPI Bus error occurred at a read cycle (see**Table 4-16**).

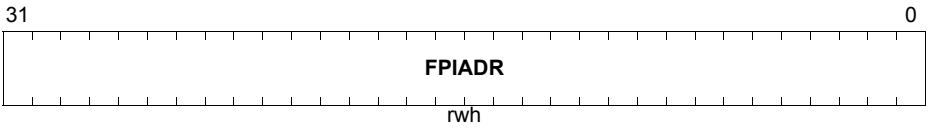
Field	Bits	Type	Description
TAG	[27:24]	rwh	**FPI Bus Master Tag Number Signals** This bit field indicates the FPI Bus master TAG number (definitions see **Table 4-17**).
OPC	[31:28]	rwh	**FPI Bus Operation Code Signals** The FPI Bus operation codes are defined in **Table 4-13**.

1) In the TC1798, aborted accesses to a 0 wait state SPB slave may also increment ERRCNT when the slave generates an error acknowledge.

Table 4-16 FPI Bus Read/Write Error Indication

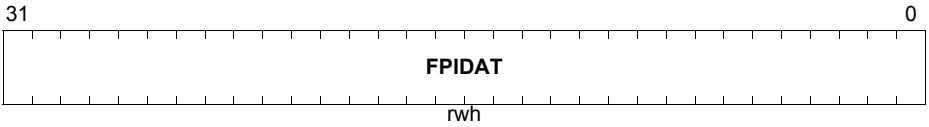
RD	WR	FPI Bus Cycle
0	0	FPI Bus error occurred at the read transfer of a read-modify-write transfer.
0	1	FPI Bus error occurred at a read cycle of a single transfer.
1	0	FPI Bus error occurred at a write cycle of a single transfer or at the write cycle of a read-modify-write transfer.
1	1	Does not occur.

SBCU_EADD
SBCU Error Address Capture Register (024_H) **Reset Value: $0000\ 0000_H$**



Field	Bits	Type	Description
FPIADR	[31:0]	rwh	**Captured FPI Bus Address** This bit field holds the 32-bit FPI Bus address that has been captured at an FPI Bus error. Note that if multiple bus errors occurred, only the address of the first bus error is captured.

SBCU_EDAT
SBCU Error Data Capture Register (028$_H$) **Reset Value: 0000 0000$_H$**



Field	Bits	Type	Description
FPIDAT	[31:0]	rwh	**Captured FPI Bus Data** This bit field holds the 32-bit FPI Bus data that has been captured at an FPI Bus error. Note that if multiple bus errors occurred, only the data of the first bus error is captured.

4.5.4.4 SBCU OCDS Registers Descriptions

SBCU_DBCNTL
SBCU Debug Control Register **(030_H)** **Reset Value: 0000 7003$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ONBOS3	ONBOS2	ONBOS1	ONBOS0	0		ONA2		0		ONA1		0			ONG
rw	rw	rw	rw	r		rw		r		rw		r			rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	CONCOM2	CONCOM1	CONCOM0	0							RA	0		OA	EO
r	rw	rw	rw	r							w	r		r	r

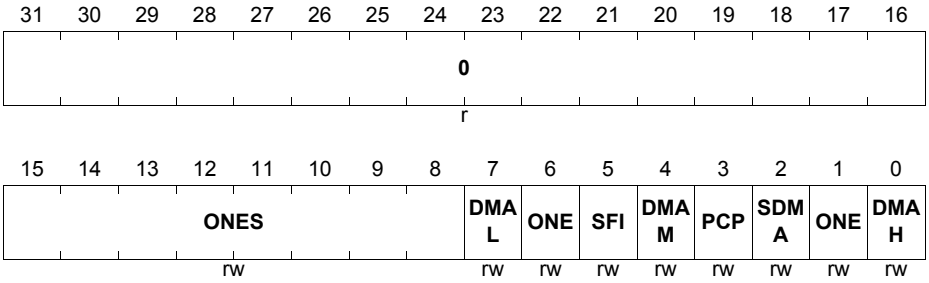
Field	Bits	Type	Description
EO	0	r	**Status of SBCU Debug Support Enable** This bit is controlled by the Cerberus and enables the SBCU debug support. 0_B SBCU debug support is disabled 1_B SBCU debug support is enabled (default after reset)
OA	1	r	**Status of SBCU Breakpoint Logic** 0_B The SBCU breakpoint logic is disarmed. Any further breakpoint activation is discarded 1_B The SBCU breakpoint logic is armed The OA bit is set by writing a 1 to bit RA. When OA is set, registers SBCU_DBGNTT, SBCU_DBADRT, and SBCU_DBBOST are reset.
RA	4	w	**Rearm SBCU Breakpoint Logic** Writing a 1 to this bit rearms SBCU breakpoint logic and sets bit OA = 1. RA is always reads as 0.

Field	Bits	Type	Description
CONCOM0	12	rw	**Grant and Address Trigger Relation** 0_B The grant phase trigger condition and the address trigger condition (see CONCOM1) are combined with a logical OR for further control 1_B The grant phase trigger condition and the address trigger condition (see CONCOM1) are combined with a logical AND for further control (see **Figure 4-11**)
CONCOM1	13	rw	**Address 1 and Address 2 Trigger Relation** 0_B Address 1 trigger condition and address 2 trigger condition are combined with a logical OR to the address trigger condition for further control 1_B Address 1 trigger condition and address 2 trigger condition are combined with a logical AND to the address trigger condition for further control (see **Figure 4-11**)
CONCOM2	14	rw	**Address and Signal Trigger Relation** 0_B Address trigger condition (see CONCOM1) and signal status trigger conditions are combined with a logical OR for further control 1_B Address phase trigger condition (see CONCOM1) and the signal status trigger conditions are combined with a logical AND for further control (see **Figure 4-11**)
ONG	16	rw	**Grant Trigger Enable** 0_B No grant debug event trigger is generated 1_B The grant debug event trigger is enabled and generated according the settings of register SBCU_DBGRNT (see **Figure 4-11**)
ONA1	[21:20]	rw	**Address 1 Trigger Control** 00_B No address 1 trigger is generated 01_B An address 1 trigger event is generated if the FPI Bus address is equal to SBCU_DBADR1 10_B An address 1 trigger event is generated if FPI Bus address is greater or equal to SBCU_DBADR1 11_B same as 00_B (See also **Figure 4-9**).

Field	Bits	Type	Description
ONA2	[25:24]	rw	**Address 2 Trigger Control** 00_B No address 2 trigger is generated 01_B An address 2 trigger event is generated if the FPI Bus address is equal to SBCU_DBADR2 10_B An address 2 trigger event is generated if FPI Bus address is greater or equal to SBCU_DBADR2 11_B same as 00_B See also **Figure 4-9**.
ONBOS0	28	rw	**Opcode Signal Status Trigger Condition** 0_B A signal status trigger is generated for all FPI Bus opcodes except a “no operation” opcode 1_B A signal status trigger is generated if the FPI Bus opcode matches the opcode as defined in DBBOS.OPC (see **Figure 4-10**)
ONBOS1	29	rw	**Supervisor Mode Signal Trigger Condition** 0_B The signal status trigger generation for the FPI Bus Supervisor Mode signal is disabled 1_B A signal status trigger is generated if the FPI Bus Supervisor Mode signal state is equal to the value of DBBOS.SVM (see **Figure 4-10**)
ONBOS2	30	rw	**Write Signal Trigger Condition** 0_B The signal status trigger generation for the FPI Bus write signal is disabled 1_B A signal status trigger is generated if the FPI Bus write signal state is equal to the value of DBBOS.WR (see **Figure 4-10**)
ONBOS3	31	rw	**Read Signal Trigger Condition** 0_B The signal status trigger generation for the FPI Bus read signal is disabled 1_B A signal status trigger is generated if the FPI Bus read signal state is equal to the value of DBBOS.RD (see **Figure 4-10**)

Field	Bits	Type	Description
0	[3:2], [11:5], 15, [19:17], [23:22], [27:26]	r	**Reserved** Read as 0; should be written with 0.

SBCU_DBGRNT
SBCU Debug Grant Mask Register (034_H) Reset Value: 0000 FFFF$_H$



Field	Bits	Type	Description
DMAH	0	rw	**Cerberus Grant Trigger Enable, High Priority**[1)] 0_B FPI Bus transactions with high-priority DMA as bus master are enabled for grant trigger event generation 1_B FPI Bus transactions with high-priority DMA as bus master are disabled for grant trigger event generation
SDMA	2	rw	**SDMA Grant Trigger Enable** 0_B FPI Bus transactions requested by the SDMA bus master are enabled for grant trigger event generation 1_B FPI Bus transactions requested by the SDMA bus master are disabled for grant trigger event generation

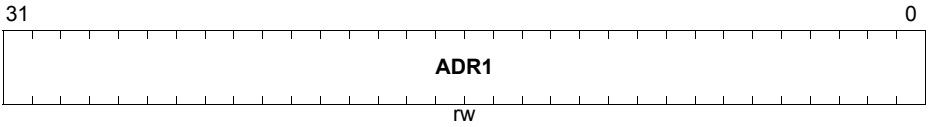
Field	Bits	Type	Description
PCP	3	rw	**PCP Grant Trigger Enable** 0_B FPI Bus transactions with PCP as bus master are enabled for grant trigger event generation 1_B FPI Bus transactions with PCP as bus master are disabled for grant trigger event generation
DMAM	4	rw	**DMA Grant Trigger Enable, Medium Priority**[2)] 0_B FPI Bus transactions with medium-priority DMA channels as bus master are enabled for grant trigger event generation 1_B FPI Bus transactions with medium-priority DMA channels as bus master are disabled for grant trigger event generation
SFI	5	rw	**SFI Bridge Grant Trigger Enable** 0_B FPI Bus transactions with SFI Bridge as bus master are enabled for grant trigger event generation 1_B FPI Bus transactions with SFI Bridge as bus master are disabled for grant trigger event generation
DMAL	7	rw	**DMA Grant Trigger Enable, Low Priority**[3)] 0_B FPI Bus transactions with low-priority DMA channels as bus master are enabled for grant trigger event generation 1_B FPI Bus transactions with low-priority DMA channels as bus master are disabled for grant trigger event generation
ONE, ONES	1, 6, [15:8]	rw	**Reserved** Read as 1 after reset; reading these bits will return the value last written.
0	[31:16]	r	**Reserved** Read as 0; should be written with 0.

1) Including DMA transactions from DMA channels with high priority and from Cerberus with high priority.

2) Including DMA transactions from DMA channels with medium priority.

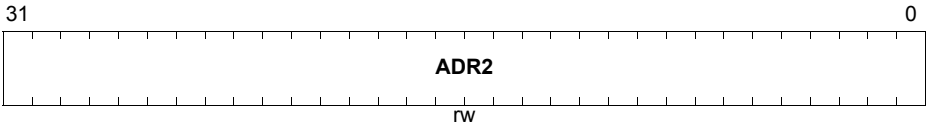
3) Including DMA transactions from DMA channels with low priority, MLI and from Cerberus with low priority.

SBCU_DBADR1
SBCU Debug Address 1 Register (038$_H$) Reset Value: 0000 0000$_H$



Field	Bits	Type	Description
ADR1	[31:0]	rw	**Debug Trigger Address 1** This register contains the address for the address 1 trigger event generation.

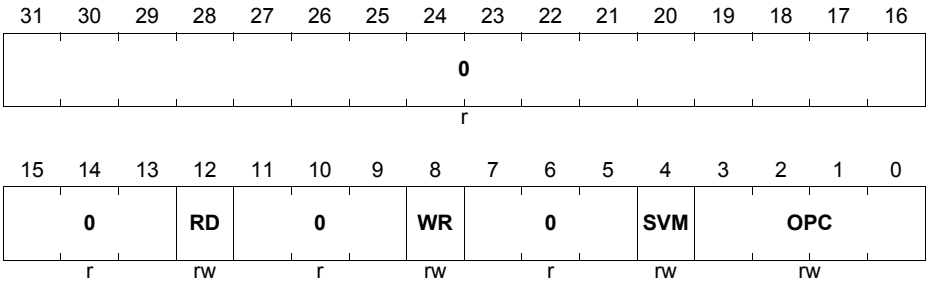
SBCU_DBADR2
SBCU Debug Address 2 Register (03C$_H$) Reset Value: 0000 0000$_H$



Field	Bits	Type	Description
ADR2	[31:0]	rw	**Debug Trigger Address 2** This register contains the address for the address 2 trigger event generation.

SBCU_DBBOS
SBCU Debug Bus Operation Signals Register

(040$_H$) Reset Value: 0000 0000$_H$



Field	Bits	Type	Description
OPC	[3:0]	rw	**Opcode for Signal Status Debug Trigger** This bit field determines the type (opcode) of an FPI Bus transaction for which a signal status debug trigger event is generated (if enabled by DBCNTL.ONBOS0 = 1). 0000_B Trigger on single byte transfer selected 0001_B Trigger on single half-word transfer selected 0010_B Trigger on single word transfer selected 0100_B Trigger on 2-word block transfer selected 0101_B Trigger on 4-word block transfer selected 0110_B Trigger on 8-word block transfer selected 1111_B Trigger on no operation selected Other bit combinations are reserved.
SVM	4	rw	**SVM Signal for Status Debug Trigger** This bit determines the mode of an FPI Bus transaction for which a signal status debug trigger event is generated (if enabled by DBCNTL.ONBOS1 = 1). 0_B Trigger on User Mode selected 1_B Trigger on Supervisor Mode selected

Field	Bits	Type	Description
WR	8	rw	**Write Signal for Status Debug Trigger** This bit determines the state of the $\overline{WR}$ signal of an FPI Bus transaction for which a signal status debug trigger event is generated (if enabled by DBCNTL.ONBOS2 = 1). 0_B Trigger on a single write transfer or write cycle of an atomic transfer selected 1_B No operation or read transaction selected
RD	12	rw	**Write Signal for Status Debug Trigger** This bit determines the state of the $\overline{RD}$ signal of an FPI Bus transaction for which a signal status debug trigger event is generated (if enabled by DBCNTL.ONBOS3 = 1). 0_B Trigger on a single read transfer or read cycle of an atomic transfer selected 1_B No operation or write transfer selected
0	[7:5], [11:9], [31:13]	r	**Reserved** Read as 0; should be written with 0.

SBCU_DBGNTT
SBCU Debug Trapped Master Register

(044_H) **Reset Value: 0000 FFFF$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0								CHNR07	CHNR06	CHNR05	CHNR04	CHNR03	CHNR02	CHNR01	CHNR00
r								rh	rh	rh	rh	rh	rh	rh	rh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ONES								DMAL	ONE	SFI	DMAM	PCP	SDMA	ONE	DMAH
r								rh	rh	rh	rh	rh	rh	r	rh

Field	Bits	Type	Description
DMAH	0	rh	**High-Priority DMA FPI Bus Master Status**[1)] This bit indicates whether the DMA with a high priority request was FPI Bus master when the break trigger event occurred. 0_B The high-priority DMA was not the FPI bus master. 1_B The high-priority DMA was the FPI Bus master.
SDMA	2	rh	**SDMA FPI Bus Master Status** This bit indicates whether the SDMA was FPI Bus master when the break trigger event occurred. 0_B The SDMA was not the FPI bus master. 1_B The SDMA was the FPI Bus master.
PCP	3	rh	**PCP FPI Bus Master Status** This bit indicates whether the PCP was FPI Bus master when the break trigger event occurred. 0_B The PCP was not an FPI bus master. 1_B The PCP was FPI bus master at the break trigger event.
DMAM	4	rh	**Medium-Priority DMA FPI Bus Master Status**[2)] This bit indicates whether the DMA with a medium priority request was FPI Bus master when the break trigger event occurred. 0_B The medium-priority DMA was not the FPI bus master. 1_B The medium-priority DMA was the FPI Bus master.
SFI	5	rh	**SFI Bridge FPI Bus Master Status** This bit indicates whether the SFI Bridge was FPI Bus master when the break trigger event occurred. 0_B The SFI Bridge was not an FPI Bus master. 1_B The SFI Bridge was FPI Bus master.

Field	Bits	Type	Description
DMAL	7	rh	**Low-Priority DMA FPI Bus Master Status**[3] This bit indicates whether the DMA with a low-priority request was the FPI Bus master when the break trigger event occurred. 0_B The low-priority DMA was not the FPI Bus master. 1_B The low-priority DMA was the FPI Bus master.
CHNR0y (y = 0-7)	16+y	rh	**DMA Channel Number Status** These bits indicate which DMA channel with number 0y was active when a DMA break trigger event occurred. 0_B DMA channel 0y was not active at a DMA break trigger event. 1_B DMA channel 0y was active at a DMA break trigger event.
ONE, ONES	1, 6, [15:8]	r	**Reserved** Read as 1; should be written with 0.
0	[31:24]	r	**Reserved** Read as 0; should be written with 0.

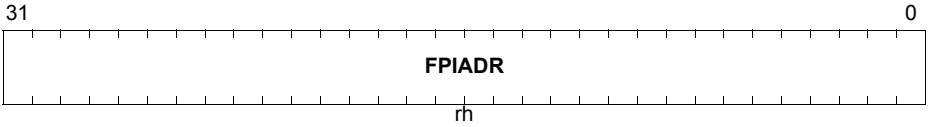
1) Including DMA transactions from DMA channels with high priority and from Cerberus with high priority.

2) Including DMA transactions from DMA channels with medium priority.

3) Including DMA transactions from DMA channels with low priority, MLI and from Cerberus with low priority.

SBCU_DBADRT
SBCU Debug Trapped Address Register

(048_H) **Reset Value: $0000\ 0000_H$**



Field	Bits	Type	Description
FPIADR	[31:0]	rh	**FPI Bus Address Status** This register contains the FPI Bus address that was captured when the OCDS break trigger event occurred.

SBCU_DBBOST
SBCU Debug Trapped Bus Operation Signals Register
($04C_H$) **Reset Value: $0000\ 3180_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0												FPI TAG			
r												rh			

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	FPI TOUT	FPI ABORT	FPI RD	FPI OPS	FPI RST		FPI WR	FPI RDY	FPI ACK		FPI SVM	FPI OPC			
r	rh	rh	rh	rh	rh		rh	rh	rh		rh	rh			

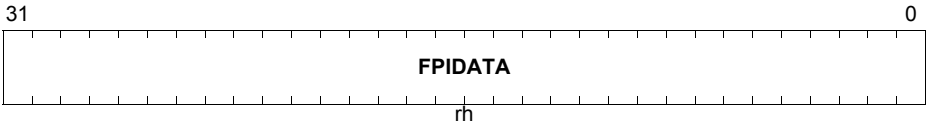
Field	Bits	Type	Description
FPIOPC	[3:0]	rh	**FPI Bus Opcode Status** This bit field indicates the type (opcode) of the FPI Bus transaction captured from the FPI Bus signal lines when the BCU break trigger event occurred. 0000_B Single byte transfer 0001_B Single half-word transfer 0010_B Single word transfer 0100_B 2-word block transfer 0101_B 4-word block transfer 0110_B 8-word block transfer 1111_B No operation Other bit combinations are reserved.
FPISVM	4	rh	**FPI Bus Supervisor Mode Status** This bit indicates the state of the Supervisor Mode signal captured from the FPI Bus signal lines when the BCU break trigger event occurred. 0_B User mode 1_B Supervisor mode

Field	Bits	Type	Description
FPIACK	[6:5]	rh	**FPI Bus Acknowledge Status** This bit field indicates the acknowledge signal status captured from the FPI Bus signal lines when the BCU break trigger event occurred. 00_B No special case 01_B Error 10_B Reserved 11_B Retry, slave did not respond
FPIRDY	7	rh	**FPI Bus Ready Status** This bit indicates the ready signal status captured from the FPI Bus signal lines when the BCU break trigger event occurred. 0_B Last cycle of transfer 1_B Not last cycle of transfer
FPIWR	8	rh	**FPI Bus Write Indication Status** This bit indicates the write signal status captured from the FPI Bus signal lines when the BCU break trigger event occurred. 0_B Single write transfer or write cycle of an atomic transfer 1_B No operation or read transfer
FPIRST	[10:9]	rh	**FPI Bus Reset Status** This bit field indicates the reset signal status captured from the FPI Bus signal lines when the BCU break trigger event occurred. 00_B Reset of all FPI Bus components 11_B No reset Others Reserved
FPIOPS	11	rh	**FPI Bus OCDS Suspend Status** This bit indicates the OCDS suspend signal status captured from the FPI Bus signal lines when the BCU break trigger event occurred. 0_B No OCDS suspend request is pending 1_B An OCDS suspend request is pending

Field	Bits	Type	Description
FPIRD	12	rh	**FPI Bus Read Indication Status** This bit indicates the read signal status captured from the FPI Bus signal lines when the BCU break trigger event occurred. 0_B Single read transfer or read cycle of an atomic transfer 1_B No operation or write transfer
FPIABORT	13	rh	**FPI Bus Abort Status** This bit indicates the abort signal status captured from the FPI Bus signal lines when the BCU break trigger event occurred. 0_B A transfer that has already started was aborted 1_B Normal operation
FPITOUT	14	rh	**FPI Bus Time-out Status** This bit indicates the time-out signal status captured from the FPI Bus signal lines when the BCU break trigger event occurred. 0_B Normal operation 1_B A time-out event was generated
FPITAG	[19:16]	rh	**FPI Bus Master TAG Status** This bit field indicates the master TAG captured from the FPI Bus signal lines when the BCU break trigger event occurred (see **Table 4-17**). The master TAG identifies the master of the transfer which generated BCU break trigger event.
0	15, [31:20]	rh	**Reserved** Read as 0; should be written with 0.

SBCU_DBDAT
SBCU Debug Data Status Register

(050_H) **Reset Value: $0000\ 0000_H$**



Field	Bits	Type	Description
FPIDATA	[31:0]	rh	**FPI Bus Data Status** This register contains the FPI Bus data that was captured when the OCDS break trigger event occurred.

4.5.4.5 SBCU Service Request Control Register Description

In case of a bus error, the SBCU generates an interrupt request to the selected service provider (usually the CPU). This interrupt request is controlled through a standard service request control register.

SBCU_SRC
SBCU Service Request Control Register

($0FC_H$) **Reset Value: $0000\ 0000_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SETR	CLRR	SRR	SRE	0	TOS	0		SRPN							
w	w	rh	rw	r	rw	r		rw							

Field	Bits	Type	Description
SRPN	[7:0]	rw	**Service Request Priority Number**
TOS	10	rw	**Type of Service Control** 0_B CPU service is initiated 1_B PCP request is initiated
SRE	12	rw	**Service Request Enable**
SRR	13	rh	**Service Request Flag**
CLRR	14	w	**Request Clear Bit**
SETR	15	w	**Request Set Bit**
0	[9:8], 11, [31:16]	r	**Reserved** Read as 0; should be written with 0.

Note: Further details on interrupt handling and processing are described in the Interrupt Chapter of this TC1798 User´s Manual.

4.6 On Chip Bus Master TAG Assignments

Each master interface on the FPI Bus and on the SRI Bus is assigned to a 4-bit identification number, the master TAG number (see **Table 4-17**). This makes it possible for software debug and MCDS purposes to distinguish which master has performed the current transaction (see **"XBAR_ERRx (x = 0-6)" on Page 4-51**[1] and **"SBCU_DBADRT" on Page 4-97**).

Table 4-17 On Chip Bus Master TAG Assignments

TAG-Number	Module	Location	Description
0000_B	-	-	Reserved
0001_B	-	-	Reserved
0010_B	PMI	SRI	Program Memory Interface
0011_B	-	-	Reserved
0100_B	DMI	SRI	Data Memory Interface
0101_B	-	-	Reserved
0110_B	-	-	Reserved
0111_B	DMA	SRI	DMA Controller Master Interface on SRI
1000_B	SDMA	SPB	Safe DMA Controller Master Interface on SPB
1001_B	PCP	SPB	Control Processor
1010_B	DMA	SPB	DMA Controller Master Interface on SPB
1011_B	-	-	Reserved
1100_B	-	-	Reserved
1101_B	-	-	Reserved
1110_B	-	-	Reserved
1111_B	-	-	Reserved

1) Pls. note that the Transaction ID bit field in the register **"XBAR_ERRx (x = 0-6)" on Page 4-51** includes the TAG ID on the 4 MSB (TRID[3:0]).

5 Program Memory Unit (PMU)

The Program Memory Unit “PMU” is part of the processor subsystem. The PMUs control the Flash memory and the BootROM and connect these to the SRI bus system.

The devices of the AudoMax and Audo-S families have at least one Program Memory Unit. This is named “PMU0”. With increasing Flash memory more PMUs are added which are named “PMU1”, and so on. All PMUs are independent from each other.

Throughout this document a generic PMU is specified. The **Chapter 5.2** lists the configuration parameters of a PMU and their values in the TC1798. When PMU functionality depends on a parameter this is indicated in the text.

This chapter has the following structure:

- Generic feature list and block diagram (**Chapter 5.1**).
- PMU configuration of the TC1798 (**Chapter 5.2**).
- Functionality of the BootROM (**Chapter 5.3**).
- Functionality of the tuning protection (**Chapter 5.4**).
- Functionality of the Flash memory (**Chapter 5.5**).
- Register Set (**Chapter 5.6**).
- Application Hints (**Chapter 5.7**).

5.1 Generic Feature List

A PMU has dependent on its configuration the following features:

- BootROM (“BROM”).
- Up to 4 MBytes of Program Flash (“PFlash”).
- Up to 256 KByte of Data Flash (“DFlash”).
- Security Flash for SHE (“KeyFlash”).
- SRI slave interface for all assigned Flash memories and registers.
- Flash command control.
- Flash and BROM access control.
- Tuning Protection.
- Interface to security module SHE.

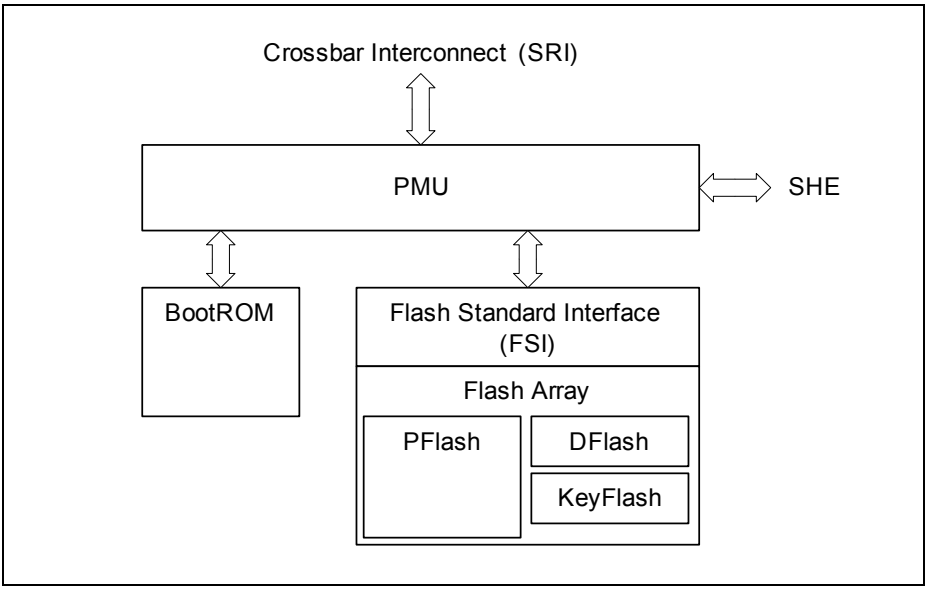


Figure 5-1 PMU Basic Block Diagram

5.2 PMU Configuration of TC1798

The following table defines the PMU configuration of TC1798.

Table 5-1 Configuration of PMU

Parameter	Value	Description
N_PMU	2	Number of PMUs
N_BROM0	1	Number of BROM in PMU0
S_BROM0	16 KByte	Size of the BROM in PMU0
AC_BROM0	8FFF C000$_H$	Base address of the BROM of PMU0 (cached)
AN_BROM0	AFFF C000$_H$	Base address of the BROM of PMU0 (non-cached)
N_PFlash0	1	Number of PFlash in PMU0
S_PFlash0	2 MByte	Size of the PFlash of PMU0
AC_PFlash0	8000 0000$_H$	Base address of the PFlash of PMU0 (cached)
AN_PFlash0	A000 0000$_H$	Base address of the PFlash of PMU0 (non-cached)

Table 5-1 Configuration of PMU (cont'd)

Parameter	Value	Description
AN_UCB0	A000 0000$_H$	Base address of the UCB area of PMU0 (non-cached)
N_DFlash0	1	Number of DFlash in PMU0
S_DFlash0	192 KByte	Size of the DFlash of PMU0
AN_DFlash0_B0	AF00 0000$_H$	Base address of bank 0 of DFlash of PMU0 (non-cached).
S_DFlash0_B0	96 KByte	Size of bank 0 of DFlash of PMU0.
AN_DFlash0_B1	AF08 0000$_H$	Base address of bank 1 of DFlash of PMU0 (non-cached)
S_DFlash0_B1	96 KByte	Size of bank 1 of DFlash of PMU0.
N_KeyFlash0	1	Number of KeyFlash in PMU0
N_RDB0	3	Number of PFlash read buffers in PMU0
N_BROM1	0	Number of BROM in PMU1
N_PFlash1	1	Number of PFlash in PMU1
S_PFlash1	2 MByte	Size of the PFlash of PMU1
AC_PFlash1	8080 0000$_H$	Base address of the PFlash of PMU1 (cached)
AN_PFlash1	A080 0000$_H$	Base address of the PFlash of PMU1 (non-cached)
AN_UCB1	A080 0000$_H$	Base address of the UCB area of PMU1 (non-cached)
N_DFlash1	0	Number of DFlash in PMU1
N_KeyFlash1	0	Number of KeyFlash in PMU1
N_RDB1	3	Number of PFlash read buffers in PMU1

5.2.1 Features of the BootROM

The BootROM contains firmware:

- Startup software "SSW": this software is executed at every reset.
- Test firmware: factory test routines for IFX purposes.

Additionally the BootROM and its control logic support the Tuning Protection.

5.2.2 Features of Program and Data Flash

Depending on the PMU configuration the following Flash features are implemented. Timing and reliability figures are just indicative. Binding data can be found in the “Data Sheet”.

Program Flash “PFlash”

- Consists of one bank.
- Commonly used for instructions and constant data.
- High throughput burst read based on a 256-bit Flash access.
- Application optimized sector structure with sectors ranging from 16 KBytes to 256 KBytes.
- Write protection separately configurable for groups of sectors.
- Hierarchical write protection control with 3 levels of which 2 are password based and 1 is a one-time programmable one.
- Password based read protection combined with write protection for the whole Flash.
- Separate configuration sector containing the protection configuration and IFX specific data.
- High throughput programming of a 256 byte page (see Data Sheet t_{PRP}).
- Erase time per sector: see Data Sheet t_{ERP}.
- All Flash operations initiated by command sequences as protection against unintended operation.
- Erase and program performed by a Flash specific control logic independent of the CPU.
- End of erase and program operations reported by interrupt.
- Dynamic correction of single-bit errors and detection of double-bit errors (“SEC-DED”).
- Error reporting by bus error, interrupts and status flags.
- “Safe read path” ensuring detection of transient and permanent errors.
- Margin reads for quality assurance.
- Delivery in the erased state.
- Configurable wait-state configuration of optimum read performance depending on FSI frequency (see Data Sheet WS_{PF}).
- Endurance and retention figures are documented in the Data Sheet separately for physical sectors (t_{RET}), logical sectors (t_{RETL}) and UCBs (t_{RTU}).
- Pad supply voltage used for program and erase.

Data Flash “DFlash”

As for PFlash but with the following differences:

- Consists of two banks.
- One sector per bank.
- Commonly used for EEPROM emulation (data storage at application run-time).

- Burst read is not supported.
- High throughput programming of a 128 byte page (see Data Sheet t_{PRD}).
- Erase time per sector: see Data Sheet t_{ERD}.
- Dynamic correction of single-bit and double-bit errors and detection of triple-bit errors (“DEC-TED”).
- The high endurance (see Data Sheet N_E) is granted under the condition of a robust EEPROM emulation algorithm (see **Chapter 5.7.3**).
- Configurable wait-state configuration of optimum read performance depending on FSI frequency (see Data Sheet WS_{DF}).

SHE KeyFlash

- Only usable by the SHE module (see corresponding chapter).
- The retention/endurance figure for keys is documented as t_{RETKF} in the Data Sheet.

5.3 BootROM

The content of the BROM is described in a separate chapter.

The BROM is readable and executable for user software but its functions shall only be executed when especially advised by IFX.

All write accesses to the BootROM are refused with a bus error.

In the SRI address range it is mapped to the following start addresses:

- AC_BROM0 (cached address range).
- AN_BROM0 (non-cached address range).

5.4 Tuning Protection

The special tuning protection support represents a security function provided additionally to Flash read/write/OTP protection.

For details on the tuning protection please contact your Infineon representative.

5.5 Flash

This chapter introduces the Flash memory of the TC1798. It is split into the following sections:

- Definition of terms (**Chapter 5.5.1**): what means “program”, “erase”, “sector”, “pages”, …
- Structure of a Flash module (**Chapter 5.5.2**): separation into “banks”, “sectors”, “word-lines”, “pages”, …
- Reading Flash (**Chapter 5.5.3**).
- Command sequences for Flash (**Chapter 5.5.4**): programming, erasing, handling protection.
- Flash protection (**Chapter 5.5.5**): read and write protection.
- Data integrity and safety (**Chapter 5.5.6**): ECC and margin checks.
- Interrupt and traps (**Chapter 5.5.7**).
- Reset and startup (**Chapter 5.5.8**).
- Power reduction by sleep and idle (**Chapter 5.5.9**).

5.5.1 Definition of Terms

The description of Flash memories uses a specific terminology for operations and the hierarchical structure.

Flash Operation Terms

- **Erasing**: The erased state of a Flash cell is logical ‘0’. Forcing a cell to this state is called “erasing”. Depending on the Flash area always complete physical sectors, logical sectors or word-lines are erased. All Flash cells in this area incur one “cycle” that counts for the “endurance”.
- **Programming**: The programmed state of a cell is logical ‘1’. Changing an erased Flash cell to this state is called “programming”. The 1-bits of a page are programmed concurrently.
- **Retention**: This is the time during which the data of a flash cell can be read reliably. The retention time is a statistical figure that depends on the operating conditions of the device (e.g. temperature profile) and is affected by operations on other Flash cells in the same word-line and physical sector. With an increasing number of program/erase cycles (see endurance) the retention is lowered.
- **Endurance**: As described above the data retention is reduced with an increasing number of program/erase cycles. The maximum number of program/erase cycles of each Flash cell is called “endurance”. As said for the retention it is a statistical figure that depends on operating conditions and the use of the flash cells and not to forget on the required quality level. The endurance is documented in the data sheet separately for PFlash physical sectors, PFlash logical sectors, UCBs, DFlash and SHE keys.

Flash Structure Terms

- **Flash Module**: A PMU contains one “Flash module” with its own operation control logic.
- **Bank**: A “Flash module” contains separate “banks”, one for PFlash and two for DFlash. “Banks” support concurrent operations (read, program, erase) with some limitations due to common logic (see **Chapter 5.5.4.4**).
- **Physical Sector**: A Flash “bank” consists of “physical sectors” ranging from 64 KBytes to 256 KBytes. The Flash cells of different “physical sectors” are isolated from each other. Therefore cycling Flash cells in one physical sectors does not affect the retention of Flash cells in other physical sectors. A “physical sector” is the largest erase unit.
- **Logical Sector**: A “logical sector” is a group of word-lines of one physical sector. They can be erased with a single operation but other Flash cells in the same physical sector are slightly disturbed.
- **Sector**: The plain term “sector” means “logical sector” when a physical sector is divided in such, else it means the complete physical sector.
- **User Configuration Block “UCB”**: A “UCB” is a specific logical sector contained in the configuration sector. It contains the protection settings and other data configured by the user. The “UCBs” are the only part of the configuration sector that can be programmed and erased by the user.
- **Configuration Sector**: The “configuration sector” is a separate physical sector of the PFlash. Because of its protection relevant content it is not directly accessible to the user.
- **KeyFlash**: The KeyFlash is used by SHE for storage of keys. It is a separate range of physical sectors in the DFlash bank only accessible to the SHE module.
- **Word-Line**: A “word-line” consists of two pages, an even one and an odd one. In the PFlash area a word-line contains aligned 512 bytes and in the DFlash area 256 bytes.
- **Page**: A “page” is a part of a word-line that is programmed at once. In PFlash a page is an aligned group of 256 bytes and in DFlash 128 bytes.

5.5.2 Flash Structure

The PMU contains the following Flash banks. The offset address of each sector is relative to the base address of its bank which is given in **Table 5-1**. In devices of the same family the Flash banks keep the same base address.

Derived devices (see data sheet) can have less Flash memory. The PFlash bank shrinks by cutting-off higher numbered physical sectors. The DFlash banks shrink by reducing the size of their (single) sectors.

PFlash

All offset addresses based on Ax_PFlashx (see **Table 5-1**). All sectors from S9 on have a size of 256 KByte.

Table 5-2 Sector Structure of PFlash

Sector	Phys. Sector	Size	Offset Address
S0	PS0	16 KB	$00'0000_H$
S1		16 KB	$00'4000_H$
S2		16 KB	$00'8000_H$
S3		16 KB	$00'C000_H$
S4	PS4	16 KB	$01'0000_H$
S5		16 KB	$01'4000_H$
S6		16 KB	$01'8000_H$
S7		16 KB	$01'C000_H$
S8	–	128 KB	$02'0000_H$
S9	–	256 KB	$04'0000_H$
S10	–	256 KB	$08'0000_H$
S11	–	256 KB	$0C'0000_H$
S12	–	256 KB	$10'0000_H$
S13	–	256 KB	$14'0000_H$
S14	–	256 KB	$18'0000_H$
S15	–	256 KB	$1C'0000_H$

DFlash

All offset addresses are based on AN_DFlashx_B0 (see **Table 5-1**).

Table 5-3 Sector Structure of DFlash Bank 0

Sector	Size	Offset Address
DS0	S_DFlashX_B0	$00'0000_H$

All offset addresses are based on AN_DFlashx_B1 (see **Table 5-1**).

Table 5-4 Sector Structure of DFlash Bank 1

Sector	Size	Offset Address
DS1	S_DFlashX_B1	$00'0000_H$

The DFlash contains also the SHE KeyFlash. It can be only used by the SHE module.

UCB

All offset addresses are based on AN_UCBx (see **Table 5-1**). As explained before the UCBx are logical sectors.

Table 5-5 Structure of UCB Area

Sector	Size	Offset Address
UCB0	1 KB	$00'0000_H$
UCB1	1 KB	$00'0400_H$
UCB2	1 KB	$00'0800_H$

5.5.3 Flash Read Access

Flash banks that are active and in read mode can be directly read as ROM.

The wait cycles for the Flash access must be configured as defined in the data sheet or in the chapter “Electrical Parameters”.

The PFlash allows SRI bursts BTR4 and BTR2 and single transfers.

The Tricore uses BTR4 for code fetches from the cached address range in order to fill one cache line. Code fetches from the non-cached area are also performed with BTR4. Data reads from the cached range are performed with BTR4. Data reads from the non-cached address range are performed with single transfers.

The DFlash allows only single transfers. Therefore they are only accessible in the non-cached address range and Tricore can’t fetch instructions from them.

Read accesses from Flash can be blocked by the read protection (see **Chapter 5.5.5**).

Read accesses to the DFlash can be blocked by SHE operations (see **Chapter 5.5.4.4** and **SEMA** on **Page 5-49**).

ECC errors can be detected and corrected (see **Chapter 5.5.6**).

Read Buffers

The PMU contains N_RDBx read buffers. Each of these read buffers is assigned by configuration (see **Chapter 5.6.2.3**) to one bus master. Additionally all read data passes

through a pipeline stage in the FSI called “global read buffer”. The read buffers can be filled with a single PFlash read which delivers 256 data bits.

Read accesses to the DFlash are always serviced by reading the Flash. Buffer hits are not supported.

5.5.4 Flash Operations

The Flash memory knows operations for reading, changing data (program/erase) and handling protection settings. This section and the following describe only the features as such. How to use them is described in the application notes (**Chapter 5.7**).

5.5.4.1 Modes of Operation

A Flash module can be in one of the following states:

- Active (normal) mode.
- Sleep mode (see **Chapter 5.5.8**).

In sleep mode write and read accesses to all Flash ranges of this PMU are refused with a bus error.

When the Flash module is in normal mode each Flash bank can be separately in one of these modes:

- Read mode.
- Command mode.

In read mode a Flash bank can be read and command sequences are interpreted. In read mode a Flash bank can additionally enter page mode which enables it to receive data for programming.

In command mode an operation is performed. During its execution the Flash bank reports BUSY in FSR. In this mode read accesses to this Flash bank are refused with a bus error. At the end of an operation the Flash bank returns to read mode and BUSY is cleared. Only operations with a significant duration (shown in the command documentation) set BUSY.

Register read and write accesses are not affected by these modes.

5.5.4.2 Command Sequences

All Flash operations except read are performed with command sequences. When a Flash bank is in read mode or page mode all write accesses to its reserved address range are interpreted as command cycle belonging to a command sequence. Write accesses to a busy bank cause SQER.

Command sequences consist of 1 to 6 command cycles. The command interpreter checks that a command cycle is correct in the current state of command interpretation. Else a SQER is reported.

When the command sequence is accepted the last command cycle finishes read mode and the Flash bank transitions into command mode.

These write accesses must be single transfers (thus they should address the non-cached address range).

All write accesses transferring write data shall address the Flash bank that will execute the program operation. This Flash bank must be in page mode.

All write accesses of one command sequence must address the same Flash bank.

Command sequences can be blocked by the Flash reservation semaphore (see **Chapter 5.5.4.4** and **SEMA** on **Page 5-49**).

Generally when the command interpreter detects an error it reports a sequence error by setting FSR.SQER. Then the command interpreter is reset and a page mode is left. The next command cycle must be the 1st cycle of a command sequence. The only exception is “Enter Page Mode” when a bank is already in page mode (see below).

5.5.4.3 Command Sequence Definitions

The command sequence descriptions use the following nomenclature (symbolic assembly language):

ST addr, data: Symbolic representation of a command cycle moving “data” to “addr”.

The parameter “addr” can be one of the following:

- **$CCCC_H$**: The “addr” must point into the bank that performs the operation. The last 16 address bits must match $CCCC_H$. It is recommended to use as address the base address of the bank incremented by $CCCC_H$.
- **PA**: Absolute start address of the Flash page.
- **UCPA**: Absolute start address of a user configuration block page.
- **SA**: Absolute start address of a Flash sector. Allowed are the PFlash sectors Sx.
- **PSA**: Absolute start address of a physical sector. Allowed are the PFlash physical sectors PSx and the DFlash sectors DSx.
- **UCBA**: Absolute start address of a user configuration block.

The parameter “data” can be one of the following:

- **WD**: 64-bit or 32-bit write data to be loaded into the page assembly buffer.
- **xxYY**: 8-bit write data as part of a command cycle. Only the byte “YY” is used for command interpretation. The higher order bytes “xx” are ignored.
  - **xx5y**: Specific case for “YY”. The “y” can be “0_H” for selecting the PFlash bank or “D_H” to select the DFlash banks.
- **UL**: User protection level ($xxx0_H$ or $xxx1_H$ for user levels 0 and 1).
- **PWx**: 32-bit password.

When using for command cycles 64-bit transfers the “data” is expected in the correct 32-bit word as indicated by the address “addr”.

Command Sequence Overview Table

The **Table 5-6** summarizes all commands sequences. The following sections describe each command sequence in detail.

Table 5-6 Command Sequences for Flash Control

Command Sequence		1. Cycle	2. Cycle	3. Cycle	4. Cycle	5. Cycle	6. Cycle
Reset to Read	Address Data	.5554 ..xx**F0**					
Enter Page Mode	Address Data	.5554 ..xx**5y**					
Load Page	Address Data	.55F0 **WD**					
Write Page	Address Data	.5554 ..xx**AA**	.AAA8 ..xx**55**	.5554 ..xx**A0**	**PA** ..xx**AA**		
Write UC Page	Address Data	.5554 ..xx**AA**	.AAA8 ..xx**55**	.5554 ..xx**C0**	**UCPA** ..xx**AA**		
Erase Sector	Address Data	.5554 ..xx**AA**	.AAA8 ..xx**55**	.5554 ..xx**80**	.5554 ..xx**AA**	.AAA8 ..xx**55**	**SA** ..xx**30**
Erase Phys Sector	Address Data	.5554 ..xx**AA**	.AAA8 ..xx**55**	.5554 ..xx**80**	.5554 ..xx**AA**	.AAA8 ..xx**55**	**SA** ..xx**40**
Erase UC Block	Address Data	.5554 ..xx**AA**	.AAA8 ..xx**55**	.5554 ..xx**80**	.5554 ..xx**AA**	.AAA8 ..xx**55**	**UCBA** ..xx**C0**
Disable Write Protection	Address Data	.5554 ..xx**AA**	.AAA8 ..xx**55**	.553C **UL**	.AAA8 **PW 0**	.AAA8 **PW 1**	.5558 ..xx**05**
Disable Read Protection	Address Data	.5554 ..xx**AA**	.AAA8 ..xx**55**	.553C ..xx**00**	.AAA8 **PW 0**	.AAA8 **PW 1**	.5558 ..xx**08**
Resume Protection	Address Data	.5554 ..xx**5E**					
Clear Status	Address Data	.5554 ..xx**F5**					

Reset to Read

Calling:

- ST 5554_H, xx$F0_H$

Function:

This function resets the command interpreter to its initial state (i.e. the next command cycle must be the 1st cycle of a sequence). A page mode is aborted.

This command is the only that is accepted without SQER when the command interpreter has already received command cycles of a different sequence but is still not in command

mode. Thus “Reset to Read” can cancel every command sequence before its last command cycle has been received.

The error flags of **FSR** (PFOPER, DFOPER, SQER, PROER, DFSBER, DFCBER, PFDBER, PFMBER, ORIER, VER) and the **XFSR** are cleared. The flags can be also cleared in the status registers without command sequence.

If any Flash bank is busy this command is executed but the flag SQER is set.

Enter Page Mode

Calling:

- ST 5554_H, $xx5y_H$

Function:

The PFlash or the addressed DFlash bank enter page mode. The selection of the PFlash assembly buffer (256 bytes) or the DFlash assembly buffer (128 bytes) is additionally done by the parameter “y_H”.

The write pointer of the page assembly buffer is set to 0, its previous content is maintained.

The page mode is signalled by the flag PAGEx in the FSR separately for PFlash and DFlash.

If a new “Enter Page Mode” command sequence is received while any Flash bank is already in page mode SQER is set but this sequence is correctly executed (i.e. in this case the command interpreter is not reset).

Load Page

Calling:

- ST $55F0_H$, WD (Note: offset $55F4_H$ is used for the higher order 32-bit transfers).

Function:

Loads the data “WD” into the page assembly buffer and increments the write pointer to the next position[1)].

All WD transfers for one page must have the same width (either all 32-bit or all 64-bit). Else the transfer is refused with SQER.

The addressed bank must be in page mode, else SQER is issued.

If “Load Page” is called more often than necessary for filling the page SQER is issued and if configured an interrupt is triggered. The overflow data is discarded. The page mode is not left.

1) More specifically: after “Load Page” has transferred 64 bits (i.e. two command with 32-bit WD or one command with one 64-bit WD) the ECC is calculated and the result is transferred to the assembly buffer.

Write Page

Calling:

- ST 5554_H, $xxAA_H$
- ST $AAA8_H$, $xx55_H$
- ST 5554_H, $xxA0_H$
- ST PA, $xxAA_H$

Function:

This function starts the programming process for one page with the data transferred previously by “Load Page” commands. Upon entering command mode the page mode is finished (indicated by clearing the corresponding PAGE flag) and the BUSY flag of the bank is set.

This command is refused with SQER when the addressed Flash bank is not in page mode.

SQER is also issued when PA addresses an unavailable Flash range or when PA does not point to a legal page start address.

If after “Enter Page Mode” too few data or no data was transferred to the assembly buffer with “Load Page” then “Write Page” programs the page but sets SQER. The missing data is programmed with the previous content of the assembly buffer.

When the page “PA” is located in a sector with active write protection or the Flash module has an active global read protection the execution fails and PROER is set.

Write User Configuration Page

Calling:

- ST 5554_H, $xxAA_H$
- ST $AAA8_H$, $xx55_H$
- ST 5554_H, $xxC0_H$
- ST UCPA, $xxAA_H$

Function:

As for “Write Page”, except that the page “UCPA” is located in a user configuration block. This changes the Flash module’s protection configuration.

When the page “UCPA” is located in an UCB with active write protection or the Flash module has an active global read protection the execution fails and PROER is set.

When UCPA is not the start address of a page in a valid UCB the command fails with SQER.

Erase Sector

Calling:

- ST 5554_H, $xxAA_H$

- ST $AAA8_H$, $xx55_H$
- ST 5554_H, $xx80_H$
- ST 5554_H, $xxAA_H$
- ST $AAA8_H$, $xx55_H$
- ST SA, $xx30_H$

Function:

The sector “SA” is erased.

SQER is returned when SA does not point to the base address of a correct sector (as specified at the beginning of this section) or to an unavailable sector.

When SA has an active write protection or the Flash module has an active global read protection the execution fails and PROER is set.

Erase Physical Sector

Calling:

- ST 5554_H, $xxAA_H$
- ST $AAA8_H$, $xx55_H$
- ST 5554_H, $xx80_H$
- ST 5554_H, $xxAA_H$
- ST $AAA8_H$, $xx55_H$
- ST PSA, $xx40_H$

Function:

The physical sector “PSA” is erased.

SQER is returned when PSA does not point to the base address of a correct sector (as specified at the beginning of this section) or an unavailable sector.

When PSA has an active write protection or the Flash module has an active global read protection the execution fails and PROER is set.

Erase User Configuration Block

Calling:

- ST 5554_H, $xxAA_H$
- ST $AAA8_H$, $xx55_H$
- ST 5554_H, $xx80_H$
- ST 5554_H, $xxAA_H$
- ST $AAA8_H$, $xx55_H$
- ST UCBA, $xxC0_H$

Function:

The addressed user configuration block “UCB” is erased.

When the UCB has an active write protection or the Flash module has an active global read protection the execution fails and PROER is set.

The command fails with SQER when UCBA is not the start address of a valid UCB.

Disable Sector Write Protection

Calling:

- ST 5554_H, $xxAA_H$
- ST $AAA8_H$, $xx55_H$
- ST $553C_H$, UL
- ST $AAA8_H$, PW0
- ST $AAA8_H$, PW1
- ST 5558_H, $xx05_H$

Function:

The sector write protection belonging to user level “UL” is temporarily disabled by setting FSR.WPRODIS when the passwords PW0 and PW1 match their configured values in the corresponding UCB.

The command fails by setting PROER when any of PW0 and PW1 does not match. In this case until the next application reset all further calls of “Disable Sector Write Protection” and “Disable Read Protection” fail with PROER independent of the supplied password.

Disable Read Protection

Calling:

- ST 5554_H, $xxAA_H$
- ST $AAA8_H$, $xx55_H$
- ST $553C_H$, $xx00_H$
- ST $AAA8_H$, PW0
- ST $AAA8_H$, PW1
- ST 5558_H, $xx08_H$

Function:

The Flash module read protection including the derived module wide write protection are temporarily disabled by setting FSR.RPRODIS when the passwords PW0 and PW1 match their configured values in the UCB0.

The command fails by setting PROER when any of PW0 and PW1 does not match. In this case until the next application reset all further calls of “Disable Sector Write Protection” and “Disable Read Protection” fail with PROER independent of the supplied password.

Resume Protection

Calling:

- ST 5554_H, $xx5E_H$

Function:

This command clears all FSR.WPRODISx and the FSR.RPRODIS effectively enabling again the Flash protection as it was configured.

A FSR.WPRODISx is not cleared when corresponding UCBx is not in the “confirmed” state (see **Chapter 5.5.5.3**).

Clear Status

Calling:

- ST 5554_H, $xxF5_H$

Function:

The flags FSR.PROG and FSR.ERASE and the error flags of **FSR** (PFOPER, DFOPER, SQER, PROER, DFSBER, DFCBER, PFDBER, PFMBER, ORIER, VER) and **XFSR** are cleared. These flags can be also cleared in the status registers without command sequence.

When any Flash bank is busy this command fails by setting additionally SQER.

5.5.4.4 Concurrent Operations

Each PMU of a device is independent of the other. Therefore they can be operated concurrently without limitation. Thus also Flash operations in different PMUs can be performed concurrently.

The Flash banks of one Flash module use common resources in Flash and in the PMU. Therefore the concurrent operations are restricted. These are the general rules:

- When the PFlash is not busy reads of all not-busy banks are allowed. This includes margin reads (**Chapter 5.5.6.2**).
- When the PFlash is busy read accesses to DFlash banks shall not be performed but do not cause a bus error.
- Read accesses to busy banks return generally a bus error.
- When any Flash bank is busy with programming the command sequence “Enter Page Mode” must not be executed. The results are unpredictable. Thus at most one programming process can be active.

The following table shows an overview of the allowed combinations. It uses the abbreviations:

- R: Read. Including margin reads (see **Chapter 5.5.6.2**).
- P: Program.
- E: Erase.

- SHE: DFlash reserved for the SHE module.

A ‘/’ indicates that both operations are allowed and ‘–’ that no operation is allowed.

Please note that even if a table row contains more than one “R” the PMU performs only one Flash read access at a time. The table indicates which reads are possible.

Table 5-7 Concurrent Flash Processes

PFlash	DFlash0	DFlash1	Comment
R	R	R	
P/E	–	–	Read of DFlash not supported but does not return a bus error.
R	P/E	R	
R	R	P/E	
R	P	E	When erase started first: “erase suspend”, when program started first: “delayed erase”.
R	E	P	
R	SHE		SHE reserves complete DFlash and prohibits all command sequences.

In all other cases not contained in the table command sequences are forbidden when any Flash bank is busy. This is not automatically prevented by hardware!

The “erase suspend” feature: For EEPROM emulation “Enter Page Mode”, “Load Page” and “Write Page” are accepted for a DFlash page when the other DFlash bank is busy with an erase operation. Suspending the erase operation does typically not exceed t_{FL_ErSusp}. After that the programming is performed and finally the erase operation is automatically resumed.

The “delayed erase” feature: when on one DFlash bank a programming is ongoing an “Erase Sector” or “Erase Physical Sector” sequence is accepted by the PMU. It sets immediately busy but internally the execution of the erase process starts after the programming has finished.

5.5.5 Flash Protection

The Flash memory can be read and write protected. The protection is configured by programming the user configuration blocks “UCB”.

Advice how to use the Flash protection can be found in **Chapter 5.7.5**. This chapter contains only the terse facts.

The SHE module offers a separate possibility to protect Flash content from unauthorized modification or use.

5.5.5.1 Effective Flash Read Protection

The effectiveness of Flash read protection is selected per master. A read access to PFlash or DFlash fails with bus error under the following conditions:

- Tricore PMI (code fetch): FCON.DCF and FCON.RPA.
- Tricore DMI (data read): FCON.DDF and FCON.RPA.
- DMA, SDMA and their submasters: (FCON.DDF and FCON.RPA) or FCON.DDFDMA.
- PCP: (FCON.DDF and FCON.RPA) or FCON.DDFPCP.
- SHE: (FCON.DDF and FCON.RPA) or FCON.DDFSHE.

The read protection bit FCON.RPA is determined during startup by the protection configuration of UCB0. It can be temporarily modified by the command sequences “Disable Read Protection” and “Resume Protection” which modify FSR.RPRODIS. FCON.RPA is determined by the following equation:

- FCON.RPA = PROCON0.RPRO and not FSR.RPRODIS.

The SHE module has always full access to its KeyFlash.

The bits FCON.DDFx and FCON.DCFx are initialized by the startup software depending on the configured protection and the startup mode. They can also be directly modified by the user software under conditions noted in the description of **FCON**.

5.5.5.2 Effective Flash Write Protection

A range of Flash can be write protected by several means:

- The complete PFlash and optionally the complete DFlash can be write protected by the read protection.
- Groups of sectors of PFlash can be write-protected by three different “users”, i.e. UCBs:
  - UCB0: Write protection that can be disabled with the password of UCB0.
  - UCB1: Write protection that can be disabled with the password of UCB1.
  - UCB2: Write protection that can not be disabled anymore (ROM or OTP function: “one-time programmable”).

The write protection is effective independent of the master.

An active write protection causes the program and erase command sequences to fail with a PROER. This was described in the command sequence documentation (**Chapter 5.5.4.3**).

A range “x” (i.e. a group of sectors, see **PROCON0**) of the PFlash is write protected if any of the following conditions is true:

- FCON.RPA
- PROCON2.SxROM
- PROCON0.SxL and not(FSR.WPRODIS0)
- PROCON1.SxL and not(PROCON0.SxL) and not(FSR.WPRODIS1)

Thus with the password of UCB0 the write protection of sectors protected by user 0 and user 1 can be disabled, however with the password of UCB1 only those sectors that are only protected by user 1. The write protection of user 2 (OTP) can be obviously not disabled. The global write protection caused by the read protection can be disabled as described above by using the password of UCB0 to disable the read protection.

The DFlash is write protected if any of the following conditions is true:

- FCON.RPA and not(PROCON0.DFEXPRO).

Thus the DFEXPRO bit can be used to exclude the DFlash from an otherwise global write protection.

5.5.5.3 Configuring Flash Protection in the UCB

As indicated above the effective protection is determined by the content of the PROCON0–2 registers. These are loaded during startup from the UCB0–2. Each UCB comprises 1 KByte of Flash organized in 4 UC pages of 256 bytes. The UCBs have the following structure:

Table 5-8 UCB Content

UC Page	Bytes	UCB0	UCB1	UCB2
0	0–3	PROCON0	PROCON1	PROCON2
	4–7	SHEBOOT0	SHEBOOT1	SHEBOOT2
	8–11	PROCON0 (copy)	PROCON1 (copy)	PROCON2 (copy)
	12–15	SHEBOOT0 (copy)	SHEBOOT1 (copy)	SHEBOOT2 (copy)
	16–19	PW0 of User 0	PW0 of User 1	unused
	20–23	PW1 of User 0	PW1 of User 1	unused
	24–27	PW0 of User 0 (copy)	PW0 of User 1 (copy)	unused
	28–31	PW1 of User 0 (copy)	PW1 of User 1 (copy)	unused
1	unused	unused	unused	unused
2	0–3	confirmation code	confirmation code	confirmation code
	8–11	confirmation code (copy)	confirmation code (copy)	confirmation code (copy)
	other	unused	unused	unused
3	unused	unused	unused	unused

If the confirmation code field is programmed with 8AFE 15C3$_H$ the UCB content is “confirmed” otherwise it is “unconfirmed”. The status flags FSR.PROIN, FSR.RPROIN and FSR.WPROIN0–2 indicate this confirmation state:

- FSR.PROIN: set when any UCB is in the confirmed state.
- FSR.RPROIN: set when PROCON0.RPRO is ‘1’ and the UCB0 is in “confirmed” state.
- FSR.WPROIN0–2: set when their UCB0–2 is in “confirmed” state.

An UCB can be erased with the command “Erase User Configuration Block”. An UCB page can be programmed with the command “Write User Configuration Page”. These commands fail with PROER when the UCB is write-protected.

An UCB is write-protected if:

- UCB0: (FSR.RPROIN and not FSR.RPRODIS) or (FSR.WPROIN0 and not FSR.WPRODIS0)
- UCB1: FSR.WPROIN1 and not FSR.WPRODIS1.
- UCB2: FSR.WPROIN2

So when the UCB2 is in the “confirmed” state its protection can not be changed anymore. Therefore this realizes a one-time programmable protection.

5.5.5.4 System Wide Effects of Flash Protection

An active Flash read protection needs to be respected in the complete system.

The SSW checks if the Flash read protection is active in any PMU, if yes:

- If the selected boot mode executes from internal PFlash.
  - The SSW clears the DCF, DDF and the DDFx.
  - The SSW leaves the debug interface locked (OSTATE.IF_LCK stays 1).
- If the selected boot mode does not execute from internal PFlash:
  - The SSW either leaves DCF and DDF set or actively sets them again in each PMU after evaluating the configuration sector.
  - Additionally the master individual DDFx flags (DDFDMA, DDFPCP, and DDFSHE) are set.
  - The debug interface is unlocked.

If the read protection is inactive in all PMUs the DCF, DDF and DDFx flags are cleared by the SSW and the debug interface is unlocked.

Only depending on the Flash read protection of PMU0 are:

- If the read protection of PMU0 is active the CPU allows only one write access to PMI_CON2 effectively allowing only one instruction cache configuration change. The field PC of the register SMACON which affects the instruction cache is ignored and the value 00_B is used.

Full Flash analysis of an FAR device is only possible when the customer has removed all installed protections or delivers the necessary passwords with the device. As the removal of an OTP protection in UCB2 is not possible the OTP protection inevitably limits analysis capabilities.

5.5.6 Data Integrity and Safety

The data in Flash is stored with error correcting codes “ECC” in order to protect against data corruption. The healthiness of Flash data can be checked with margin checks.

5.5.6.1 ECC

The data in Flash is stored with ECC codes. These are automatically generated when the data is programmed. When data is read these codes are evaluated. Depending on the Flash bank different algorithms with different error correction capabilities are used:

- Data in PFlash uses an ECC code with SEC-DED (Single Error Correction, Double Error Detection) capabilities. Each block of 64 data bits is accompanied with 8 ECC bits.
  Two different algorithms can be selected:
  – Standard ECC as used in previous product generations (default).
  – “Safety ECC” or “Address ECC”: this algorithm calculates the ECC not only over the data bits but additionally over address bits.
- Data in DFlash uses an ECC code with DEC-TED (Double Error Correction, Triple Error Detection) capabilities. Each block of 64 data bits is accompanied with 16 ECC bits.

The selection of the standard PFlash ECC or the “Address ECC” for generation and evaluation is done by the register bit FCON.ADDECC. This is set by the startup software depending on the PROCON0.ADDECC but can also be modified by software.

Standard PFlash ECC

In the standard PFlash ECC the 8-bit ECC value is calculated over 64 data bits. An erased data block (all bits ‘0’) has an ECC value of 00_H. Therefore an erased sector is free of ECC errors. A data block with all bits ‘1’ has an ECC value of FF_H.

The ECC is automatically generated when programming the PFlash when this is not disabled with ECCW.PECENCDIS.

The ECC is automatically evaluated when reading data.

This algorithm has the following capabilities:

- Single-bit error:
  – Is noted in FSR.PFSBER.
  – Data and ECC value are corrected if this is not disabled with ECCR.PECDECDIS.
  – Interrupt is triggered if enabled with FCON.PFSBERM.
- Double-bit error:
  – Is noted in FSR.PFDBER.
  – Is noted in XFSR.PFDBER.
  – Causes a bus error if not disabled by MARP.TRAPDIS.
  – Interrupt is triggered if enabled with FCON.PFDBERM.

Address errors are not detected.

Safety PFlash ECC

The standard ECC can not detect addressing errors, i.e. delivery of a correct data block from an incorrect address. The SRI bus ensures that addressing errors are detected between master and PMU. But addressing errors in the PMU and Flash can not be detected. This missing capability is added by the “Address ECC”.

An 8-bit ECC value is calculated over 64 data bit and the address bits 23:3.

The detection and correction features of the standard ECC are kept as described above.

Additionally the PMU can detect single-bit address corruptions:

- It is noted in FSR.PFDBER[1].
- It is noted in XFSR.PFADER.
- Causes a bus error if not disabled by MARP.TRAPDIS.
- Interrupt is triggered if enabled with FCON.PFDBERM.

As side effect of this ECC algorithm an erased sector (containing 0 data and 0 ECC) can not be read without detecting ECC errors. Thus when this algorithm is enabled data must be programmed before the Flash range may be read.

DFlash ECC

In the DFlash a 16-bit ECC value is calculated over 64 data bits. An erased data block has an ECC value 0000_H. Therefore an erased sector is free of ECC errors. A data block with all bits ‘1’ has an ECC value of $FFFF_H$.

The algorithm has the following capabilities:

- Single-bit error and double-bit error:
  - Is noted in FSR.DFCBER.
  - Data and ECC value are corrected if this is not disabled with ECCR.DECDECDIS.
  - Interrupt is triggered if enabled with FCON.DFCBERM.
- Triple-bit error:
  - Is noted in FSR.DFMBER.
  - Causes a bus error if not disabled by MARD.TRAPDIS.
  - Interrupt is triggered if enabled with FCON.DFMBERM.

Address errors are not detected.

5.5.6.2 Margin Checks

The Flash memory offers a “margin check feature”: the limit which defines if a Flash cell is read as logic ‘0’ or logic ‘1’ can be shifted. This is controlled by the registers **MARP** and **MARD**.

1) This bit is set because it is used in the FSR to notify uncorrectable errors.

The margin selection of PFlash and DFlash is independent. The margin selected with MARD is effective for the complete DFlash.

After changing the read margin at least $t_{FL\_MarginDel}$ have to be waited before reading the affected Flash module.

5.5.7 Interrupts and Traps

Generally the PMU reports fatal errors by issuing a bus error which is translated by the CPU into a trap (PMI sets PSE trap and DMI the DSE trap).

This is a list of conditions for reporting a bus error:

- Uncorrectable ECC error (if not disabled by MARP or MARD).
- Write access to read-only register.
- Not allowed write access to protected register (e.g. SV or ENDINIT).
- Not allowed Flash read access with active read protection.
- Read access to not available Flash memory.
- Read-modify-write access to the Flash memory.
- Read accesses to a busy Flash bank.
- Read accesses to a Flash bank reserved by SHE.

Furthermore selected events can trigger interrupts. The service request node is documented in the SCU. It is controlled by the SCU registers INTSET, INTCLR, INTDIS, INTNP, and INTSTAT. The selection of the events for interrupt triggering is done by **FCON**.

The following events can trigger an interrupt when enabled:

- End of busy: any transition of any of PBUSY, D0BUSY or D1BUSY from ‘1’ to ‘0’ triggers the interrupt (program and erase sequences, wake-up).
- Operational error: see OPER flag.
- Verify error: see VER flag.
- Protection error: see PROER flag.
- Sequence error: see SQER flag.
- Correctable bit-error: read access delivered corrected data.
- Uncorrectable bit-error: read access had an uncorrectable bit error.

The event that triggered the interrupt can be determined from the FSR register.

An interrupt event it also triggered when the event appears again and the corresponding status flag is still set.

5.5.8 Reset and Startup

All PMU and Flash functionality is reset with the application reset with the exception of the register bits: FSR.PROG, FSR.ERASE, FSR.PFOPER, FSR.DFOPER. These bits are reset with the power-on reset.

During Flash startup the logical sectors are checked for an over-erased state (caused by an aborted sector erase) which could prevent read access to all logical sectors of the same physical sector. This feature is configured with **PROCON1** and further described in **Chapter 5.7.8.3**.

During startup after each reset the protection setting is installed from the UCBs. If a protection field has a double-bit error its copy is used. This is indicated by setting FSR.ORIER. If a copy has also a double-bit error the startup software does not enter the user code.

5.5.9 Power Reduction

The Flash module can enter sleep mode to reduce its power consumption. The sleep request can have two sources:

- Global sleep mode requested by the SCU (see “Power Management”). Only executed by the Flash when FCON.ESLDIS = 0.
- Programming ‘1’ to the bit FCON.SLEEP.

After receiving a sleep request the Flash starts the ramp down when the Flash becomes idle, i.e. none of the banks is in command mode and no reads are executed anymore. An ongoing read burst is finished completely. During ramp down to sleep mode all FSR.BUSYx are set.

The sleep mode is indicated in FSR.SLM. The FSR.BUSYx stay set.

The Flash module can be woken up by releasing the sleep request. It enters read mode again after t_{WU}. During the wake-up phase the FSR.BUSYx are set.

Note: It is not recommended to use the SCU controlled sleep mode with FCON.ESLDIS = 0. Because software had to ensure that upon wake-up the Flash is only read after it has returned to read mode. Earlier reads cause bus errors! Therefore the reset value of FCON.ESLDIS is 1.

Note: Requesting sleep mode does not disable automatically an enabled end-of-busy interrupt. When requesting sleep mode during an ongoing Flash operation with enabled end-of-busy interrupt, the operation finishes, the interrupt is issued and then the Flash enters sleep mode. However this end-of-busy interrupt will wake-up the CPU again.

An additional power reduction feature is enabled by setting FCON.IDLE. In this case the PFlash read path is switched off when no read access is pending and the read buffers are filled. System performance is slightly reduced because a flash line hit can not be exploited.

5.6 Register Set

The register set consists of some general PMU registers which are partly only implemented for PMU0 because they control its specific functionality (**Chapter 5.6.1**). The other registers control Flash functionality (**Chapter 5.6.2**). Register fields related to DFlash, KeyFlash and SHE are implemented also when these Flash banks or functionalities are not available but they are without function.

The register access conditions use the following abbreviations:

- "U": Access permitted in User Mode 0 or 1 (applicable to write and read).
- "SV": Access permitted in Supervisor Mode (applicable to write and read).
- "E": ENDINIT protected write. "E" means a write access is only allowed before ENDINIT or after disabling this protection with a password as described in the SCU chapter.
- "–" or "BE": Access not permitted.

The PMU and Flash use the following combinations (see **Table 5-10** and **Table 5-12**):

- U, SV: access always allowed (i.e. in user mode or supervisor mode).
- BE: access never allowed, causing a bus error.
- SV, E: access only in supervisor mode with disabled ENDINIT protection.

All accesses prevented due to these restrictions fail with a bus error.

Also accesses to unoccupied register addresses fail with a bus error.

Note: It is convention to use short register names (e.g. "FCON") in the chapter that defines these registers. In all other chapters and in the development tools long register names are used that are a concatenation of the module instance (e.g. "PMU0" or "FLASH0"), an underscore and the short register name, i.e. "FLASH0_FCON". This document uses for clarification also mostly the long names.

5.6.1 PMU Registers

Non-Flash related registers for the PMU. They have the prefix "PMUx_".

Table 5-9 Registers Address Space

Module	Base Address	End Address	Note
PMU0	$F800\ 0500_H$	$F800\ 052B_H$	
PMU1	$F800\ 0600_H$	$F800\ 062B_H$	

Table 5-10 Registers Overview

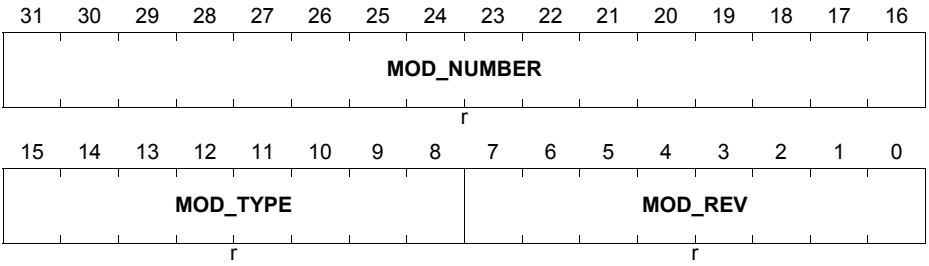
Short Name	Description	Offset Addr.[1]	Access Mode		Reset Class	Page Number
			Read	Write		
ID	Module Identification	08_H	U, SV	BE	3	5-28

1) The absolute register address is calculated as follows:
Module Base Address (Table 5-9) + Offset Address (shown in this column)

5.6.1.1 PMU Identification

The PMU_ID register identifies the PMU and its version.

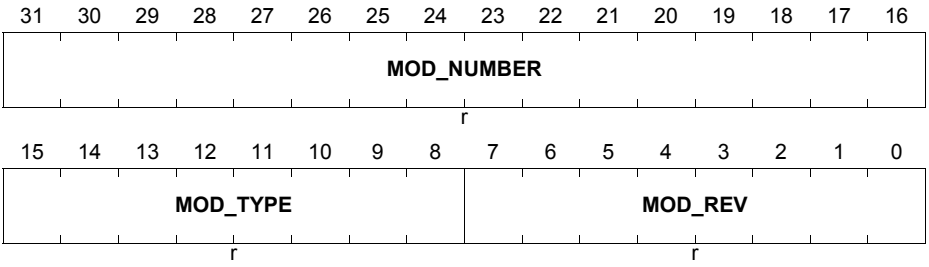
PMU0_ID
PMU0 Identification Register (F800 0508$_H$) Reset Value: 0081 C0XX$_H$



Field	Bits	Type	Description
MOD_REV	[7:0]	r	**Module Revision Number** MOD_REV defines the module revision number. The value of a module revision starts with 01_H (first rev.).
MOD_TYPE	[15:8]	r	**Module Type** This bit field is $C0_H$. It defines the module as a 32-bit module.
MOD_NUMBER	[31:16]	r	**Module Number Value** This bit field defines the module identification number for PMU0.

PMU1_ID

PMU1 Identification Register (F800 0608$_H$) Reset Value: 0082 C0XX$_H$



Field	Bits	Type	Description
MOD_REV	[7:0]	r	**Module Revision Number** MOD_REV defines the module revision number. The value of a module revision starts with 01$_H$ (first rev.).
MOD_TYPE	[15:8]	r	**Module Type** This bit field is C0$_H$. It defines the module as a 32-bit module.
MOD_NUMBER	[31:16]	r	**Module Number Value** This bit field defines the module identification number for PMU1.

5.6.2 Flash Registers

The absolute address of a Flash register is calculated by the base address from Table 5-11 plus the offset address of this register from Table 5-12.

Table 5-11 Registers Address Space

Module	Base Address	End Address	Note
FLASH0	F800 1000$_H$	F800 23FF$_H$	Flash registers of PMU0
FLASH1	F800 3000$_H$	F800 43FF$_H$	Flash registers of PMU1

Table 5-12 Registers Overview

Short Name	Description	Offset Addr.[1]	Access Mode		Reset Class	Page Number
			Read	Write		
ID	Flash Module Identification Register	1008$_H$	U, SV	BE	3	5-47
FSR	Flash Status Register	1010$_H$	U, SV	U, SV	3 [2]	5-32
FCON	Flash Configuration Register	1014$_H$	U, SV	SV, E	3	5-41
MARP	Margin Control Register PFLASH	1018$_H$	U, SV	SV, E	3	5-50
MARD	Margin Control Register DFLASH	101C$_H$	U, SV	U, SV	3	5-51
PROCON0	Flash Protection Config. User 0	1020$_H$	U, SV	BE	3	5-52
PROCON1	Flash Protection Config. User 1	1024$_H$	U, SV	BE	3	5-55
PROCON2	Flash Protection Config. User 2	1028$_H$	U, SV	BE	3	5-58
XFSR	Extended Flash Status Register	102C$_H$	U, SV	U, SV	3	5-39
SEMA	Flash Access Semaphore	1030$_H$	U, SV	U, SV	3	5-49
SHEBOOT0	SHE Secure Boot Configuration 0	1034$_H$	U, SV	BE	3	5-62
SHEBOOT1	SHE Secure Boot Configuration 1	1038$_H$	U, SV	BE	3	5-62

Table 5-12 Registers Overview (cont'd)

Short Name	Description	Offset Addr.[1]	Access Mode		Reset Class	Page Number
			Read	Write		
SHEBOOT2	SHE Secure Boot Configuration 2	$103C_H$	U, SV	BE	3	5-62
RDBCFG0	Read Buffer Configuration 0	1040_H	U, SV	SV, E	3	5-46
RDBCFG1	Read Buffer Configuration 1	1044_H	U, SV	SV, E	3	5-46
RDBCFG2	Read Buffer Configuration 2	1048_H	U, SV	SV, E	3	5-46
ECCW	ECC Write Register	$10E0_H$	U, SV	SV, E	3	5-60
ECCR	ECC Read Register	$10E4_H$	U, SV	SV, E	3	5-61

1) The absolute register address is calculated as follows:
Module Base Address (Table 5-11) + Offset Address (shown in this column)

2) Some bits are not reset with the application reset but only with the power-on reset.

5.6.2.1 Flash Status

The Flash Status Register FSR reflects the overall status of the Flash module after Reset and after reception of the different commands.

The error flags and the two status flags (PROG, ERASE) are affected by the "Clear Status" command. The error flags are also cleared with the "Reset to Read" command.

Some error flags are marked as writable. These flags can be cleared by writing a '1' to this bit.

Flash Status Register

FSR
Flash Status Register **(1010_H)** **Reset Value: $0000\ 0000_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VER	ORIER	0	SLM	0	WPRODIS1	WPRODIS0	0	WPROIN2	WPROIN1	WPROIN0	0	RPRODIS	RPROIN	0	PROIN
rwh	rh	r	rh	r	rh	rh	r	rh	rh	rh	r	rh	rh	r	rh
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DFMBER	PFDBER	DFCBER	PFSBER	PROER	SQER	DFOPER	PFOPER	DFPAGE	PFPAGE	ERASE	PROG	D1BUSY	D0BUSY	FABUSY	PBUSY
rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rh	rh	rwh	rwh	rh	rh	rh	rh

Field	Bits	Type	Description
PBUSY	0	rh	**Program Flash Busy** [1)] HW-controlled status flag. 0_B PFlash ready, not busy; PFlash in read mode. 1_B PFlash busy; PFlash not in read mode. Indication of busy state of PFlash because of active execution of program or erase operation; PFlash busy state is also indicated during Flash startup after reset or in sleep mode; while in busy state, the PFlash is not in read mode.
FABUSY	1	rh	**Flash Array Busy**[1)] Internal busy flag for testing purposes. Must be ignored by application software. This may only use PBUSY, D0BUSY and D1BUSY.
D0BUSY	2	rh	**Data Flash Bank 0 Busy**[1)] HW-controlled status flag. 0_B DFlash0 ready, not busy; DFlash0 in read mode. 1_B DFlash0 busy; DFlash0 not in read mode. Indication of busy state of DFlash bank 0 because of active execution of program or erase operation; DFlash0 busy state is also indicated during Flash startup after reset or in sleep mode; while in busy state the DFlash0 is not in read mode.

Field	Bits	Type	Description
D1BUSY	3	rh	**Data Flash Bank 1 Busy**[1)] HW-controlled status flag. 0_B DFlash1 ready, not busy; DFlash1 in read mode. 1_B DFlash1 busy; DFlash1 not in read mode. Indication of busy state of DFlash bank 1 because of active execution of program or erase operation; DFlash1 busy state is also indicated during Flash startup after reset or in sleep mode; while in busy state the DFlash0 is not in read mode.
PROG	4	rwh	**Programming State** [2)3)] HW-controlled status flag. 0_B There is no program operation requested or in progress or just finished. 1_B Programming operation (write page) requested (from FIM) or in action or finished. Set with last cycle of Write Page command sequence, cleared with Clear Status command (if not busy) or with power-on reset. If one BUSY flag is coincidently set, PROG indicates the type of busy state. If xOPER is coincidently set, PROG indicates the type of erroneous operation. Otherwise, PROG indicates, that operation is still requested or finished. Can be also cleared by writing ‘1’ to it.
ERASE	5	rwh	**Erase State**[2)3)] HW-controlled status flag. 0_B There is no erase operation requested or in progress or just finished 1_B Erase operation requested (from FIM) or in action or finished. Set with last cycle of Erase command sequence, cleared with Clear Status command (if not busy) or with power-on reset. Indications are analogous to PROG flag. Can be also cleared by writing ‘1’ to it.

Field	Bits	Type	Description
PFPAGE	6	rh	**Program Flash in Page Mode** [1)4)] HW-controlled status flag. 0_B Program Flash not in page mode 1_B Program Flash in page mode; assembly buffer of PFlash (256 byte) is in use (being filled up) Set with Enter Page Mode for PFlash, cleared with Write Page command *Note: Concurrent page and read modes are allowed*
DFPAGE	7	rh	**Data Flash in Page Mode**[1)4)] HW-controlled status flag. 0_B Data Flash not in page mode 1_B Data Flash in page mode; assembly buffer of DFlash (128 byte) is in use (being filled up) Set with Enter Page Mode for DFlash, cleared with Write Page command. *Note: Concurrent page and read modes are allowed*
PFOPER	8	rwh	**Program Flash Operation Error**[2)3)4)] 0_B No operation error reported by Program Flash 1_B Flash array operation aborted, because of a Flash array failure, e.g. an ECC error in microcode. This bit is not cleared with application reset, but with power-on reset. Registered status bit; must be cleared per command or by writing ‘1’.
DFOPER	9	rwh	**Data Flash Operation Error**[2)3)4)] Function analogous to Program Flash OPER
SQER	10	rwh	**Command Sequence Error**[1)2)4)] 0_B No sequence error 1_B Command state machine operation unsuccessful because of improper address or command sequence. A sequence error is not indicated if the Reset to Read command aborts a command sequence. Registered status bit; must be cleared per command or by writing ‘1’.

Field	Bits	Type	Description
PROER	11	rwh	**Protection Error**[1)2)4)] 0_B No protection error 1_B Protection error. A Protection Error is reported e.g. because of a not allowed command, for example an Erase or Write Page command addressing a locked sector, or because of wrong password(s) in a protected command sequence such as “Disable Read Protection” Registered status bit; must be cleared per command or by writing ‘1’.
PFSBER	12	rwh	**PFlash Single-Bit Error and Correction**[1)2)4)] 0_B No Single-Bit Error detected during read access to PFlash 1_B Single-Bit Error detected and corrected The error is set when in a 256-bit block read from Flash at least one 64-bit block contained a single-bit error. This is independent of cached/non-cached addressing. Registered status bit; must be cleared per command or by writing ‘1’.
DFCBER	13	rwh	**DFlash Correctable Bit Error and Correction**[1)2)4)] 0_B No Correctable Bit Error detected during read access to DFlash. 1_B Correctable Bit Error detected and corrected. Registered status bit; must be cleared per command or by writing ‘1’.
PFDBER	14	rwh	**PFlash Double-Bit Error**[1)2)4)] 0_B No Double-Bit Error or Address Error detected during read access to PFlash 1_B Double-Bit Error or Address Error detected in PFlash The error is set when in a 256-bit block read from Flash at least one 64-bit block contained a double-bit error. This is independent of cached/non-cached addressing. Registered status bit; must be cleared per command or by writing ‘1’.

Field	Bits	Type	Description
DFMBER	15	rwh	**DFlash Multi-Bit Error**[1)2)4)] 0_B No uncorrectable Multi-Bit Error detected during read access to DFlash 1_B Uncorrectable Multi-Bit Error detected in DFlash Registered status bit; must be cleared per command or by writing '1'.
PROIN	16	rh	**Protection Installed** 0_B No protection is installed 1_B Read or/and write protection for one or more users is configured and correctly confirmed in the User Configuration Block(s). HW-controlled status flag
RPROIN	18	rh	**Read Protection Installed** 0_B No read protection installed 1_B Read protection and global write protection (with or without Data Flash) is configured and correctly confirmed in the User Configuration Block 0. Supported only for the master user (user zero). HW-controlled status flag
RPRODIS	19	rh	**Read Protection Disable State** [1)5)] 0_B Read protection (if installed) is not disabled 1_B Read and global write protection is temporarily disabled. Flash read with instructions from other memory, as well as program or erase on not separately write protected sectors is possible. HW-controlled status flag
WPROIN0	21	rh	**Sector Write Protection Installed for User 0** 0_B No write protection installed for user 0 1_B Sector write protection for user 0 is configured and correctly confirmed in the User Configuration Block 0. HW-controlled status flag

Field	Bits	Type	Description
WPROIN1	22	rh	**Sector Write Protection Installed for User 1** 0_B No write protection installed for user 1 1_B Sector write protection for user 1 is configured and correctly confirmed in the User Configuration Block 1. HW-controlled status flag
WPROIN2	23	rh	**Sector OTP Protection Installed for User 2** 0_B No OTP write protection installed for user 2 1_B Sector OTP write protection with ROM functionality is configured and correctly confirmed in the UCB2. The protection is locked for ever. HW-controlled status flag
WPRODIS0	25	rh	**Sector Write Protection Disabled for User 0**[1)5)] 0_B All protected sectors of user 0 are locked if write protection is installed 1_B All write-protected sectors of user 0 are temporarily unlocked, if not coincidently locked by user 2 or via read protection. Hierarchical protection control: User-0 sectors are also unlocked, if coincidently protected by user 1. But not vice versa. HW-controlled status flag
WPRODIS1	26	rh	**Sector Write Protection Disabled for User 1**[1)5)] 0_B All protected sectors of user 1 are locked if write protection is installed 1_B All write-protected sectors of user 1 are temporarily unlocked, if not coincidently locked by user 0 or user 2 or via read protection. HW-controlled status flag
SLM	28	rh	**Flash Sleep Mode**[1)] HW-controlled status flag. Indication of Flash sleep mode taken because of global or individual sleep request; additionally indicates when the Flash is in shut down mode. 0_B Flash not in sleep mode 1_B Flash is in sleep or shut down mode

Field	Bits	Type	Description
ORIER	30	rh	**Original Error**[1)2)4)] 0_B No original error detected during startup. 1_B Original data replaced by its copy.
VER	31	rwh	**Verify Error**[1)2)4)] 0_B The page is correctly programmed or the sector correctly erased. All programmed or erased bits have full expected quality. 1_B A program verify error or an erase verify error has been detected. Full quality (retention time) of all programmed (“1”) or erased (“0”) bits cannot be guaranteed. See **Chapter 5.7.7.1** and **Chapter 5.7.7.2** for proper reaction. This flag is set when either PFlash, D0Flash, or D1Flash reported VER. Registered status bit; must be cleared per command or writing ‘1’.
0	17,20, 24, 27, 29	r	**Reserved** Read zero, no write

1) Cleared with application reset (class 3 reset)
2) Cleared with command “Clear Status”
3) Cleared with power-on reset (PORST)
4) Cleared with command “Reset to Read”
5) Cleared with command “Resume Protection”

Note: The xBUSY flags as well as the protection flags cannot be cleared with the “Clear Status” command or with the “Reset to Read” command. These flags are controlled by HW.

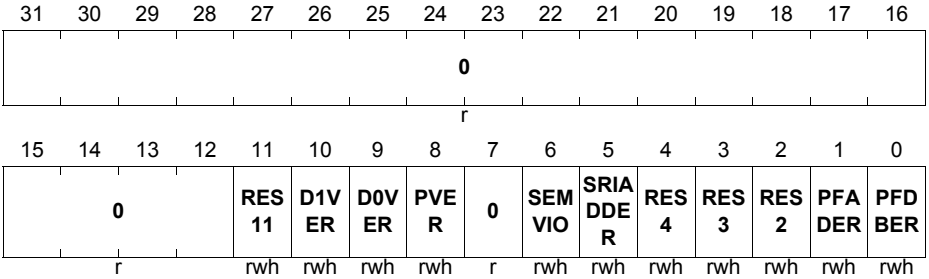
*Note: The reset value above is indicated after correct execution of Flash startup. Additionally, errors are possible after startup (see **Chapter 5.7.7.2**).*

Extended Flash Status Register

The extended Flash status contains additional information about error conditions.

All bits can be cleared by writing a ‘1’ to it. Additionally the complete register is cleared by the command sequences “Reset to Read” and “Clear Status”.

XFSR
Extended Flash Status Register (102C$_H$) Reset Value: 0000 0000$_H$



Field	Bits	Type	Description
PFDBER	0	rwh	**PFlash DBER** A DBER was noted when decoding the ECC of data read from PFlash. The error is set when in a 256-bit block read from Flash at least one 64-bit block contained a double-bit error. This is independent of cached/non-cached addressing.
PFADER	1	rwh	**PFlash Address ECC Error** An address ECC error was noted when decoding the address ECC of data read from PFlash. The error is set when in a 256-bit block read from Flash at least one 64-bit block contained an address ECC error. This is independent of cached/non-cached addressing.
RES2	2	rwh	**Reserved** Status information for internal use.
RES3	3	rwh	**Reserved** Status information for internal use.
RES4	4	rwh	**Reserved** Status information for internal use.
SRIADDERR	5	rwh	**SRI Bus Address ECC Error** This flag is set when the PMU detects an ECC error in the address phase bus transaction on the SRI bus.

Field	Bits	Type	Description
SEMVIO	6	rwh	**Semaphore Violation** When the Flash is reserved by the SHE module command cycles received by any other master set this bit.
PVER	8	rwh	**PFlash Verify Error** A VER was reported during a PFlash operation (see VER in FSR).
D0VER	9	rwh	**D0Flash Verify Error** A VER was reported during a D0Flash operation (see VER in FSR).
D1VER	10	rwh	**D1Flash Verify Error** A VER was reported during a D1Flash operation (see VER in FSR).
RES11	11	rwh	**Reserved** Status information for internal use.
0	[31:12], 7	r	**Reserved;** always read as 0; should be written with 0.

5.6.2.2 Flash Configuration Control

The Flash Configuration Register FCON reflects and controls the following general Flash configuration functions:

- Number of wait states for Flash accesses.
- Indication of installed and active read protection.
- Instruction and data access control for read protection.
- Interrupt mask bits.
- Power reduction and shut down control.

FCON
Flash Configuration Register (1014_H) Reset value: $0007\ 4F08_H$[1)]

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
EOBM	DFMBERM	PFDBERM	DFCBERM	PFSBERM	PROERM	SQERM	VOPERM	ADDECC	DDFSHE	DDFPCP	DDFDMA	0	DDF	DCF	RPA
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	r	rwh	rwh	rh
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SLEEP	ESLDIS	IDLE	WSECDF	WSDFLASH				0	0	0	WSECPF	WSPFLASH			
rw	rw	rw	rw	rw				r	r	r	rw	rw			

1) After Flash startup and execution of the startup SW in BootROM (after firmware exit), the initial value is $000X\ 4F08_H$. The initial value of ADDECC depends on PROCON0.ADDECC.

Field	Bits	Type	Description
WSPFLASH	[3:0]	rw	**Wait States for read access to PFlash** This bitfield defines the number of wait states in number of FSI clock cycles (see SCU chapter CCUCON0), which are used for an initial read access to the Program Flash memory area. 0000_B PFlash access with one wait state 0001_B PFlash access with one wait state 0010_B PFlash access with two wait states 0011_B PFlash access with three wait states 0100_B PFlash access with four wait states 0101_B PFlash access with five wait states 0110_B PFlash access with six wait states 0111_B PFlash access with seven wait states. .... PFlash access with eight up to fourteen wait states. 1111_B PFlash access with fifteen wait states.
WSECPF	4	rw	**Wait State for Error Correction of PFlash** 0_B No additional wait state for error correction 1_B One additional wait state for error correction during read access to Program Flash. If enabled, this wait state is only used for the first transfer of a burst transfer. Set this bit only when requested by Infineon.

Field	Bits	Type	Description
WSDFLASH	[11:8]	rw	**Wait States for read access to DFlash** This bitfield defines the number of wait states in number of FSI clock cycles (see SCU chapter CCUCON0), which are used for a read access to the Data Flash memory area. 0000_B DFlash access with one wait state 0001_B DFlash access with one wait state 0010_B DFlash access with two wait states 0011_B DFlash access with three wait states 0100_B DFlash access with four wait states 0101_B DFlash access with five wait states 0110_B DFlash access with six wait states 0111_B DFlash access with seven wait states. 1000_B DFlash access with eight wait states. .... DFlash access with nine up to fourteen wait states. 1111_B DFlash access with fifteen wait states.
WSECDF	12	rw	**Wait State for Error Correction of DFlash** 0_B No additional wait state for error correction 1_B One additional wait state for error correction during read access to Data Flash Set this bit only when requested by Infineon.
IDLE	13	rw	**Dynamic Flash Idle** 0_B Normal/standard Flash read operation 1_B Dynamic idle of Program Flash enabled for power saving; static prefetching disabled *Note: In Data Flash, dynamic idle is always enabled (prefetching not supported).*
ESLDIS	14	rw	**External Sleep Request Disable** 0_B External sleep request signal input is enabled 1_B Externally requested Flash sleep is disabled The ‘external’ signal input is connected with a global power-down/sleep request signal from SCU.
SLEEP	15	rw	**Flash SLEEP** 0_B Normal state or wake-up 1_B Flash sleep mode is requested, Wake-up from sleep is started with clearing of the SLEEP-bit.

Field	Bits	Type	Description
RPA	16	rh	**Read Protection Activated** This bit monitors the status of the Flash-internal read protection. This bit can only be ‘0’ when read protection is not installed or while the read protection is temporarily disabled with password sequence. 0_B The Flash-internal read protection is not activated. Bits DCF, DDF are not taken into account. Bits DCF, DDFx can be cleared 1_B The Flash-internal read protection is activated. Bits DCF, DDF are enabled and evaluated.
DCF	17	rwh	**Disable Code Fetch from Flash Memory** This bit enables/disables the code fetch from the internal Flash memory area. Once set, this bit can only be cleared when RPA=’0’. This bit is automatically set with reset and is cleared during startup, if no RP installed, and during startup (BootROM SW) in case of internal start out of Flash. 0_B Code fetching from the Flash memory area is allowed. 1_B Code fetching from the Flash memory area is not allowed. This bit is not taken into account while RPA=’0’.
DDF	18	rwh	**Disable Any Data Fetch from Flash** This bit enables/disables the data read access to the Flash memory area (Program Flash and Data Flash). Once set, this bit can only be cleared when RPA=’0’. This bit is automatically set with reset and is cleared during startup, if no RP installed, and during startup (BootROM SW) in case of internal start out of Flash. 0_B Data read access to the Flash memory area is allowed. 1_B Data read access to the Flash memory area is not allowed. This bit is not taken into account while RPA=’0’.

Field	Bits	Type	Description
DDFDMA	20	rw	**Disable Data Fetch from DMA Controller** This bit enables/disables the data read access to PFlash and DFlash memory from the DMA controller, the SDMA controller and other bus masters that access the SRI bus via the DMA peripheral interfaces — these are, dependent on the device: Cerberus, MLI and Memcheck. Once set, this bit can only be cleared when RPA='0'. 0_B The data read access by the DMA, SDMA controller and its peripheral interfaces to the Flash memory area is allowed. 1_B The data read access to the Flash memory area is not allowed for the DMA, SDMA controller and its peripheral interfaces.
DDFPCP	21	rw	**Disable Data Fetch from PCP Controller** This bit enables/disables the data read access to PFlash and DFlash memory via the LFI bridge from PCP controller. Once set, this bit can only be cleared when RPA='0'. 0_B The data read access by the PCP controller to the Flash memory area is allowed. 1_B The data read access to the Flash memory area is not allowed for the PCP controller.
DDFSHE	22	rw	**Disable Data Fetch from SHE Module** This bit enables/disables the data read access to PFlash and DFlash memory via the LFI bridge from the SHE module. Once set, this bit can only be cleared when RPA='0'. 0_B The data read access by the SHE module to the Flash memory area is allowed. 1_B The data read access to the Flash memory area is not allowed for the SHE module.
ADDECC	23	rw	**Address ECC in PFlash** This bit selects if the data in PFlash is written and read with an ECC code that is calculated over address bits (see **Chapter 5.5.6**). 0_B Standard ECC is used. 1_B Address ECC is used. **Attention: this bit must not be changed while accessing Flash (reading, programming, erasing).**

Field	Bits	Type	Description
VOPERM	24	rw	**Verify and Operation Error Interrupt Mask** 0_B Interrupt not enabled 1_B Flash interrupt because of Verify Error or Operation Error in Flash array (FSI) is enabled
SQERM	25	rw	**Command Sequence Error Interrupt Mask** 0_B Interrupt not enabled 1_B Flash interrupt because of Sequence Error is enabled
PROERM	26	rw	**Protection Error Interrupt Mask** 0_B Interrupt not enabled 1_B Flash interrupt because of Protection Error is enabled
PFSBERM	27	rw	**PFlash Single-Bit Error Interrupt Mask** 0_B No Single-Bit Error interrupt enabled 1_B Single-Bit Error interrupt enabled for PFlash
DFCBERM	28	rw	**DFlash Correctable Bit Error Interrupt Mask** 0_B No Correctable Bit Error interrupt enabled 1_B Correctable Bit Error interrupt enabled for DFlash
PFDBERM	29	rw	**PFlash Double-Bit Error Interrupt Mask** 0_B Double-Bit Error interrupt for PFlash not enabled 1_B Double-Bit Error interrupt for PFlash enabled. Especially intended for margin check
DFMBERM	30	rw	**DFlash Multi-Bit Error Interrupt Mask** 0_B Multi-Bit Error interrupt for DFlash not enabled 1_B Multi-Bit Error interrupt for DFlash enabled. Especially intended for margin check
EOBM	31	rw	**End of Busy Interrupt Mask** 0_B Interrupt not enabled 1_B EOB interrupt is enabled
0	[7:5], 19	r	**Reserved** Read/write zero

Note: The default numbers of wait states represent the slow cases. This is a general proceeding and additionally opens the possibility to execute higher frequencies without changing the configuration.

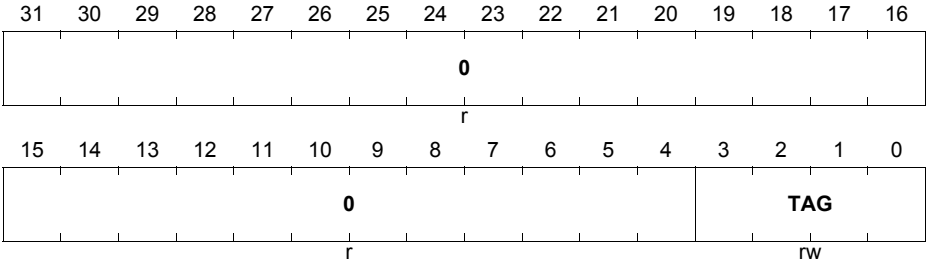
Note: After reset and execution of BootROM startup SW, the read protection control bits are coded as follows:
DDF, DCF, RPA = "110": No read protection installed
DDF, DCF, RPA = "001": Read protection installed; start in internal Flash
DDF, DCF, RPA = "111": Read protection installed; start not in internal Flash.

5.6.2.3 Flash Read Buffer Configuration

The RDBCFG0–2 registers define the assignment of read buffers to masters. The functionality of the read buffers is described in **Chapter 5.5.3**.

It is forbidden to assign more than one read buffer to the same master. The resulting behavior is unpredictable.

RDBCFG0
Read Buffer Cfg 0 **(1040_H)** **Reset Value: $0000\ 0002_H$**
RDBCFG1
Read Buffer Cfg 1 **(1044_H)** **Reset Value: $0000\ 0004_H$**
RDBCFG2
Read Buffer Cfg 2 **(1048_H)** **Reset Value: $0000\ 000D_H$**



Field	Bits	Type	Description
TAG	[3:0]	rw	**Master Tag** This read buffer is assigned to the master with SRI tag = TAG.
0	[31:4]	r	**Reserved** Write 0, read 0.

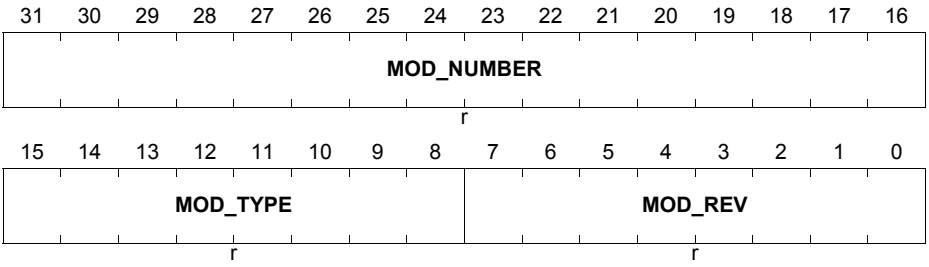
5.6.2.4 Flash Identification Register

The register identifies the Flash module which can have a different version from the PMU.

Flash0 Identification

FLASH0_ID

Flash Module Identification Register (1008_H) **Reset Value: 0083 C0XX$_H$**



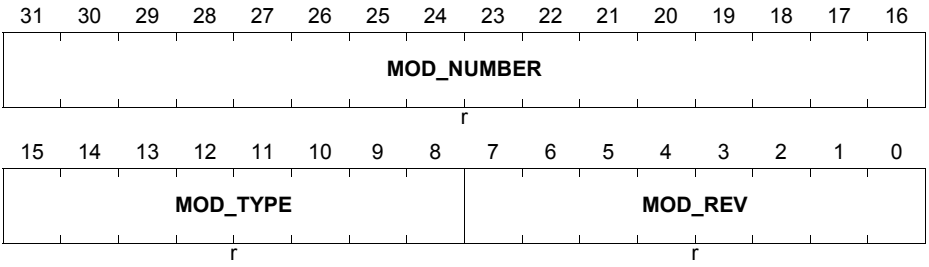
Field	Bits	Type	Description
MOD_REV	[7:0]	r	**Module Revision Number** MOD_REV defines the module revision number. The value of a module revision starts with 01_H (first revision).
MOD_TYPE	[15:8]	r	**Module Type** This bit field is $C0_H$. It defines the module as a 32-bit module.
MOD_NUMBER	[31:16]	r	**Module Number Value** This bit field defines a module identification number. For the TC1798 Flash0 this number is 0083_H.

Flash1 Identification

The second Flash array (Flash1) controlled by PMU1 can have a different feature set from the Flash0 at PMU0, e.g. it typically does not contain a DFlash. Therefore it has another ID number than the Flash0 array.

FLASH1_ID

Flash Module Identification Register (1008_H) **Reset Value: 0084 C0XX$_H$**



Field	Bits	Type	Description
MOD_REV	[7:0]	r	**Module Revision Number** MOD_REV defines the module revision number. The value of a module revision starts with 01_H (first revision).
MOD_TYPE	[15:8]	r	**Module Type** This bit field is $C0_H$. It defines the module as a 32-bit module.
MOD_NUMBER	[31:16]	r	**Module Number Value** This bit field defines a module identification number. For the TC1798 Flash1 this number is 0084_H.

5.6.2.5 Flash Reservation Semaphore

The Flash banks use common resources which limits the concurrency of Flash processes (see **Chapter 5.5.4.4**). This is especially an issue when the SHE module and a Flash EEPROM emulation driver both need access to the DFlash. The Flash user interface is not suitable for multi-master operation. Therefore this semaphore enables different masters or SW threads to reserve the Flash interface.

The bit “SHE” can be set and cleared exclusively by the SHE module using a separate communication path. This is done by the SHE module when it executes commands that need Flash access.

The bits Sx can be set by writing a ‘1’ to this bit. No bit is changed to ‘1’ when already SHE or any Sx is ‘1’ or if the write access contains more than one ‘1’-bit in the Sx positions.

A bit can be cleared by writing a ‘1’ to the corresponding clear bit SxC.

When the SHE bit is set:

- Command cycles are only accepted from the SHE module. All others are rejected with a bus error and set XFSR.SEMVIO.
- Read accesses from DFlash and KeyFlash by any other bus master than SHE fail with a bus error.
- Command cycles addressing the PFlash fail with SQER.
- Further protections (especially of registers) are not activated. The application is responsible to configure the Flash so that it can be operated by the SHE module. This is not security risk because the SHE module verifies all operations.

When an other Sx bit is set the SHE module can not request Flash access. The Sx bits do not affect the hardware operation any further. Flash drivers can use them to organize competing Flash accesses.

This register is also existing in PMU1 and higher. In these the bit SHE is not connected to the SHE module and stays always at ‘0’.

SEMA
Flash Access Semaphore **(1030_H)** **Reset Value: $0000\ 0000_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
S7C	S7	S6C	S6	S5C	S5	S4C	S4	S3C	S3	S2C	S2	S1C	S1	0	SHE
w	rwh	w	rwh	w	rwh	w	rwh	w	rwh	w	rwh	w	rwh	r	rh

Field	Bits	Type	Description
SHE	0	rh	**SHE Semaphore** If set only the SHE module has full Flash access (see **Chapter 5.5.4.4**)
Sx (x=1-7)	2*x	rwh	**Semaphore x** This bit can be written to ‘1’ if no other Sx or the SHE bit is ‘1’. This bit can be cleared by writing a ‘1’ to the corresponding SxC.
SxC (x=1-7)	2*x+1	w	**Semaphore x Clear** Writing a ‘1’ clears the corresponding Sx. Read 0.

Field	Bits	Type	Description
0	[31:16], 1	r	**Reserved** Write 0, read 0.

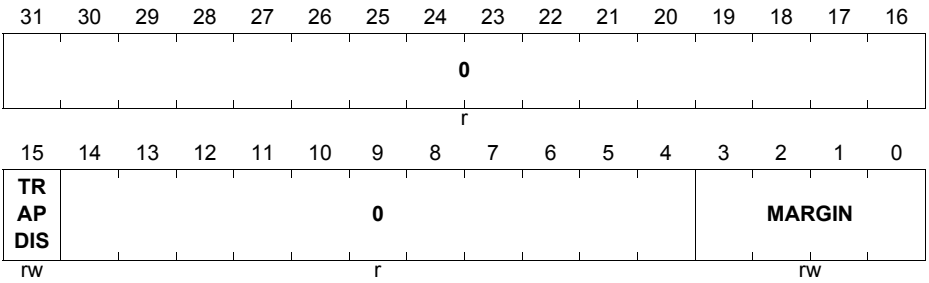
5.6.2.6 Margin Check Control

Note: Although double-bit error traps are disabled with reset, the traps are enabled by the startup SW (firmware) in Boot ROM before Boot ROM exit.

Margin Check Control PFlash

MARP

Margin Control Register PFLASH (1018$_H$) **Reset Value: 0000 8000$_H$**



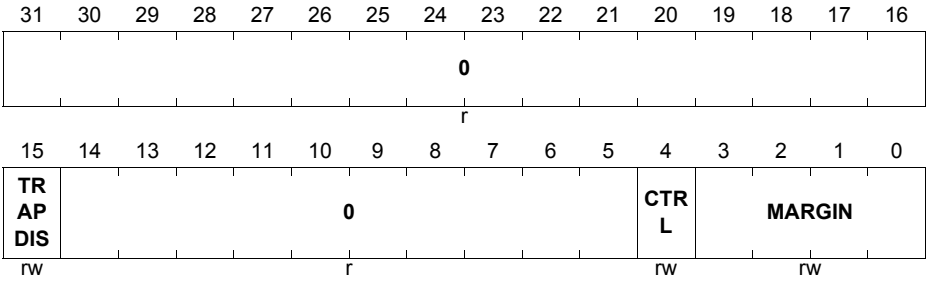
Field	Bits	Type	Description
MARGIN	[3:0]	rw	**PFLASH Margin Selection** 0000_B **Default**, Standard (default) margin. 0001_B **Tight0**, Tight margin for 0 (low) level. Suboptimal 0-bits are read as 1s. 0100_B **Tight1**, Tight margin for 1 (high) level. Suboptimal 1-bits are read as 0s. – Reserved.
TRAPDIS	15	rw	**PFLASH Double-Bit Error Trap Disable** 0_B If a double-bit error occurs in PFLASH, a bus error trap is generated[1]. 1_B The double-bit error trap is disabled. Shall be used only during margin check
0	[14:4], [31:16]	r	**Reserved;** always read as 0; should be written with 0.

1) After Boot ROM exit, double-bit error traps are enabled (TRAPDIS = 0).

Margin Check Control DFlash

MARD

Margin Control Register DFLASH (101C$_H$) **Reset Value: 0000 8000$_H$**



Field	Bits	Type	Description
MARGIN	[3:0]	rw	**DFLASH Margin Selection** 0000$_B$ **Default**, Standard (default) margin. 0001$_B$ **Tight0**, Tight margin for 0 (low) level. Suboptimal 0-bits are read as 1s. 0100$_B$ **Tight1**, Tight margin for 1 (high) level. Suboptimal 1-bits are read as 0s. – Reserved.
CTRL	4	rw	**Margin Control Enable** 0_B The active read margin for both DFLASH banks is determined by MARGIN. 1_B Both DFlash banks are read with standard (default) margin independently of MARGIN.
TRAPDIS	15	rw	**DFLASH Multiple-Bit Error Trap Disable** 0_B If an uncorrectable multi-bit error occurs in DFLASH, a bus error trap is generated[1]. 1_B The multi-bit error trap is disabled. Shall be used only during margin check
0	[14:5], [31:16]	r	**Reserved;** always read as 0; should be written with 0.

1) After Boot ROM exit, multi-bit error traps are enabled (TRAPDIS = 0).

5.6.2.7 Protection Configuration Indication

The configuration of read/write/OTP protection is indicated with registers PROCON0, PROCON1 and PROCON2, thus separately for every user, and it is generally indicated in the status register FSR.

The three PROCONx registers are read-only registers. They are defined as follows:

Protection Configuration for User 0

PROCON0
Flash Protection Config. User 0 (1020_H) Reset Value: 0000 0000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RPRO	DFEXPRO	ADDECC	RES												S22/S23L
rh	rh	rh	rh												rh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
S20/S21L	S18/S19L	S16/S17L	S14/S15L	S12/S13L	S10/S11L	S9L	S8L	S7L	S6L	S5L	S4L	S3L	S2L	S1L	S0L
rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh

Field	Bits	Type	Description
SnL (n=0-9)	n	rh	**Sector n Locked for Write Protection by User 0** These bits indicate whether PFLASH sector n is write-protected by user 0 or not. 0_B No write protection is configured for sector n. 1_B Write protection is configured for sector n.
S10/S11L	10	rh	**Sectors 10 and 11 Locked for Write Protection by User 0** This bit indicates whether PFLASH sectors 10+11 (together 512 KB) are write-protected by user 0 or not. 0_B No write protection is configured for sectors 10+11. 1_B Write protection is configured for sectors 10+11.

Field	Bits	Type	Description
S12/S13L	11	rh	**Sectors 12 and 13 Locked for Write Protection by User 0** This bit indicates whether PFLASH sectors 12+13 (together 512 KB) are write-protected by user 0 or not. 0_B No write protection is configured for sectors 12+13. 1_B Write protection is configured for sectors 12+13.
S14/S15L	12	rh	**Sectors 14 and 15 Locked for Write Protection by User 0** This bit indicates whether PFLASH sectors 14+15 (together 512 KB) are write-protected by user 0 or not. 0_B No write protection is configured for sectors 14+15. 1_B Write protection is configured for sectors 14+15.
S16/S17L	13	rh	**Reserved: Sectors 16 and 17 Locked for Write Protection by User 0** This bit indicates whether PFLASH sectors 16+17 (together 512 KB) are write-protected by user 0 or not. 0_B No write protection is configured for sectors 16+17. 1_B Write protection is configured for sectors 16+17.
S18/S19L	14	rh	**Reserved: Sectors 18 and 19 Locked for Write Protection by User 0** This bit indicates whether PFLASH sectors 18+19 (together 512 KB) are write-protected by user 0 or not. 0_B No write protection is configured for sectors 18+19. 1_B Write protection is configured for sectors 18+19.

Field	Bits	Type	Description
S20/S21L	15	rh	**Reserved: Sectors 20 and 21 Locked for Write Protection by User 0** This bit indicates whether PFLASH sectors 20+21 (together 512 KB) are write-protected by user 0 or not. 0_B No write protection is configured for sectors 20+21. 1_B Write protection is configured for sectors 20+21.
S22/S23L	16	rh	**Reserved: Sectors 22 and 23 Locked for Write Protection by User 0** This bit indicates whether PFLASH sectors 22+23 (together 512 KB) are write-protected by user 0 or not. 0_B No write protection is configured for sectors 22+23. 1_B Write protection is configured for sectors 22+23.
ADDECC	29	rh	**Address ECC Configuration** This bit is evaluated by SSW to initialize FCON.ADDECC.
DFEXPRO	30	rh	**Data Flash Excluded from Read Protection** When read protection is configured this bit determines whether the DFLASH shall be excluded from read protection and global write protection or not. 0_B DFLASH not excluded from read protection and global write protection. 1_B DFLASH is excluded from read/write protection; read protection and global write protection is configured by user 0 only for the PFLASH
RPRO	31	rh	**Read Protection Configuration** This bit indicates whether read protection is configured for PFLASH and DFLASH by user 0. 0_B No read protection configured 1_B Read protection and global write protection is configured by user 0 (master user)

Field	Bits	Type	Description
RES	[28:17]	rh	**Reserved** Deliver the corresponding content of UCB0.

Protection Configuration for User 1

PROCON1
Flash Protection Config. User 1 (1024_H) **Reset Value: $0000\ 0000_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ALSEDIS								SPREC	RES						S22/S23L
rh								rh	rh						rh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
S20/S21L	S18/S19L	S16/S17L	S14/S15L	S12/S13L	S10/S11L	S9L	S8L	S7L	S6L	S5L	S4L	S3L	S2L	S1L	S0L
rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh

Field	Bits	Type	Description
SnL (n=0-9)	n	rh	**Sector n Locked for Write Protection by User 1** These bits indicate whether PFLASH sector n is write-protected by user 1 or not. 0_B No write protection is configured for sector n. 1_B Write protection is configured for sector n.
S10/S11L	10	rh	**Sectors 10 and 11 Locked for Write Protection by User 1** This bit indicates whether PFLASH sectors 10+11 (together 512 KB) are write-protected by user 1 or not. 0_B No write protection is configured for sectors 10+11. 1_B Write protection is configured for sectors 10+11.

Field	Bits	Type	Description
S12/S13L	11	rh	**Sectors 12 and 13 Locked for Write Protection by User 1** This bit indicates whether PFLASH sectors 12+13 (together 512 KB) are write-protected by user 1 or not. 0_B No write protection is configured for sectors 12+13. 1_B Write protection is configured for sectors 12+13.
S14/S15L	12	rh	**Sectors 14 and 15 Locked for Write Protection by User 1** This bit indicates whether PFLASH sectors 14+15 (together 512 KB) are write-protected by user 1 or not. 0_B No write protection is configured for sectors 14+15. 1_B Write protection is configured for sectors 14+15.
S16/S17L	13	rh	**Reserved: Sectors 16 and 17 Locked for Write Protection by User 1** This bit indicates whether PFLASH sectors 16+17 (together 512 KB) are write-protected by user 1 or not. 0_B No write protection is configured for sectors 16+17. 1_B Write protection is configured for sectors 16+17.
S18/S19L	14	rh	**Reserved: Sectors 18 and 19 Locked for Write Protection by User 1** This bit indicates whether PFLASH sectors 18+19 (together 512 KB) are write-protected by user 1 or not. 0_B No write protection is configured for sectors 18+19. 1_B Write protection is configured for sectors 18+19.

Field	Bits	Type	Description
S20/S21L	15	rh	**Reserved: Sectors 20 and 21 Locked for Write Protection by User 1** This bit indicates whether PFLASH sectors 20+21 (together 512 KB) are write-protected by user 1 or not. 0_B No write protection is configured for sectors 20+21. 1_B Write protection is configured for sectors 20+21.
S22/S23L	16	rh	**Reserved: Sectors 22 and 23 Locked for Write Protection by User 1** This bit indicates whether PFLASH sectors 22+23 (together 512 KB) are write-protected by user 1 or not. 0_B No write protection is configured for sectors 22+23. 1_B Write protection is configured for sectors 22+23.
SPREC	23	rh	**SPREC** Soft-Programming Recover. 0_B Program 1-data. 1_B Soft Recover. See **Chapter 5.7.8.3**.
ALSEDIS	[31:24]	rh	**ALSE Disable** Each bit of ALSEDIS[7:0] corresponds to one of the logical sectors S[7:0]. If a bit is set the logical sector is not checked for an aborted erase nor is any of the repair algorithms performed. See **Chapter 5.7.8.3**.
RES	[22:17]	rh	**Reserved** Deliver the corresponding content of UCB1.

Protection Configuration for User 2

PROCON2
Flash Protection Config. User 2 (1028_H) **Reset Value: 0000 0000_H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RES 31	DATM	RES													S22/ S23 ROM
rh	rh							rh							rh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
S20/ S21 ROM	S18/ S19 ROM	S16/ S17 ROM	S14/ S15 ROM	S12/ S13 ROM	S10/ S11 ROM	S9 ROM	S8 ROM	S7 ROM	S6 ROM	S5 ROM	S4 ROM	S3 ROM	S2 ROM	S1 ROM	S0 ROM
rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh

Field	Bits	Type	Description
SnROM (n=0-9)	n	rh	**Sector n Locked Forever by User 2** These bits indicate whether PFLASH sector n is an OTP protected sector with read-only functionality, thus if it is locked for ever. 0_B No ROM functionality configured for sector n. 1_B ROM functionality is configured for sector n. Re-programming of this sector is no longer possible.
S10/S11ROM	10	rh	**Sectors 10 and 11 Locked Forever by User 2** This bit indicates whether PFLASH sectors 10+11 (together 512 KB) are read-only sectors or not. 0_B No ROM functionality is configured for sectors 10+11. 1_B ROM functionality is configured for sectors 10+11.
S12/S13ROM	11	rh	**Sectors 12 and 13 Locked Forever by User 2** This bit indicates whether PFLASH sectors 12+13 (together 512 KB) are read-only sectors or not. 0_B No ROM functionality is configured for sectors 12+13. 1_B ROM functionality is configured for sectors 12+13.

Field	Bits	Type	Description
S14/S15ROM	12	rh	**Sectors 14 and 15 Locked Forever by User 2** This bit indicates whether PFLASH sectors 14+15 (together 512 KB) are read-only sectors or not. 0_B No ROM functionality is configured for sectors 14+15. 1_B ROM functionality is configured for sectors 14+15.
S16/S17ROM	13	rh	**Reserved: Sectors 16 and 17 Locked Forever by User 2** This bit indicates whether PFLASH sectors 16+17 (together 512 KB) are read-only sectors or not. 0_B No ROM functionality is configured for sectors 16+17. 1_B ROM functionality is configured for sectors 16+17.
S18/S19ROM	14	rh	**Reserved: Sectors 18 and 19 Locked Forever by User 2** This bit indicates whether PFLASH sectors 18+19 (together 512 KB) are read-only sectors or not. 0_B No ROM functionality is configured for sectors 18+19. 1_B ROM functionality is configured for sectors 18+19.
S20/S21ROM	15	rh	**Reserved: Sectors 20 and 21 Locked Forever by User 2** This bit indicates whether PFLASH sectors 20+21 (together 512 KB) are read-only sectors or not. 0_B No ROM functionality is configured for sectors 20+21. 1_B ROM functionality is configured for sectors 20+21.
S22/S23ROM	16	rh	**Reserved: Sectors 22 and 23 Locked Forever by User 2** This bit indicates whether PFLASH sectors 22+23 (together 512 KB) are read-only sectors or not. 0_B No ROM functionality is configured for sectors 22+23. 1_B ROM functionality is configured for sectors 22+23.

Field	Bits	Type	Description
DATM	30	rh	**Disable ATM** This bit indicates if the ATM “Application Test Mode” is disabled or not. 0_B ATM is enabled. 1_B ATM is disabled. This bit is only used in PMU0.
RES31	31	rh	**Reserved** Deliver the corresponding content of UCB2.
RES	[29:17]	rh	**Reserved** Deliver the corresponding content of UCB2.

5.6.2.8 Flash ECC Access

ECC Write Register

The Error Correction Code Write register ECCW contains bits for disabling the ECC encoding separately for PFlash and DFlash.

When disabling the ECC encoding for PFlash with PECENCDIS = ‘1’ the 8-bit ECC code for the next 64-bit data block transferred from PMU to the Flash assembly buffer is taken from ECCW.WCODEL.

When disabling the ECC encoding for DFlash with DECENCDIS = ‘1’ the 16-bit ECC code for the next 64-bit data block transferred from PMU to the Flash assembly buffer is taken from ECCW.WCODEH (bits 15:8) and ECCW.WCODEL (bits 7:0).

Because of internal dependencies only one of PECENCDIS or DECENCDIS may be set to ‘1’.

ECCW
ECC Write Register **($10E0_H$)** **Reset Value: $0000\ 0000_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PECENCDIS	DECENCDIS	0													
rw	rw	r													

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WCODEH								WCODEL							
rw								rw							

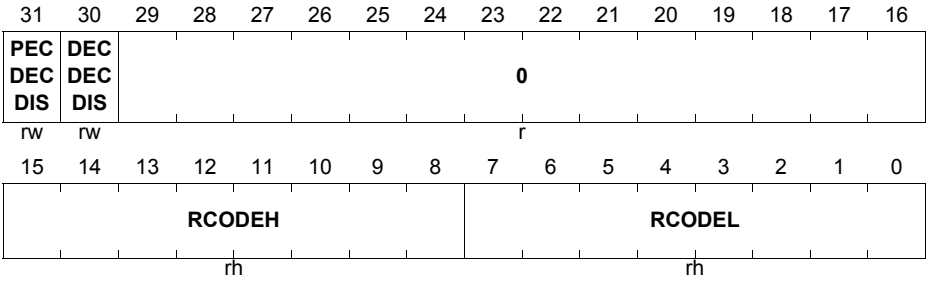
Field	Bits	Type	Description
WCODEL	[7:0]	rw	**Error Correction Write Code Low** 8-bit ECC code for the current 64-bit write buffer to be written into the assembly buffer instead of generated ECC.
WCODEH	[15:8]	rw	**Error Correction Write Code High** 8-bit ECC code for the current 64-bit write buffer to be written into the assembly buffer instead of generated ECC.
DECENCDIS	30	rw	**DFlash ECC Encoding Disable** 0_B The ECC code is automatically calculated. 1_B The ECC code is taken from WCODEH and WCODEL.
PECENCDIS	31	rw	**PFlash ECC Encoding Disable** 0_B The ECC code is automatically calculated. 1_B The ECC code is taken from WCODEL.
0	[29:16]	r	**Reserved;** always read as 0.

ECC Read Register

The Error Correction Code Read register ECCR allows to disable the ECC correction. The ECC decoding (i.e. the error detection) is not influenced. If necessary the trap generation has to be separately disabled by MARP.TRAPDIS and MARD.TRAPDIS. Further on this register allows to read the uncorrected ECC code.

The ECC code of the last read access is stored in ECCR.RCODEx. For PFlash reads the 8-bit ECC code is stored in ECCR.RCODEL and for DFlash the 16-bit ECC code is stored in ECCR.RCODEH and ECCR.RCODEL.

ECCR
ECC Read Register **($10E4_H$)** **Reset value: $0000\ 0000_H$**

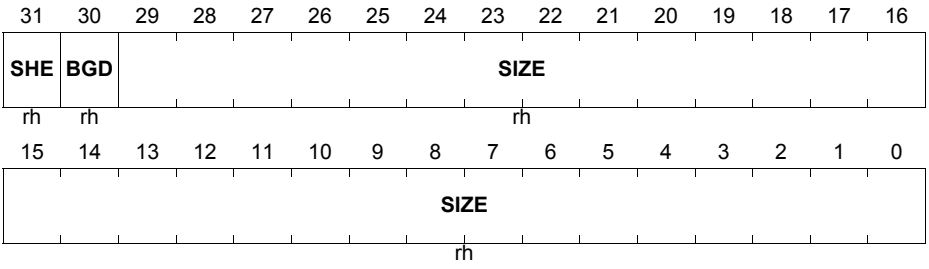


Field	Bits	Type	Description
RCODEL	[7:0]	rh	**Error Correction Read Code Low** 8-Bit ECC code, read from the Flash read buffer with last data read operation. For PFlash this is the complete ECC value. For DFlash this is the lower half of the 16-bit ECC value.
RCODEH	[15:8]	rh	**Error Correction Read Code High** 8-Bit ECC code, read from the Flash read buffer with last data read operation. Unused for PFlash reads. For DFlash this is the upper half of the 16-bit ECC value.
DECDECDIS	30	rw	**DFlash ECC Decoding Disable** 0_B ECC correction for DFlash enabled. 1_B ECC correction for DFlash disabled.
PECDECDIS	31	rw	**PFlash ECC Decoding Disable** 0_B ECC correction for PFlash enabled. 1_B ECC correction for PFlash disabled.
0	[29:16]	r	**Reserved;** always read as 0.

5.6.2.9 SHE Secure Internal Flash Boot

The SHEBOOT0–2 registers supply the bytes 4–7 of the user configuration blocks 0–2. As documented in the SHE chapter these fields can be used to configure a secure boot from internal Flash.

SHEBOOTx (x=0-2)
SHE Secure Boot Cfg **(1034_H+4*x)** **Reset Value: 0000 0000_H**



Field	Bits	Type	Description
SHE	31	rh	**Secure Boot Enable** As documented in the SHE chapter this bit enables the secure boot from internal Flash with SIZE taken as size of the boot loader.
BGD	30	rh	**Background Secure Boot** As documented in the SHE chapter the secure boot can be performed in background or foreground. 0_B **FGD**, Foreground secure boot. 1_B **BGD**, Background secure boot.
SIZE	[29:0]	rh	**SHE Bootloader Size** Byte length of the SHE bootloader.

5.7 Application Hints

The following application hints should support the user in using the PMU and Flash optimally.

5.7.1 Changes with Respect to Audo-NG and Audo-F

The following changes of the PMU with respect to Audo-NG and Audo-F products are highlighted:

- Changed bus interface from LMB to SRI.
- No bus “retry” anymore in case of reading busy flash banks. Always a bus error is triggered.
- The wait-state settings in FCON don’t relate to the bus clock as in Audo-F (i.e. the LMB clock) but to the FSI clock. This clock has its own divider from the PLL clock which needs to be configured in SCU_CCUCON0.FSIDIV. It must be configured to have a relation f_{SRI}/f_{FSI} or 2/1 or 1/1.
- Enhanced Flash read buffer concept with master specific read buffers.
- The OVRAM and the EMEM were moved to a different module “LMU”.
- Support of SHE
  - Software handling Flash memory should negotiate Flash access with SHE module using the SEMA semaphore.
  - Different content of UCBs supporting SHE secure boot function. New SHEBOOTx registers.
  - DDFSHE flag in FCON.
  - Handling key storage for SHE in additional private sectors of the DFlash.
- Configuration of ALSE with UCB1: possibility to disable ALSE for selected logical sectors.
- DFEXPRO set independent of RPROIN.
- TP: changed address RTPWT. Changed configuration. See separate documentation.
- Programming and reading data with disabled ECC generation and correction allows customers to program data with invalid ECC.
- Error flags in FSR can be selectively cleared to enable easier flag handling for concurrent operations.
- New extended status register XSFR.
- Reorganization of PROCONs due to extended memory range.
- Changed base addresses of all Flash modules.
- DEC-TED ECC algorithm in DFlash.
- Address ECC and normal SEC-DED ECC in PFlash.
  Attention: this feature can cause incompatibility of Audo-NG/F Flash drivers with this device.

5.7.2 Performing Flash Operations

This section offers advice for programming command sequences.

General Advice

- Code that performs PFlash programming or erasing must not be executed from the same PFlash.
- The command cycles shall address the non-cached address range of the Flash (otherwise the data may stay in the cache or could be received by the PMU in an incorrect order).
- The non-cached Flash range is not regarded as peripheral address space by the TriCore. This means that a read (notably reading the FSR for checking the flags) placed behind the last command cycle write in program order might be executed before this last write.
  The FSR flags PAGE, PROG, ERASE can be used to ensure that polling for a cleared BUSY starts only after the command was accepted by the PMU.
  Additionally it is recommended to place a “DSYNC” instruction between a command sequence and read accesses to depending data including affected registers.
- The caches (data cache in DMI “DCache” and instruction cache in PMI “ICACHE”) as well as the data line buffer in the DMI “DLB” are not automatically invalidated nor updated after changing Flash content by erasing or programming. It is therefore recommended to either invalidate them actively or read the Flash content via the non-cached address range. Otherwise old data might be delivered from these buffers.
  The DMI cache and line buffer can be invalidated by writing OVC_OCON.DCINVAL to ‘1’. The ICACHE can be invalidated by writing PCON1.PCINV to ‘1’. All buffers are invalidated by a reset.
- The PMU and Flash work with the SRI and FSI clocks. When changing the divider values of these clocks in SCU_CCUCON0 the following rules apply:
  – The only allowed PMU/Flash “operation” when switching is reading from Flash memory. Programming or erasing the Flash is forbidden.
  – It must be ensured that before, during and after the divider change the configured number of Flash wait-cycles is sufficient for the selected clock frequency. Remember that the wait-cycles are counted with f_{FSI}.

Sequence for Programming

The following sequence is the most defensive one for programming a page. It is however acceptable to skip some checks because the programmed data should be verified anyhow afterwards:

- “Clear Status” to clear flags.
- “Enter Page Mode”.
- DSYNC.
- Wait until FSR.xFPAGE = ‘1’ or fail if FSR.SQER = ‘1’ or FSR.PROER = ‘1’.

- Repeat “Load Page” until the page is filled.
- “Write Page”.
- DSYNC.
- Wait until FSR.PROG = ‘1’ or fail if FSR.SQER = ‘1’ or FSR.PROER = ‘1’.
- Wait until FSR.xBUSY = ‘0’ or enable the interrupt.
  – While FSR.xBUSY is ‘1’ the flags FSR.xFOPER can be checked for ‘1’ as abort criterion to protect against hardware failures causing BUSY to stay ‘1’.
- Check for FSR.VER flag (see handling advice in **Chapter 5.7.7.1**).
- Fail if FSR.xFOPER = ‘1’.
- Check programmed content, evaluate FSR.xDBER and possibly count single-bit errors.
- Clear error flags and FSR.PROG either with “Clear Status” or by directly writing to FSR.

Sequence for Erasing

The following sequence is the most defensive one for erasing a sector. It is however acceptable to skip some checks because the programmed data should be verified anyhow after programming:

- “Clear Status” to clear flags.
- “Erase Sector”.
- DSYNC.
- Wait until FSR.ERASE = ‘1’ or fail if FSR.SQER = ‘1’ or FSR.PROER = ‘1’.
- Wait until FSR.xBUSY = ‘0’ or enable the interrupt.
  – While FSR.xBUSY is ‘1’ the flags FSR.xFOPER can be checked for ‘1’ as abort criterion to protect against hardware failures causing BUSY to stay ‘1’.
- Check for FSR.VER flag (see handling advice in **Chapter 5.7.7.1**).
- Fail if FSR.xFOPER = ‘1’.
- Clear error flags and FSR.ERASE either with “Clear Status” or by directly writing to FSR.

Concurrent Use of D0Flash and D1Flash

The DFlash supports concurrent operations, notably programming in one bank and erasing in the second bank (see **Chapter 5.5.4.4**). This feature was already available in previous product generations Audo-NG and Audo-F. In these product generations the Flash driver faced some challenges because error flags were not separated for each bank and flags could not be easily cleared while an operation was ongoing. With this product generation flag handling for concurrent operations was significantly enhanced.

The following depicts the flow for a programming routine on D0Flash which can be executed while an erase is already ongoing in D1Flash:

- “Enter Page Mode”
- DSYNC.

- Wait until FSR.DFPAGE = ‘1’ or fail if FSR.SQER = ‘1’ or FSR.PROER = ‘1’ (development time check).
- Repeat “Load Page” until the page is filled.
- “Write Page”.
- DSYNC.
- Wait until FSR.PROG = ‘1’ or fail if FSR.SQER = ‘1’ or FSR.PROER = ‘1’ (development time check).
- Wait until FSR.D0BUSY = ‘0’ or enable the interrupt.
  – While FSR.D0BUSY is ‘1’ the flags FSR.DFOPER can be checked for ‘1’ as abort criterion to protect against hardware failures causing BUSY to stay ‘1’.
- Check for XFSR.D0VER (see handling advice in **Chapter 5.7.7.1**). Clear flag by writing XFSR.D0VER = ‘1’.
- Fail if FSR.DFOPER = ‘1’ (could have been caused by programming or erasing).
- Check programmed content and evaluate FSR.DFMBER. Clear flag by writing FSR.DFMBER = ‘1’.
- Clear FSR.PROG by directly writing to FSR.

ENDINIT Register Protection

As described in **Chapter 5.6** many registers are write protected. The write protection “E” is changed by an SPB write access. The user should be aware that this SPB write access changing the protection and preceding or following SRI accesses to registers affected by this protection can incur different system delays. Thus they may not become effective in program order. As remedy it is recommended to read back the protection register (WDT_CON0) before performing the depending SRI accesses.

5.7.3 EEPROM Emulation With DFlash

The term “EEPROM emulation” designates an algorithm with the following features:

- It increases the effective endurance by spreading the EEPROM write accesses over a larger range of Flash memory.
- It ensures that all Flash cells incur a similar number of cycles independent of the update frequency of the EEPROM data (“wear levelling”).
- It manages the allocation of EEPROM data to Flash ranges so that stale data can be erased.

As the DFlash of the TC1798 contains 2 sectors (one in each bank) and only complete sectors can be erased all EEPROM emulation algorithms follow the same general idea:

- The EEPROM writes are performed in one sector, the “active” one. The other sector stays erased.
- The data is stored so that several writes of the same EEPROM address can be performed in one DFlash sector. The position of the latest data version and the original EEPROM address can be determined from the address in Flash and

additional administrative data (e.g. all data is pushed to a stack and the pushed data contains the EEPROM address).
- At a certain sector fill level a sector switch is performed. This moves all active data to the erased sector. After that the active sector is erased and the other sector becomes the active one.

One specific requirement for an EEPROM emulation algorithm is the resistance against aborts during its operation. In any case the algorithm must be able after device startup to recover without data loss, determine the active sector and resume operation.

In many applications even resistance against aborted Flash processes (program, erase) is needed. See details in **Chapter 5.7.8.2**.

5.7.3.1 Robust EEPROM Emulation

A key requirement for an EEPROM emulation algorithm is the reliability of the stored data. The DFlash with its DEC-TED ECC algorithm protects perfectly against bit or bit-line oriented failures. However word-line oriented failures need to be handled by the EEPROM emulation algorithm.

The following hints shall be followed to achieve highest possible robustness:

- Before programming a page save the content of the other page on the same word-line in SRAM.
- Program the new page and compare the content of this page and of the saved page with their reference data. This can be done with normal read margins. Ignore correctable errors and the VER flag.
- If the data comparison fails program this page and the saved content of the other page to a different word-line.
- This procedure can be repeated if the data comparison fails again. The number of repetitions should be limited (e.g. to 3) in case the programming fails because of out-of-spec operating conditions.
- Word-line oriented fails can also have the effect that the affected word-lines can not be erased anymore (other word-lines stay fully functional). A robust EEPROM emulation is immune against such word-lines (e.g. by identifying old data by version counters).

For the TC1798 this robust EEPROM algorithm is required for the usage of the DFlash.

Due to the specificity of each application the appropriate usage and implementation of these measures (together with the more elaborate VER handling) must be chosen according to the context of the application.

5.7.4 Performance Considerations

This section contains advice for optimizing the performance of Flash accesses.

DFlash Performance

The features of the DFlash were optimized for the requirements of an EEPROM emulation. As side effect the access time is significantly higher as in the PFlash. Additionally it can't be read with burst accesses. Therefore it is not recommended to use the DFlash directly memory mapped in the application. In its typical use scenario the active EEPROM data is retrieved from the DFlash once during application startup and is copied to SRAM from where it is used by the application. Further read accesses are only done by the emulation driver when performing updates.

Read Buffers

As described in **Chapter 5.5.3** the PMU contains a set of configurable read buffers. Each of them is assigned to one bus master. It is filled by pre-fetching an incremental following address. For optimum performance a read buffer should be assigned to each master with a high number of PFlash reads.

After reset one read buffer is assigned to the SHE module for optimum performance of the secure boot. When the SHE module is not needed or after finishing the secure boot it is advisable to change this buffer tag depending on application needs (e.g. DMA).

As the pre-fetching is done with increasing addresses reading PFlash ranges with decreasing addresses (e.g. reading an array from a high index to low indices) doesn't benefit from the read buffers.

5.7.5 Handling Flash Protection

Failing to use the Flash protection correctly can on one hand lock the device forever, even damage it or on the other hand leave the protection ineffective.

Effective Use of Flash Protection

For an effective IP protection the Flash read protection must be activated. As described in **Chapter 5.5.5.4** this ensures system wide that the Flash cannot be read from external or changed without authorization.

With the default setting of PROCON0.DFEXPRO (= '0') an active Flash read protection causes a global write protection of PFlash and DFlash in this PMU. Thus for programming the DFlash at application run-time the read protection would have to be disabled with the correct password. This means the password needs to be installed in the Flash.

By programming DFEXPRO to '1' the DFlash is excluded from the global write protection. Now the application can program the DFlash without disabling the read protection and the password doesn't need to be known to the application.

Attention: Full Flash analysis of an FAR device is only possible when the customer has removed all installed protections or delivers the necessary passwords with the device.

As the removal of an OTP protection in UCB2 is not possible the OTP protection inevitably limits analysis capabilities.

Changing UCBs

The protection installation is modified by erasing and programming the UCBs (see **Chapter 5.5.5.3**). These operations need to be performed with care as described in the following.

Aborting an “Erase UC Block” operation (e.g. due to reset or power failure) must be avoided at all means. As an UCB is a logical sector of the configuration sector an aborted erase can affect readability of the complete configuration sector content. With an unreadable configuration sector the device is unusable. An automatic repair (as for the logical sectors, see **Chapter 5.7.8.3**) is not implemented.

For the same reason the allowed number of program/erase cycles of the UCBs must not be exceeded. Over-cycling the UCBs can disturb data in the configuration sector which finally leads to an unusable device.

The installation of the protection and its confirmation on different pages of the UCB offers the possibility to check the installation before programming the confirmation. First the protection needs to be programmed, then an application reset must be triggered to trigger the reading of the UCBs by the PMU and after that the protection can be verified (e.g. “Disable … Protection” to check the password and by checking PROCONs, SHEBOOTs and FCON). The application reset is inevitable because the PMU reads the UCBs only during the startup phase.

5.7.6 Cooperation with SHE

As described in **Chapter 5.5.4.4** the SHE module stores its keys in the KeyFlash. As this KeyFlash has common resources with the PFlash and DFlash the SHE module blocks the DFlash (completely) and the PFlash (only program/erase) by setting its semaphore bit SHE_SEMA.SHE when it accesses the KeyFlash.

Therefore in all applications supporting SHE functionality the Flash drivers should cooperate with the SHE module by setting an other SHE_SEMA bit before doing a program/erase access to PFlash or DFlash and before reading the DFlash. After finishing their access they have to release the semaphore bit again to enable the SHE module access to its KeyFlash.

When Flash drivers don’t set the semaphore bit it might happen that their command sequences are disturbed due to an interception by the SHE module.

When Flash driver don’t release their semaphore bit in time they can prevent the SHE module from performing key updates.

Please note that the SHE subroutines SHE::LOAD_KEY and SHE::DEBUG_AUTHORIZATION call “Clear Status” before programming the keys, effectively clearing FSR. But SHE never calls “Clear Status” when finishing a subroutine

(either reading keys or programming keys). Thus errors reported by a SHE subroutine can be analyzed by reading FSR.

5.7.7 Handling Errors

The earlier sections described shortly the functionality of “error indicating” bits in the flash status registers **FSR** and **XFSR**. This section elaborates on this with more in-depth explanation of the error conditions and recommendations how these should be handled by customer software.

5.7.7.1 Handling Errors During Operation

This first part handles error conditions occurring during operation (i.e. after issuing command sequences) and the second part (**Section 5.7.7.2**) error conditions detected during startup.

SQER “Sequence Error”

Fault conditions:

- Improper command cycle address or data, i.e. incorrect command sequence.
- Write access to busy Flash bank.
- New “Enter Page” in Page Mode.
- “Load Page” and not in Page Mode.
- “Load Page” results in buffer overflow.
- “Load Page” with mixed 32/64 transfers.
- First “Load Page” addresses 2. word.
- “Write Page” with buffer underflow.
- “Write Page” and not in Page Mode.
- “Write Page” to unavailable Flash range.
- Command sequence with address not pointing to a legal start address (e.g. page, UCB or sector).
- Byte transfer to password or data.
- “Erase Sector” command to DFlash.
- Erase UCB with wrong UCBA.

New state:

Read mode is entered with following exceptions:

- “Enter Page” in Page Mode re-enters Page Mode.
- “Write Page” with buffer underflow is executed.
- After “Load Page” causing a buffer overflow the Page Mode is not left, a following “Write Page” is executed.

Proposed handling by software:

Usually this bit is only set due to a bug in the software. Therefore in development code the responsible error tracer should be notified. In production code this error will not occur. It is however possible to clear this flag with “Clear Status” or “Reset to Read” and simply issue the corrected command sequence again.

PFOPER/DFOPER “Operation Error”

Fault conditions:

ECC double-bit error detected in Flash microcode SRAM during a program or erase operation in PFlash or DFlash. This can be a transient event due to alpha-particles or illegal operating conditions or it is a permanent error due to a hardware defect. This situation will practically not occur.

Attention: these bits can also be set during startup (see **Chapter 5.7.7.2**).

New state:

The Flash operation is aborted, the BUSY flag is cleared and read mode is entered. It is however possible that an ECC failure in the Flash SRAM prevents the BUSY flag from being cleared.

Proposed handling by software:

The flag should be cleared with “Clear Status”. The last operation can be determined from the PROG and ERASE flags[1)]. In case of an erase operation the affected physical sector must be assumed to be in an invalid state, in case of a program operation only the affected page. Other physical sectors can still be read. New program or erase commands must not be issued before the next reset.

Consequently a reset must be performed (please note that an application reset is sufficient but it does not automatically clear the PFOPER/DFOPER flags). This performs a new Flash startup with initialization of the microcode SRAM. The application must determine from the context which operation failed and react accordingly. Mostly erasing the addressed sector and re-programming its data is most appropriate. If a “Program Page” command was affected and the sector can not be erased (e.g. in Flash EEPROM emulation) the word-line could be invalidated if needed by marking it with all-one data and the data could be programmed to another empty word-line.

Only in case of a defective microcode SRAM the next program or erase operation will incur again this error.

As protection against an endless BUSY a Flash driver can check for PFOPER/DFOPER during Flash operation.

1) Only when both DFlash banks were busy, one with program and the other with erase the affected bank and operation can not be determined.

Note: Although this error indicates a failed operation it is possible to ignore it and rely on a data verification step to determine if the Flash memory has correct data. Before re-programming the Flash the flow must ensure that a new reset is applied.

*Note: Even when the flag is ignored it is recommended to clear it. Otherwise all following operations — including "sleep" — could trigger an interrupt even when they are successful (see **Chapter 5.5.7**, interrupt because of operational error).*

PROER "Protection Error"

Fault conditions:

- Password failure.
- Erase/Write to protected sector.
- Erase UCB and protection active.
- Write UC-Page to protected UCB.

Attention: a protection violation can even occur when a protection was not explicitly installed by the user. This is the case when the Flash startup detects an error and starts the user software with read-only Flash (see **Chapter 5.7.7.2**). Trying to change the Flash memory will then cause a PROER.

New state:

Read mode is entered. The protection violating command is not executed.

Proposed handling by software:

Usually this bit is only set during runtime due to a bug in the software. In case of a password failure a reset must be performed in the other cases the flag can be cleared with "Clear Status" or "Reset to Read". After that the corrected sequence can be executed.

VER "Verification Error"

Fault conditions:

This flag is a warning indication and not an error. It is set when a program or erase operation was completed but with a suboptimal result. This bit is already set when only a single bit is left over-erased or weakly programmed which would be corrected by the ECC anyhow.

However excessive VER occurrence can be caused by operating the Flash out of the specified limits, e.g. incorrect voltage or temperature. A VER after programming can also be caused by programming a page whose sector was not erased correctly (e.g. aborted erase due to power failure).

Under correct operating conditions a VER after programming will practically not occur. A VER after erasing is not unusual.

Attention: this bit can also be set during startup (see **Chapter 5.7.7.2**).

New state:

No state change. Just the bit is set.

Proposed handling by software:

This bit can be ignored. It should be cleared with “Clear Status” or “Reset to Read”. In-spec operation of the Flash memory must be ensured.

If the application allows (timing and data logistics), a more elaborate procedure can be used to get rid of the VER situation:

- VER after program: erase the sector and program the data again. This is only recommended when there are more than 3 program VERs in the same sector. When programming the DFlash in field (EEPROM emulation) ignoring program VER is normally the best solution because its most likely cause are violated operating conditions. Take care that never a sector is programmed in which the erase was aborted. In the EEPROM emulation the algorithm must ensure this e.g. by programming a marker after finishing successfully the erase.
- VER after erase: the erase operation can be repeated until VER disappears. Repeating the erase more than 3 times consecutively for the same sector is not recommended. After that it is better to ignore the VER, program the data and check its readability. Again for EEPROM emulation its most likely cause are violated operating conditions. Therefore it is recommended to repeat the erase at most once or ignore it altogether.

For optimizing the quality of Flash programming see the following section about handling single-bit ECC errors.

*Note: Even when this flag is ignored it is recommended to clear it. Otherwise all following operations — including “sleep” — could trigger an interrupt even when they are successful (see **Chapter 5.5.7**, interrupt because of verify error).*

PFSBER/DFSBER “Single-Bit Error”

Fault conditions:

When reading data or fetching code from PFlash or DFlash the ECC evaluation detected a single-bit error (“SBE”) which was corrected.

This flag is a warning indication and not an error. A certain amount of single-bit errors must be expected because of known physical effects.

New state:

No state change. Just the bit is set.

Proposed handling by software:

This flag can be used to analyze the state of the Flash memory. During normal operation it should be ignored. In order to count single-bit errors it must be cleared by “Clear Status” or “Reset to Read” after each occurrence[1)].

Usually it is sufficient after programming data to compare the programmed data with its reference values ignoring the SBE bits. When there is a comparison error the sector is erased and programmed again.

When programming the PFlash (end-of-line programming or SW updates) customers can further reduce the probability of future read errors by performing the following check after programming:

- Change the read margin to “high margin 0”.
- Verify the data and count the number of SBEs.
- When the number of SBEs exceeds a certain limit (e.g. 10 in 2 MByte) the affected sectors could be erased and programmed again.
- Repeat the check for “high margin 1”.
- Each sector should be reprogrammed at most once, afterwards SBEs can be ignored.

In case of EEPROM emulation using DFlash the verification of programmed data should be done with the normal read level and SBEs should be ignored. Further advice can be found in **Chapter 5.7.3**.

5.7.7.2 Handling Errors During Startup

The FSR flags are not only used to inform about the success of Flash command sequences but they are also used to inform (1) the startup software and (2) the user software about special situations incurred during startup. In order to react on this information these flags must be evaluated after reset before performing any flag clearing sequence as “Clear Status” or “Reset to Read”.

The following two levels of situations are separated:

- Fatal level: the user software is not started. A WDT reset is performed.
- Error level: the user software is started but the Flash memory must not be programmed or erased.
- Warning level: the user software is started but a warning is issued.

Fatal Level (WDT Reset)

These error conditions are evaluated by the startup software which decides that the Flash is not operable and thus waits for a WDT reset. The application sees only a longer startup time followed by a WDT reset.

The reason for a failed Flash startup can be a hardware error or damaged configuration data.

1) Further advice: the ECC error flags of the PFlash in **FSR** and **XFSR** represent the errors found in an aligned block of 256 bits independent of the read data width of the CPU. This is also independent of the addressed range (cached or non-cached). Thus errors can’t be counted exactly.

Error Level (Flash Read-Only)

In this condition the user software is started but the Flash memory must not be programmed or erased. If writability of the Flash is mandatory the user software itself has to perform a reset.

Flash microcode error:

FSR bits set: PFOPER and DFOPER.

The user software is started normally but the Flash must not be programmed or erased. Please note that programming or erasing is not blocked by hardware. Issuing program or erase sequences despite this condition is forbidden.

Warning Level

These conditions inform the user software about an internally corrected or past error condition.

Logical sector corrected:

FSR bits set: VER.

The Flash detected that a logical sector erase was apparently aborted by reset or power failure. In order to maintain readability of the other logical sectors the Flash tried to repair this state. The aborted erase operation must be repeated. See also **“Recovery From Aborted Logical Sector Erase (“ALSE”)” on Page 5-78**.

Leftover OPER:

FSR bits set: PFOPER or/and DFOPER.

The OPER flags are only cleared by the command sequence “Clear Status” or with a power-on reset. After any other reset a OPER flag can still be set when the user software is started.

Single-bit error in protection:

FSR bits set: PFSBER.

An corrected ECC single-bit error was detected during installation of the protection.

5.7.8 Resets During Flash Operation

A reset or power failure during an ongoing Flash operation (i.e. program or erase) must be considered as violation of stable operating conditions. However the Flash was designed to prevent damage to non-addressed Flash ranges when the reset is applied as defined in the data sheet. The exceptions are erasing logical sectors and UCBs. Aborting an erase process of a logical sector can leave the complete physical sector unreadable. An automatic recovery mechanism is implemented (see **Chapter 5.7.8.3**). When an UCB erase is aborted the complete Flash can become unusable. There is no recovery implemented because UCBs are usually only erased in a controlled environment. The addressed Flash range is left in an undefined state.

5.7.8.1 General Advice

When an erase operation is aborted the addressed logical or physical sector can contain any data. It can even be in a state that doesn't allow this range to be programmed.

When a page programming operation is aborted the page can still appear as erased (but contain slightly programmed bits), it can appear as being correctly programmed (but the data has a lowered retention) or the page contains garbage data. It is also possible that the read data is instable so that depending on the operating conditions different data is read.

For the detection of an aborted Flash process the flags FSR.PROG and FSR.ERASE could be used as indicator but only when the reset was an application reset. Power-on resets can not be determined from any flags. It is not possible to detect an aborted operation simply by reading the Flash range. Even the margin reads don't offer a reliable indication.

When erasing or programming the PFlash usually an external instance can notice the reset and simply restart the operation by erasing the Flash range and programming it again.

5.7.8.2 Advice for EEPROM Emulation

However for the case of EEPROM emulation in the DFlash this external instance is not existing. A common solution is detecting an abort by performing two operations in sequence and determine after reset from the correctness of the second the completeness of the first operation.

E.g. after erasing a DFlash sector a page is programmed. After reset the existence of this page proves that the erase process was performed completely.

The detection of aborted programming processes can be handled similarly. After programming a block of data an additional page is programmed as marker. When after reset the block of data is readable and the marker is existent it is ensured that the block of data was programmed without interruption.

Because often very small amounts of data need to be programmed in EEPROM emulation not always a complete page can be spent as marker. The following recipe allows to reduce the marker size to 8 bytes. This recipe violates the rule that a page may be programmed only once. This violation is only allowed for this purpose (EEPROM emulation with DFlash) and only when the algorithm is robust against disturbed pages (see **Chapter 5.7.3**) by repeating a programming step when it detects a failure.

Robust programming of a page of data with an 8 byte marker:

1. After reset program preferably always first to an even page ("Target Page").
2. If the Other Page on the same word-line contains active data save it to SRAM (the page can become disturbed because of the 4 programming operations per word-line).

3. Program the data to the Target Page (marker bytes of step 5 left as ‘0’).
4. Perform strict check of the Target Page and Other Page (see below).
5. Program 8 byte marker to Target Page (data bytes of step 3 left as ‘0’).
6. Perform strict check of the Target Page and Other Page.
7. In case of any error of the strict check go to the next word-line and program the saved data and the target data again following the same steps.
8. Ensure that the algorithm doesn’t repeat unlimited in case of a violation of operating conditions.

Strict checking of programmed data:

1. Ignore correctable errors and the VER flag.
2. Switch to tight margin 0.
3. If the data (check the complete page) is not equal to the expected data report an error.
4. If an uncorrectable error is detected report an error.

After reset the algorithm has to check the last programmed page if it was programmed completely:

1. Read with normal read level. Ignore single-bit errors.
2. Read 8-byte marker and check for double-bit error.
3. Read data part and verify its consistency (e.g. by evaluating a CRC). Check for double-bit error.
4. If the data part is defective don’t use it (e.g. by invalidating the page).
5. If the data part is ok:
   a) If the marker is erased the data part could have been programmed incompletely. Therefore the data part should not be used or alternatively it could be programmed again to a following page.
   b) If the marker contains incorrect data the data part was most likely programmed correctly but the marker was programmed incompletely. The page could be used as is or alternatively the data could be programmed again to a following page.
   c) If the marker is ok the data part was programmed completely and has the full retention. However this is not ensured for the marker part itself. Therefore the algorithm must be robust against the case that the marker becomes unreadable later.

In very specific cases it is allowed to repair data left from an aborted programming operation: if the algorithm can detect that an abort occurred and the algorithm knows which data must be present in the page it is possible to simply redo the programming by programming the same data again. However the previous methods which “jump” over incorrect data are preferred.

5.7.8.3 Recovery From Aborted Logical Sector Erase (“ALSE”)

When while erasing one of the logical sectors in PFlash a power failure occurs or a reset is triggered the aborted erase process might leave the complete physical sector

unreadable. As often the logical sectors contain important boot code the application might not start anymore. Thus the recommended step to repeat the aborted erase after startup can not be realized.

The FSI implements two recovery algorithms. The selection between the two is done with the SPREC bit (“Soft-Programming Recovery”), i.e. bit 0 of byte 2 in the UCB1 (see **“Configuring Flash Protection in the UCB” on Page 5-21**).

In both cases the algorithm checks first the sectors PS0 and PS4 for an over-erased state. When this is detected the bit FSR.VER is set to inform the application (see **Chapter 5.7.7.2**). After that the algorithm tries to repair this state:

- The default algorithm is selected with SPREC = 0. The over-erased logical sector is searched. When finding one this algorithm programs it shortly with all-one data. The other logical sectors become readable again.
  At least theoretically (especially when operating the device outside of the allowed operating conditions) this algorithm could destroy valid data: when an over-erased logical sector is reported incorrectly during normal startup without a preceding sector erase the data of a logical sector would be overwritten with all-one.
- An alternative algorithm is selected when SPREC = 1. This algorithm searches also for the over-erased logical sector as before. For repair a smarter but more time consuming algorithm is performed. The affected logical sector is not overwritten with all-one but only the over-erased 0-bits are slightly programmed so that they become normal 0-bits again. Under all circumstances this algorithm can not destroy any data but when a lot of data has to be repaired the flash startup time can be increased to t_{FL_SPREC}.

In case this feature is not needed (e.g. because the Alternate Boot Mode “ABM” is used) the execution of the recovery algorithm can be disabled for selected logical sectors with the field “ALSEDIS” of **PROCON1**.

Note: If not disabled the ALSE recovery algorithm is triggered by every reset. However in case of an application reset at high clock frequencies the algorithm “SPREC=1” might not finish before the watchdog is triggered. This can cause a device hang-up. A power-on reset (which switches to a slower clock during startup) lets the repair algorithm finish and the device boot successfully again.

Attention: The ALSE repair algorithm was designed to recover the device after a reset during erase in PFlash caused by an accidental loss of power. Any other possible cause of resets must be prevented by the customer.

5.7.9 ECC

For special applications the ECC features need to be considered.

Using Address ECC

The address ECC is a vital part of the safe fetch path needed for safety applications. The difference between standard ECC and address (“safety”) ECC is explained in Chapter 5.5.6.1.

The calculation of the safety ECC is done over data bits and the address bits 23:3. As side effect erased PFlash ranges or PFlash ranges programmed with the standard ECC will be read with ECC errors.

Thus the installation of an application using the safety ECC should be done as follows:

- By default the devices starts with the standard ECC enabled.
- The Flash loader can enabled the safety ECC by setting FCON.ADDECC.
- From this point on the data is programmed with the safety ECC to the PFlash. Erased ranges can not be verified anymore.
- A sector should be programmed completely to ensure that it can be read without ECC errors.
- In order to configure the safety ECC as standard for the next startup the UCB0 shall be programmed so that PROCON0.ADDECC is set to ‘1’.

Attention: Changing FCON.ADDECC while accessing the Flash (reading, programming, erasing) is forbidden and can cause unpredictable behavior.

Creating Incorrect ECC

In safety applications error detection features are usually verified at each startup. In order to verify the detection logic for ECC double-bit errors an address in PFlash needs to be programmed with such an error.

This can be done by programming a page twice. The data and the calculated ECC bits of both programming steps are effectively or-ed in the Flash because only the 1-bits are programmed. With the knowledge of the ECC calculation the data of the first and second programming step can be chosen to create a page containing a double-bit error. Programming a page twice is allowed if the other page of this word-line is not programmed because then the word-line is programmed only two times.

In the TC1798 the customer can disable automatic ECC generation with ECCW.PECENCDIS. With this feature and with the knowledge of the ECC calculation a page with a double-bit ECC error can be programmed with just one programming step.

Ready-to-use programming routines for the creation of double-bit errors are part of the IFX safety software “SafeTcore”.

6 Local Memory Unit (LMU)

The Local Memory Unit is an SRI peripheral providing access to volatile memory resources. It's primary purpose is to provide 128 kbytes of local memory for general purpose usage but it will also provide access to the separate block of emulation and debug memory (EMEM) provided in the Emulation Devices.

6.1 Feature List

An overview of the features implemented in the LMU follows:

- 128 kbytes of SRAM
  - organised as 64 bit words
  - support for byte, half word and word accesses as well as double-word and burst accesses
- Interface to the EMEM of the ED device.
- OLDA region support.

6.2 Local Memory

The local memory can be used for code execution, data storage or overlay memory. The address range of the memory is 90000000_H to $9001FFFF_H$. As well as being accessed via cached (segment 9_H), the memory can be accessed via non-cached (segment B_H) memory addresses.

The memory implements memory integrity checking for error detection and correction. This means that the memory must be initialised before reads are attempted with the integrity checking enabled to avoid generating spurious data corruption errors. Initialising before enabling the memory integrity logic allows the local memory to support initialisation using word (32 bit) or smaller writes as well as 64 bit writes. The memory integrity checking is enabled using the **LMU_MEMCON.DED_EN** bitfield. After a class 3 reset, this is disabled (0_B).

If memory integrity checking is enabled, a read access which fails the integrity check will be terminated with an SRI error condition. This behaviour can be changed by setting the **LMU_MEMCON.ERRDIS** bit to 1_B. If the bit is set then an SRI error will not occur.

An ECC error will also be reportedto the SCU. The SCU will use this signal for error indication and triggering of an NMI trap (if enabled). Errors will also be flagged using the status bit **DBERR** in the **LMU_MEMCON** register. These bits are set when an error condition occurs and can be cleared by a valid write of 0_B to the bit location. This behaviour is not altered by the setting of **LMU_MEMCON.ERRDIS**.

Note that if multiple accesses are occurring to the LMU, it is possible that a write access to clear the error status will be pipelined behind another access which triggers a new error. In this case, the error will be flagged to the SCU but not reported in the **LMU_MEMCON** register.

If the **LMU_MEMCON.DED_EN** bitfield is set to 0_B after an error has occurred but before and **DBERR** flags has been cleared, then the error flag will remain set to allow software to determine the source of the ECC error.

Local memory performance will be the same as, or better than, the performance of the embedded flash. This applies to both the initial latency of the first word returned and also the incremental latency for each word in the same cache line fetched.

If the CPU access can't be handled by the local memory (e.g. an unsupported SRI opcode has been received), an SRI bus error is reported by the LMU. This will cause a DSE trap.

Some bitfields of the **LMU_MEMCON** register are protected by **LMU_MEMCON.PMIC** bit. If the data written to the register has the bitfield set to 0_B, no change will be made to bit 23_D to 9_D of the register regardless of the data written to these fields.

6.3 Emulation Memory (EMEM)

In the Emulation Device , an Emulation Memory (EMEM) of 768 kbytes is provided, which can be used for either calibration via overlay of non-volatile memory or OLDA (see **Chapter 6.4** below). The address range of the memory is $9F000000_H$ to $9F0BFFFF_H$ (which is identical for all EMEM sizes in the derivatives). As well as the cached addresses (segment 9_H), noncached address (segment B_H) accesses can be used for EMEM accesses via the LMU.

The Emulation Memory interface is a 64-bit wide memory interface that controls the CPU-accesses to the Emulation Memory in the Emulation Device. All widths of write accesses are supported (byte, halfword, word, double-word).

CPU-controlled Load-Modify-Store accesses (with LDMST instruction) are supported as separate read and write instructions not as an atomic operation.

In the production device, the EMEM interface is always disabled. A CPU read access from the Emulation Memory region causes a DSE trap by returning an SRI bus error. If the Emulation Memory region read access is initiated by a SPB master (e.g. PCP), additionally a SPB error interrupt can be generated.

By default, write accesses to the Emulation Memory by any master cause an SRI bus error trap in the production device.

In the Emulation Device, a SRI bus error is returned by the LMU if a read access can't be handled by the EMEM, for example, when the CPU accesses a trace memory tile in EMEM. In this case, the EMEM access is aborted by the LMU.

Write accesses which cannot be handled by the EMEM will fail silently as the write access is completed on the SRI bus before being passed to the EMEM. Therefore any error condition encountered by the EMEM will occur after the SRI access has completed.

The LMU contains a read buffer which is used during EMEM accesses. The contents of the buffer will be used if a subsequent read access overlaps the address range of the

data stored in the buffer. Coherency with the EMEM contents is not maintained. If the address stored in the read buffer has been modified in EMEM by another master on the backbone bus, then invalid data will be returned from the read buffer if the address is then read again via the LMU.

6.4 Online Data Acquisition (OLDA) and its Overlay

Calibration is additionally supported by an OLDA memory range of up to 32 Kbyte, which is a virtual memory and physically only available, if it is redirected (by the overlay feature of the processor) to internal or external physical memory or to the EMEM in the Emulation Device.

If OLDA support is enabled in the LMU, direct write accesses (without redirection) to the OLDA range are not really executed, and they do not generate a bus error trap[1)]. If OLDA support is not enabled, write accesses will generate a bus error trap. OLDA support is enabled by setting LMU_MEMCON.OLDAEN to 1_B.

Read accesses to the OLDA range generate a bus error trap, if not redirected to a physically available overlay block. Successful accesses to the OLDA memory range will only take place when the accesses are redirected to real, physical memory.

The base address of the virtual OLDA memory range is A/8FE7 0000_H, the end address is A/8FE7 $7FFF_H$. Accesses to the OLDA range are also supported in cached address space.

Note: In OTARx registers, any target address can be selected for redirection, thus also addresses in the OLDA range. However, the handling of direct accesses to the OLDA range is completely controlled in the LMU.

6.5 Clock Control

The LMU contains a clock control register, **LMU_CLC**, which allows the LMU to be put into a power saving mode.

If LMU_CLC.DISR is set then the LMU will be disabled and all accesses will be errored unless they are addressed to a register.

1) Write accesses to a cached memory address will trigger a read to fill the cache line before the data is written to the cache. This read will trigger a bus error.

6.6 LMU Registers

The LMU registers are mapped into a 256 byte address space which allows for 64 registers. Accesses to unused register space will cause an SRI bus error.

Table 6-1 Registers Address Space

Module	Base Address	End Address	Note
LMU	F870 0800$_H$	F870 08FF$_H$	All registers are endinit protected and are accessible in Supervisor mode only

Table 6-2 Registers Overview

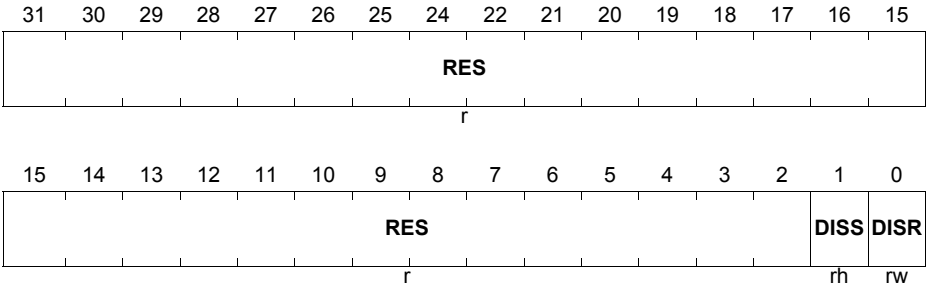
Short Name	Description	Offset Addr.[1]	Access Mode		Reset Class	Page Number
			Read	Write		
LMU_CLC	LMU Clock Control	0$_H$	SV,BE,32	SV,E,BE,32	3	6-5
LMU_MEMCON	LMU Memory Control	4$_H$	SV,BE,32	SV,E,BE,32	3	6-6
LMU_MODID	LMU Module ID	8$_H$	SV, BE,32	R,BE	3	6-9

1) The absolute register address is calculated as follows:
Module Base Address (Table 6-1) + Offset Address (shown in this column)

LMU Clock Control Register

LMU_CLC

LMU Clock Control Register **(000_H)** **Reset Value: 0000 0000_H**

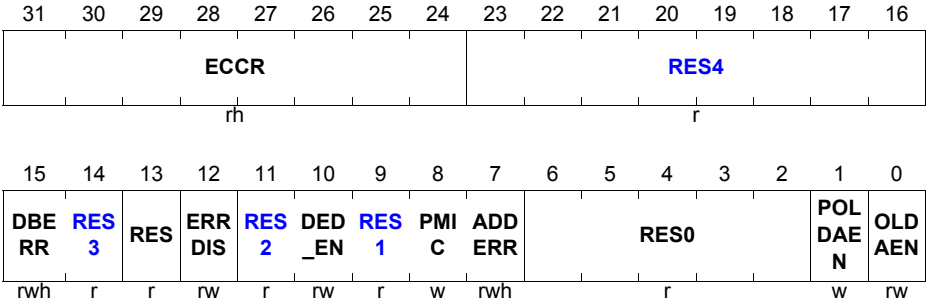


Field	Bits	Type	Description
DISR	0	rw	**LMU Disable Request Bit** This bit is used for enable/disable control of the LMU. 0_B LMU disable is not requested 1_B LMU disable is requested
DISS	1	rh	**LMU Disable Status Bit** Current state of LMU. 0_B LMU is enabled (default after reset) 1_B LMU is disabled
RES	31:2	r	**Reserved**

LMU Memory Control Register

Provides Control of the memory integrity error checking, error signalling to the SCU and error injection for ECC logic test. Also control of the OLDA function. The register is cleared by a Class 3 reset.

LMU_MEMCON
LMU Memory Control Register (004$_H$) Reset Value: 0000 0800$_H$



Field	Bits	Type	Description
OLDAEN	0	rw	**Online Data Acquisition Enabled** This bit is used to control trap generation for write accesses to the OLDA address range. 0_B Trap generation on write access to OLDA memory range is enabled 1_B No trap generated on write access to OLDA memory range.
POLDAEN	1	w	**Protection Bit for OLDAEN** 0_B Bit Protection: Bit OLDAEN remains unchanged after LMU_MEMCON write. 1_B OLDAEN can be changed by current write to LMU_MEMCON
RES0	6:2	r	**Reserved** Read and write 0_B

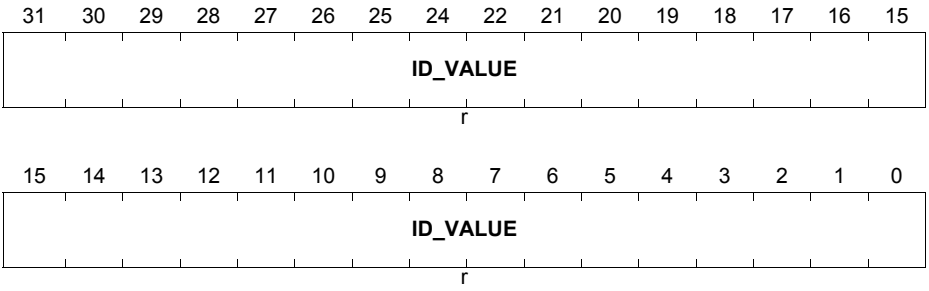
Field	Bits	Type	Description
ADDERR	7	rwh	**SRI Address Phase ECC Error** Flag set by hardware when the SRI interface detects an ECC error on an incoming transaction. This bit is cleared by writing 0_B but cannot be set by software. 0_B No error has occurred 1_B An ECC error has been observed on an SRI transaction addressed to the LMU
PMIC	8	w	**Protection Bit for Memory Integrity Control Bits** Will always return 0_B when read 0_B Bit Protection: Bits 23 to 9 remain unchanged after LMU_MEMCON write. 1_B Bits 23 to 9 will be updated by the current write to LMU_MEMCON
RES1	9	r	**Reserved** read as 0_B. Must be written as 0_B
DED_EN	10	rw	**Memory Integrity Dual Error Detection Enable** 0_B ECC errors in local memory read data do not cause an error indication (interrupt, bus trap, error bits). 1_B ECC errors are enabled. Memory errors are flagged to the SCU.
RES2	11	r	**Reserved** read as 1_B. Must be written as 1_B
ERRDIS	12	rw	**ECC Error Disable** When set SRI bus errors caused by ECC errors in data read from the SRAM will be disabled 0_B Normal behaviour. SRI error will occur on SRAM ECC errors if DED_EN is set. Default after reset 1_B Test Mode. SRI errors will not be generated on an SRAM ECC error. This does not affect the generation of interrupts.
RES	13	r	**Reserved**
RES3	14	r	**Reserved** Read as 0_B

Field	Bits	Type	Description
DBERR	15	rwh	**Double Bit Error Status** This bit set when a double bit error has occurred when reading from the local memory. The bit is cleared by writing 0_B. Writing 1_B has no effect. 0_B read access did not have a double bit error 1_B read access did have a double bit error
RES4	23:16	r	**Reserved** Read as 00_H, must be written as 00_H
ECCR	31:24	rh	**ECC Code for Last Read Access** This field contains the ECC code retrieved from the local memory with the last read access.

LMU Module ID Register

LMU_MODID

LMU Module ID Register **(008_H)** **Reset Value: $0088\ C001_H$**



Field	Bits	Type	Description
ID_VALUE	31:0	r	**Module Identification Value**

7 Data Access Overlay (OVC)

The data overlay functionality provides the capability to redirect data accesses by the TriCore to program memory (internal Program Flash or external memory) to the LMU SRAM, or to the Emulation Memory in Emulation Device ED, or to the external memory. This functionality makes it possible, for example, to modify the application's test and calibration parameters (which are typically stored in the program memory) during run time of a program. Note that read and write data accesses from/to program memory are redirected.

Attention: As the address translation is implemented in the DMI it is only effective for data accesses by the TriCore. Instruction fetches by the TriCore or accesses by any other master (including the debug interface) are not affected!

Note: The external memory can be used as overlay memory only in selected devices. Please contact Infineon sales representative for more information.

Summary of Features and Functions

- 16 overlay ranges ("blocks") configurable for Program Flash and external memory;
- Support redirection to Overlay memory located in:
  - Local Memory (LMU)
  - Emulation Memory (Emulation Device only)
  - External EBU Space (selected devices only)
- Support of up to 2 MB overlay memory address range;
- Overlay block size from 32 byte to 128 Kbyte;
- Support of Online Data Acquisition into range of up to 32 KB and of its overlay;
- Overlay memory and block size selected individually for every overlay block;
- All prepared overlay blocks can be enabled with only one register write access;
- Programmable flush (invalidate) control for data cache in DMI.

7.1 Basic Overlay Control

Per overlay block, there are three possibilities for redirection of the original data address, redirection to the LMU SRAM, redirection to the external memory and redirection to the Emulation Memory EMEM, if the chip includes the Emulation Extension Control EEC for an Emulation Device. In all cases, the same overlay mechanism is used.

The basic overlay scheme is shown in **Figure 7-1**.

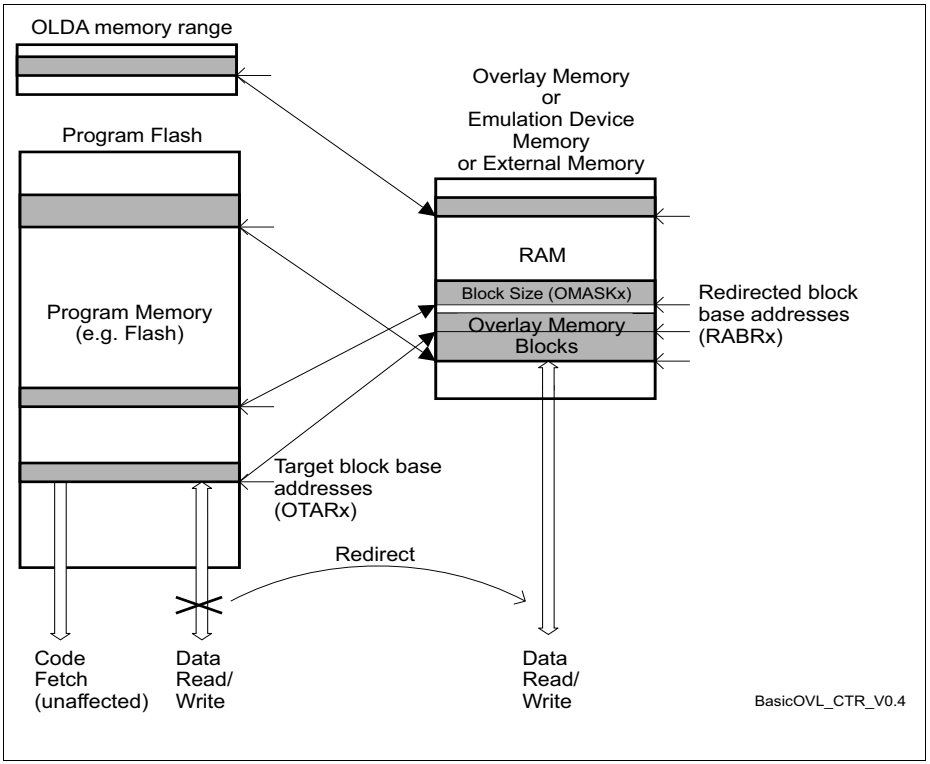


Figure 7-1 Redirection of Data Accesses to/from Code Memory to Overlay Memory

In the TC1798, the target memory (Program Flash, external memory or OLDA range, see **Chapter 7.4.1**) can be divided into a maximum of sixteen memory blocks for redirection into an overlay memory. The base address in target and overlay memory as well as the block size of each overlay block can be individually selected. The possible sizes of overlay blocks depend on the selected overlay memory: Blocks in the internal LMU SRAM are smaller than overlay blocks in EMEM or external memory. All overlay blocks can be enabled concurrently with one register access. In addition, the data cache may be flushed.

The operation of the address translation process is described in **Figure 7-2**, shown for redirection into the LMU SRAM.

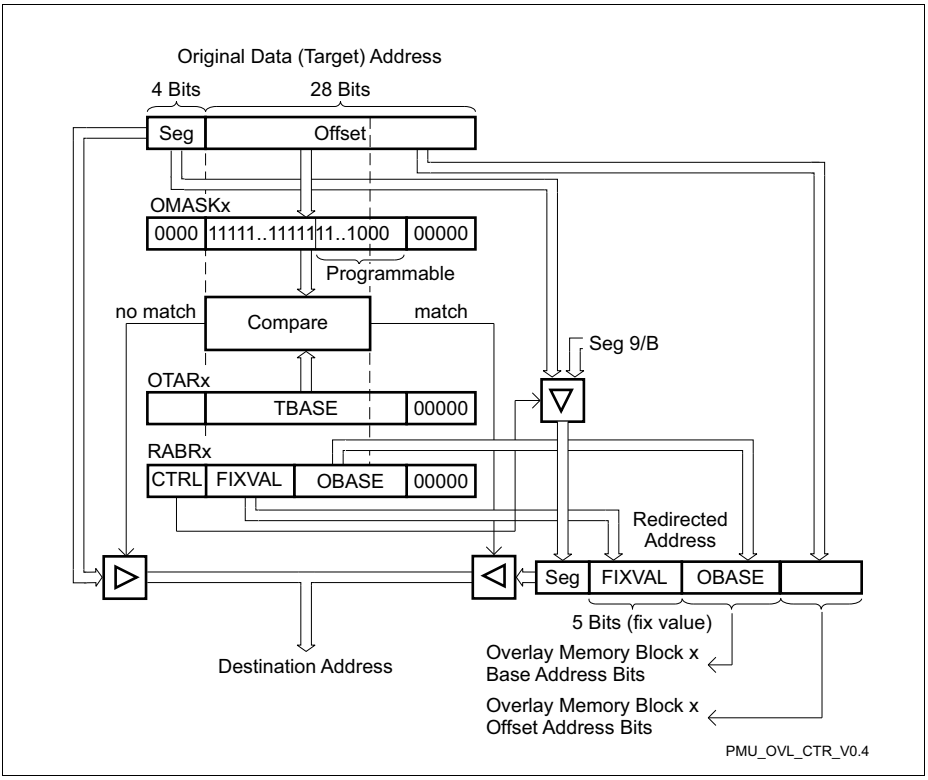


Figure 7-2 Address Translation Process

In each enabled overlay block control logic, three registers hold the information to control the overlay functionality:

- The overlay target address in the Overlay Target Address Register OTARx, which determines the base address of the program or OLDA memory data block x to be redirected.
- The base address of the LMU SRAM, external memory or EMEM (if emulation Device) in the Redirected Address Base Register RABRx, and the related enable and control bits.
- A mask in the Overlay Mask Register OMASKx, defining the size of the block, the address bits to be checked for an address match, and which bits are used from the redirected address base and which from the original data address.

The size of the overlay memory blocks can be 2^n x 32 bytes, with n = 0 to 12. This gives the block size range from 32 bytes to 128 Kbytes. The start address of the block can be an integer multiple of the programmed block size (natural page boundary).

If the data segment address is A_H or 8_H, the segment offset of the original data address is compared with the target base addresses of all overlay blocks which are enabled in RABRx. This bit-wise comparison is qualified by the content of the mask, ignoring the address bits that form the offset into the overlaid block.

If there is no match, the original data address is taken to perform the access.

If there is a match (see **Figure 7-2**):

- The four segment address bits (A_H or 8_H) are either taken directly from the data address (for external overlay memory) or changed to B_H and 9_H, respectively (for internal and emulation overlay memory).
- The most significant part of the segment offset, that addresses the base address of the overlay memory, is set to predefined values according to the address map (fixed bits in registers RABRx).
- The part of the target block address, that corresponds to the overlay block base address, is replaced by the respective overlay block base address bits (bits OBASE in RABRx, where the corresponding mask bits OMASK in registers OMASKx are set to “1”).
- The address is completed by the original offset into the block; the number of bits used are determined by the bits set to “0” in the mask OMASK.

7.2 Online Data Acquisition (OLDA) and its Overlay

Calibration is additionally supported by an OLDA memory range of up to 32 Kbyte, which is a virtual memory and physically only available, if it is redirected (as described above) to the internal or external overlay memory or to the EMEM in Emulation Device. If OLDA is enabled in PMU, direct write accesses (without redirection) to the OLDA range are not really executed, and they do not generate a bus error trap. This trap suppression works only for accesses to the non-cached range. Read accesses to the OLDA range generate a bus error trap, if not redirected to a physically available overlay block.

The base address of the virtual OLDA memory range is A/8FE7 0000_H, the end address is A/8FE7 $7FFF_H$. Accesses to the OLDA range are also supported in cached address space but there the bus error trap for write accesses is not suppressed.

Note: In OTARx registers, any target address can be selected for redirection, thus also addresses in the OLDA range. However, the handling of direct accesses to the OLDA range is completely controlled in the PMU.

7.3 Enable Control of Overlay Blocks

For basic control of overlay execution, the OCON register is provided with following functionality:

- 16 enable bits (SHOVENx), one for every overlay block configuration, to support concurrent and parallel switching of up to 16 overlay ranges (blocks); shadow

functionality to the single enable bits in the 16 block control registers (RABRx) provide compatibility to enable-control in TC1766/96.
- One common overlay start bit (OVSTRT) to enable all prepared (enabled) overlay configurations by writing all shadow enable bits into the 16 block control registers in parallel (write-only bit); stop-function if all-zeros are written.
- One control flag (DCINVAL), to be set by the CPU or Cerberus, to flush (invalidate) the (clean) data cache lines in the DMI (write-only bit).
- One common overlay stop (OVSTP) bit to disable all overlay configurations in the 16 block control registers (write-only bit), without changing the configuration
- One overlay configured status bit (OVCONF), which may be set when overlay registers are configured by the Cerberus via JTAG interface, and which may be cleared by the CPU after common overlay start (re-direction of all enabled overlay blocks).

The control flag in the high byte of the Overlay Control Register OCON (see **Page 7-14**) is implemented with additional protection bit, supporting write access to OCON by different users without violation of such control bit which shall remain unchanged. Additionally, byte protection is possible by support of byte write accesses to OCON.

7.4 Target and Overlay Memories

In the following, the possible target and overlay memories are described. Address range of 2 MB is supported for the overlay memories. The LMU SRAM and the interface to the Emulation Memory EMEM are located in the LMU module.

7.4.1 Target Memories

Any data read or write access to the segments 8_H and A_H is checked for a valid overlay target address, using all 16 OTARx registers concurrently for comparison (if they are enabled for overlay execution). Since the OTARx registers are writable, any data memory within the segments 8_H and A_H may be used for redirection to an overlay memory. Thus, the following memories can be selected as target memories:

- Program Flash
- Data Flash
- The (virtual) OLDA memory range
- The external memory.

7.4.2 Internal Overlay Memory

The internal LMU SRAM is available in both the Production Device and the Emulation Device. The LMU SRAM is selected for overlay redirection, if the bits IEMS and EXOMS in the block-related RABRx register are zero. The base address of the LMU SRAM is B/9000 0000_H (non-cached/cached space). During address translation, the upper 9 address bits are set to $B/90_H0_B$, respectively.

7.4.3 Emulation Overlay Memory

The EMEM can only be selected for overlay blocks, if the chip is an Emulation Device ED. The Emulation Memory EMEM is selected for overlay execution, if the block-related RABRx bits IEMS=1 and EXOMS=0. The base address of the Emulation Memory is B/9F00 0000_H. During address translation, the upper 9 address bits are set to BF_H0_B (non-cached) or to $9F_H0_B$ (cached space).

7.4.4 External Overlay Memory

If an external memory is available in the Emulation Device system, it can also be used for calibration via program memory or OLDA overlay. The overlay blocks can be located in the external memory only in selected devices.The External Memory is selected for overlay execution, if the block-related RABRx bit EXOMS=1 (IEMS value is ignored). The base address of the Emulation Memory is A/8300 0000_H. During address translation, the upper 9 address bits are set to $A3_H0_B$ (non-cached) or to 83_H0_B (cached space).

7.5 Change of Overlay Parameters and Overlay Start

When changing the overlay parameters of a block or when switching a block from one overlay memory to another overlay memory, it must be ensured that the respective OVEN bit in register RABRx is reset, before the block parameters are set properly, and then the overlay block is enabled again. Otherwise, unintended access redirections may occur.

It is especially supported to enable (start) all prepared overlay blocks concurrently, when using the shadow mechanism for the OVEN bits in the one OCON register instead of the single OVEN bits in the different RABRx registers (see **Chapter 7.3**). With this function it is possible to switch directly from one set of overlay blocks to another set of overlay blocks, without any restriction concerning the block-specific use of (available) overlay memories.

Note: The Overlay Control does not prevent configuring the translation logic incorrectly so that memory accesses are translated to not implemented or forbidden memory ranges.

7.6 Concurrent Matches and Access Performance

Concurrent matches in more than one enabled overlay block are not supported. When an address matches two, or more, of the enabled overlay blocks, an exception is raised and the memory access is not performed. A load operation with multiple matches on overlay ranges, raises a Data Access Synchronous Error (DSE) trap, and a store operation raises Data Access Asynchronous Error (DAE) trap. In such case, relevant trap information registers: Data Synchronous Trap Register (DSTR), Data

Asynchronous Trap Register (DATR), and Data Error Address Register (DEADD) are updated, see DMI Registers chapter for more information.

The dynamic address translation for redirection to the overlay memory is executed without performance penalty.

7.7 Overlay Control Registers

Figure 7-3 shows all the overlay control registers associated with control of the overlay memory blocks.

Overlay Control Registers Overview

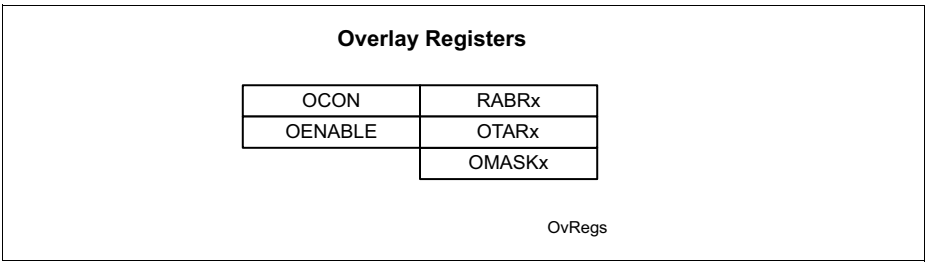


Figure 7-3 Overlay Control Registers

The address space for the overlay control registers is as follows:

Table 7-1 Registers Address Space of OVC Registers

Module	Base Address	End Address	Note
OVC	F87F FB00$_H$	F87F FBFF$_H$	

Table 7-2 Registers Overview

Register[1] Short Name	Register Long Name	Offset Address	Access Mode[2]		Description see
			Read	Write	
RABRx	Redirected Address Base Register x (x = 0-15)	0020$_H$ + x * C$_H$	U, SV, 32	SV, 32	Page 7-9
OTARx	Overlay Target Address Register x (x = 0-15)	0024$_H$ + x * C$_H$	U, SV, 32	SV, 32	Page 7-11

Table 7-2 Registers Overview (cont'd)

Register[1] Short Name	Register Long Name	Offset Address	Access Mode[2]		Description see
			Read	Write	
OMASKx	Overlay Mask Register x (x = 0-15)	0028_H + x ∗ C_H	U, SV, 32	SV, 32	Page 7-12
OCON	Overlay Control Register	$00E0_H$	U, SV, 32	SV, 32	Page 7-14
OENABLE	Overlay Enable Register	$00E8_H$	U, SV, 32	SV, E, 32	Page 7-16

1) The OVC register short names are extended with the module name prefix "OVC_".

2) Symbol U: Access permitted in User Mode 0 or 1
Symbol SV: Access permitted in Supervisor Mode
Symbol E: Endinit-protected register
Symbol 32: Only 32-bit word access is permitted

Note: Accesses to free/not used register addresses within the OVC address space are not executed and not serviced with a bus error trap.

Register Descriptions

For each of the 16 overlay memory blocks (indicated by index x), three registers control the overlay operation and the memory selection:

- The Redirected Address Base Register RABRx, which holds the base address of the overlay memory to be used (with fixed address bits) and of the overlay memory block within the overlay memory, and some control bits.
- The Overlay Target Address Register OTARx, which holds the base address of the memory block in internal Flash, in external memory or in the OLDA memory being overlaid (and being compared with original data address).
- The Overlay Mask Register OMASKx, which determines which bits (from RABRx) are used for the base address (of overlay memory and block) and which bits (of original data address) are directly used as offset within the block (remaining unchanged).

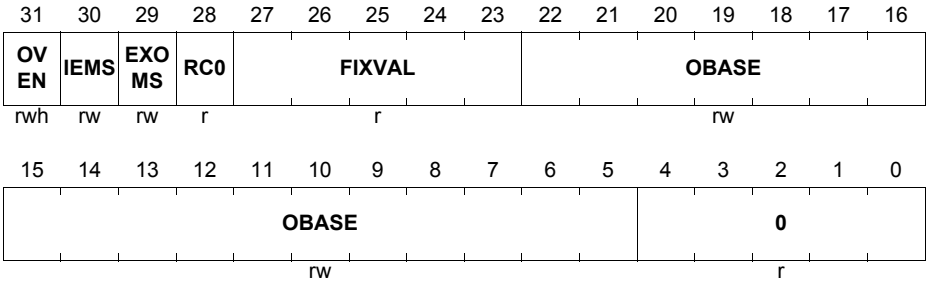
Additionally, for general overlay control the registers OCON and OENABLE are provided.

All overlay block and control registers are reset to their default values with the application reset. A special debug reset is not considered.

The RABRx register is defined as follows:

RABRx (x=0-15)
Redirected Address Base Register x

(20_H+x*C_H) **Reset Value: 0000 0000_H**



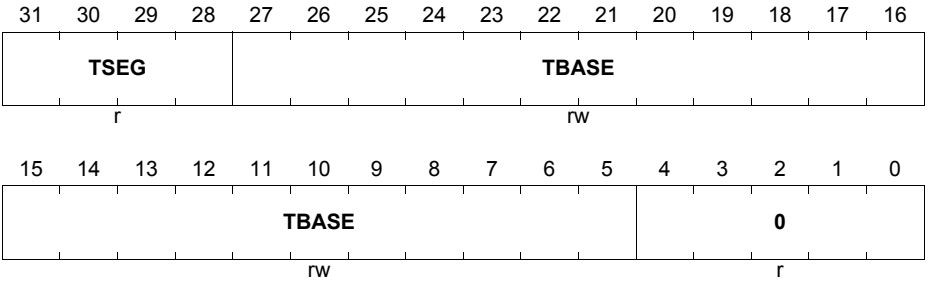
Field	Bits	Type	Description
OBASE	[22:5]	rw	**Overlay Block Base Address** This bit field holds the base address of the overlay memory block in the overlay memory.
FIXVAL	[27:23]	r	**Fixed Value** Base address of the selected overlay memory within segment. 00000_B LMU SRAM base address (when EXOMS=0 and IEMS = 0) 11110_B EMEM base address (when EXOMS=0 and IEMS = 1) 00110_B EMEM base address (when EXOMS=1) All other values are reserved. Should be written with the same value.
RC0	28	r	**Reserved Control Bit** Reserved for future control expansions. Read returns 0. Must be written with 0.

Field	Bits	Type	Description
EXOMS	29	rw	**External Overlay Memory Select** If set, the external memory is used as overlay memory. This is only available in selected devices. 0_B Overlay memory of block x type is selected by IEMS. 1_B Overlay memory of block x is the external memory.
IEMS	30	rw	**Internal or Emulation/External Memory Select** If EXOMS is not set, IEMS selects the type of the overlay memory. If EXOMS is set, IEMS value is ignored. 0_B Internal LMU SRAM is selected as overlay memory. 1_B Emulation Memory EMEM is selected as overlay memory. IEMS must be written with zero in production device.
OVEN	31	rwh	**Overlay Enabled** This bit controls whether or not the overlay function of overlay block x is enabled. 0_B Overlay function of block x is disabled. 1_B Overlay function of block x is enabled. This bit can also be changed via its shadow bit in the OCON register.
0	[4:0]	r	**Fixed Value** Read as 0; should be written with 0.

The Overlay Target Address Register OTARx is defined as follows:

OTARx (x=0-15)
Overlay Target Address Register x

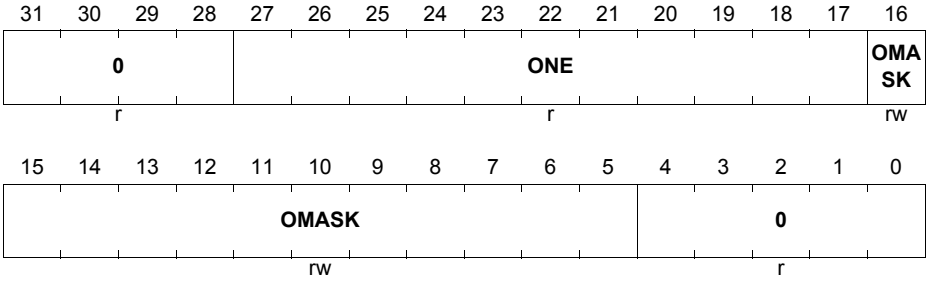
(24_H+x*C_H) **Reset Value: 0000 0000$_H$**



Field	Bits	Type	Description
TBASE	[27:5]	rw	**Target Base** This field holds the base address of the overlay memory block in the target memory (Program Flash or OLDA memory or external memory). For each TBASE bit: If the corresponding bit in OMASK register is set to one TBASE bit value is used in the address match. If the corresponding bit in OMASK register is set to zero TBASE bit value is ignored.
TSEG	[31:28]	r	**Target Segment (reserved)** This bit field is reserved for future use, to select a segment. In TC1798 implementation, any access to segments 8_H, or A_H will be checked for a valid base address. Returns 0 if read; should be written with 0.
0	[4:0]	r	**Reserved** Reads as 0; should be written with 0.

The Overlay Mask Register OMASKx determines the size of the overlay memory block x (by the number of least significant zero's). It also determines which address bits will participate in the address compare for the block base address (all high-order one's), and in case of address match which bits are taken from RABRx (as many high order bits as defined in OMASKx for address compare) and which bits are used from the original data address as offset within the block (all low order bits related to zero values in OMASKx).

OMASKx (x=0-15)
Overlay Mask Register x **(28_H+x*C_H)** **Reset Value: 0FFF FFE0$_H$**



Field	Bits	Type	Description
OMASK	[16:5]	rw	**Overlay Address Mask** This bitfield determines the overlay block size and the bits used for address comparison and translation. 000000000000_B, 128 Kbyte block size 100000000000_B, 64 Kbyte block size 110000000000_B, 32 Kbyte block size [...] 111111111110_B64 byte block size 111111111111_B32 byte block size "Zero" bits determine the corresponding address bits which are not used in the address comparison and thus determine the block size; corresponding final address bits are derived from the original data address. "One" bits determine the corresponding address bits which are used for the address comparison; corresponding final address bits are derived from RABRx register in case of address match.

Field	Bits	Type	Description
ONE	[27:17]	r	**Fixed “1” Values** Corresponding address bits are participating in the address comparison. Corresponding final address bits are taken from RABRx.
0	[4:0], [31:28]	r	**Fixed “0” Values** Corresponding address bits are not used in the address comparison. Corresponding final address bits are taken from the original data address.

The Overlay Control Register OCON is defined as follows:

OCON
Overlay Control Register **($00E0_H$)** **Reset Value: $0000\ 0000_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	0	0	0	0	0	POVCONF	OVCONF	0	0	0	0	0	DCINVAL	OVSTP	OVSTRT
r	r	r	r	r	r	w	rw	r	r	r	r	r	w	w	w

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SHOVENx															
rw															

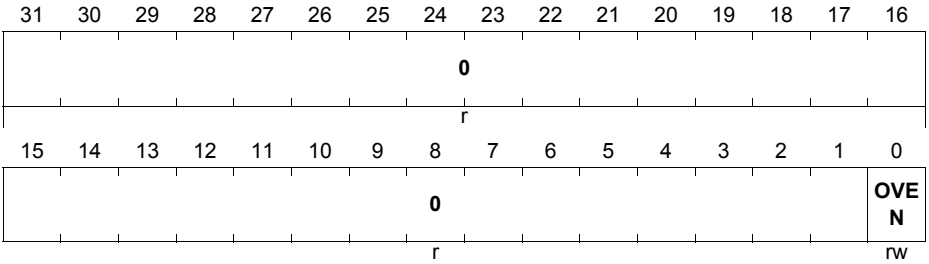
Field	Bits	Type	Description
SHOVENx (x=0-15)	x	rw	**Shadow Overlay Enable x** 0_B Overlay block x is disabled with next OVSTRT 1_B Overlay block x is enabled with next OVSTRT For each of the 16 overlay blocks (indicated by index x), one enable (disable) bit is provided.
OVSTRT	16	w	**Overlay Start** 0_B No action 1_B All 16 shadow overlay enable bits SHOVEN ar loaded into the related OVEN bits in RABRx registers in parallel. Related to the SHOVEN bits state, the overlay blocks are concurrently enabled or disabled. Return 0 if read.
OVSTP	17	w	**Overlay Stop** 0_B No action 1_B All 16 OVEN bits in RABRx registers are cleared in parallel independently of the SHOVEN bits and without changing the SHOVEN bits. Return 0 if read.

Field	Bits	Type	Description
DCINVAL	18	w	**Data Cache Invalidate** No function in devices without data cache in Tricore. 0_B No action 1_B Data Cache Lines in DMI are invalidated (flushed). *Note: Per write modified cache lines are not invalidated.*[1)] Return 0 if read.
OVCONF	24	rw	**Overlay Configured** Overlay configured status bit 0_B Overlay is not configured or it has been already started by CPU 1_B Overlay block control registers are configured and ready for overlay start This bit may be used as handshake bit between a debug device (via JTAG interface and Cerberus) and the CPU.
POVCONF	25	w	**Protection Bit for OVCONF** 0_B Bit protection: Bit OVCONF remains unchanged with register OCON write 1_B OVCONF can be changed with actual write access to register OCON This bit enables OVCONF-write during OCON write. Return 0 if read.
0	[23:19], [31:26]	r	**Reserved** Read/write 0.

1) Because the data cache is a writeback cache (not a writethrough cache; therefore saving of modified data in cache has to be performed by the user) it is highly recommended to use only non-cached accesses for overlaid (redirected) accesses to the target memory (normally the Program Flash), if write accesses are involved.

The Overlay Enable Register OENABLE is defined as follows:

OENABLE
Overlay Enable Register **($00E8_H$)** **Reset Value: $0000\ 0000_H$**



Field	Bits	Type	Description
OVEN	0	rw	**Overlay Enable** 0_B OVC is disabled. All Overlay redirections are disabled. 1_B OVC is enabled.
0	[31:1]	r	**Reserved** Read/write 0.

This register is Endinit-protected.

8 BootROM Content

TC1798 BootROM from user point of view consists of two parts:

- Startup Software (short name SSW);
- Software modules implementing additional functions (Bootstrap Loaders).

8.1 Startup Software

The Startup Software is the first software executed after a chip reset. This means, the first value loaded into the Program Counter register PC points to first address inside BootROM - the SSW entry-point.

The Startup Software contains procedures to initialize the device depending on:

- values applied to external (configuration-) pins;
- the type of event which has triggered the SSW-execution (the last reset event);
- information previously stored into the Flash Configuration Sector;
- the current state of special bits/fields in dedicated register/memory locations.

The SSW also calls - in case - other firmware modules.

8.1.1 Boot Options Summary

This chapter summarizes the TC1798 startup configurations.

Internal Start

In this basic startup mode, the first user instruction is fetched from the Internal Program Flash of the device.

Bootloader Modes

Different Bootstrap Loader routines are used in these modes to download code/data into the Program Scratchpad Memory PSPR.

Alternate Boot Modes

In these modes, program code is started from user-defined address but only if at least one of the two check-conditions is satisfied. If both the conditions are false - a Bootstrap Loader routine is started to download the code into the device, this code is afterwards started by the SSW.

Secure Booting

This startup option is only supported in devices having Secure Hardware Extension (SHE) implemented and available for the user.

When selected, Secure Booting implements an extension of the startup procedure in Internal start and Alternate Boot Modes, using SHE to check the user code.

8.1.2 Startup Software Main Flow

In next Chapters, the SSW functionality is specified, during different execution-steps (refer to **Figure 8-1**) and upon various configuration settings.

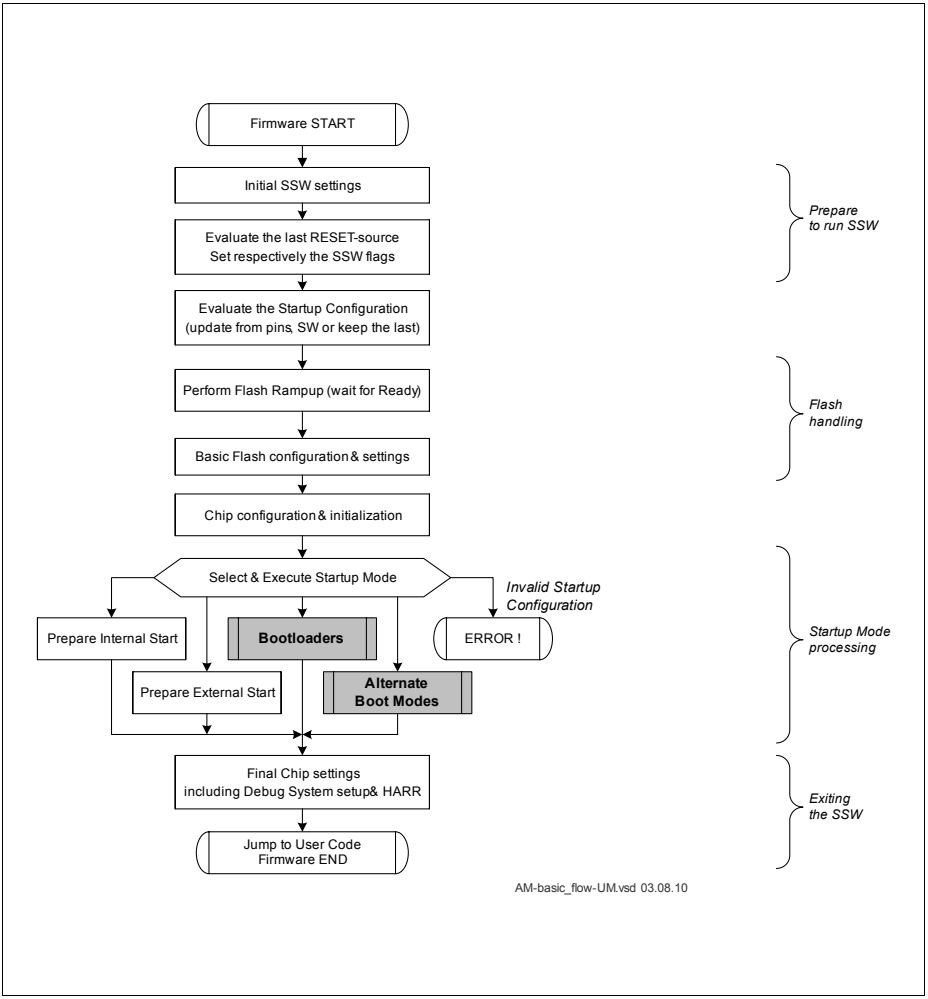


Figure 8-1 TC1798 Firmware: SSW main flow

8.1.2.1 Entering the Startup Software

The first SSW instruction is fetched after any reset from address AFFF'C000$_H$ in BootROM.

8.1.2.2 Initial Handling of the Startup Configuration

The SSW determines which startup mode to execute based on the configuration coded in SCU_STSTAT.HWCFG bit field.

The value in this bit field can be updated in different ways:

1. with values latched at the configuration pins P0[7:0] upon the rising reset-edge
   This happens when SCU_STSTAT.LUDIS=0, therefore after any system (class 0) reset, and after other resets - depending on LUDIS bit.
2. with values from SCU_SWRSTCON.SWCFG bit field
   This happens upon Software reset - triggered by writing 1 to SCU_SWRSTCON.SWRSTREQ - if at the same time Software Boot Configuration is selected - SCU_SWRSTCON.SWBOOT=1.

Due to the way HWCFG-bit field is handled by TC1798 hardware, at this point of its flow the SSW does not need to do some special processing regarding the startup configuration. besides of setting SSW-internal flag:

- "Reset Configuration Updated" flag
  – is set to 1 if
    - the last reset has been a software-reset with software-configuration
      ((SCU_RSTSTAT.SW=1) AND (SCU_SWRSTCON.SWBOOT=1))
  – if the last reset is of a type NOT stated in a)
    - the flag is set to the inverted value of SCU_STSTAT.LUDIS bit

8.1.2.3 Flash Rampup

The Flash Rampup is automatically started after every reset by hardware (refer to PMU Chapter, Program and Data Flash). Therefore the SSW does not initiate the Rampup but only observes the flags in Flash SFRs and reacts accordingly.

The Flash Rampup is further handled by the SSW. Basically the Flash "Busy" status is checked as the section below describes.

If after the time-out the Flash is still "Busy", then:

- "Flash Rampup" error-code is created
- the Flash is put into sleep mode
- a jump to the SSW Error-processing routine is performed

Flash Rampup

Flash "Busy" status is continuously checked but no longer than for a defined time-out. Once all of the Flash Array Banks are "Ready" (PBUSY=0), the startup procedure

continues immediately. As far as the Rampup duration varies from device to device and upon operational conditions, the overall startup time respectively will be slightly different.

8.1.2.4 Basic Device Settings

The target of this functional module is to initialize several TC1798-registers with the values, which will be first seen by the user - or generally available - after exiting the SSW.

Following device resources are initialized here:

- JTAG Device Identification register (JTAGID.JTAG_ID)
- Unique Chip ID - it is written by the SSW at the beginning of DSPR - 4 Words starting at $D000'0000_H$.

8.1.2.5 Select and Prepare Startup Modes

TC1798 User Startup Configurations and modes are summarized in **Table 8-1**.

Table 8-1 Startup Modes supported in TC1798

HWCFG[7:0]	Startup Mode	Pins used
11xxxxxx$_B$	Internal Start from Flash	2
011xxxxx$_B$	Internal Start from Flash	3
010xxxxx$_B$	Bootstrap Loader Mode, Generic Bootloader at CAN pins	3
10101xxx$_B$	Bootstrap Loader Mode, ASC Bootloader	5
10100xxx$_B$	Alternate Boot Mode (ABM),ASC Bootloader on fail	5
1011xxxx$_B$	Alternate Boot Mode, Generic Bootloader at CAN pins on fail	4
1000xxxx$_B$	Alternate Boot Mode, Generic Bootloader at CAN pins on fail	4
1001C1Ax$_B$ [1)]	External Alternate Boot Modes	7
0010E1Ax$_B$ [1)]	External Start Modes	7
0001xxxx$_B$	Reserved	7
000011xx$_B$	Reserved	6

1) C bit - Pins used for bootloading: 0 - ASC (ASC bootloader);1 - CAN (Generic bootloader)
A bit - EBU Arbitration Mode: 0 - Participant; 1 - Arbiter (previously referred as “External Master”)
E bit - EBU Configuration: 0 - Default; 1 - Automatic

The SSW evaluates the configuration in SCU_STSTAT.HWCFG and device-start is prepared in accordance to the mode currently selected.

Basically, the User Start Address is prepared in STADD, as well as additional functions are executed in case - like Bootstrap Loaders and Alternate Boot.

Internal Start

This is the basic TC1798 type of operation in which the user code is started out of the Internal Flash Memory.

The User Start Address STADD is set to the beginning of Internal Flash Memory Module at address A000'0000$_H$.

External Starts

The User Start Address STADD is set to address A300'0000$_H$ in external EBU space.

Bootstrap Loader Modes

The selected Bootstrap Loader (these routines are described in **Chapter 8.2**) is executed only if the SSW-flag "Reset Configuration Updated" is set (refer to **Chapter 8.1.2.2**). This is to avoid multiple executions of the Bootstrap Loader and to start directly the code already downloaded after some - intended to be "application only" - reset events, for example after a Watchdog Timer reset which has been configured as class 3 reset.

The supported Bootloader selections are:

- ASC Bootloader - ASC communication protocol via ASC pins
- Generic Bootloader via CAN pins - the communication protocol is automatically selected by the SSW between ASC and CAN

After downloading (in case) the code, the User Start Address STADD is set to the beginning of Program Scratchpad RAM at C000'0000$_H$.

Alternate Boot Modes

There are variety of such modes in TC1798, whereas the differences are in:

1. where the Headers and (in case being available) the application code is located
   a) in Internal Flash Memory
   b) in External Memory
2. which Bootloader to execute upon an error in ABM Header
   a) ASC Bootloader
   b) Generic Bootloader at CAN pins

The SSW flow in these modes is:

- evaluate the startup configuration to decide where are the Headers located
- check the Headers - refer to the description in **Chapter 8.1.3.1** - and react accordingly:
  – if the check is OK for one of the Headers - set the User Start Address STADD to the respective value from this correct header (STADABMx) and continue

– if the Header-checks fail - start a Bootloader (ASC/Generic) corresponding to the startup configuration. After downloading the code, the User Start Address STADD is set to the beginning of Program Scratchpad RAM at $C000'0000_H$.

Secure Booting is possible in Alternate Start mode - see below.

Secure Boot option handling

If SHE-module is available - Secure Booting is supported for the device. In such a case the SSW performs additional steps in different startup modes, as below described.

- in **Internal Start** mode:

1. check the SHE-bit sequentially in SHEBOOT2, SHEBOOT0 and SHEBOOT1 registers
   a) if all the bits are zero - Secure Booting is not requested, then:
      -call SHE_NON_SECURE_BOOT procedure
      -continue SSW (executing Internal Start)
   b) if bit SHE=1 is found in a SHEBOOTx register - continue with 2.
2. read SIZE from the respective bitfield in SHEBOOTx register
3. call SHE_SECURE_BOOT procedure with parameters BL_START=STADD ($A000'0000_H$) and BL_SIZE=SHEBOOTx.SIZE
4. check the BGD-bit tn the respective SHEBOOTx register (with SHE=1)
   a) if SHEBOOTx.BGD=1 (background secure boot is selected) - continue SSW with user code start without waiting for SHE-operation finished
   b) if SHEBOOTx.BGD=0 (not background secure boot is selected) - wait until SHE_SECURE_BOOT procedure is finished

- in **External and Bootstrap Loader** modes:

Call SHE_NON_SECURE_BOOT procedure.

- in **Alternate Boot** modes:

There are two cases regarding SHE-handling in Alternate Boot Mode

1. if one of the Header-checks with CRC passed -Secure Boot procedure is executed to check the user code by SHE
2. if both the Header-checks with CRC failed - Bootstrap Loader mode is started and SHE_NON_SECURE_BOOT procedure called there.

8.1.2.6 Final Chip Settings

The last device configuration steps performed by the SSW include:

Unique Chip ID Installation

The Unique Chip ID represents a 16-Byte value which is written by the SSW after any reset at the beginning of DSPR - starting from address $D000'0000_H$.

Calibration Data Installation

The Calibration Data (for DTS as well as placeholder for future extensions) represents a 128-Byte value which is written after power-on reset by the SSW into DSPR starting from address $D000'0018_H$.

Flash Protection Control

The SSW processing on Flash protection differs upon the startup mode currently selected:

1. in modes where the user code is started from Internal Flash - Internal start, Internal ABM with CRC OK:
   a) if Read Protection is NOT activated (FCON.RPA=0):
      - SSW enables all the specific (DMA, PCP, Debug) Data Fetches from Flash
      - no SSW action is needed regarding Code and Data Fetches from Flash - they are generally enabled by hardware.
   b) if Read Protection is Activated (FCON.RPA=1):
      - SSW enables Code Fetch from Flash;
      - SSW enables Data Fetch from Flash in general as well as in particular for DMA (FCON.DDFDMA=0) and PCP;
      - SSW disables Data Fetch from Flash for the Debug Controller.
2. in modes where the user code is not started from Internal Flash - all Bootstrap Loader modes, all ABM modes after the CRC fails:
   a) if Read Protection is NOT activated (FCON.RPA=0) - the same functionality as upon a start from Internal Flash - refer to 1.a) above;
   b) if Read Protection is activated (FCON.RPA=1):
      - SSW disables all Code and Data Fetches from Flash
      - SSW disables all the specific (DMA, PCP, Debug) Data Fetches from Flash.

At the end of this module, accesses to Configuration Sector Data are disabled.

Debug System handling

As first point of this processing, the SSW internal flag Unlock Debug Interface is set, with exception of the following case only:

- Internal start with active Flash protection

In any other case, debugging is no security risk as far as either the protection is not activated or reading from Flash is not possible.

Next, Halt after Reset is prepared if requested. Besides a Halt itself is no security risk - even the system is stopped but a channel (communication/debug) is still needed to access internal resources - this feature is configured and enabled only if the SSW-flag “Unlock Debug IF” is set.

The SSW processing here is as follows:

- check either external (debug) access to the device will be generally granted (SSW_Internal_flag=1)
  – if Not -> exit this procedure
- check either Halt After Reset is requested (OSTATE.HARR=1)
  – if Not -> exit this procedure
- configure a Break After Make breakpoint at the last SSW instruction
  – write the respective address into Code Segment Protection Lower Bound register MPR_CPR0_0L
  – configure signal assertion from Memory Protection System to Core Debug Controller upon instruction fetch access match with MPR_CPR0_0L (write MPR_CPM0.BL0=1)
  – configure debug action in Trigger Event 0 control register TR0EVT as follows:
    - Halt on break - EVTA := 010_B
    - Break After Make - BBM := 0
    - Suspend output active - SUSP := 1
- enable On-Chip Debug Support system.

*Note: The final debug-related operation - unlocking (in case) the debug interface - is performed later - refer to **Chapter 8.1.2.7**.*

8.1.2.7 Ending the SSW and Starting the User Code

The last steps executed by the SSW are:

- activate the Startup Protection
  - as a result, the Watchdog Timer starts to run
- if the Debug Interface is to be unlocked (SSW_Unlock_DIF=1):
  – perform a write to OEC with IF_LCK=0 and IF_LCK_P=1 (protection bit). With this operation OSTATE.IF_LCK gets reset to 0 and the debug interface is unlocked - the IOClient (Cerberus) is allowed to enter RW Mode and therefore can access potentially all the system resources.
- restore default content of registers modified by SSW
- jump to the first User Instruction at address STADD.

8.1.3 Specific SSW Features

Below some specific procedures are described, which are used at several places during the SSW flow. The definition is given separately here for a more readable form of the complete document.

8.1.3.1 Header Check in Alternate Boot Modes

The Alternate Boot Modes (ABM) in TC1798 are intended to start program code already available at arbitrary user-defined address if a check-condition is satisfied. If the check-condition fails - a Bootstrap Loader routine is invoked in accordance to the current startup mode.

The address of the code to be started together with all information needed to verify the check-condition are contained in dedicated memory areas named Headers.

The address of the code to be started together with all information needed to verify the check-condition are contained in dedicated memory areas named Headers. The Headers can be located in Internal Flash memory of the device, whereas the locations are defined:

- Header 0 - Base address A001'FFE0$_H$; End address A001'FFFF$_H$
- Header 1 - Base address A000'FFE0$_H$; End address A000'FFFF$_H$

If External starts are also supported as Startup Configurations, respectively so-call External Alternate Boot Modes are defined. In such a case, the Headers are located in External EBU address space as follows:

- Header 0, External - Base address A300'FFE0$_H$; End address A300'FFFF$_H$
- Header 1, External - Base address A308'FFE0$_H$; End address A308'FFFF$_H$

Note: In all the External ABM, the SSW first tries to fetch the configuration word as check for availability of an external memory. If this fetch fails to return valid data - the situation is considered as error in the Header and a bootloader is started.

In Alternate Boot Mode of TC1798 two Headers are defined - Header 0 and Header 1 (referred as ABM.HD0 and ABM.HD1), the user code can be started from:

- up to two different addresses - if Secure Booting is not selected
- one only address - if Secure Boot option is activated.

The Headers are 32 Bytes long, containing information in accordance to **Table 8-2**.

Table 8-2 ABM Header Structure

Offset Addr.	Size Byte	Field Name	Description
00_H	4	STADABM	User Code Start Address
04_H	4	ABMHDID	ABM Header ID (Confirmation code): Standard ID = DEAD $BEEF_H$ (STDHID) Secure ID = CODE 0000_H (SECHID) 1) Background ID = CODE 0001_H (BSECHID) 1)
08_H	4	ChkStart 2)	Memory Range to be checked - Start Address
$0C_H$	4	ChkEnd 3)	Memory Range to be checked - End Address
10_H	4	CRCrange	Check Result for the Memory Range
14_H	4	$\overline{\text{CRCrange}}$	Inverted Check Result for the Memory Range
18_H	4	CRChead	Check Result for the ABM Header (offset 00H..17H)
$1C_H$	4	$\overline{\text{CRChead}}$	Inverted Check Result for the ABM Header

1) Only in Header 0

2) Address of the first word to be checked.

3) Address of the last word to be checked.

Header 0 is checked first, if failed and Secure Booting is not selected - Header 1 is checked next. Where the check gives OK, the full start address is taken from the respective Header field STADABMx (index x=0,1 for Header 0,1).

The validation procedure executes CRC calculation based on a 32-bit polynomial:

$$f(x) = x^{32}+x^{26}+x^{23}+x^{22}+x^{16}+x^{12}+x^{11}+x^{10}+x^8+x^7+x^5+x^4+x^2+x+1 \quad (8.1)$$

If Secure Booting is activated and the CRC calculation pass - the user code is also checked by SHE module.

The check procedure is as follows:

1. check the ABM Header ID (ABMHID) at offsets $04_H..07_H$:
   a) if ABMHDID=STDHID or SECHID or BSECHID - continue with 2.
   b) else - exit the check-procedure for this Header with Error.
2. calculate the CRC of the first 24 Bytes from the ABM Header (refer to **Table 8-2**) - process the fields STADABM...CRCRange at offsets $00_H...17_H$
   a) compare the result with the CRChead value (offset 18_H)
      - if OK - continue with 2.b)
      - if Not - exit the check-procedure for this Header with Error.
   b) inverse the result value and compare with $\overline{\text{CRChead}}$ (offset $1C_H$)
      - if OK - continue with 3.
      - if Not - exit the check-procedure for this Header with Error.

3. calculate the CRC over the memory address range ChkStart...ChkEnd (start- and end- addresses taken from offsets 08_H and $0C_H$ respectively)
   a) compare the result with the CRCrange value (offset 10_H)
      - if OK - continue with 3. b)
      - if Not - exit the check-procedure for this Header with Error.
   b) inverse the result value and compare with $\overline{\text{CRCrange}}$ (offset 14_H)
      - if OK - continue with 4.
      - if Not - exit the check-procedure for this Header with Error.
4. check the ABM Header ID (ABMHID) at offsets $04_H..07_H$:
   a) if ABMHDID=STDHID - continue SSW to start the user-code from STADABMx address.
   b) if ABMHDID=SECHID or BSECHID - continue with 5.
   c) else - exit the check-procedure for this Header with Error.
5. check are the requested memory addresses correct:
   a) both ChkEnd and ChkStart must be between A000 0000_H and A11F $FFFF_H$ or between 8000 0000_H and 811F $FFFF_H$ (cached or not-cached area) occupying only addresses reserved for PFlash and not overlapping a RAM or External area
   b) ChkStart must be aligned to 128 Byte (i.e. the 7 LS bit = zero)
      - if both the conditions are met - continue with 6.
      - if Not - exit the check-procedure for this Header with Error.
6. check with which Header ID the procedure passed till this point:
   a) if ABMHDID=BSECHID selecting background secure boot - continue SSW, Secure Boot will be triggered later by SSW
   b) if ABMHDID=SECHID selecting secure boot not background - then:
      - start secure boot and wait until finished
      - continue SSW to start the user-code from STADABMx address.

Note: As seen from the above definitions, both in Secure and in Standard ABM modes only error in Header or wrong CRC prevents starting the used code.
The result from code-check done by SHE is not relevant for the user code start but affects the further SHE behavior.

In case the check procedure is exited with error:

- if Header 0 is currently processed - restart the procedure from 1. using Header 1
- else - jump either to ASC- or to Generic- (CAN pins) Bootloader according to the startup mode currently configured in HWCFG.

8.1.4 Startup Errors Handling

There are a number of check-points during the Startup Software execution where Errors can be raised (refer to the SSW block-diagrams). The processing upon an Error is as follows:

- an Exit-code according to the error is stored into CBS_COMDATA register (refer to **Table 8-3**
- the Watchdog Timer Reset is configured to class 3
- all code- and data- fetches from Flash are disabled
- access to the Flash Config sector is disabled
- startup protection is activated, which activation starts the Watchdog Timer
- the debug interface is unlocked
- an endless loop is executed (jump to itself)

As far as the Watchdog Timer is already enabled, the endless loop is aborted by a WDT reset which triggers a new SSW-execution. If this new startup fails again, the following error-processing will lead to the same endless loop. Respectively, a second WDT reset will occur being already a locked reset, which can be aborted only by a next power-on sequence.

Table 8-3 Errors reported by the TC1798 SSW

Coding in d12/COMDATA	Description
00000001_H	Bootcode wrongly called after exiting startup mode
00000002_H	Flash error during rampup
00000003_H	Error in Flash Configuration sector
00000004_H	Invalid Startup mode selected
00000008_H	MultiCAN module not available but CAN Bootloader selected
00000018_H	CAN0 node not available (due to ATM) but CAN Bootloader selected
00000009_H	ASC module not available but ASC Bootloader selected
00000010_H	Error in BootROM
00000011_H	
00000012_H	Error in SHE module
00000013_H	Error in ERAY module during initialization (no XTAL clock)
$0000004x_H$	Trap of Class x (0..7) raised during SSW

8.2 Bootstrap Loaders

These routines provide mechanisms to load an user program via selected interface by moving code into Program Scratchpad RAM. The loaded code is started after exiting the BootROM.

Two interfaces can be utilized for downloading in TC1798 - ASC and CAN. Besides two separate procedures are supporting any of these interfaces/protocols, they have a common first part. In other words, there is one entry-point **bl_entry** for all bootloader procedures.

8.2.1 Common Procedures for all Bootloaders

The first such a common procedure is to reconfigure the clock system in case the last reset is a Power-on. This reconfiguration switches from the initial PLL Freerunning mode (VCO base frequency) to Prescaler Mode with F_{FPI}:F_{OSC}=1:2.

Therefore the FPI-peripherals (including MultiCAN and ASC modules) run at half the frequency of an external crystal which must be connected between XTAL1/XTAL2 pins if a Bootloader mode will be selected upon Power-on. This 1:2 relation must be taken into account when selecting the host speed for downloading. For example, when using the MultiCAN bootstrap loader F_{OSC} should be greater or equal to 20 MHz for a baud rate of 1 Mbit/s.

Attention: This clock-switch to external oscillator upon Power-on is overwritten by a switch back to PLL freerunning mode at the end of SSW .
Therefore if it is desired after downloading to continue communication with the same baudrate, the user code must first reinstall:
- PLL prescaler mode (SCU_PLLCON0.VCOBYP:=0) and
- K1 divider 1:1 (SCU_PLLCON1.KDIV:=00_H).

Upon any other reset but not power-on, the clock configuration - respectively the system frequency - remains the same as previously selected.

Next, depending on the Bootloader-type currently configured in HWCFG a pin is selected as receive-data input (RxD) which will be evaluated on the following step. Note, that still no further pin-configuration is done here - e.g. no assignment to a specific (ASC/CAN) module functionality - but only the pin input-value is directly checked in this procedure.

The procedure waits to receive a low-level pulse at RxD and measures its duration - the time between the falling and rising edges - into the BL_meas work variable.

Then, the SSW checks the startup configuration in HWCFG:

- upon ASC Bootloader Mode - a jump to the respective routine (**Chapter 8.2.2**) is directly executed
- upon Generic Bootloader Mode - the type of interface (ASC/CAN) currently used must be detected by the SSW. For this the RxD pin is checked until:

– low level is found there - then a jump to **CAN Bootstrap Loader**will be executed; **OR**
– no edge is found for a time 6 time longer than the value in BL_meas - then **ASC Bootstrap loader** will be executed.

This interface-detection procedure is based on the following principles:

- an ASC-Bootloader Host sends one only start Byte and then waits for a response from the target system
- a CAN-Bootloader Host sends a complete frame, whereas no more than 5 consecutive bits can be sent having equal logical levels - i.e. after two consecutive edges for a given time dT, in any case another edge must follow within the next time-frame of 6*dT.

8.2.2 ASC Bootstrap loader

The ASC Bootloading routine implements the following steps:

- RxD/TxD pins configuration is done in accordance to the TC1798 definitions, as well as depending either the routine is invoked upon “ASC Bootloader”-startup mode (ASC-only pins are used) or following an ASC-protocol detection upon “Generic Bootloader”-mode (CAN/ASC-shared pins are used but configured to ASC module)
- baudrate calculation is done based on the value already captured
- ASC0 is initialized (without enabling the receiver) to the baudrate as determined, 8 data and 1 stop bit
- acknowledge byte $D5_H$ is sent to the host indicating the device is ready to accept a data transfer
- after the acknowledge byte is transmitted, the receiver is enabled
- the bootloader enters a loop waiting to receive exactly 128 bytes which are stored as 32 words in Program Scratchpad RAM starting from address $C000'0000_H$

Once 128 bytes are received, the SSW starts the user code from address $C000'0000_H$.

8.2.3 CAN Bootstrap Loader

The CAN bootstrap loader transfers program code/data via node 0 of the MultiCAN module into the Program Scratchpad RAM. Data is transferred from the external host to the TC1798 using eight-byte data frames. The number of data frames to be received is programmable and determined by the 16-bit data message count value DMSGC.

The communication between TC1798 and external host is based on the following three CAN standard frames:

- Initialization frame - sent by the external host to the TC1798
- Acknowledge frame - sent by the TC1798 to the external host
- Data frame(s) - sent by the external host to the TC1798

The initialization frame is used in the TC1798 for baud rate detection. After a successful baud rate detection is reported to the external host by sending the acknowledge frame, data is transmitted using data frames.

Initialization Phase

The first task is to determine the CAN baud rate at which the external host is communicating. This task requires the external host to send initialization frames continuously to the TC1798. The first two data bytes of the initialization frame include a 2-byte baud rate detection pattern (5555_H), an 11-bit (2-byte) identifier ACKID for the acknowledge frame, a 16-bit data message count value DMSGC, and an 11-bit (2-byte) identifier DMSGID to be used by the data frame(s).

The CAN baud rate is determined by analyzing the received baud rate detection pattern (5555_H) and the baud rate registers of the MultiCAN module are set accordingly. The TC1798 is now ready to receive CAN frames with the baud rate of the external host.

Acknowledge Phase

In the acknowledge phase, the bootstrap loader waits until it receives the next correctly recognized initialization frame from the external host, and acknowledges this frame by generating a dominant bit in its ACK slot. Afterwards, the bootstrap loader transmits an acknowledge frame back to the external host, indicating that it is now ready to receive data frames. The acknowledge frame uses the message identifier ACKID that has been received with the initialization frame.

Data Transmission Phase

In the data transmission phase, data frames are sent by the external host and received by the TC1798. The data frames use the 11-bit data message identifier DMSGID that has been sent with the initialization frame. Eight data bytes are transmitted with each data frame. The first data byte is stored in Program Scratchpad RAM starting from address $C000'0000_H$. Consecutive data bytes are stored at incrementing addresses.

Both communication partners evaluate the data message count DMSGC until the requested number of CAN data frames has been transmitted.

After the reception of the last CAN data frame, the SSW starts the user code from address $C000'0000_H$.

8.3 Additional information and usage hints

The information below is provided to help the customer to use properly the functionality of TC1798 startup software.

8.3.1 Conditions upon user code start

After SSW, the user code execution starts upon the following basic conditions within TC1798:

- system clock
  - after power-on/PORST: PLL in freerunning mode, 16.66 MHz system frequency (nominal)

*Note: When in Bootloader mode - keep in mind the Attention-note at the beginning of **Chapter 8.2.1** (**Common Procedures for all Bootloaders**)!*

  - otherwise: as previously configured - no change due to the bootcode
- interrupts and traps
  - all maskable interrupts are disabled by ICR.IE=0
  - all NMI-traps are disabled in SCU_TRAPDIS
- Watchdog-Timer - running in time-out mode

8.3.2 RAMs Handling

No RAM initialization is performed by the Startup Software in TC1798.

Attention: In regard to TC1798 RAMs after startup the user must consider:

- if ECC will be enabled for a RAM module - correct initial content of this memory must be assured
- upon application software start, error detection is disabled in all memories

8.3.3 Influencing the next SSW-execution

By writing 1 to SYSCON.SETLUDIS (no protection), the user software will prevent automatic update of SCU_STSTAT.HWCFG upon the next application reset.

If such setting is active when a Bootstrap Loader mode is configured in STSTAT.HWCFG bitfield, after the next application reset the Bootloader routine will not be executed but directly the application-code will be started from SPRAM.

The LUDIS=1 setting will have effect until a system/power-on reset which will force the SYSCON register to its reset value with LUDIS=0. Therefore, upon system/power-on reset the startup HW-configuration (SCU_STSTAT.HWCFG) is always updated from pins.

8.3.4 TC1798 registers modified by SSW

TC1798 SSW modifies some registers against their reset value - refer to **Table 8-4**.

Table 8-4 TC1798 registers modified by SSW

Register	Value	Comments
SCU_STSTAT[18], [7:0]	EXTBEN, HWCFG	According to the current start-up mode
SCU_STCON[15]	1	Start-up protection activated
ERAY_SEDCON	$0000\ 0000_H$	SED disabled in ERAY RAMs
ERAY_DEDCON	$0000\ 0000_H$	DED disabled in ERAY RAMs
ERAY_CLC	$0000\ 0003_H$	ERAY module disabled
FLASHx_MARP[15], FLASH0_MARD[15]	0	Flash double-bit error traps enabled
FLASHx_FCON [22:17]	000000_B 111111_B	If Flash is not protected or Internal start mode If Flash is protected and not Internal start mode
CBS_OEC[17]	1	If Flash is not protected or Internal start mode

Additionally to the above, registers can be affected by dynamic conditions/events during SSW execution:

1. ASC/CAN configuration (clock settings, pin usage etc.) registers in BSL modes - depending on the start-up configuration and baudrate.
   The settings in these registers allow user software generally to continue using the same interface (ASC/CAN) after downloading - for this, keep attention to the note at **Page 8-13**.
2. PLLSTAT, TRAPSTAT registers - flag(s) can be set due to event/exception(s) during boot phase like loss-of-lock upon power-on and system reset.
   This is not critical for the application because the traps are generally disabled (in SCU_TRAPDIS) after any reset.

9 Memory Maps

This chapter gives an overview of the TC1798 memory map, and describes the address locations and access possibilities for the units, memories, and reserved areas as “seen” from the two different on-chip buses’ point of view.

The TC1798 has the following memories

- Program Memory Unit (PMU) with
  - 4 Mbyte of Program Flash Memory (PFLASH)
  - 192 Kbyte of Data Flash Memory (DFLASH)
  - 16 Kbyte of Boot ROM (BROM)
- Program Memory Interface (PMI)
  - 32 Kbyte of Instruction Scratch-Pad SRAM (PSPR)[1)]
  - 16 Kbyte of Instruction Cache (ICACHE)[2)]
- Data Memory Interface (DMI)
  - 128 Kbyte of Data Scratch-Pad SRAM (DSPR)[1)]
  - 16 Kbyte of Data Cache (DCACHE)[2)]
- Local Memory Unit (LMU)
  - 128 Kbyte of SRAM (LMURAM)[1)]
- PCP memory
  - 32 Kbyte of PCP Code Memory (CMEM)[1)]
  - 16 Kbyte of PCP Data Memory (PRAM)[1)]

Furthermore, the TC1798 has two on-chip buses:

- System Peripheral Bus (SPB)
- Shared Resource Interconnect (SRI)

Note: After PORST the ECC (single bit) correction is enabled, signalling of corrected ECC errors is disabled, signalling of detected non-correctable ECC errors is enabled.

1) Before used by the application, the memory has to be initialized by customer SW by overwriting it one time

2) When mapping Cache SRAM into the memory map and accessing as normal SRAM: the memory has to be initialized by customer SW before using it as normal SRAM by overwriting it one time

9.1 What is new

The target for the AudoMax devices memory map is to keep it compatible to AudoNG and AudoFuture wherever it is possible. This means to keep memory space/flash segment start addresses and peripheral control register address spaces where they where mapped to in AudoNG and AudoFuture.

Major differences of the TC1798 Memory Map compared to AudoFuture, TC1784 and TC1387:

- General:
  - Flash sizes, SRAM sizes and module instances adapted to the TC1798 requirements
  - Adaptation of the system address map to the TC1.6 requirements
  - Some modules shifted (start address / segment)
- Segment 8 / A:
  - PMU1 PFlash start address shifted
  - External EBU Space start address shifted, size reduced to 192 MB
  - OVRAM removed, LMU sram to be used as overlay memory instead
  - Emulation memory was shifted into segment 9 / B.
- Segment 8:
  - DFlash removed from segment 8
- Segment 9:
  - Added LMU SRAM
  - Added Emulation memory
- Segment A:
  - DFlash Bank0/1 start address shifted, size of DFlash Bank 0/1 increased
  - Address ranges for SHE KeyFlash Banks 0/1 added
- Segment B:
  - Added LMU SRAM
  - Added Emulation memory
- Segment C:
  - Segment is reserved for TC1.6 PMI SRAMs (Program Scratch Pad SRAM, ICache[1)] SRAM, PTAG SRAM[1)], image of Program Scratch Pad, PTAG[1)] and ICache SRAMs)
- Segment D:
  - Removed External EBU Space
  - Segment is reserved for TC1.6 DMI SRAMs (Data Scratch Pad SRAM, DCache[1)] and DTAG SRAMs[1)], image of Data Scratch Pad, DTAG[1)] and DCache SRAMs)
- Segment C / D:
  - Renamed SPRAM to PSPR (Program Scratch Pad SRAM)
  - Renamed LDRAM to DSPR (Data Scratch Pad SRAM)

1) Mapping of Cache and TAG SRAMs into the memory map is controlled by CPU register SMACON.

  - Lower half of segment C / D is fixed non-cached bahiour
  - Physical Memory Attributes (PMA) of upper half can be defined now via TC1.6 control registers (cached, non-cached)
- Segment E:
  - Reserved. There is no FPI->CPU bus address translation any more in SRI/TC1.6 systems.
- Segment F:
  - Shifted SSC0, SSC1, SSC2 to keep SSC3 and the SSC Guardian together
  - Lower part of the segment F reserved for FPI peripheral control registers, upper part reserved for SRI peripheral control registers
  - Added SSC2 / SSC3 module
  - Added SSC Guardian instances SSCG01 and SSCG21
  - Added Port16 and Port17 modules
  - Added ADC3 kernel
  - Added SDMA (Safe DMA module)
  - Added Bus Monitor Unit (BMU)
  - Removed LMBH, LFI and TC1.3 PMI/DMI registers
  - Added XBar_SRI module
  - Added LMU module
  - Added Flexible CRC Engine (FCE)
  - Added Secure Hardware Extension module (SHE)
  - Replaced TC1.3 against TC1.6 register ranges

9.2 How to Read the Address Maps

The bus-specific address maps describe how the different bus master devices react on accesses to on-chip memories and modules, and which address ranges are valid or invalid for the corresponding buses.

The FPI Bus address map shows the system addresses from the point of view of the SPB master agents. SPB master agents are PCP2 and is the DMA[1)].

The SRI address map shows the system addresses from the point of view of the SRI master agents. SRI master agents are PMI, DMI and DMA[1)].

The SFI is a bi-directional bridge between SRI and SPB and therefore not mentioned here as SRI or SPB master in the Address Map. The SFI is fully transparent and does not include an address translation mechanism.

1) DMA including: DMA Move Engines and module connected to the DMA Peripheral Interface like MLI modules.

Table 9-1 defines the acronyms and other terms that are used in the address maps (Table 9-2 and Table 9-3).

Table 9-1 Definition of Acronyms and Terms

Term	Description
…BE	Means “Bus error” generation.
…BET	Means “Bus error & trap” generation.
SPBBE	A bus access is terminated with a bus error on the SPB.
SPBBET	A bus access is terminated with a bus error on the SPB and a DSE trap (read access) or DAE trap (write access).
SRIBE	A bus access is terminated with a bus error on the SRI.
SRIBET	A bus access is terminated with a bus error on the SRI and a DSE trap (read access) or DAE trap (write access).
access	A bus access is allowed and is executed.
ignore	A bus access is ignored and is not executed. No bus error is generated.
trap	A DSE trap (read access) or DAE trap (write access) is generated.
32	Only 32-bit word bus accesses are permitted to that register/address range.
nE	A bus access generates no bus error, although the bus access points to an undefined address or address range. This is valid e.g. for CPU accesses (MTCR/MFCR) to undefined addresses in the CSFR range.

9.3 Contents of the Segments

This section summarizes the contents of the segments.

Segments 0-7

These segments are reserved segments in the TC1798.

Segment 8

This memory segment allows cacheable access to PFlash, External EBU Space, BROM.

Accesses from the DMA Move Engines, Cerberus or MLI to this segment are processed by the DMA SRI master interface on the SRI Bus.

Segment 9

This memory segment allows cacheable access to LMU SRAM and EMEM (Emulation Device only).

Segment 10

This memory segment allows non-cacheable access to PFlash, DFlash, External EBU Space, BROM.

From the DMA point of view, Move Engine, Cerberus and MLI accesses to this segment are processed by the DMA SRI master interface on the SRI Bus.

Segment 11

This memory segment allows non cacheable access to LMU SRAM and EMEM (Emulation Device only).

Segment 12

This memory segment allows access to the Program Scratch Pad SRAM (PSPR), PTAG SRAM and the Program Cache (ICache).

ICache and PTAG SRAM can be only accessed if the Program Cache is disabled[1)].

The attribute of this segment (cached / non-cached) can be partially configured[1)].

Segment 13

This memory segment allows access to the Data Scratch Pad SRAM (DSPR), DTAG SRAM and the Data Cache (DCache).

DCache and DTAG SRAM can be only accessed if the Data Cache is disabled[1)].

1) see CPU chapter, register SMACON, for details.

The attribute of this segment (cached / non-cached) can be partially configured.

Segment 14

This memory segment is reserved in the TC1798.

Segment 15

This memory segment allows accesses to all SFRs, CSFRs, the PCP memories and the MLI transfer windows.

Access from DMA Move Engines, Cerberus and MLI to the lower 128 MB of this segment are processed by the DMA FPI master interface on the SPB Bus, to the upper 128 MB of this segment by the DMA SRI master interface on the SRI Bus.

9.4 Address Map of the On Chip Bus System

This chapter describes the system address map as it is seen from the SRI and SPB bus masters PMI, DMI, PCP, DMA, SDMA, SHE, MLI and Cerberus.

9.4.1 Segments 0 to 14

Table 9-2 shows the address map of segments 0 to 14.

Table 9-2 On Chip Bus Address Map of Segment 0 to 14

Segment	Address Range	Size	Description	Access Type	
				Read[1]	Write[2]
0-7	$0000\ 0000_H$ - $0000\ 0007_H$	8 byte	Reserved (virtual address space)	SPBBE	SPBBE
	$0000\ 0008_H$ - $7FFF\ FFFF_H$	8×256 Mbyte		SPBBE	SPBBE
8	$8000\ 0000_H$ - $801F\ FFFF_H$	2 Mbyte	Program Flash 0 (PFLASH0)	access	access[2]
	$8020\ 0000_H$ - $803F\ FFFF_H$	2 Mbyte	Reserved	SRIBE	SRIBE
	$8040\ 0000_H$ - $807F\ FFFF_H$	-	Reserved	SRIBE & SPBBE	SRIBE
	$8080\ 0000_H$ - $809F\ FFFF_H$	2 Mbyte	Program Flash 1 (PFLASH1)	access	access[2]
	$80A0\ 0000_H$ - $80FF\ FFFF_H$	-	Reserved	SRIBE	SRIBE
	$8100\ 0000_H$ - $82FF\ FFFF_H$	-	Reserved	SRIBE	SRIBE
	$8300\ 0000_H$ - $8EFF\ FFFF_H$	192 Mbyte	External EBU Space	access	access
	$8F00\ 0000_H$ - $8F1F\ FFFF_H$	-	Reserved	SRIBE	SRIBE
	$8F20\ 0000_H$ - $8FE6\ FFFF_H$	-	Reserved	SRIBE	SRIBE
	$8FE7\ 0000_H$ - $8FE7\ 7FFF_H$	32 Kbyte	Online Data Acquisition (OLDA)	SRIBE	access[3] / SRIBE
	$8FE7\ 8000_H$ - $8FFF\ BFFF_H$	-	Reserved	SRIBE	SRIBE

Table 9-2 On Chip Bus Address Map of Segment 0 to 14 (cont'd)

Segment	Address Range	Size	Description	Access Type	
				Read[1)]	Write[2)]
	$8FFF\ C000_H$ - $8FFF\ FFFF_H$	16 Kbyte	Boot ROM (BROM)	access	SRIBE
9	$9000\ 0000_H$ - $9001\ FFFF_H$	128 Kbyte	LMU SRAM	access	access
	$9002\ 0000_H$ - $9EFF\ FFFF_H$	-	Reserved	SRIBE	SRIBE
	$9F00\ 0000_H$ - $9F0B\ FFFF_H$	768 Kbyte	Reserved for TC1798 Emulation Device Memory (EMEM)	SRIBE	SRIBE
	$9F0C\ 0000_H$ - $9FFF\ FFFF_H$	-	Reserved	SRIBE	SRIBE
10	$A000\ 0000_H$ - $A01F\ FFFF_H$	2 Mbyte	Program Flash 0 (PFLASH0)	access	access[2)]
	$A020\ 0000_H$ - $A03F\ FFFF_H$	-	Reserved	SRIBE	SRIBE
	$A040\ 0000_H$ - $A07F\ FFFF_H$	-	Reserved	SRIBE	SRIBE
	$A080\ 0000_H$ - $A09F\ FFFF_H$	2 Mbyte	Program Flash 1 (PFLASH1)	access	access[2)]
	$A0A0\ 0000_H$ - $A0FF\ FFFF_H$	-	Reserved	SRIBE	SRIBE
	$A100\ 0000_H$ - $A2FF\ FFFF_H$	-	Reserved	SRIBE	SRIBE
	$A300\ 0000_H$ - $AEFF\ FFFF_H$	192 Mbyte	External EBU Space	access	access
	$AF00\ 0000_H$ - $AF01\ 7FFF_H$	96 Kbyte	Data Flash (DFLASH) Bank 0	access	access[2)]
	$AF01\ 8000_H$ - $AF07\ FFFF_H$	-	Reserved	SRIBE	SRIBE
	$AF08\ 0000_H$ - $AF09\ 7FFF_H$	96 Kbyte	Data Flash (DFLASH) Bank 1	access	access[2)]
	$AF09\ 8000_H$ - $AF0F\ FFFF_H$	-	Reserved	SRIBE	SRIBE

Table 9-2 On Chip Bus Address Map of Segment 0 to 14 (cont'd)

Segment	Address Range	Size	Description	Access Type	
				Read[1]	Write[2]
	AF10 0000$_H$ - AF1F FFFF$_H$	~ 1 MByte	Reserved	SRIBE	SRIBE
	AF20 0000$_H$ - AF20 1FFF$_H$	-	Reserved	SRIBE	access[2]SRIBE
	AF20 2000$_H$ - AF20 3FFF$_H$	-	Reserved	SRIBE	SRIBE
	AF20 4000$_H$ - AF2F FFFF$_H$	-	Reserved	SRIBE	SRIBE
	AF30 0000$_H$ - AFE6 FFFF$_H$	-	Reserved	SRIBE	SRIBE
	AFE7 0000$_H$ - AFE7 7FFF$_H$	32 Kbyte	Online Data Acquisition (OLDA)	SRIBE	access[3] / SRIBE
	AFE7 8000$_H$ - AFFF BFFF$_H$	-	Reserved	SRIBE	SRIBE
	AFFF C000$_H$ - AFFF FFFF$_H$	16 Kbyte	Boot ROM (BROM)	access	SRIBE
11	B000 0000$_H$ - B001 FFFF$_H$	128 Kbyte	LMU SRAM	access	access
	B002 0000$_H$ - BEFF FFFF$_H$	-	Reserved	SRIBE	SRIBE
	BF00 0000$_H$ - BF0B FFFF$_H$	768 Kbyte	Reserved for TC1798 Emulation Device Memory (EMEM)	SRIBE	SRIBE
	BF0C 0000$_H$ - BFFF FFFF$_H$	-	Reserved	SRIBE	SRIBE
12	C000 0000$_H$ - C000 7FFF$_H$	32 Kbyte	Program Scratch-Pad SRAM (PSPR)	access	access
	C000 8000$_H$ - C01F FFFF$_H$	-	Reserved	SRIBE	SRIBE
	C020 0000$_H$ - C020 3FFF$_H$	16 Kbyte	Program Cache SRAM (ICACHE)	access[4] / SRIBE	access[4] / SRIBE
	C020 4000$_H$ - C02F FFFF$_H$	-	Reserved	SRIBE	SRIBE

Table 9-2 On Chip Bus Address Map of Segment 0 to 14 (cont'd)

Segment	Address Range	Size	Description	Access Type	
				Read[1]	Write[2]
	$C030\ 0000_H$ - $C030\ 01FF_H$	0.5 Kbyte	Program Cache TAG SRAM[5] (PTAG)	access[4] / SRIBE	access[4] / SRIBE
	$C030\ 0200_H$ - $C7FF\ FFFF_H$	-	Reserved	SRIBE	SRIBE
	$C800\ 0000_H$ - $C800\ 7FFF_H$	32 Kbyte	Program Scratch-Pad SRAM (PSPR)	access	access
	$C800\ 8000_H$ - $C81F\ FFFF_H$	-	Reserved	SRIBE	SRIBE
	$C820\ 0000_H$ - $C820\ 3FFF_H$	16 Kbyte	Program Cache SRAM (ICACHE)	access[4] / SRIBE	access[4] / SRIBE
	$C820\ 4000_H$ - $C82F\ FFFF_H$	-	Reserved	SRIBE	SRIBE
	$C830\ 0000_H$ - $C830\ 01FF_H$	0.5 Kbyte	Program Cache TAG SRAM[5] (PTAG)	access[4] / SRIBE	access[4] / SRIBE
	$C830\ 0200_H$ - $CFFF\ FFFF_H$	-	Reserved	SRIBE	SRIBE
13	$D000\ 0000_H$ - $D001\ FFFF_H$	128 Kbyte	Data Scratch-Pad SRAM (DSPR)	access	access
	$D002\ 0000_H$ - $D01F\ FFFF_H$	-	Reserved	SRIBE	SRIBE
	$D020\ 0000_H$ - $D020\ 3FFF_H$	16 Kbyte	Data Cache SRAM (DCACHE)	access[4] / SRIBE	access[4] / SRIBE
	$D020\ 4000_H$ - $D02F\ FFFF_H$	-	Reserved	SRIBE	SRIBE
	$D030\ 0000_H$ - $D030\ 01FF_H$	0.5 Kbyte	Data Cache TAG SRAM[5] (DTAG)	access[4] / SRIBE	access[4] / SRIBE
	$D030\ 0200_H$ - $D7FF\ FFFF_H$	-	Reserved	SRIBE	SRIBE
	$D040\ 0000_H$ - $D7FF\ FFFF_H$	-	Reserved	SRIBE	SRIBE
	$D800\ 0000_H$ - $D801\ FFFF_H$	128 Kbyte	Data Scratch-Pad SRAM (DSPR)	access	access

Table 9-2 On Chip Bus Address Map of Segment 0 to 14 (cont'd)

Segment	Address Range	Size	Description	Access Type	
				Read[1]	Write[2]
	$D802\ 0000_H$ - $D81F\ FFFF_H$	-	Reserved	SRIBE	SRIBE
	$D820\ 0000_H$ - $D820\ 3FFF_H$	16 Kbyte	Data Cache SRAM (DCACHE)	access[4]	access[4]
	$D820\ 4000_H$ - $D82F\ FFFF_H$	-	Reserved	SRIBE	SRIBE
	$D830\ 0000_H$ - $D830\ 01FF_H$	0.5 Kbyte	Data Cache TAG SRAM[5] (DTAG)	access[4]	access[4]
	$D830\ 0000_H$ - $DFFF\ FFFF_H$	-	Reserved	SRIBE	SRIBE
14	$E000\ 0000_H$ - $EFFF\ FFFF_H$	-	Reserved	SRIBE	SRIBE
15	$F000\ 0000_H$ - $FFFF\ FFFF_H$	256 Mbyte	see **Table 9-3**		

1) A read transaction through the SRI to FPI bridge that is terminated with Bus Error will result in Bus Errors on SRI and FPI (valid for transactions from FPI to SRI and SRI to FPI)

2) Write access to Flash resources are handled by the PMU module (Flash command sequence, see PMU chapter for details)

3) Online Data Acquisition address space can be disabled/enabled via PMU control register bit LMU_MEMCON.OLDAEN. CPU access to OLDA address space via segment 8 (cached) results in SRIBE independent of the LMU_MEMCON.OLDAEN bit setting.

4) ICache/DCache SRAMs (and the corresponding TAG SRAMs) can be only accessed when mapped into the address space (ICache / DCache disabled, see CPU chapter for details)via 32 bit access and only with 64 bit aligned address.

5) TAG SRAMs are not meant to be used as general SRAMS and can be accessed only with single data access and only with 64 bit aligned address. Mapping of TAG SRAMs in the address map can be used as additional option for memory testing.

9.4.2 Segment 15

Table 9-3 shows the address map of segment 15 as seen from the SRI and SPB bus masters PMI, DMI, PCP, SHE, DMA, SDMA and OCDS.

Please note that Table 9-3 describes the mapping of modules to segment F. The details of the module address ranges can be found in the module chapters register overview.

Table 9-3 On Chip Bus Address Map of Segment 15

Unit	Address Range	Size	Access Type	
			Read	Write
Reserved	$F000\ 0000_H$ - $F000\ 00FF_H$	–	SPBBE	SPBBE
System Peripheral Bus Control Unit (SBCU)	$F000\ 0100_H$ - $F000\ 01FF_H$	256 byte	access	access
System Timer (STM)	$F000\ 0200_H$ - $F000\ 02FF_H$	256 byte	access	access
Reserved	$F000\ 0300_H$ - $F000\ 03FF_H$	–	SPBBE	SPBBE
On-Chip Debug Support (Cerberus)	$F000\ 0400_H$ - $F000\ 04FF_H$	256 byte	access	access
System Control Unit (SCU) and Watchdog Timer (WDT)	$F000\ 0500_H$ - $F000\ 06FF_H$	2×256 byte	access	access
Reserved	$F000\ 0700_H$ - $F000\ 07FF_H$	–	SPBBE	SPBBE
MicroSecond Bus Controller 0 (MSC0)	$F000\ 0800_H$ - $F000\ 08FF_H$	256 byte	access	access
MicroSecond Bus Controller 1 (MSC1)	$F000\ 0900_H$ - $F000\ 09FF_H$	256 byte	access	access
Async./Sync. Serial Interface 0 (ASC0)	$F000\ 0A00_H$ - $F000\ 0AFF_H$	256 byte	access	access
Async./Sync. Serial Interface 1 (ASC1)	$F000\ 0B00_H$ - $F000\ 0BFF_H$	256 byte	access	access
Port 0	$F000\ 0C00_H$ - $F000\ 0CFF_H$	256 byte	access	access
Port 1	$F000\ 0D00_H$ - $F000\ 0DFF_H$	256 byte	access	access
Port 2	$F000\ 0E00_H$ - $F000\ 0EFF_H$	256 byte	access	access

Table 9-3 On Chip Bus Address Map of Segment 15 (cont'd)

Unit	Address Range	Size	Access Type	
			Read	Write
Port 3	$F000\ 0F00_H$ - $F000\ 0FFF_H$	256 byte	access	access
Port 4	$F000\ 1000_H$ - $F000\ 10FF_H$	256 byte	access	access
Port 5	$F000\ 1100_H$ - $F000\ 11FF_H$	256 byte	access	access
Port 6	$F000\ 1200_H$ - $F000\ 12FF_H$	256 byte	access	access
Port 7	$F000\ 1300_H$ - $F000\ 13FF_H$	256 byte	access	access
Port 8	$F000\ 1400_H$ - $F000\ 14FF_H$	256 byte	access	access
Port 9	$F000\ 1500_H$ - $F000\ 15FF_H$	256 byte	access	access
Port 10	$F000\ 1600_H$ - $F000\ 16FF_H$	256 byte	access	access
Port 11	$F000\ 1700_H$ - $F000\ 17FF_H$	256 byte	access	access
General Purpose Timer Array (GPTA0)	$F000\ 1800_H$ - $F000\ 1FFF_H$	8×256 byte	access	access
General Purpose Timer Array (GPTA1)	$F000\ 2000_H$ - $F000\ 27FF_H$	8×256 byte	access	access
Local Timer Cell Array (LTCA2)	$F000\ 2800_H$ - $F000\ 2FFF_H$	8×256 byte	access	access
Capture/Compare Unit 6 0 (CCU60)	$F000\ 3000_H$ - $F000\ 30FF_H$	256 byte	access	access
Capture/Compare Unit 6 1 (CCU61)	$F000\ 3100_H$ - $F000\ 31FF_H$	256 byte	access	access
Capture/Compare Unit 6 2 (CCU62)	$F000\ 3200_H$ - $F000\ 32FF_H$	256 byte	access	access
Capture/Compare Unit 6 3 (CCU63)	$F000\ 3300_H$ - $F000\ 33FF_H$	256 byte	access	access

Table 9-3 On Chip Bus Address Map of Segment 15 (cont'd)

Unit		Address Range	Size	Access Type	
				Read	Write
General Purpose Timer 12 0 (GPT120)		$F000\ 3400_H$ - $F000\ 34FF_H$	256 byte	access	access
General Purpose Timer 12 1 (GPT121)		$F000\ 3500_H$ - $F000\ 35FF_H$	256 byte	access	access
Reserved		$F000\ 3600_H$ - $F000\ 37FF_H$	–	SPBBE	SPBBE
Safety Direct Memory Access Controller (SDMA)		$F000\ 3800_H$ - $F000\ 3AFF_H$	3×256 byte	access	access
Reserved		$F000\ 3B00_H$ - $F000\ 3BFF_H$	–	SPBBE	SPBBE
Direct Memory Access Controller (DMA)		$F000\ 3C00_H$ - $F000\ 3EFF_H$	3×256 byte	access	access
Reserved		$F000\ 3F00_H$ - $F000\ 3FFF_H$	–	SPBBE	SPBBE
MultiCAN Controller (CAN)		$F000\ 4000_H$ - $F000\ 7FFF_H$	16 Kbyte	access	access
Reserved		$F000\ 8000_H$ - $F000\ FFFF_H$	–	SPBBE	SPBBE
FlexRay™ Protocol Controller (E-Ray)		$F001\ 0000_H$ - $F001\ 7FFF_H$	32 Kbyte	access	access
Reserved		$F001\ 8000_H$ - $F003\ FFFF_H$	–	SPBBE	SPBBE
PCP	Reserved	$F004\ 0000_H$ - $F004\ 3EFF_H$	–	SPBBE	SPBBE
	PCP Registers	$F004\ 3F00_H$ - $F004\ 3FFF_H$	256 byte	access	access
	Reserved	$F004\ 4000_H$ - $F004\ FFFF_H$	–	SPBBE	SPBBE
	PCP Data Memory (PRAM)	$F005\ 0000_H$ - $F005\ 3FFF_H$	16 Kbyte	nE, 32	nE, 32
	Reserved	$F005\ 4000_H$ - $F005\ FFFF_H$	–	SPBBE	SPBBE

Table 9-3 On Chip Bus Address Map of Segment 15 (cont'd)

Unit	Address Range	Size	Access Type	
			Read	Write
PCP Code Memory (CMEM)	$F006\ 0000_H$ - $F006\ 7FFF_H$	32 Kbyte	nE, 32	nE, 32
Reserved	$F006\ 8000_H$ - $F007\ FFFF_H$	–	SPBBE	SPBBE
Reserved	$F008\ 0000_H$ - $F010\ 03FF_H$	–	SPBBE	SPBBE
Fast Analog-to-Digital Converter (FADC)	$F010\ 0400_H$ - $F010\ 04FF_H$	256 byte	access	access
Reserved	$F010\ 0500_H$ - $F010\ 0FFF_H$	–	SPBBE	SPBBE
Analog-to-Digital Converter 0 (ADC0)	$F010\ 1000_H$ - $F010\ 13FF_H$	4 × 256 byte	access	access
Analog-to-Digital Converter 1 (ADC1)	$F010\ 1400_H$ - $F010\ 17FF_H$	4 × 256 byte	access	access
Analog-to-Digital Converter 2 (ADC2)	$F010\ 1800_H$ - $F010\ 1BFF_H$	4 × 256 byte	access	access
Analog-to-Digital Converter 3 (ADC3)	$F010\ 1C00_H$ - $F010\ 1FFF_H$	4 × 256 byte	access	access
Reserved	$F010\ 2000_H$ - $F010\ BFFF_H$	–	SPBBE	SPBBE
Micro Link Interface 0 (MLI0)	$F010\ C000_H$ - $F010\ C0FF_H$	256 byte	access	access
Micro Link Interface 1 (MLI1)	$F010\ C100_H$ - $F010\ C1FF_H$	256 byte	access	access
Memory Checker (MCHK)	$F010\ C200_H$ - $F010\ C2FF_H$	256 byte	access	access
Reserved	$F010\ C300_H$ - $F01D\ FFFF_H$	–	SPBBE	SPBBE
MLI0 Small Transfer Windows	$F01E\ 0000_H$ - $F01E\ 7FFF_H$	4 × 8 Kbyte	access	access
MLI1 Small Transfer Windows	$F01E\ 8000_H$ - $F01E\ FFFF_H$	4 × 8 Kbyte	access	access

Table 9-3 On Chip Bus Address Map of Segment 15 (cont'd)

Unit	Address Range	Size	Access Type	
			Read	Write
Reserved	$F01F\ 0000_H$ - $F01F\ FFFF_H$	–	SPBBE	SPBBE
MLI0 Large Transfer Windows	$F020\ 0000_H$ - $F023FFFF_H$	4 × 64 Kbyte	access	access
MLI1 Large Transfer Windows	$F024\ 0000_H$ - $F027\ FFFF_H$	4 × 64 Kbyte	access	access
Reserved	$F028\ 0000_H$ - $F02F\ FFFF_H$	–	SPBBE	SPBBE
Port 12	$F030\ 0000_H$ - $F030\ 00FF_H$	256 byte	access	access
Port 13	$F030\ 0100_H$ - $F030\ 01FF_H$	256 byte	access	access
Port 14	$F030\ 0200_H$ - $F030\ 02FF_H$	256 byte	access	access
Port 15	$F030\ 0300_H$ - $F030\ 03FF_H$	256 byte	access	access
Port 16	$F030\ 0400_H$ - $F030\ 04FF_H$	256 byte	access	access
Port 17	$F030\ 0500_H$ - $F030\ 05FF_H$	256 byte	access	access
Port 18	$F030\ 0600_H$ - $F030\ 06FF_H$	256 byte	access	access
Reserved	$F030\ 0700_H$ - $F030\ FFFF_H$	–	SPBBE	SPBBE
Synchronous Serial Interface 0 (SSC0)	$F031\ 0000_H$ - $F031\ 00FF_H$	256 byte	access	access
Synchronous Serial Interface 1 (SSC1)	$F031\ 0100_H$ - $F031\ 01FF_H$	256 byte	access	access
Synchronous Serial Interface 2 (SSC2)	$F031\ 0200_H$ - $F031\ 02FF_H$	256 byte	access	access
Synchronous Serial Interface 3 (SSC3)	$F031\ 0300_H$ - $F031\ 03FF_H$	256 byte	access	access

Table 9-3 On Chip Bus Address Map of Segment 15 (cont'd)

Unit	Address Range	Size	Access Type	
			Read	Write
Reserved	$F031\ 0400_H$ - $F031\ 07FF_H$	–	SPBBE	SPBBE
Guardian for SSC0 (SSCG0)	$F031\ 0800_H$ - $F031\ 09FF_H$	2x256 byte	access	access
Guardian for SSC1 (SSCG1)	$F031\ 0A00_H$ - $F031\ 0BFF_H$	2x256 byte	access	access
Guardian for SSC2 (SSCG2)	$F031\ 0C00_H$ - $F031\ 0DFF_H$	2x256 byte	access	access
Guardian for SSC3 (SSCG3)	$F031\ 0E00_H$ - $F031\ 0FFF_H$	2x256 byte	access	access
Reserved	$F031\ 1000_H$ - $F031\ FFFF_H$	–	SPBBE	SPBBE
Flexible CRC Engine (FCE)	$F032\ 0000_H$ - $F032\ 00FF_H$	256 byte	access	access
Reserved	$F032\ 0100_H$ - $F032\ 01FF_H$	–	SPBBE	SPBBE
Secure Hardware Extension (SHE)	$F032\ 0200_H$ - $F032\ 02FF_H$	256 byte	access	access
Reserved	$F032\ 0300_H$ - $F032\ 0FFF_H$	–	SPBBE	SPBBE
SENT Module (SENT)	$F032\ 1000_H$ - $F032\ 19FF_H$	10x256 byte	access	access
Reserved	$F032\ 1A00_H$ - $F032\ 2FFF_H$	–	SPBBE	SPBBE
Bus Monitor Unit Registers (BMU)	$F032\ 3000_H$ - $F032\ 31FF_H$	2x256 byte	access	access
Reserved	$F032\ 3200_H$ - $F032\ 3FFF_H$	–	SPBBE	SPBBE
Bus Monitor Unit Memory (BMURAM)	$F032\ 4000_H$ - $F032\ 5FFF_H$	8 Kbyte	access	access
Reserved	$F032\ 6000_H$ - $F7E0\ FEFF_H$	–	SPBBE	SPBBE

Table 9-3 On Chip Bus Address Map of Segment 15 (cont'd)

Unit		Address Range	Size	Access Type	
				Read	Write
CPU	CPU Slave Interface Registers (CPS)	$F7E0\ FF00_H$ - $F7E0\ FFFF_H$	256 byte	access	access
	CPU Core SFRs & GPRs	$F7E1\ 0000_H$ - $F7E1\ FFFF_H$	64 Kbyte	access	access
Reserved		$F7E2\ 0000_H$ - $F7FF\ FFFF_H$	–	SPBBE	SPBBE
External Bus Unit (EBU)		$F800\ 0000_H$ - $F800\ 03FF_H$	1 Kbyte	access	access
Reserved		$F800\ 0400_H$ - $F800\ 04FF_H$	–	SRIBE & SPBBE	SRIBE
Program Memory Unit 0 (PMU0)		$F800\ 0500_H$ - $F800\ 05FF_H$	256 byte	access	access
Program Memory Unit 1 (PMU1)		$F800\ 0600_H$ - $F800\ 06FF_H$	256 byte	access	access
Reserved		$F800\ 0700_H$ - $F800\ 0FFF_H$	–	SRIBE & SPBBE	SRIBE
Flash Register (PMU0)		$F800\ 1000_H$ - $F800\ 23FF_H$	5 Kbyte	access	access
Reserved		$F800\ 2400_H$ - $F800\ 2FFF_H$	–	SRIBE & SPBBE	SRIBE
Flash Register PMU1		$F800\ 3000_H$ - $F800\ 43FF_H$	5 Kbyte	access	access
Reserved		$F800\ 4400_H$ - $F801\ 00FF_H$	–	SRIBE & SPBBE	SRIBE
Reserved		$F801\ 0100_H$ - $F86F\ FFFF_H$	–	SRIBE & SPBBE	SRIBE
SRI Crossbar (XBar_SRI)		$F870\ 0000_H$ - $F870\ 04FF_H$	5x256 byte	access	access
Reserved		$F870\ 0500_H$ - $F870\ 07FF_H$	–	SRIBE & SPBBE	SRIBE
Local Memory Unit (LMU)		$F870\ 0800_H$ - $F870\ 08FF_H$	256 byte	access	access

Table 9-3 On Chip Bus Address Map of Segment 15 (cont'd)

Unit	Address Range	Size	Access Type	
			Read	Write
Reserved	$F870\ 0900_H$ - $F87F\ FAFF_H$	–	SRIBE & SPBBE	SRIBE
Overlay Control Unit (OVC)	$F87F\ FB00_H$ - $F87F\ FBFF_H$	256 byte	access	access
Reserved	$F87F\ FC00_H$ - $FFFF\ FFFF_H$	–	SRIBE & SPBBE	SRIBE

9.5 Memory Module Access Restrictions

Table 9-4 describes which type of accesses are possible to the different memories in the TC1798.

Table 9-4 Possible Memory Accesses[1)]

Memory		Bit	Byte		Half-word		Word		Double-word	
		rmw	r	w	r	w	r	w	r	w
PMI[2)]	PSPR	y	y	y	y	y	y	y	y	y
	PTAG[3)]	-	-	-	-	-	y	y	-	y
	PCACHE	y	y	y	y	y	y	y	y	y
DMI[2)]	DSPR	y	y	y	y	y	y	y	y	y
	DTAG[3)]	-	-	-	-	-	y	y	-	-
	DCACHE	y	y	y	y	y	y	y	y	y
LMU[2)]	LMURAM	y	y	y	y	y	y	y	y	y
PMU	BROM	–	y	–	y	–	y	–	y	–
	PFLASH	–	y	–	y	–	y	y	y	y
	DFLASH	–	y	–	y	–	y	y	y	y
PCP[4)]	CMEM	y	–	–	–	–	y	y	y	y
	PRAM	y	–	–	–	–	y	y	y	y
BMU[4)]	BMURAM	–	–	–	–	–	y	y	y	y

1) ´y´ means: supported. ´-´ means: not supported

2) The module also supports SRI 2-Word and 4-Word Block read and write accesses.

3) TAG SRAMs are not meant to be used as general SRAMS and can be accessed only via 32 bit single data access and only with 64 bit aligned address. Mapping of TAG SRAMs in the address map can be used as additional option for memory testing.

4) The module also supports FPI/SPB 4-Word and 8-Word Block read and write accesses.

9.6 Side Effects from Modules to Data Scratch Pad SRAM (DSPR)

Please note that the DSPR is also used by Boot routine and can be used by the CPU for system tasks:

- the Boot routine copies some devices informations during the startup into the DSPR (see chapter ´BootROM Content´)
- DSPR can be used as context save area (for details see chapter ´CPU Subsystem´)

10 General Purpose I/O Ports and Peripheral I/O Lines (Ports)

The TC1798 has 252 digital General Purpose Input/Output (GPIO) port lines which are connected to the on-chip peripheral units. They are divided into:

Table 10-1 Ports Overview

Port	Pins	Base Address	End Address	Note
P0	16	F000 0C00$_H$	F000 0CFF$_H$	+hwcfg, +E-Ray, EMSTOP, CCU6/GPT12
P1	16	F000 0D00$_H$	F000 0DFF$_H$	EMSTOP, CCU6/GPT12
P2	14	F000 0E00$_H$	F000 0EFF$_H$	EMSTOP, CCU6/GPT12
P3	16	F000 0F00$_H$	F000 0FFF$_H$	EMSTOP, CCU6/GPT12
P4	16	F000 1000$_H$	F000 10FF$_H$	EMSTOP, SSC2, CCU6/GPT12
P5	16	F000 1100$_H$	F000 11FF$_H$	extended with LVDS, EMSTOP, CCU6/GPT12
P6	12	F000 1200$_H$	F000 12FF$_H$	6.4 to 6.15, CCU6/GPT12
P7	8	F000 1300$_H$	F000 13FF$_H$	SSC3
P8	8	F000 1400$_H$	F000 14FF$_H$	EMSTOP, SENT, CCU6/GPT12
P9	9 -> 15	F000 1500$_H$	F000 15FF$_H$	EMSTOP only 6 added. no change to the old ones. $\overline{\text{BRKIN}}$, $\overline{\text{BRKOUT}}$. SENT, TTCAN, CCU6/GPT12
P10	4 -> 6	F000 1600$_H$	F000 16FF$_H$	fully changed, - EBU
P11	16	F000 1700$_H$	F000 17FF$_H$	-
P12	8	F030 0000$_H$	F030 00FF$_H$	-
P13	16	F030 0100$_H$	F030 01FF$_H$	EMSTOP

Table 10-1 Ports Overview (cont'd)

Port	Pins	Base Address	End Address	Note
P14	16	$F030\ 0200_H$	$F030\ 02FF_H$	EMSTOP, CCU6/GPT12
P15	16	$F030\ 0300_H$	$F030\ 03FF_H$	CCU6/GPT12
P16	16	$F030\ 0400_H$	$F030\ 04FF_H$	DDR Burst Flash
P17	16	$F030\ 0500_H$	$F030\ 05FF_H$	Analog / digital SENT
P18	2	$F030\ 0600_H$	$F030\ 06FF_H$	SSC2

The External Bus Interface (EBU) has its own set of dedicated signal lines. Further details are described in the port-specific sections of this chapter.

10.1 Basic Port Operation

Figure 10-1 is a general block diagram of a TC1798 GPIO port slice.

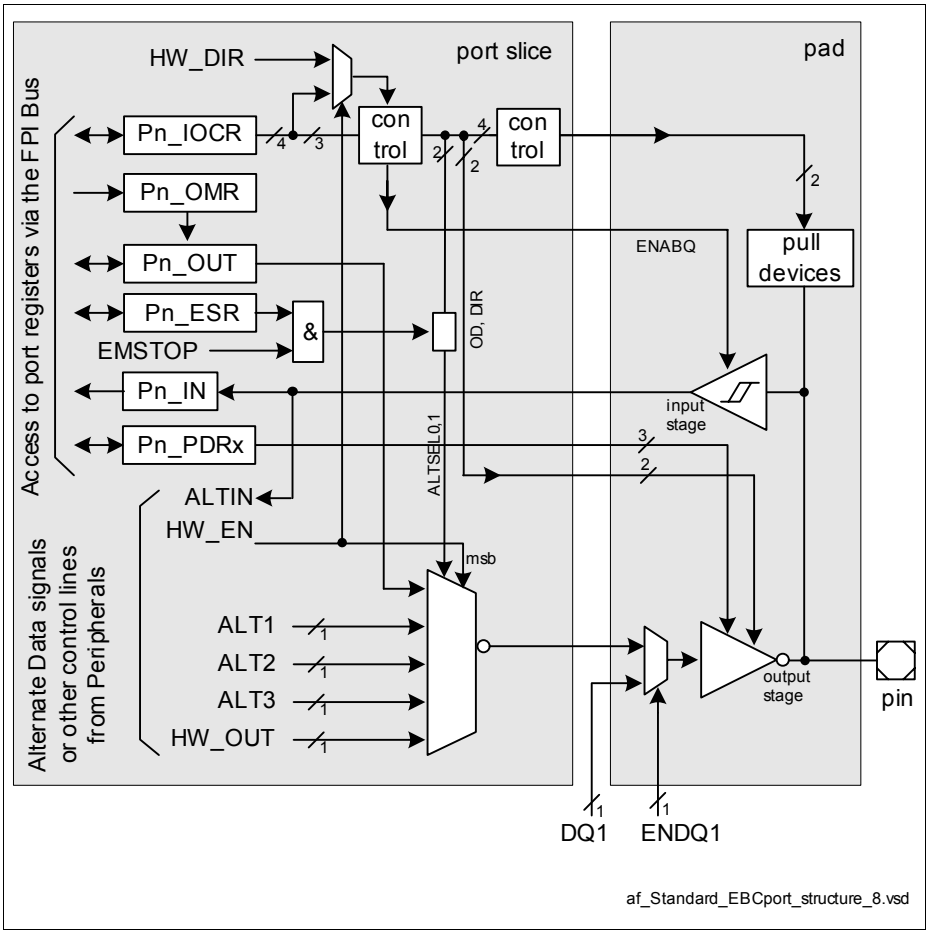


Figure 10-1 General Structure of a Port Pin

Each port line has a number of control and data bits, enabling very flexible usage of the line. Each port pin (except Port 10) can be configured for input or output operation. In input mode (default after reset), the output driver is switched off (high-impedance). The actual voltage level present at the port pin is translated into a logical 0 or 1 via a Schmitt-Trigger device and can be read via the read-only register Pn_IN. An input signal can also be connected directly to the various inputs of the peripheral units (AltDataIn). The

function of the input line from the pin to the input register Pn_IN and to AltDataIn is independent of whether the port pin operates as input or output. This means that when the port is in output mode, the level of the pin can be read by software via Pn_IN or a peripheral can use the pin level as an input.

In output mode, the output driver is activated and drives the value supplied through the multiplexer to the port pin. Switching between input and output mode is accomplished through the Pn_IOCR register, which enables or disables the output driver. If a peripheral unit uses a GPIO port line as a bi-directional I/O line, register Pn_IOCR has to be written for input or output selection. The Pn_IOCR register further controls the driver type of the output driver, and determines whether an internal weak pull-up or pull-down device is alternatively connected to the pin when used as an input. This offers additional advantages in an application.

The output multiplexer in front of the output driver selects the signal source for the GPIO line when used as output. If the pin is used as general-purpose output, the multiplexer is switched by software (Pn_IOCR register) to the Output Data Register Pn_OUT. Software can set or clear the bit in Pn_OUT, and therefore it can directly influence the state of the port pin. If the on-chip peripheral units use the pin for output signals, the alternate output lines ALT1 to ALT3 can be switched via the multiplexer to the output driver. The data written into the output register Pn_OUT by software can be used as input data to an on-chip peripheral. This enables, for example, peripheral tests via software without external circuitry.

When selected as general-purpose output line, the logic state of each port pin can be changed individually by programming the pin-related bits in the Output Modification Register Pn_OMR. The bits in Pn_OMR make it possible to set, reset, toggle, or leave the bits in the Pn_OUT register unchanged.

When selected as general-purpose output line, the actual logic level at the pin can be examined through reading Pn_IN and compared against the applied output level (either applied through software via the output register Pn_OUT, or via an alternate output function of a peripheral unit). This can be used to detect some electrical failures at the pin caused through external circuitry. In addition, software-supported arbitration schemes can be implemented in this way using the open-drain configuration and an external wired-And circuitry. Collisions on the external communication lines can be detected when a high level (1) is output, but a low level (0) is seen when reading the pin value via the input register Pn_IN.

All GPIO lines of the TC1798 that are used by the GPTA modules (GPTA0, GPTA1, LTCA2) have an emergency stop logic. This logic makes it possible to individually disconnect GPTA outputs from the driving GPTA module outputs and to put them onto a well defined logic state in an emergency case. In en emergency case, the content of the port output register Pn_OUT is driven at the output pin instead of the GPTA module output. The Emergency Stop Register Pn_EMR determines whether a GPTA output is enabled or disabled in an emergency case.

10.2 Description Scheme for the Port IO Functions

The following two general building block can be used to describe each GPIO pin:

Table 10-2 Port x Input/Output Functions

Port Pin	I/O	Select	Connected Signal(s)	From / to Module
Px.y	Input		Signal(s)	module(s)
	Output	GPIO	Signal	module
		ALT1	Signal	module
		ALT2	Signal	module
		ALT3	Signal	module
	HW_DIR	HW_Out	Signal	module; group En

or:

Table 10-3 Port x Functions

Port Pin	I/O	Pin Functionality	Associated Reg./ I/O Line	Port I/O Control Select.	
				Reg./Bit Field	Value
Px.y	I	GPIOt	Px_IN.Py	Px_IOCRz. PC0	$0XXX_B$
	O	GPIO	Px_OUT.Py		$1X00_B$
					$1X01_B$
					$1X10_B$
					$1X11_B$
	HW_DIR	module; group En	Signal		HW_DIR

- HW_DIR:
  The type Alternate Direction signal which is needed if HW_En is active:
  – Out -always output
    DIRx - the pins in one port having the same DIRx (x=0, 1, 2, ...), are controlled as a group by a dedicated HW_DIR signal.
    SDIR- Single DIR- the pin is controlled by its own, dedicated, single HW_DIR signal.
- grouping indicates if the respective pin is controlled by hardware:

  - ENx - the pins in one port having the same ENx (x=0, 1, 2, ...), are controlled as a group by a dedicated HW_EN signal.
  - SEN - Single EN - the pin is controlled by its own, dedicated, single HW_EN signal
- Digital port slices with HW_DIR defined are the ports described in **Figure 10-1**.

Note: HW_EN signal has higher priority then Emergency Stop. Emergency Stop is functional when the pins are set in the GPIO mode.

Note: HW_DIR signal, output case, switches the pad to push-pull output state.
HW_DIR signal, input case, switches the pad to the input state with pull-up/down setting as defined by the IOCR register.

10.3 Port Register Description

The individual control and data bits of each GPIO port are implemented in a number of registers. The registers are used to configure and use the port as general-purpose I/O or alternate function input/output. For some ports, not all registers are implemented. The availability of the registers in the specific ports is described in **Table 10-10** on **Page 10-28** up to **Table 10-28** on **Page 10-87**.

Note: All port-registers have control bits implemented in groups of four (a nibble), starting from the bit position 0. If a port is do not fit to multiple of four without rest, or starts with a bit number other than zero, then some control bits remain unused. These bits behave as standard read-write bits, but do not have any function. The registers of not implemented groups of bits starting on the position 0 are implemented, but do not have any function. For example, Port 6 contains control registers and bitfields for the first nibble P6.0 to P6.3, although there are no such pins physically implemented. The not implemented bits appear in the boundary-scan chain, although they do not have an external connection.

Port Register Overview

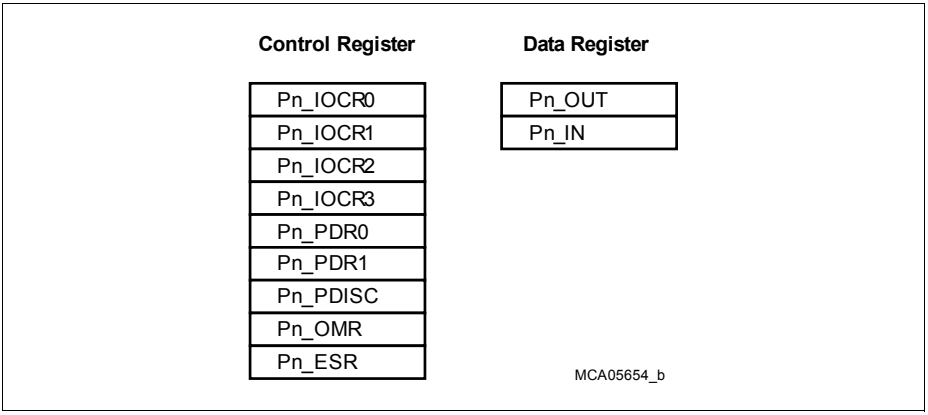


Figure 10-2 Port Registers

Table 10-4 Registers Address Space

Module	Base Address	End Address	Note
P0	F000 0C00$_H$	F000 0CFF$_H$	16
P1	F000 0D00$_H$	F000 0DFF$_H$	16
P2	F000 0E00$_H$	F000 0EFF$_H$	14
P3	F000 0F00$_H$	F000 0FFF$_H$	16

Table 10-4 Registers Address Space

Module	Base Address	End Address	Note
P4	$F000\ 1000_H$	$F000\ 10FF_H$	16
P5	$F000\ 1100_H$	$F000\ 11FF_H$	16
P6	$F000\ 1200_H$	$F000\ 12FF_H$	12
P7	$F000\ 1300_H$	$F000\ 13FF_H$	8
P8	$F000\ 1400_H$	$F000\ 14FF_H$	8
P9	$F000\ 1500_H$	$F000\ 15FF_H$	15
P10	$F000\ 1600_H$	$F000\ 16FF_H$	6
P11	$F000\ 1700_H$	$F000\ 17FF_H$	16
P12	$F030\ 0000_H$	$F030\ 00FF_H$	8
P13	$F030\ 0100_H$	$F030\ 01FF_H$	16
P14	$F030\ 0200_H$	$F030\ 02FF_H$	16
P15	$F030\ 0300_H$	$F030\ 03FF_H$	16
P16	$F030\ 0400_H$	$F030\ 04FF_H$	13
P17	$F030\ 0500_H$	$F030\ 05FF_H$	16
P18	$F030\ 0600_H$	$F030\ 06FF_H$	8

Table 10-5 Registers Overview

Register Short Name	Register Long Name	Offset Address	Access Mode		Desc. see
			Read	Write	
Pn_OUT	Port n Output Register	0000_H	U, SV	U, SV	Page 10-21
Pn_OMR	Port n Output Modification Register	0004_H	U, SV	U, SV	Page 10-22
–	Reserved	0008_H-$000C_H$	BE	BE	–
Pn_IOCR0	Port n Input/Output Control Register 0	0010_H	U, SV	U, SV	Page 10-11
Pn_IOCR4	Port n Input/Output Control Register 4	0014_H	U, SV	U, SV	Page 10-12

Table 10-5 Registers Overview (cont'd)

Register Short Name	Register Long Name	Offset Address	Access Mode		Desc. see
			Read	Write	
Pn_IOCR8	Port n Input/Output Control Register 8	0018_H	U, SV[1)]	U, SV[1)]	Page 10-13
Pn_IOCR12	Port n Input/Output Control Register 12	$001C_H$	U, SV[1)]	U, SV[1)]	Page 10-14
–	Reserved	0020_H	BE	BE	–
Pn_IN	Port n Input Register	0024_H	U, SV	U, SV	Page 10-25
–	Reserved	0028_H-$003C_H$	BE	BE	–
Pn_PDR0	Port n Pad Driver Mode 0 Register	0040_H	U, SV	SV, E	Page 10-18
Pn_PDR1	Port n Pad Driver Mode 1 Register	0044_H	U, SV[1)]	SV, E[1)]	Page 10-19
–	Reserved	0048_H-$004C_H$	BE	BE	–
Pn_ESR	Port n Emergency Stop Register	0050_H	U, SV[2)]	SV, E[2)]	Page 10-24
–	Reserved	0054_H-$005C_H$	BE	BE	–
Pn_PDISC	Port n Pin Function Decision Control Register	0060_H	U, SV	SV, E	Page 10-20
–	Reserved	0064_H-$00FC_H$	BE	BE	–

1) Applicable to n=0-6, 9, 11, 13-18. Otherwise, this location is reserved and returns "BE" upon read and write accesses.

2) Applicable to n=0-5, 8-9, 13-14. Otherwise, this location is reserved and returns "BE" upon read and write accesses.

Register Access Rights and Reset Class

Table 10-6 Registers Access Rights and Reset Classes

Register Short Name	Access Rights		Reset Class
	Read	Write	
Pn_OUT	U,SV	U,SV	Class 3
Pn_OMR			
Pn_IOCR0			
Pn_IOCR4			
Pn_IOCR8			
Pn_IOCR12			
Pn_IN			
Pn_PDISC		SV,E	
Pn_PDR0			
Pn_PDR1			
Pn_ESR			

10.3.1 Port Input/Output Control Registers

The port input/output control registers select the digital output and input driver functionality and characteristics of a GPIO port pin. Port direction (input or output), pull-up or pull-down devices for inputs, and push-pull or open-drain functionality for outputs can be selected by the corresponding bit fields PCx (x = 0-15). Each 32-bit wide port input/output control register controls four GPIO port lines:

Register Pn_IOCR0 controls the Pn.[3:0] port lines
Register Pn_IOCR4 controls the Pn.[7:4] port lines
Register Pn_IOCR8 controls the Pn.[11:8] port lines
Register Pn_IOCR12 controls the Pn.[15:12] port lines

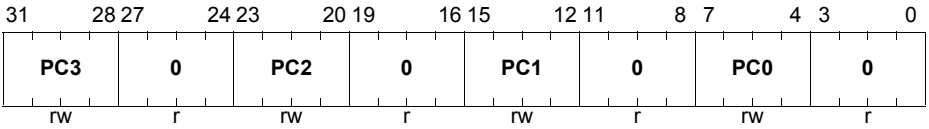
The diagrams below show the register layouts of the port input/output control registers with the PCx bit fields. One PCx bit field controls exactly one port line Pn.x.

Pn_IOCR0 (n=0-1)
Port n Input/Output Control Register 0
($F000\ 0C10_H + n*100_H$) **Reset Value: $2020\ 2020_H$**

Pn_IOCR0 (n=3-11)
Port n Input/Output Control Register 0
($F000\ 0C10_H + n*100_H$) **Reset Value: $2020\ 2020_H$**

Pn_IOCR0 (n=12-16)
Port n Input/Output Control Register 0
($F02F\ F410_H + n*100_H$) **Reset Value: $2020\ 2020_H$**

P18_IOCR0
Port 18 Input/Output Control Register 0
(10_H) **Reset Value: $2020\ 2020_H$**

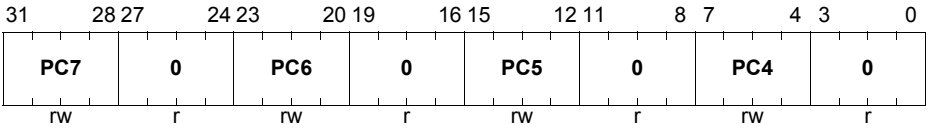


Field	Bits	Type	Description
PC0, PC1, PC2, PC3	[7:4], [15:12], [23:20], [31:28]	rw	**Port Control for Port n Pin 0 to 3** This bit field determines the Port n line x functionality (x = 0-3) according to the coding table (see **Table 10-7**).
0	[3:0], [11:8], [19:16], [27:24]	r	**Reserved** Read as 0; should be written with 0.

Pn_IOCR4 (n=0-11)
Port n Input/Output Control Register 4
(F000 0C14$_H$ + n*100$_H$) **Reset Value: 2020 2020$_H$**

Pn_IOCR4 (n=12-16)
Port n Input/Output Control Register 4
(F02F F414$_H$ + n*100$_H$) **Reset Value: 2020 2020$_H$**

P18_IOCR4
Port 18 Input/Output Control Register 4
(14$_H$) **Reset Value: 2020 2020$_H$**



Field	Bits	Type	Description
PC4, PC5, PC6, PC7	[7:4], [15:12], [23:20], [31:28]	rw	**Port Control for Port n Pin 4 to 7** This bit field determines the Port n line x functionality (x = 4-7) according to the coding table (see **Table 10-7**).
0	[3:0], [11:8], [19:16], [27:24]	r	**Reserved** Read as 0; should be written with 0.

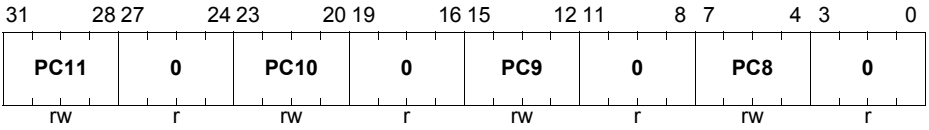
Pn_IOCR8 (n=0-6)
Port n Input/Output Control Register 8
(F000 0C18$_H$ + n*100$_H$) **Reset Value: 2020 2020$_H$**

P9_IOCR8
Port 9 Input/Output Control Register 8
(18$_H$) **Reset Value: 2020 2020$_H$**

P11_IOCR8
Port 11Input/Output Control Register 8
(18$_H$) **Reset Value: 2020 2020$_H$**

Pn_IOCR8 (n=13-15)
Port n Input/Output Control Register 8
(F02F F418$_H$ + n*100$_H$) **Reset Value: 2020 2020$_H$**

P16_IOCR8
Port 16 Input/Output Control Register 8
(18$_H$) **Reset Value: 2020 2020$_H$**

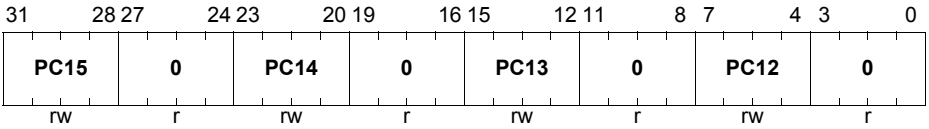


Field	Bits	Type	Description
PC8, PC9, PC10, PC11	[7:4], [15:12], [23:20], [31:28]	rw	**Port Control for Port n Pin 8 to 11** This bit field determines the Port n line x functionality (x = 8-11) according to the coding table (see **Table 10-7**).
0	[3:0], [11:8], [19:16], [27:24]	r	**Reserved** Read as 0; should be written with 0.

Pn_IOCR12 (n=0-6)
Port n Input/Output Control Register 12
(F000 0C1C$_H$ + n*100$_H$) **Reset Value: 2020 2020$_H$**

P11_IOCR12
Port 11 Input/Output Control Register 12
(1C$_H$) **Reset Value: 2020 2020$_H$**

Pn_IOCR12 (n=13-15)
Port n Input/Output Control Register 12
(F02F F41C$_H$ + n*100$_H$) **Reset Value: 2020 2020$_H$**



Field	Bits	Type	Description
PC12, PC13, PC14, PC15	[7:4], [15:12], [23:20], [31:28]	rw	**Port Control for Port n Pin 12 to 15** This bit field determines the Port n line x functionality (x = 12-15) according to the coding table (see Table 10-7).
0	[3:0], [11:8], [19:16], [27:24]	r	**Reserved** Read as 0; should be written with 0.

Depending on the GPIO port functionality (number of GPIO lines of a port), not all of the port input/output control registers are implemented.

The structure with one control bit field for each port pin located in different register bytes offers the possibility to configure the port pin functionality of a single pin with byte-oriented accesses without accessing the other PCx bit fields.

Port Control Coding

Table 10-7 describes the coding of the PCx bit fields that determine the port line functionality. Port 4 has a different PCx coding than the other ports (in input mode, no pull devices can be connected).

Table 10-7 PCx Coding

PCx[3:0]	I/O	Output Characteristics	Selected Pull-up / Pull-down / Selected Output Function
$0X00_B$	Input	–	No input pull device connected
$0X01_B$			Input pull-down device connected
$0X10_B$			Input pull-up device connected[1)]
$0X11_B$			No input pull device connected
1000_B	Output	Push-pull	General-purpose output
1001_B			Alternate output function 1
1010_B			Alternate output function 2
1011_B			Alternate output function 3
1100_B		Open-drain	General-purpose output
1101_B			Alternate output function 1
1110_B			Alternate output function 2
1111_B			Alternate output function 3

1) This is the default pull-up state after reset.

10.3.2 Pad Driver Mode Register

Overview

The pad structure of the TC1798 GPIO lines offers the possibility to select the output driver strength and the slew rate. These two parameters are controlled by the bit fields in the pad driver mode registers Pn_PDR0/1, independently from input/output and pull-up/pull-down control functionality as programmed in the Pn_IOCR register. Pn_PDR0 and Pn_PDR1 registers are assigned to each port.

The GPIO pads classes are:

- Class A1 pins (low speed 3.3V LVTTL outputs)
- Class A1+ pins (medium speed 3.3V LVTTL outputs)
- Class A2 pins (high speed 3.3V LVTTL outputs. e.g. for serial outputs)

The assignment of each port pin to one of these pad classes is shown in the port configuration figures. Further details about pad driver classes that are available in the TC1798 are summarized in the “Electrical Specification” chapter.

Depending on the assigned pad class, the 3-bit wide pad driver mode selection bit fields PDx in the pad driver mode registers Pn_PDR make it possible to select the port line functionality as shown in **Table 10-8**. Note that the pad driver mode registers are specific for each port. Therefore, the Pn_PDR layout is described for each port in the port-specific sections.

Class A1 pins make it possible to select between medium and weak output drivers. Class A1+ pins make it possible to select between strong/medium/weak output drivers. Class A2 pins make it possible to select between strong/medium/weak output drivers. Class B pins make it possible to select between strong/medium/weak output drivers, however class B pins with a PDx configured to an other value than 000_B have the behavior of class A2 pins. In the case of strong driver type, the signal transition edge can be additionally selected as sharp/medium/soft.

Table 10-8 Pad Driver Mode Selection

Pad Class	PDx.2	PDx.1	PDx.0	Functionality
A1	X	X	0	Medium driver
			1	Weak driver
A1+	0	X	0	Strong driver soft edge
	0	X	1	Strong driver slow edge
	1	X	0	Medium driver
	1	X	1	Weak driver

Table 10-8 Pad Driver Mode Selection (cont'd)

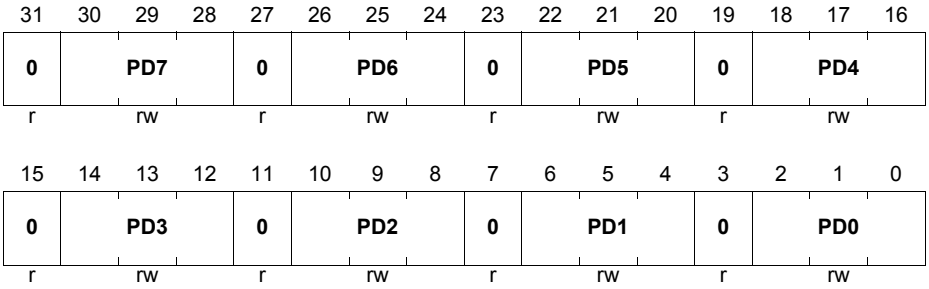
Pad Class	PDx.2	PDx.1	PDx.0	Functionality
A2 / B	0	0	0	Strong driver, sharp edge
	0	0	1	Strong driver, medium edge
	0	1	0	Strong driver, soft edge
	0	1	1	Strong driver, sharp - edge
	1	0	0	Medium driver
	1	0	1	Medium driver
	1	1	0	Strong driver, medium - edge
	1	1	1	Weak driver

Note: TC1798 Data Sheet describes the DC characteristics of all pad classes.

Pad Driver Mode Registers

This is the general description of the PDR registers. Each port contains its own specific PDR registers, described additionally at each port, that can contain between one and eight PDx fields for PDR0 and PDR1 registers, respectively. Each field controls 1 pin. For coding of PDx, see **Page 10-16**.

Pn_PDR0 (n=0-1)
Port n Pad Driver Mode 0 Register(F000 0C40$_H$+n*100$_H$) Reset Value: 0000 0000$_H$
Pn_PDR0 (n=3-5)
Port n Pad Driver Mode 0 Register(F000 0C40$_H$+n*100$_H$) Reset Value: 0000 0000$_H$
Pn_PDR0 (n=7-9)
Port n Pad Driver Mode 0 Register(F000 0C40$_H$+n*100$_H$) Reset Value: 0000 0000$_H$
P11_PDR0
Port 11 Pad Driver Mode 0 Register (40$_H$) Reset Value: 0000 0000$_H$
Pn_PDR0 (n=12-16)
Port n Pad Driver Mode 0 Register(F02F F440$_H$+n*100$_H$) Reset Value: 0000 0000$_H$
P18_PDR0
Port 18 Pad Driver Mode 0 Register (40$_H$) Reset Value: 0000 0000$_H$



Field	Bits	Type	Description
PD0	[2:0]	rw	**Pad Driver Mode for Pn.0**
PD1	[6:4]	rw	**Pad Driver Mode for Pn.1**
PD2	[10:8]	rw	**Pad Driver Mode for Pn.2**
PD3	[14:12]	rw	**Pad Driver Mode for Pn.3**
PD4	[18:16]	rw	**Pad Driver Mode for Pn.4**
PD5	[22:20]	rw	**Pad Driver Mode for Pn.5**
PD6	[26:24]	rw	**Pad Driver Mode for Pn.6**
PD7	[30:28]	rw	**Pad Driver Mode for Pn.7**
0	3, 7, 11, 15, 19, 23, 27, 31	r	**Reserved** Read as 0; should be written with 0.

Pn_PDR1 (n=0-6)
Port n Pad Driver Mode 1 Register(F000 0C44$_H$+n*100$_H$) Reset Value: 0000 0000$_H$
P8_PDR1
Port 8 Pad Driver Mode 1 Register (44$_H$) Reset Value: 0000 0000$_H$
P11_PDR1
Port 11 Pad Driver Mode 1 Register (44$_H$) Reset Value: 0000 0000$_H$
Pn_PDR1 (n=13-15)
Port n Pad Driver Mode 1 Register(F02F F444$_H$+n*100$_H$) Reset Value: 0000 0000$_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	PD15			0	PD14			0	PD13			0	PD12		
r	rw			r	rw			r	rw			r	rw		

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	PD11			0	PD10			0	PD9			0	PD8		
r	rw			r	rw			r	rw			r	rw		

Field	Bits	Type	Description
PD8	[2:0]	rw	**Pad Driver Mode for Pn.8**
PD9	[6:4]	rw	**Pad Driver Mode for Pn.9**
PD10	[10:8]	rw	**Pad Driver Mode for Pn.10**
PD11	[14:12]	rw	**Pad Driver Mode for Pn.11**
PD12	[18:16]	rw	**Pad Driver Mode for Pn.12**
PD13	[22:20]	rw	**Pad Driver Mode for Pn.13**
PD14	[26:24]	rw	**Pad Driver Mode for Pn.14**
PD15	[30:28]	rw	**Pad Driver Mode for Pn.15**
0	3, 7, 11, 15, 19, 23, 27, 31	r	**Reserved** Read as 0; should be written with 0.

10.3.3 Pin Function Decision Control Register

Pin Function Decision Control Register

The pad structure of the TC1798 GPIO lines offers the possibility to select the digital SENT input or analog ADC input functionalities at Port 17.This feature can be controlled by individual bits in the P17_PDISC, independently from input/output and pull-up/pull-down control functionality as programmed in the Pn_IOCR register.

P17_PDISC
Port 17 Pin Function Decision Control Register(60_H) **Reset Value: FFFF $FFFF_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PDIS 15	PDIS 14	PDIS 13	PDIS 12	PDIS 11	PDIS 10	PDIS 9	PDIS 8	PDIS 7	PDIS 6	PDIS 5	PDIS 4	PDIS 3	PDIS 2	PDIS 1	PDIS 0
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
PDISx (x = 0-15)	x	rw	**Pad Disable for Port n Pin x** This bit disables the port pad. 0_B Pad Pn.x is enabled. 1_B Pad Pn.x is disabled.
0	[31:16]	r	**Reserved** Read as 0; should be written with 0.

10.3.4 Port Output Register

The port output register determines the value of a GPIO pin when it is selected by Pn_IOCRx as output. Writing a 0 to a Pn_OUT.Px (x = 0-15) bit position delivers a low level at the corresponding output pin. A high level is output when the corresponding bit is written with a 1. Note that the bits of Pn_OUT.Px can be individually set/reset by writing appropriate values into the port output modification register Pn_OMR.

Pn_OUT (n=0-11)
Port n Output Register **($F000\ 0C00_H + n*100_H$)** **Reset Value: $0000\ 0000_H$**
Pn_OUT (n=12-16)
Port n Output Register **($F02F\ F400_H + n*100_H$)** **Reset Value: $0000\ 0000_H$**
P18_OUT
Port 18 Output Register **(00_H)** **Reset Value: $0000\ 0000_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P15	P14	P13	P12	P11	P10	P9	P8	P7	P6	P5	P4	P3	P2	P1	P0
rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh

Field	Bits	Type	Description
Px **(x = 0-15)**	x	rwh	**Port n Output Bit x** This bit determines the level at the output pin Pn.x if the output is selected as GPIO output. 0_B The output level of Pn.x is 0. 1_B The output level of Pn.x is 1. Pn.x can also be set/reset by control bits of the Pn_OMR register.
0	[31:16]	r	**Reserved** Read as 0; should be written with 0.

Note: Only Port 0, 1, 3, 4, 5, 11, 13, 14, 15and 17 are 16-bit wide ports. The Pn_OUT registers of the other ports have a reduced number of Px bits (see Pn_OUT register descriptions in the corresponding port sections).

10.3.5 Port Output Modification Register

The port output modification register contains control bits that make it possible to individually set, reset, or toggle the logic state of a single port line by manipulating the output register.

Pn_OMR (n=0-11)
Port n Output Modification Register (F000 0C04$_H$ + n*100$_H$) Reset Value: 0000 0000$_H$
Pn_OMR (n=12-16)
Port n Output Modification Register (F02F F404$_H$ + n*100$_H$) Reset Value: 0000 0000$_H$
P18_OMR
Port 18 Output Modification Register (04$_H$) Reset Value: 0000 0000$_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PR 15	**PR 14**	**PR 13**	**PR 12**	**PR 11**	**PR 10**	**PR 9**	**PR 8**	**PR 7**	**PR 6**	**PR 5**	**PR 4**	**PR 3**	**PR 2**	**PR 1**	**PR 0**
w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PS 15	**PS 14**	**PS 13**	**PS 12**	**PS 11**	**PS 10**	**PS 9**	**PS 8**	**PS 7**	**PS 6**	**PS 5**	**PS 4**	**PS 3**	**PS 2**	**PS 1**	**PS 0**
w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w

Field	Bits	Type	Description
PSx (x = 0-15)	x	w	**Port n Set Bit x** Setting this bit will set or toggle the corresponding bit in the port output register Pn_OUT. The function of this bit is shown in **Table 10-9**.
PRx (x = 0-15)	x + 16	w	**Port n Reset Bit x** Setting this bit will reset or toggle the corresponding bit in the port output register Pn_OUT. The function of this bit is shown in **Table 10-9**.

Note: Register Pn_OMR is virtual and does not contain any flip-flop. A read action delivers the value of 0. One 8 or 16-bits write behaves as a 32-bit write padded with zeros.

Table 10-9 Function of the Bits PRx and PSx

PRx	PSx	Function
0	0	Bit Pn_OUT.Px is not changed.
0	1	Bit Pn_OUT.Px is set.
1	0	Bit Pn_OUT.Px is reset.
1	1	Bit Pn_OUT.Px is toggled.

10.3.6 Emergency Stop Register

All GPIO lines which are used by the GPTA modules (GPTA0, GPTA1, LTCA2) have an emergency stop logic implemented (see **Figure 10-1**). These GPTA related GPIO lines are:

- P0.[7:0], P1.[15:8], P2.[15:8], P3.[15:0], P4.[15:0], P5.[15:0], P8.[7:0], P9.[7:0], P13.[15:0], and P14.[15:0]

Each of these GPIO lines has its own emergency stop enable bit ENx that is located in the emergency stop register Pn_ESR of Port n. If the emergency stop signal becomes active, one of two states can be selected:

- Emergency stop function disabled (ENx = 0):
  A GPTA output line remains connected to the GPTA module (alternate function).
- Emergency stop function enabled (ENx = 1):
  A GPTA output line is disconnected from the GPTA module (alternate function) and connected to the corresponding bit of the Pn_OUT output register (the content of the corresponding PCx bit fields in register Pn_IOCR is discarded).

Pn_ESR (n=0-5)
Port n Emergency Stop Register ($F000\ 0C50_H + n*100_H$) Reset Value: $0000\ 0000_H$
Pn_ESR (n=8-9)
Port n Emergency Stop Register ($F000\ 0C50_H + n*100_H$) Reset Value: $0000\ 0000_H$
Pn_ESR (n=13-14)
Port n Emergency Stop Register ($F02F\ F450_H + n*100_H$) Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EN 15	EN 14	EN 13	EN 12	EN 11	EN 10	EN 9	EN 8	EN 7	EN 6	EN 5	EN 4	EN 3	EN 2	EN 1	EN 0
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
ENx (x = 0-15)	x	rw	**Emergency Stop Enable for Port n Pin x** This bit enables the emergency stop function for GPIO lines used as GPTA outputs. If the emergency stop condition is met and enabled, the output selection is automatically switched from alternate (GPTA output) function to GPIO output function. 0_B Emergency stop function for Pn.x is disabled. 1_B Emergency stop function for Pn.x is enabled.
0	[31:16]	r	**Reserved** Read as 0; should be written with 0.

Note: Ports 3, 4, 5, 13, and 14 are 16-bit wide ports entirely used by the GPTA modules. The Pn_ESR registers of the other ports have a reduced number of bits (see Pn_ESR register descriptions in the corresponding port sections).

10.3.7 Port Input Register

The logic level of a GPIO pin can be read via the read-only port input register Pn_IN. Reading the Pn_IN register allways returns the current logical value at the GPIO pin independently whether the pin is selected as input or output.

Pn_IN (n=0-11)
Port n Input Register **(F000 0C24$_H$ + n*100$_H$)** **Reset Value: 0000 XXXX$_H$**
Pn_IN (n=12-16)
Port n Input Register **(F02F F424$_H$ + n*100$_H$)** **Reset Value: 0000 XXXX$_H$**
Pn_IN (n=17-18)
Port n Input Register **(F02F F424$_H$ + n*100$_H$)** **Reset Value: 0000 XXXX$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P15	P14	P13	P12	P11	P10	P9	P8	P7	P6	P5	P4	P3	P2	P1	P0
rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh

Field	Bits	Type	Description
Px **(x = 0-15)**	x	rh	**Port n Input Bit x** This bit indicates the level at the input pinPn.x. 0_B The input level of Pn.x is 0. 1_B The input level of Pn.x is 1.
0	[31:16]	r	**Reserved** Read as 0.

Note: Only Port 0, 1, 3, 4, 5, 11, 13, 14, 15and 17 are 16-bit wide ports. The Pn_IN registers of the other ports have a reduced number of Px bits (see Pn_IN register descriptions in the corresponding port sections).

10.4 Port 0

This section describes the Port 0 functionality in detail.

10.4.1 Port 0 Configuration

Port 0 is a general-purpose 16-bit bi-directional port. It serves as GPIO lines without secondary functions.

Table 10-10 summarizes the I/O control selection functions of each Port 0 line.

10.4.2 Port 0 Function Table

Table 10-10 summarizes the I/O control selection functions of each Port 0 line.

Table 10-10 Port 0 Functions

Port Pin	I/O	Pin Functionality	Associated Reg./ I/O Line	Port I/O Control Select.	
				Reg./Bit Field	Value
P0.0	I	General-purpose input	P0_IN.P0	P0_IOCR0.PC0	$0XXX_B$
			HWCFG0		
	O	General-purpose output	P0_OUT.P0		$1X00_B$
		GPTA0 output	OUT56		$1X01_B$
		GPTA1 output	OUT56		$1X10_B$
		LTCA2 output	OUT80		$1X11_B$
P0.1	I	General-purpose input	P0_IN.P1	P0_IOCR0.PC1	$0XXX_B$
			HWCFG1		
	O	General-purpose output	P0_OUT.P1		$1X00_B$
		GPTA0 output	OUT57		$1X01_B$
		GPTA1 output	OUT57		$1X10_B$
		LTCA2 output	OUT81		$1X11_B$
P0.2	I	General-purpose input	P0_IN.P2	P0_IOCR0.PC2	$0XXX_B$
			HWCFG2		
	O	General-purpose output	P0_OUT.P2		$1X00_B$
		GPTA0 output	OUT58		$1X01_B$
		GPTA1 output	OUT58		$1X10_B$
		LTCA2 output	OUT82		$1X11_B$
P0.3	I	General-purpose input	P0_IN.P3	P0_IOCR0.PC3	$0XXX_B$
			HWCFG3		
	O	General-purpose output	P0_OUT.P3		$1X00_B$
		GPTA0 output	OUT59		$1X01_B$
		GPTA1 output	OUT59		$1X10_B$
		LTCA2 output	OUT83		$1X11_B$

Table 10-10 Port 0 Functions (cont'd)

Port Pin	I/O	Pin Functionality	Associated Reg./ I/O Line	Port I/O Control Select.	
				Reg./Bit Field	Value
P0.4	I	General-purpose input	P0_IN.P4	P0_IOCR4.PC4	$0XXX_B$
			HWCFG4		
	O	General-purpose output	P0_OUT.P4		$1X00_B$
		GPTA0 output	OUT60		$1X01_B$
		GPTA1 output	OUT60		$1X10_B$
		MCDS event output 0[1)]	EVTO0		$1X11_B$
P0.5	I	General-purpose input	P0_IN.P5	P0_IOCR4.PC5	$0XXX_B$
			HWCFG5		
	O	General-purpose output	P0_OUT.P5		$1X00_B$
		GPTA0 output	OUT61		$1X01_B$
		GPTA1 output	OUT61		$1X10_B$
		MCDS event output 1[1)]	EVTO1		$1X11_B$
P0.6	I	General-purpose input	P0_IN.P6	P0_IOCR4.PC6	$0XXX_B$
			HWCFG6		
	O	General-purpose output	P0_OUT.P6		$1X00_B$
		GPTA0 output	OUT62		$1X01_B$
		GPTA1 output	OUT62		$1X10_B$
		MCDS event output 2[1)]	EVTO2		$1X11_B$
P0.7	I	General-purpose input	P0_IN.P7	P0_IOCR4.PC7	$0XXX_B$
			HWCFG7		
	O	General-purpose output	P0_OUT.P7		$1X00_B$
		GPTA0 output	OUT63		$1X01_B$
		GPTA1 output	OUT63		$1X10_B$
		MCDS event output 3[1)]	EVTO3		$1X11_B$
P0.8	I	General-purpose input	P0_IN.P8	P0_IOCR8.PC8	$0XXX_B$
	O	General-purpose output	P0_OUT.P8		$1X00_B$
		Reserved	–		$1X01_B$
		Reserved	–		$1X10_B$
		Reserved	–		$1X11_B$

Table 10-10 Port 0 Functions (cont'd)

Port Pin	I/O	Pin Functionality	Associated Reg./ I/O Line	Port I/O Control Select.	
				Reg./Bit Field	Value
P0.9	I	General-purpose input	P0_IN.P9	P0_IOCR8.PC9	$0XXX_B$
		E-Ray	RXDA0		
	O	General-purpose output	P0_OUT.P9		$1X00_B$
		Reserved	–		$1X01_B$
		Reserved	–		$1X10_B$
		Reserved	–		$1X11_B$
P0.10	I	General-purpose input	P0_IN.P10	P0_IOCR8. PC10	$0XXX_B$
	O	General-purpose output	P0_OUT.P10		$1X00_B$
		E-Ray	TXENA		$1X01_B$
		Reserved	–		$1X10_B$
		Reserved	–		$1X11_B$
P0.11	I	General-purpose input	P0_IN.P11	P0_IOCR8. PC11	$0XXX_B$
		GPT120	T5INB		
		GPT121	T5INA		
	O	General-purpose output	P0_OUT.P11		$1X00_B$
		E-Ray	TXENB		$1X01_B$
		Reserved	–		$1X10_B$
		Reserved	–		$1X11_B$
P0.12	I	General-purpose input	P0_IN.P12	P0_IOCR12. PC12	$0XXX_B$
		GPT120	T5EUDA		
		GPT121	T5EUDB		
	O	General-purpose output	P0_OUT.P12		$1X00_B$
		E-Ray	TXDB		$1X01_B$
		Reserved	–		$1X10_B$
		Reserved	–		$1X11_B$

Table 10-10 Port 0 Functions (cont'd)

Port Pin	I/O	Pin Functionality	Associated Reg./ I/O Line	Port I/O Control Select.	
				Reg./Bit Field	Value
P0.13	I	General-purpose input	P0_IN.P13	P0_IOCR12. PC13	$0XXX_B$
		E-Ray	RXDB0		
		GPT120	T5EUDB		
		GPT121	T5EUDA		
	O	General-purpose output	P0_OUT.P13		$1X00_B$
		Reserved	–		$1X01_B$
		Reserved	–		$1X10_B$
		Reserved	–		$1X11_B$
P0.14	I	General-purpose input	P0_IN.P14	P0_IOCR12. PC14	$0XXX_B$
		GPT120	T6INA		
		GPT121	T6INB		
	O	General-purpose output	P0_OUT.P14		$1X00_B$
		E-Ray	TXDA		$1X01_B$
		Reserved	–		$1X10_B$
		Reserved	–		$1X11_B$
P0.15	I	General-purpose input	P0_IN.P15	P0_IOCR12. PC15	$0XXX_B$
	O	General-purpose output	P0_OUT.P15		$1X00_B$
		Reserved	–		$1X01_B$
		Reserved	–		$1X10_B$
		Reserved	–		$1X11_B$

1) Only applicable in TC1798ED

10.4.3 Port 0 Registers

The following registers are available on Port 0:

Table 10-11 Port 0 Registers

Register Short Name	Register Long Name	Offset[1] Address	Description see
P0_OUT	Port 0 Output Register	0000_H	Page 10-21
P0_OMR	Port 0 Output Modification Register	0004_H	Page 10-22
P0_IOCR0	Port 0 Input/Output Control Register 0	0010_H	Page 10-11
P0_IOCR4	Port 0 Input/Output Control Register 4	0014_H	Page 10-12
P0_IOCR8	Port 0 Input/Output Control Register 8	0018_H	Page 10-13
P0_IOCR12	Port 0 Input/Output Control Register 12	$001C_H$	Page 10-14
P0_IN	Port 0 Input Register	0024_H	Page 10-25
P0_PDR0	Port 0 Pad Driver Mode 0 Register	0040_H	Page 10-18
P0_PDR1	Port 0 Pad Driver Mode 1 Register	0044_H	Page 10-19
P0_ESR	Port 0 Emergency Stop Register	0050_H	Page 10-24

1) The absolute addresses are calculated by adding the offset address to the module base address (see Table 10-4)

10.4.3.1 Port 0 Emergency Stop Register

The basic P0_ESR register functionality is described on Page 10-24. At Port 0, only port lines P0.[7:0] have GPTA outputs. Therefore, the P0_ESR bits EN[15:8] are not implemented. They are always read as 0 and should be written with 0.

10.5 Port 1

This section describes the Port 1 functionality in detail.

10.5.1 Port 1 Configuration

Port 1 is a 16-bit bi-directional general-purpose I/O port that can be alternatively used for the MLI0 I/O lines or for the external trigger inputs REQ[3:0] of the CPU. Furthermore, the system clock output SYSCLK is provided at Port 1.

10.5.2 Port 1 Function Table

Table 10-12 summarizes the I/O control selection functions of each Port 1 line.

Table 10-12 Port 1 Functions

Port Pin	I/O	Pin Functionality	Associated Reg./ I/O Line	Port I/O Control Select.	
				Reg./Bit Field	Value
P1.0	I	General-purpose input	P1_IN.P0	P1_IOCR0.PC0	$0XXX_B$
		SCU input	REQ0		
	O	General-purpose output	P1_OUT.P0		$1X00_B$
		SCU Output	EXTCLK1		$1X01_B$
		Reserved	–		$1X10_B$
		Reserved	–		$1X11_B$
P1.1	I	General-purpose input	P1_IN.P1	P1_IOCR0.PC1	$0XXX_B$
		SCU input	REQ1		
		CCU60	CC60INA		
		CCU61	CC60INB		
	O	General-purpose output	P1_OUT.P1		$1X00_B$
		CCU60	CC60		$1X01_B$
		Reserved	–		$1X10_B$
		Reserved	–		$1X11_B$
P1.2	I	General-purpose input	P1_IN.P2	P1_IOCR0.PC2	$0XXX_B$
		SCU input	REQ2		
	O	General-purpose output	P1_OUT.P2		$1X00_B$
		Reserved	–		$1X01_B$
		Reserved	–		$1X10_B$
		Reserved	–		$1X11_B$
P1.3	I	General-purpose input	P1_IN.P3	P1_IOCR0.PC3	$0XXX_B$
		SCU input	REQ3		
		MLI0 input	TREADY0B		
	O	General-purpose output	P1_OUT.P3		$1X00_B$
		Reserved	–		$1X01_B$
		Reserved	–		$1X10_B$
		Reserved	–		$1X11_B$

Table 10-12 Port 1 Functions (cont'd)

Port Pin	I/O	Pin Functionality	Associated Reg./ I/O Line	Port I/O Control Select.	
				Reg./Bit Field	Value
P1.4	I	General-purpose input	P1_IN.P4	P1_IOCR4.PC4	$0XXX_B$
	O	General-purpose output	P1_OUT.P4		$1X00_B$
		MLI0 output	TCLK0		$1X01_B$
		Reserved	–		$1X10_B$
		Reserved	–		$1X11_B$
P1.5	I	General-purpose input	P1_IN.P5	P1_IOCR4.PC5	$0XXX_B$
		MLI0 input	TREADY0A		
	O	General-purpose output	P1_OUT.P5		$1X00_B$
		Reserved	–		$1X01_B$
		Reserved	–		$1X10_B$
		Reserved	–		$1X11_B$
P1.6	I	General-purpose input	P1_IN.P6	P1_IOCR4.PC6	$0XXX_B$
	O	General-purpose output	P1_OUT.P6		$1X00_B$
		MLI0 output	TVALID0A		$1X01_B$
		SSC1 output	SLSO10		$1X10_B$
		CCU60	COUT60		$1X11_B$
P1.7	I	General-purpose input	P1_IN.P7	P1_IOCR4.PC7	$0XXX_B$
		CCU60	CC61INB		
		CCU61	CC61INA		
	O	General-purpose output	P1_OUT.P7		$1X00_B$
		MLI0 output	TDATA0		$1X01_B$
		CCU61	CC61		$1X10_B$
		GPT120	T3OUT		$1X11_B$
P1.8	I	General-purpose input	P1_IN.P8	P1_IOCR8.PC8	$0XXX_B$
		MLI0 input	RCLK0A		
	O	General-purpose output	P1_OUT.P8		$1X00_B$
		GPTA0 output	OUT64		$1X01_B$
		GPTA1 output	OUT64		$1X10_B$
		LTCA2 output	OUT88		$1X11_B$

Table 10-12 Port 1 Functions (cont'd)

Port Pin	I/O	Pin Functionality	Associated Reg./ I/O Line	Port I/O Control Select.	
				Reg./Bit Field	Value
P1.9	I	General-purpose input	P1_IN.P9	P1_IOCR8.PC9	$0XXX_B$
	O	General-purpose output	P1_OUT.P9		$1X00_B$
		MLI0 output	RREADY0A		$1X01_B$
		SSC1 output	SLSO11		$1X10_B$
		GPTA0 output	OUT65		$1X11_B$
P1.10	I	General-purpose input	P1_IN.P10	P1_IOCR8.PC10	$0XXX_B$
		MLI0 input	RVALID0A		
	O	General-purpose output	P1_OUT.P10		$1X00_B$
		GPTA0 output	OUT66		$1X01_B$
		GPTA1 output	OUT66		$1X10_B$
		LTCA2 output	OUT90		$1X11_B$
P1.11	I	General-purpose input	P1_IN.P11	P1_IOCR8.PC11	$0XXX_B$
		MLI0 input	RDATA0A		
		SSC3 input	$\overline{\text{SLSI3}}$		
	O	General-purpose output	P1_OUT.P11		$1X00_B$
		GPTA0 output	OUT67		$1X01_B$
		GPTA1 output	OUT67		$1X10_B$
		LTCA2 output	OUT91		$1X11_B$
P1.12		General-purpose input	P1_IN.P12	P1_IOCR12. PC12	$0XXX_B$
	O	General-purpose output	P1_OUT.P12		$1X00_B$
		System clock output	EXTCLK0		$1X01_B$
		GPTA0 output	OUT68		$1X10_B$
		GPTA1 output	OUT68		$1X11_B$
P1.13	I	General-purpose input	P1_IN.P13	P1_IOCR12. PC13	$0XXX_B$
		MLI0 input	RCLK0B		
	O	General-purpose output	P1_OUT.P13		$1X00_B$
		GPTA0 output	OUT69		$1X01_B$
		GPTA1 output	OUT69		$1X10_B$
		LTCA2 output	OUT93		$1X11_B$

Table 10-12 Port 1 Functions (cont'd)

Port Pin	I/O	Pin Functionality	Associated Reg./ I/O Line	Port I/O Control Select.	
				Reg./Bit Field	Value
P1.14	I	General-purpose input	P1_IN.P14	P1_IOCR12. PC14	$0XXX_B$
		MLI0 input	RVALID0B		
	O	General-purpose output	P1_OUT.P14		$1X00_B$
		GPTA0 output	OUT70		$1X01_B$
		GPTA1 output	OUT70		$1X10_B$
		LTCA2 output	OUT94		$1X11_B$
P1.15	I	General-purpose input	P1_IN.P15	P1_IOCR12. PC15	$0XXX_B$
		MLI0 input	RDATA0B		
	O	General-purpose output	P1_OUT.P15		$1X00_B$
		GPTA0 output	OUT71		$1X01_B$
		GPTA1 output	OUT71		$1X10_B$
		LTCA2 output	OUT95		$1X11_B$

10.5.3 Port 1 Registers

The following registers are available on Port 1:

Table 10-13 Port 1 Registers

Register Short Name	Register Long Name	Offset[1] Address	Description see
P1_OUT	Port 1 Output Register	0000_H	Page 10-21
P1_OMR	Port 1 Output Modification Register	0004_H	Page 10-22
P1_IOCR0	Port 1 Input/Output Control Register 0	0010_H	Page 10-11
P1_IOCR4	Port 1 Input/Output Control Register 4	0014_H	Page 10-12
P1_IOCR8	Port 1 Input/Output Control Register 8	0018_H	Page 10-13
P1_IOCR12	Port 1 Input/Output Control Register 12	$001C_H$	Page 10-14
P1_IN	Port 1 Input Register	0024_H	Page 10-25
P1_PDR0	Port 1 Pad Driver Mode 0 Register	0040_H	Page 10-18
P1_PDR1	Port 1 Pad Driver Mode 1 Register	0044_H	Page 10-19
P1_ESR	Port 1 Emergency Stop Register	0050_H	Page 10-24

1) The absolute addresses are calculated by adding the offset address to the module base address (see Table 10-4)

10.5.3.1 Port 1 Emergency Stop Register

The basic P1_ESR register functionality is described on **Page 10-24**. At Port 1, only port lines P1.[15:8] have GPTA outputs. Therefore, the P1_ESR bits EN[7:0] are not implemented. They are always read as 0 and should be written with 0.

10.6 Port 2

This section describes the Port 2 functionality in detail.

10.6.1 Port 2 Configuration

Port 2 is a 14-bit bi-directional general-purpose I/O port that can be used either for the SSC0/SSC1 chip select output lines or for MSC0/MSC1 or GPTA0/GPTA1/LTCA2 I/O lines.

10.6.2 Port 2 Function Table

Table 10-14 summarizes the I/O control selection functions of each Port 2 line.

Table 10-14 Port 2 Functions

Port Pin	I/O	Pin Functionality	Associated Reg./ I/O Line	Port I/O Control Select.	
				Reg./Bit Field	Value
P2.2	I	General-purpose input	P2_IN.P2	P2_IOCR0.PC2	$0XXX_B$
	O	General-purpose output	P2_OUT.P2		$1X00_B$
		SSC0 output	SLSO02		$1X01_B$
		SSC1 output	SLSO12		$1X10_B$
		SSC1 output	SLSOANDO12		$1X11_B$
P2.3	I	General-purpose input	P2_IN.P3	P2_IOCR0.PC3	$0XXX_B$
	O	General-purpose output	P2_OUT.P3		$1X00_B$
		SSC0 output	SLSO03		$1X01_B$
		SSC1 output	SLSO13		$1X10_B$
		SSC1 output	SLSOANDO13		$1X11_B$
P2.4	I	General-purpose input	P2_IN.P4	P2_IOCR4.PC4	$0XXX_B$
	O	General-purpose output	P2_OUT.P4		$1X00_B$
		SSC0 output	SLSO04		$1X01_B$
		SSC1 output	SLSO14		$1X10_B$
		SSC1 output	SLSOANDO14		$1X11_B$

Table 10-14 Port 2 Functions (cont'd)

Port Pin	I/O	Pin Functionality	Associated Reg./ I/O Line	Port I/O Control Select.	
				Reg./Bit Field	Value
P2.5	I	General-purpose input	P2_IN.P5	P2_IOCR4.PC5	$0XXX_B$
	O	General-purpose output	P2_OUT.P5		$1X00_B$
		SSC0 output	SLSO05		$1X01_B$
		SSC1 output	SLSO15		$1X10_B$
		SSC1 output	SLSOANDO15		$1X11_B$
P2.6	I	General-purpose input	P2_IN.P6	P2_IOCR4.PC6	$0XXX_B$
	O	General-purpose output	P2_OUT.P6		$1X00_B$
		SSC0 output	SLSO06		$1X01_B$
		SSC1 output	SLSO16		$1X10_B$
		SSC1 output	SLSOANDO16		$1X11_B$
P2.7	I	General-purpose input	P2_IN.P7	P2_IOCR4.PC7	$0XXX_B$
	O	General-purpose output	P2_OUT.P7		$1X00_B$
		SSC0 output	SLSO07		$1X01_B$
		SSC1 output	SLSO17		$1X10_B$
		SSC1 output	SLSOANDO17		$1X11_B$
P2.8	I	General-purpose input	P2_IN.P8	P2_IOCR8.PC8	$0XXX_B$
		GPTA0/GPTA1/LTCA2 input	IN0		
		CCU62	CCPOS0A		
		CCU63	T12HRB		
		GPT120	T3INB		
		GPT121	T3INA		
	O	General-purpose output	P2_OUT.P8		$1X00_B$
		GPTA0 output	OUT0		$1X01_B$
		GPTA1 output	OUT0		$1X10_B$
		LTCA2 output	OUT0		$1X11_B$

Table 10-14 Port 2 Functions (cont'd)

Port Pin	I/O	Pin Functionality	Associated Reg./ I/O Line	Port I/O Control Select.	
				Reg./Bit Field	Value
P2.9	I	General-purpose input	P2_IN.P9	P2_IOCR8.PC9	$0XXX_B$
		GPTA0/GPTA1/LTCA2 input	IN1		
	O	General-purpose output	P2_OUT.P9		$1X00_B$
		GPTA0 output	OUT1		$1X01_B$
		GPTA1 output	OUT1		$1X10_B$
		LTCA2 output	OUT1		$1X11_B$
P2.10	I	General-purpose input	P2_IN.P10	P2_IOCR8. PC10	$0XXX_B$
		GPTA0/GPTA1/LTCA2 input	IN2		
		CCU60	T12HRE		
		CCU60	CC61INC		
		CCU61	$\overline{\text{CTRAPA}}$		
		CCU61	CC60INC		
		CCU63	$\overline{\text{CTRAPB}}$		
	O	General-purpose output	P2_OUT.P10		$1X00_B$
		GPTA0 output	OUT2		$1X01_B$
		GPTA1 output	OUT2		$1X10_B$
		LTCA2 output	OUT2		$1X11_B$
P2.11	I	General-purpose input	P2_IN.P11	P2_IOCR8. PC11	$0XXX_B$
		GPTA0/GPTA1/LTCA2 input	IN3		
	O	General-purpose output	P2_OUT.P11		$1X00_B$
		GPTA0 output	OUT3		$1X01_B$
		GPTA1 output	OUT3		$1X10_B$
		LTCA2 output	OUT3		$1X11_B$

Table 10-14 Port 2 Functions (cont'd)

Port Pin	I/O	Pin Functionality	Associated Reg./ I/O Line	Port I/O Control Select.	
				Reg./Bit Field	Value
P2.12	I	General-purpose input	P2_IN.P12	P2_IOCR12. PC12	$0XXX_B$
		GPTA0/GPTA1/LTCA2 input	IN4		
		CCU62	T12HRB		
		CCU63	CCPOS0A		
		GPT120	T2INB		
		GPT121	T2INA		
	O	General-purpose output	P2_OUT.P12		$1X00_B$
		GPTA0 output	OUT4		$1X01_B$
		GPTA1 output	OUT4		$1X10_B$
		LTCA2 output	OUT4		$1X11_B$
P2.13	I	General-purpose input	P2_IN.P13	P2_IOCR12. PC13	$0XXX_B$
		GPTA0/GPTA1/LTCA2 input	IN5		
	O	General-purpose output	P2_OUT.P13		$1X00_B$
		GPTA0 output	OUT5		$1X01_B$
		GPTA1 output	OUT5		$1X10_B$
		LTCA2 output	OUT5		$1X11_B$
P2.14	I	General-purpose input	P2_IN.P14	P2_IOCR12. PC14	$0XXX_B$
		GPTA0/GPTA1/LTCA2 input	IN6		
		CCU60	CCPOS0A		
		CCU61	T12HRB		
		GPT120	T3INA		
		GPT121	T3INB		
	O	General-purpose output	P2_OUT.P14		$1X00_B$
		GPTA0 output	OUT6		$1X01_B$
		GPTA1 output	OUT6		$1X10_B$
		LTCA2 output	OUT6		$1X11_B$

Table 10-14 Port 2 Functions (cont'd)

Port Pin	I/O	Pin Functionality	Associated Reg./ I/O Line	Port I/O Control Select.	
				Reg./Bit Field	Value
P2.15	I	General-purpose input	P2_IN.P15	P2_IOCR12. PC15	$0XXX_B$
		GPTA0/GPTA1/LTCA2 input	IN7		
	O	General-purpose output	P2_OUT.P15		$1X00_B$
		GPTA0 output	OUT7		$1X01_B$
		GPTA1 output	OUT7		$1X10_B$
		LTCA2 output	OUT7		$1X11_B$

10.6.3 Port 2 Registers

The following registers are available on Port 2:

Table 10-15 Port 2 Registers

Register Short Name	Register Long Name	Offset[1] Address	Description see
P2_OUT	Port 2 Output Register	0000_H	below[2]
P2_OMR	Port 2 Output Modification Register	0004_H	
P2_IOCR0	Port 2 Input/Output Control Register 0	0010_H	Page 10-45[2]
P2_IOCR4	Port 2 Input/Output Control Register 4	0014_H	Page 10-12
P2_IOCR8	Port 2 Input/Output Control Register 8	0018_H	Page 10-13
P2_IOCR12	Port 2 Input/Output Control Register 12	$001C_H$	Page 10-14
P2_IN	Port 2 Input Register	0024_H	Page 10-45[2]
P2_PDR0	Port 2 Pad Driver Mode 0 Register	0040_H	Page 10-46
P2_PDR1	Port 2 Pad Driver Mode 1 Register	0044_H	Page 10-19
P2_ESR	Port 2 Emergency Stop Register	0050_H	Page 10-46[2]

1) The absolute addresses are calculated by adding the offset address to the module base address (see Table 10-4)

2) These registers are listed and noted here in the Port 2 section because they differ from the general port register description given in Section 10.3.

10.6.3.1 Port 2 Output Register

The basic P2_OUT register functionality is described on Page 10-21. Port lines P2.[1:0] are not connected to port lines. Therefore, reading the P2_OUT bits P[1:0] returns the value that was last written (0 after reset). These bits can be also set/reset by the corresponding P2_OMR bits.

10.6.3.2 Port 2 Output Modification Register

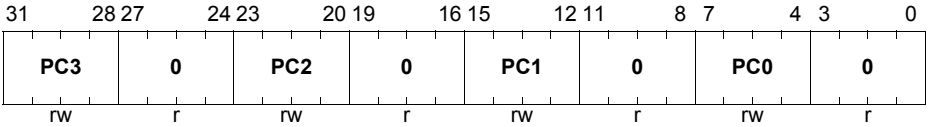
The basic P2_OMR register functionality is described on Page 10-22. However, port lines P2.0 and P2.1 are not available. Therefore, the P2_OMR bits PS[1:0] and PR[1:0] have no direct effect on port lines but only on register bits P2_OUT.P[1:0].

10.6.3.3 Port 2 Input/Output Control Register 0

Port lines P2.0 and P2.1 are not available. Therefore, the PC0 and PC1 bit fields in register P2_IOCR0 are not connected to any port lines.

P2_IOCR0
Port 2 Input/Output Control Register 0

(10_H) **Reset Value: 2020 2020_H**



Field	Bits	Type	Description
PC0, PC1	[7:4], [15:12]	rw	**Reserved** Read as 0010_B after reset; returns value that was written.
PC2	[23:20]	rw	**Port Control for Port 2.2** (coding see **Table 10-7** on **Page 10-15**)
PC3	[31:28]	rw	**Port Control for Port 2.3** (coding see **Table 10-7** on **Page 10-15**)
0	[3:0], [11:8], [19:16], [27:24]	r	**Reserved** Read as 0; should be written with 0.

10.6.3.4 Port 2 Input Register

The basic P2_IN register functionality is described on **Page 10-25**. However, port lines P2.0 and P2.1 are not available. Therefore, bits P0 and P1 in register P2_IN are always read as 0.

10.6.3.5 Port 2 Pad Driver Mode 0 Register

The basic P2_PDR0 register functionality is described on Page 10-18. However, port lines P2.0 and P2.1 are not available.

P2_PDR0
Port 2 Pad Driver Mode 0 Register (40_H) Reset Value: 0000 0000$_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	PD7			0	PD6			0	PD5			0	PD4		
r	rw			r	rw			r	rw			r	rw		

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	PD3			0	PD2			0	PD1			0	PD0		
r	rw			r	rw			r	rw			r	rw		

Field	Bits	Type	Description
PD0	[2:0]	rw	**Reserved** Read as 000_B after reset; returns value that was written.
PD1	[6:4]	rw	**Reserved** Read as 000_B after reset; returns value that was written.
PD2	[10:8]	rw	**Pad Driver Mode for P2.2**
PD3	[14:12]	rw	**Pad Driver Mode for P2.3**
PD4	[18:16]	rw	**Pad Driver Mode for P2.4**
PD5	[22:20]	rw	**Pad Driver Mode for P2.5**
PD6	[26:24]	rw	**Pad Driver Mode for P2.6**
PD7	[30:28]	rw	**Pad Driver Mode for P2.7**
0	3, 7, 11, 15, 19, 23, 27, 31	r	**Reserved** Read as 0; should be written with 0.

10.6.3.6 Port 2 Emergency Stop Register

The basic P2_ESR register functionality is described on Page 10-24. At Port 2, only port lines P2.[15:8] are connected to GPTA I/O lines. Therefore, only these port lines of Port 2

can be controlled for the emergency stop function. The P2_ESR bits EN[7:0] are not implemented. They are always read as 0 and should be written with 0.

10.7 Port 3

This section describes the Port 3 functionality in detail.

10.7.1 Port 3 Configuration

Port 3 is a 16-bit bi-directional general-purpose I/O port that can be used for the GPTA0/GPTA1/LTCA2 I/O lines.

10.7.2 Port 3 Function Table

Table 10-16 summarizes the I/O control selection functions of each Port 3 line.

Table 10-16 Port 3 Functions

Port Pin	I/O	Pin Functionality	Associated Reg./ I/O Line	Port I/O Control Select.	
				Reg./Bit Field	Value
P3.0	I	General-purpose input	P3_IN.P0	P3_IOCR0.PC0	$0XXX_B$
		GPTA0/GPTA1/LTCA2 input	IN8		
		CCU62	$\overline{\text{CTRAPA}}$		
		CCU62	CC60INC		
		CCU63	T12HRE		
		CCU63	CC61INC		
		CCU61	$\overline{\text{CTRAPB}}$		
		GPT120	T5INA		
		GPT121	T5INB		
	O	General-purpose output	P3_OUT.P0		$1X00_B$
		GPTA0 output	OUT8		$1X01_B$
		GPTA1 output	OUT8		$1X10_B$
		LTCA2 output	OUT8		$1X11_B$
P3.1	I	General-purpose input	P3_IN.P1	P3_IOCR0.PC1	$0XXX_B$
		GPTA0/GPTA1/LTCA2 input	IN9		
	O	General-purpose output	P3_OUT.P1		$1X00_B$
		GPTA0 output	OUT9		$1X01_B$
		GPTA1 output	OUT9		$1X10_B$
		LTCA2 output	OUT9		$1X11_B$

Table 10-16 Port 3 Functions (cont'd)

Port Pin	I/O	Pin Functionality	Associated Reg./ I/O Line	Port I/O Control Select.	
				Reg./Bit Field	Value
P3.2	I	General-purpose input	P3_IN.P2	P3_IOCR0.PC2	$0XXX_B$
		GPTA0/GPTA1/LTCA2 input	IN10		
		CCU63	T13HRE		
	O	General-purpose output	P3_OUT.P2		$1X00_B$
		GPTA0 output	OUT10		$1X01_B$
		GPTA1 output	OUT10		$1X10_B$
		LTCA2 output	OUT10		$1X11_B$
P3.3	I	General-purpose input	P3_IN.P3	P3_IOCR0.PC3	$0XXX_B$
		GPTA0/GPTA1/LTCA2 input	IN11		
	O	General-purpose output	P3_OUT.P3		$1X00_B$
		GPTA0 output	OUT11		$1X01_B$
		GPTA1 output	OUT11		$1X10_B$
		LTCA2 output	OUT11		$1X11_B$
P3.4	I	General-purpose input	P3_IN.P4	P3_IOCR4.PC4	$0XXX_B$
		GPTA0/GPTA1/LTCA2 input	IN12		
		CCU62	T12HRE		
		CCU62	CC61INC		
		CCU63	$\overline{\text{CTRAPA}}$		
		CCU63	CC60INC		
		CCU60	$\overline{\text{CTRAPB}}$		
	O	General-purpose output	P3_OUT.P4		$1X00_B$
		GPTA0 output	OUT12		$1X01_B$
		GPTA1 output	OUT12		$1X10_B$
		LTCA2 output	OUT12		$1X11_B$

Table 10-16 Port 3 Functions (cont'd)

Port Pin	I/O	Pin Functionality	Associated Reg./ I/O Line	Port I/O Control Select.	
				Reg./Bit Field	Value
P3.5	I	General-purpose input	P3_IN.P5	P3_IOCR4.PC5	$0XXX_B$
		GPTA0/GPTA1/LTCA2 input	IN13		
	O	General-purpose output	P3_OUT.P5		$1X00_B$
		GPTA0 output	OUT13		$1X01_B$
		GPTA1 output	OUT13		$1X10_B$
		LTCA2 output	OUT13		$1X11_B$
P3.6	I	General-purpose input	P3_IN.P6	P3_IOCR4.PC6	$0XXX_B$
		GPTA0/GPTA1/LTCA2 input	IN14		
		CCU62	T13HRE		
		GPT120	T6EUDB		
		GPT121	T6EUDA		
	O	General-purpose output	P3_OUT.P6		$1X00_B$
		GPTA0 output	OUT14		$1X01_B$
		GPTA1 output	OUT14		$1X10_B$
		LTCA2 output	OUT14		$1X11_B$
P3.7	I	General-purpose input	P3_IN.P7	P3_IOCR4.PC7	$0XXX_B$
		GPTA0/GPTA1/LTCA2 input	IN15		
	O	General-purpose output	P3_OUT.P7		$1X00_B$
		GPTA0 output	OUT15		$1X01_B$
		GPTA1 output	OUT15		$1X10_B$
		LTCA2 output	OUT15		$1X11_B$

Table 10-16 Port 3 Functions (cont'd)

Port Pin	I/O	Pin Functionality	Associated Reg./ I/O Line	Port I/O Control Select.	
				Reg./Bit Field	Value
P3.8	I	General-purpose input	P3_IN.P8	P3_IOCR8.PC8	$0XXX_B$
		GPTA0/GPTA1/LTCA2 input	IN16		
		CCU61	T13HRE		
	O	General-purpose output	P3_OUT.P8		$1X00_B$
		GPTA0 output	OUT16		$1X01_B$
		GPTA1 output	OUT16		$1X10_B$
		LTCA2 output	OUT16		$1X11_B$
P3.9	I	General-purpose input	P3_IN.P9	P3_IOCR8.PC9	$0XXX_B$
		GPTA0/GPTA1/LTCA2 input	IN17		
	O	General-purpose output	P3_OUT.P9		$1X00_B$
		GPTA0 output	OUT17		$1X01_B$
		GPTA1 output	OUT17		$1X10_B$
		LTCA2 output	OUT17		$1X11_B$
P3.10	I	General-purpose input	P3_IN.P10	P3_IOCR8. PC10	$0XXX_B$
		GPTA0/GPTA1/LTCA2 input	IN18		
		CCU62	CCPOS1A		
		CCU63	T13HRB		
		GPT120	T3EUDB		
		GPT121	T3EUDA		
	O	General-purpose output	P3_OUT.P10		$1X00_B$
		GPTA0 output	OUT18		$1X01_B$
		GPTA1 output	OUT18		$1X10_B$
		LTCA2 output	OUT18		$1X11_B$

Table 10-16 Port 3 Functions (cont'd)

Port Pin	I/O	Pin Functionality	Associated Reg./ I/O Line	Port I/O Control Select.	
				Reg./Bit Field	Value
P3.11	I	General-purpose input	P3_IN.P11	P3_IOCR8. PC11	$0XXX_B$
		GPTA0/GPTA1/LTCA2 input	IN19		
	O	General-purpose output	P3_OUT.P11		$1X00_B$
		GPTA0 output	OUT19		$1X01_B$
		GPTA1 output	OUT19		$1X10_B$
		LTCA2 output	OUT19		$1X11_B$
P3.12	I	General-purpose input	P3_IN.P12	P3_IOCR12. PC12	$0XXX_B$
		GPTA0/GPTA1/LTCA2 input	IN20		
		CCU62	CCPOS2A		
		CCU63	T12HRC		
		CCU63	T13HRC		
		GPT120	T4INB		
		GPT121	T4INA		
	O	General-purpose output	P3_OUT.P12		$1X00_B$
		GPTA0 output	OUT20		$1X01_B$
		GPTA1 output	OUT20		$1X10_B$
		LTCA2 output	OUT20		$1X11_B$
P3.13	I	General-purpose input	P3_IN.P13	P3_IOCR12. PC13	$0XXX_B$
		GPTA0/GPTA1/LTCA2 input	IN21		
	O	General-purpose output	P3_OUT.P13		$1X00_B$
		GPTA0 output	OUT21		$1X01_B$
		GPTA1 output	OUT21		$1X10_B$
		LTCA2 output	OUT21		$1X11_B$

Table 10-16 Port 3 Functions (cont'd)

Port Pin	I/O	Pin Functionality	Associated Reg./ I/O Line	Port I/O Control Select.	
				Reg./Bit Field	Value
P3.14	I	General-purpose input	P3_IN.P14	P3_IOCR12. PC14	$0XXX_B$
		GPTA0/GPTA1/LTCA2 input	IN22		
		CCU60	T13HRE		
	O	General-purpose output	P3_OUT.P14		$1X00_B$
		GPTA0 output	OUT22		$1X01_B$
		GPTA1 output	OUT22		$1X10_B$
		LTCA2 output	OUT22		$1X11_B$
P3.15	I	General-purpose input	P3_IN.P15	P3_IOCR12. PC15	$0XXX_B$
		GPTA0/GPTA1/LTCA2 input	IN23		
	O	General-purpose output	P3_OUT.P15		$1X00_B$
		GPTA0 output	OUT23		$1X01_B$
		GPTA1 output	OUT23		$1X10_B$
		LTCA2 output	OUT23		$1X11_B$

10.7.3 Port 3 Registers

The following registers are available on Port 3:

Table 10-17 Port 3 Registers

Register Short Name	Register Long Name	Offset[1] Address	Description see
P3_OUT	Port 3 Output Register	0000_H	Page 10-21
P3_OMR	Port 3 Output Modification Register	0004_H	Page 10-22
P3_IOCR0	Port 3 Input/Output Control Register 0	0010_H	Page 10-11
P3_IOCR4	Port 3 Input/Output Control Register 4	0014_H	Page 10-12
P3_IOCR8	Port 3 Input/Output Control Register 8	0018_H	Page 10-13
P3_IOCR12	Port 3 Input/Output Control Register 12	$001C_H$	Page 10-14
P3_IN	Port 3 Input Register	0024_H	Page 10-25
P3_PDR0	Port 3 Pad Driver Mode 0 Register	0040_H	Page 10-18
P3_PDR1	Port 3 Pad Driver Mode 1 Register	0044_H	Page 10-19
P3_ESR	Port 3 Emergency Stop Register	0050_H	Page 10-24

1) The absolute addresses are calculated by adding the offset address to the module base address (see Table 10-4)

10.8 Port 4

This section describes the Port 4 functionality in detail.

10.8.1 Port 4 Configuration

Port 4 is a 16-bit bi-directional general-purpose I/O port that can be used for the GPTA0/GPTA1/LTCA2 I/O lines.

10.8.2 Port 4 Function Table

Table 10-18 summarizes the I/O control selection functions of each Port 4 line.

Table 10-18 Port 4 Functions

Port Pin	I/O	Pin Functionality	Associated Reg./ I/O Line	Port I/O Control Select.	
				Reg./Bit Field	Value
P4.0	I	General-purpose input	P4_IN.P0	P4_IOCR0.PC0	$0XXX_B$
		GPTA0/GPTA1/LTCA2 input	IN24		
		SSC2 input A (Slave Mode)	MRST2A		
	O	General-purpose output	P4_OUT.P0		$1X00_B$
		GPTA0 output	OUT24		$1X01_B$
		GPTA1 output	OUT24		$1X10_B$
		SSC2 output (Master Mode)	MRST2		$1X11_B$

Table 10-18 Port 4 Functions (cont'd)

Port Pin	I/O	Pin Functionality	Associated Reg./ I/O Line	Port I/O Control Select.	
				Reg./Bit Field	Value
P4.1	I	General-purpose input	P4_IN.P1	P4_IOCR0.PC1	$0XXX_B$
		GPTA0/GPTA1/LTCA2 input	IN25		
		SSC2 input A (Master Mode)	MTSR2A		
		SSC Guardian 2 Master Receive Input A (Master Mode)	MRSTG2A		
	O	General-purpose output	P4_OUT.P1		$1X00_B$
		GPTA0 output	OUT25		$1X01_B$
		GPTA1 output	OUT25		$1X10_B$
		SSC2 output (Slave Mode)	MTSR2		$1X11_B$
P4.2	I	General-purpose input	P4_IN.P2	P4_IOCR0.PC2	$0XXX_B$
		GPTA0/GPTA1/LTCA2 input	IN26		
		SSC2 input A	SCLK2A		
	O	General-purpose output	P4_OUT.P2		$1X00_B$
		GPTA0 output	OUT26		$1X01_B$
		GPTA1 output	OUT26		$1X10_B$
		SSC2 output	SCLK2		$1X11_B$
P4.3	I	General-purpose input	P4_IN.P3	P4_IOCR0.PC3	$0XXX_B$
		GPTA0/GPTA1/LTCA2 input	IN27		
	O	General-purpose output	P4_OUT.P3		$1X00_B$
		GPTA0 output	OUT27		$1X01_B$
		GPTA1 output	OUT27		$1X10_B$
		SSC2 output	SLSO20		$1X11_B$

Table 10-18 Port 4 Functions (cont'd)

Port Pin	I/O	Pin Functionality	Associated Reg./ I/O Line	Port I/O Control Select.	
				Reg./Bit Field	Value
P4.4	I	General-purpose input	P4_IN.P4	P4_IOCR4.PC4	$0XXX_B$
		GPTA0/GPTA1/LTCA2 input	IN28		
	O	General-purpose output	P4_OUT.P4		$1X00_B$
		GPTA0 output	OUT28		$1X01_B$
		GPTA1 output	OUT28		$1X10_B$
		SSC2 output	SLSO21		$1X11_B$
P4.5	I	General-purpose input	P4_IN.P5	P4_IOCR4.PC5	$0XXX_B$
		GPTA0/GPTA1/LTCA2 input	IN29		
	O	General-purpose output	P4_OUT.P5		$1X00_B$
		GPTA0 output	OUT29		$1X01_B$
		GPTA1 output	OUT29		$1X10_B$
		SSC2 output	SLSO22		$1X11_B$
P4.6	I	General-purpose input	P4_IN.P6	P4_IOCR4.PC6	$0XXX_B$
		GPTA0/GPTA1/LTCA2 input	IN30		
	O	General-purpose output	P4_OUT.P6		$1X00_B$
		GPTA0 output	OUT30		$1X01_B$
		GPTA1 output	OUT30		$1X10_B$
		SSC2 output	SLSO23		$1X11_B$
P4.7	I	General-purpose input	P4_IN.P7	P4_IOCR4.PC7	$0XXX_B$
		GPTA0/GPTA1/LTCA2 input	IN31		
		GPT120	T6INB		
		GPT121	T6INA		
	O	General-purpose output	P4_OUT.P7		$1X00_B$
		GPTA0 output	OUT31		$1X01_B$
		GPTA1 output	OUT31		$1X10_B$
		SSC2 output	SLSO24		$1X11_B$

Table 10-18 Port 4 Functions (cont'd)

Port Pin	I/O	Pin Functionality	Associated Reg./ I/O Line	Port I/O Control Select.	
				Reg./Bit Field	Value
P4.8	I	General-purpose input	P4_IN.P8	P4_IOCR8.PC8	$0XXX_B$
		GPTA0/GPTA1input	IN32		
		CCU60	CCPOS1A		
		CCU61	T13HRB		
		GPT120	T3EUDA		
		GPT121	T3EUDB		
	O	General-purpose output	P4_OUT.P8		$1X00_B$
		GPTA0 output	OUT32		$1X01_B$
		GPTA1 output	OUT32		$1X10_B$
		LTCA2 output	OUT0		$1X11_B$
P4.9	I	General-purpose input	P4_IN.P9	P4_IOCR8.PC9	$0XXX_B$
		GPTA0/GPTA1input	IN33		
		SSC2 input	$\overline{SLSI2}$		
		CCU60	CCPOS2A		
		CCU61	T12HRC		
		CCU61	T13HRC		
		GPT120	T4INA		
		GPT121	T4INB		
	O	General-purpose output	P4_OUT.P9		$1X00_B$
		GPTA0 output	OUT33		$1X01_B$
		GPTA1 output	OUT33		$1X10_B$
		LTCA2 output	OUT1		$1X11_B$

Table 10-18 Port 4 Functions (cont'd)

Port Pin	I/O	Pin Functionality	Associated Reg./ I/O Line	Port I/O Control Select.	
				Reg./Bit Field	Value
P4.10	I	General-purpose input	P4_IN.P10	P4_IOCR8. PC10	$0XXX_B$
		CCU60	T12HRB		
		CCU61	CCPOS0A		
		GPT120	T2INA		
		GPT121	T2INB		
		GPTA0/GPTA1 input	IN34		
	O	General-purpose output	P4_OUT.P10		$1X00_B$
		GPTA0 output	OUT34		$1X01_B$
		GPTA1 output	OUT34		$1X10_B$
		LTCA2 output	OUT2		$1X11_B$
P4.11	I	General-purpose input	P4_IN.P11	P4_IOCR8. PC11	$0XXX_B$
		GPTA0/GPTA1 input	IN35		
	O	General-purpose output	P4_OUT.P11		$1X00_B$
		GPTA0 output	OUT35		$1X01_B$
		GPTA1 output	OUT35		$1X10_B$
		LTCA2 output	OUT3		$1X11_B$
P4.12	I	General-purpose input	P4_IN.P12	P4_IOCR12. PC12	$0XXX_B$
		GPTA0/GPTA1 input	IN36		
		CCU60	T13HRB		
		CCU61	CCPOS1A		
		GPT120	T2EUDA		
		GPT121	T2EUDB		
	O	General-purpose output	P4_OUT.P12		$1X00_B$
		GPTA1 output	OUT36		$1X10_B$
		GPTA0 output	OUT36		$1X01_B$
		LTCA2 output	OUT4		$1X11_B$

Table 10-18 Port 4 Functions (cont'd)

Port Pin	I/O	Pin Functionality	Associated Reg./ I/O Line	Port I/O Control Select.	
				Reg./Bit Field	Value
P4.13	I	General-purpose input	P4_IN.P13	P4_IOCR12. PC13	$0XXX_B$
		GPTA0/GPTA1 input	IN37		
	O	General-purpose output	P4_OUT.P13		$1X00_B$
		GPTA0 output	OUT37		$1X01_B$
		GPTA1 output	OUT37		$1X10_B$
		LTCA2 output	OUT5		$1X11_B$
P4.14	I	General-purpose input	P4_IN.P14	P4_IOCR12. PC14	$0XXX_B$
		GPTA0/GPTA1 input	IN38		
		CCU60	T12HRC		
		CCU60	T13HRC		
		CCU61	CCPOS2A		
		GPT120	T4EUDA		
		GPT121	T4EUDB		
	O	General-purpose output	P4_OUT.P14		$1X00_B$
		GPTA0 output	OUT38		$1X01_B$
		GPTA1 output	OUT38		$1X10_B$
		LTCA2 output	OUT6		$1X11_B$
P4.15	I	General-purpose input	P4_IN.P15	P4_IOCR12. PC15	$0XXX_B$
		GPTA0/GPTA1 input	IN39		
	O	General-purpose output	P4_OUT.P15		$1X00_B$
		GPTA0 output	OUT39		$1X01_B$
		GPTA1 output	OUT39		$1X10_B$
		LTCA2 output	OUT7		$1X11_B$

10.8.3 Port 4 Registers

The following registers are available on Port 4:

Table 10-19 Port 4 Registers

Register Short Name	Register Long Name	Offset[1] Address	Description see
P4_OUT	Port 4 Output Register	0000_H	Page 10-21
P4_OMR	Port 4 Output Modification Register	0004_H	Page 10-22
P4_IOCR0	Port 4 Input/Output Control Register 0	0010_H	Page 10-11
P4_IOCR4	Port 4 Input/Output Control Register 4	0014_H	Page 10-12
P4_IOCR8	Port 4 Input/Output Control Register 8	0018_H	Page 10-13
P4_IOCR12	Port 4 Input/Output Control Register 12	$001C_H$	Page 10-14
P4_IN	Port 4 Input Register	0024_H	Page 10-25
P4_PDR0	Port 4 Pad Driver Mode 0 Register	0040_H	Page 10-18
P4_PDR1	Port 4 Pad Driver Mode 1 Register	0044_H	Page 10-19
P4_ESR	Port 4 Emergency Stop Register	0050_H	Page 10-24

1) The absolute addresses are calculated by adding the offset address to the module base address (see Table 10-4)

10.9 Port 5

Port 5 is an 16-bit GPIO port. Pins associated to it be used in two ways:

- as a CMOS Port where each pin outputs one signal, as any other port (only exception - no open drain mode available), and
- as an output LVDS port where a pin pair (two pins) outputs one differential MSC signal.

The switching between the two modes is done via the PDR registers.

The swithcing between Input/Ouput and Pull-Up/Pull-Down control is done via the IOCR register.

Attention: In the LVDS mode the IOCR.PCx bit field of each pin of the LVDS pair must be programed as output, that is $1xxx_B$.

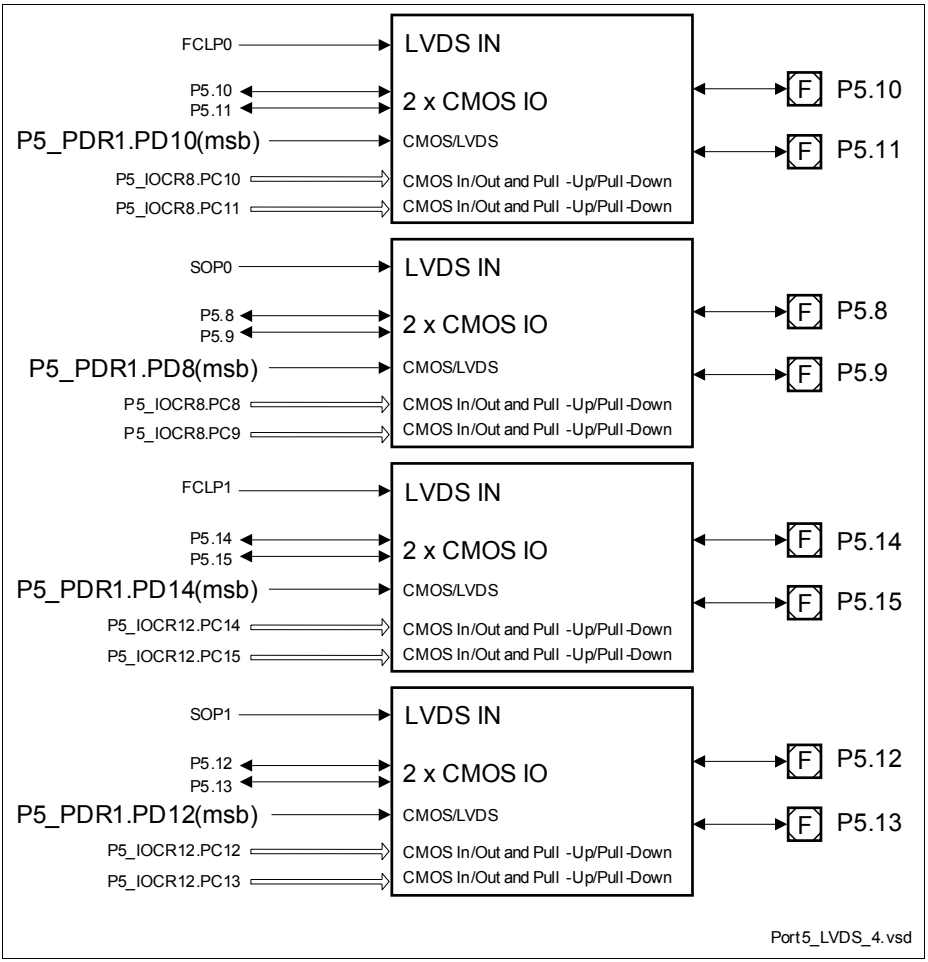


Figure 10-3 Port 5 Pad Connections

10.9.1 Port 5 Configuration

Port 5 is an bi-directional general-purpose I/O port which can be used for the ASC0/ASC1, MSC0/MSC1, or MLI0 interface I/O lines.

10.9.2 Port 5 Function Table

Table 10-20 summarizes the I/O control selection functions of each Port 5 line.

Table 10-20 Port 5 Functions

Port Pin	I/O	Pin Functionality	Associated Reg./ I/O Line	Port I/O Control Select.	
				Reg./Bit Field	Value
P5.0	I	General-purpose input	P5_IN.P0	P5_IOCR0.PC0	$0XXX_B$
		ASC0 input	RXD0A		
		GPT120	T6EUDA		
		GPT121	T6EUDB		
	O	General-purpose output	P5_OUT.P0		$1X00_B$
		ASC0 output (sync. mode)	RXD0A		$1X01_B$
		GPTA0 output	OUT72		$1X10_B$
		GPTA1 output	OUT72		$1X11_B$
P5.1	I	General-purpose input	P5_IN.P1	P5_IOCR0.PC1	$0XXX_B$
	O	General-purpose output	P5_OUT.P1		$1X00_B$
		ASC0 output	TXD0		$1X01_B$
		GPTA0 output	OUT73		$1X10_B$
		GPTA1 output	OUT73		$1X11_B$
P5.2	I	General-purpose input	P5_IN.P2	P5_IOCR0.PC2	$0XXX_B$
		ASC1 input	RXD1A		
	O	General-purpose output	P5_OUT.P2		$1X00_B$
		ASC1 output (sync. mode)	RXD1A		$1X01_B$
		GPTA0 output	OUT74		$1X10_B$
		GPTA1 output	OUT74		$1X11_B$

Table 10-20 Port 5 Functions (cont'd)

Port Pin	I/O	Pin Functionality	Associated Reg./ I/O Line	Port I/O Control Select.	
				Reg./Bit Field	Value
P5.3	I	General-purpose input	P5_IN.P3	P5_IOCR0.PC3	$0XXX_B$
	O	General-purpose output	P5_OUT.P3		$1X00_B$
		ASC1 output	TXD1		$1X01_B$
		GPTA0 output	OUT75		$1X10_B$
		GPTA1 output	OUT75		$1X11_B$
P5.4	I	General-purpose input	P5_IN.P4	P5_IOCR4.PC4	$0XXX_B$
		CCU62	T13HRB		
		CCU63	CCPOS1A		
		GPT120	T2EUDB		
		GPT121	T2EUDA		
	O	General-purpose output	P5_OUT.P4		$1X00_B$
		MSC0 output	EN00		$1X01_B$
		MLI0 output	RREADY0B		$1X10_B$
		GPTA0 output	OUT76		$1X11_B$
P5.5	I	General-purpose input	P5_IN.P5	P5_IOCR4.PC5	$0XXX_B$
		MSC0 input	SDI0		
		CCU62	T12HRC		
		CCU62	T13HRC		
		CCU63	CCPOS2A		
		GPT120	T4EUDB		
		GPT121	T4EUDA		
	O	General-purpose output	P5_OUT.P5		$1X00_B$
		GPTA0 output	OUT77		$1X01_B$
		GPTA1 output	OUT77		$1X10_B$
		LTCA2 output	OUT101		$1X11_B$

Table 10-20 Port 5 Functions (cont'd)

Port Pin	I/O	Pin Functionality	Associated Reg./ I/O Line	Port I/O Control Select.	
				Reg./Bit Field	Value
P5.6	I	General-purpose input	P5_IN.P6	P5_IOCR4.PC6	$0XXX_B$
		CCU62	CC60INA		
		CCU63	CC60INB		
	O	General-purpose output	P5_OUT.P6		$1X00_B$
		MSC1 output	EN10		$1X01_B$
		MLI0 output	TVALID0B		$1X10_B$
		CCU62	CC60		$1X11_B$
P5.7	I	General-purpose input	P5_IN.P7	P5_IOCR4.PC7	$0XXX_B$
		MSC1 input	SDI1		
		CCU62	CC61INA		
		CCU63	CC61INB		
	O	General-purpose output	P5_OUT.P7		$1X00_B$
		GPTA0 output	OUT79		$1X01_B$
		GPTA1 output	OUT79		$1X10_B$
		CCU62	CC61		$1X11_B$
P5.8	I	General-purpose input	P5_IN.P8	P5_IOCR8.PC8	$0XXX_B$
		CCU62	CC62INA		
		CCU63	CC62INB		
	O	General-purpose output	P5_OUT.P8		$1X00_B$
		MSC0 Output	SON0		$1X01_B$
		GPTA0 output	OUT80		$1X10_B$
		CCU62	CC62		$1X11_B$
P5.9	I	General-purpose input	P5_IN.P9	P5_IOCR8.PC9	$0XXX_B$
	O	General-purpose output	P5_OUT.P9		$1X00_B$
		MSC0 Output	SOP0A		$1X01_B$
		GPTA0 output	OUT81		$1X10_B$
		CCU62	COUT60		$1X11_B$

Table 10-20 Port 5 Functions (cont'd)

Port Pin	I/O	Pin Functionality	Associated Reg./ I/O Line	Port I/O Control Select.	
				Reg./Bit Field	Value
P5.10	I	General-purpose input	P5_IN.P10	P5_IOCR8. PC10	$0XXX_B$
	O	General-purpose output	P5_OUT.P10		$1X00_B$
		MSC0 Output	FCLN0		$1X01_B$
		GPTA0 output	OUT82		$1X10_B$
		CCU62	COUT61		$1X11_B$
P5.11	I	General-purpose input	P5_IN.P11	P5_IOCR8. PC11	$0XXX_B$
	O	General-purpose output	P5_OUT.P11		$1X00_B$
		MSC0 Output	FCLP0A		$1X01_B$
		GPTA0 output	OUT83		$1X10_B$
		CCU62	COUT62		$1X11_B$
P5.12	I	General-purpose input	P5_IN.P12	P5_IOCR12. PC12	$0XXX_B$
	O	General-purpose output	P5_OUT.P12		$1X00_B$
		MSC1 Output	SON1		$1X01_B$
		GPTA0 output	OUT84		$1X10_B$
		GPTA1 output	OUT84		$1X11_B$
P5.13	I	General-purpose input	P5_IN.P13	P5_IOCR12. PC13	$0XXX_B$
	O	General-purpose output	P5_OUT.P13		$1X00_B$
		MSC1 Output	SOP1A		$1X01_B$
		GPTA0 output	OUT85		$1X10_B$
		GPTA1 output	OUT85		$1X11_B$
P5.14	I	General-purpose input	P5_IN.P14	P5_IOCR12. PC14	$0XXX_B$
	O	General-purpose output	P5_OUT.P14		$1X00_B$
		MSC1 Output	FCLN1		$1X01_B$
		GPTA0 output	OUT86		$1X10_B$
		GPTA1 output	OUT86		$1X11_B$

Table 10-20 Port 5 Functions (cont'd)

Port Pin	I/O	Pin Functionality	Associated Reg./ I/O Line	Port I/O Control Select.	
				Reg./Bit Field	Value
P5.15	I	General-purpose input	P5_IN.P15	P5_IOCR12. PC15	$0XXX_B$
	O	General-purpose output	P5_OUT.P15		$1X00_B$
		MSC1 Output	FCLP1A		$1X01_B$
		GPTA0 output	OUT87		$1X10_B$
		GPTA1 output	OUT87		$1X11_B$

10.9.3 Port 5 Registers

The following registers are available on Port 5:

Table 10-21 Port 5 Registers

Register Short Name	Register Long Name	Offset[1] Address	Description see
P5_OUT	Port 5 Output Register	0000_H	below[2]
P5_OMR	Port 5 Output Modification Register	0004_H	
P5_IOCR0	Port 5 Input/Output Control Register 0	0010_H	Page 10-11
P5_IOCR4	Port 5 Input/Output Control Register 4	0014_H	Page 10-13
P5_IOCR8	Port 5 Input/Output Control Register 8	0018_H	Page 10-13
P5_IOCR12	Port 5 Input/Output Control Register 12	$001C_H$	Page 10-13
P5_IN	Port 5 Input Register	0024_H	below[2]
P5_PDR0	Port 5 Pad Driver Mode 0 Register	0040_H	Page 10-18
P5_PDR1	Port 5 Pad Driver Mode 1 Register	0044_H	Page 10-19
P5_ESR	Port 5 Emergency Stop Register	0050_H	Page 10-24

1) The absolute addresses are calculated by adding the offset address to the module base address (see Table 10-4)

2) These registers are noted here in the Port 5 section because they differ from the general port register description given in Section 10.3.

10.9.3.1 Port 5 Output Register

The basic P5_OUT register functionality is described on Page 10-21.

10.9.3.2 Port 5 Output Modification Register

The basic P5_OMR register functionality is described on Page 10-22.

10.9.3.3 Port 5 Input Register

The basic P5_IN register functionality is described on Page 10-25.

10.9.3.4 Port 5 Emergency Stop Register

The basic P5_ESR register functionality is described on Page 10-24. At Port 5, all port lines P5.[15:0] have GPTA outputs and correspondent ESR lines.

10.10 Port 6

This section describes the Port 6 functionality in detail.

10.10.1 Port 6 Configuration

Port 6 is a 12-bit bi-directional general-purpose I/O port which can be used for the SSC1, ASC0/ASC1, or for the MultiCAN controller I/O lines.

10.10.2 Port 6 Function Table

Table 10-22 summarizes the I/O control selection functions of each Port 6 line.

Table 10-22 Port 6 Functions

Port Pin	I/O	Pin Functionality	Associated Reg./ I/O Line	Port I/O Control Select.	
				Reg./Bit Field	Value
P6.4	I	General-purpose input	P6_IN.P4	P6_IOCR4.PC4	$0XXX_B$
		SSC1 input (slave mode)	MTSR1		
		SSC Guardian 1 Master Receive Input (Master Mode)	MRSTG1		
	O	General-purpose output	P6_OUT.P4		$1X00_B$
		SSC1 output (master mode)	MTSR1		$1X01_B$
		Reserved	–		$1X10_B$
		Reserved	–		$1X11_B$
P6.5	I	General-purpose input	P6_IN.P5	P6_IOCR4.PC5	$0XXX_B$
		SSC1 input (master mode)	MRST1		
	O	General-purpose output	P6_OUT.P5		$1X00_B$
		SSC1 output (slave mode)	MRST1		$1X01_B$
		Reserved	–		$1X10_B$
		Reserved	–		$1X11_B$
P6.6	I	General-purpose input	P6_IN.P6	P6_IOCR4.PC6	$0XXX_B$
		SSC1 input (slave mode)	SCLK1		
	O	General-purpose output	P6_OUT.P6		$1X00_B$
		SSC1 output (master mode)	SCLK1		$1X01_B$
		Reserved	–		$1X10_B$
		Reserved	–		$1X11_B$

Table 10-22 Port 6 Functions (cont'd)

Port Pin	I/O	Pin Functionality	Associated Reg./ I/O Line	Port I/O Control Select.	
				Reg./Bit Field	Value
P6.7	I	General-purpose input	P6_IN.P7	P6_IOCR4.PC7	$0XXX_B$
		SSC1 input	$\overline{SLSI1}$		
	O	General-purpose output	P6_OUT.P7		$1X00_B$
		GPT120	T6OFL		$1X01_B$
		Reserved	–		$1X10_B$
		Reserved	–		$1X11_B$
P6.8	I	General-purpose input	P6_IN.P8	P6_IOCR8.PC8	$0XXX_B$
		CAN node 0 rec. input 0 CAN node 3 rec. input 1	RXDCAN0		
		ASC0 input	RXD0B		
		GPT120	CAPINB		
		GPT121	CAPINA		
	O	General-purpose output	P6_OUT.P8		$1X00_B$
		Reserved	–		$1X01_B$
		ASC0 output (sync. mode)	RXD0B		$1X10_B$
		Reserved	–		$1X11_B$
P6.9	I	General-purpose input	P6_IN.P9	P6_IOCR8.PC9	$0XXX_B$
	O	General-purpose output	P6_OUT.P9		$1X00_B$
		CAN node 0 output	TXDCAN0		$1X01_B$
		ASC0 output	TXD0		$1X10_B$
		GPT121	T6OFL		$1X11_B$
P6.10	I	General-purpose input	P6_IN.P10	P6_IOCR8. PC10	$0XXX_B$
		CAN node 1 rec. input 0 CAN node 0 rec. input 1	RXDCAN1		
		ASC1 input	RXD1B		
	O	General-purpose output	P6_OUT.P10		$1X00_B$
		Reserved	–		$1X01_B$
		ASC1 output (sync. mode)	RXD1B		$1X10_B$
		E-Ray output	TXENA		$1X11_B$

Table 10-22 Port 6 Functions (cont'd)

Port Pin	I/O	Pin Functionality	Associated Reg./ I/O Line	Port I/O Control Select.	
				Reg./Bit Field	Value
P6.11	I	General-purpose input	P6_IN.P11	P6_IOCR8. PC11	$0XXX_B$
	O	General-purpose output	P6_OUT.P11		$1X00_B$
		CAN node 1 output	TXDCAN1		$1X01_B$
		ASC1 output	TXD1		$1X10_B$
		E-Ray output	TXENB		$1X11_B$
P6.12	I	General-purpose input	P6_IN.P12	P6_IOCR12. PC12	$0XXX_B$
		CAN node 2 rec. input 0 CAN node 1 rec. input 1	RXDCAN2		
		E-Ray input	RXDA1		
	O	General-purpose output	P6_OUT.P12		$1X00_B$
		Reserved	–		$1X01_B$
		Reserved	–		$1X10_B$
		CCU60	COUT61		$1X11_B$
P6.13	I	General-purpose input	P6_IN.P13	P6_IOCR12. PC13	$0XXX_B$
	O	General-purpose output	P6_OUT.P13		$1X00_B$
		CAN node 2 output	TXDCAN2		$1X01_B$
		E-Ray output	TXDA		$1X10_B$
		CCU60	COUT62		$1X11_B$
P6.14	I	General-purpose input	P6_IN.P14	P6_IOCR12. PC14	$0XXX_B$
		CAN node 3 rec. input 0 CAN node 2 rec. input 1	RXDCAN3		
		E-Ray Input	RXDB1		
	O	General-purpose output	P6_OUT.P14		$1X00_B$
		Reserved	–		$1X01_B$
		Reserved	–		$1X10_B$
		CCU60	COUT63		$1X11_B$

Table 10-22 Port 6 Functions (cont'd)

Port Pin	I/O	Pin Functionality	Associated Reg./ I/O Line	Port I/O Control Select.	
				Reg./Bit Field	Value
P6.15	I	General-purpose input	P6_IN.P15	P6_IOCR12. PC15	$0XXX_B$
		CCU60	CC60INB		
		CCU61	CC60INA		
	O	General-purpose output	P6_OUT.P15		$1X00_B$
		CAN node 3 output	TXDCAN3		$1X01_B$
		E-Ray output	TXDB		$1X10_B$
		CCU61	CC60		$1X11_B$

10.10.3 Port 6 Registers

The following registers are available on Port 6:

Table 10-23 Port 6 Registers

Register Short Name	Register Long Name	Offset[1] Address	Description see
P6_OUT	Port 6 Output Register	0000_H	below[2]
P6_OMR	Port 6 Output Modification Register	0004_H	
P6_IOCR4	Port 6 Input/Output Control Register 4	0014_H	Page 10-12
P6_IOCR8	Port 6 Input/Output Control Register 8	0018_H	Page 10-13
P6_IOCR12	Port 6 Input/Output Control Register 12	$001C_H$	Page 10-14
P6_IN	Port 6 Input Register	0024_H	below[2]
P6_PDR0	Port 6 Pad Driver Mode 0 Register	0040_H	Page 10-76
P6_PDR1	Port 6 Pad Driver Mode 1 Register	0044_H	Page 10-19

1) The absolute addresses are calculated by adding the offset address to the module base address (see Table 10-4)

2) These registers are listed and noted here in the Port 6 section because they differ from the general port register description given in Section 10.3.

10.10.3.1 Port 6 Output Register

The basic P6_OUT register functionality is described on Page 10-21. Port lines P6.[3:0] are not connected to port lines. Therefore, reading the P6_OUT bits P[3:0] returns the value that was last written (0 after reset). These bits can be also set/reset by the corresponding P6_OMR bits.

10.10.3.2 Port 6 Output Modification Register

The basic P6_OMR register functionality is described on Page 10-22. Port lines P6.[3:0] are not available. Therefore, they are not implemented. These bits should always be written with 0.

10.10.3.3 Port 6 Input Register

The basic P6_IN register functionality is described on Page 10-25. Port lines P6.[3:0] are not available. Therefore, the P6_IN bits P[3:0] are always read as 0.

10.10.3.4 Port 6 Pad Driver Mode 0 Register

The basic P6_PDR0 register functionality is described on Page 10-18. However, port lines P6.[3:0] are not available.

P6_PDR0
Port 6 Pad Driver Mode 0 Register (40_H) Reset Value: 0000 0000$_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0		**PD7**		**0**		**PD6**		**0**		**PD5**		**0**		**PD4**	
r		rw		r		rw		r		rw		r		rw	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0		**PD3**		**0**		**PD2**		**0**		**PD1**		**0**		**PD0**	
r		rw		r		rw		r		rw		r		rw	

Field	Bits	Type	Description
PD0	[2:0]	rw	**Reserved** Read as 000_B after reset; returns value that was written.
PD1	[6:4]	rw	**Reserved** Read as 000_B after reset; returns value that was written.
PD2	[10:8]	rw	**Reserved** Read as 000_B after reset; returns value that was written.
PD3	[14:12]	rw	**Reserved** Read as 000_B after reset; returns value that was written.
PD4	[18:16]	rw	**Pad Driver Mode for P6.4**
PD5	[22:20]	rw	**Pad Driver Mode for P6.5**
PD6	[26:24]	rw	**Pad Driver Mode for P6.6**
PD7	[30:28]	rw	**Pad Driver Mode for P6.7**
0	3, 7, 11, 15, 19, 23, 27, 31	r	**Reserved** Read as 0; should be written with 0.

10.11 Port 7

This section describes the Port 7 functionality in detail.

10.11.1 Port 7 Configuration

Port 7 is an 8-bit bi-directional general-purpose I/O port that can be used for the external trigger input lines REQ[7:4] or for the ADC0/ADC1 external multiplexer control output lines.

10.11.2 Port 7 Function Table

Table 10-24 summarizes the I/O control selection functions of each Port 7 line.

Table 10-24 Port 7 Functions

Port Pin	I/O	Pin Functionality	Associated Reg./ I/O Line	Port I/O Control Select.	
				Reg./Bit Field	Value
P7.0	I	General-purpose input	P7_IN.P0	P7_IOCR0.PC0	$0XXX_B$
		SCU input	REQ4		
		SSC3 input (Slave Mode)	MRST3		
	O	General-purpose output	P7_OUT.P0		$1X00_B$
		ADC2 output	AD2EMUX2		$1X01_B$
		SSC3 output (Master Mode)	MRST3		$1X10_B$
		Reserved	–		$1X11_B$
P7.1	I	General-purpose input	P7_IN.P1	P7_IOCR0.PC1	$0XXX_B$
		SCU input	REQ5		
		SSC3 input (Master Mode)	MTSR3		
		SSC Guardian 3 Master Receive Input B (Master Mode)	MRSTG3B		
	O	General-purpose output	P7_OUT.P1		$1X00_B$
		ADC0 output	AD0EMUX2		$1X01_B$
		SSC3 output (Slave Mode)	MTSR3		$1X10_B$
		Reserved	–		$1X11_B$
P7.2	I	General-purpose input	P7_IN.P2	P7_IOCR0.PC2	$0XXX_B$
		SSC3 input	SCLK3		
	O	General-purpose output	P7_OUT.P2		$1X00_B$
		ADC0 output	AD0EMUX0		$1X01_B$
		SSC3 output	SCLK3		$1X10_B$
		Reserved	–		$1X11_B$

Table 10-24 Port 7 Functions (cont'd)

Port Pin	I/O	Pin Functionality	Associated Reg./ I/O Line	Port I/O Control Select.	
				Reg./Bit Field	Value
P7.3	I	General-purpose input	P7_IN.P3	P7_IOCR0.PC3	$0XXX_B$
	O	General-purpose output	P7_OUT.P3		$1X00_B$
		ADC0 output	AD0EMUX1		$1X01_B$
		SSC3 output	SLSO30		$1X10_B$
		Reserved	–		$1X11_B$
P7.4	I	General-purpose input	P7_IN.P4	P7_IOCR4.PC4	$0XXX_B$
		SCU input	REQ6		
	O	General-purpose output	P7_OUT.P4		$1X00_B$
		ADC2 output	AD2EMUX0		$1X01_B$
		SSC3 output	SLSO31		$1X10_B$
		Reserved	–		$1X11_B$
P7.5	I	General-purpose input	P7_IN.P5	P7_IOCR4.PC5	$0XXX_B$
		SCU input	REQ7		
	O	General-purpose output	P7_OUT.P5		$1X00_B$
		ADC2 output	AD2EMUX1		$1X01_B$
		SSC3 output	SLSO32		$1X10_B$
		Reserved	–		$1X11_B$
P7.6	I	General-purpose input	P7_IN.P6	P7_IOCR4.PC6	$0XXX_B$
	O	General-purpose output	P7_OUT.P6		$1X00_B$
		ADC1 output	AD1EMUX0		$1X01_B$
		SSC3 output	SLSO33		$1X10_B$
		Reserved	–		$1X11_B$
P7.7	I	General-purpose input	P7_IN.P7	P7_IOCR4.PC7	$0XXX_B$
	O	General-purpose output	P7_OUT.P7		$1X00_B$
		ADC1 output	AD1EMUX1		$1X01_B$
		SSC3 output	SLSO34		$1X10_B$
		Reserved	–		$1X11_B$

10.11.3 Port 7 Registers

The following registers are available on Port 7:

Table 10-25 Port 7 Registers

Register Short Name	Register Long Name	Offset[1] Address	Description see
P7_OUT	Port 7 Output Register	0000_H	below[2]
P7_OMR	Port 7 Output Modification Register	0004_H	
P7_IOCR0	Port 7 Input/Output Control Register 0	0010_H	Page 10-11
P7_IOCR4	Port 7 Input/Output Control Register 4	0014_H	Page 10-12
P7_IN	Port 7 Input Register	0024_H	below[2]
P7_PDR0	Port 7 Pad Driver Mode 0 Register	0040_H	Page 10-18

1) The absolute addresses are calculated by adding the offset address to the module base address (see Table 10-4)

2) These registers are listed and noted here in the Port 7 section because they differ from the general port register description given in Section 10.3.

10.11.3.1 Port 7 Output Register

The basic P7_OUT register functionality is described on Page 10-21. Port lines P7.[15:8] are not available. Therefore, the P7_OUT bits P[15:8] should be written with 0, and are always read as 0.

10.11.3.2 Port 7 Output Modification Register

The basic P7_OMR register functionality is described on Page 10-22. Port lines P7.[15:8] are not available. Therefore, the P7_OMR bits PS[15:8] and PR[15:8] are not implemented. These bits should always be written with 0.

10.11.3.3 Port 7 Input Register

The basic P7_IN register functionality is described on Page 10-25. Port lines P7.[15:8] are not available. Therefore, the P7_IN bits P[15:8] are always read as 0.

10.12 Port 8

This section describes the Port 8 functionality in detail.

10.12.1 Port 8 Configuration

Port 8 is an 8-bit bi-directional general-purpose I/O port which can be used for the MLI1 interface lines or for the GPTA0/GPTA1 I/O lines.

10.12.2 Port 8 Function Table

Table 10-26 summarizes the I/O control selection functions of each Port 8 line.

Table 10-26 Port 8 Functions

Port Pin	I/O	Pin Functionality	Associated Reg./ I/O Line	Port I/O Control Select.	
				Reg./Bit Field	Value
P8.0	I	General-purpose input	P8_IN.P0	P8_IOCR0.PC0	$0XXX_B$
		GPTA0/GPTA1 input	IN40		
		SENT digital input	SENT0		
	O	General-purpose output	P8_OUT.P0		$1X00_B$
		GPTA0 output	OUT40		$1X01_B$
		CCU61	COUT62		$1X10_B$
		MLI1 output	TCLK1		$1X11_B$
P8.1	I	General-purpose input	P8_IN.P1	P8_IOCR0.PC1	$0XXX_B$
		GPTA0/GPTA1 input	IN41		
		MLI1 input	TREADY1A		
		SENT digital input	SENT1		
		CCU60	CC61INA		
		CCU61	CC61INB		
	O	General-purpose output	P8_OUT.P1		$1X00_B$
		GPTA0 output	OUT41		$1X01_B$
		CCU60	CC61		$1X10_B$
		SENT digital output[1)]	SENT1		$1X11_B$
P8.2	I	General-purpose input	P8_IN.P2	P8_IOCR0.PC2	$0XXX_B$
		GPTA0/GPTA1 input	IN42		
		SENT digital input	SENT2		
		GPT120	CAPINA		
		GPT121	CAPINB		
	O	General-purpose output	P8_OUT.P2		$1X00_B$
		CCU61	COUT63		$1X01_B$
		GPTA1 output	OUT42		$1X10_B$
		MLI1 output	TVALID1A		$1X11_B$

Table 10-26 Port 8 Functions (cont'd)

Port Pin	I/O	Pin Functionality	Associated Reg./ I/O Line	Port I/O Control Select.	
				Reg./Bit Field	Value
P8.3	I	General-purpose input	P8_IN.P3	P8_IOCR0.PC3	$0XXX_B$
		GPTA0/GPTA1 input	IN43		
		SENT digital input	SENT3		
		CCU60	CC62INA		
		CCU61	CC62INB		
	O	General-purpose output	P8_OUT.P3		$1X00_B$
		GPTA0 output	OUT43		$1X01_B$
		CCU60	CC62		$1X10_B$
		MLI1 output	TDATA1		$1X11_B$
P8.4	I	General-purpose input	P8_IN.P4	P8_IOCR4.PC4	$0XXX_B$
		GPTA0/GPTA1 input	IN44		
		MLI1 input	RCLK1A		
		SENT digital input	SENT4		
		CCU60	CC62INB		
		CCU61	CC62INA		
	O	General-purpose output	P8_OUT.P4		$1X00_B$
		GPTA0 output	OUT44		$1X01_B$
		CCU61	CC62		$1X10_B$
		GPT121	T3OUT		$1X11_B$

Table 10-26 Port 8 Functions (cont'd)

Port Pin	I/O	Pin Functionality	Associated Reg./ I/O Line	Port I/O Control Select.	
				Reg./Bit Field	Value
P8.5	I	General-purpose input	P8_IN.P5	P8_IOCR4.PC5	$0XXX_B$
		GPTA0/GPTA1 input	IN45		
		SENT digital input	SENT5		
		CCU60	$\overline{\text{CTRAPA}}$		
		CCU60	CC60INC		
		CCU61	T12HRE		
		CCU61	CC61INC		
		CCU62	$\overline{\text{CTRAPB}}$		
	O	General-purpose output	P8_OUT.P5		$1X00_B$
		GPTA0 output	OUT45		$1X01_B$
		GPTA1 output	OUT45		$1X10_B$
		MLI1 output	RREADY1A		$1X11_B$
P8.6	I	General-purpose input	P8_IN.P6	P8_IOCR4.PC6	$0XXX_B$
		GPTA0/GPTA1 input	IN46		
		MLI1 input	RVALID1A		
		SENT digital input	SENT6		
	O	General-purpose output	P8_OUT.P6		$1X00_B$
		GPTA0 output	OUT46		$1X01_B$
		CCU61	COUT60		$1X10_B$
		GPT120	T6OUT		$1X11_B$
P8.7	I	General-purpose input	P8_IN.P7	P8_IOCR4.PC7	$0XXX_B$
		GPTA0/GPTA1 input	IN47		
		MLI1 input	RDATA1A		
		SENT digital input	SENT7		
	O	General-purpose output	P8_OUT.P7		$1X00_B$
		GPTA0 output	OUT47		$1X01_B$
		CCU61	COUT61		$1X10_B$
		GPT121	T6OUT		$1X11_B$

1) The PCx should not be configured as push-pull. Only open-drain mode is applicable.

10.12.3 Port 8 Register

The following registers are available on Port 8:

Table 10-27 Port 8 Registers

Register Short Name	Register Long Name	Offset[1] Address	Description see
P8_OUT	Port 8 Output Register	0000_H	below[2]
P8_OMR	Port 8 Output Modification Register	0004_H	
P8_IOCR0	Port 8 Input/Output Control Register 0	0010_H	Page 10-11
P8_IOCR4	Port 8 Input/Output Control Register 4	0014_H	Page 10-12
P8_IN	Port 8 Input Register	0024_H	below[2]
P8_PDR0	Port 8 Pad Driver Mode 0 Register	0040_H	Page 10-18
P8_ESR	Port 8 Emergency Stop Register	0050_H	below[2]

1) The absolute addresses are calculated by adding the offset address to the module base address (see Table 10-4)

2) These registers are listed here in the Port 8 section because they differ from the general port register description given in Section 10.3.

10.12.3.1 Port 8 Output Register

The basic P8_OUT register functionality is described on Page 10-21. Port lines P8.[15:8] are not available. Therefore, the P8_OUT bits P[15:8] should be written with 0 and are always read as 0.

10.12.3.2 Port 8 Output Modification Register

The basic P8_OMR register functionality is described on Page 10-22. Port lines P8.[15:8] are not available. Therefore, the P8_OMR bits PS[15:8] and PR[15:8] are not implemented. These bits should always be written with 0.

10.12.3.3 Port 8 Input Register

The basic P8_IN register functionality is described on Page 10-25. Port lines P8.[15:8] are not available. Therefore, the P8_IN bits P[15:8] are always read as 0.

10.12.3.4 Port 8 Emergency Stop Register

The basic P8_ESR register functionality is described on Page 10-24. At Port 8, only port lines P8.[7:0] are implemented. Therefore, the P8_ESR bits EN[15:8] are not implemented. They are always read as 0 and should be written with 0.

10.13 Port 9

This section describes the Port 9 functionality in detail.

10.13.1 Port 9 Configuration

Port 9 is a 15-bit bi-directional general-purpose I/O port which can be used for the MSC0/MSC1 interface output lines or for the GPTA0/GPTA1 I/O lines.

10.13.2 Port 9 Function Table

Table 10-28 summarizes the I/O control selection functions of each Port 9 line.

Table 10-28 Port 9 Functions

Port Pin	I/O	Pin Functionality	Associated Reg./ I/O Line	Port I/O Control Select.	
				Reg./Bit Field	Value
P9.0	I	General-purpose input	P9_IN.P0	P9_IOCR0.PC0	$0XXX_B$
		GPTA0/GPTA1 input	IN48		
	O	General-purpose output	P9_OUT.P0		$1X00_B$
		CCU62	COUT63		$1X01_B$
		GPTA1 output	OUT48		$1X10_B$
		MSC1 output	EN12		$1X11_B$
P9.1	I	General-purpose input	P9_IN.P1	P9_IOCR0.PC1	$0XXX_B$
		GPTA0/GPTA1 input	IN49		
		CCU62	CC60INB		
		CCU63	CC60INA		
	O	General-purpose output	P9_OUT.P1		$1X00_B$
		CCU63	CC60		$1X01_B$
		GPTA1 output	OUT49		$1X10_B$
		MSC1 output	EN11		$1X11_B$
P9.2	I	General-purpose input	P9_IN.P2	P9_IOCR0.PC2	$0XXX_B$
		GPTA0/GPTA1 input	IN50		
		CCU62	CC61INB		
		CCU63	CC61INA		
	O	General-purpose output	P9_OUT.P2		$1X00_B$
		CCU63	CC61		$1X01_B$
		GPTA1 output	OUT50		$1X10_B$
		MSC1 output	SOP1B		$1X11_B$

Table 10-28 Port 9 Functions (cont'd)

Port Pin	I/O	Pin Functionality	Associated Reg./ I/O Line	Port I/O Control Select.	
				Reg./Bit Field	Value
P9.3	I	General-purpose input	P9_IN.P3	P9_IOCR0.PC3	$0XXX_B$
		GPTA0/GPTA1 input	IN51		
		CCU62	CC62INB		
		CCU63	CC62INA		
	O	General-purpose output	P9_OUT.P3		$1X00_B$
		CCU63	CC62		$1X01_B$
		GPTA1 output	OUT51		$1X10_B$
		MSC1 output	FCLP1B		$1X11_B$
P9.4	I	General-purpose input	P9_IN.P4	P9_IOCR4.PC4	$0XXX_B$
		GPTA0/GPTA1 input	IN52		
	O	General-purpose output	P9_OUT.P4		$1X00_B$
		CCU63	COUT60		$1X01_B$
		GPTA1 output	OUT52		$1X10_B$
		MSC0 output	EN03		$1X11_B$
P9.5	I	General-purpose input	P9_IN.P5	P9_IOCR4.PC5	$0XXX_B$
		GPTA0/GPTA1 input	IN53		
		SENT digital input	SENT1		
	O	General-purpose output	P9_OUT.P5		$1X00_B$
		CCU63	COUT61		$1X01_B$
		GPTA1 output	OUT53		$1X10_B$
		MSC0 output	EN02		$1X11_B$
P9.6	I	General-purpose input	P9_IN.P6	P9_IOCR4.PC6	$0XXX_B$
		GPTA0/GPTA1 input	IN54		
		SENT digital input	SENT3		
	O	General-purpose output	P9_OUT.P6		$1X00_B$
		GPTA0 output	OUT54		$1X01_B$
		SENT digital output[1)]	SENT3		$1X10_B$
		MSC0 output	EN01		$1X11_B$

Table 10-28 Port 9 Functions (cont'd)

Port Pin	I/O	Pin Functionality	Associated Reg./ I/O Line	Port I/O Control Select.	
				Reg./Bit Field	Value
P9.7	I	General-purpose input	P9_IN.P7	P9_IOCR4.PC7	$0XXX_B$
		GPTA0/GPTA1 input	IN55		
		SENT digital input	SENT4		
	O	General-purpose output	P9_OUT.P7		$1X00_B$
		GPTA0 output	OUT55		$1X01_B$
		SENT digital output[1)]	SENT4		$1X10_B$
		MSC0 output	SOP0B		$1X11_B$
P9.8	I	General-purpose input	P9_IN.P8	P9_IOCR8.PC8	$0XXX_B$
		SENT digital input	SENT6		
	O	General-purpose output	P9_OUT.P8		$1X00_B$
		CCU63	COUT62		$1X01_B$
		SENT digital output[1)]	SENT6		$1X10_B$
		MSC0 output	FCLP0B		$1X11_B$
P9.9	I	General-purpose input	P9_IN.P9	P9_IOCR8.PC9	$0XXX_B$
		SENT digital input	SENT0		
	O	General-purpose output	P9_OUT.P9		$1X00_B$
		Reserved	–		$1X01_B$
		SENT digital output[1)]	SENT0		$1X10_B$
		Reserved	–		$1X11_B$
P9.10	I	General-purpose input	P9_IN.P10	P9_IOCR8.PC10	$0XXX_B$
		SCU	EMGSTOP		
		SENT digital input	SENT7		
	O	General-purpose output	P9_OUT.P10		$1X00_B$
		CCU63	COUT63		$1X01_B$
		SENT digital output[1)]	SENT7		$1X10_B$
		Reserved	–		$1X11_B$

Table 10-28 Port 9 Functions (cont'd)

Port Pin	I/O	Pin Functionality	Associated Reg./ I/O Line	Port I/O Control Select.	
				Reg./Bit Field	Value
P9.11	I	General-purpose input	P9_IN.P11	P9_IOCR8.PC11	$0XXX_B$
		SENT digital input	SENT2		
	O	General-purpose output	P9_OUT.P11		$1X00_B$
		Reserved	–		$1X01_B$
		SENT digital output[1)]	SENT2		$1X10_B$
		Reserved	–		$1X11_B$
P9.12	I	General-purpose input	P9_IN.P12	P9_IOCR12.PC12	$0XXX_B$
		SENT digital input	SENT5		
	O	General-purpose output	P9_OUT.P12		$1X00_B$
		Reserved	–		$1X01_B$
		SENT digital output[1)]	SENT5		$1X10_B$
		Reserved	–		$1X11_B$
P9.13	I	General-purpose input	P9_IN.P13	P9_IOCR12.PC13	$0XXX_B$
		OCDS	$\overline{\text{BRKIN}}$		
		TTCAN input	ECTT1		
	O	General-purpose output	P9_OUT.P13		$1X00_B$
		Reserved	–		$1X01_B$
		Reserved	–		$1X10_B$
		Reserved	–		$1X11_B$
	HW_OUT	OCDS;SEN	$\overline{\text{BRKOUT}}$		SDIR

Table 10-28 Port 9 Functions (cont'd)

Port Pin	I/O	Pin Functionality	Associated Reg./ I/O Line	Port I/O Control Select.	
				Reg./Bit Field	Value
P9.14	I	General-purpose input	P9_IN.P14	P9_IOCR12.PC14	$0XXX_B$
		OCDS	$\overline{BRKIN}$		
		TTCAN input	ECTT2		
		SCU input	REQ15		
	O	General-purpose output	P9_OUT.P14		$1X00_B$
		Reserved	–		$1X01_B$
		Reserved	–		$1X10_B$
		Reserved	–		$1X11_B$
	HW_OUT	OCDS;SEN	$\overline{BRKOUT}$		SDIR

1) The PCx should not be configured as push-pull. Only open-drain mode is applicable.

10.13.3 Port 9 Registers

The following registers are available on Port 9:

Table 10-29 Port 9 Registers

Register Short Name	Register Long Name	Offset[1] Address	Description see
P9_OUT	Port 9 Output Register	0000_H	below[2]
P9_OMR	Port 9 Output Modification Register	0004_H	
P9_IOCR0	Port 9 Input/Output Control Register 0	0010_H	Page 10-11
P9_IOCR4	Port 9 Input/Output Control Register 4	0014_H	Page 10-12
P9_IOCR8	Port 9 Input/Output Control Register 8	0018_H	Page 10-13
P9_IOCR12	Port 9 Input/Output Control Register 12	$001C_H$	Page 10-93[2]
P9_IN	Port 9 Input Register	0024_H	Page 10-93[2]
P9_PDR0	Port 9 Pad Driver Mode 0 Register	0040_H	Page 10-18
P9_PDR1	Port 9 Pad Driver Mode 1 Register	0044_H	Page 10-94
P9_ESR	Port 9 Emergency Stop Register	0050_H	Page 10-95[2]

1) The absolute addresses are calculated by adding the offset address to the module base address (see Table 10-4)

2) These registers are listed and noted here in the Port 9 section because they differ from the general port register description given in Section 10.3.

10.13.3.1 Port 9 Output Register

The basic P9_OUT register functionality is described on Page 10-21. Port line P9.15 is not available. Therefore, the P9_OUT bit 15 should be written with 0 and is always read as 0.

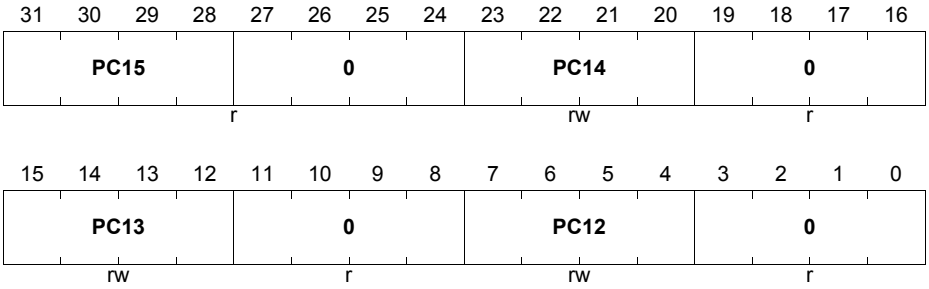
10.13.3.2 Port 9 Output Modification Register

The basic P9_OMR register functionality is described on Page 10-22. Port line P9.15 is not available. Therefore, the P9_OMR bits PS15 and PR15 are not implemented. These bits should always be written with 0.

10.13.3.3 Port 9 Input/Output Control Register 8

P9_IOCR12
Port 9 Input/Output Control Register 12

($1C_H$) **Reset Value: 2020 2020_H**



Field	Bits	Type	Description
PC12	[7:4]	rw	**Port Control for P9.12** This bit field determines the P9.12 functionality.
PC13	[15:12]	rw	**Port Control for P9.13** This bit field determines the P9.13 functionality.
PC14	[23:20]	rw	**Port Control for P9.14** This bit field determines the P9.14 functionality.
PC15	[31:28]	rw	**Reserved** Read as 0010_B after reset; returns value that was written.
0	[3:0], [11:8], [19:16], [27:24]	r	**Reserved** Read as 0; should be written with 0.

10.13.3.4 Port 9 Input Register

The basic P9_IN register functionality is described on **Page 10-25**. Port line P9.15 is not available. Therefore, the P9_IN bit P9.15 is always read as 0.

10.13.3.5 Port 9 Pad Driver Mode 1 Register

The basic P9_PDR1 register functionality is described on Page 10-18. However, port lines P9.15 is not available. Therefore, bit fields PD7 in P9_PDR1 is always read as 0 and should be written with 0.

10.13.3.6 Port 9 Pad Driver Mode 1 Register

The basic P9_PDR1 register functionality is described on Page 10-18. However, port lines P9.15 is not available.

P9_PDR1
Port 9 Pad Driver Mode 1 Register (44_H) Reset Value: 0000 0000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	PD15			0	PD14			0	PD13			0	PD12		
r	rw			r	rw			r	rw			r	rw		

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	PD11			0	PD10			0	PD9			0	PD8		
r	rw			r	rw			r	rw			r	rw		

Field	Bits	Type	Description
PD8	[2:0]	rw	**Pad Driver Mode for P9.8**
PD9	[6:4]	rw	**Pad Driver Mode for P9.9**
PD10	[10:8]	rw	**Pad Driver Mode for P9.10**
PD11	[14:12]	rw	**Pad Driver Mode for P9.11**
PD12	[18:16]	rw	**Pad Driver Mode for P9.12**
PD13	[22:20]	rw	**Pad Driver Mode for P9.13**
PD14	[26:24]	rw	**Pad Driver Mode for P9.14**
PD15	[30:28]	rw	**Reserved** Read as 000_B after reset; returns value that was written.
0	3, 7, 11, 15, 19, 23, 27, 31	r	**Reserved** Read as 0; should be written with 0.

10.13.3.7 Port 9 Emergency Stop Register

The basic P9_ESR register functionality is described on Page 10-24. At Port 9, only port lines P9.[7:0] have GPTA outputs. Therefore, the P9_ESR bits EN[15:8] are not implemented. They are always read as 0 and should be written with 0.

10.14 Port 10

This section describes the Port 10 functionality in detail.

10.14.1 Port 10 Configuration

Port 10 is a 6-bit port.

10.14.2 Port 10 Function Table

Table 10-26 summarizes the I/O control selection functions of each line.

Table 10-30 Port 10 Functions

Port Pin	I/O	Pin Functionality	Associated Reg./I/O Line	Port I/O Control Select.	
				Reg./Bit Field	Value
P10.0	I	General-purpose input	P10_IN.P0	P10_IOCR0 .PC0	$0XXX_B$
		SSC0 Input, master mode	MRST0		
	O	General-purpose output	P10_OUT.P0		$1X00_B$
		SSC0 Output, slave mode	MRST0		$1X01_B$
		Reserved	–		$1X10_B$
		Reserved	–		$1X11_B$
P10.1	I	General-purpose input	P10_IN.P1	P10_IOCR0 .PC1	$0XXX_B$
		SSC0 Input, slave mode	MTSR0		
		SSC Guardian 0 Master Receive Input (Master Mode)	MRSTG0		
	O	General-purpose output	–		$1X00_B$
		SSC0 Output, master mode	MTSR0		$1X01_B$
		Reserved	–		$1X10_B$
		Reserved[1)]	–		$1X11_B$

Table 10-30 Port 10 Functions (cont'd)

Port Pin	I/O	Pin Functionality	Associated Reg./I/O Line	Port I/O Control Select.	
				Reg./Bit Field	Value
P10.2	I	General-purpose input	P10_IN.P2	P10_IOCR0 .PC2	$0XXX_B$
		SSC0 Input	$\overline{SLSI0}$		
	O	General-purpose output	P10_OUT.P2		$1X00_B$
		Reserved	–		$1X01_B$
		Reserved	–		$1X10_B$
		Reserved	–		$1X11_B$
P10.3	I	General-purpose input	P10_IN.P3	P10_IOCR0 .PC3	$0XXX_B$
		SSC0 Input	SCLK0		
	O	General-purpose output	P10_OUT.P3		$1X00_B$
		SSC0 Output	SCLK0		$1X01_B$
		Reserved	–		$1X10_B$
		Reserved	–		$1X11_B$
P10.4	I	General-purpose input	P10_IN.P4	P10_IOCR4 .PC4	$0XXX_B$
	O	General-purpose output	P10_OUT.P4		$1X00_B$
		SSC0 Output	SLSO0		$1X01_B$
		Reserved	–		$1X10_B$
		Reserved	–		$1X11_B$
P10.5	I	General-purpose input	P10_IN.P5	P10_IOCR4 .PC5	$0XXX_B$
	O	General-purpose output	P10_OUT.P5		$1X00_B$
		SSC0 Output	SLSO1		$1X01_B$
		Reserved	–		$1X10_B$
		Reserved	–		$1X11_B$

1) The port I/O control values P10_IOCRx.Py that are assigned to this reserved alternate output control selection should not be used.

10.14.3 Port 10 Registers

The following registers are available on Port 10:

Table 10-31 Port 10 Registers

Register Short Name	Register Long Name	Offset Address[1)]	Description see
P10_OUT	Port 10 Output Register	0000_H	Page 10-98
P10_OMR	Port 10 Output Modification Register	0004_H	Page 10-98
P10_IOCR0	Port 10 Input/Output Control Register 0	0010_H	Page 10-11
P10_IOCR4	Port 10 Input/Output Control Register 4	0014_H	Page 10-99[2)]
P10_IN	Port 10 Input Register	0024_H	Page 10-99[2)]
P10_PDR0	Port 10 Pad Driver Mode 0 Register	0040_H	Page 10-100

1) The absolute addresses are calculated by adding the offset address to the module base address (see Table 10-4)

2) This register is listed here in the Port 10 section because it differs from the general port register description given in Section 10.3.

Note: Register P10_IN makes it possible to read the actual logic levels of the Port 10 inputs.

10.14.3.1 Port 10 Output Register

The basic P10_OUT register functionality is described on Page 10-21. Port lines P10.[15:6] are not connected to port lines. Therefore, reading the P10_OUT bits P[15:6] returns the value that was last written (0 after reset). These bits can be also set/reset by the corresponding P10_OMR bits.

10.14.3.2 Port 10 Output Modification Register

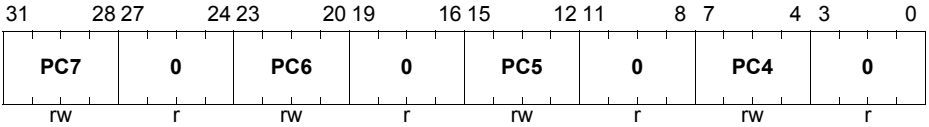
The basic P10_OMR register functionality is described on Page 10-22. However, port lines P10.[15:6] are not available. Therefore, the P10_OMR bits PS[15:6] and PR[15:6] have no direct effect on port lines but only on register bits P10_OUT.P[15:6].

10.14.3.3 Port 10 Input/Output Control Register 4

Port lines P10.[15:6] are not available. Therefore, the PC6 and PC7 bit fields in register P10_IOCR4 are not connected to any port lines.

P10_IOCR4
Port 10 Input/Output Control Register 4

(14_H) **Reset Value: 2020 2020_H**



Field	Bits	Type	Description
PC4	[7:4]	rw	**Port Control for Port 10.4** (coding see **Table 10-7** on **Page 10-15**)
PC5	[15:12]	rw	**Port Control for Port 10.5** (coding see **Table 10-7** on **Page 10-15**)
PC6, PC7	[23:20], [31:28]	rw	**Reserved** Read as 0010_B after reset; returns value that was written.
0	[3:0], [11:8], [19:16], [27:24]	r	**Reserved** Read as 0; should be written with 0.

10.14.3.4 Port 10 Input Register

The basic P10_IN register functionality is described on **Page 10-25**. Port lines P10.[15:6] are not available. Therefore, the P10_IN bits P[15:6] are always read as 0.

10.14.3.5 Port 10 Pad Driver Mode 0 Register

The basic P10_PDR0 register functionality is described on Page 10-18. However, port lines P10.[15:6] are not available.

P10_PDR0
Port 10 Pad Driver Mode 0 Register (40$_H$) **Reset Value: 0000 0000$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	PD7			0	PD6			0	PD5			0	PD4		
r	rw			r	rw			r	rw			r	rw		

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	PD3			0	PD2			0	PD1			0	PD0		
r	rw			r	rw			r	rw			r	rw		

Field	Bits	Type	Description
PD0	[2:0]	rw	**Pad Driver Mode for P10.0**
PD1	[6:4]	rw	**Pad Driver Mode for P10.1**
PD2	[10:8]	rw	**Pad Driver Mode for P10.2**
PD3	[14:12]	rw	**Pad Driver Mode for P10.3**
PD4	[18:16]	rw	**Pad Driver Mode for P10.4**
PD5	[22:20]	rw	**Pad Driver Mode for P10.5**
PD6	[26:24]	rw	**Reserved** Read as 000_B after reset; returns value that was written.
PD7	[30:28]	rw	**Reserved** Read as 000_B after reset; returns value that was written.
0	3, 7, 11, 15, 19, 23, 27, 31	r	**Reserved** Read as 0; should be written with 0.

10.15 Port 11

This section describes the Port 11 functionality in detail.

10.15.1 Port 11 Configuration

Port 11 is a general-purpose 16-bit bi-directional port. It serves as GPIO lines without secondary functions.

Table 10-10 summarizes the I/O control selection functions of each Port 11 line.

10.15.2 Port 11 Function Table

Table 10-10 summarizes the I/O control selection functions of each Port 11 line.

Table 10-32 Port 11 Functions

Port Pin	I/O	Pin Functionality	Associated Reg./ I/O Line	Port I/O Control Select.	
				Reg./Bit Field	Value
P11.0	I	General-purpose input	P11_IN.P0	P11_IOCR0.PC0	$0XXX_B$
	O	General-purpose output	P11_OUT.P0		$1X00_B$
		Reserved	–		$1X01_B$
		Reserved	–		$1X10_B$
		Reserved	–		$1X11_B$
	HW_Out	EBU;EN	A0		DIR
P11.1	I	General-purpose input	P11_IN.P1	P11_IOCR0.PC1	$0XXX_B$
	O	General-purpose output	P11_OUT.P1		$1X00_B$
		Reserved	–		$1X01_B$
		Reserved	–		$1X10_B$
		Reserved	–		$1X11_B$
	HW_Out	EBU;EN	A1		DIR
P11.2	I	General-purpose input	P11_IN.P2	P11_IOCR0.PC2	$0XXX_B$
	O	General-purpose output	P11_OUT.P2		$1X00_B$
		Reserved	–		$1X01_B$
		Reserved	–		$1X10_B$
		Reserved	–		$1X11_B$
	HW_Out	EBU;EN	A2		DIR
P11.3	I	General-purpose input	P11_IN.P3	P11_IOCR0.PC3	$0XXX_B$
	O	General-purpose output	P11_OUT.P3		$1X00_B$
		Reserved	–		$1X01_B$
		Reserved	–		$1X10_B$
		Reserved	–		$1X11_B$
	HW_Out	EBU;EN	A3		DIR

Table 10-32 Port 11 Functions (cont'd)

Port Pin	I/O	Pin Functionality	Associated Reg./ I/O Line	Port I/O Control Select.	
				Reg./Bit Field	Value
P11.4	I	General-purpose input	P11_IN.P4	P11_IOCR4. PC4	$0XXX_B$
	O	General-purpose output	P11_OUT.P4		$1X00_B$
		Reserved	–		$1X01_B$
		Reserved	–		$1X10_B$
		Reserved	–		$1X11_B$
	HW_Out	EBU;EN	A4		DIR
P11.5	I	General-purpose input	P11_IN.P5	P11_IOCR4. PC5	$0XXX_B$
	O	General-purpose output	P11_OUT.P5		$1X00_B$
		Reserved	–		$1X01_B$
		Reserved	–		$1X10_B$
		Reserved	–		$1X11_B$
	HW_Out	EBU;EN	A5		DIR
P11.6	I	General-purpose input	P11_IN.P6	P11_IOCR4. PC6	$0XXX_B$
	O	General-purpose output	P11_OUT.P6		$1X00_B$
		Reserved	–		$1X01_B$
		Reserved	–		$1X10_B$
		Reserved	–		$1X11_B$
	HW_Out	EBU;EN	A6		DIR
P11.7	I	General-purpose input	P11_IN.P7	P11_IOCR4. PC7	$0XXX_B$
	O	General-purpose output	P11_OUT.P7		$1X00_B$
		Reserved	–		$1X01_B$
		Reserved	–		$1X10_B$
		Reserved	–		$1X11_B$
	HW_Out	EBU;EN	A7		DIR

Table 10-32 Port 11 Functions (cont'd)

Port Pin	I/O	Pin Functionality	Associated Reg./ I/O Line	Port I/O Control Select.	
				Reg./Bit Field	Value
P11.8	I	General-purpose input	P11_IN.P8	P11_IOCR8. PC8	$0XXX_B$
	O	General-purpose output	P11_OUT.P8		$1X00_B$
		Reserved	–		$1X01_B$
		Reserved	–		$1X10_B$
		Reserved	–		$1X11_B$
	HW_Out	EBU;EN	A8		DIR
P11.9	I	General-purpose input	P11_IN.P9	P11_IOCR8. PC9	$0XXX_B$
	O	General-purpose output	P11_OUT.P9		$1X00_B$
		Reserved	–		$1X01_B$
		Reserved	–		$1X10_B$
		Reserved	–		$1X11_B$
	HW_Out	EBU;EN	A9		DIR
P11.10	I	General-purpose input	P11_IN.P10	P11_IOCR8. PC10	$0XXX_B$
	O	General-purpose output	P11_OUT.P10		$1X00_B$
		Reserved	–		$1X01_B$
		Reserved	–		$1X10_B$
		Reserved	–		$1X11_B$
	HW_Out	EBU;EN	A10		DIR
P11.11	I	General-purpose input	P11_IN.P11	P11_IOCR8. PC11	$0XXX_B$
	O	General-purpose output	P11_OUT.P11		$1X00_B$
		Reserved	–		$1X01_B$
		Reserved	–		$1X10_B$
		Reserved	–		$1X11_B$
	HW_Out	EBU;EN	A11		DIR

Table 10-32 Port 11 Functions (cont'd)

Port Pin	I/O	Pin Functionality	Associated Reg./ I/O Line	Port I/O Control Select.	
				Reg./Bit Field	Value
P11.12	I	General-purpose input	P11_IN.P12	P11_IOCR12. PC12	$0XXX_B$
	O	General-purpose output	P11_OUT.P12		$1X00_B$
		Reserved	–		$1X01_B$
		Reserved	–		$1X10_B$
		Reserved	–		$1X11_B$
	HW_Out	EBU;EN	A12		DIR
P11.13	I	General-purpose input	P11_IN.P13	P11_IOCR12. PC13	$0XXX_B$
	O	General-purpose output	P11_OUT.P13		$1X00_B$
		Reserved	–		$1X01_B$
		Reserved	–		$1X10_B$
		Reserved	–		$1X11_B$
	HW_Out	EBU;EN	A13		DIR
P11.14	I	General-purpose input	P11_IN.P14	P11_IOCR12. PC14	$0XXX_B$
	O	General-purpose output	P11_OUT.P14		$1X00_B$
		Reserved	–		$1X01_B$
		Reserved	–		$1X10_B$
		Reserved	–		$1X11_B$
	HW_Out	EBU;EN	A14		DIR
P11.15	I	General-purpose input	P11_IN.P15	P11_IOCR12. PC15	$0XXX_B$
	O	General-purpose output	P11_OUT.P15		$1X00_B$
		Reserved	–		$1X01_B$
		Reserved	–		$1X10_B$
		Reserved	–		$1X11_B$
	HW_Out	EBU;EN	A15		DIR

10.15.3 Port 11 Registers

The following registers are available on Port 11:

Table 10-33 Port 11 Registers

Register Short Name	Register Long Name	Offset[1] Address	Description see
P11_OUT	Port 11 Output Register	0000_H	Page 10-21
P11_OMR	Port 11 Output Modification Register	0004_H	Page 10-22
P11_IOCR0	Port 11 Input/Output Control Register 0	0010_H	Page 10-11
P11_IOCR4	Port 11 Input/Output Control Register 4	0014_H	Page 10-12
P11_IOCR8	Port 11 Input/Output Control Register 8	0018_H	Page 10-13
P11_IOCR12	Port 11 Input/Output Control Register 12	$001C_H$	Page 10-14
P11_IN	Port 11 Input Register	0024_H	Page 10-25
P11_PDR0	Port 11 Pad Driver Mode 0 Register	0040_H	Page 10-18
P11_PDR1	Port 11 Pad Driver Mode 1 Register	0044_H	Page 10-19

1) The absolute addresses are calculated by adding the offset address to the module base address (see Table 10-4)

10.16 Port 12

This section describes the Port 12 functionality in detail.

10.16.1 Port 12 Configuration

Port 12 is an 8-bit bi-directional general-purpose I/O port.

10.16.2 Port 12 Function Table

Table 10-26 summarizes the I/O control selection functions of each Port 12 line.

Table 10-34 Port 12 Functions

Port Pin	I/O	Pin Functionality	Associated Reg./I/O Line	Port I/O Control Select.	
				Reg./Bit Field	Value
P12.0	I	General-purpose input	P12_IN.P0	P12_IOCR 0.PC0	$0XXX_B$
	O	General-purpose output	P12_OUT.P0		$1X00_B$
		Reserved	–		$1X01_B$
		Reserved	–		$1X10_B$
		Reserved	–		$1X11_B$
	HW_Out	EBU;EN	A16		DIR
P12.1	I	General-purpose input	P12_IN.P1	P12_IOCR 0.PC1	$0XXX_B$
	O	General-purpose output	P12_OUT.P1		$1X00_B$
		Reserved	–		$1X01_B$
		Reserved	–		$1X10_B$
		Reserved[1)]	–		$1X11_B$
	HW_Out	EBU;EN	A17		DIR
P12.2	I	General-purpose input	P12_IN.P2	P12_IOCR 0.PC2	$0XXX_B$
	O	General-purpose output	P12_OUT.P2		$1X00_B$
		Reserved	–		$1X01_B$
		Reserved	–		$1X10_B$
		Reserved	–		$1X11_B$
	HW_Out	EBU;EN	A18		DIR
P12.3	I	General-purpose input	P12_IN.P3	P12_IOCR 0.PC3	$0XXX_B$
	O	General-purpose output	P12_OUT.P3		$1X00_B$
		Reserved	–		$1X01_B$
		Reserved	–		$1X10_B$
		Reserved	–		$1X11_B$
	HW_Out	EBU;EN	A19		DIR

Table 10-34 Port 12 Functions (cont'd)

Port Pin	I/O	Pin Functionality	Associated Reg./I/O Line	Port I/O Control Select.	
				Reg./Bit Field	Value
P12.4	I	General-purpose input	P12_IN.P4	P12_IOCR 4.PC4	$0XXX_B$
	O	General-purpose output	P12_OUT.P4		$1X00_B$
		Reserved	–		$1X01_B$
		Reserved	–		$1X10_B$
		Reserved	–		$1X11_B$
	HW_Out	EBU;EN	A20		DIR
P12.5	I	General-purpose input	P12_IN.P5	P12_IOCR 4.PC5	$0XXX_B$
	O	General-purpose output	P12_OUT.P5		$1X00_B$
		Reserved	–		$1X01_B$
		Reserved	–		$1X10_B$
		Reserved	–		$1X11_B$
	HW_Out	EBU;EN	A21		DIR
P12.6	I	General-purpose input	P12_IN.P6	P12_IOCR 4.PC6	$0XXX_B$
	O	General-purpose output	P12_OUT.P6		$1X00_B$
		Reserved	–		$1X01_B$
		Reserved	–		$1X10_B$
		Reserved	–		$1X11_B$
	HW_Out	EBU;EN	A22		DIR
P12.7	I	General-purpose input	P12_IN.P7	P12_IOCR 4.PC7	$0XXX_B$
	O	General-purpose output	P12_OUT.P7		$1X00_B$
		Reserved	–		$1X01_B$
		Reserved	–		$1X10_B$
		Reserved	–		$1X11_B$
	HW_Out	EBU;EN	A23		DIR

1) The port I/O control values P12_IOCRx.Py that are assigned to this reserved alternate output control selection should not be used.

10.16.3 Port 12 Registers

The following registers are available on Port 12:

Table 10-35 Port 12 Registers

Register Short Name	Register Long Name	Offset[1] Address	Description see
P12_OUT	Port 12 Output Register	0000_H	below[2]
P12_OMR	Port 12 Output Modification Register	0004_H	
P12_IOCR0	Port 12 Input/Output Control Register 0	0010_H	Page 10-11
P12_IOCR4	Port 12 Input/Output Control Register 4	0014_H	Page 10-12
P12_IN	Port 12 Input Register	0024_H	below[2]
P12_PDR0	Port 12 Pad Driver Mode 0 Register	0040_H	Page 10-18

1) The absolute addresses are calculated by adding the offset address to the module base address (see Table 10-4)

2) These registers are listed here in the Port 12 section because they differ from the general port register description given in Section 10.3.

10.16.3.1 Port 12 Output Register

The basic P12_OUT register functionality is described on Page 10-21. Port lines P12.[15:8] are not available. Therefore, the P12_OUT bits P[15:8] should be written with 0 and are always read as 0.

10.16.3.2 Port 12 Output Modification Register

The basic P12_OMR register functionality is described on Page 10-22. Port lines P12.[15:8] are not available. Therefore, the P12_OMR bits PS[15:8] and PR[15:8] are not implemented. These bits should always be written with 0.

10.16.3.3 Port 12 Input Register

The basic P12_IN register functionality is described on Page 10-25. Port lines P12.[15:8] are not available. Therefore, the P12_IN bits P[15:8] are always read as 0.

10.17 Port 13

This section describes the Port 13 functionality in detail.

10.17.1 Port 13 Configuration

Port 13 is a general-purpose 16-bit bi-directional port. It serves as GPIO lines without secondary functions.

Table 10-10 summarizes the I/O control selection functions of each Port 0 line.

10.17.2 Port 13 Function Table

Table 10-10 summarizes the I/O control selection functions of each Port 13 line.

Table 10-36 Port 13 Functions

Port Pin	I/O	Pin Functionality	Associated Reg./ I/O Line	Port I/O Control Select.	
				Reg./Bit Field	Value
P13.0	I	General-purpose input	P13_IN.P0	P13_IOCR0.PC0	$0XXX_B$
		EBU Input	D0		
	O	General-purpose output	P13_OUT.P0		$1X00_B$
		GPTA0 output	OUT88		$1X01_B$
		GPTA1 output	OUT88		$1X10_B$
		LTCA2 output	OUT80		$1X11_B$
	HW_Out	EBU;EN	D0		DIR
P13.1	I	General-purpose input	P13_IN.P1	P13_IOCR0.PC1	$0XXX_B$
		EBU Input	D1		
	O	General-purpose output	P13_OUT.P1		$1X00_B$
		GPTA0 output	OUT89		$1X01_B$
		GPTA1 output	OUT89		$1X10_B$
		LTCA2 output	OUT81		$1X11_B$
	HW_Out	EBU;EN	D1		DIR
P13.2	I	General-purpose input	P13_IN.P2	P13_IOCR0.PC2	$0XXX_B$
		EBU Input	D2		
	O	General-purpose output	P13_OUT.P2		$1X00_B$
		GPTA0 output	OUT90		$1X01_B$
		GPTA1 output	OUT90		$1X10_B$
		LTCA2 output	OUT82		$1X11_B$
	HW_Out	EBU;EN	D2		DIR

Table 10-36 Port 13 Functions (cont'd)

Port Pin	I/O	Pin Functionality	Associated Reg./ I/O Line	Port I/O Control Select.	
				Reg./Bit Field	Value
P13.3	I	General-purpose input	P13_IN.P3	P13_IOCR0.PC3	$0XXX_B$
		EBU Input	D3		
	O	General-purpose output	P13_OUT.P3		$1X00_B$
		GPTA0 output	OUT91		$1X01_B$
		GPTA1 output	OUT91		$1X10_B$
		LTCA2 output	OUT83		$1X11_B$
	HW_Out	EBU;EN	D3		DIR
P13.4	I	General-purpose input	P13_IN.P4	P13_IOCR4.PC4	$0XXX_B$
		EBU Input	D4		
	O	General-purpose output	P13_OUT.P4		$1X00_B$
		GPTA0 output	OUT92		$1X01_B$
		GPTA1 output	OUT92		$1X10_B$
		LTCA2 output	OUT84		$1X11_B$
	HW_Out	EBU;EN	D4		DIR
P13.5	I	General-purpose input	P13_IN.P5	P13_IOCR4.PC5	$0XXX_B$
		EBU Input	D5		
	O	General-purpose output	P13_OUT.P5		$1X00_B$
		GPTA0 output	OUT93		$1X01_B$
		GPTA1 output	OUT93		$1X10_B$
		LTCA2 output	OUT85		$1X11_B$
	HW_Out	EBU;EN	D5		DIR
P13.6	I	General-purpose input	P13_IN.P6	P13_IOCR4.PC6	$0XXX_B$
		EBU Input	D6		
	O	General-purpose output	P13_OUT.P6		$1X00_B$
		GPTA0 output	OUT94		$1X01_B$
		GPTA1 output	OUT94		$1X10_B$
		LTCA2 output	OUT86		$1X11_B$
	HW_Out	EBU;EN	D6		DIR

Table 10-36 Port 13 Functions (cont'd)

Port Pin	I/O	Pin Functionality	Associated Reg./ I/O Line	Port I/O Control Select.	
				Reg./Bit Field	Value
P13.7	I	General-purpose input	P13_IN.P7	P13_IOCR4. PC7	$0XXX_B$
		EBU Input	D7		
	O	General-purpose output	P13_OUT.P7		$1X00_B$
		GPTA0 output	OUT95		$1X01_B$
		GPTA1 output	OUT95		$1X10_B$
		LTCA2 output	OUT87		$1X11_B$
	HW_Out	EBU;EN	D7		DIR
P13.8	I	General-purpose input	P13_IN.P8	P13_IOCR8. PC8	$0XXX_B$
		EBU Input	D8		
	O	General-purpose output	P13_OUT.P8		$1X00_B$
		GPTA0 output	OUT96		$1X01_B$
		GPTA1 output	OUT96		$1X10_B$
		LTCA2 output	OUT88		$1X11_B$
	HW_Out	EBU;EN	D8		DIR
P13.9	I	General-purpose input	P13_IN.P9	P13_IOCR8. PC9	$0XXX_B$
		EBU Input	D9		
	O	General-purpose output	P13_OUT.P9		$1X00_B$
		GPTA0 output	OUT97		$1X01_B$
		GPTA1 output	OUT97		$1X10_B$
		LTCA2 output	OUT89		$1X11_B$
	HW_Out	EBU;EN	D9		DIR
P13.10	I	General-purpose input	P13_IN.P10	P13_IOCR8. PC10	$0XXX_B$
		EBU Input	D10		
	O	General-purpose output	P13_OUT.P10		$1X00_B$
		GPTA0 output	OUT98		$1X01_B$
		GPTA1 output	OUT98		$1X10_B$
		LTCA2 output	OUT90		$1X11_B$
	HW_Out	EBU;EN	D10		DIR

Table 10-36 Port 13 Functions (cont'd)

Port Pin	I/O	Pin Functionality	Associated Reg./ I/O Line	Port I/O Control Select.	
				Reg./Bit Field	Value
P13.11	I	General-purpose input	P13_IN.P11	P13_IOCR8.PC11	$0XXX_B$
		EBU Input	D11		
	O	General-purpose output	P13_OUT.P11		$1X00_B$
		GPTA0 output	OUT99		$1X01_B$
		GPTA1 output	OUT99		$1X10_B$
		LTCA2 output	OUT91		$1X11_B$
	HW_Out	EBU;EN	D11		DIR
P13.12	I	General-purpose input	P13_IN.P12	P13_IOCR12.PC12	$0XXX_B$
		EBU Input	D12		
	O	General-purpose output	P13_OUT.P12		$1X00_B$
		GPTA0 output	OUT100		$1X01_B$
		GPTA1 output	OUT100		$1X10_B$
		LTCA2 output	OUT92		$1X11_B$
	HW_Out	EBU;EN	D12		DIR
P13.13	I	General-purpose input	P13_IN.P13	P13_IOCR12.PC13	$0XXX_B$
		EBU Input	D13		
	O	General-purpose output	P13_OUT.P13		$1X00_B$
		GPTA0 output	OUT101		$1X01_B$
		GPTA1 output	OUT101		$1X10_B$
		LTCA2 output	OUT93		$1X11_B$
	HW_Out	EBU;EN	D13		DIR
P13.14	I	General-purpose input	P13_IN.P14	P13_IOCR12.PC14	$0XXX_B$
		EBU Input	D14		
	O	General-purpose output	P13_OUT.P14		$1X00_B$
		GPTA0 output	OUT102		$1X01_B$
		GPTA1 output	OUT102		$1X10_B$
		LTCA2 output	OUT94		$1X11_B$
	HW_Out	EBU;EN	D14		DIR

Table 10-36 Port 13 Functions (cont'd)

Port Pin	I/O	Pin Functionality	Associated Reg./ I/O Line	Port I/O Control Select.	
				Reg./Bit Field	Value
P13.15	I	General-purpose input	P13_IN.P15	P13_IOCR12.PC15	$0XXX_B$
		EBU Input	D15		
	O	General-purpose output	P13_OUT.P15		$1X00_B$
		GPTA0 output	OUT103		$1X01_B$
		GPTA1 output	OUT103		$1X10_B$
		LTCA2 output	OUT95		$1X11_B$
	HW_Out	EBU;EN	D15		DIR

10.17.3 Port 13 Registers

The following registers are available on Port 13:

Table 10-37 Port 13 Registers

Register Short Name	Register Long Name	Offset[1] Address	Description see
P13_OUT	Port 13 Output Register	0000_H	Page 10-21
P13_OMR	Port 13 Output Modification Register	0004_H	Page 10-22
P13_IOCR0	Port 13 Input/Output Control Register 0	0010_H	Page 10-11
P13_IOCR4	Port 13 Input/Output Control Register 4	0014_H	Page 10-12
P13_IOCR8	Port 13 Input/Output Control Register 8	0018_H	Page 10-13
P13_IOCR12	Port 13 Input/Output Control Register 12	$001C_H$	Page 10-14
P13_IN	Port 13 Input Register	0024_H	Page 10-25
P13_PDR0	Port 13 Pad Driver Mode 0 Register	0040_H	Page 10-18
P13_PDR1	Port 13 Pad Driver Mode 1 Register	0044_H	Page 10-19
P13_ESR	Port 13 Emergency Stop Register	0050_H	Page 10-24

1) The absolute addresses are calculated by adding the offset address to the module base address (see Table 10-4)

10.17.3.1 Port 13 Emergency Stop Register

The basic P13_ESR register functionality is described on Page 10-24. At Port 13, all port lines P13.[15:0] have GPTA outputs and correspondent ESR lines.

10.18 Port 14

This section describes the Port 14 functionality in detail.

10.18.1 Port 14 Configuration

Port 14 is a general-purpose 16-bit bi-directional port. It serves as GPIO lines without secondary functions.

Table 10-10 summarizes the I/O control selection functions of each Port 14 line.

10.18.2 Port 14 Function Table

Table 10-10 summarizes the I/O control selection functions of each Port 14 line.

Table 10-38 Port 14 Functions

Port Pin	I/O	Pin Functionality	Associated Reg./ I/O Line	Port I/O Control Select.	
				Reg./Bit Field	Value
P14.0	I	General-purpose input	P14_IN.P0	P14_IOCR0.PC0	$0XXX_B$
		EBU Input	D16		
	O	General-purpose output	P14_OUT.P0		$1X00_B$
		CCU60	CC60		$1X01_B$
		GPTA1 output	OUT96		$1X10_B$
		LTCA2 output	OUT96		$1X11_B$
	HW_Out	EBU;EN	D16		DIR
P14.1	I	General-purpose input	P14_IN.P1	P14_IOCR0.PC1	$0XXX_B$
		EBU Input	D17		
	O	General-purpose output	P14_OUT.P1		$1X00_B$
		CCU60	CC61		$1X01_B$
		GPTA1 output	OUT97		$1X10_B$
		LTCA2 output	OUT97		$1X11_B$
	HW_Out	EBU;EN	D17		DIR
P14.2	I	General-purpose input	P14_IN.P2	P14_IOCR0.PC2	$0XXX_B$
		EBU Input	D18		
	O	General-purpose output	P14_OUT.P2		$1X00_B$
		CCU60	CC62		$1X01_B$
		GPTA1 output	OUT98		$1X10_B$
		LTCA2 output	OUT98		$1X11_B$
	HW_Out	EBU;EN	D18		DIR

Table 10-38 Port 14 Functions (cont'd)

Port Pin	I/O	Pin Functionality	Associated Reg./ I/O Line	Port I/O Control Select.	
				Reg./Bit Field	Value
P14.3	I	General-purpose input	P14_IN.P3	P14_IOCR0.PC3	$0XXX_B$
		EBU Input	D19		
	O	General-purpose output	P14_OUT.P3		$1X00_B$
		CCU60	COUT60		$1X01_B$
		GPTA1 output	OUT99		$1X10_B$
		LTCA2 output	OUT99		$1X11_B$
	HW_Out	EBU;EN	D19		DIR
P14.4	I	General-purpose input	P14_IN.P4	P14_IOCR4.PC4	$0XXX_B$
		EBU Input	D20		
	O	General-purpose output	P14_OUT.P4		$1X00_B$
		CCU60	COUT61		$1X01_B$
		GPTA1 output	OUT100		$1X10_B$
		LTCA2 output	OUT100		$1X11_B$
	HW_Out	EBU;EN	D20		DIR
P14.5	I	General-purpose input	P14_IN.P5	P14_IOCR4.PC5	$0XXX_B$
		EBU Input	D21		
	O	General-purpose output	P14_OUT.P5		$1X00_B$
		CCU60	COUT62		$1X01_B$
		GPTA1 output	OUT101		$1X10_B$
		LTCA2 output	OUT101		$1X11_B$
	HW_Out	EBU;EN	D21		DIR
P14.6	I	General-purpose input	P14_IN.P6	P14_IOCR4.PC6	$0XXX_B$
		EBU Input	D22		
	O	General-purpose output	P14_OUT.P6		$1X00_B$
		CCU60	COUT63		$1X01_B$
		GPTA1 output	OUT102		$1X10_B$
		LTCA2 output	OUT102		$1X11_B$
	HW_Out	EBU;EN	D22		DIR

Table 10-38 Port 14 Functions (cont'd)

Port Pin	I/O	Pin Functionality	Associated Reg./ I/O Line	Port I/O Control Select.	
				Reg./Bit Field	Value
P14.7	I	General-purpose input	P14_IN.P7	P14_IOCR4. PC7	$0XXX_B$
		EBU Input	D23		
	O	General-purpose output	P14_OUT.P7		$1X00_B$
		CCU61	CC60		$1X01_B$
		GPTA1 output	OUT103		$1X10_B$
		LTCA2 output	OUT103		$1X11_B$
	HW_Out	EBU;EN	D23		DIR
P14.8	I	General-purpose input	P14_IN.P8	P14_IOCR8. PC8	$0XXX_B$
		EBU Input	D24		
	O	General-purpose output	P14_OUT.P8		$1X00_B$
		CCU61	CC61		$1X01_B$
		GPT120	T3OUT		$1X10_B$
		LTCA2 output	OUT104		$1X11_B$
	HW_Out	EBU;EN	D24		DIR
P14.9	I	General-purpose input	P14_IN.P9	P14_IOCR8. PC9	$0XXX_B$
		EBU Input	D25		
	O	General-purpose output	P14_OUT.P9		$1X00_B$
		CCU61	CC62		$1X01_B$
		GPT121	T3OUT		$1X10_B$
		LTCA2 output	OUT105		$1X11_B$
	HW_Out	EBU;EN	D25		DIR
P14.10	I	General-purpose input	P14_IN.P10	P14_IOCR8. PC10	$0XXX_B$
		EBU Input	D26		
	O	General-purpose output	P14_OUT.P10		$1X00_B$
		CCU61	COUT60		$1X01_B$
		GPT120	T6OUT		$1X10_B$
		LTCA2 output	OUT106		$1X11_B$
	HW_Out	EBU;EN	D26		DIR

Table 10-38 Port 14 Functions (cont'd)

Port Pin	I/O	Pin Functionality	Associated Reg./ I/O Line	Port I/O Control Select.	
				Reg./Bit Field	Value
P14.11	I	General-purpose input	P14_IN.P11	P14_IOCR8. PC11	$0XXX_B$
		EBU Input	D27		
	O	General-purpose output	P14_OUT.P11		$1X00_B$
		CCU61	COUT61		$1X01_B$
		GPT121	T6OUT		$1X10_B$
		LTCA2 output	OUT107		$1X11_B$
	HW_Out	EBU;EN	D27		DIR
P14.12	I	General-purpose input	P14_IN.P12	P14_IOCR12. PC12	$0XXX_B$
		EBU Input	D28		
	O	General-purpose output	P14_OUT.P12		$1X00_B$
		CCU61	COUT62		$1X01_B$
		GPTA1 output	OUT108		$1X10_B$
		LTCA2 output	OUT108		$1X11_B$
	HW_Out	EBU;EN	D28		DIR
P14.13	I	General-purpose input	P14_IN.P13	P14_IOCR12. PC13	$0XXX_B$
		EBU Input	D29		
	O	General-purpose output	P14_OUT.P13		$1X00_B$
		CCU61	COUT63		$1X01_B$
		GPTA1 output	OUT109		$1X10_B$
		LTCA2 output	OUT109		$1X11_B$
	HW_Out	EBU;EN	D29		DIR

Table 10-38 Port 14 Functions (cont'd)

Port Pin	I/O	Pin Functionality	Associated Reg./ I/O Line	Port I/O Control Select.	
				Reg./Bit Field	Value
P14.14	I	General-purpose input	P14_IN.P14	P14_IOCR12. PC14	$0XXX_B$
		EBU Input	D30		
		GPT120	T3INC		
		GPT121	T3IND		
	O	General-purpose output	P14_OUT.P14		$1X00_B$
		GPTA0 output	OUT110		$1X01_B$
		GPTA1 output	OUT110		$1X10_B$
		LTCA2 output	OUT110		$1X11_B$
	HW_Out	EBU;EN	D30		DIR
P14.15	I	General-purpose input	P14_IN.P15	P14_IOCR12. PC15	$0XXX_B$
		EBU Input	D31		
		GPT120	T3EUDC		
		GPT121	T3EUDD		
	O	General-purpose output	P14_OUT.P15		$1X00_B$
		GPTA0 output	OUT111		$1X01_B$
		GPTA1 output	OUT111		$1X10_B$
		LTCA2 output	OUT111		$1X11_B$
	HW_Out	EBU;EN	D31		DIR

10.18.3 Port 14 Registers

The following registers are available on Port 14:

Table 10-39 Port 14 Registers

Register Short Name	Register Long Name	Offset[1] Address	Description see
P14_OUT	Port 14 Output Register	0000_H	Page 10-21
P14_OMR	Port 14 Output Modification Register	0004_H	Page 10-22
P14_IOCR0	Port 14 Input/Output Control Register 0	0010_H	Page 10-11
P14_IOCR4	Port 14 Input/Output Control Register 4	0014_H	Page 10-12
P14_IOCR8	Port 14 Input/Output Control Register 8	0018_H	Page 10-13
P14_IOCR12	Port 14 Input/Output Control Register 12	$001C_H$	Page 10-14
P14_IN	Port 14 Input Register	0024_H	Page 10-25
P14_PDR0	Port 14 Pad Driver Mode 0 Register	0040_H	Page 10-18
P14_PDR1	Port 14 Pad Driver Mode 1 Register	0044_H	Page 10-18
P14_ESR	Port 14 Emergency Stop Register	0050_H	Page 10-24

1) The absolute addresses are calculated by adding the offset address to the module base address (see Table 10-4)

10.18.3.1 Port 14 Emergency Stop Register

The basic P14_ESR register functionality is described on Page 10-24. At Port 14, all port lines P14.[15:0] have GPTA outputs and correspondent ESR lines.

10.19 Port 15

This section describes the Port 15 functionality in detail.

10.19.1 Port 15 Configuration

Port 15 is a general-purpose 16-bit bi-directional port. It serves as GPIO lines without secondary functions.

Table 10-10 summarizes the I/O control selection functions of each Port 15 line.

10.19.2 Port 15 Function Table

Table 10-10 summarizes the I/O control selection functions of each Port 0 line.

Table 10-40 Port 15 Functions

Port Pin	I/O	Pin Functionality	Associated Reg./ I/O Line	Port I/O Control Select.	
				Reg./Bit Field	Value
P15.0	I	General-purpose input	P15_IN.P0	P15_IOCR0.PC0	$0XXX_B$
		GPT120	T4INC		
		GPT121	T4IND		
		CCU60	CCPOS2B		
	O	General-purpose output	P15_OUT.P0		$1X00_B$
		Reserved	–		$1X01_B$
		Reserved	–		$1X10_B$
		Reserved	–		$1X11_B$
	HW_Out	EBU;EN	$\overline{CS0}$		DIR
P15.1	I	General-purpose input	P15_IN.P1	P15_IOCR0.PC1	$0XXX_B$
		GPT120	T4EUDC		
		GPT121	T4EUDD		
		CCU61	CCPOS2B		
	O	General-purpose output	P15_OUT.P1		$1X00_B$
		Reserved	–		$1X01_B$
		Reserved	–		$1X10_B$
		Reserved	–		$1X11_B$
	HW_Out	EBU;EN	$\overline{CS1}$		DIR
P15.2	I	General-purpose input	P15_IN.P2	P15_IOCR0.PC2	$0XXX_B$
	O	General-purpose output	P15_OUT.P2		$1X00_B$
		Reserved	–		$1X01_B$
		Reserved	–		$1X10_B$
		Reserved	–		$1X11_B$
	HW_Out	EBU;EN	$\overline{CS2}$		DIR

Table 10-40 Port 15 Functions (cont'd)

Port Pin	I/O	Pin Functionality	Associated Reg./ I/O Line	Port I/O Control Select.	
				Reg./Bit Field	Value
P15.3	I	General-purpose input	P15_IN.P3	P15_IOCR0.PC3	$0XXX_B$
	O	General-purpose output	P15_OUT.P3		$1X00_B$
		Reserved	–		$1X01_B$
		Reserved	–		$1X10_B$
		Reserved	–		$1X11_B$
	HW_Out	EBU;EN	$\overline{CS3}$		DIR
P15.4	I	General-purpose input	P15_IN.P4	P15_IOCR4.PC4	$0XXX_B$
	O	General-purpose output	P15_OUT.P4		$1X00_B$
		Reserved	–		$1X01_B$
		Reserved	–		$1X10_B$
		Reserved	–		$1X11_B$
	HW_Out	EBU;EN	$\overline{BC0}$		DIR
P15.5	I	General-purpose input	P15_IN.P5	P15_IOCR4.PC5	$0XXX_B$
	O	General-purpose output	P15_OUT.P5		$1X00_B$
		Reserved	–		$1X01_B$
		Reserved	–		$1X10_B$
		Reserved	–		$1X11_B$
	HW_Out	EBU;EN	$\overline{BC1}$		DIR
P15.6	I	General-purpose input	P15_IN.P6	P15_IOCR4.PC6	$0XXX_B$
	O	General-purpose output	P15_OUT.P6		$1X00_B$
		Reserved	–		$1X01_B$
		Reserved	–		$1X10_B$
		Reserved	–		$1X11_B$
	HW_Out	EBU;EN	$\overline{BC2}$		DIR

Table 10-40 Port 15 Functions (cont'd)

Port Pin	I/O	Pin Functionality	Associated Reg./ I/O Line	Port I/O Control Select.	
				Reg./Bit Field	Value
P15.7	I	General-purpose input	P15_IN.P7	P15_IOCR4. PC7	$0XXX_B$
	O	General-purpose output	P15_OUT.P7		$1X00_B$
		Reserved	–		$1X01_B$
		Reserved	–		$1X10_B$
		Reserved	–		$1X11_B$
	HW_Out	EBU;EN	$\overline{BC3}$		DIR
P15.8	I	General-purpose input	P15_IN.P8	P15_IOCR8. PC8	$0XXX_B$
	O	General-purpose output	P15_OUT.P8		$1X00_B$
		Reserved	–		$1X01_B$
		Reserved	–		$1X10_B$
		Reserved	–		$1X11_B$
	HW_Out	EBU;EN	$\overline{RD}$		DIR
P15.9	I	General-purpose input	P15_IN.P9	P15_IOCR8. PC9	$0XXX_B$
	O	General-purpose output	P15_OUT.P9		$1X00_B$
		Reserved	–		$1X01_B$
		Reserved	–		$1X10_B$
		Reserved	–		$1X11_B$
	HW_Out	EBU;EN	RD/$\overline{WR}$		DIR
P15.10	I	General-purpose input	P15_IN.P10	P15_IOCR8. PC10	$0XXX_B$
	O	General-purpose output	P15_OUT.P10		$1X00_B$
		Reserved	–		$1X01_B$
		Reserved	–		$1X10_B$
		Reserved	–		$1X11_B$
	HW_Out	EBU;EN	$\overline{ADV}$		DIR

Table 10-40 Port 15 Functions (cont'd)

Port Pin	I/O	Pin Functionality	Associated Reg./ I/O Line	Port I/O Control Select.	
				Reg./Bit Field	Value
P15.11	I	General-purpose input	P15_IN.P11	P15_IOCR8. PC11	$0XXX_B$
		EBU Input	$\overline{WAIT}$		
	O	General-purpose output	P15_OUT.P11		$1X00_B$
		Reserved	–		$1X01_B$
		Reserved	–		$1X10_B$
		Reserved	–		$1X11_B$
P15.12	I	General-purpose input	P15_IN.P12	P15_IOCR12. PC12	$0XXX_B$
	O	General-purpose output	P15_OUT.P12		$1X00_B$
		Reserved	–		$1X01_B$
		Reserved	–		$1X10_B$
		Reserved	–		$1X11_B$
	HW_Out	EBU;EN	MR/$\overline{W}$		DIR
P15.13	I	General-purpose input	P15_IN.P13	P15_IOCR12. PC13	$0XXX_B$
	O	General-purpose output	P15_OUT.P13		$1X00_B$
		Reserved	–		$1X01_B$
		Reserved	–		$1X10_B$
		Reserved	–		$1X11_B$
	HW_Out	EBU;EN	$\overline{BAA}$		DIR
P15.14	I	General-purpose input	P15_IN.P14	P15_IOCR12. PC14	$0XXX_B$
		EBU Input	BFCLKI		
	O	General-purpose output	P15_OUT.P14		$1X00_B$
		Reserved	–		$1X01_B$
		Reserved	–		$1X10_B$
		Reserved	–		$1X11_B$

Table 10-40 Port 15 Functions (cont'd)

Port Pin	I/O	Pin Functionality	Associated Reg./ I/O Line	Port I/O Control Select.	
				Reg./Bit Field	Value
P15.15	I	General-purpose input	P15_IN.P15	P15_IOCR12. PC15	$0XXX_B$
	O	General-purpose output	P15_OUT.P15		$1X00_B$
		Reserved	–		$1X01_B$
		Reserved	–		$1X10_B$
		Reserved	–		$1X11_B$
	HW_Out	EBU;EN	BFCLKO		DIR

10.19.3 Port 15 Registers

The following registers are available on Port 15:

Table 10-41 Port 15 Registers

Register Short Name	Register Long Name	Offset[1] Address	Description see
P15_OUT	Port 15 Output Register	0000_H	Page 10-21
P15_OMR	Port 15 Output Modification Register	0004_H	Page 10-22
P15_IOCR0	Port 15 Input/Output Control Register 0	0010_H	Page 10-11
P15_IOCR4	Port 15 Input/Output Control Register 4	0014_H	Page 10-12
P15_IOCR8	Port 15 Input/Output Control Register 8	0018_H	Page 10-13
P15_IOCR12	Port 15 Input/Output Control Register 12	$001C_H$	Page 10-14
P15_IN	Port 15 Input Register	0024_H	Page 10-25
P15_PDR0	Port 15 Pad Driver Mode 0 Register	0040_H	Page 10-18
P15_PDR1	Port 15 Pad Driver Mode 1 Register	0044_H	Page 10-19

1) The absolute addresses are calculated by adding the offset address to the module base address (see Table 10-4)

10.20 Port 16

This section describes the Port 16 functionality in detail.

10.20.1 Port 16 Configuration

Port 16 is an 13-bit bi-directional general-purpose I/O port which can be used for the EBU I/O lines.

10.20.2 Port 16 Function Table

Table 10-26 summarizes the I/O control selection functions of each Port 16 line.

Table 10-42 Port 16 Functions

Port Pin	I/O	Pin Functionality	Associated Reg./I/O Line	Port I/O Control Select.	
				Reg./Bit Field	Value
P16.0	I	General-purpose input	P16_IN.P0	P16_IOCR 0.PC0	$0XXX_B$
		EBU	HOLD		
	O	General-purpose output	P16_OUT.P0		$1X00_B$
		Reserved	–		$1X01_B$
		Reserved	–		$1X10_B$
		Reserved	–		$1X11_B$
P16.1	I	General-purpose input	P16_IN.P1	P16_IOCR 0.PC1	$0XXX_B$
		EBU Input	HLDA		
	O	General-purpose output	P16_OUT.P1		$1X00_B$
		Reserved	–		$1X01_B$
		Reserved	–		$1X10_B$
		Reserved	–		$1X11_B$
	HW_Out	EBU;EN	HLDA		
P16.2	I	General-purpose input	P16_IN.P2	P16_IOCR 0.PC2	$0XXX_B$
	O	General-purpose output	P16_OUT.P2		$1X00_B$
		Reserved	–		$1X01_B$
		Reserved	–		$1X10_B$
		Reserved	–		$1X11_B$
	HW_Out	EBU;EN	BREQ		DIR
P16.3	I	General-purpose input	P16_IN.P3	P16_IOCR 0.PC3	$0XXX_B$
	O	General-purpose output	P16_OUT.P3		$1X00_B$
		Reserved	–		$1X01_B$
		Reserved	–		$1X10_B$
		Reserved	–		$1X11_B$
	HW_Out	EBU;EN	$\overline{\text{CSCOMB}}$		DIR

Table 10-42 Port 16 Functions (cont'd)

Port Pin	I/O	Pin Functionality	Associated Reg./I/O Line	Port I/O Control Select.	
				Reg./Bit Field	Value
P16.4	I	General-purpose input	P16_IN.P4	P16_IOCR 4.PC4	$0XXX_B$
	O	General-purpose output	P16_OUT.P4		$1X00_B$
		Reserved	–		$1X01_B$
		Reserved	–		$1X10_B$
		Reserved	–		$1X11_B$
	HW_Out	EBU;EN	$\overline{RAS}$		DIR
P16.5	I	General-purpose input	P16_IN.P5	P16_IOCR 4.PC5	$0XXX_B$
	O	General-purpose output	P16_OUT.P5		$1X00_B$
		Reserved	–		$1X01_B$
		Reserved	–		$1X10_B$
		Reserved	–		$1X11_B$
	HW_Out	EBU;EN	$\overline{CAS}$		DIR
P16.6	I	General-purpose input	P16_IN.P6	P16_IOCR 4.PC6	$0XXX_B$
	O	General-purpose output	P16_OUT.P6		$1X00_B$
		Reserved	–		$1X01_B$
		Reserved	–		$1X10_B$
		Reserved	–		$1X11_B$
	HW_Out	EBU;EN	DDRCLK		DIR
P16.7	I	General-purpose input	P16_IN.P7	P16_IOCR 4.PC7	$0XXX_B$
	O	General-purpose output	P16_OUT.P7		$1X00_B$
		Reserved	–		$1X01_B$
		Reserved	–		$1X10_B$
		Reserved	–		$1X11_B$
	HW_Out	EBU;EN	DDRCLKN		DIR

Table 10-42 Port 16 Functions (cont'd)

Port Pin	I/O	Pin Functionality	Associated Reg./I/O Line	Port I/O Control Select.	
				Reg./Bit Field	Value
P16.8	I	General-purpose input	P16_IN.P8	P16_IOCR 8.PC8	$0XXX_B$
	O	General-purpose output	P16_OUT.P8		$1X00_B$
		Reserved	–		$1X01_B$
		Reserved	–		$1X10_B$
		Reserved	–		$1X11_B$
	HW_Out	EBU;EN	CKE		DIR
P16.9	I	General-purpose input	P16_IN.P9	P16_IOCR 8.PC9	$0XXX_B$
		EBU Input	DQS0		
	O	General-purpose output	P16_OUT.P9		$1X00_B$
		Reserved	–		$1X01_B$
		Reserved	–		$1X10_B$
		Reserved	–		$1X11_B$
	HW_Out	EBU;EN	DQS0		DIR
P16.10	I	General-purpose input	P16_IN.P10	P16_IOCR 8.PC10	$0XXX_B$
		EBU Input	DQS1		
	O	General-purpose output	P16_OUT.P10		$1X00_B$
		Reserved	–		$1X01_B$
		Reserved	–		$1X10_B$
		Reserved	–		$1X11_B$
	HW_Out	EBU;EN	DQS1		DIR
P16.11	I	General-purpose input	P16_IN.P11	P16_IOCR 8.PC11	$0XXX_B$
		EBU Input	DQS2		
	O	General-purpose output	P16_OUT.P11		$1X00_B$
		Reserved	–		$1X01_B$
		Reserved	–		$1X10_B$
		Reserved	–		$1X11_B$
	HW_Out	EBU;EN	DQS2		DIR

Table 10-42 Port 16 Functions (cont'd)

Port Pin	I/O	Pin Functionality	Associated Reg./I/O Line	Port I/O Control Select.	
				Reg./Bit Field	Value
P16.12	I	General-purpose input	P16_IN.P12	P16_IOCR 12.PC12	$0XXX_B$
		EBU Input	DQS3		
	O	General-purpose output	P16_OUT.P12		$1X00_B$
		Reserved	–		$1X01_B$
		Reserved	–		$1X10_B$
		Reserved	–		$1X11_B$
	HW_Out	EBU;EN	DQS3		DIR

10.20.3 Port 16 Registers

The following registers are available on Port 16:

Table 10-43 Port 16 Registers

Register Short Name	Register Long Name	Offset[1] Address	Description see
P16_OUT	Port 16 Output Register	0000_H	below[2]
P16_OMR	Port 16 Output Modification Register	0004_H	below[2]
P16_IOCR0	Port 16 Input/Output Control Register 0	0010_H	Page 10-11
P16_IOCR4	Port 16 Input/Output Control Register 4	0014_H	Page 10-13
P16_IOCR8	Port 16 Input/Output Control Register 8	0018_H	Page 10-13
P16_IOCR12	Port 16 Input/Output Control Register 12	$001C_H$	Page 10-138[2]
P16_IN	Port 16 Input Register	0024_H	below[2]
P16_PDR0	Port 16 Pad Driver Mode 0 Register	0040_H	Page 10-18
P16_PDR1	Port 16 Pad Driver Mode 1 Register	0044_H	Page 10-140[2]

1) The absolute addresses are calculated by adding the offset address to the module base address (see Table 10-4)

2) These registers are listed here in the Port 16 section because they differ from the general port register description given in Section 10.3.

10.20.3.1 Port 16 Output Register

The basic P16_OUT register functionality is described on Page 10-21. Port lines P16.[15:13] are not available. Therefore, the P16_OUT bits P[15:13] should be written with 0 and are always read as 0.

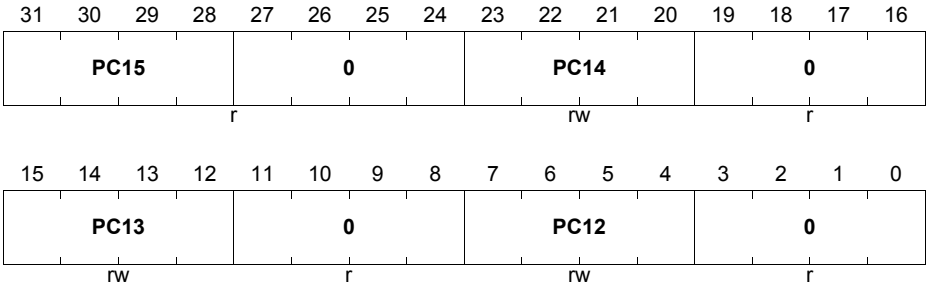
10.20.3.2 Port 16 Output Modification Register

The basic P16_OMR register functionality is described on Page 10-22. Port lines P16.[15:13] are not available. Therefore, the P16_OMR bits PS[15:13] and PR[15:13] are not implemented. These bits should always be written with 0.

10.20.3.3 Port 16 Input/Output Control Register 12

P16_IOCR12
Port 16 Input/Output Control Register 12

($1C_H$) **Reset Value: 2020 2020_H**



Field	Bits	Type	Description
PC12	[7:4]	rw	**Port Control for P16.12** This bit field determines the P16.12 functionality.
PC13	[15:12]	rw	**Reserved** Read as 0010_B after reset; returns value that was written.
PC14	[23:20]	rw	**Reserved** Read as 0010_B after reset; returns value that was written.
PC15	[31:28]	rw	**Reserved** Read as 0010_B after reset; returns value that was written.
0	[3:0], [11:8], [19:16], [27:24]	r	**Reserved** Read as 0; should be written with 0.

10.20.3.4 Port 16 Input Register

The basic P16_IN register functionality is described on **Page 10-25**. Port lines P16.[15:13] are not available. Therefore, the P16_IN bits P16.[15:13] are always read as 0.

10.20.3.5 Port 16 Emergency Stop Register

The P16_ESR register is not implemented. Nevertheless, access to its address 0xF0300450 does not generate a Bus Error.

10.20.3.6 Port 16 Pad Driver Mode 1 Register

The basic P16_PDR1 register functionality is described on Page 10-18. However, port lines P16[15:13] are not available.

P16_PDR1
Port 16 Pad Driver Mode 1 Register (44_H) Reset Value: 0000 0000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	**PD15**			**0**	**PD14**			**0**	**PD13**			**0**	**PD12**		
r	rw			r	rw			r	rw			r	rw		

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	**PD11**			**0**	**PD10**			**0**	**PD9**			**0**	**PD8**		
r	rw			r	rw			r	rw			r	rw		

Field	Bits	Type	Description
PD8	[2:0]	rw	**Pad Driver Mode for P16.8**
PD9	[6:4]	rw	**Pad Driver Mode for P16.9**
PD10	[10:8]	rw	**Pad Driver Mode for P16.10**
PD11	[14:12]	rw	**Pad Driver Mode for P16.11**
PD12	[18:16]	rw	**Pad Driver Mode for P16.12**
PD13	[22:20]	rw	**Reserved** Read as 000_B after reset; returns value that was written.
PD13	[26:24]	rw	**Reserved** Read as 000_B after reset; returns value that was written.
PD13	[30:28]	rw	**Reserved** Read as 000_B after reset; returns value that was written.
0	3, 7, 11, 15, 19, 23, 27, 31	r	**Reserved** Read as 0; should be written with 0.

10.21 Port 17

This section describes the Port 17 functionality in detail.

10.21.1 Port 17 Configuration

Port 17 is a 16-bit input port.

Table 10-44 summarizes the input control selection functions of each Port 17 line.

10.21.2 Port 17 Function Table

Table 10-44 summarizes the input control selection functions of each Port 17 line.

Table 10-44 Port 17 Functions

Port Pin	I/O	Pin Functionality	Associated Reg./ Input Line	Port Functionality Control Select	
				Reg./Bit Field	Value
P17.0	I	ADC Analog Input	AN8	P17_PDISC.PDIS0	1_B
		SENT Digital Input	SENT0		0_B
P17.1	I	ADC Analog Input	AN9	P17_PDISC.PDIS1	1_B
		SENT Digital Input	SENT1		0_B
P17.2	I	ADC Analog Input	AN10	P17_PDISC.PDIS2	1_B
		SENT Digital Input	SENT2		0_B
P17.3	I	ADC Analog Input	AN11	P17_PDISC.PDIS3	1_B
		SENT Digital Input	SENT3		0_B
P17.4	I	ADC Analog Input	AN12	P17_PDISC.PDIS4	1_B
		SENT Digital Input	SENT4		0_B
P17.5	I	ADC Analog Input	AN13	P17_PDISC.PDIS5	1_B
		SENT Digital Input	SENT5		0_B
P17.6	I	ADC Analog Input	AN14	P17_PDISC.PDIS6	1_B
		SENT Digital Input	SENT6		0_B
P17.7	I	ADC Analog Input	AN15	P17_PDISC.PDIS7	1_B
		SENT Digital Input	SENT7		0_B
P17.8	I	ADC Analog Input	AN36	P17_PDISC.PDIS8	1_B
		SENT Digital Input	SENT0		0_B
P17.9	I	ADC Analog Input	AN37	P17_PDISC.PDIS9	1_B
		SENT Digital Input	SENT1		0_B
P17.10	I	ADC Analog Input	AN38	P17_PDISC.PDIS10	1_B
		SENT Digital Input	SENT2		0_B
P17.11	I	ADC Analog Input	AN39	P17_PDISC.PDIS11	1_B
		SENT Digital Input	SENT3		0_B
P17.12	I	ADC Analog Input	AN40	P17_PDISC.PDIS12	1_B
		SENT Digital Input	SENT4		0_B

Table 10-44 Port 17 Functions (cont'd)

Port Pin	I/O	Pin Functionality	Associated Reg./ Input Line	Port Functionality Control Select	
				Reg./Bit Field	Value
P17.13	I	ADC Analog Input	AN41	P17_PDISC.PDIS13	1_B
		SENT Digital Input	SENT5		0_B
P17.14	I	ADC Analog Input	AN42	P17_PDISC.PDIS14	1_B
		SENT Digital Input	SENT6		0_B
P17.15	I	ADC Analog Input	AN43	P17_PDISC.PDIS15	1_B
		SENT Digital Input	SENT7		0_B

10.21.3 Port 17 Registers

The following registers are available on Port 17:

Table 10-45 Port 17 Registers

Register Short Name	Register Long Name	Offset[1] Address	Description see
P17_IOCR0	Port 17 Input/Output Control Register 0	0010_H	Page 10-145[2]
P17_IOCR4	Port 17 Input/Output Control Register 4	0014_H	Page 10-145[2]
P17_IOCR8	Port 17 Input/Output Control Register 8	0018_H	Page 10-145[2]
P17_IOCR12	Port 17 Input/Output Control Register 12	$001C_H$	Page 10-145[2]
P17_IN	Port 17 Input Register	0024_H	Page 10-25
P17_PDISC	Port 17 Pin Function Decision Control Register	0060_H	Page 10-148[2]

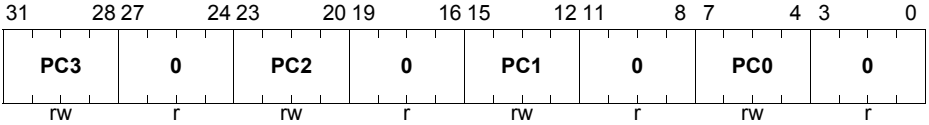
1) The absolute addresses are calculated by adding the offset address to the module base address (see Table 10-4)

2) These registers are listed here in the Port 17 section because they differ from the general port register description given in Section 10.3.

10.21.4 Port 17 Input/Output Control Registers

P17_IOCR0
Port 17 Input/Output Control Register 0

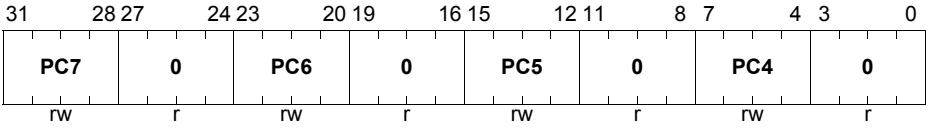
(10_H) **Reset Value: 2020 2020_H**



Field	Bits	Type	Description
PC0, PC1, PC2, PC3	[7:4], [15:12], [23:20], [31:28]	rw	**Port Control for Port n Pin x** This bit field defines the Port n line x functionality according to **Table 10-46**.
0	[3:0], [11:8], [19:16], [27:24]	r	**Reserved** Read as 0; should be written with 0.

P17_IOCR4
Port 17 Input/Output Control Register 4

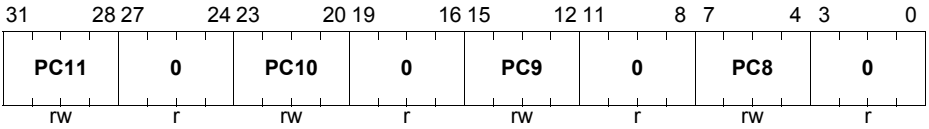
(14_H) **Reset Value: 2020 2020_H**



Field	Bits	Type	Description
PC4, PC5, PC6, PC7	[7:4], [15:12], [23:20], [31:28]	rw	**Port Control for Port n Pin x** This bit field defines the Port n line x functionality according to **Table 10-46**.
0	[3:0], [11:8], [19:16], [27:24]	r	**Reserved** Read as 0; should be written with 0.

P17_IOCR8
Port 17 Input/Output Control Register 8

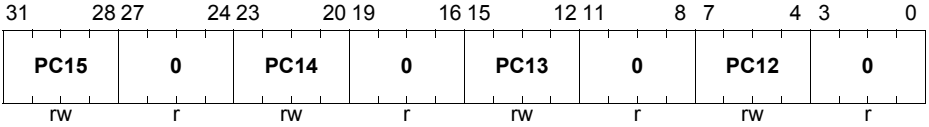
(18_H) **Reset Value: 2020 2020_H**



Field	Bits	Type	Description
PC8, PC9, PC10, PC11	[7:4], [15:12], [23:20], [31:28]	rw	**Port Control for Port n Pin x** This bit field defines the Port n line x functionality according to **Table 10-46**.
0	[3:0], [11:8], [19:16], [27:24]	r	**Reserved** Read as 0; should be written with 0.

P17_IOCR12
Port 17 Input/Output Control Register 12

($1C_H$) **Reset Value: 2020 2020_H**



Field	Bits	Type	Description
PC12, PC13, PC14, PC15	[7:4], [15:12], [23:20], [31:28]	rw	**Port Control for Port n Pin x** This bit field defines the Port n line x functionality according to **Table 10-46**.
0	[3:0], [11:8], [19:16], [27:24]	r	**Reserved** Read as 0; should be written with 0.

Table 10-46 PCx Coding for Port 17

PCx[3:0]	I/O	Output Characteristics	Selected Pull-up / Pull-down / Selected Output Function
$0X00_B$	Input	–	No input pull device connected
$0X01_B$			Input pull-down device connected
$0X10_B$			Input pull-up device connected[1)]
$0X11_B$			No input pull device connected

1) This is the default pull-up state after reset.

10.21.5 Port 17 Pin Function Decision Control Register

P17_PDISC

Port 17 Pin Function Decision Control Register(60_H) **Reset Value: FFFF FFFF$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PDIS 15	PDIS 14	PDIS 13	PDIS 12	PDIS 11	PDIS 10	PDIS 9	PDIS 8	PDIS 7	PDIS 6	PDIS 5	PDIS 4	PDIS 3	PDIS 2	PDIS 1	PDIS 0
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
PDIS0	0	rw	**Pad Disable for Port 17 Pin 0** This bit disables or enables the pad. The disabled (default) state of the pad selects the ADC analog input. Upon enabling, the functionality switches to the SENT digital input. 0_B Pad is enabled, SENT digital input 0. 1_B Pad is disabled, ADC analog input 8.
PDIS1	1	rw	**Pad Disable for Port 17 Pin 1** This bit disables or enables the pad. The disabled (default) state of the pad selects the ADC analog input. Upon enabling, the functionality switches to the SENT digital input. 0_B Pad is enabled, SENT digital input 1. 1_B Pad is disabled, ADC analog input 9.
PDIS2	2	rw	**Pad Disable for Port 17 Pin 2** This bit disables or enables the pad. The disabled (default) state of the pad selects the ADC analog input. Upon enabling, the functionality switches to the SENT digital input. 0_B Pad is enabled, SENT digital input 2. 1_B Pad is disabled, ADC analog input 10.

Field	Bits	Type	Description
PDIS3	3	rw	**Pad Disable for Port 17 Pin 3** This bit disables or enables the pad. The disabled (default) state of the pad selects the ADC analog input. Upon enabling, the functionality switches to the SENT digital input. 0_B Pad is enabled, SENT digital input 3. 1_B Pad is disabled, ADC analog input 11.
PDIS4	4	rw	**Pad Disable for Port 17 Pin 4** This bit disables or enables the pad. The disabled (default) state of the pad selects the ADC analog input. Upon enabling, the functionality switches to the SENT digital input. 0_B Pad is enabled, SENT digital input 4. 1_B Pad is disabled, ADC analog input 12.
PDIS5	5	rw	**Pad Disable for Port 17 Pin 5** This bit disables or enables the pad. The disabled (default) state of the pad selects the ADC analog input. Upon enabling, the functionality switches to the SENT digital input. 0_B Pad is enabled, SENT digital input 5. 1_B Pad is disabled, ADC analog input 13.
PDIS6	6	rw	**Pad Disable for Port 17 Pin 6** This bit disables or enables the pad. The disabled (default) state of the pad selects the ADC analog input. Upon enabling, the functionality switches to the SENT digital input. 0_B Pad is enabled, SENT digital input 6. 1_B Pad is disabled, ADC analog input 14.
PDIS7	7	rw	**Pad Disable for Port 17 Pin 7** This bit disables or enables the pad. The disabled (default) state of the pad selects the ADC analog input. Upon enabling, the functionality switches to the SENT digital input. 0_B Pad is enabled, SENT digital input 7. 1_B Pad is disabled, ADC analog input 15.

Field	Bits	Type	Description
PDIS8	8	rw	**Pad Disable for Port 17 Pin 8** This bit disables or enables the pad. The disabled (default) state of the pad selects the ADC analog input. Upon enabling, the functionality switches to the SENT digital input. 0_B Pad is enabled, SENT digital input 0. 1_B Pad is disabled, ADC analog input 36.
PDIS9	9	rw	**Pad Disable for Port 17 Pin 9** This bit disables or enables the pad. The disabled (default) state of the pad selects the ADC analog input. Upon enabling, the functionality switches to the SENT digital input. 0_B Pad is enabled, SENT digital input 1. 1_B Pad is disabled, ADC analog input 37.
PDIS10	10	rw	**Pad Disable for Port 17 Pin 10** This bit disables or enables the pad. The disabled (default) state of the pad selects the ADC analog input. Upon enabling, the functionality switches to the SENT digital input. 0_B Pad is enabled, SENT digital input 2. 1_B Pad is disabled, ADC analog input 38.
PDIS11	11	rw	**Pad Disable for Port 17 Pin 11** This bit disables or enables the pad. The disabled (default) state of the pad selects the ADC analog input. Upon enabling, the functionality switches to the SENT digital input. 0_B Pad is enabled, SENT digital input 3. 1_B Pad is disabled, ADC analog input 39.
PDIS12	12	rw	**Pad Disable for Port 17 Pin 12** This bit disables or enables the pad. The disabled (default) state of the pad selects the ADC analog input. Upon enabling, the functionality switches to the SENT digital input. 0_B Pad is enabled, SENT digital input 4. 1_B Pad is disabled, ADC analog input 40.

Field	Bits	Type	Description
PDIS13	13	rw	**Pad Disable for Port 17 Pin 13** This bit disables or enables the pad. The disabled (default) state of the pad selects the ADC analog input. Upon enabling, the functionality switches to the SENT digital input. 0_B Pad is enabled, SENT digital input 5. 1_B Pad is disabled, ADC analog input 41.
PDIS14	14	rw	**Pad Disable for Port 17 Pin 14** This bit disables or enables the pad. The disabled (default) state of the pad selects the ADC analog input. Upon enabling, the functionality switches to the SENT digital input. 0_B Pad is enabled, SENT digital input 6. 1_B Pad is disabled, ADC analog input 42.
PDIS15	15	rw	**Pad Disable for Port 17 Pin 15** This bit disables or enables the pad. The disabled (default) state of the pad selects the ADC analog input. Upon enabling, the functionality switches to the SENT digital input. 0_B Pad is enabled, SENT digital input 7. 1_B Pad is disabled, ADC analog input 43.
0	[31:16]	r	**Reserved** Read as 0; should be written with 0.

10.22 Port 18

This section describes the Port 18 functionality in detail.

10.22.1 Port 18 Configuration

Port 18 is a general-purpose 8-bit bi-directional port.

Table 10-47 summarizes the I/O control selection functions of each Port 18 line.

10.22.2 Port 18 Function Table

Table 10-47 summarizes the I/O control selection functions of each Port 18 line.

Table 10-47 Port 18 Functions

Port Pin	I/O	Pin Functionality	Associated Reg./ I/O Line	Port I/O Control Select.	
				Reg./Bit Field	Value
P18.0	I	General-purpose input	P18_IN.P0	P1_IOCR0.PC0	$0XXX_B$
		SSC2 input (Slave Mode)	MRST2B		
	O	General-purpose output	P18_OUT.P0		$1X00_B$
		SSC2 output (Master Mode)	MRST2		$1X01_B$
		Reserved	–		$1X10_B$
		Reserved	–		$1X11_B$
P18.1	I	General-purpose input	P18_IN.P1	P1_IOCR0.PC1	$0XXX_B$
		SSC2 input (Master Mode)	MTSR2B		
		SSC Guardian 2 Master Receive Input B (Master Mode)	MRSTG2B		
	O	General-purpose output	P18_OUT.P1		$1X00_B$
		SSC2 output (Slave Mode)	MTSR2		$1X01_B$
		Reserved	–		$1X10_B$
		Reserved	–		$1X11_B$
P18.2	I	General-purpose input	P18_IN.P2	P1_IOCR0.PC2	$0XXX_B$
		SSC2 input	SCLK2B		
	O	General-purpose output	P18_OUT.P2		$1X00_B$
		SSC2 output	SCLK2		$1X01_B$
		Reserved	–		$1X10_B$
		Reserved	–		$1X11_B$

Table 10-47 Port 18 Functions (cont'd)

Port Pin	I/O	Pin Functionality	Associated Reg./ I/O Line	Port I/O Control Select.	
				Reg./Bit Field	Value
P18.3	I	General-purpose input	P18_IN.P3	P1_IOCR0.PC3	$0XXX_B$
		Reserved	–		
		Reserved	–		
	O	General-purpose output	P18_OUT.P3		$1X00_B$
		SSC2 output	SLSO20		$1X01_B$
		Reserved	–		$1X10_B$
		Reserved	–		$1X11_B$
P18.4	I	General-purpose input	P18_IN.P4	P1_IOCR4.PC4	$0XXX_B$
	O	General-purpose output	P18_OUT.P4		$1X00_B$
		SSC2 output	SLSO21		$1X01_B$
		Reserved	–		$1X10_B$
		Reserved	–		$1X11_B$
P18.5	I	General-purpose input	P18_IN.P5	P1_IOCR4.PC5	$0XXX_B$
		Reserved	–		
	O	General-purpose output	P18_OUT.P5		$1X00_B$
		SSC2 output	SLSO22		$1X01_B$
		Reserved	–		$1X10_B$
		Reserved	–		$1X11_B$
P18.6	I	General-purpose input	P18_IN.P6	P1_IOCR4.PC6	$0XXX_B$
	O	General-purpose output	P18_OUT.P6		$1X00_B$
		SSC2 output	SLSO23		$1X01_B$
		Reserved	–		$1X10_B$
		Reserved	–		$1X11_B$
P18.7	I	General-purpose input	P18_IN.P7	P1_IOCR4.PC7	$0XXX_B$
	O	General-purpose output	P18_OUT.P7		$1X00_B$
		SSC2 output	SLSO24		$1X01_B$
		Reserved	–		$1X10_B$
		Reserved	–		$1X11_B$

10.22.3 Port 18 Registers

The following registers are available on Port 18 :

Table 10-48 Port 18 Registers

Register Short Name	Register Long Name	Offset[1] Address	Description see
P18_OUT	Port 0 Output Register	0000_H	Page 10-155[2]
P18_OMR	Port 0 Output Modification Register	0004_H	Page 10-155[2]
P18_IOCR0	Port 0 Input/Output Control Register 0	0010_H	Page 10-11
P18_IOCR4	Port 0 Input/Output Control Register 4	0014_H	Page 10-12
P18_IN	Port 0 Input Register	0024_H	Page 10-155[2]
P18_PDR0	Port 0 Pad Driver Mode 0 Register	0040_H	Page 10-18

1) The absolute addresses are calculated by adding the offset address to the module base address (see Table 10-4)

2) These registers are listed here in the Port 18 section because they differ from the general port register description given in Section 10.3.

10.22.3.1 Port 18 Output Register

The basic P18_OUT register functionality is described on Page 10-21. Port lines P18.[15:8] are not available. Therefore, the P18_OUT bits P[15:8] should be written with 0 and are always read as 0.

10.22.3.2 Port 18 Output Modification Register

The basic P18_OMR register functionality is described on Page 10-22. Port lines P18.[15:8] are not available. Therefore, the P18_OMR bits PS[15:8] and PR[15:8] are not implemented. These bits should always be written with 0.

10.22.3.3 Port 18 Input Register

The basic P18_IN register functionality is described on Page 10-25. Port lines P18.[15:8] are not available. Therefore, the P18_IN bits P18.[15:8] are always read as 0.

10.22.3.4 Port 18 Emergency Stop Register

The P18_ESR register is not implemented. Nevertheless, access to its address 0xF0300650 does not generate a Bus Error.

11 Peripheral Control Processor (PCP)

This chapter describes the Peripheral Control Processor (PCP), its architecture, programming model, registers, and instructions. The TC1798's PCP is an enhanced version of the TC1767's and TC1797's PCP peripheral control processor, which is an enhanced version of the TC1766's and TC1796's PCP, which is, in turn, an enhanced version of TC1775's PCP.

Section 11.2 of this chapter describes the TC1798's PCP in general. TC1798 implementation-specific details are described in **Section 11.22**.

11.1 PCP Feature/Enhancement History List

The following table lists all PCP enhancements sequentially, for all versions of the PCP. The table will therefore list enhancements that may not apply to the PCP version included in TC1798.

Table 11-1 PCP Feature/Enhancement History List

Version	Enhancement
TC1775	First released version of PCP
TC1766, TC1796	• Optimised Context switching • Support for nested interrupts • Enhanced instruction set • Enhanced instruction execution speed • Enhanced interrupt queueing
TC1767, TC1797	• Enhanced PCP core to support higher clock frequencies • Multiple clock ratios PCP:FPI 1:1 and 2:1 • Adaption of PCP Trace Interface to PAL-MCDS • Implementation of Parity
TC1387, TC1784, TC1798, TC172x Only enhancements in this row and above are included in TC1798	• Support for High Integrity Operation (see **Chapter 11.2.1**). – Programmable ENDINIT write protection for all Registers. – Programmable write protection for CMEM. – Programmable write protection for PRAM. – Programmable limit of FPI addresses than can be written by the PCP. • Implementation of ECC (replacing Parity) • Various Errata fixes.

11.1.1 Switchable Core Clock Ratio

For shorter interrupt latency, shorter uninterruptible task time and increased computing power the PCP is improved to allow operation with a core clock that is faster than the FPI clock (of the FPI Bus to which the PCP is connected). The available clocking ratios (f_{FPI}/f_{PCP}) are 1:1 and 1:2. The clock is controlled and generated in the SCU. The PCP has separate clock inputs for the core and for the FPI-bus related circuits.

11.2 Peripheral Control Processor Overview

The PCP in the TC1798 performs tasks that would normally be performed by the combination of a DMA controller and its supporting CPU interrupt service routines in a traditional computer system. It could easily be considered as the host processor's first line of defence as an interrupt-handling engine. The PCP can unload the CPU from having to service time-critical interrupts. This provides many benefits, including:

- Avoiding large interrupt-driven task context-switching latencies in the host processor
- Reducing the cost of interrupts in terms of processor register and memory overhead
- Improving the responsiveness of interrupt service routines to data-capture and data-transfer operations
- Easing the implementation of multitasking operating systems.

The PCP has an architecture that efficiently supports DMA-type transactions to and from arbitrary devices and memory addresses within the TC1798 and also has reasonable stand-alone computational capabilities.

11.2.1 High Integrity Operation

The PCP can be used in High Integrity Systems to perform various system critical tasks. It follows that, when using the PCP for this function, a fundamental requirement is that the operation of the software running on the PCP must be robust against interference by an external agent (e.g. TriCore). Otherwise a system failure outside PCP could impact the operation of the PCP which might, in turn, cause the system critical task (running on the PCP) to fail.

This concept of immunity is further extended such the PCP can be configured to operate with a number of "Protected" channel programs. These channels are protected not only against failure of external agents but also against software failures in other "Unprotected" channel programs running on the PCP itself.

For High Integrity Systems it is also necessary to prevent the PCP from generating unwanted FPI writes to critical locations in the event of a PCP software malfunction. For this reason a programmable Memory Protection feature is provided to control (in hardware) the address range that can be written to by the PCP.

11.3 PCP Architecture

The PCP is made up of several modular blocks as follows. Please refer to **Figure 11-1**.

- PCP Processor Core
- Code Memory (CMEM)
- Parameter Memory (PRAM)
- PCP Interrupt Control Unit (PICU)
- PCP Service Request Nodes (PSRN)
- System bus interface to the Flexible Peripheral Interface (FPI Bus)

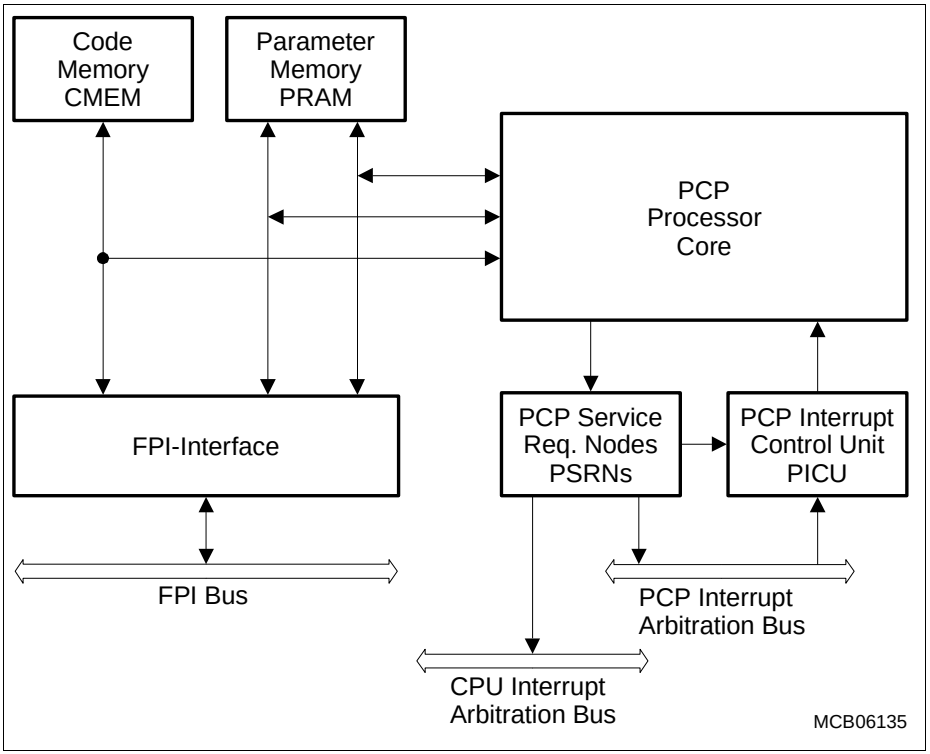


Figure 11-1 PCP Block Diagram

11.3.1 PCP Processor

The PCP Processor is the main engine of the PCP. It contains an instruction pipeline, a set of GPRs, an arithmetic/logic unit (ALU), as well as control and status registers and logic. Its instruction set is optimized especially for the tasks it has to perform. **Table 11-2** provides an overview of the PCP instruction set.

The PCP Processor Core receives service requests from peripherals or other modules in the system via its PCP Interrupt Control Unit (PICU) and executes a channel program (see **Page 11-8**) selected via the priority number of each service request. It first restores the channel program's context from the PRAM and then starts to execute the channel program's instructions stored in the Code Memory (CMEM). Upon an exit condition, it terminates the channel program and saves its context into PRAM. It is then ready to receive the next service request.

The PCP Processor Core is capable of suspending execution of a Channel Program on receipt of a service request with a higher priority than the channel currently being executed. The Core will automatically resume processing of the original Channel Program once the higher-priority request (or requests) has been processed. A channel that has been suspended in this way is termed as "Suspended Channel".

The PCP is fully interrupt-driven, meaning it is only activated through service requests; there is no main program running in the background as with a conventional processor.

Table 11-2 PCP Instruction Set Overview

Instruction Group	Description
DMA Primitives	Efficient DMA channel implementation
Load/Store	Transfer data between PRAM or FPI memory and the GPRs, as well as move or exchange values between registers
Arithmetic	Add, subtract, compare and complement
Divide/Multiply	Divide and multiply
Logical	And, Or, Exclusive Or, Negate
Shift	Shift right or left, rotate right or left, prioritize
Bit Manipulation	Set, clear, insert, and test bits
Flow Control	Jump conditionally, jump long, exit
Miscellaneous	No operation, Debug

11.3.2 PCP Code Memory

The Code Memory (CMEM) of the PCP holds the channel programs, consisting of PCP instructions. All instructions of the PCP are 16 bits long; thus, the PCP accesses its CMEM in 16-bit (half-word) quantities. With the 16-bit Program Counter (PC) of the PCP, a maximum of 64 K instructions can be addressed. This results in a maximum size of the PCP code memory of 128 Kbytes. The actual type (Flash, ROM, SRAM, etc.) and size of the code memory is implementation-specific; see **Page 11-157** for the implemented type and size of the code memory in the TC1798.

The PCP CMEM is viewed from the FPI Bus as a 32-bit wide memory, that must be accessed with 32-bit (word) accesses, and is addressed with byte addresses. Thus, care has to be taken when calculating PCP instruction FPI addresses. See **Page 11-57** for details.

Note: The PCP has a "Harvard" architecture and therefore cannot directly access the CMEM other than reading instructions from it. It is recommended that the PCP should not access CMEM via the FPI Bus.

11.3.2.1 CMEM Protection

To allow the PCP to handle system critical tasks it is necessary to ensure that the PCP can operate properly regardless of a failure in another part of the system or the PCP itself. This means that it is necessary to protect the content of the CMEM from such failures.

CMEM content can only be modified via the FPI. Protection of CMEM therefore consists of prevention of unwanted FPI writes to CMEM.

The normal model of PCP operation is that the program code (i.e. CMEM) is loaded at system initialization and remains unchanged for the duration of operation of the system. Thus a simple locking scheme is provided to prevent any write to CMEM once the content has been loaded during initialization. When CMEM has been loaded (at system initialization) the memory can be locked such that all incoming FPI write accesses are issued with an error response and the CMEM content will remain unmodified.

Regardless of protection the entire CMEM remains readable via FPI.

This function is controlled by the **PCP_CPROT** register (see **Page 11-86**).

11.3.3 PCP Parameter RAM

The PCP Parameter RAM (PRAM) is the local holding place for each channel program's context, and for general data storage. It is also an area that the PCP and the host processor or other FPI Bus masters can use to communicate and share data.

While a portion of the PRAM is always implicitly used for the Context Save Areas (CSAs) of the channel programs (see **Chapter 11.4.2.2**), the remaining area can be used for channel-specific or general data storage. A programmable 8-bit Data Pointer (DPTR),

concatenated with a 6-bit offset, is provided for arbitrary access to the PRAM. The effective address is a 14-bit word address, allowing a PRAM size of up to 64 Kbytes. The actual type (SRAM, DRAM, etc.) and size of the parameter RAM is implementation-specific; see **Page 11-157** for the implemented size of the PRAM in this derivative.

Both the PCP and FPI Bus masters address the PRAM as 32-bit words. There is no concept of half-word or byte accesses to PRAM. FPI Bus masters must, however, use byte addresses in order to access the PRAM. As for the CMEM, care has to be taken when calculating PRAM FPI addresses. See **Page 11-57** for details.

11.3.3.1 PRAM Protection

To allow the PCP to handle system critical tasks it is necessary to ensure that the PCP can operate properly regardless of a failure in another part of the system or the PCP itself. This means that it is necessary to protect all or part of the content of the PRAM from such failures.

All or part of PRAM can be protected from FPI writes using the **PCP_PPROT** register (see **Page 11-87**). This register also allows a region of PRAM to be selected which can only be used by Protected PCP channel programs.

11.3.4 FPI Bus Interface

The PCP can access all peripheral units on the FPI Bus and other resources through the FPI Bus interface. The PCP can become an FPI Bus slave, so that other FPI Bus master may access CMEM and PRAM and the control and status registers in the PCP.

The CMEM and PRAM blocks are visible to FPI Bus masters as a block of memory on the FPI Bus. If an FPI Bus master accesses CMEM or PRAM memory concurrently with the PCP, the external FPI Bus master is given precedence over the PCP to avoid deadlocks. The PCP access is stalled for several cycles until the FPI Bus master has completed its access. If an FPI Bus master performs an atomic read-modify-write access to a PCP memory block, any concurrent PCP access to that block is stalled for the duration of the atomic operation.

11.3.5 PCP Interrupt Control Unit and Service Request Nodes

The PCP is activated in response to an interrupt request programmed for PCP service in one of the Service Request Nodes (SRNs) of the system (nodes associated with a peripheral, the CPU, external interrupts, etc.). The PCP Interrupt Control Unit (PICU) determines the request with the currently highest priority and routes the request together with its priority number to the PCP Processor Core. It also acknowledges the requesting source when the PCP starts the service of this interrupt.

The PCP itself can generate service requests to either the CPU or itself through a number of PCP Service Request Nodes (PSRNs). The PSRNs are also used to store all information required by the PCP Processor Core to allow the later restart of a channel

program when it is suspended in favor of a higher-priority Service Request. Please refer to **Section 11.6.3** for more detailed information on the operation of these nodes.

11.4 PCP Programming Model

The PCP programming model can be viewed as a set of autonomous programs, or tasks, called channel programs, that share the processing resources of the PCP. Channel programs may be short and simple, or very complex; but they can coexist persistently within the PCP.

From the programming point of view, the individual parts of a channel program are its instruction sequence in the CMEM and its context in the PRAM. It uses the instruction set and the GPRs (R0 - R7) of the PCP Processor Core to perform the necessary operations, and to communicate with the various resources of the on-chip and off-chip system depending on its task in the application.

These parts of the programming model are discussed in the following sections (with the obvious exception of the system environment outside of the scope of the PCP).

11.4.1 General Purpose Register Set of the PCP

The program-accessible register file of the PCP is composed of eight 32-bit General Purpose Registers (GPRs). These registers are all accessible by PCP programs directly as part of the PCP instruction set. Source and destination registers must be specified in most instructions. These registers are referenced to in this document as Rn or R[n], where n is in the range 0 to 7.

Table 11-3 Directly Accessible Registers

Register	Implicit Use	Description
R0	Accumulator	Implicit target for some arithmetic and logical instructions
R1	–	32-bit general-use register
R2	Return Address	32-bit general-use register
R3	–	32-bit general-use register
R4	SRC (Source)	Source Pointer for BCOPY/COPY instructions
R5	DST (Destination)	Destination Pointer for BCOPY/COPY instruction
R6	CPPN/SRPN/ TOS/CNT1	CNT1: Transfer Count for COPY TOS: Type-of-Service SRPN: 8-bit field used for posting interrupt on EXIT instruction CPPN: Current PCP Priority Number
R7	DPTR/Flags	PRAM Data Pointer (DPTR) and Status Flags

R7 is the only one of the eight registers that may not be used as a full GPR. The most significant 16 bits of R7 may not be written, and will always read back as 0. However, no error will occur when writing to the most significant 16 bits.

Note: The GPRs of the PCP are not memory-mapped into the overall address space. They can only be directly accessed through PCP instructions. The contents of all or some of the registers are part of a channel program's context stored in the PRAM between executions of the channel program. This context is then accessible from outside the PCP.

11.4.1.1 Register R0

R0 is used as an implicit operand destination for some instructions. These are detailed in the individual instruction descriptions.

11.4.1.2 Registers R1, R2, and R3

R1, R2, and R3 are general-use registers. It is recommended that, by convention, R2 should be used as a return address register when call and return program structures are used.

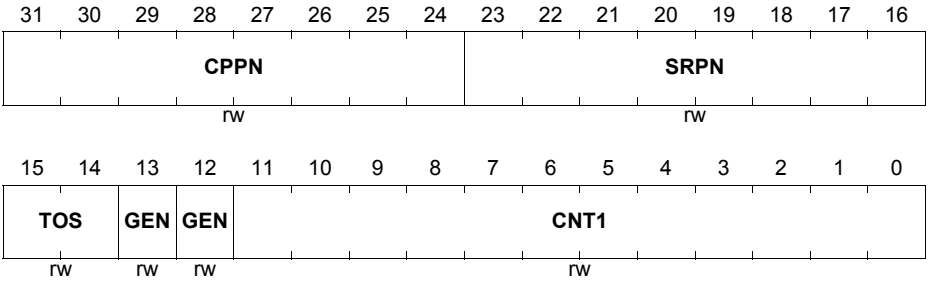
11.4.1.3 Registers R4 and R5

Registers R4 and R5 are also general-use registers. However, the BCOPY/COPY instructions implicitly use R4 and R5 as full 32-bit address pointers (R4 is used as the source address and R5 as the destination address). As the BCOPY/COPY instructions use these registers to maintain the address pointers, either or both R4 and R5 values may or may not be modified by the BCOPY/COPY instructions, depending on the options used in the instructions.

11.4.1.4 Register R6

Register R6 may also be used as a general-use register. Again however, there are some instructions that use fields within R6. If the COPY or EXIT instructions are used, then the field R6.CNT1 can optionally be used implicitly as a counter. If an EXIT instruction is used that causes an interrupt, R6.SRPN and R6.TOS must be configured properly prior to execution of the EXIT. If interrupt priority management is used, then R6.CPPN must be set to the priority level at which the channel shall run at its next invocation, before the EXIT is executed. The fields for R6 are shown below.

PCP Register R6 **Reset Value: 0000 0000$_H$**



Field	Bits	Type	Description
CPPN	[31:24]	rw	**General-use/PCP Priority Number Posted to PICU**
SRPN	[23:16]	rw	**General-use/Service Request Priority Number for EXIT Interrupt**
TOS	[15:14]	rw	**General-use/Type-of-Service for EXIT Interrupt** Upper bit of TOS is always forced to 0 when transferred into the PCP SRNs, regardless of the value specified in R6[15].
GEN	13	rw	**General-use**
GEN	12	rw	**General-use**
CNT1	[11:0]	rw	**General-use/Outer Loop count for COPY Instruction or EXIT Instruction**

11.4.1.5 Register R7

Register R7 is an exception with respect to the other registers in that not all bits within the register can be written, and the implicit use of the remaining bits virtually excludes the use of R7 as a GPR. R7 serves similar purposes as those in the Program Status Word found in traditional processors.

R7 holds the flag bits, a channel enable/disable control bit, and the PRAM Data Pointer (DPTR). The upper 16 bits of R7 are reserved.

Most instructions of the PCP update the flags (CN1Z, V, C, N, Z) in R7 according to the result of their operation. See **Table 11-15** on **Page 11-134** for details on the flag updates of the individual instructions. The values of the flag bits in R7 maintain their state until another instruction that updates their state is executed.

Note: Implicit updates to the flags caused by instruction take precedence over any bits that are explicitly moved to R7. For example, if a MOV instruction is used to place $0000FF07_H$ in R7, then the bit positions for the C (carry), Z (zero) and N (negative) flags are being written with 1. The MOV instruction, however, implicitly updates the Z and N flag bits in R7 as a result of its operation. Because the number is not negative, and not zero, it will update the Z and N flags to 0. As a result, the value left in R7 after the MOV is complete will be $0000FF04_H$ (i.e C = 1, Z = 0, N = 0). It is recommended that only SET and CLR instructions should be used to explicitly modify flags in R7.

The Data Pointer, R7.DPTR, is the means of accessing PRAM variables programmatically. It points to a 64-word PRAM segment that may be addressed by instructions that can use the PRAM for source or destination operands (xx.P and xx.PI instructions). The 8 bits of the DPTR are concatenated with a 6-bit offset value (either specified in the instruction as an immediate value or contained in one of the registers) to give a 14-bit (word) address. A program is able to update the DPTR value dynamically, in order to index more than 64 words of PRAM.

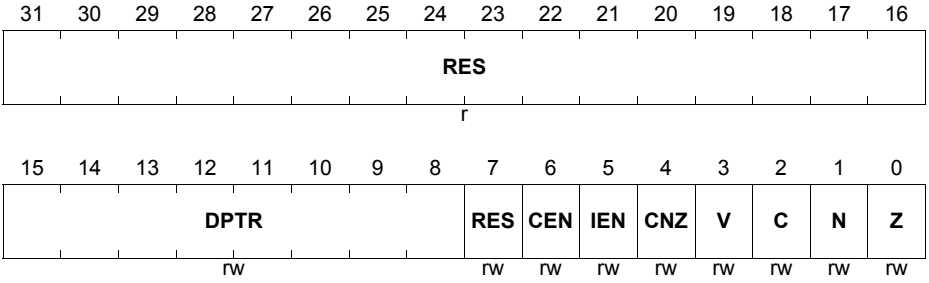
Note: Care must be taken when updating R7.DPTR to ensure that other bits within R7 (e.g. R7.CEN) are not inadvertently corrupted.

The channel enable control bit, R7.CEN, allows the enabling or disabling of specific channel programs. If an interrupt request is received for a channel that is disabled an error exit is forced, and an error interrupt to the CPU is activated.

The interrupt enable control bit, R7.IEN, allows the enabling or disabling of channel interruption on a channel to channel basis. When R7.IEN is 0, the channel will continue its execution regardless of the priority of any new service requests. When R7.IEN is 1, and conditions allow, the channel will be suspended on receipt of a higher-priority service request.

*Note: See **Section 11.21.3.1** regarding the use of R7.IEN.*

PCP Register R7 **Reset Value: 0000 0000$_H$**



Field	Bits	Type	Description
RES	[31:16]	r	**Reserved** read as 0; should be written with 0.
DPTR	[15:8]	rw	**Data Pointer Segment Address for PRAM accesses**
RES	7	rw	**Reserved** should always be written with 0.
CEN	6	rw	**Channel Enable Control Bit**
IEN	5	rw	**Interrupt Enable** 0_B Channel is not interruptible 1_B Channel can be suspended in favor of a higher-priority service request
CNZ	4	rw	**Outer Loop Counter 1 Zero Flag**
V	3	rw	**Overflow**
C	2	rw	**Carry**
N	1	rw	**Negative**
Z	0	rw	**Zero**

11.4.2 Contexts and Context Models

After initialization, the instruction sequence of a PCP channel program is permanently stored (i.e. usually at least as long as the application is running) in the CMEM, and data parameters are held in the PRAM. These will remain stored regardless of whether a particular channel program is currently idle or is executing (although, of course, the value of data variables in the PRAM might be modified by the PCP or external FPI Bus masters). The contents of the GPRs of the PCP (used as address pointers, data variables, intermediate results, etc.) however, are usually only valid for a given channel program as long as it is executing. If another channel program is executed, the channel program will re-use the GPRs according to its needs.

Thus, the state of the GPRs of a channel program (termed the “Context” of the channel) needs to be preserved while a channel program is not being executed. The content of the registers needs to be saved when execution of a channel program finishes, and needs to be restored before execution starts again.

The PCP implements automatic handling of these context save and restore operations. On termination of a channel program, the state of all or some of the GPRs is automatically copied to a defined area in the PRAM (Context Save). If the same channel program is re-activated, the contents of the registers are restored by copying the values from the same defined PRAM area into the appropriate registers (Context Restore).

The defined area in the PRAM for the context save and restore operations is called the CSA. Each channel program has its own individual, predefined region in the CSA. When a service request is accepted by the PCP, the service request priority number (SRPN) associated with the request is used to select the channel program and its respective CSA region.

11.4.2.1 Context Models

A Context Model is a means of selecting whether some or all of the registers are saved and restored when a context switch occurs. In order to serve different application needs in terms of PRAM space usage, the PCP offers a choice between three different Context Models:

- Full Context Model: Eight Registers (8 × 32-bit words) are saved/restored per channel.
- Small Context Model: Four Registers (4 × 32-bit words) are saved/restored per channel.
- Minimum Context Model: Two Registers (2 × 32-bit words) are saved/restored.

As illustrated in **Figure 11-2**, the contents of R0 through R7 constitute the Full Context of a channel program. A Small Context consists of R4 through R7. Use of the Small Context Model allows for correct operation of DMA channels, as well as channels which are not required to save large amounts of data in their contexts between invocations. A Minimum Context saves and restores only R6 and R7.

To distinguish the actual register contents from the copies stored in the PRAM context regions, the term CRx is used throughout the rest of this document to refer to the register values in the context regions. Registers R6 and R7 are always handled in a special way during context save and restore operations, this is described in detail in **Section 11.4.2.3**.

The Context Model is selected via bit field (PCP_CS.CS), this is a global setting (i.e. the selected Context Model is used for all channels). Once a context model has been selected (during PCP configuration) and the PCP has been started the PCP must continue to use that Context Model. Attempting to change the Context Model in use during PCP operation will lead to invalid context restore operations which will in turn lead to invalid PCP operation.

In the case of Small and Minimum Context Models, the unsaved and un-restored registers (shaded in **Figure 11-2**) can be thought of as global registers that any channel program can use or change, or reference as constants – for example as base address pointers (see **Section 11.20.2** for more detail).

*Note: Special care must be taken when using Minimum or Small Context Model with nested interrupts (see **Page 11-151**).*

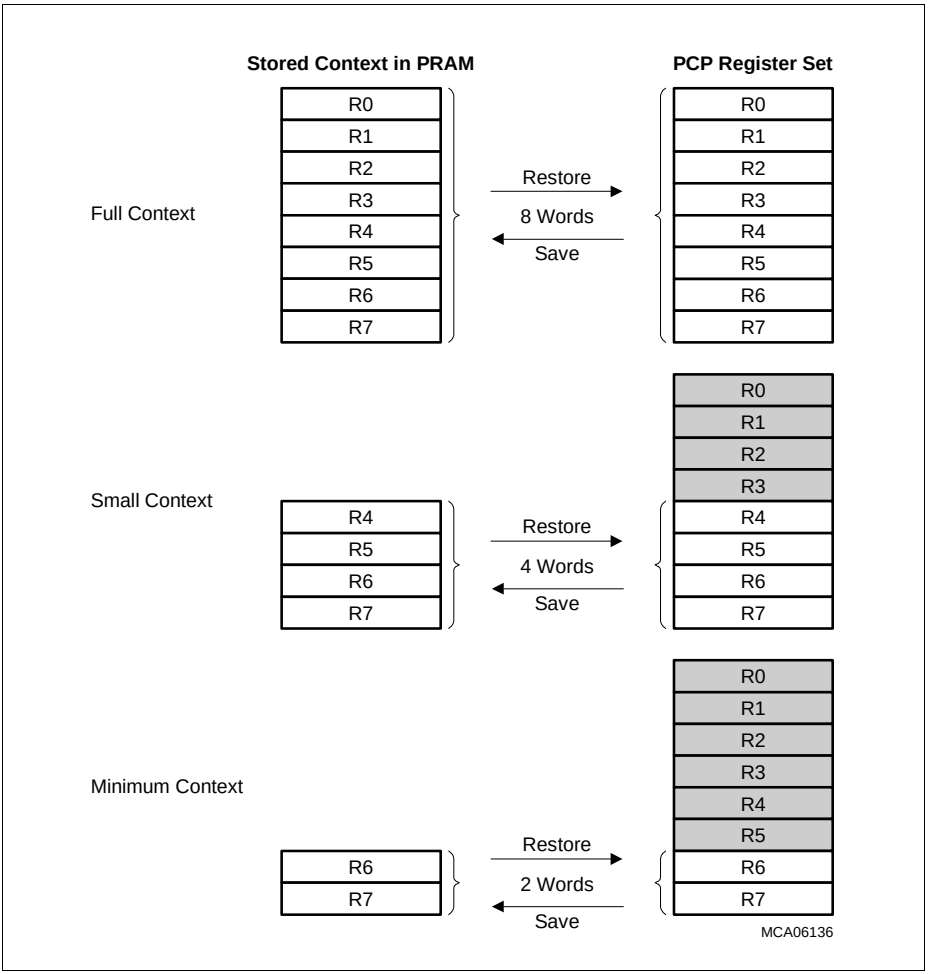


Figure 11-2 PCP Context Models

11.4.2.2 Context Save Area

The Context Save Area (CSA) is a region in PRAM reserved for storing the contexts for all channel programs (while any particular channel is not executing). Each channel's context is stored in a region of the CSA based on the channel number. The channel number is equal to the priority number (SRPN) of the service request. The PCP uses this number to calculate the start address of the context of the associated channel program. The size of a context is determined by the Context Model that the PCP has been initialized to use. As all channels use the same context size, the PRAM address (word address) of the context for a particular channel is simply calculated by multiplying the channel number by the number of registers in the context (8 for Full Context, 4 for Small Context and 2 for Minimum Context). **Figure 11-3** shows the resulting PRAM layout, and from this it can be seen that changing the Context Model also changes the base address for all regions within the CSA. Thus, the chosen Context Model may only be set when the PCP is initialized, and may not be changed during operation.

The CSA in the PRAM starts at address 00_H and grows upward. It is partitioned into equally sized regions, where the size of these regions is determined by the selected Context Model. The priority number (SRPN) of a service request is used to access the appropriate context region for the associated channel program. Since a request with an SRPN of 00_H is not considered as valid request in the TriCore Architecture, the bottom region (context region 0) of the CSA is never used for an actual context.

The total size of the CSA depends on the Context Model and the number of service request numbers used in a given system. Each priority number used in a service request node which can activate interrupts to the PCP must be represented through a dedicated context region in the PRAM. The highest address range in the PRAM used for a context region is determined by the highest priority number presented to the PCP with a service request.

The range of usable priority numbers is further determined by the size of the implemented PRAM and by the space required for other variables and global data located in the PRAM. See **Page 11-157** for the implemented size of the PRAM in the TC1798. As an example, a PRAM of 2 Kbytes, solely used for the CSA, can store up to 255 Minimum Contexts, allowing the highest SRPN used for a PCP service request to be 255 (remember, an SRPN of 0 and an associated context region is never used; the valid SRPNs and the context and channel numbers range from 1 to 255). With a Small Context Model, 127 contexts can be stored, resulting in 127 being the highest usable SRPN in this configuration. Finally, a Full Context Model allows 63 context areas, with 63 being the highest usable SRPN. Interrupt requests to the PCP with priority numbers that would cause loading of a context from outside the available PRAM area must not be generated. Invalid PCP operation will result should this situation be allowed to occur. The PCP can be optionally configured such that if an interrupt request is received that would cause loading of a context from outside the available PRAM area then an error exit is forced, and an error interrupt to the CPU is activated (see **Page 11-44**).

If portions of the PRAM are used for other variables and global data, the space available for the CSA and the range of valid SRPNs is reduced by the memory space required for this data. For best utilization of PRAM, it is advisable to have the CSA grow upwards as a contiguous area without any “holes”, meaning that all SRPNs in the range 1 … max. are actually used to place interrupt requests on the PCP. Unused regions within the CSA (that is, the unused region at the base of the CSA and any context regions associated with unused channels) cannot be used for general variable storage.

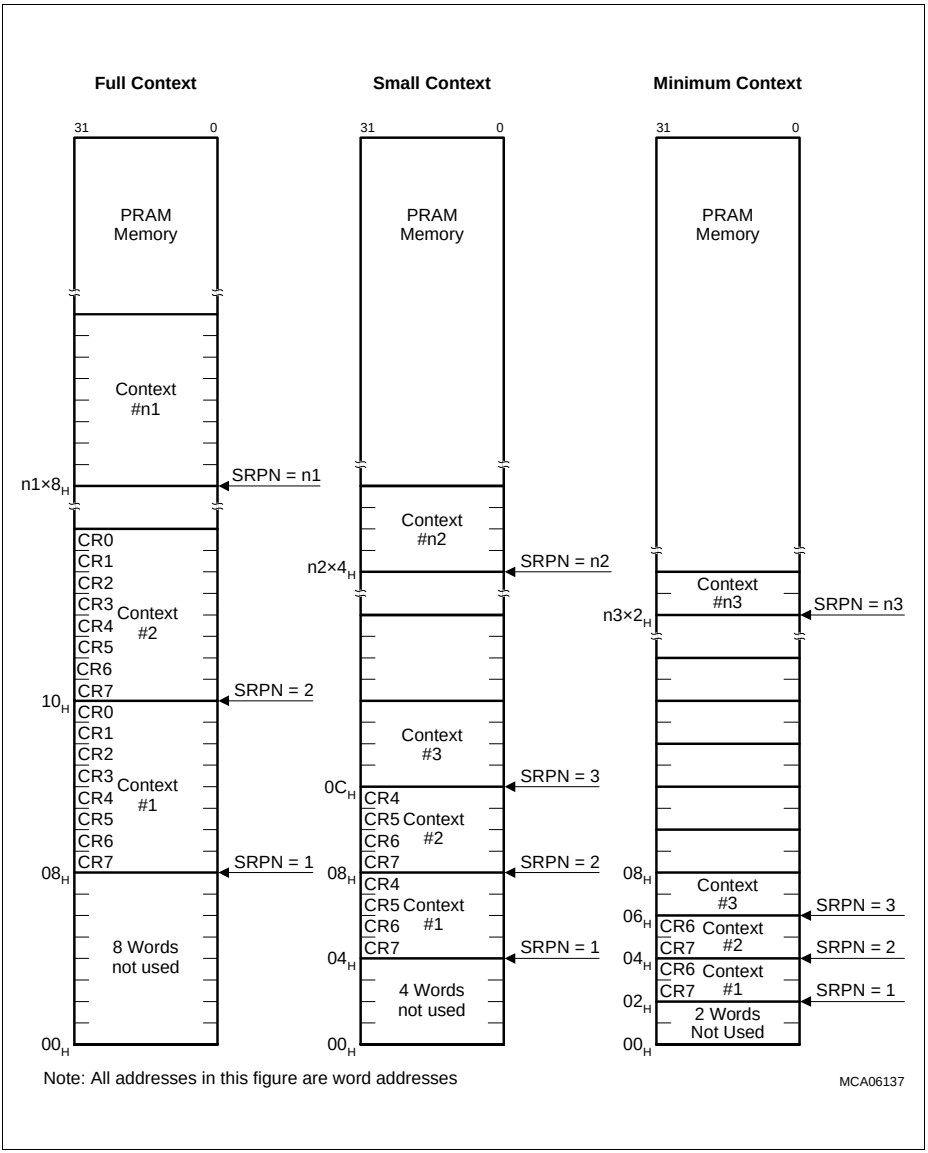


Figure 11-3 Context Storage in PRAM

When choosing the Context Model for a given application, the following considerations can be helpful. When choosing the Small or the Minimum Context Models, save and restore operations for registers not handled in the automatic context operations can still be handled through explicit load and store instructions under control of the user. This may be advantageous for applications in which the majority of the channels do not need the Full Context, and only some would require more context to be saved. In this case, a Smaller Context Model can be used, and the channels which would require more register to be saved/restored would do this via explicit load and store instructions. This is especially advantageous if the channel program can be designed such that the initial real-time response operations can be executed using only the registers which have been automatically restored. Then, as the timing requirements of the service are relaxed, further register contents can be restored from PRAM through regular load instructions. Of course, the contents of these registers needs to be explicitly saved, through regular store instructions, before the exit of the channel program.

Note: Special care must be exercised when using Minimum or Small Context Models in conjunction with nested interrupts (see **Page 11-151***).*

The criteria for choosing the Context Model are listed in the following:

- Size of PRAM implemented in a given derivative
- Amount of channels (= SRPNs) that need to be used in a system
- Amount of PRAM used for general variables and global's
- Amount of context (register content) which need to be saved and restored quickly by most of the most important channels

While registers R0 through R5 are always restored in a normal manner (according to the context size), registers R6 and R7 merit discussion regarding context restore operations. The memory location CR7 in a context region is used to hold two different pieces of information: The lower part of register R7, and the PC value of the channel. Similarly, the memory location CR6 in a context region can also be used to hold two different pieces of information: The value to be restored to register R6, and the Operating Priority (CPPN) value of the channel. This leads to the Restore/Save operations described in the following two sections.

11.4.2.3 Context Restore Operation for CR6 and CR7

The operation of R6 and R7 context restore varies according to whether the channel program that is starting is a "new" channel program (i.e. a channel program that is starting in response to the receipt of a new service request) or is a "suspended" channel program (i.e. a channel program that is re-starting after being suspended in favor of a higher-priority channel program). In addition, when a "new" channel program is starting, the context restore operation depends on the channel start mode that has been selected (see **Page 11-27**).

Channel Resume Mode

Figure 11-4 illustrates the operation of a context restore for a “new” channel program when Channel Resume Mode has been selected (see Page 11-28). The PC is loaded from CR7[31:16], and the lower half of R7 is loaded from CR7[15:0]. The operating priority of the channel is taken from CR6[31:24] and all of R6 is loaded from CR6.

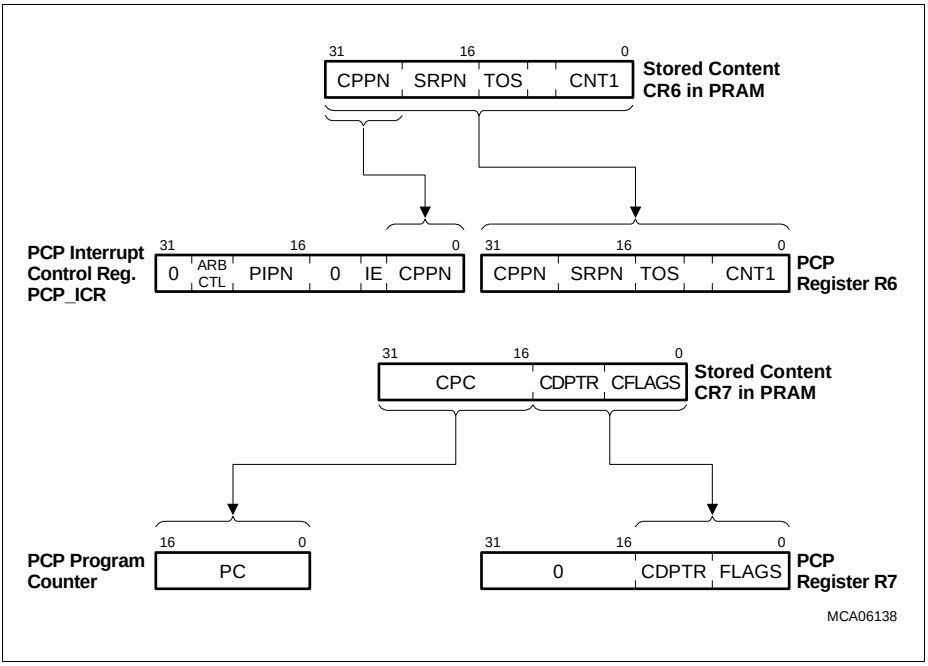


Figure 11-4 Context Restore: Channel Start in “Channel Resume Mode”

Channel Restart Mode

Figure 11-5 illustrates the operation of a context restore for a “new” channel program when Channel Restart Mode has been selected (see Page 11-27). The PC is loaded with the channel entry table address, and the lower half of R7 is loaded from CR7[15:0]. The upper half of CR6 is discarded. The operating priority of the channel is taken from CR6[31:24] and all of R6 is loaded from CR6.

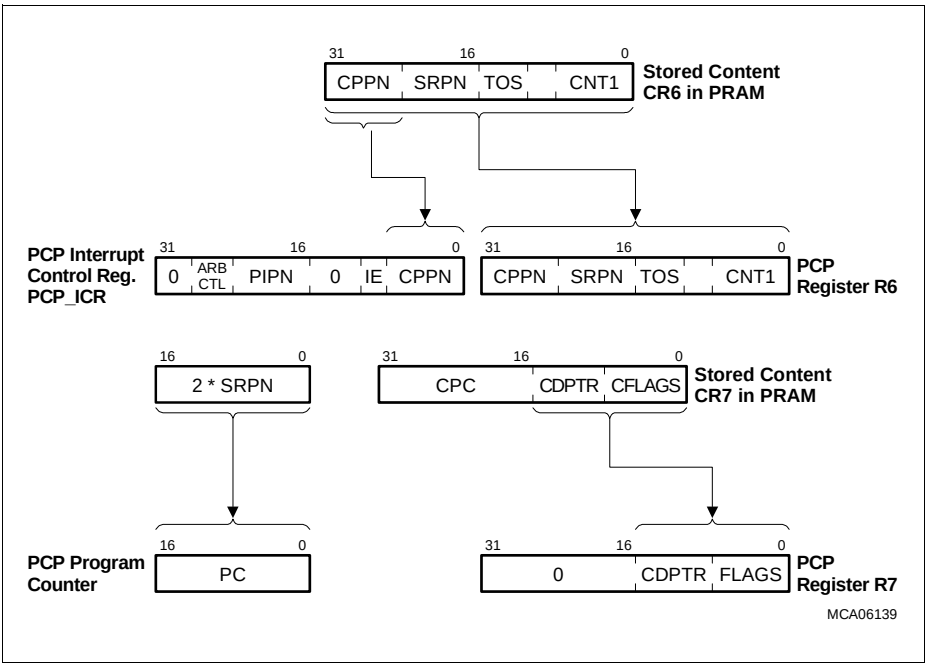
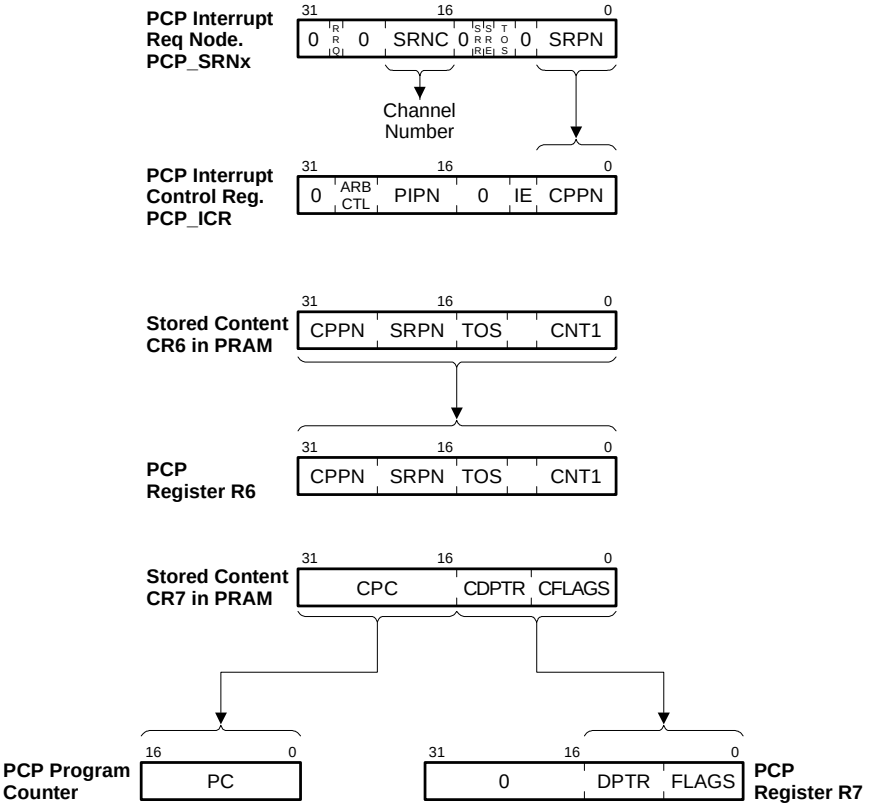


Figure 11-5 Context Restore: Channel Start in Channel Restart Mode

Suspended Channel Restart

Figure 11-6 illustrates the operation of a context restore for a “suspended” channel program. The PC is loaded from CR7[31:16] (regardless of the Channel Start Mode), and the lower half of R7 is loaded from CR7[15:0]. All of R6 is loaded from CR6. The figure also shows how the operating priority of the channel (PCP_IR.CPPN) is restored from the Service Request Node that was used to store the Suspended Interrupt Request (see Page 11-96).



Note: During a context restore for a suspended channel the PCP_SRCNx.SRNC field (n = 9, 10, 11) is used to determine the channel number.

MCA06140

Figure 11-6 Context Restore: Suspended Channel Restart

11.4.2.4 Context Save Operation for CR6 and CR7

The operation of R6 and R7 context save varies according to whether the save operation is the result of a channel exit condition, or whether the channel is being suspended in favor of a higher-priority channel program.

Channel Resume Mode

Figure 11-7 illustrates the operation of a context save for a channel exit when Channel Resume Mode has been selected. The value written to CR7 is created by concatenating the 16-bit PC value with the lower 16 bits of R7. CR6 is written with the value taken from R6.

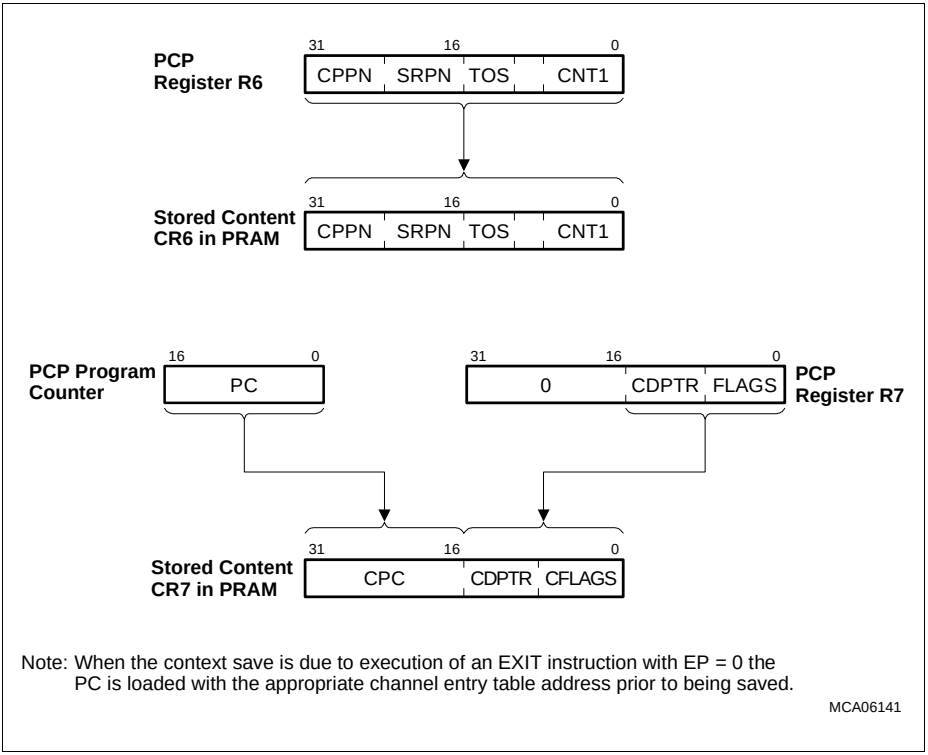


Figure 11-7 Context Save: Channel Exit in Channel Resume Mode

Channel Restart Mode

Figure 11-8 illustrates the operation of a context save for a channel exit when Channel Restart Mode has been selected. This is the same as for Channel Resume mode except that the PC value is discarded, and the appropriate Channel Entry Table address is written to CR7[31:16].

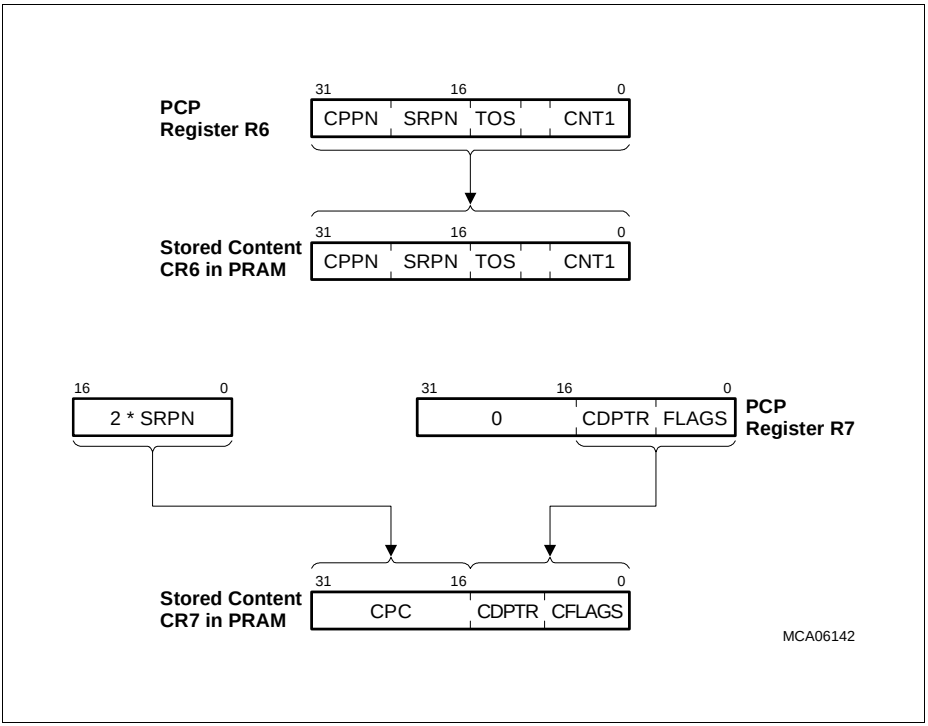


Figure 11-8 Context Save: Channel Exit in Channel Restart Mode

Channel Suspend

Figure 11-9 illustrates the operation of a context save for a channel that is being suspended. This is the same as for Channel Resume mode except that an interrupt request is created to allow the channel to be restarted at a later time. This restore operation utilizes one of three specially extended SRNs (see Page 11-96) to store the interrupt request. The information stored as part of the interrupt request is the channel number (SRPN), and the operating priority (CPPN) with which the channel was operating prior to being suspended. This operation in conjunction with the suspended channel restore operation shown in Figure 11-6 allows the temporary suspension of a channel in favor of a higher-priority channel.

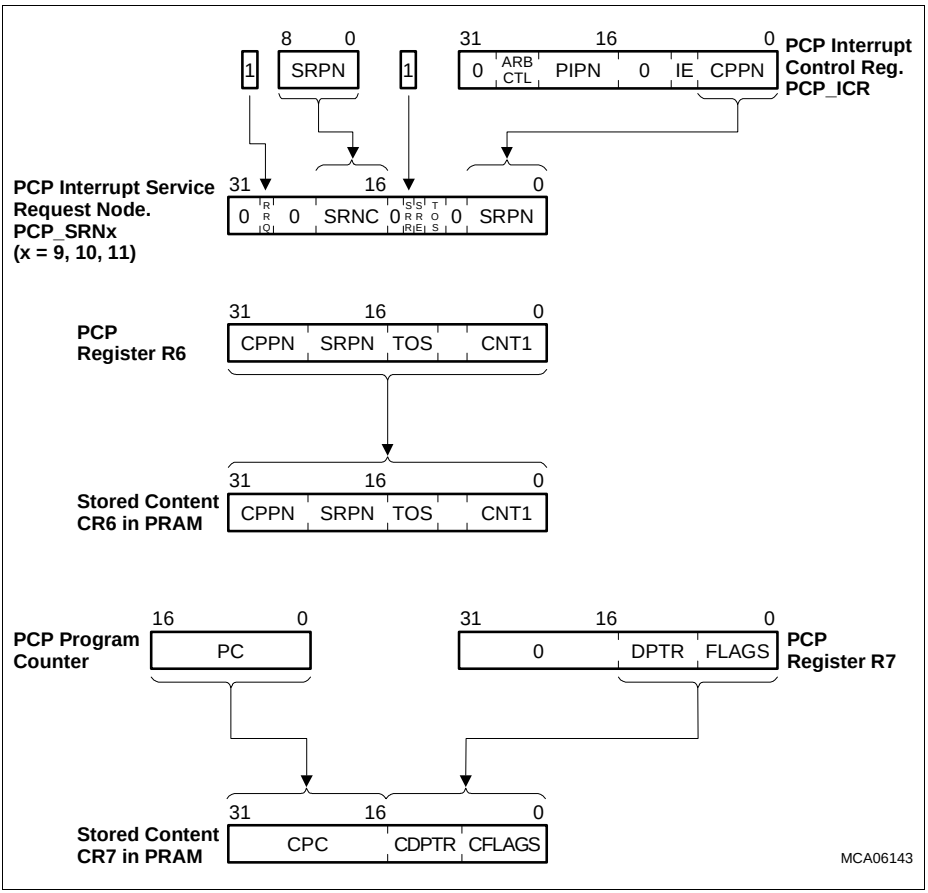


Figure 11-9 Context Save: Channel Suspend

11.4.2.5 Initialization of the Contexts

The programmer is responsible for configuring each channel program's context before commencing operation. Because this must be done by writing to the PCP across the FPI Bus, it is important to understand exactly where each channel program's context is from the FPI Bus perspective (see **Page 11-58** for details).

11.4.2.6 Context Save Optimization

The PCP has an optimized context-switching strategy consisting of optimization of both context load and store. During a context load in which the channel that is starting is also the last channel that the PCP was running then the PCP GPRs already contain the values appropriate to the channel. In this case there is no need to reload the context (i.e. the PCP can immediately continue operation at the appropriate point in the code without having to perform a context load). During a Context Store (i.e. the PCP exits a channel as a result of EXIT or DEBUG instructions or exits in response to a higher-priority channel interrupt), only those registers that have been updated (i.e. written to) since the context was loaded are saved to the CSA.

11.4.3 Channel Programs

The PCP CMEM is used to store the instruction sequences, the channel programs, for each of the PCP channels. The individual channel programs for the individual PCP service requests can usually be viewed as independent and separate programs. There is no background program defined and running for the PCP in TC1798 as there would be with traditional processors.

When the PCP receives a service request for a specific channel program, it needs to determine exactly which channel program to activate and where to start its execution. To accommodate different application needs, the PCP architecture allows the selection of two different entry methods into the channel programs:

- Channel Restart Mode
- Channel Resume Mode

Channel Restart Mode forces the PCP to begin each channel program from a known fixed point in the CMEM that is related to the interrupt number. At the entry point related to the interrupt number in question, there will typically be a jump instruction which vectors the PCP to the main body of the channel program. This is identical to the traditional interrupt vector jump table. In Channel Restart Mode, channel code execution will always start at the same address in the interrupt entry table each time the channel is requested.

Channel Resume Mode allows the PCP to begin execution at the PC address restored as part of the channel program context. This mode allows code to be contiguous and start at any arbitrary address. It also allows for the implementation of interrupt-driven state machines, and even the sharing of code across multiple programs with different context.

The selection of one of the two modes is a global PCP setting, that is, it applies to all channels. Selection is made via the PCP_CS.RCB bit in the PCP configuration register PCP_CS (see **Page 11-69**).

11.4.3.1 Channel Restart Mode

Channel Restart Mode is selected with PCP_CS.RCB = 1. In this mode, the PCP views the CMEM as being partitioned into an interrupt entry table at the beginning of the CMEM, and a general code storage area above this table.

The interrupt entry table consists of two instruction slots (2×16-bit) for each channel. When a PCP service request is received, the PCP calculates the start PC for the requested channel by a simple equation based on the SRPN of that request (PC = $2 \times$ SRPN). It then executes the instruction found on that address. If more than two instructions are required for the operation of the channel program, then one of the instructions within the interrupt entry table must be a jump to the remainder of the channel's code. The PCP executes the channel's code until an exit condition or higher-priority interrupt is detected.

It is recommended that all EXIT instructions for all channels should use the EP = 0 setting when the PCP is operated in Channel Restart Mode (see **Page 11-115**).

Note that when Channel Restart Mode is in use a Channel Entry Table must be provided with a valid entry for every channel being used. **Figure 11-10** shows an example of CMEM organization when Channel Restart Mode has been selected. Failure to provide a valid entry for all channels that are in use will lead to invalid PCP operation.

11.4.3.2 Channel Resume Mode

Channel Resume Mode is selected with PCP_CS.RCB = 0. In this mode, the user can arbitrarily determine the address at which the channel program will be started the next time it is invoked. For this purpose, the PC is saved and restored as part of the context of a PCP channel.

Additional flexibility is available when Channel Resume Mode is globally selected by configuring each EXIT instruction to determine the channel start address to be used on the next invocation of a channel (see **Page 11-115**). When the EP = 0 setting is used, the PC value saved in the channel's context (saved in CPC) is the address of the appropriate location in the channel entry table. This forces the channel to start at the appropriate location in the interrupt entry table at next invocation. When the EP = 1 setting is used, the PC value saved in the channel's context is the address of the instruction immediately following the EXIT instruction. The use of the EP = x setting with the EXIT instruction allows the mixture of channels that use a Channel Restart strategy with others using a Channel Resume strategy, and also allows individual channels to use either strategy as appropriate on different invocations.

Note: A valid entry within a Channel Entry Table must be provided for every channel that uses an EXIT instruction with the EP = 0 setting when Channel Resume Mode has been selected. Failure to provide a valid entry for such channels will lead to invalid PCP operation.

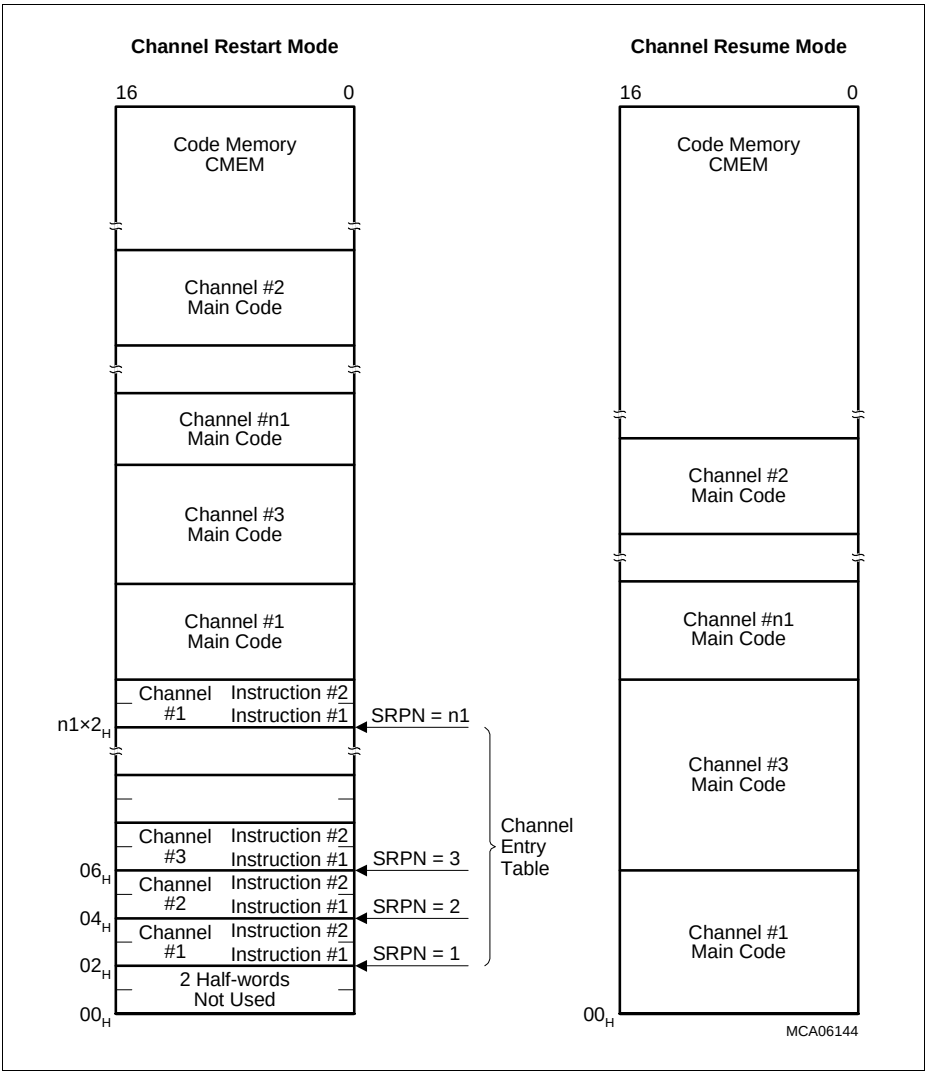


Figure 11-10 Examples of Code Memory Organization for Channel Restart and Channel Resume Modes

Note: The CMEM address offsets in the above figure are shown as PCP instruction (half-word) offsets. To obtain FPI address offsets (byte offset) multiply each offset by two.

11.5 PCP Operation

This section describes how to initialize the PCP, how to invoke a channel program, and the general operation of the PCP.

11.5.1 PCP Initialization

The PCP is placed in a quiescent state when the TC1798 is first powered-on or reset. Before a channel program can be enabled, the PCP as a whole must be initialized by some other FPI Bus master, typically the CPU. Initialization steps include:

- Configure global PCP registers.
  - Initialize PCP Control and Status Register (with PCP_CS.EN = 0).
  - Configure interrupt system via PCP_ICR.
- Load channel programs into the CMEM.
- Load initial context (if/as required) of channel programs in PRAM (R0 - R7 for Maximum context, R4 - R7 for Small Context, R6 - R7 for Minimum Context). Only those registers in each channel whose initial content is required on first invocation of the channel need to be loaded. This may need to include the initial PC, depending on the value of PCP_CS.RCB.
- Clear R7 in the context for unused channels.
- Enable PCP operation PCP_CS.EN = 1.

Now, the PCP is able to begin accepting interrupts and executing channel programs.

11.5.2 Channel Invocation and Context Restore Operation

A channel program is started when one or other of the following conditions occurs:

- The current round of PCP interrupt arbitration results in a winning interrupt number (SRPN) and the PCP is currently quiescent (has exited the previous channel and stored the context for that channel).
- The current round of PCP interrupt arbitration results in a winning interrupt number (SRPN) that has to be greater than the current channel priority (SRPN > CPPN), if suitable Service Request Node space is available in the PSRN to store a suspended interrupt request and the current channel allows interrupts (R7.IEN = 1). See also **Page 11-35**).

When this happens the winning SRPN becomes the current interrupt, and a context restore operation occurs before the new channel program can begin operation, as follows:

- The context of the channel (= winning SRPN) is restored from PRAM into the GPRs from the appropriate address within the CSA. Depending on the value of PCP_CS.CS, a Full, Small, or Minimum Context restore is performed.
- The new priority level of the PCP is taken from R6.CPPN field and is written to PCP_ICR.CPPN. This value can be useful during debugging, as the CPPN of the currently executing or last-executed channel program can be read from PCP_ICR.

After the channel program starts, the value of R6 may be changed without altering the value of the effective CPPN, because updates to the value of R6.CPPN have no effect until the next invocation of the channel program.

- If the R7.CEN bit is clear (0), then an error has occurred because a disabled channel program has been invoked, the PCP_ES.DCR bit is set to flag the error, and the channel program performs an error exit (see Page 11-31).
- If the R7.CEN bit is set (1), then code execution begins at the value of the restored PC or at the address of the interrupt routine in the Channel Entry Table, depending on the value of PCP_CS.RCB.

Special care needs to be taken regarding the number of clock cycles required to switch context when the last state of the PCP before channel exit was execution of channel “N” (SRPN = “N”), and the current service request is also SRPN = “N”. In this case, the PCP Processor Core should not load the context (as the PCP GPRs already contain the correct content), but continue operation from the current point and state (noting that the PC value should be set to the appropriate channel entry point if PCP_CS.RCB = 1).

11.5.3 Channel Exit and Context Save Operation

The context of a channel program must be saved when it terminates. Three events can cause the termination of a channel program:

- Execution of the EXIT instruction (normal termination)
- Occurrence of an error
- Execution of the DEBUG instruction (channel termination is optional). The DEBUG instruction must only be used in DEBUG mode; otherwise an “Illegal Operation” (IOP) error will be generated

These channel termination possibilities are described in the next sections.

11.5.3.1 Normal Exit

Under normal circumstances, a channel program finishes by executing an EXIT instruction. This instruction has several setting fields that allow the user to specify a number of optional actions to be performed during the channel exit sequence (see Page 11-115). These optional actions are:

- Decrement counter CNT1
- Set the start PC for the next channel invocation to the next instruction address (Channel Resume) or to the channel entry address (Channel Restart)
- Disable further invocations of this channel
- Generate an interrupt request to the CPU or to the PCP itself

When the EXIT instruction is executed, the following sequence occurs:

- If EC = 1 is specified Counter R6.CNT1 is decremented and the CN1Z flag is updated.

- If ST = 1 is specified bit R7.CEN (Channel Enable) is cleared (i.e. the channel is disabled).
- If EP = 0 is specified **or** PCP_CS.RCB = 1 (Channel Restart Mode has been selected), the PCP program counter to be saved to context location CR7.PC is set to the appropriate channel entry table address. If EP = 1 is specified **and** PCP_CS.RCB = 1 (Channel Resume Mode has been selected), the PCP program counter to be saved to context location CR7.PC is set to the address of the instruction immediately following the EXIT instruction.
- If INT = 1 is specified **and** the specified condition cc_B is True, then an interrupt request is raised according to the SRPN value held in R6.SRPN. The interrupt is asserted via one of the PCP_SRCx registers, where x is determined by the combination of the value of R6.TOS and the list of free entries. This allows the conditional creation of a service request to the CPU or PCP with the SRPN value indicated in register R6.SRPN.
- The channel program's context (including all register modifications caused within this EXIT sequence) is saved to the appropriate region in the PRAM Context Save Area. Depending on the value of PCP_CS.CS, either a Full, Small, or Minimum Context save is used.

Special care needs to be taken to optimize the number of clock cycles required to perform a Context Save. During a Context Save, the PCP Processor Core needs only to save those registers that have been written since the last Context Restore was performed.

Note: Particular attention must be paid to the values of R6 and R7 prior to execution of the EXIT instruction. When posting an interrupt request, the user must ensure that R6.SRPN and R6.TOS contain the correct values to generate the required interrupt request. When using the Outer Loop Counter (CNT1), the user must ensure that the value in R6.CNT1 will provide the required function. When using interrupt priority management, the user must ensure that R6.CPPN contains the interrupt priority with which the channel is to run on next invocation. If the channel is to be subsequently re-invoked, the user must ensure that the Channel Enable Bit (R7.CEN) is set.

11.5.3.2 Error Condition Channel Exit

PCP error conditions can occur for a variety of reasons (e.g. an invalid operation code was executed by a channel program, or an FPI Bus error occurred). When an error condition occurs, the PCP Error Status Register (PCP_ES) is updated to reflect the error, and the channel program is aborted. The error exit sequence is as follows:

- The channel enable bit R7.CEN is cleared. This means the channel program will be unable to restart until another FPI Bus master has re-configured the channel program's stored context to set CR7.CEN to 1 again.

- The PC of the instruction that was executing when the error occurred is stored in PCP_ES.EPC.
- The number of the channel program that was executing when the error occurred is stored in PCP_ES.EPN.
- The error type is set in the appropriate field of register PCP_ES.
- The context is saved back to the PRAM CSA. Depending on the chosen context size (PCP_ES.CS) a Full, Small, or Minimum Context save is performed.
- If the error condition was not due to an FPI Bus error or a DEBUG instruction, then an interrupt request to the CPU is generated with the priority number stored in register PCP_CS.ESR.

The repetitive posting of PCP error interrupts will not cause an overwhelming number of interrupts to the CPU. In this situation, the PCP's CPU service request queue (see **Page 11-35**) will quickly fill, and force the PCP to stall until the CPU can resolve the situation.

Note: An error condition (other than an FPI Bus error) will result in an interrupt being sent to the CPU. The interrupt routine that responds to this interrupt must be capable of dealing with the cause as recorded in PCP_ES, and it must be able to restore the channel program to operation. The minimum required to restart the channel program is to set the context value of CR7.CEN = 1.

11.5.3.3 Debug Exit

If the DEBUG instruction is programmed to stop the channel program execution (SDB = 1 has been specified), the PCP performs an exit sequence that is very similar to the error exit sequence, with the exception that no interrupt request to the CPU is generated. This sequence is:

- If RTA = 0, then the channel enable bit R7.CEN is cleared. This means the channel program will be unable to restart until another FPI Bus master has re-configured the channel program's stored context to set CR7.CEN to 1 again. Otherwise, the R7.CEN bit remains unchanged, and the PC is decremented (such that it points to the DEBUG instruction)
- If EDA = 1, a break-point event is generated
- If DAC = 1, then the PCP_CS.EN bit is cleared. This means that the PCP will not execute any further channel programs until the PCP_CS.EN bit is set by another FPI Bus master
- The address of the DEBUG instruction (i.e. the current PC) is stored in register PCP_ES.PC
- The current channel number is stored in register PCP_ES.PN

The execution of the current channel program is stopped at the point of the DEBUG instruction. This instruction only disables the current channel; the PCP will continue to operate, accepting service requests for other channels as they arise.

Note: The DEBUG instruction must be only used in DEBUG mode; otherwise an "Illegal Operation" (IOP) error will be generated.

11.6 PCP Interrupt Operation

The PICU and the PSRNs (PCP_SRC[11:0]) are similar to the CPU's ICU and all other SRNs in the system. They do, however, have some special characteristics, which are described in the following sections. **Figure 11-11** shows an overview of the PCP interrupt scheme.

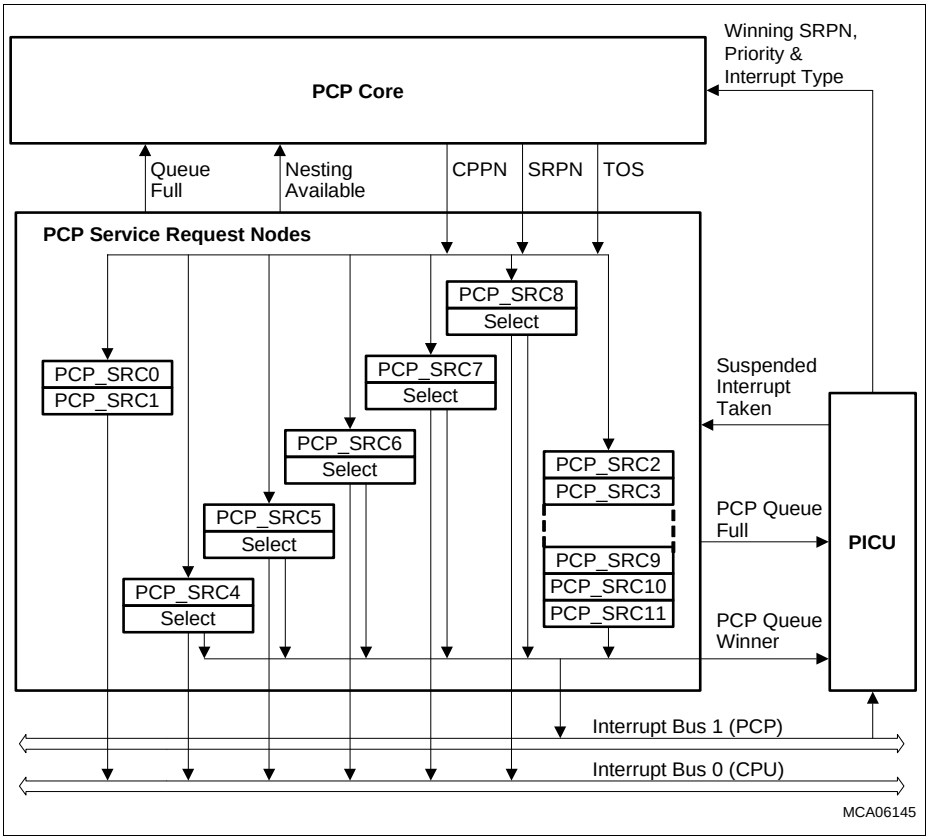


Figure 11-11 PCP Interrupt Block Diagram

11.6.1 Issuing Service Requests to CPU or PCP

The PCP may use one of two mechanisms to raise an interrupt request to the CPU or itself. The first, and most inefficient, method for a PCP channel program is to issue service requests by performing an FPI Bus write operation to an external service request node (SRN). Alternately, the PCP can raise a service request using one of its own internal SRNs. An interrupt can only be generated by the PCP via an internal SRN when executing an EXIT instruction, or when an error condition occurs. In the following descriptions, PCP service requests triggered through an EXIT instruction or the occurrence of an error are called “implicit” PCP service requests to distinguish them from the “explicit” way of generating a service request through an FPI Bus write to a service request node external to the PCP.

11.6.2 PCP Interrupt Control Unit

The PICU operates in a similar manner to the ICU of the CPU. The PICU manages the PCP service request arbitration bus, and handles the communication of service requests and priority numbers to and from the PCP kernel. The PCP_ICR register is provided to control and monitor the arbitration process.

When one or more service requests to the PCP are activated, the PICU performs an arbitration round to determine the request with the highest priority. It then places the priority number of this “winning” service request into the PIPN field of register PCP_ICR, and generates a service request to the PCP kernel.

If the PCP kernel is currently busy processing a channel program, the new request is left pending until the current channel program has finished.

When the PCP kernel is ready to accept a new service request, it calculates the context start address from the Pending Interrupt Priority Number, PIPN, stored in register ICR, and begins with the context restore. It notifies the PICU of the acceptance of this request, and in turn the PICU acknowledges the winner of the last arbitration round. This service request node then resets its Service Request Flag, SRR.

There is one special condition in which the PICU operates differently from the way that the CPU Interrupt Control Unit operates. This special operation is described on **Page 11-38**.

The PCP interrupt arbitration can be adapted to the application’s needs and characteristics through controls in register PCP_ICR. Bit field PCP_ICR.PARBCYC controls the number of arbitration cycles per arbitration round (one through four cycles), while bit PCP_ICR.PONECYC controls whether one arbitration cycle equals one or two system (FPI Bus) clock cycles.

11.6.3 PCP Service Request Nodes

The PCP contains twelve service request nodes, including twelve service request control registers, PCP_SRC0 to PCP_SRC11, which are provided for implicit PCP service

requests. The service request control registers differ from standard SRC registers in that they are fully controlled by the PCP kernel; they are read-only registers during PCP operation. The user cannot generate interrupts by writing to them.

The twelve service request nodes are split into four groups.

- The first group, containing registers PCP_SRC0 and PCP_SRC1, handles implicit PCP service requests targeted to the CPU. The Type-of-Service control fields, TOS, of these registers are hard-wired to 00_B, directing the requests to the CPU.
- The second group, registers PCP_SRC2 and PCP_SRC3, handles the service requests targeted to the PCP itself. The respective TOS field of these registers are hard-wired to 01_B, directing the requests to the PCP.
- The third group, containing registers PCP_SRC4 to PCP_SRC8, have programmable TOS fields which allow these registers to be assigned (at configuration time) to any of the available interrupt buses.
- The fourth group, containing registers PCP_SRC9, PCP_SRC10 and PCP_SRC11, are an extended version of a standard Service Request Node. These handle service requests targeted to the PCP itself, including service requests representing a suspended interrupt. The respective TOS field of these registers are hard-wired to 01_B, directing the requests to the PCP.

The service request enable bits, SRE, of the PCP_SRCx registers are hard-wired to 1, meaning these service requests are always enabled.

Note: The number of interrupt buses is device-dependent. Programming a PCP_SRCx register (x = 4 to 8) with a TOS value representing a non-available interrupt bus (10_B or 11_B in the TC1798) will disable Service Request Node x.

The actual service request flag and the service request priority number of the PCP_SRCx registers are updated by the PCP when it generates an implicit service request. The way this is performed is described in the following section.

The service request nodes in each of the groups described above are implemented as queues with the appropriate number of entries. When the PCP generates an implicit service request, it places the request into the next available free entry of the appropriate queue rather than writing it into a specific register. Queue management logic automatically ensures proper handling of the queue. If all entries of a queue are filled with pending service requests, the queue management reports this condition to the PCP kernel via a “queue full” signal.

In the following descriptions, the terms “CPU Queue” and “PCP Queue” are used to refer to the queues in the two groups of PCP service request nodes.

11.6.4 Issuing PCP Service Requests

The PCP can issue implicit service requests on the execution of an EXIT instruction, when suspending a channel, or when an error occurs during a channel program execution. While the service request generation for the EXIT instruction is optional, a

service request is always generated when a channel is suspended or an error occurs. Further differences between these three mechanisms are detailed in the following sections.

11.6.4.1 Service Request on EXIT Instruction

An implicit PCP service request is issued when the INT field of the EXIT instruction is set to 1 and the specified condition code, cc_B, of this instruction is true. Such a service request can be issued to any of the available interrupt buses, depending on the programmed value in the TOS field of register R6. The PCP examines the TOS field in register R6 and issues a service request to the appropriate queue of the service request nodes. Along with this request, it passes the service request priority number stored in the SRPN field of register R6 to the queue. If the queue has a free entry left, the service request flag, SRR, of the associated service request register, PCP_SRCx, will be set, and the service request priority number will be written to the SRPN field of the SRC register. Please see **Page 11-38** for the case where there is no free entry in the queue.

Because the desired service request is programmed through the TOS and SRPN fields in register R6, each channel program can issue its individual service request. Note that this register needs to be programmed properly if a service request is to be generated by the EXIT instruction.

11.6.4.2 Service Request on Suspension of Interrupt

An implicit PCP service request is issued when the PCP suspends execution of the ongoing channel program in favor of a service request with a higher priority. Such a service request is always issued to the PCP's own interrupt bus and is stored in one of the three extended Service Request Nodes (PCP_SCR9, PCP_SRC10, PCP_SRC11). Along with this request, it passes the current channel operating priority (CPPN) as an SRPN and also the channel number (the original SRPN). The service request flag, SRR, and the Restart Request flag, RRQ, of the associated service request register, PCP_SRCx, will be set, the Operating Priority will be written to the SRPN field, and the channel number will be written to the SRNC field of the SRC register.

Use of the Operating Priority as the SRPN for resumption of the channel program ensures that during subsequent arbitration rounds the PCP will resume execution of the suspended channel program at the appropriate time.

The PCP treats an interrupt request with the RRQ bit set in a special fashion. In this case the PCP clears the interrupt request bit in the appropriate internal Service Request Node but does not issue an interrupt acknowledge to any external nodes. This prevents the unwanted clearing of external service requests with an SRPN that matches the priority of a suspended channel.

Note: The PCP will only suspend channel operation when there are two or more free SRNs with the appropriate TOS value for the PCP, and one of the free SRNs is an

Extended Service Request Node. This allows for the posting of an interrupt request to the PCP on exit from the new channel program.

11.6.4.3 Service Request on Error

While a service request triggered through an EXIT instruction is optional and can be issued either to the CPU or to the PCP itself, a service request due to an error condition will always be automatically issued and will always be directed to the CPU. The PCP issues a service request to the CPU queue of the service request nodes. Along with this request, it passes the SRPN stored in the ESR field of register PCP_CS to the queue. If the queue has a free entry left, the SRR flag of the associated service request register, PCP_SRCx, will be set, and the SRPN will be written to the SRPN field of the SRC register. See next section for the case where there is no free entry in the queue (queue full).

Due to the fact that the priority number is stored in the global control register PCP_CS, all channel programs share the same service request routine in case of an error. The exact cause of the error and the channel number of the program that was executed when the error occurred can be determined through examination of the contents of the Error/Debug Status Register, PCP_ES.

11.6.4.4 Queue Full Operation

Queuing the implicit service requests typically allows the PCP to continue with the next service request without stalling. The depth of the queue and the number of channel programs using them determines the stall rate. Depending on the selected service provider (via R6.TOS in case of an EXIT interrupt or always to the CPU in case of an error interrupt), the request is routed to a free entry in the appropriate queue.

If no free entries are available in a queue at the time the PCP wants to post a request to that queue, the PCP is forced to stall until an entry becomes clear. This ensures that the PCP does not lose any interrupts. An entry in a queue becomes free when its SRR flag, is cleared through an acknowledge from the PICU (that is, the CPU or PCP, as appropriate, has started to service this request).

One special case needs to be resolved for the PCP-related queue through special operation of the PICU. Consider the case in which the PCP queue is full, meaning registers PCP_SRC2, PCP_SRC3 and PCP_SRC9 to PCP_SRC11 are already loaded with pending service requests to the PCP. If the PCP kernel now needed to post an additional service request into that queue, a deadlock situation would be generated: The PCP would stall, since there is not a free entry in the PCP queue in which to place the request. In turn, as the PCP is stalled, it cannot accept new service requests and so the PCP service request queue cannot be emptied. This would result in a deadlock of the PCP.

To avoid such a deadlock, the PICU performs a special arbitration round as soon as the PCP queue becomes full. In this arbitration round, only the service request nodes assigned to the PCP queue are allowed to participate; all service requests from nodes external to the PCP are excluded, regardless of whether their priorities are higher or lower than those of the PCP queue. In this way, it is guaranteed that one entry in the PCP queue gets serviced, freeing one slot in the queue.

The PCP programmer needs to carefully consider this special operation. It ensures that deadlocks are avoided, but it implies that if too many PCP channel programs post service requests to the PCP (self-interrupt), the PCP will have to service these rather than outside interrupt sources. Depending on the priority given to these requests, this could undermine an otherwise appropriate use of the interrupt priority scheme. It is recommended that the system be designed such that in most cases, high-priority numbers can be assigned to these self-interrupts, so that they can win normal arbitration rounds, avoiding the situation where the PCP queue becomes full.

Note: If the CPU queue is full, the PCP can continue to operate until it needs to post another service request to the CPU queue.

11.7 PRAM Protection

To allow the PCP to handle system critical tasks it is necessary to ensure that the PCP can operate properly regardless of a failure in another part of the system or the PCP itself. this means that it is necessary to protect all or part of the content of the PRAM from such failures.

By default, after reset, the PRAM can be considered to be a single memory space writeable both by FPI Masters and by instructions executed by the PCP itself. However the PCP contains a programmable protection scheme allowing the definition of up to four memory regions with different protection from FPI PRAM writes and internally generated PRAM writes. This is illustrated in **Figure 11-12** below:-

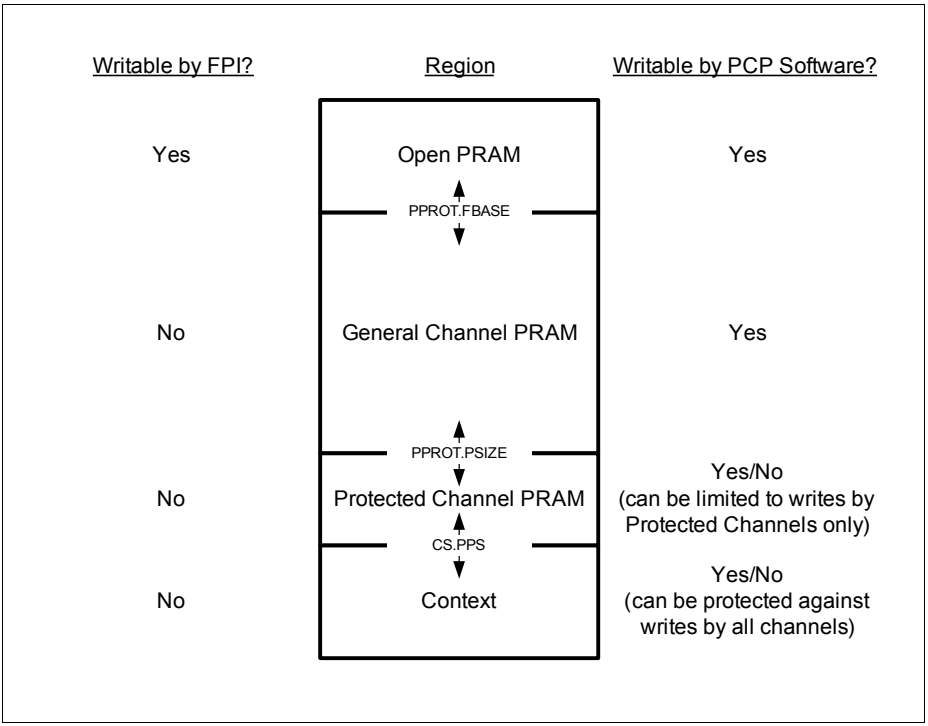


Figure 11-12 PRAM Regions

*Note: **Figure 11-12** shows a typical configuration that might be used. Configuration is sufficiently flexible, however, that all of, none of, or any combination of the above regions can be implemented and that the region boundaries can be set with a granularity of at least 256 bytes.*

While **Figure 11-12** shows four regions, in reality the protection scheme can be seen from two viewpoints:-

- Protection from FPI writes (see **Section 11.7.1**).
- Protection from internally generated PRAM writes (see **Section 11.7.2**).

Protection of PRAM is provided to allow running of system critical tasks on the PCP. Protection means that such tasks can be made immune from failures outside of the PCP or indeed from software failures in non-critical tasks running on the PCP itself.

PRAM protection is based around the concept of “Protected” and “Unprotected” Channel Programs. A “Protected” channel program is one that is running a critical system task and is termed “Protected” since it (and any other Protected Channel Programs) have

write access to an area of PRAM that cannot be modified by an Unprotected Channel Program.

Determination of whether a channel is Protected or Unprotected is performed by examination of the channel number against a programmable threshold (programmed via PCP_PPROT.PTHRES). In addition to the threshold the user can select (via PCP_PPROT.PCAT) whether Channel Programs above (and including the threshold) are Protected or whether Channel Programs below (and including the threshold) are Protected.

11.7.1 Protection of PRAM against FPI Writes

The PRAM FPI protection function is provided so that once the PRAM has been loaded (typically at system initialization) the PRAM can be partially or totally protected against FPI write accesses. This function is controlled by the PCP_PPROT register (**“PRAM Protection Register, PCP_PPROT” on Page 11-87**).

When the protection function is enabled (via PCP_PPROT.EN) any incoming FPI write access outside a defined PRAM address range (defined by PCP_PPROT.FBASE) is issued with an error response and the PRAM content remains unmodified.

The address range can be select such that an “Open Window” of PRAM (based at the top of PRAM) remains available for incoming FPI write accesses. The “Open Window” is provided as PRAM is often used for implementation of a “mail-box” to allow communication between the PCP and other on-chip cores.

Regardless of the enabling of write protection the entire PRAM content remains readable via FPI.

Note: The PCP internal PRAM write instructions (i.e. instructions that modify the PRAM content) are unaffected by this protection.

11.7.2 Protection of PRAM against Internally Generated PRAM Writes

Protection of PRAM against internal writes is performed via two regions:-

- Context Save Region
- Protected Channel PRAM

11.7.2.1 Context Save Region Protection

The Context Save Region can be protected by the PRAM Partitioning Scheme (see **“PCP Control and Status Register, PCP_CS” on Page 11-69**). This protection is enabled via PCP_CS.PPE and the size of the context area being protected is defined by PCP_CS.PPS. When enabled the context region is protected from writes by any Channel Program (i.e. regardless of whether Protected or Unprotected).

Note: This scheme also limits the number of Channel Programs that can be invoked.

Note: FPI PRAM write accesses to PRAM are unaffected by this protection.

11.7.2.2 Protected Channel PRAM Protection

To ensure that an Unprotected Channel Program cannot corrupt the PRAM assigned to a protected channel program it is necessary to protect the PRAM space used by the protected channels from instruction executed by non-protected channels. The PCP provides a protection scheme which prevents corruption of a programmable range of locations at the base of PRAM by writes generated by a non-protected channel. This region is termed the “Protected Channel PRAM”. Protection is enabled via PPROT.ENI and the size of the protected region is controlled by PPROT.PSIZE. This function is controlled by the PCP_PPROT register (**“PRAM Protection Register, PCP_PPROT” on Page 11-87**).

Whenever a Unprotected Channel Program executes a PRAM write instruction (and protection is enabled) the target address will be examined to determine whether it lies within the Protected Channel PRAM region. If the address lies within the region then the PRAM write will not take place and the PCP will exit the channel with an IOP (Illegal Operation) error.

Note: FPI PRAM write accesses to PRAM are unaffected by this protection.

11.8 FPI Interface

The PCP operates both as an FPI Master and an FPI Slave.

11.8.1 Operation as an FPI Master

The PCP generates FPI read and write transactions in response to execution of PCP FPI instructions. The PCP can generate Byte, Half-word and Word single transactions and bursts of length two, four and eight. All FPI transactions are generated in Supervisor Mode.

For High Integrity Systems it is necessary to prevent the PCP from generating unwanted FPI writes to critical locations in the event of a PCP malfunction. To address this problem a Memory Protection feature is provided to control the address range that can be written to by the PCP. The scheme is based around a user definable FPI address window. Along with defining the window base address and size the user can select whether:-

- Writes are allowed only to addresses that are within the window (Limit).
- Writes are allowed only to addresses that are outside the window (Exclude).

Whenever the PCP executes an FPI instruction that will result in an FPI write accesses the destination address is checked to ensure that it is to an allowed address. If a write access is to an address that is not allowed then the write will not take place and the PCP will exit the channel with an IOP (Illegal Operation) error.

This function is controlled by the **PCP_FWWIN** register (see **Page 11-91**).

11.8.2 Operation as an FPI Slave

The PCP is visible to FPI Masters as a 256 Kbyte R/W block of memory on the System Bus. The PCP must be accessed only with word (32 bit) accesses. Accessing an unassigned address (i.e. an address outside the range of Control & Status Registers, PRAM and CMEM) will generate an FPI bus error. All PCP locations can be read in either User or Supervisor Modes. All writes must be performed in Supervisor Mode. Attempting to write to any PCP location in User Mode will generate an FPI error. Some Control and Status Registers are ENDINIT protected.

There are some additional user selectable FPI write protection options to support High Integrity operation:-

- Some/all Control and Status registers can be programmed to be ENDINIT protected.
- CMEM can be programmed to be read only.
- PRAM can be programmed to be partially or wholly read-only.

11.9 PCP Error Handling

The PCP contains a number of fail-safe mechanisms to ensure that error conditions are handled gracefully and predictably. In addition to providing an extra level of system robustness suitable for high integrity and safety-critical systems, these mechanisms can often ease the task of finding programming errors during the development process. Whenever an error is detected, the channel program that was executing exits and the PCP_ES register is updated with information to allow determination of the error that occurred, the instruction address, and the channel program that was executing when the error occurred (see **Page 11-32**).

11.9.1 PRAM Protection Violation

PRAM can be considered as being split into a number of distinct areas (see **Section 11.7**).

The default configuration of the PCP allows the PCP to use PRAM as a single area. While this default configuration allows complete flexibility regarding the use of PRAM, this flexibility also introduces the possibility of invalid PCP operation as a result of the following issues:

- Any channel program is allowed to write to any PRAM location (including any location in the CSA). This means that a channel program may be inadvertently programmed to corrupt the context save region or PRAM storage belonging to another channel, causing invalid operation of the corrupted channel when it next executes.
- Generation of an interrupt request to the PCP with a priority number that would cause loading of a context from outside the CSA will cause the spurious execution of a channel program with an invalid context loaded from outside the CSA.

11.9.1.1 Enforced PRAM Partitioning

The lowest of the PRAM areas is the CSA (see **Page 11-16**) which is used for storing context information for each active channel while the channel program is not actually executing.

To avoid spurious PCP operation as a result of programming errors, the PCP can be optionally configured via the global PCP control and status register (PCP_CS) to enforce strict partitioning of PRAM between the CSA and the remainder of PRAM. PRAM partitioning is selected by programming PCP_CS.PPE = 1 and the size of the CSA in use is selected via the PCP_CS.PPS bit field (see **Page 11-69**). When PRAM partitioning has been enabled, a PCP Error will be generated on either one of the following events:

- A channel program executes a PRAM write instruction with a target area within the CSA. This prevents a channel from corrupting the context save region of any other channel.

- An incoming interrupt request causes the PCP to attempt to load a context from outside the CSA. This prevents the PCP from running an invalid channel program as a result of an invalid interrupt request.

Note: Enabling PRAM partitioning (PCP_CS.PPE = 1) with a CSA size of zero (PCP_CS.PPS = 0) is an invalid setting and will cause a PCP error event whenever any interrupt request is received by the PCP.

11.9.1.2 Protected Channel PRAM

When a Protected Channel PRAM area has been programmed (see **Section 11.7.2.2**) then any attempt by an Unprotected Channel Program to write to the Protected Channel PRAM area will generate a PCP error.

11.9.2 FPI Write Window Violation

When an FPI Write Window has been programmed (see **Section 11.8.1**) then any attempt by a Channel Program to write to an FPI address that has been disallowed will generate a PCP error.

11.9.3 Channel Watchdog

The Channel Watchdog is a PCP internal watchdog that optionally allows the user to ensure that the PCP will not become locked into executing a single channel due to an endless loop or unexpected software sequence. As each channel executes, the PCP maintains an internal count of the number of instructions that have been read from CMEM since the channel started. If the watchdog function is enabled (by programming PCP_CS.CWE = 1) and the internal instruction fetch counter reaches the threshold programmed by the user (programmed via PCP_CS.CWT), a PCP Error is generated. The threshold setting (PCP_CS.CWT) is global to all channels. From this it follows that the threshold must be selected to be greater than the maximum number of instructions that can be fetched by any channel program, taking all channels into consideration. It should be noted that the instruction width of the PCP is 16 bits and that therefore execution of an instruction that is encoded into 32 bits (e.g. LDL.IL) will generate two CMEM instruction reads. That will therefore cause the internal watchdog counter to be incremented twice.

Note: Enabling the Channel Watchdog function (PCP_CS.CWE = 1) with a threshold of zero (PCP_CS.CWT = 0) is an invalid setting and will cause a PCP error event whenever any interrupt request is received by the PCP.

11.9.4 Invalid Opcode

The PCP includes the Invalid Opcode mechanism to check that each instruction fetched from CMEM is a legal instruction. If the PCP attempts to execute an illegal instruction, then a PCP error is generated.

Note: The DEBUG instruction must be only used in DEBUG mode otherwise it will be considered to be an illegal operation and will generate an IOP error.

11.9.5 Instruction Address Error

An Instruction Address Error is generated if the PCP attempts to execute an instruction from an illegal address. An address is considered to be illegal if:

- The address is outside the available CMEM area (see **Page 11-157** for the CMEM size implemented in this derivative)

and/or

- The specified address could not be contained in the 16-bit PC (i.e. an address calculation yielded a 16-bit unsigned overflow).

The second of these cases can result from an address calculation either from the execution of a PC relative jump instruction (either a JC, JC.I, or JL instruction), or the PC being incremented following execution of the previous instruction.

11.10 Software In-System Test Support

The PCP protects against memory integrity errors by ECC protection of the PCP memories. This has the unfortunate side-effect of requiring memory blocks wider than the normal data access path to the memory. The additional ECC storage bits are not easily accessible via the existing data paths, causing significant problems where SIST based testing of the memories is required. In order to address this problem the PCP includes improved SIST support, allowing all PCP memory arrays to be accessedto allow the test and debug of the fault tolerant memory systems.

The mapping of hidden memory ECC bits into the PCP address space is controlled by the setting of bits within the SIST Mode Access Control Register (SMACON). The existence of the SMACON register is architecturally defined. However, the fields within SMACON and the effect of the fields on the memory map of the PCP are implementation specific.

Hidden ECC bits are mapped into the CMEM and PRAM areas by setting bits in the SMACON register. The SMACON register is a SFR which can only be written in supervisor mode and is endinit protected. The definition of the SMACON register for the PCP is shown on **Page 11-81**.

The control fields within the SMACON register allow individual control of the local memories. Each memory may be mapped to operate in a number of different modes.

Normal Operation, No Mapping, error detection/correction enabled

No mapping of the ECC bits is performed and normal operation is possible. Error detection/correction is active.

Data Array Mapping, no error detection/correction

No mapping of the ECC bits is performed. Writes to the memory will not affect the ECC bits. Error correction/detection for the memory is disabled. Normal operation (with the exception that ECC protection is not operational) is possible.

Check Array Mapping, no error detection/correction

The ECC bit array (only) of the memory is made visible in the address map (i.e. the memory data array cannot be accessed). Writes to the memory will not affect the data bits. Error correction/detection for the memory is disabled. The PCP must be disabled before, and remain disabled while, this mode is selected for any of the PCP memories.

When this mode is selected the memory ECC bit array replaces the memory data array in the address map. During a read the value of the ECC bits for a location can be determined from bits 6 to 0 of the value read from the location (all other bits read as '0'). During a write the ECC bits are updated from bits 6 to 0 of the written value. The written value of all bits other than bits 6 to 0 is discarded.

Data Array Mapping, error detection/correction enabled.

No mapping of the ECC bits is performed and normal operation is possible.

Note: Unlike TriCore the PCP has no hidden memory arrays (i.e. all PCP memories reside permanently in the system address map). As a result, for the PCP, this mode is identical to "Normal Operation". This mode is retained for compatibility with TriCore SIST.

11.11 Memory Integrity Error Detection and Correction

The PCP includes support for Memory Integrity Error Detection and Correction logic to address the increasing occurrence of memory errors in deep sub-micron CMOS technologies. Soft errors are transient errors in state (not permanent) typically caused by alpha particle hits to the die, causing induced charge which flips the state of storage elements. In current process geometries SRAM arrays are most susceptible to soft error events due to their small size and low stored charge. The detection and deterministic recovery from such memory integrity errors is especially important for automotive applications, such as electronic braking systems and engine management.

The PCP includes the following SRAM arrays:

- Code Memory (CMEM)
- Parameter Memory (PRAM)

Each of these memory arrays will be protected from memory integrity errors, with the specific mechanisms described in the following sections.

Note: Before enabling Error Detection/Correction on an SRAM (i.e. CMEM or PRAM) the user must ensure that all locations within the SRAM have been initialised. If this is not done then unwanted spurious memory errors can be generated.

11.11.1 Definitions

In the following sections memory integrity errors are considered to be either Correctable or Un-correctable. These are defined as follows:-

Un-correctable Memory Integrity Error

If on accessing a memory element containing a memory integrity error hardware is not able to provide the expected data to the core, the integrity error is defined as being Un-correctable.

Correctable Memory Integrity Error

If on accessing a memory element containing a memory integrity error hardware is able to provide the expected data to the core, the integrity error is defined as being correctable.

11.11.2 Architectural Extensions - Registers

A number of additional Special Function Registers (SFRs) have been added to the PCP in order to fully support memory integrity error handling. The function of these registers is explained below while the specific register information is detailed in **Section 11.15**.

11.11.3 Memory Integrity Error Control

The MIECON register controls whether memory errors generate a notification to the SCU or not. MIECON may only be written in supervisor mode and is ENDINIT protected.

Two status registers (MIESTATP for PRAM and MIESTATC for CMEM) are provided to allow software to easily identify locations that have generated memory error events. The xxIEE bits and the appropriate SMACON field settings interact to control the update of these registers.

Errors are reported and the MIESTATx registers are updated only when data read from the memory is actually being utilized (i.e. the memory is either being read via FPI or by the core). In the event of error detection being enabled, a PRAM (double word) location containing an error in both word lanes and the PCP performing a double word read (only during a context restore) the MIESTATP register will be updated as though the error was in the lower word of PRAM.

11.12 Instruction Set Overview

The following sections present an overview of the instruction set and the available addressing modes of the PCP in the TC1798.

11.12.1 DMA Primitives

Table 11-3 describes the two DMA instructions of the PCP.

Table 11-4 DMA Transfer Instructions

DMA Transfer	BCOPY	Move block of data value from FPI Bus source address location to FPI Bus destination address location. Optionally increment or decrement source and destination pointer registers. Optionally repeat instruction until counter CNT1 reaches 0.
	COPY	Move value from FPI Bus source address location to FPI Bus destination address location. Optionally increment or decrement source and destination pointer registers. Optionally repeat instruction until counter CNT1 reaches 0.

11.12.2 Load and Store

Table 11-4 describes the load and store instructions of the PCP.

Note: If a conditional instruction's condition code is false, the operation will be treated as a "No Operation". Register values will not be changed and the flags will not be updated.

Table 11-5 Load and Store Instructions

Load	LD.F	Load value from FPI Bus address location into register (FPI Bus address = register content)
	LD.I	Load immediate value into register
	LD.IF	Load value from FPI Bus address location into register (FPI Bus address = register content + immediate offset)
	LD.P	Load value from PRAM address location into register (PRAM address = DPTR + register offset)
	LD.PI	Load value from PRAM address location into register (PRAM address = DPTR + immediate offset)
	LDL.IL	Load 16-bit immediate value into lower bits [15:0] of register
	LDL.IU	Load 16-bit immediate value into upper bits [31:16] of register
Store	ST.F	Store register value to FPI Bus address location (FPI Bus address = register content)
	ST.IF	Store register value to FPI Bus address location (FPI Bus address = register content + immediate offset)
	ST.P	Store register value to PRAM address location (PRAM address = DPTR + register offset)
	ST.PI	Store register value to PRAM address location (PRAM address = DPTR + immediate offset)
Move	MOV	Conditionally move register value to register

11.12.3 Arithmetic and Logical Instructions

Arithmetic instructions that are fully register-based execute conditionally depending on the specified Condition Code A (see Page 11-99). All other arithmetic instructions such as PRAM (.PI), indirect (.I), and FPI (.F and .IF) execute unconditionally.

Note: If a conditional instruction's condition code is false, the operation will be treated as a "No Operation". Register values will not be changed and the flags will not be updated.

Table 11-6 Arithmetic Instructions

Add	ADD	Add register to register (conditionally)
	ADD.I	Add immediate value to register
	ADD.F	Add content of FPI Bus address location to register (byte, half-word or word)
	ADD.PI	Add content of PRAM address location to register
Subtract	SUB	Subtract register from register (conditionally)
	SUB.I	Subtract immediate value from register
	SUB.F	Subtract content of FPI Bus address location from register (byte, half-word or word)
	SUB.PI	Subtract content of PRAM address location from register
Compare	COMP	Compare register to register (conditionally)
	COMP.I	Compare immediate value to register
	COMP.F	Compare content of FPI Bus address location to register (byte, half-word or word)
	COMP.PI	Compare content of PRAM address location to register
Negate	NEG	Negate register (2's complement, conditionally)

Logical instructions that are fully register-based execute conditionally as determined by the specified Condition Code A. All other logical instructions, such as PRAM (.PI), indirect (.I), and FPI (.F and .IF) execute unconditionally.

Table 11-7 Logical Instructions

Logical And	AND	Register AND register (conditionally)
	AND.F	Content of FPI Bus address location AND register (byte, half-word or word)
	AND.PI	Content of PRAM address location AND register
	MCLR.PI	Clear specified bits within a PRAM location

Table 11-7 Logical Instructions (cont'd)

Logical Or	OR	Register OR register (conditionally)
	OR.F	Content of FPI Bus address location OR register (byte, half-word or word)
	OR.PI	Content of PRAM address location OR register
	MSET.PI	Set specified bits within a PRAM location
Logical Exclusive-Or	XOR	Register XOR register (conditionally)
	XOR.F	Content of FPI Bus address location XOR register (byte, half-word or word)
	XOR.PI	Content of PRAM address location XOR register
Logical Not	NOT	Invert register (1's complement, conditionally)
Shift	SHL	Shift left register
	SHR	Shift right register
Rotate	RL	Rotate left register
	RR	Rotate right register
Prioritize	PRI	Calculate position of first set bit (1-bit) in register, from left

Note: If a conditional instruction's condition code is false, the operation will be treated as a "No Operation". Register values will not be changed and the flags will not be updated.

11.12.4 Bit Manipulation

All bit manipulation instructions except INB are executed unconditionally. If conditional bit handling is required, INB should be used.

Table 11-8 Bit Manipulation Instructions

Set Bit	SET	Set bit in register
	SET.F	Set bit in FPI Bus address location
Clear Bit	CLR	Clear bit in register
	CLR.F	Clear bit in FPI Bus address location
Insert Bit	INB	Insert carry flag into register (position given by content of a register)
	INB.I	Insert carry flag into register (position given by immediate value)
Check Bit	CHKB	Set carry flag depending on value of specified register bit

11.12.5 Flow Control

Table 11-8 describes flow control instructions of the PCP in the TC1798.

Table 11-9 Flow Control Instructions

Jump	JC	Jump conditionally to PC + short immediate offset address
	JC.A	Jump conditionally to immediate absolute address
	JC.I	Jump conditionally to PC + register offset address
	JC.IA	Jump conditionally to register absolute address
	JL	Jump unconditionally to PC + long immediate offset address
Exit Channel	EXIT	Unconditionally exit channel program execution (optionally generate interrupt request and/or inhibit channel)
No Operation	NOP	Low-power No-Operation
Debug	DEBUG	Conditionally generate debug event (optionally stop channel program execution)

11.12.6 Addressing Modes

The PCP needs to address locations in memory in different ways, as determined by the type of memory being accessed and the type of action being performed on that location.

11.12.6.1 FPI Bus Addressing

All FPI Bus accesses from the PCP are indirect to some extent. The main indirect addressing on the FPI Bus uses a 32-bit absolute address located in the GPR indicated in the instruction. This address must be properly aligned for the type of data access – byte, half-word or word. If it is not aligned, the results are undefined.

- Effective Target Address [31:0] = <R[a]>

where a is the number of the register, for instance, R2. Instructions using this address mode are indicated through the ".F" suffix.

For indirect-plus-immediate addressing on the FPI Bus, the 32-bit absolute address located in the GPR indicated in the instruction is added to the immediate 5-bit offset value encoded in the instruction. This address must be properly aligned for the type of data access (byte, half-word or word). If it is not aligned, the results are undefined.

- Effective Target Address [31:0] = <R[a]> + #offset5

where a is the number of the register and #offset5 is a 5-bit immediate offset value. Instructions using this addressing mode are indicated through the ".IF" suffix (only available for load and store, LD.IF and ST.IF).

This addressing mode is particularly useful for managing peripherals, where the peripheral base address is held in R[a], and the offset can index directly into a specific control register.

The BCOPY and COPY instructions use the indirect absolute addressing with predefined PCP registers. Register R4 is used as the source address pointer, while R5 represents the destination address pointer.

- Effective Source Address [31:0] = <R4>
- Effective Destination Address [31:0] = <R5>

Note: All FPI Bus accesses by the PCP are performed in Supervisor mode.

Note: The PCP is not allowed to access its own registers via instructions executed in the PCP.

11.12.6.2 PRAM Addressing

The PRAM is always addressed indirectly by the PCP. The normal address used is the value of the R7.DPTR field (8 bits) concatenated with an immediate 6-bit offset value encoded in the instruction, yielding a 14-bit word address. This enables access to 16 Kwords (64 Kbytes). Because R7.DPTR is part of a channel program's context, a channel program may alter the DPTR value at any time.

- Effective PRAM Address[13:0] = <R7.DPTR> << 6 + #offset6

Instructions using this addressing mode are indicated through the ".PI" suffix.

To provide effective indexing into large tables or stores of data, an alternate form of indirect addressing can also be used on load and store operations to PRAM. The value of the DPTR field (8 bits) is concatenated with the least significant 6 bits of R[a], again yielding a 14-bit word address. The most significant bits [31:6] of R[a] are ignored.

- Effective PRAM Address[13:0] = <R7.DPTR> << 6 + <R[a][5:0]>

Instructions using this addressing mode are indicated through the ".P" suffix (load and store only, LD.P and ST.P).

11.12.6.3 Bit Addressing

Single bits can be addressed in the PCP GPRs or in FPI Bus address locations. A 5-bit value indicates the location of a bit in the register specified in the instruction. This bit location is either given through an immediate value in the instruction or through the lower five bits of a second register (indirect addressing).

- Effective Bit Position[31:0] = #imm5
- Effective Bit Position[31:0] = <R[a][5:0]>

The immediate bit addressing is used by instructions SET and CLR and their variants as well as by INB.I and CHKB. Indirect bit addressing is used by the INB instruction only.

11.12.6.4 Flow Control Destination Addressing

The jump instructions are split into two groups: PC-relative jumps, and jumps to an absolute address.

For PC-relative jumps, the destination address is a positive or negative offset from the PC of the next instruction. The offset is either contained in the lower 16 bits of a register (the upper 16 bits are ignored), or is given as immediate value of the instruction. The immediate values are sign-extended to 16 bits. If the effective jump address is outside the available CMEM area (or the jump address calculation caused an overflow), then a PCP error condition has occurred.

- Effective JUMP Address[15:0] = NextPC + Signed(R[a][15:0]); +/- 32K instructions
- Effective JUMP Address[15:0] = NextPC + Sign-Extend(#offset10);
  +/- 512 instructions

- Effective JUMP Address[15:0] = NextPC + Sign-Extend(#offset6);
  +/- 32 instructions

The function NextPC indicates the instruction that would be fetched next by the program counter. Instructions using this addressing are JL, JC and JC.I.

For absolute addressing, the actual address in CMEM where program flow is to resume is either an immediate value #imm16 in the CMEM location immediately following the jump instruction, or it is contained in the lower 16 bits of a register. If the value is greater than the PC size implemented, an error condition has occurred.

- Effective JUMP Address[15:0] = #imm16
- Effective JUMP Address[15:0] = <R[a]>

Instructions using these addressing modes are JC.A (immediate absolute address) and JC.IA (indirect absolute address).

11.13 FPI Interface

Any FPI Bus master (on the TC1798's System Peripheral Bus) can access the three distinct PCP address ranges from the FPI Bus side, on the other hand the PCP master interface can also access any address on the FPI bus. Normally, the CPU initializes the control registers via FPI Bus access. Thereafter, the PCP should not access its control registers itself through PCP instructions. Apart from the access via FPI Bus, there is no direct way to the PCP control registers.

Accesses to the PCP control and status register, the PRAM, and the CMEM are detailed in the following sections.

11.13.1 Access to the PCP Control Registers from the FPI Bus

FPI Bus accesses to the PCP control registers must always be performed in Supervisor Mode with word accesses; byte or half-word accesses will result in a bus error.

All PCP control registers can be read at any time. Register PCP_CS can be optionally Endinit-protected via bit PCP_CS.EIE (see **Page 11-69**). If CS.EIE & ENDINIT = True, then any write access to this register is inhibited. The clock control register PCP_CLC is endinit-protected. The Software In-System Test register is also endinit-protected.

Additionally (see below) for High Integrity applications the entire Register content can be ENDINIT protected (see below).

11.13.1.1 PCP Control Register Protection

To allow the PCP to handle system critical tasks it is necessary to ensure that the PCP can operate properly regardless of a failure in another part of the system or the PCP itself. This means that it is necessary to protect the Control and Status Registers from such failures.

The configuration register content can only be modified via the FPI. Protection of the PCP configuration therefore consists of prevention of unwanted FPI writes to the PCP registers.

The normal model of PCP operation is that the PCP is configured at system initialization and the configuration remains unchanged for the duration of operation of the system. Protection therefore consists of a simple locking scheme to prevent any write to registers once the PCP has been configured. Once the PCP has been configured (at system initialization) the Registers can be locked such that, unless ENDINIT is clear, all incoming FPI write accesses are issued with an error response and the PCP configuration will remain unmodified.

If is required to modify content of the registers once they have been locked it is necessary to clear the ENDINIT bit (via the system Watchdog Timer) such that the Registers become writeable again.

Regardless of protection the entire Register content remains readable via FPI.

This function is controlled by the RPROT register (**“Register Protection Register, PCP_RPROT” on Page 11-85**).

11.13.2 Access to the PRAM from the FPI Bus

FPI Bus accesses to the PRAM must always be performed with word accesses; byte or half-word accesses will result in a bus error.

Attention needs to be paid when accessing the CSAs and data sections of the PCP channel programs. The location of a specific channel’s CSA is dependent on the chosen Context Model, Full, Small or Minimum Context. **Table 11-10** shows these addresses.

Table 11-10 FPI Bus Access to CSAs

Channel	Full Context	Small Context	Minimum Context
0 (see note)	PRAM Base Address + 00_H	PRAM Base Address + 00_H	PRAM Base Address + 00_H
1	PRAM Base Address + 20_H	PRAM Base Address + 10_H	PRAM Base Address + 08_H
2	PRAM Base Address + 40_H	PRAM Base Address + 20_H	PRAM Base Address + 10_H
3	PRAM Base Address + 60_H	PRAM Base Address + 30_H	PRAM Base Address + 18_H
n	PRAM Base Address + $n \times 20_H$	PRAM Base Address + $n \times 10_H$	PRAM Base Address + $n \times 08_H$

Note: Since channel 0 is not defined (no service request with SRPN = 0), the first area is not an actual CSA. It is recommended that this area should not be used by PCP channel programs.

The FPI Bus address of a word location pointed to by the Data Pointer R7_DPTR is calculated by the following formula:

- Effective FPI Bus address[31:0] = (PRAM Base Address) + (<DPTR> << 6)

11.13.3 Access to the CMEM from the FPI Bus

FPI Bus accesses to the CMEM must always be performed with word accesses; byte or half-word accesses will result in a bus error.

When using a channel entry table, the FPI Bus address of a specific channel’s entry location is given by the following formula:

- Effective FPI Bus address[31:0] = (CMEM Base Address) + $04_H \times$ channel number

The FPI Bus address of an instruction pointed to by the PCP program counter, PC, is calculated by the following formula:

- Effective FPI Bus address[31:0] = (CMEM Base Address) + <PC> << 1

11.14 Debugging the PCP

For debugging the PCP, a special instruction, DEBUG, is provided. This instruction can only be used when the PCP is in Debug Mode. It can be placed at important locations inside the code to track and trace program execution. The execution of the instruction depends on a condition code specified with the instruction. The actions programmed for this instruction will only take place if the specified condition is true.

The following actions are performed when the DEBUG instruction is executed and the condition code is true:

- Store the current PC, i.e. the address of the DEBUG instruction, in register PCP_ES.EPC
- Store the current channel number in register PCP_ES.EPN

In addition, the following operations can be programmed through fields in the DEBUG instruction:

- Optionally stop the channel program execution (instruction field SDB)
- Optionally generate an external debug event at pin $\overline{\text{BRKOUT}}$ (instruction field EDA)
- Optionally prevent the PCP from executing any further channel programs (instruction field DAC)
- Optionally cause the PCP to decrement the PC prior to saving the channel context (instruction field RTA)

If the DEBUG instruction is programmed to stop the channel program execution, the action taken by the PCP depends on the value of the RTA instruction field:

- If RTA = 0, the PCP disables further invocations of the current channel through clearing bit R7.CEN, and then performs a context save. The execution of this channel is stopped at the point of the DEBUG instruction. If the DAC instruction field = 0, the PCP will continue to operate, accepting service requests for other channels as they arise. Since the stopped channel was disabled before saving its context, service requests for this channel will result in an error exit (see **Page 11-32**). When re-enabling the channel, its enable bit CEN in the saved context location CR7 must be set.
- If RTA = 1, the PCP does not modify bit R7.CEN (i.e. the channel remains enabled), decrements the PC (so that it again points to the DEBUG instruction), and then performs a context save. The execution of this channel is stopped at the point of the DEBUG instruction. If the DAC instruction field = 0, the PCP will continue to operate, accepting service requests for channels as they arise. Since the stopped channel was not disabled before saving its context, service requests for this channel will not result in an error exit, but will simply cause re-execution of the DEBUG instruction and hence a repeat of the channel exit.

Note: When a channel is stopped by DEBUG, the context of the stopped channel will be saved to the appropriate region of the CSA before the channel terminates. Where a Small or Minimum Context model is being used, the values of the GPRs not

included in the context will not be saved, and indeed these register values may be changed by the operation of another active channel. In this case, the required registers should be explicitly saved to PRAM by store instructions prior to execution of the DEBUG instruction.

If the DEBUG instruction is programmed to stop all channel program execution, the PCP disables further invocations of any channel by clearing bit PCP_CS.EN. The execution of this channel is only stopped according to the SDB instruction field value. The PCP will only start to reaccept service requests when PCP_CS.EN is written to 1.

Note: The DEBUG instruction must be only used in DEBUG mode; otherwise it will generate an IOP error.

Note: If PCP_CS.RCB = 0 (Channel Resume Mode), then the channel program will begin executing at whichever PC is restored from the context location CR7.PC. If PCP_CS.RCB = 1 (Channel Restart Mode), then the channel program is forced to always start at its channel entry table location, no matter what the restored context value is for the PC. This means that in Channel Restart Mode, it is not possible to restart the channel program from where it was halted by the debug event. It is recommended that when using Channel Restart Mode, the user should also program all EXIT instructions with the "EP = 0" setting to allow selection of Channel Resume Mode for debugging without changing operation of the channel programs.

11.15 PCP Registers

The PCP can be viewed as being a peripheral on the FPI Bus. As with any other peripheral, there are control registers, normally set by the CPU acting as an external FPI Bus master to the PCP during initialization. Control registers select the operating modes of the PCP, and status registers provide information about the current state of the PCP to the external FPI Bus master.

Accessing of Control Registers

The control registers are accessible by any master via the FPI Bus. The control registers must be configured at initialization and then left unaltered. This is typically done by the CPU. The only setting that can be dynamically modified is the PCP_CS.EN bit. All other bits must only be modified when PCP_CS.EN = 0 and PCP_CS.RS = 0.

The PCP control and status registers are accessible only to the CPU when it is operating in Supervisor mode. PCP control and status registers must be accessed with 32-bit read and write operations only.

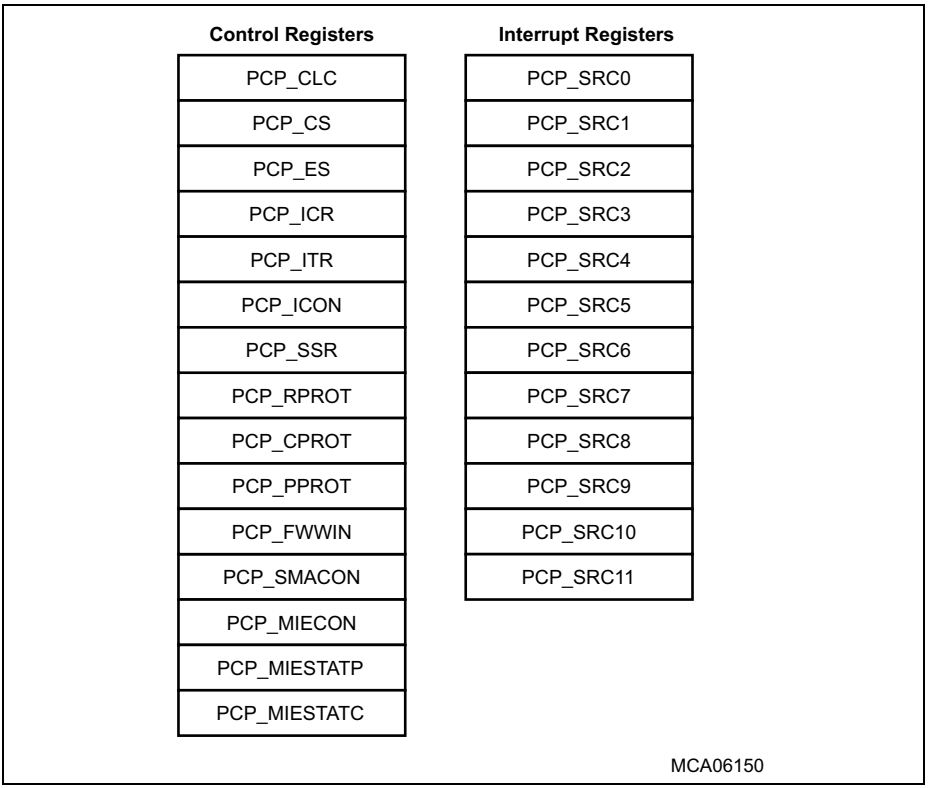


Figure 11-13 PCP Registers

PCP Register Overview

The address map of the PCP starts at its base address as shown in **Table 11-19**. The address offsets of the PCP registers are described in **Table 11-11**.

Table 11-11 Register Overview of PCP

Short Name	Description	Offset Addr.[1]	Access Mode		Reset	Description See
			Read	Write		
PCP_CLC	Clock Control Register	00_H	U, SV, 32	SV, 32, E	FPI Reset	**Page 11-67**
PCP_ID	Module Identification Register	08_H	U, SV, 32	SV, 32[2]	FPI Reset	**Page 11-68**

Table 11-11 Register Overview of PCP (cont'd)

Short Name	Description	Offset Addr.[1]	Access Mode		Reset	Description See
			Read	Write		
PCP_CS	Control/Status Register	10_H	U, SV, 32	SV, 32, E[3]	FPI Reset	Page 11-69
PCP_ES	Error/Debug Status Register	14_H	U, SV, 32	SV, 32[2]	FPI Reset	Page 11-71
PCP_ICR	Interrupt Control Register	20_H	U, SV, 32	SV, 32	FPI Reset	Page 11-74
PCP_ITR	Interrupt Threshold Control Register	24_H	U, SV, 32	SV, 32	FPI Reset	Page 11-76
PCP_ICON	Interrupt Configuration Register	28_H	U, SV, 32	SV, 32[2]	FPI Reset	Page 11-77
PCP_SSR	Stall Status Register	$2C_H$	U, SV, 32	SV, 32[2]	FPI Reset	Page 11-79
PCP_SMACON	SIST Mode Access Control Register	40_H	U, SV, 32	SV, 32	FPI Reset	Page 11-81
PCP_MIECON	Memory Integrity Error Control Register	50_H	U, SV, 32	SV, E, 32	FPI Reset	Page 11-82
PCP_MIESTATP	Memory Integrity Error Status for PRAM Register	58_H	U, SV, 32	SV, 32	FPI Reset	Page 11-83
PCP_MIESTATC	Memory Integrity Error Status for CMEM Register	$5C_H$	U, SV, 32	SV, 32	FPI Reset	Page 11-84
PCP_RPROT	Register Protection Register	70_H	U, SV, 32	SV, E, 32	FPI Reset	Page 11-85
PCP_CPROT	CMEM Protection Register	74_H	U, SV, 32	SV, E, 32	FPI Reset	Page 11-86
PCP_PPROT	PRAM Protection Register	78_H	U, SV, 32	SV, E, 32	FPI Reset	Page 11-87
PCP_FWWIN	FPI Write Window Register	$7C_H$	U, SV, 32	SV, E, 32	FPI Reset	Page 11-91

Table 11-11 Register Overview of PCP (cont'd)

Short Name	Description	Offset Addr.[1]	Access Mode		Reset	Description See
			Read	Write		
PCP_SRC11	Service Request Control Register 11	$D0_H$	U, SV, 32	SV, 32[2]	FPI Reset	Page 11-96
PCP_SRC10	Service Request Control Register 10	$D4_H$	U, SV, 32	SV, 32[2]	FPI Reset	Page 11-96
PCP_SRC9	Service Request Control Register 9	$D8_H$	U, SV, 32	SV, 32[2]	FPI Reset	Page 11-96
PCP_SRC8	Service Request Control Register 8	DC_H	U, SV, 32	SV, 32	FPI Reset	Page 11-95
PCP_SRC7	Service Request Control Register 7	$E0_H$	U, SV, 32	SV, 32	FPI Reset	Page 11-95
PCP_SRC6	Service Request Control Register 6	$E4_H$	U, SV, 32	SV, 32	FPI Reset	Page 11-95
PCP_SRC5	Service Request Control Register 5	$E8_H$	U, SV, 32	SV, 32	FPI Reset	Page 11-95
PCP_SRC4	Service Request Control Register 4	EC_H	U, SV, 32	SV, 32	FPI Reset	Page 11-95
PCP_SRC3	Service Request Control Register 3	$F0_H$	U, SV, 32	SV, 32[2]	FPI Reset	Page 11-94
PCP_SRC2	Service Request Control Register 2	$F4_H$	U, SV, 32	SV, 32[2]	FPI Reset	Page 11-94
PCP_SRC1	Service Request Control Register 1	$F8_H$	U, SV, 32	SV, 32[2]	FPI Reset	Page 11-92
PCP_SRC0	Service Request Control Register 0	FC_H	U, SV, 32	SV, 32[2]	FPI Reset	Page 11-92

1) The absolute register address is calculated as follows:
Module Base Address + Offset Address (shown in this column)

2) A write access is allowed to this register (i.e. no bus error is generated) but as there are no writable bits the register value is unaffected by the write.

3) Endinit protection is controlled by the EIE bit.

11.16 PCP Registers Address Space

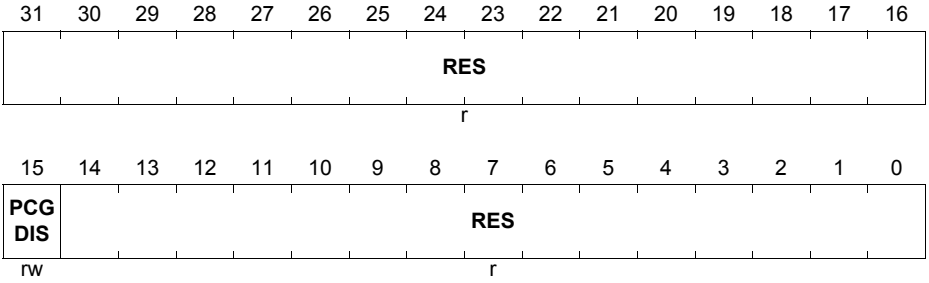
Table 11-12 Registers Address Space

Module	Base Address	End Address	Note
PCP	$F004\ 3F00_H$	$F004\ 3FFF_H$	

11.17 Registers

11.17.1 PCP Clock Control Register, PCP_CLC

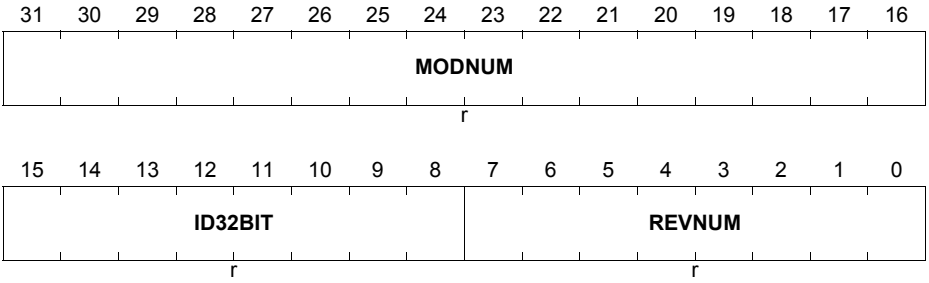
PCP_CLC
PCP Clock Control Register **(00_H)** **Reset Value: $0000\ 0000_H$**



Field	Bits	Type	Description
RES	[31:16]	r	**Reserved** Read as 0; should be written with 0.
PCGDIS	15	rw	**Clock Gating Disable Bit** Allows clock gating to be disabled. 0_B PCP Internal Clock stops when PCP is idle (default after reset) 1_B PCP Internal Clock always runs
RES	[14:0]	r	**Reserved** Read as 0; should be written with 0.

11.17.2 PCP Module Identification Register, PCP_ID

PCP_ID
PCP Module Identification Register (08_H) **Reset Value: 0020 C0XX$_H$**



Field	Bits	Type	Description
MODNUM	[31:16]	r	**PCP Identification Number** value = 0020_H
ID32BIT	[15:8]	r	**32-bit Module Identification Number Marker** value = $C0_H$
REVNUM	[7:0]	r	**PCP Revision Number** Implementation specific value = 08_H

11.17.3 PCP Control and Status Register, PCP_CS

This register can be Endinit-protected via bit EIE.

PCP_CS
PCP Control/Status Register **(10_H)** **Reset Value: 0000 0000$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ESR								CWT							CWE
rw								rw							rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PPS							PPE	CS		EIE	RCB	RES	RS	RES	EN
rw							rw	rw		rw	rw	r	rh	r	rw

Field	Bits	Type	Description
ESR	[31:24]	rw	**Error Service Request Number** SRPN for interrupt to CPU on an error condition. 00_H No interrupt request posted (default) 01_H Post an SRPN interrupt to CPU on an error condition 10_H Post an SRPN interrupt to CPU on an error condition
CWT	[23:17]	rw	**Channel Watchdog Threshold** 0_D Reserved 1_D Threshold = 16 instructions ...$_B$ ... 127_D From 1_D up to 127_D (n), the threshold = 16 × 'n' instructions
CWE	16	rw	**Channel Watchdog Enable** 0_B Disable Channel Watchdog 1_B Enable Channel Watchdog *Note: When enabled, the Channel Watchdog counts the number of instructions executed since the channel started. If this number exceeds the Channel Watchdog Threshold, a PCP error is generated.*

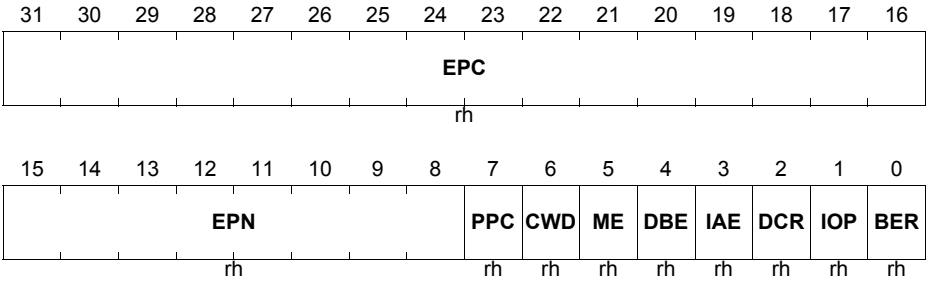
Field	Bits	Type	Description
PPS	[15:9]	rw	**PRAM Partition Size** 0_D Default, only allowed with PPE = 0 1_D CSA contains 3 context save regions $...B$ ... 127_D CSA contains 1 + 2 × 127 context save regions *Note: The actual size of the CSA (in words) is given by the formula (2 × n + 1) × m, where m is the number of registers in the selected Context Model.* *If PPE = 1 and the PCP attempts to perform a data write to PRAM addresses below the CSA, an error condition has occurred.* *This setting also controls the maximum channel number (MCN) used in system. The maximum channel number is MCN = 2 × n. If the SRPN is greater than MCN, an error condition has occurred.* *For example, setting PPS to n = 3 will give a CSA containing 7 context save regions. As channel 0 cannot be used and MCN = 6, channels 1 to 6 are allowed.*
PPE	8	rw	**PRAM Partitioning Enable** 0_B PRAM is not partitioned 1_B PRAM is partitioned *Note: When partitioned, the PRAM is divided into two areas (CSA and remainder). A PCP error will be generated on an inappropriate action in either region (PCP write operation with a target address in the CSA, or context restore from outside the CSA).*
CS	[7:6]	rw	**Context Size Selection** 00_B Use Full Context for all channels 01_B Use Small Context for all channels 10_B Use Minimum Context for all channels 11_B Reserved
EIE	5	rw	**Endinit Enable** 0_B PCP_CS is not Endinit protected. 1_B PCP_CS is Endinit protected.

Field	Bits	Type	Description
RCB	4	rw	**Channel Start Mode Control** 0_B Channel resume operation mode selected; channel start PC is taken from restored context 1_B Channel restart operation mode selected; channel start PC is derived from the requested channel number (= priority number of service request) *Note: This is a global control bit and applies to all channels.*
RES	3	r	**Reserved** Read as 0; should be written with 0.
RS	2	rh	**PCP Run/Stop Status Flag** 0_B PCP is stopped or idle (default) 1_B PCP is currently running
RES	1	r	**Reserved** Read as 0; should be written with 0.
EN	0	rw	**PCP Enable** 0_B PCP is disabled for operation (default) 1_B PCP is enabled for operation *Note: This bit does not enable/disable clocks for power saving. It stops the PCP from accepting new service requests.*

11.17.4 PCP Error/Debug Status Register, PCP_ES

This is a read-only register, providing state information about error and debug conditions.

PCP_ES
PCP Error/Debug Status Register (14_H) Reset Value: 0000 0000$_H$



Field	Bits	Type	Description
EPC	[31:16]	rh	**Error PC** PC value of the instruction that was executing when an error or debug event occurred. Default = 0000_H.
EPN	[15:8]	rh	**Error Service Request Priority Number** Channel number of the channel that was operating when the last error/debug event occurred. The value stored is the SRPN which invoked this channel (= channel number), NOT the current PCP priority number stored in field CPPN in register PICR. Default = 00_H.
PPC	7	rh	**PRAM Partitioning Check** Set if the last error/debug event was an error generated by a channel program attempting to perform a write to a PRAM address within the CSA, or receipt of an interrupt request that would have caused a context restore from outside the CSA.
CWD	6	rh	**Channel Watchdog Triggered** Set if the last error/debug event was an error generated by a channel program attempting to execute more instructions than allowed by PCP_CS.CWT.
ME	5	rh	**Memory Error** This bit is set if a PCP internal memory error has occurred. See **Table 11.22 "Implementation of the PCP in the TC1798" on Page 11-157** for TC1798 specific implementation.
DBE	4	rh	**Debug Event Flag** Set if the last error/debug event was a debug event. *Note: A debug event does not cause the posting of an interrupt to the CPU.*
IAE	3	rh	**Instruction Address Error** Set if the last error/debug event was an error generated by the PCP attempting to fetch an instruction from an address outside the implemented CMEM range as a result of a jump or branch instruction; otherwise, clear.

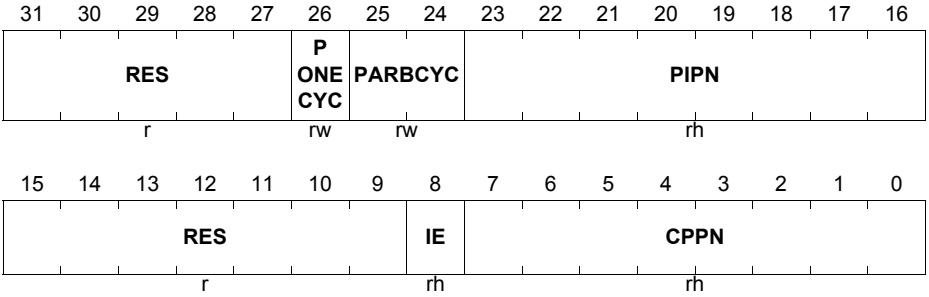
Field	Bits	Type	Description
DCR	2	rh	**Disabled Channel Request Flag** Set if the last error/debug event was an error generated by receipt of an interrupt request with an SRPN that attempted to start a disabled PCP channel; otherwise, clear.
IOP	1	rh	**Invalid Opcode** Set if the last error/debug event was an error generated by the PCP attempting to execute an Invalid Opcode (i.e. the value fetched from CMEM for execution by the PCP did not represent a valid instruction), otherwise clear.
BER	0	rh	**Bus Error Flag** Set if the last error/debug event was an error generated by an FPI Bus error or an invalid address access; otherwise, clear. *Note: An FPI Bus error event does not cause the PCP to post an error interrupt to the CPU. An FPI Bus error interrupt is, however, generated by the FPI control logic.*

Note: An interrupt request with the SRPN held in PCP_CS.ESR is posted to the CPU whenever a PCP error event, other than an FPI Bus error occurs. FPI Bus error interrupt generation is automatically handled by the FPI Bus control logic, rather than by the PCP. The execution of a DEBUG instruction is not classed as an error event and does not therefore generate an interrupt request to the CPU. The entire contents of the register are updated whenever there is a debug or an error event detected (i.e. all status/error bits, other than the bit representing the last PCP error/debug event, are cleared). This register therefore only provides a record of the last error/debug event encountered. The only way to clear this register is to reset the PCP.

11.17.5 PCP Interrupt Control Register, PCP_ICR

This register controls the operation of the PCP Interrupt Control Unit (PICU).

PCP_ICR
PCP Interrupt Control Register (20_H) Reset Value: 0000 0000$_H$

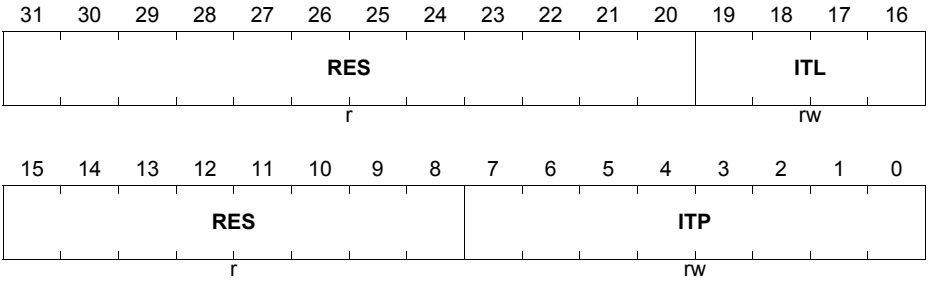


Field	Bits	Type	Description
RES	[31:27]	r	**Reserved** Read as 0; should be written with 0.
PONECYC	26	rw	**Clocks per Arbitration Cycle Control** This bit determines the number of clocks per arbitration cycle. 0_B Two clocks per arbitration cycle (default) 1_B One clock per arbitration cycle
PARBCYC	[25:24]	rw	**Number of Arbitration Cycles Control** This bit field controls the number of arbitration cycles used to determine the request with the highest priority. It follows the same coding scheme as described for the CPU interrupt arbitration. 00_B Four arbitration cycles (default) 01_B Three arbitration cycles 10_B Two arbitration cycles 11_B One arbitration cycle
PIPN	[23:16]	rh	**Pending Interrupt Priority Number** This read-only field is updated by the PICU at the end of each arbitration process, and indicates the priority number of a pending request. PIPN is set to 00_H when no request is pending and at the beginning of a new arbitration process.
RES	[15:9]	r	**Reserved** Read as 0; should be written with 0.

Field	Bits	Type	Description
IE	8	rh	**Reserved**
CPPN	[7:0]	rh	**Current PCP Priority Number** This field indicates the current priority level of the PCP and is automatically updated by hardware on entry into an interrupt service routine.

11.17.6 PCP Interrupt Threshold Register, PCP_ITR

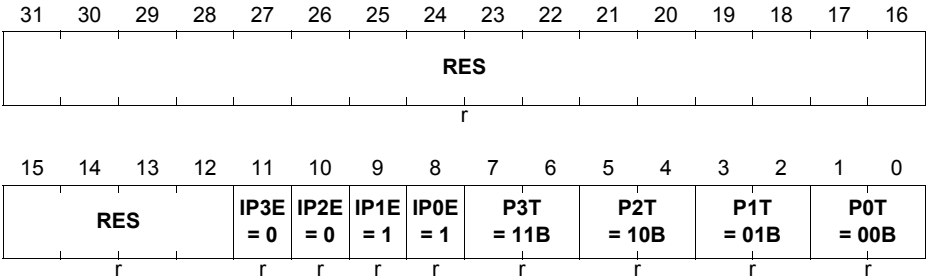
PCP_ITR
PCP Interrupt Threshold Control Register
(24_H) **Reset Value: $0000\ 0000_H$**



Field	Bits	Type	Description
RES	[31:20]	r	**Reserved** Read as 0; should be written with 0.
ITL	[19:16]	rw	**Interrupt Threshold Level** This bit field specifies the number of active interrupt entries at which an warning interrupt should be issued to the interrupt queue associated with interrupt bus 0 (i.e. when the number of active port 0 interrupt requests stored in all SRCx registers reaches this value then an interrupt is posted to port 0 with the priority programmed into the ITP field). When ITL is programmed to 0 or is ≥ the number of SRCx registers that can contain port 0 interrupt requests, the threshold warning mechanism is disabled).
RES	[15:8]	r	**Reserved** Read as 0; should be written with 0.
ITP	[7:0]	rw	**PCP Interrupt Threshold Service Request Priority Number** This field contains the interrupt priority that is to be posted to the interrupt queue associated with interrupt bus 0 when the threshold condition is reached (setting this value to 0 or disables the threshold detection mechanism).

11.17.7 PCP Interrupt Configuration Register, PCP_ICON

PCP_ICON
PCP Interrupt Configuration Register (28_H) **Reset Value: 0000 03E4$_H$**

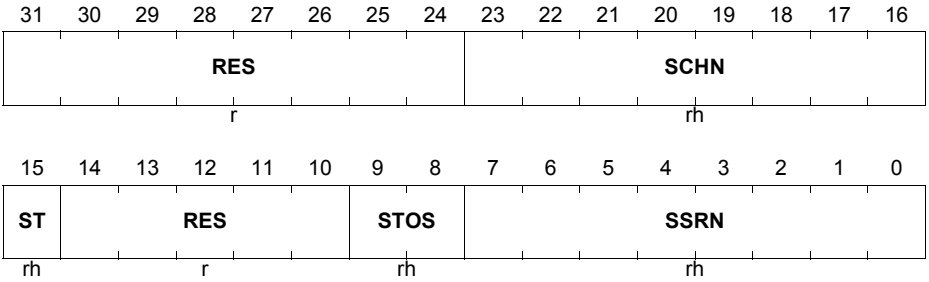


Field	Bits	Type	Description
RES	[31:12]	r	**Reserved** Read as 0.
IP3E	11	r	**PCP Interrupt Bus 3 Enable** This bit reflects the status of interrupt bus 3. Interrupt bus 3 is always disabled (not implemented in the TC1798).
IP2E	10	r	**PCP Interrupt Bus 2 Enable** This bit reflects the status of interrupt bus 2. Interrupt bus 2 is always disabled (not implemented in the TC1798).
IP1E	9	r	**PCP Interrupt Bus 1 Enable** This bit reflects the status of interrupt bus 1 (PCP interrupt arbitration bus). Interrupt bus 1 is always enabled.
IP0E	8	r	**PCP Interrupt Bus 0 Enable** This bit reflects the status of interrupt bus 0 (CPU interrupt arbitration bus). Interrupt bus 0 is always enabled.
P3T	[7:6]	r	**PCP Interrupt Bus 3 TOS Mapping** This field reflects the TOS associated with interrupt bus 3. *Note: Interrupt bus 3 is not available in the TC1798.*

Field	Bits	Type	Description
P2T	[5:4]	r	**PCP Interrupt Bus 2 TOS Mapping** This field reflects the TOS associated with interrupt bus 2. *Note: Interrupt bus 2 is not available in the TC1798.*
P1T	[3:2]	r	**PCP Interrupt Bus 1 TOS Mapping** This field reflects the TOS associated with interrupt bus 1 (PCP interrupt arbitration bus). The PCP should use this value in R6.TOS when it wishes to raise an interrupt request to itself (the PCP is always connected to interrupt bus 1).
P0T	[1:0]	r	**PCP Interrupt Bus 0 TOS Mapping** This field reflects the TOS associated with interrupt bus 0 (CPU interrupt arbitration bus). The PCP should use this value in R6.TOS when it wishes to raise an interrupt request via interrupt bus 0.

11.17.8 PCP Stall Status Register, PCP_SSR

PCP_SSR
PCP Stall Status Register **($2C_H$)** **Reset Value: 0000 0000$_H$**



Field	Bits	Type	Description
RES	[31:24]	r	**Reserved** Read as 0.
SCHN	[23:16]	rh	**PCP Stalled Channel Number** This field shows the channel number of the channel that was executing when the last (or present) stall condition occurred. This field can only be cleared by a reset.
ST	15	rh	**PCP Stalled Status** This bit shows the stalled status of the PCP 0_B PCP is not stalled 1_B PCP is stalled
RES	[14:10]	r	**Reserved** Read as 0.
STOS	[9:8]	rh	**PCP Stalled Type-of-Service** This field shows the Type-Of-Service to which an interrupt was being posted that caused the last (or present) stall condition (i.e. the service request queue that was full when the PCP attempted to post a request to it). This field can only be cleared by a reset.

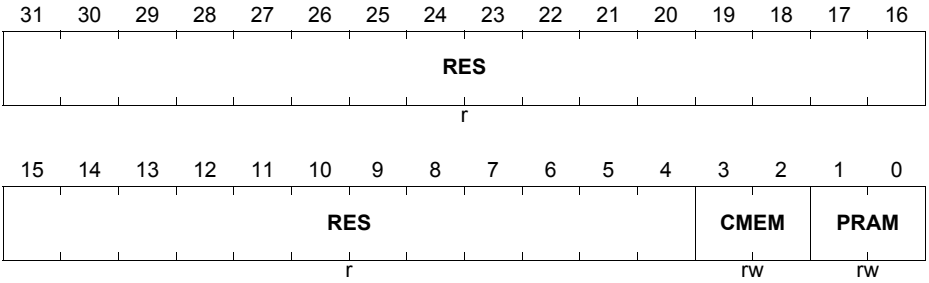
Field	Bits	Type	Description
SSRN	[7:0]	rh	**PCP Stalled Service Request Number** This field shows the Service Request Number that was being posted when the last (or present) stall condition occurred. This field can only be cleared by a reset.

11.17.9 SIST Mode Access Control Register, PCP_SMACON

*Note: Please see **Section 11.10** on **Page 11-46** for more information regarding the use of this register.*

This register is ENDINIT protected.

PCP_SMACON
SIST Mode Access Control Register (40_H) **Reset Value: $0000\ 0000_H$**



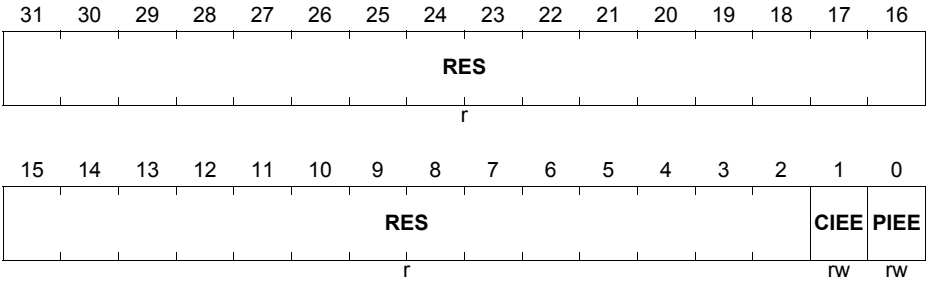
Field	Bits	Type	Description
RES	[31:4]	r	**Reserved** returns ‘0’ if read; should be written with ‘0’.
CMEM	[3:2]	rw	**CMEM SIST mode access control** 00_B Normal Operation, No Mapping 01_B Data Array Mapping, no error detection/correction 10_B Check Array Mapping, no error detection/correction 11_B Data Array Mapping, error detection/correction enabled
PRAM	[1:0]	rw	**PRAM SIST mode access control** 00_B Normal Operation, No Mapping 01_B Data Array Mapping, no error detection/correction 10_B Check Array Mapping, no error detection/correction 11_B Data Array Mapping, error detection/correction enabled

11.17.10 Memory Integrity Error Control Register, PCP_MIECON

*Note: Please see **Section 11.11** on **Page 11-47** for more information regarding the use of this register.*

This register is ENDINIT protected.

PCP_MIECON
SIST Mode Access Control Register (50_H) **Reset Value: $0000\ 0000_H$**

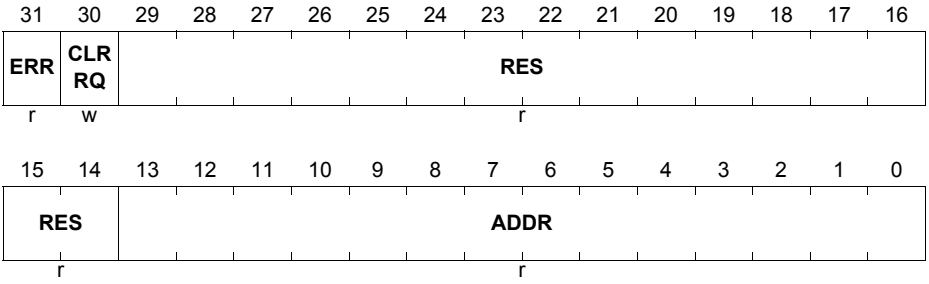


Field	Bits	Type	Description
RES	[31:2]	r	**Reserved** returns ‘0’ if read; should be written with ‘0’.
CIEE	1	rw	**CMEM Integrity Error Enable** Enables the integrity error handling for CMEM.
PIEE	0	rw	**PRAM Integrity Error Enable** Enables the integrity error handling for PRAM.

11.17.11 Memory Integrity Error Status Register for PRAM, PCP_MIESTATP

*Note: Please see **Section 11.11** on **Page 11-47** for more information regarding the use of this register.*

PCP_MIESTATP
Memory Integrity Error Status Register for PRAM(58_H) Reset Value: $0000\ 0000_H$

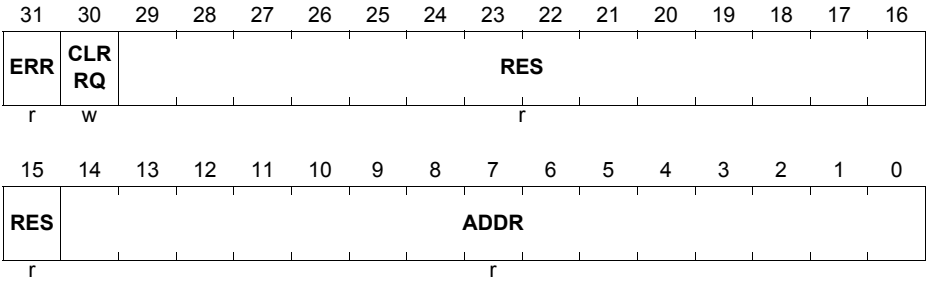


Field	Bits	Type	Description
ERR	31	r	**PRAM Memory Integrity Error Flag** Set when a memory integrity error is encountered . This bit remains set until the CLRRQ bit is written with ‘1’ or the PCP is reset.
CLRRQ	30	w	**Clear Status Request Bit** When written with ‘1’ this causes all other bits within the register to be cleared.
RES	[29:14]	r	**Reserved** returns ‘0’ if read; should be written with ‘0’.
ADDR	[13:0]	r	**PRAM Error Address** The (word) address of the PRAM location containing an error which caused the ERR bit to transition from ‘0’ to ‘1’.

11.17.12 Memory Integrity Error Status Register for CMEM, PCP_MIESTATC

*Note: Please see **Section 11.11** on **Page 11-47** for more information regarding the use of this register.*

PCP_MIESTATC
Memory Integrity Error Status Register for CMEM($5C_H$) Reset Value: $0000\ 0000_H$

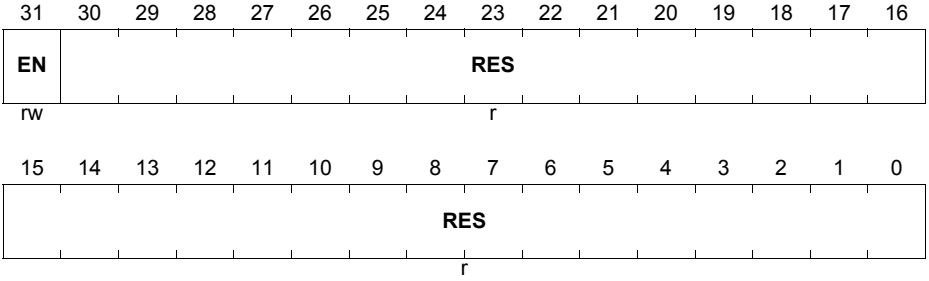


Field	Bits	Type	Description
ERR	31	r	**CMEM Memory Integrity Error Flag** Set when a memory integrity error is encountered. This bit remains set until the CLRRQ bit is written with ‘1’ or the PCP is reset.
CLRRQ	30	w	**Clear Status Request Bit** When written with ‘1’ this causes all other bits within the register to be cleared.
RES	[29:15]	r	**Reserved** returns ‘0’ if read; should be written with ‘0’.
ADDR	[14:0]	r	**CMEM Error Address** The (word) address of the CMEM location containing an error which caused the ERR bit to transition from ‘0’ to ‘1’.

11.17.13 Register Protection Register, PCP_RPROT

This register is ENDINIT protected.

PCP_RPROT
Register Protection Register **(70_H)** **Reset Value: 0000 0000_H**



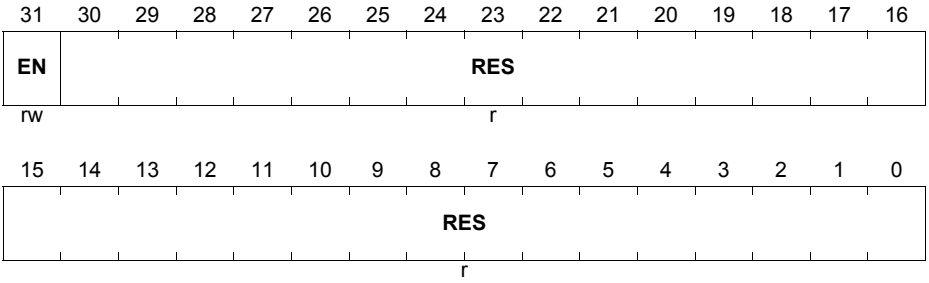
Field	Bits	Type	Description
EN	31	rw	**Register Protection Enable** 0_B Registers are not protected and can be written at any time. 1_B Registers are protected and can only be written when ENDINT is ‘0’.
RES	[30:0]	r	**Reserved** returns ‘0’ if read; should be written with ‘0’.

11.17.14 CMEM Protection Register, PCP_CPROT

*Note: Please see **Section 11.13.3** on **Page 11-58** for more information regarding the use of this register.*

This register is ENDINIT protected.

PCP_CPROT
CMEM Protection Register **(74_H)** **Reset Value: 0000 0000$_H$**



Field	Bits	Type	Description
EN	31	rw	**Register Protection Enable** 0_B CMEM is not protected and can be written at any time. 1_B CMEM is protected and can not be written.
RES	[30:0]	r	**Reserved** returns ‘0’ if read; should be written with ‘0’.

11.17.15 PRAM Protection Register, PCP_PPROT

This register is ENDINIT protected.

PCP_PPROT
PRAM Protection Register **(78_H)** **Reset Value: 0000 0000$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
EN	ENI	RES					PCAT	PTHRES							
rw	rw	r					rw	rw							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PSIZE								FBASE							
rw								rw							

Field	Bits	Type	Description
EN	31	rw	**PRAM Protection Enable for FPI Writes** 0_B PRAM is not protected and can be written via FPI at any time. 1_B All PRAM outside the Open Window is protected and can not be written via FPI. PRAM inside the Open Window remains writable via FPI.

Field	Bits	Type	Description
ENI	30	rw	**PRAM Protection Enable for Internal Writes** 0_B The entire PRAM (subject to PRAM partitioning) is not protected and can be written using PCP PRAM write instructions. 1_B All PRAM outside the Protected Window (and subject to PRAM partitioning) is not protected and can be written using PCP PRAM write instructions. PRAM inside the Protected Window remains writable using PCP PRAM write instructions only by a protected channel (subject to PRAM partitioning). *Note: PRAM partitioning (which is enabled/controlled by CS.PPE and CS.PPS) takes precedence over PRAM protection. Therefore if PRAM Partitioning is enabled, the entire Context Region will be protected against PCP PRAM write instructions, regardless of the Protection settings or whether the channel is Protected or not.*
RES	[29:25]	r	**Reserved** Returns ‘0’ if read. Should be written with ‘0’.
PCAT	24	rw	**Protected Channels Above Threshold** When ENI (above) is ‘0’, this bit has no effect. When ENI is ‘1’, this bit defines whether the Channel number defined in the PTHRES represents the lowest of the highest protected Channel; 0_B The Channel with the number defined by PPROT.PTHRES is the highest Channel Program that is treated as protected. All Channel’s with numbers below the value of PPROT.PTHRES are also treated as protected. 1_B The Channel with the number defined by PPROT.PTHRES is the lowest Channel program that is treated as protected. All Channel’s with numbers above the value of PPROT.PTHRES are also treated as protected.

Field	Bits	Type	Description
PTHRES	[23:16]	rw	**Protected Channel Threshold** When PPROT.ENI is ‘0’, this field has no effect. When PPROT.ENI is ‘1’, this field defines the Channel number which is used to distinguish between protected and non-protected Channels.
PSIZE	[15:8]	rw	**PRAM Internally Protected Window Size** When PPROT.ENI is ‘0’, this field has no effect. When PPROT.ENI is ‘1’, this field defines the size (in multiples of 256 bytes) of the region at the bottom of PRAM that can only be written (using PRAM write instructions) by Protected Channels. *Note: Each value n, from 1_D, up to the maximum 255_D,is multiplied by 256 Bytes* 0_D 0 Bytes (i.e. there is no Protected Window; the entire PRAM (subject to PRAM Partitioning) can be written by the use of PRAM write instructions by any Channel). 1_D 256 Bytes (i.e. the lowest 64 words of PRAM are protected against PRAM write instructions executed by non-protected Channels). ....$_B$ ... 255_D 255 * 256 Bytes *Note: Use of an eight bit field allows for the maximum PRAM size currently supported by the architecture (64Kbytes). Where a PCP is implemented with a smaller PRAM, setting a Protected Window size greater than the actual PRAM size will result in the entire PRAM being protected against PRAM write instructions executed by non-protected Channels.* *Note: When enabled, the PRAM Partitioning protection scheme (enabled via CS.PPE and CS.PPE) takes precedence and will protect the Context Save region from modification by PRAM write instructions (regardless of whether an instruction was executed by a Protected Channel or not).*

Field	Bits	Type	Description
FBASE	[7:0]	rw	**PRAM FPI Open Window Base** When PPROT.EN is ‘0’, this field has no effect. When PPROT.EN is '1' (see above) this field defines the base address (in multiples of 256 bytes and relative to the base of PRAM) of the region at the top of PRAM that remains writable by FPI writes. *Note: From 1_D up to 254_D: Base of PRAM + n * 256 Bytes* 0_D Base of PRAM (i.e. the entire PRAM can be written by FPI writes). 1_D Base of PRAM + 256 Bytes (i.e. all but the lowest 64 words of PRAM can be written via the FPI bus, the lowest 64 words of PRAM are protected against FPI Writes) …$_B$ … 254_D Base of PRAM + 254 * 256 Bytes. 255_D The entire PRAM is protected against FPI writes. *Note: Use of an eight bit field allows for the maximum PRAM size currently supported by the architecture (64Kbytes). Where a PCP is implemented with a smaller PRAM, setting an Open Window base above the actual top of PRAM will result in the entire PRAM being protected against FPI writes.* *Note: There is a small limitation with this scheme in that if a device is implemented with a 64K PRAM then it will not be possible to protect the entire PRAM (the top 64 words cannot be protected in this case). If this is a problem then bit 29 could be used as a “protect entire PRAM bit).*

11.17.16 FPI Write Window Register, PCP_FWWIN

*Note: Please see **Section 11.8.1** on **Page 11-42** for more information regarding the use of this register.*

This register is ENDINIT protected.

PCP_FWWIN
FPI Write Window Register **($7C_H$)** **Reset Value: 0000 0000$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
EN	EX	RES	SIZE					BASE							
rw	rw	r	rw					rw							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BASE															
rw															

Field	Bits	Type	Description
EN	31	rw	**FPI Protection Enable** 0_B The addresses of outgoing FPI writes are not checked. 1_B During execution of an instruction that generates an FPI write, a check is performed that the target address within the programmed allowed address range. If the address not to an allowed address then an FPI write is not issued and the PCP exits the current Channel with IOP error.
EX	30	rw	**Window Mode** 0_B Limit mode. The destination address of FPI write instructions must lie within the defined window. 1_B Exclude mode. The destination address of FPI write instructions must lie outside the defined window.
RES	29	r	**Reserved** Returns ‘0’ if read. Should be written with ‘0’.

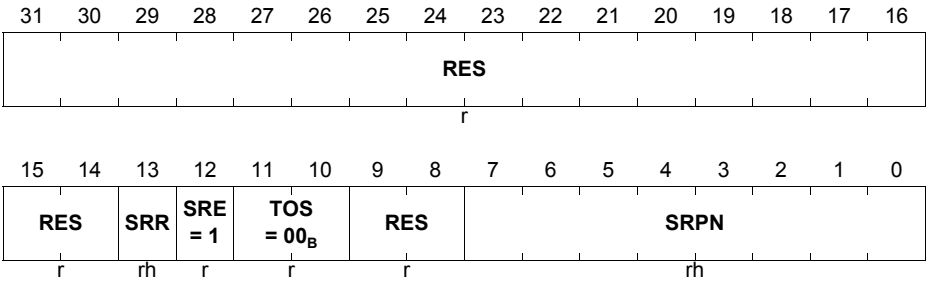
Field	Bits	Type	Description
SIZE	[28:24]	rw	**Window Size** The FPI window size (binary sizing) 0_D 256 bytes 1_D 512 bytes ...$_B$ ... 31_D $2^{(n+8)}$ bytes
BASE	[23:0]	rw	**Window Base Address** Controls the base address of the FPI window (binary aligned according to the window size. Bit 23 maps to the bit 31 of the FPI byte address. The appropriate number of subsequent bits defines the aligned address according to the window size (e.g. when using a 1Kbyte window, the lower 2 bits of this field are treated as zero, regardless of their actual value, in order to obtain the base address of the window).

11.17.17 PCP Service Request Control Registers m, PCP_SRC[1:0]

Service request nodes for interrupt bus 0 (CPU interrupt arbitration bus).

PCP_SRCm (m = 0-1)
PCP Service Request Control Register m

(FC_H-m*4_H) **Reset Value: 0000 1000$_H$**



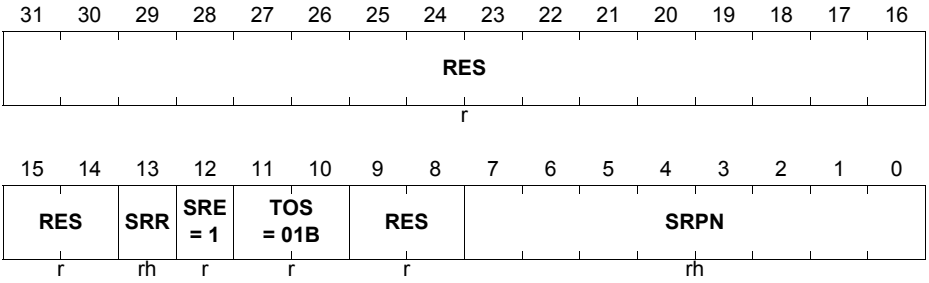
Field	Bits	Type	Description
RES	[31:14]	r	**Reserved** Read as 0.

Field	Bits	Type	Description
SRR	13	rh	**PCP Node m Service Request Flag** 0_B No service requested (default). 1_B Valid active service requested.
SRE	12	r	**PCP Node m Service Request Enable** Always read as 1 (enabled).
TOS	[11:10]	r	**PCP Node m Type-of-Service State** Always read as 00_B. This means TOS is associated with interrupt bus 0 (CPU interrupt arbitration bus).
RES	[9:8]	r	**Reserved** Read as 0.
SRPN	[7:0]	rh	**PCP Node m Service Request Priority Number** This number is automatically set by the PCP if it needs to place a service request on interrupt bus 0 (CPU interrupt arbitration bus). Default after reset is 00_H.

11.17.18 PCP Service Request Control Registers m, PCP_SRC[3:2]

Service request nodes for interrupt bus 1 (PCP interrupt arbitration bus).

PCP_SRCm (m = 2-3)
PCP Service Request Control Register m
(FC_H-m*4_H) **Reset Value: 0000 1400$_H$**

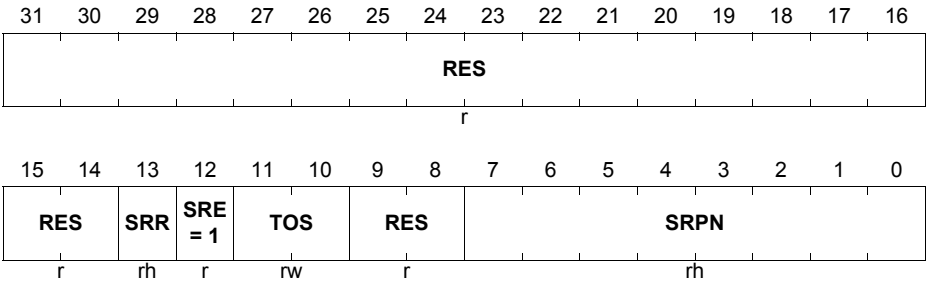


Field	Bits	Type	Description
RES	[31:14]	r	**Reserved** Read as 0.
SRR	13	rh	**PCP Node m Service Request Flag** 0_B No service requested (default). 1_B Valid active service requested.
SRE	12	r	**PCP Node m Service Request Enable** Always read as 1 (enabled).
TOS	[11:10]	r	**PCP Node m Type-of-Service State** Always read as 01_B. This means TOS is associated with interrupt bus 1 (PCP interrupt arbitration bus).
RES	[9:8]	r	**Reserved** Read as 0.
SRPN	[7:0]	rh	**PCP Node m Service Request Priority Number** This number is automatically set by the PCP if it needs to place a service request on interrupt bus 1 (PCP interrupt arbitration bus). Default after reset is 00_H.

11.17.19 PCP Service Request Control Registers m, PCP_SRC[8:4]

Service request nodes programmable for interrupt bus 0 (CPU interrupt arbitration bus) or 1 (PCP interrupt arbitration bus).

PCP_SRCm (m = 4-8)
PCP Service Request Control Register m
(FC_H-m*4_H) **Reset Value: 0000 1000$_H$**



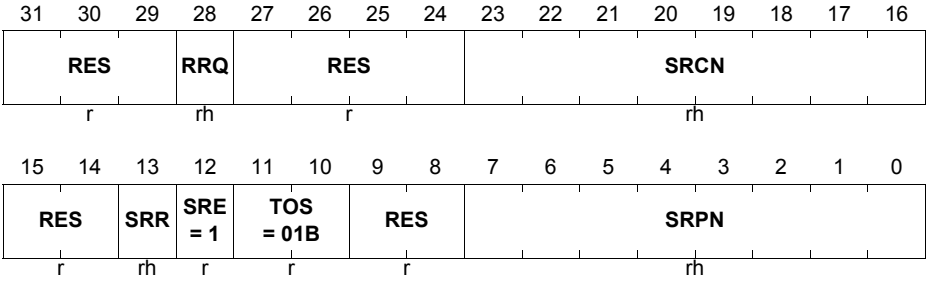
Field	Bits	Type	Description
RES	[31:14]	r	**Reserved** Read as 0. Should be written with 0.
SRR	13	rh	**PCP Node m Service Request Flag** 0_B No service requested (default). 1_B Valid active service requested.
SRE	12	r	**PCP Node m Service Request Enable** Always read as 1 (enabled).
TOS	[11:10]	rw	**PCP Node m Type-of-Service State/Control** TOS value depends on the interrupt mapping that has been selected (see **Page 11-151**). This bit field must be written at PCP configuration time and should not subsequently modified while the PCP is operating.
RES	[9:8]	r	**Reserved** Read as 0. Should be written with 0.

Field	Bits	Type	Description
SRPN	[7:0]	rh	**PCP Node m Service Request Priority Number** This number is automatically set by the PCP if it needs to place a service request on interrupt bus 0 (CPU interrupt arbitration bus) or 1 (PCP interrupt arbitration bus). Default after reset is 00_H.

11.17.20 PCP Service Request Control Registers m, PCP_SRC[11:9]

Service request nodes for interrupt bus 1 (PCP interrupt arbitration bus) with suspended interrupt capability.

PCP_SRCm (m = 9-11)
PCP Service Request Control Register m
(FC_H-m*4_H) **Reset Value: 0000 1400$_H$**



Field	Bits	Type	Description
RES	[31:29]	r	**Reserved** Read as 0.
RRQ	28	rh	**PCP Node m Channel Restart Request** Set when this service request register n contains an active service request that is associated with a suspended interrupt (i.e. a channel that has been interrupted by a higher-priority channel). 0_B The interrupt is not suspended 1_B The interrupt is suspended RRQ is always 0 when SRR is 0.
RES	[27:24]	r	**Reserved** Read as 0.

Field	Bits	Type	Description
SRCN	[23:16]	rh	**PCP Node m Service Request Channel Number** Channel Number Entry (default = 0). When the PCP interrupt request was raised by the PCP Processor Core when executing an EXIT instruction, then this bit field contains the SRPN value taken from R6 when the exit instruction was executed. When the PCP interrupt request was raised by the PCP Processor Core when suspending execution of a channel program in order to service a higher-priority interrupt then this bit field contains the channel number of the channel that was suspended.
RES	[15:14]	r	**Reserved** Read as 0.
SRR	13	rh	**PCP Node m Service Request Flag** 0_B No service requested (default) 1_B Valid active service requested
SRE	12	r	**PCP Node m Service Request Enable** Always read as 1 (enabled).
TOS	[11:10]	r	**PCP Node m Type-of-Service State** Always read as 01_B. This means TOS is associated with interrupt bus 1 (PCP interrupt arbitration bus).
RES	[9:8]	r	**Reserved** Read as 0.
SRPN	[7:0]	rh	**PCP Node m Service Request Priority Number** This number is automatically set by the PCP if it needs to place a service request on interrupt bus 0 (CPU interrupt arbitration bus) or 1 (PCP interrupt arbitration bus). When the PCP interrupt request contained was raised by the PCP Processor Core when executing an EXIT instruction then this bit field contains the SRPN value taken from R6 when the exit instruction was executed. When the PCP interrupt request was raised by the PCP Processor Core when suspending execution of a channel program in order to service a higher-priority interrupt then this bit field contains the CPPN value of the PCP when the interrupt was suspended.

11.18 PCP Instruction Set Details

This section describes the instruction set architecture of the PCP in detail.

11.18.1 Instruction Codes and Fields

All PCP instructions use a common set of fields to describe such things as the source register, and the state of flags. Additionally, many instructions (including arithmetic and many flow control instructions), are conditionally executed.

The descriptions of the PCP instructions are based on the following conventions.

>>, <<	Shift left or right, respectively.
[ ]	Indirect access based on contents of brackets (de-reference).
#immNN	Immediate value encoded into an instruction with width NN.
#offsetNN	Address offset immediate value with width NN.
NextPC	The current executing instruction’s address + 1. (The next instruction to be fetched.)
cc_A, cc_B	Condition Code CONDCA/CONDCB.

11.18.1.1 Conditional Codes

Many PCP instructions have the option of being executed conditionally. The condition code of an instruction is the field that specifies the condition to be tested before the instruction is executed. Depending on the type of instruction there are 8 or 16 condition codes available. The set of 8-condition codes is referred to as CONDCA, while the set of 16-condition codes is referred to as CONDCB. The condition codes are based on an equation of the Flags held in R7. See **Table 11-13**.

Table 11-13 Condition Codes

Description	CONDCA/B	Test (Flag Bits)	Code	Mnemonic
Unconditional	A / B	–	0_H	cc_UC
Zero/Equal	A / B	Z = 1	1_H	cc_Z
Not Zero/Not Equal	A / B	Z = 0	2_H	cc_NZ
Overflow	A / B	v = 1	3_H	cc_V
Carry/Unsigned Less Than/ Check Bit True	A / B	C = 1	4_H	cc_C, cc_ULT
Unsigned Greater Than	A / B	C OR Z = 0	5_H	cc_UGT
Signed Less Than	A / B	N XOR V = 1	6_H	cc_SLT
Signed Greater Than	A / B	(N XOR V) OR Z = 0	7_H	cc_SGT
Negative	B	N = 1	8_H	cc_N
Not Negative	B	N = 0	9_H	cc_NN
Not Overflow	B	V = 0	A_H	cc_NV
No Carry/Unsigned Greater than or Equal	B	C = 0	B_H	cc_NC, cc_UGE
Signed Greater Than or Equal	B	N XOR V = 0	C_H	cc_SGE
Signed Less than or Equal	B	(N XOR V) OR Z = 1	D_H	cc_SLE
CNT1 Equal Zero	B	CNZ1 = 1	E_H	cc_CNZ
CNT1 Not Equal Zero	B	CNZ1 = 0	F_H	cc_CNN

11.18.1.2 Instruction Fields

Table 11-14 lists the instruction field definitions of the PCP instruction set architecture.

Note: The exact syntax for these fields may be different depending on which tool (e.g. assembler) is used. Please refer to the respective tool descriptions.

Table 11-14 Instruction Field Definitions

Symbol	Syntax	Description
cc_A, cc_B	see Table 11-13	**Condition Code** Specifies conditional execution of instruction according to CONDCA or CONDCB.
CNC		**Counter Control** This field is used by the BCOPY/COPY instructions to control the number of repetitions of the data transfer. For BCOPY operation see Figure 11 - 2 on Page 11-104. For COPY operation see Figure 11 - 1 on Page 11-103.
	$CNC = 00_B$	Perform the number of transfers specified by CNT0 then proceed to next instruction.
	$CNC = 01_B$	Perform the number of transfers specified by CNT0 then decrement CNT1 and proceed to next instruction.
	$CNC = 10_B$	Perform the number of transfers specified by CNT0 then decrement CNT1. Repeat until CNT1 = 0, then proceed to next instruction.
	$CNC = 11_B$	Reserved.
CNT0		**Counter Reload Value (COPY)** The COPY instruction uses an implicit counter to generate multiple data transfers. The CNT0 value given in the instruction specifies how many data transfers are to be performed by the instruction. See also Figure 11 - 1 on Page 11-103.
	CNT0 = $001_B..111_B$	Perform 1..7 data transfers
	CNT0 = 000_B	Perform 8 data transfers
		Block Size (BCOPY) Selects the FPI block size used for a BCOPY instruction.
	$CNT0 = 00_B$	Use block size of 8 words.
	$CNT0 = 10_B$	Use block size of 2 words.
	$CNT0 = 11_B$	Use block size of 4 words.
	Others	Reserved

Table 11-14 Instruction Field Definitions (cont'd)

Symbol	Syntax	Description
DAC		**Stop PCP**
	DAC = 0	Allow the PCP to continue to execute channel programs in response to service requests.
	DAC = 1	Prevent the PCP from executing further channel programs (PCP_CS.EN = 0).
DST+-		**Destination Address Pointer Control**
	DST (00_B)	No Change (DST)
	DST+ (01_B)	Post Increment by Size (DST+)
	DST- (10_B)	Post Decrement by Size (DST-)
	(11_B)	Reserved
EC		**Exit Count Control**
	EC = 0	No action
	EC = 1	Decrement CNT1
EDA		**External Debug Action**
	EDA = 0	No External Debug Action caused
	EDA = 1	Cause an External Debug Action (breakpoint pin etc.)
EP		**Entry Point Control**
	EP = 0	Set the PC to channel program Start. EP = 0 assumes that a Channel Entry Table exists in the base of CMEM. Failure to provide such a table will cause improper operation.
	EP = 1	Set the PC to the address contained in NextPC (next instruction) address.
INT		**Interrupt Control**
	INT = 0	No Interrupt
	INT = 1	INT = 1 AND (cc_B = True) means Issue Interrupt
RTA		**Action on Debug Exit**
	RTA = 0	Stop channel program from accepting new service requests (clear R7.CEN)
	RTA = 1	Allow further channel program execution and decrement PC (so that DEBUG instruction is re-executed on next invocation) *Note: This field has no effect if SDB = 0 (see below)*
S/C		**Test Bit Control**
	S/C = 0	Check for Clear (0)
	S/C = 1	Check for Set (1)
SDB		**Stop on Debug**
	SDB = 0	Continue running if debug event triggered
	SDB = 1	Stop PCP if debug event triggered

Table 11-14 Instruction Field Definitions (cont'd)

Symbol	Syntax	Description
SIZE		**Data Size Control**
	SIZE = 00_B	Byte (8-bit)
	SIZE = 01_B	Half-word (16-bit)
	SIZE = 10_B	Word (32-bit)
	SIZE = 11_B	Reserved
SRC+-		**Source Address Pointer Control**
	SRC (00_B)	No Change (SRC)
	SRC+ (01_B)	Post Increment by Size (SRC+)
	SRC- (10_B)	Post Decrement by Size (SRC-)
	(11_B)	Reserved
ST		**Stop Channel**
	ST = 0	Continue channel execution, leave channel program enabled
	ST = 1	Stop Channel Execution, perform actions according to RTA setting (see above)

11.18.2 Counter Operation for COPY Instruction

Figure 11 - 1 shows the flow of a COPY instruction.

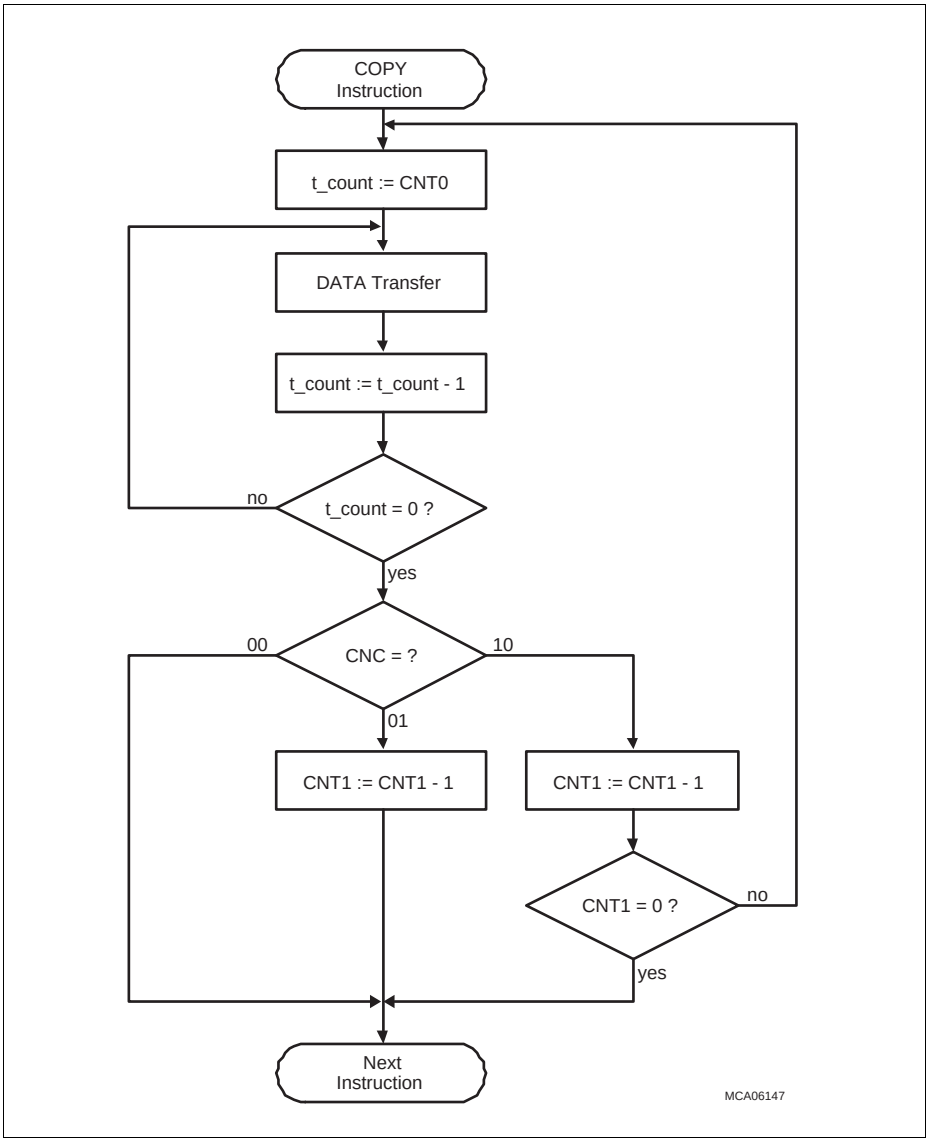


Figure 11 - 1 Counter Operation for COPY Instruction

11.18.3 Counter Operation for BCOPY Instruction

Figure 11 - 2 shows the flow of a BCOPY instruction.

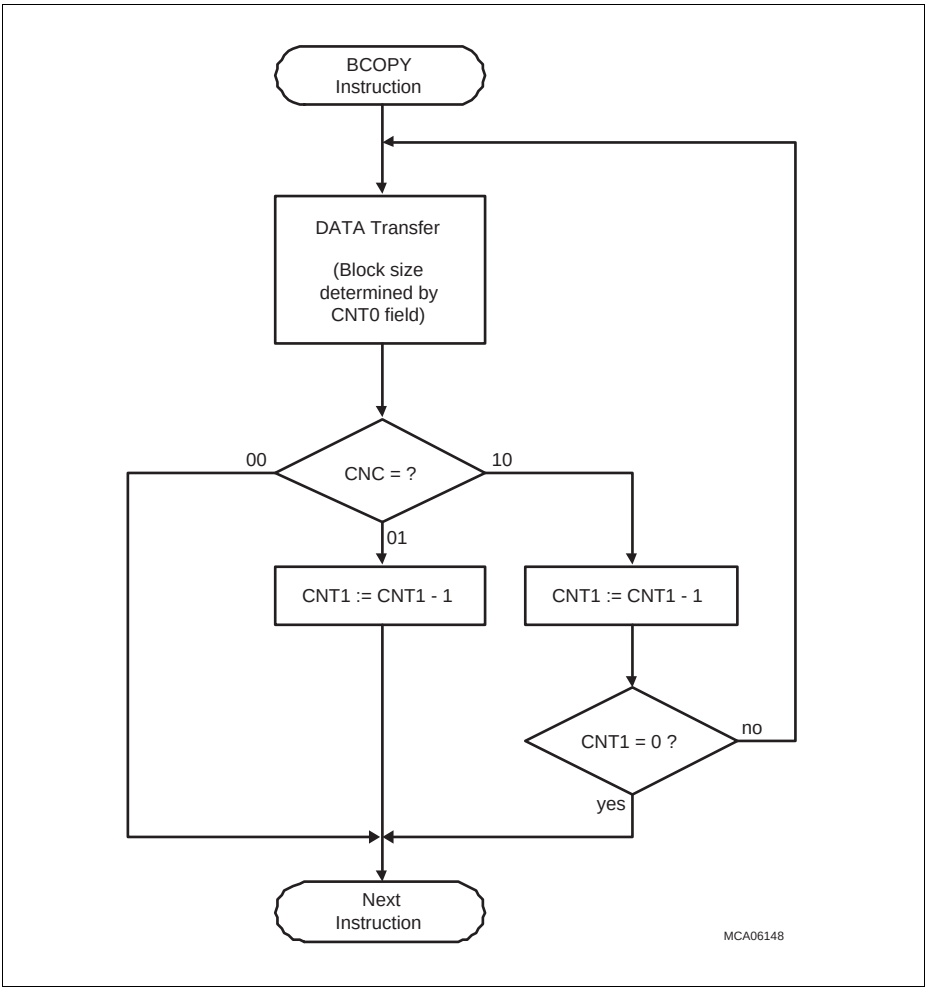


Figure 11 - 2 Counter Operation for BCOPY Instruction

11.18.4 Divide and Multiply Instructions

The PCP has Multiply and Divide capabilities (unsigned values only). All Multiply and divide instructions operate on 8 bits of data (taken from the dividend for divide, from the multiplicand for multiply). This strategy allows the user to implement the appropriate number of instructions (“steps”) as required for the user’s data format.

Each execution of a divide instruction (DSTEP) performs a division which generates 8 bits of result, and also manipulates the registers being used to allow the execution of consecutive divide (DSTEP) instructions to build divide algorithms in multiples of 8 bits (see **Page 11-154** for more details).

Each execution of a multiply instruction (MSTEP32 and MSTEP64) performs a multiplication on 8 bits of data (taken from the multiplicand) and also manipulates the registers to allow execution of consecutive multiply instructions to build multiply algorithms in multiples of 8 bits (see **Page 11-155** for more details).

The following restrictions apply to the use of Divide and Multiply instructions:

- The first instruction of any divide sequence must be the DINIT (initialization) instruction. Any additional instructions other than MINIT, MSTEP32 or MSTEP64 may also be used within the sequence as long as they do not modify any of the registers used for division (R0, Ra and Rb). All subsequent divide instructions within the sequence (DSTEP) must use the same register for dividend and the same register for divisor as used in the preceding DINIT instruction.
- The first instruction of any multiply sequence must be the MINIT (initialization) instruction. Any additional instructions other than DINIT or DSTEP may also be used within the sequence as long as they do not modify any of the registers used for multiplication (R0, Ra and Rb). All subsequent multiply instructions within the sequence (MSTEP32 and MSTEP64) must use the same register for multiplicand and the same register for multiplier as used in the preceding MINIT instruction.
- Neither of the operand registers (Ra or Rb) may be R0 (which is used implicitly within all the instructions), and the same register may not be supplied as both operand registers of an instruction (e.g. DSTEP R3, R3 is invalid).

Note: Failure to adhere to these restrictions will yield undefined results.

2. *Special care must be taken when using multiply and divide sequences when a channel program is interruptible. In this case it must be ensured that a sequence cannot be corrupted by the execution of multiply or divide instructions executed by a higher-priority channel. The R7.IEN bit can be used to ensure that a sequence is not interruptible (see* ***Page 11-153****).*

In the descriptions attached to each multiply and divide instruction, a pseudo-code model is supplied to provide an unambiguous definition of the function of the instruction. The models supplied for the DSTEP and MSTEP32 instructions use 32 bit unsigned integer arithmetic, ignoring any possible overflows. The model supplied for the MSTEP64 uses

a 40-bit unsigned multiply and then shifts this result right by 8 bits (discards the least significant 8 bits of the 40-bit result).

The DSTEP instruction also has some conditions stipulated regarding input values to the instruction. Use of the pseudo-code model for the DSTEP instruction with invalid input values will yield an invalid result.

11.18.5 ADD, 32-bit Addition

This section describes the ADD instructions of the PCP.

ADD	Syntax	**ADD Rb, Ra, cc_A**
	Description	If the condition CONDCA is true, then add the contents of register Ra to the contents of register Rb; place the result in Rb. If CONDCA is false, no operation is performed.
	Operation	if (CONDCA = True) then R[b] = R[b] + R[a] else NOP
	Flags	N, Z, V, C
ADD.I	Syntax	**ADD.I Ra, #imm6**
	Description	Add the zero-extended immediate value imm6 to the contents of register Ra; place the result in Ra.
	Operation	R[a] = R[a] + zero_ext(imm6)
	Flags	N, Z, V, C
ADD.F	Syntax	**ADD.F Rb, [Ra], Size**
	Description	Add the contents of the address location specified by the contents of register Ra to the contents of register Rb; place the result in Rb. *Note: Byte and Half-word values are zero-extended.*
	Operation	R[b] = R[b] + zero_ext(FPI[R[a]])
	Flags	N, Z, V, C
ADD.PI	Syntax	**ADD.PI Ra, [#offset6]**
	Description	Add the contents of the PRAM location specified by the addition of contents of the PRAM Data Pointer, shifted left by six bits, and the zero-extended 6-bit value offset6 to the contents of register Ra; place the result in Ra.
	Operation	R[a] = R[a] + PRAM[(DPTR<<6) + zero_ext(#offset6)]
	Flags	N, Z, V, C

11.18.6 AND, 32-bit Logical AND

This section describes the AND instructions of the PCP.

AND	Syntax	**AND Rb, Ra, cc_A**
	Description	If the condition CONDCA is true, then perform a bit-wise logical AND of the contents of register Ra and the contents of register Rb; place the result in Rb. If CONDCA is false, no operation is performed.
	Operation	if (CONDCA = True) then R[b] = R[b] AND R[a] else NOP
	Flags	N, Z
AND.F	Syntax	**AND.F Rb, [Ra], Size**
	Description	Perform a bit-wise logical AND of the contents of the address location, specified by the contents of register Ra, and the contents of register Rb; place the result in Rb.
	Operation	R[b] = R[b] AND zero_ext(FPI[R[a]])
	Flags	N, Z
AND.PI	Syntax	**AND.PI Ra, [#offset6]**
	Description	Perform a bit-wise logical AND of the contents of the PRAM location specified by the addition of contents of the PRAM Data Pointer, shifted left by six bits, and the zero-extended 6-bit value offset6, and the contents of register Ra; place the result in Ra.
	Operation	R[a] = R[a] AND PRAM[(DPTR<<6) + zero_ext(#offset6)]
	Flags	N, Z

11.18.7 BCOPY, DMA Operation

This section describes the BCOPY instruction of the PCP in the TC1798.

BCOPY	Syntax	**BCOPY DST+-, SRC+-, CNC, CNT0**
	Description	Allows the PCP to perform DMA type transfers using FPI block transfers. Moves the contents of FPI Bus source location to FPI Bus destination location. Source location is pointed to by the contents of register R4; destination location is pointed to by the contents of register R5. Options (see also **Table 11-14** at **Page 11-100**): Source pointer (SRC+-): Increment, decrement or unchanged Destination pointer (SRC+-): Increment, decrement or unchanged Counter control (CNC): see **Table 11-14** Block size value (CNT0): see **Table 11-14**
	Operation	temp = zero_ext(FPI[R[4]]); value loaded and extended depending on SIZE FPI(R[5]) = temp R4 = R4 +/- n; n depending on SRC+- and CNT0 R5 = R5 +/- n; n depending on DST+- and CNT0 For counter operation see **Figure 11 - 2** on **Page 11-104** and **Table 11-14** on **Page 11-100**.
	Flags	CN1Z

See also **Page 11-157** for TC1798 specific details of the BCOPY instruction.

11.18.8 CHKB, Check Bit

This section describes the CHKB instruction of the PCP.

CHKB	Syntax	**CHKB Ra, #imm5, S/C**
	Description	If bit imm5 of register Ra is equal to the specified test value S/C then set the carry flag R7.C, else clear the carry flag.
	Operation	if (R[a][imm5] = S/C) then R7_C = 1 else R7_C = 0
	Flags	C

11.18.9 CLR, Clear Bit

This section describes the CLR instructions of the PCP.

CLR	Syntax	**CLR Ra, #imm5**
	Description	Clear bit imm5 of register Ra to 0.
	Operation	R[a][imm5] = 0
	Flags	None
CLR.F	Syntax	**CLR.F [Ra], #imm5, Size**
	Description	Clear bit imm5 of the address location specified through the contents of register Ra to 0. This instruction is executed using a locked read-modify-write FPI Bus transaction.
	Operation	FPI[(R[a])][imm5] = 0
	Flags	None

11.18.10 COMP, 32-bit Compare

This section describes the COMP instructions of the PCP.

COMP	Syntax	**COMP Rb, Ra, cc_A**
	Description	If the condition CONDCA is true, then subtract the contents of register Ra from the contents of register Rb; set the flags in register R7 according to the result of the subtraction; discard the subtraction result. If CONDCA is false, no operation is performed.
	Operation	if (CONDCA = True) then R7_FLAGS = Flags(R[b] - R[a])
	Flags	N, Z, V, C
COMP.I	Syntax	**COMP.I Ra, #imm6**
	Description	Subtract the immediate value imm6 from the contents of register Ra; set the flags in register R7 according to the result of the subtraction; discard the subtraction result.
	Operation	R7_FLAGS = Flags(R[a] - zero_ext(imm6))
	Flags	N, Z, V, C
COMP.F	Syntax	**COMP.F Rb, [Ra], Size**
	Description	Subtract the contents of the address location specified by the contents of register Ra from the contents of register Rb; set the flags in register R7 according to the result of the subtraction; discard the subtraction result.
	Operation	R7_FLAGS = Flags(R[b] - zero_ext(FPI[R[a]]))
	Flags	N, Z, V, C
COMP.PI	Syntax	**COMP.PI Ra, [#offset6]**
	Description	Subtract the contents of the PRAM location specified by the addition of contents of the PRAM Data Pointer, shifted left by six bits, and the zero-extended 6-bit value offset6, from the contents of register Ra; set the flags in register R7 according to the result of the subtraction; discard the subtraction result.
	Operation	R7_FLAGS = Flags(R[a] - PRAM[(DPTR<<6) + zero_ext(#offset6)])
	Flags	N, Z, V, C

11.18.11 COPY, DMA Instruction

This section describes the COMP instruction of the PCP.

COPY	Syntax	**COPY DST+-, SRC+-, CNC, CNT0, SIZE**
	Description	Moves the contents of FPI Bus source location to FPI Bus destination location. Source location is pointed to by the contents of register R4; destination location is pointed to by the contents of register R5. Options (see also **Table 11-14** on **Page 11-100**): Source pointer (SRC+-): Increment, decrement or unchanged Destination pointer (SRC+-): Increment, decrement or unchanged Counter control (CNC): see **Table 11-14** Counter 0 reload value (CNT0): see **Table 11-14** Data transfer width (SIZE): byte, half-word, word (pointers are incremented/decremented based upon SIZE).
	Operation	temp = zero_ext(FPI[R[4]]); value loaded and extended depending on SIZE FPI(R[5]) = temp R4 = R4 +/- n; n depending on SRC+- and SIZE R5 = R5 +/- n; n depending on DST+- and SIZE For counter operation see **Figure 11 - 1** on **Page 11-103** and **Table 11-14** on **Page 11-100**.
	Flags	CN1Z

11.18.12 DEBUG, Debug Instruction

This section describes the DEBUG instruction of the PCP.

DEBUG	Syntax	**DEBUG EDA, DAC, RTA, SDB, cc_B**
	Description	Conditionally cause a debug event if condition CONDCB is true. Optionally stop channel execution (SDB = 1) and/or generate an external debug event (EDA = 1).

	Operation	if (CONDCB = True) then
		  if (EDA = 1) then activate BRK_OUT pin
		  if (SDB = 1) then
		  if (RTA = 0) then
		  R7_CEN = 0; disable further channel invocation
		  else
		  PC = PC - 1
		  endif
		  save_context
		  idle
		  endif
		  if (DAC = 1)
		  PCP_CS>EN = 0
		  endif
		  set ES.DBE; indicate debug event
		  ES.PC = NextPC
		  ES.PN = channel_number
		endif

	Flags	none

Note: Execution of the DEBUG command when not in Debug Mode will cause the PCP to generate an “Illegal Operation” Error Exit.

11.18.13 DINIT, Divide Initialization

This section describes the DINIT instruction of the PCP.

DINIT	Syntax	**DINIT <R0>, Rb, Ra**
	Description	Initialize Divide logic ready for divide sequence (Rb / Ra) and Clear R0. If value of Ra is 0 then set V (to flag divide by 0 error); otherwise, clear V. If value of Rb is 0 and value of Ra is not 0 then set Z (to flag a zero result); otherwise, clear Z.
	Operation	R0 = 0
	Flags	Z, V

11.18.14 DSTEP, Divide Instruction

This section describes the DSTEP instruction of the PCP.

DSTEP	Syntax	**DSTEP <R0>, Rb, Ra**
	Description	Perform 1 step (eight bits) of an unsigned 32- by 32-bit divide (Rb / Ra). Shift R0 left by 8 bits, copy the most significant byte of Rb into LS byte of R0. Shift Rb left by 8 bits and add (R0 divided by Ra). Load R0 with (the remainder of R0 divided by Ra).
	Operation	R0 = (R0 << 8) + (Rb >> 24) Rb = (Rb << 8) + R0 / Ra R0 = R0 % Ra
	Flags	Z

Note: The value in Ra must always be greater than the value in R0 prior to execution of the DSTEP instruction. If the rules specified on ***Page 11-105*** *are followed, then the above description and operation are correct. Failure to adhere to these rules will yield undefined results.*

11.18.15 EXIT, Exit Instruction

This section describes the EXIT instruction of the PCP.

EXIT	Syntax	**EXIT EC, ST, INT, EP, cc_B**
	Description	Unconditionally exit channel program execution. Optionally decrement counter CNT1 (EC = 1), disable further channel invocation (ST = 1), generate an interrupt request (INT = 1) if condition CONDCB is true. Field EP is used to set the channel code entry point in Channel Resume Mode to either the address of the next instruction (EP = 1) or to the start address of the channel (EP = 0). The EXIT instruction is finished with a context save operation. The EP option is only in effect when Channel Resume operation is globally selected through PCP_CS.RCB = 0. If PCP_CS.RCB = 1, Channel restart mode is selected for all channels, and the EP field of the EXIT instruction is disregarded.

	Operation	if (EC = 1) then CNT1 = CNT1 - 1
		if (ST = 1) then R7_CEN = 0
		if ((INT = 1) AND (cc_B = True)) then activate_interrupt_request
		if (EP = 1) then R7_PC = NextPC else R7_PC = channel_entry_point
		save_context

	Flags	CN1Z

11.18.16 INB, Insert Bit

This section describes the INB instructions of the PCP.

INB	Syntax	**INB Rb, Ra, cc_A**
	Description	If CONDCA is true, then insert the carry flag R7.C into register Rb at the bit position specified through bits [4..0] of register Ra. If CONDCA is false, no operation is performed.
	Operation	if (CONDCA = True) then R[b][R[a][4:0]] = R7_C else NOP
	Flags	None
INB.I	Syntax	**INB.I Ra, #imm5**
	Description	Insert the carry flag R7.C into register Ra at the bit position specified through the immediate value imm5.
	Operation	R[a][imm5] = R7_C
	Flags	None

11.18.17 JC, Jump Conditionally

This section describes the conditional jump instructions of the PCP.

JC	Syntax	**JC offset6, cc_B**
	Description	If CONDCB is true, then add the sign-extended value specified by offset6 to the contents of the PC, and jump to that address. If CONDCB is false, no operation is performed.
	Operation	if (CONDCB = True) then (PC = PC + sign_ext(offset6)) else NOP
	Flags	None
JC.A	Syntax	**JC.A #address16, cc_B**
	Description	If CONDCB is true, then load the value specified by address16 into the PC, and jump to that address. If CONDCB is false, no operation is performed.
	Operation	if (CONDCB = True) then (PC = address16) else NOP
	Flags	None
JC.I	Syntax	**JC.I Ra, cc_B**
	Description	If CONDCB is true, then add the value specified by Ra[15:0] to the contents of the PC, and jump to that address. Value Ra[15:0] is treated as a signed 16-bit number. If CONDCB is false, no operation is performed.
	Operation	if (CONDCB = True) then (PC = PC + (R[a][15:0])) else NOP
	Flags	None
JC.IA	Syntax	**JC.IA Ra, cc_B**
	Description	If CONDCB is true, then load the value specified by Ra[15:0] into the PC, and jump to that address. Value Ra[15:0] is treated as an unsigned 16-bit number. If CONDCB is false, no operation is performed.
	Operation	if (CONDCB = True) then (PC = (R[a][15:0])) else NOP
	Flags	None

11.18.18 JL, Jump Long Unconditional

This section describes the long jump instruction JL of the PCP.

JL	Syntax	**JL offset10**
	Description	Add the sign-extended value specified by offset10 to the contents of the PC, and jump to that address.
	Operation	PC = PC + sign_ext(offset10)
	Flags	None

11.18.19 LD, Load

This section describes the LD instructions of the PCP.

LD.F	Syntax	**LD.F Rb, [Ra], Size**
	Description	Load the zero-extended contents of the address location specified by the contents of register Ra into register Rb.
	Operation	R[b] = zero_ext(FPI[R[a]])
	Flags	N, Z
LD.I	Syntax	**LD.I Ra, #imm6**
	Description	Load the zero-extended value specified by imm6 into register Ra.
	Operation	R[a] = zero_ext(imm6)
	Flags	N, Z
LD.IF	Syntax	**LD.IF [Ra], #offset5, Size**
	Description	Load the zero-extended contents of the address location, specified by the addition of the contents of register Ra and the value specified by imm5, into register R0.
	Operation	R[0] = zero_ext(FPI[R[a] + zero_ext(imm5)])
	Flags	N, Z

LD.P	Syntax	**LD.P Rb, [Ra], cc_A**
	Description	If condition CONDCA is true, then load the contents of the PRAM address location, specified by the addition of contents of the PRAM Data Pointer, shifted left by six bits, and the zero-extended 6-bit value Ra[5:0] into register Rb. If condition CONDCA is false, no operation is performed.
	Operation	if (CONDCA = True) then R[b] = PRAM[(DPTR<<6) + zero_ext(R[a][5:0])] else NOP
	Flags	N, Z
LD.PI	Syntax	**LD.PI Ra, [#offset6]**
	Description	Load the contents of the PRAM location specified by the addition of contents of the PRAM Data Pointer, shifted left by six bits, and the zero-extended 6-bit value offset6 into register Ra.
	Operation	R[a] = PRAM[(DPTR<<6) + zero_ext(offset6)]
	Flags	N, Z

11.18.20 LDL, Load 16-bit Value

This section describes the LDL instructions of the PCP.

LDL.IL	Syntax	**LDL.IL Ra, #imm16**
	Description	Load the immediate value imm16 into the lower bits of register Ra (bits [15:0]). Bits [31:16] of register Ra are unaffected. Value imm16 is treated as an unsigned 16-bit number.
	Operation	R[a][15:0] = imm16
	Flags	N, Z
LDL.IU	Syntax	**LDL.IU Ra, #imm16**
	Description	Load the immediate value imm16 into the upper bits of register Ra (bits [31:16]). Bits [15:0] of register Ra are unaffected.
	Operation	R[a][31:16] = imm16
	Flags	N, Z

11.18.21 MINIT, Multiply Initialization

This section describes the MINIT instruction of the PCP.

MINIT	Syntax	**MINIT <R0>, Rb, Ra**
	Description	Initialize Multiply logic ready for multiply sequence. Clear R0. If value of Ra is zero or value of Rb is zero then set Z (to flag zero result) else clear Z.
	Operation	R0 = 0
	Flags	Z

11.18.22 MOV, Move Register to Register

This section describes the MOV instruction of the PCP.

MOV	Syntax	**MOV Rb, Ra, cc_A**
	Description	If condition CONDCA is true, then move the contents of register Ra into register Rb. If CONDCA is false, no operation is performed.
	Operation	if (CONDCA = True) then R[b] = R[a] else NOP
	Flags	N, Z

11.18.23 Multiply Instructions

This section describes the multiply instructions of the PCP.

MSTEP32	Syntax	**MSTEP32 <R0>, Rb, Ra**
	Description	Perform an unsigned multiply step, using eight bits of data taken from Rb, keeping the least significant 32 bits of a potential 64-bit result. Left rotate Rb by 8 bits. Shift R0 left by 8 bits. Add (Ra multiplied by the least significant 8 bits of Rb) to R0. If value of R0 is zero then set Z (to signal zero result) else clear Z.
	Operation	Rb = (Rb << 8) + (Rb >> 24) R0 = (R0 << 8) + (Rb & 0xff) × Ra
	Flags	Z
MSTEP64	Syntax	**MSTEP64 <R0>, Rb, Ra**
	Description	Perform an unsigned multiply step, using eight bits of data taken from Rb, keeping 40 bits of a potential 64-bit result. Add (Ra multiplied by the least significant 8 bits of Rb) to R0 and retain the 40 bit result (shown as temp below). Store the most significant 32 bits of the result (temp) in R0. Shift Rb right by 8 bits. Store the least significant 8 bits of the first result (temp) in the most significant 8 bits of Rb. If value of R0 is zero then set Z (to signal zero result) else clear Z.
	Operation	temp = R0 + Ra × (Rb & 0xff) R0 = temp >> 8 Rb = (Rb >> 8) + ((temp & 0xff) << 24)
	Flags	Z

Note: In the case of the MSTEP64 instruction above, the “temp” variable is a 40-bit variable and all calculations are performed using 40-bit unsigned arithmetic. All other calculations use 32-bit unsigned arithmetic.

11.18.24 NEG, Negate

This section describes the NEG instruction of the PCP.

NEG	Syntax	**NEG Rb, Ra, cc_A**
	Description	If condition CONDCA is true, then move the 2's complement of the contents of register Ra into register Rb. If CONDCA is false, no operation is performed.
	Operation	if (CONDCA = True) then R[b] = (- R[a]) else NOP
	Flags	N, Z, V, C

11.18.25 NOP, No Operation

This section describes the NOP instruction of the PCP.

NOP	Syntax	**NOP**
	Description	No operation. The NOP instruction puts the PCP in low-power operation.
	Operation	no operation
	Flags	None

11.18.26 NOT, Logical NOT

This section describes the NOT instruction of the PCP.

NOT	Syntax	**NOT Rb, Ra, cc_A**
	Description	If condition CONDCA is true, then move the 1's complement of the contents of register Ra into register Rb. If CONDCA is false, no operation is performed.
	Operation	if (CONDCA = True) then R[b] = NOT(R[a]) else NOP
	Flags	N, Z

11.18.27 OR, Logical OR

This section describes the OR instructions of the PCP.

OR	Syntax	**OR Rb, Ra, cc_A**
	Description	If the condition CONDCA is true, then perform a bit-wise logical OR of the contents of register Ra and the contents of register Rb; place the result in Rb. If CONDCA is false, no operation is performed.
	Operation	if (CONDCA = True) then R[b] = R[b] OR R[a] else NOP
	Flags	N, Z
OR.F	Syntax	**OR.F Rb, [Ra], Size**
	Description	Perform a bit-wise logical OR of the contents of the address location, specified by the contents of register Ra, and the contents of register Rb; place the result in Rb.
	Operation	R[b] = R[b] OR zero_ext(FPI[R[a]])
	Flags	N, Z
OR.PI	Syntax	**OR.PI Ra, [#offset6]**
	Description	Perform a bit-wise logical OR of the contents of the PRAM location specified by the addition of contents of the PRAM Data Pointer, shifted left by six bits, and the zero-extended 6-bit value offset6, and the contents of register Ra; place the result in Ra.
	Operation	R[a] = R[a] OR PRAM[(DPTR<<6) + zero_ext(#offset6)]
	Flags	N, Z

11.18.28 PRAM Bit Operations

This section describes the MCLR and MSET instructions of the PCP.

MCLR	Syntax	**MCLR.PI Ra, [#offset6]**
	Description	Perform an ‘AND’ of the contents of the specified register with the contents of the PRAM location specified by the addition of contents of the PRAM Data Pointer, shifted left by six bits, and the zero-extended 6-bit value offset. Write the result back to the PRAM location.
	Operation	R[a] = R[a].AND.PRAM[DPTR<<6 + #offset6] PRAM[DPTR<<6 + #offset6] = R[a]
	Flags	N, Z
MSET	Syntax	**MSET.PI Ra, [#offset6]**
	Description	Perform an ‘OR’ of the contents of the specified register with the contents of the PRAM location specified by the addition of contents of the PRAM Data Pointer, shifted left by six bits, and the zero-extended 6-bit value offset. Write the result back to the PRAM location.
	Operation	R[a] = R[a].OR.PRAM[DPTR<<6 + #offset6] PRAM[DPTR<<6 + #offset6] = R[a]
	Flags	N, Z

Note: MCLR and MSET are read/modify/write operations that cannot be interrupted by an access from another FPI master. They can be used to implement semaphore systems.

11.18.29 PRI, Prioritize

This section describes the PRI instruction of the PCP.

PRId	Syntax	**PRI Rb, Ra, cc_A**
	Description	If condition CONDCA is true, then find the bit position of the most significant 1 in register Ra and put the number into register Rb. The bit location, 31-0, is encoded as a 5-bit number stored in Rb[4:0]. If the contents of Ra is zero, bit Rb[5] is set, while all other bits in Rb are cleared. If CONDCA is false, no operation is performed.

	Operation	if (CONDCA = False) then
		NOP
		else
		if (R[a] = 0) then
		R[b] = 0x20
		else
		R[b] = bit_pos(most_significant_1(R[a]))

	Flags	N, Z

11.18.30 RL, Rotate Left

This section describes the RL instruction of the PCP.

RL	Syntax	**RL Ra, #imm5**
	Description	Rotate the contents of register Ra to the left by the number of bit positions specified through the 5-bit value imm5. The values defined for imm5 are 1, 2, 4 and 8. The carry flag, R7.C, is set to the last bit shifted out of bit 31 of register Ra.
	Operation	tmp = R[a] R[a] = R[a] << imm5; imm5 = 1, 2, 4, 8 R7_C = last bit shifted out of R[a] tmp = tmp >> 32 - imm5 R[a] = tmp OR R[a]
	Flags	N, Z

11.18.31 RR, Rotate Right

This section describes the RR instruction of the PCP.

RR	Syntax	**RR Ra, #imm5**
	Description	Rotate the contents of register Ra to the right by the number of bit positions specified through the 5-bit value imm5. The values allowed for imm5 are 1, 2, 4 and 8.
	Operation	tmp = R[a] R[a] = R[a] >> imm5; imm5 = 1, 2, 4, 8 tmp = tmp << 32 - imm5 R[a] = tmp OR R[a]
	Flags	N, Z

11.18.32 SET, Set Bit

This section describes the SET bit instruction of the PCP.

SET	Syntax	**SET Ra, #imm5**
	Description	Set bit imm5 of register Ra to 1.
	Operation	R[a][imm5] = 1
	Flags	None
SET.F	Syntax	**SET.F [Ra], #imm5, Size**
	Description	Set bit imm5 of the address location specified through the contents of register Ra to 1. This instruction is executed using a locked read-modify-write FPI Bus transaction.
	Operation	FPI[(R[a])][imm5] = 1
	Flags	None

11.18.33 SHL, Shift Left

This section describes the SHL instruction of the PCP.

SHL	Syntax	**SHL Ra, #imm5**
	Description	Shift the contents of register Ra to the left by the number of bit positions specified through the 5-bit value imm5. The values allowed for imm5 are 1, 2, 4 and 8. The carry flag, R7.C, is set to the last bit shifted out of bit 31 of register Ra. Zeros are shifted in from right.
	Operation	R[a] = R[a] << imm5; imm5 = 1, 2, 4, 8 R7_C = last bit shifted out of R[a]
	Flags	N, Z, C

11.18.34 SHR, Shift Right

This section describes the SHR instruction of the PCP.

SHR	Syntax	**SHR Ra, #imm5**
	Description	Shift the contents of register Ra to the right by the number of bit positions specified through the 5-bit value imm5. The values allowed for imm5 are 1, 2, 4 and 8. Zeros are shifted in from left.
	Operation	R[a] = R[a] >> imm5; imm5 = 1, 2, 4, 8
	Flags	N, Z

11.18.35 ST, Store

This section describes the ST instructions of the PCP.

ST.F	Syntax	**ST.F Rb, [Ra], Size**
	Description	Store the contents of register Rb to the address location specified by the contents of register Ra. When the Size is byte or half-word, the data is stored with the internal LSB (bit 0) properly aligned to the correct FPI Bus byte or half-word lane.
	Operation	FPI[R[a]] = R[b]
	Flags	None
ST.IF	Syntax	**ST.IF [Ra], #offset5, Size**
	Description	Store the contents of R0 to the address location specified by the addition of the contents of register Ra and the value specified by imm5. When the Size is byte or half-word, the data is stored with the internal LSB (bit 0) properly aligned to the correct FPI Bus byte or half-word lane.
	Operation	FPI[R[a] + zero_ext(imm5)] = R[0]
	Flags	None
ST.P	Syntax	**ST.P Rb, [Ra], cc_A**
	Description	If condition CONDCA is true, then store the contents of Rb to the PRAM address location specified by the addition of the contents of the PRAM Data Pointer, shifted left by six bits, and the zero-extended 6-bit value Ra[5:0]. If condition CONDCA is false, no operation is performed.
	Operation	if (CONDCA = True) then PRAM[(DPTR<<6) + zero_ext(R[a][5:0])] = R[b] else NOP
	Flags	None
ST.PI	Syntax	**ST.PI Rb, [#offset6]**
	Description	Store the contents of register Rb to the PRAM location specified by the addition of the contents of the PRAM Data Pointer, shifted left by six bits, and the zero-extended 6-bit value offset6.
	Operation	PRAM[(DPTR<<6) + zero_ext(offset6)] = R[b]
	Flags	None

11.18.36 SUB, 32-bit Subtract

This section describes the SUB instructions of the PCP.

SUB	Syntax	**SUB Rb, Ra, cc_A**
	Description	If the condition CONDCA is true, then subtract the contents of register Ra from the contents of register Rb; place the result in Rb. If CONDCA is false, no operation is performed.
	Operation	if (CONDCA = True) then R[b] = R[b] - R[a] else NOP
	Flags	N, Z, V, C
SUB.I	Syntax	**SUB.I Ra, #imm6**
	Description	Subtract the zero-extended immediate value imm6 from the contents of register Ra; place the result in Ra.
	Operation	R[a] = R[a] - zero_ext(imm6)
	Flags	N, Z, V, C
SUB.F	Syntax	**SUB.F Rb, [Ra], Size**
	Description	Subtract the zero-extended contents of the address location specified by the contents of register Ra from the contents of register Rb; place the result in Rb.
	Operation	R[b] = R[b] - zero_ext(FPI[R[a]])
	Flags	N, Z, V, C
SUB.PI	Syntax	**SUB.PI Ra, [#offset6]**
	Description	Subtract the contents of the PRAM location specified by the addition of contents of the PRAM Data Pointer, shifted left by six bits, and the zero-extended 6-bit value offset6 from the contents of register Ra; place the result in Ra.
	Operation	R[a] = R[a] - PRAM[(DPTR<<6) + zero_ext(#offset6)]
	Flags	N, Z, V, C

11.18.37 XCH, Exchange

This section describes the XCH instructions of the PCP.

XCH.F	Syntax	**XCH.F Rb, [Ra], Size**
	Description	Exchange contents of R[b] and FPI[R[a]] when Size is byte or half-word, the value is stored with the internal LSB (bit 0) properly aligned to the correct FPI byte or half-word lane. The exchange is done via a locked FPI bus transfer.
	Operation	temp = R[b] R[b] = zero_ext(FPI[R[a]]) FPI[R[a]] = temp
	Flags	N, Z
XCH.PI	Syntax	**XCH.PI Ra, [#offset6]**
	Description	Exchange contents of R[a] and PRAM[DPTR <<6 + #offset6]. *Note: The exchange is un-interruptible, and locks out external accesses; it will not be interrupted by any external FPI bus master transfer requests.*
	Operation	temp = R[a] R[a] = PRAM[(DPTR<<6) + zero_ext(#offset6)] PRAM[(DPTR<<6) + zero_ext(#offset6)] = temp
	Flags	N, Z

11.18.38 XOR, 32-bit Logical Exclusive OR

This section describes the XOR instructions of the PCP.

XOR	Syntax	**XOR Rb, Ra, cc_A**
	Description	If the condition CONDCA is true, then perform a bit-wise logical Exclusive-OR of the contents of register Ra and the contents of register Rb; place the result in Rb. If CONDCA is false, no operation is performed.
	Operation	if (CONDCA = True) then R[b] = R[b] XOR R[a] else NOP
	Flags	N, Z
XOR.F	Syntax	**XOR.F Rb, [Ra], Size**
	Description	Perform a bit-wise logical Exclusive-OR of the contents of the address location, specified by the contents of register Ra, and the contents of register Rb; place the result in Rb.
	Operation	R[b] = R[b] XOR zero_ext(FPI[R[a]])
	Flags	N, Z
XOR.PI	Syntax	**XOR.PI Ra, [#offset6]**
	Description	Perform a bit-wise logical Exclusive-OR of the contents of the PRAM location specified by the addition of contents of the PRAM Data Pointer, shifted left by six bits, and the zero-extended 6-bit value offset6, and the contents of register Ra; place the result in Ra.
	Operation	R[a] = R[a] XOR PRAM[(DPTR<<6) + zero_ext(#offset6)]
	Flags	N, Z

11.18.39 Flag Updates of Instructions

Most instructions update the state flags in R7. In **Table 11-15**, each instruction is shown with the flags that it updates.

Table 11-15 Flag Updates

Instruction	CN1Z	V	C	N	Z
ADD	–	yes	yes	yes	yes
AND	–	–	–	yes	yes
BCOPY	yes[1)]	–	–	–	–
CHKB	–	–	yes	–	–
CLR	–	–	–	–	–
COMP	–	yes	yes	yes	yes
COPY	yes[1)]	–	–	–	–
DEBUG	–	–	–	–	–
DINIT	–	yes	–	–	yes
DSTEP	–	–	–	–	yes
EXIT	yes[1)]	–	–	–	–
INB	–	–	–	–	–
JC	–	–	–	–	–
JL	–	–	–	–	–
LD	–	–	–	yes[2)]	yes
LDL	–	–	–	yes	yes
MCLR	–	–	–	yes	yes
MSET	–	–	–	yes	yes
MOV	–	–	–	yes	yes
NEG	–	yes	yes	yes	yes
NOP	–	–	–	–	–
NOT	–	–	–	yes	yes
OR	–	–	–	yes	yes
PRI	–	–	–	yes[3)]	yes
RR	–	–	–	yes	yes
RL	–	–	yes	yes	yes
SET	–	–	–	–	–

Table 11-15 Flag Updates (cont'd)

Instruction	CN1Z	V	C	N	Z
SHR	–	–	–	yes[3)]	yes
SHL	–	–	yes	yes	yes
ST	–	–	–	–	–
SUB	–	yes	yes	yes	yes
XCH	–	–	–	yes	yes
XOR	–	–	–	yes	yes

1) CN1Z is only modified by the BCOPY, COPY or EXIT instructions if the instruction has been configured to decrement R6.CNT1 (for BCOPY/COPY CNC = 1 or CNC = 2, for EXIT EC = 1). All other instructions have no effect on the CN1Z flag.

2) For the LD.I type of instruction, flag N is always cleared, as bit 31 of the result is always 0.

3) Flag N is always cleared, as bit 31 of the result is always 0.

11.18.40 Instruction Timing

This section gives some information about the duration of PCP instructions. Please note that there are various conditions that can further affect the duration of PCP instructions (e.g. external FPI accesses from another FPI Bus master to the PCP memories stall the PCP Processor Core).

*Note: The clock cycles listed in **Table 11-16** are PCP core clock cycles. When running in 2:1 clocking mode the maximum allowed PCP core clock frequency is 180 MHz (resulting in a minimum PCP core clock cycle time of 5.6ns). When running in 1:1 clocking mode the maximum PCP core clock frequency is the same as the maximum System Peripheral Bus frequency. In the TC1798 the System Peripheral Bus (which is an FPI Bus) is clocked with f_{FPI}, resulting in a minimum PCP core clock cycle time of 11.1ns (in 1:1 clocking mode).*

*Note: Where an execution time is stated for an FPI instruction this is always a **minimum** value. A number of FPI instructions must wait for the completion of an FPI transaction (or transactions). When running in 2:1 mode each FPI clock cycle consists of two core clock frequencies. Where this applies the cycle count is shown with an "FPI" superscript designation (e.g. "3^{FPI}"). In addition there may be an additional single core clock cycle taken according to alignment of execution of an FPI instruction relative to an FPI clock edge.*

Table 11-16 Instruction Timing

Instruction	Number of Clock Cycles	Comments	Notes
Control			
NOP	1	–	–

Table 11-16 Instruction Timing (cont'd)

Instruction	Number of Clock Cycles	Comments	Notes
COPY	–	–	1)
EXIT	f = 9, s = 7, m = 6	–	2)
BCOPY	–	–	1)
FPI Access			
ADD.F	8 min.	5 int. + 3^{FPI} min. for FPI read	3)
AND.F	8 min.	5 int. + 3^{FPI} min. for FPI read	3)
COMP.F	8 min.	5 int. + 3^{FPI} min. for FPI read	3)
LD.F	8 min.	5 int. + 3^{FPI} min. for FPI read	3)
OR.F	8 min.	5 int. + 3^{FPI} min. for FPI read	3)
ST.F	5 min.	2 int. + 3^{FPI} min. for FPI write	3)
SUB.F	8 min.	5 int. + 3^{FPI} min. for FPI read	3)
XCH.F	8 min.	4 int. + 4^{FPI} min. for FPI read and write	3)
XOR.F	8 min.	5 int. + 3^{FPI} min. for FPI read	3)
PRAM Access			
ADD.PI	2	–	–
AND.PI	2	–	–
COMP.PI	2	–	–
LD.PI	2	–	–
MCLR.PI	6	–	–
MSET.PI	6	–	–
OR.PI	2	–	–
ST.PI	4	–	–
SUB.PI	2	–	–
XCH.PI	5	–	–
XOR.PI	2	–	–
Arithmetic (Conditional)			
ADD	1	–	–
AND	1	–	–
COMP	1	–	–
INB	1	–	–

Table 11-16 Instruction Timing (cont'd)

Instruction	Number of Clock Cycles	Comments	Notes
LD.P	2	–	–
MOV	1	–	–
NEG	1	–	–
NOT	1	–	–
OR	1	–	–
PRI	1	–	–
ST.P	4	–	–
SUB	1	–	–
XOR	1	–	–
Immediate Access			
ADD.I	1	–	–
CHKB	1	–	–
CLR	1	–	–
COMP.I	1	–	–
INB.I	1	–	–
LD.I	1	–	–
LDL.IL	1	–	–
LDL.IU	1	–	–
RL	1	–	–
RR	1	–	–
SET	1	–	–
SHL	1	–	–
SHR	1	–	–
SUB.I	1	–	–
FPI + Immediate Access			
CLR.F	8 min.	4 int. + 4^{FPI} min. for locked FPI RMW (Read, Modify, Write)	4)
LD.IF	8 min.	5 int. + 3^{FPI} min. for FPI read	3)
SET.F	8 min.	4 int. + 4^{FPI} min. for locked FPI RMW (Read, Modify, Write)	4)
ST.IF	5 min.	2 int. + 3^{FPI} min. for FPI write	5)

Table 11-16 Instruction Timing (cont'd)

Instruction	Number of Clock Cycles	Comments	Notes
Complex Math			
DINIT	1	–	6)
DSTEP	10	–	6)
MINIT	1	–	7)
MSTEP.L	10	–	7)
MSTEP.U	11	–	7)
Jump			
DEBUG	sdb - 0 = 2 sdb - 1 = exit_time	–	8)
JC	y = 4, n = 2	–	9)
JC.A	y = 4, n = 2	–	8)
JC.I	y = 4, n = 2	–	8)
JC.IA	y = 4, n = 2	–	8)
JL	4	–	–

1) The number of clock cycles for these instructions depends on several parameters such as the amount of data to be copied, the type of memory, and the effective bus load.

2) f = Full Context save, s = Small Context save, m = Minimum Context save time extended until any previous ST.F instruction has completed.

3) Cycles = 5 internal + 3 minimum for FPI read (with 0 wait cycles + 1 cycle for bus arbitration and assuming 1:1 clocking mode)

4) Cycles = 4 internal + 4 minimum for FPI read/modify/write (with 0 wait cycles + 1 cycle bus arbitration and assuming 1:1 clocking mode)

5) Cycles = 2 internal + 3 minimum for FPI write (with 0 wait cycles + 1 cycle for bus arbitration and assuming 1:1 clocking mode)
Time starts after any previous ST.F instruction has completed.

6) 32/32 bit divide requires instruction DINIT + JC + 4 × DSTEP = 1 + 4(2) + 4 × 10 = 45 cycles
8/32 bit divide requires instruction RR + DINIT + JC + DSTEP = 1 + 1 + 4(2) + 10 = 16 cycles

7) 32 × 8 bit multiply requires instructions RR + MINIT + MSTEP.L = 1 + 1 + 10 = 12 cycles
32 × 16 bit multiply requires instructions 2 × RR + MINIT + 2 × MSTEP.L = 2 × 1 + 1 + 2 × 10 = 23 cycles
32 × 32 bit multiply requires instructions MINIT + 4 × MSTEP.U= 1 + 4 × 11 = 45 cycles

8) sdb - 0 = Stop_on_Debug bit in instruction = 0 (disabling stop)
sdb - 1 = Stop_on_Debug bit in instruction = 1 (enabling stop)
exit_time = same time as for an exit instruction

9) y = jump taken, n = jump not taken

11.19 Instruction Encoding

Most instructions are encoded in 16 bits.

This allows two instruction to be fetched out of 32 bit instruction memory per access.

For example, a COPY and an EXIT instruction can be fetched simultaneously, performing a simple DMA transaction.

Table 11-17 Field Definitions

Symbol	Name	Description
CNC	Counter Control	00: Perform the number/type of transfers appropriate to the instruction, and proceed to the next instruction. 01: Perform the number/type of transfers appropriate to the instruction, then decrement CNT1 and proceed to next instruction. 10: Use CNT1 as an “outer loop counter”. Perform the number/type of transfers appropriate to the instruction, then decrement CNT1. Repeat until CNT1 = 0, then proceed to next instruction. If R[7].IEN = True (interrupts enabled) the instruction may be interrupted at the end of each iteration of the “outer loop”. 11: N/A (error)
CNT0	Internal Loop Counter /Block Size Control	Internal Loop Counter for COPY: 000: Perform a sequence of 8 read/write transfers n: Perform a sequence of n (1 <= n <= 7) read/write transfers Block Size control for BCOPY: 000: 8 Words 001: N/A (error) 010: 2 Words 011: 4 Words 1xx: N/A (error)
CONDCA/B	Condition Code	Condition Code for conditional execution of instruction.
DAC	Disable All Channels Control	0: no action 1: Clear CS.EN which stops the PCP executing and further channel programs.
DST+/-	Destination Address Increment / Decrement	00: No Change 01: Post Increment by Size 10: Post Decrement by Size 11: N/A (error)

Table 11-17 Field Definitions (cont'd)

Symbol	Name	Description
EC	Exit Count Control	0: no action 1: decrement CNT1
EDA	External Debug Action	0: No External Debug Action caused 1: Cause an External Debug Action (breakpoint pin etc.)
EP	Entry Point	Entry Point on next Channel Invocation: 0: Set the PC to Channel Start 1: Set the PC to the address contained in NextPC (next instruction) address. Note: EP=0 assumes that a Channel Entry Table exists in the base of Code Memory. Failure to provide one will cause improper operation.
INT	Interrupt	Issue interrupt 0: No 1: Yes if (CONDCB = True)
RTA	Return to This Address	0: The channel is disabled (R7.CEN=0) and the PC value stored in the context is NextPC. 1: The channel remains enabled and the PC value stored in the context is NextPC - 1.
SDB	Stop on Debug	0: Continue running if Debug Event Triggered 1: Stop PCP Channel if Debug Event Triggered
Set/Clr	Set/Clear	0: Check for Clear (0) 1: Check for Set (1)
SIZE	Data Size	00: Byte (8-bit) 01: Half Word (16-bit) 10: Word (32-bit) 11: Reserved
SRC+/-	Source Address Increment / Decrement	00: No Change 01: Post Increment by Size 10: Post Decrement by Size 11: N/A (error)
ST	Stop Channel	0: Leave Channel enabled 1: Stop Channel from accepting new Service Requests (clear R[7].CEN)

Table 11-18 Instruction Encoding

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0 -:Control			**fmt**	**Instr**	**DST + -**		**SRC + -**		**CNC**		**CNT0**			**Size**	
NOP			0	0											
COPY			0	1											
					ST	**INT**	**EP**	**EC**	**-**		**-**	**CONDC B**			
EXIT			1	0								Condition for Interrupt			
			fmt	**Instr**	**DST + -**		**SRC + -**		**CNC**		**-**	**CNT0**		**-**	
BCOPY			1	1											

1 -:FPI	**Instruction**	**R[b]**	**R[a]**	**-**	**Size**
ADD.F	0				
SUB.F	1				
COMP.F	2				
error	3				
error	4				
AND.F	5				
error	6				
OR.F	7				
XOR.F	8				
LD.F	9				
ST.F	A				
XCH.F	B				
error	C				
error	D				
error	E				
error	F				

2 -:PRAM	**Instruction**	**R[a]**	**Offset 6 - bit**
ADD.PI	0		
SUB.PI	1		
COMP.PI	2		

Table 11-18 Instruction Encoding (cont'd)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
error			3												
MCLR.PI			4												
AND.PI			5												
MSET.PI			6												
OR.PI			7												
XOR.PI			8												
LD.PI			9												
ST.PI			A												
XCH.PI			B												
error			C												
error			D												
error			E												
error			F												
3 -:Arithmetic			**Instruction**				**R[b]**			**R[a]**			**CONDC A**		
ADD			0												
SUB			1												
COMP			2												
NEG			3												
NOT			4												
AND			5												
error			6												
OR			7												
XOR			8												
LD.P			9												
ST.P			A												
error			B												
MOV			C												
INB			D												
PRI			E												
error			F												

Table 11-18 Instruction Encoding (cont'd)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
4 - Immediate			**Instruction**				**R[a]**			**Immediate 6 - bit**					
SUB.I			1												
ADD.I			0												
COMP.I			2												
error			3												
SHR			4												
SHL			5												
RR			6												
RL			7												
LDL.IU			8							**following #imm16 instruction**					
LDL.IL			9							**following #imm16 instruction**					
SET			A												
CLR			B												
LD.I			C												
INB.I			D												
CHKB			E							S/C					
error			F												
5 -:FPI Immediate			**Instruction**			**Size1**	**R[a]**			**Size0**	**Immediate 5 - bit**				
error			0												
error			1												
error			2												
SET.F			3												
CLR.F			4												
LD.IF			5												
ST.IF			6												
error			7												
6 -:Complex Maths			**op2:Instruction**				**R[b]**			**R[a]**			**Reserved**		
DINIT			0												
DSTEP			1												

Table 11-18 Instruction Encoding (cont'd)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MINIT			2												
MSTEP.L			3												
MSTEP.U			4												
error			5												
error			6												
error			7												
error			8												
error			9												
error			A												
error			B												
error			C												
error			D												
error			E												
error			F												
7 -:JUMP			**op2:Instr**			**Offset 10 - bit**									
JL			0	0	0										
			op2:Instr			**CONDC B**				**Offset 6 - bit**					
JC			0	0	1										
JC.A			0	1	0					**Absolute Destination in next 16 bits**					
error			0	1	1										
			op2:Instr			**CONDCB**				**R[a]**			**-**	**-**	**-**
JC.I			1	0	0										
JC.IA			1	0	1										
error			1	1	0										
			op2:Instr			**CONDCB**				**-**	**-**	**DAC**	**RTA**	**EDA**	**SDB**
DEBUG			1	1	1										

11.20 Programming of the PCP

In this section, several techniques are outlined to help design channel programs. There are also examples on configuring a channel program's context.

11.20.1 Initial PC of a Channel Program

A channel program can begin operation at the Channel Entry Table location corresponding to the priority of the interrupt. This is much like an interrupt vector location for that channel in a traditional processor architecture. When the channel program is started, the PC is set to two-times the channel number (SRPN). Since the base of the Channel Entry Table is the bottom of the CMEM address range, and since each entry in the table is two instructions long, this address computation results in the first instruction of the channel program for that SRPN being fetched from memory for execution.

Alternately, the channel program can be made to begin executing at whatever address its restored context holds in R7.PC.

If PCP_CS.RCB = 1, then the channel program is forced to always start at its Channel Entry Table location regardless of the PC value stored in the CSA. If PCP_CS.RCB = 0, then the channel program will simply begin executing at whatever PC value is restored in the context R7.PC.

It is important to be aware of the implications of these two approaches on how CMEM should be configured, and what the initial value of the PC should be in the channel program's context that is loaded in the PRAM CSA at boot time.

11.20.1.1 Channel Entry Table

When PCP_CS.RCB = 1, the program counter of the PCP is vectored to the appropriate channel entry table each time a channel program is invoked by the receipt of an interrupt. The PCP is forced to start executing from its channel entry table location, regardless of its previous context or PC state.

If the EXIT instruction is executed with EP = 0, the PC saved during the context save operation will be the channel entry table location for that channel. That means that the next time the channel program is started, it will begin operation at the appropriate location in the Channel Entry Table.

Note: If EP = 0 is set in any channel program, or if PCP_CS.RCB = 1, a Channel Entry Table must be provided at the base of CMEM. Otherwise this table is not needed.

11.20.1.2 Channel Resume

When PCP_CS.RCB = 0, the program counter of the PCP is vectored to the address that is restored from the channel program's context. This means that before exiting, a channel program must itself arrange for where it will resume execution by configuring the value of its PC in its saved context so that it restarts at the desired location.

In this way, arbitrarily complex interrupt-driven state machines can be created as individual channel programs. Channel programs can be constructed that always start at their beginning, pick up where they left off, or pick up elsewhere, or have a mix of these approaches.

An example of a restarting channel program is shown below. Before exiting, the channel branches back to the address of the START label minus 1 (note that START - 1 = CH16) and then exits. This will leave the next value of the PC in the channel program's context as the address of the START label.

```
CH16:                              ;channel program 16
     EXIT EC=1 ST=0 INT=0 EP=1 cc_UC
                                   ;exit, no intr., leave PC @ next
START:                             ;nominal channel start address
     ST.IFbase #0x8 SIZE=32        ;output note from R0
     JC   CH16, cc_UC              ;loop back before exit
```

Note that when the channel program is originally configured by the programmer, the PC field in the R7 context of this channel program should also be set to the address of the START label.

Similarly, an interrupt-driven state machine can be created by exiting with the next PC value pointing to the start of the next state in a state machine implemented by the channel program. The next example below shows a program starting at the address to the STATE0 label. It proceeds after the first interrupt to STATE1 - 1, where the channel program is left ready for the next state, STATE1 in the state machine. After the next interrupt, it executes to address STATE2 - 1 and the channel program is left ready for the next state, STATE2. After another interrupt, it proceeds through STATE2. The channel program jumps back to START, which is STATE0 - 1. The state machine has gone through one cycle and it is ready to restart in STATE0.

```
;This program is intended to test the sequence of exit/operate
;just as if you were implementing an interrupt driven
;state machine.
;It requires a periodic sequence of interrupts.

START:
     EXIT EC=1,ST=0,INT=0,EP=1,cc_UC;begin exit
STATE0:
     COMP.I     R5,#0x0            ;compare to interrupt number
                                   ;it should be
```

```
      JC          ERROR,cc_NZ      ;jump to error routine
                                   ;if not correct
      ADD.I       R5,#0x1          ;increment state number
      EXIT EC=1,ST=0,INT=0,EP=1,cc_UC      ;begin exit
STATE1:
      COMP.I      R5,#0x1          ;compare to interrupt number
                                   ;it should be
      JC          ERROR,cc_NZ      ;jump to error routine
                                   ;if not correct
      ADD.I       R5,#0x1          ;increment state number
      EXIT EC=1,ST=0,INT=0,EP=1,cc_UC      ;begin exit
STATE2:
      COMP.I      R5,#0x2          ;compare to interrupt number
                                   ;it should be
      JC          ERROR,cc_NZ      ;jump to error routine if
                                   ;not correct
      LD.I        R5,#0x0          ;reset state number
      JC          START,cc_UC      ;jump back to start of
                                   ;state machine
```

The last state could just as easily have ended with an EXIT that resets the PC to the Channel Entry Table (EP = 0) rather than jumping back to START.

11.20.2 Channel Management for Small and Minimum Contexts

If Small or Minimum Contexts are being used, only some of the registers are saved and restored. The integrity of the GPRs that are **not** included in the context must be handled explicitly by channel programs, since these are not saved and restored with the context of the interrupted channel program.

Channel programs may still use all registers reliably. Channel programs can be so designed that they either ignore the values in unsaved registers, or use those registers to store constants that no channel program changes. Hence, they never need to be saved and restored. Alternately, channel programs can use these unused GPRs as temporary variables as long as the values of such registers cannot be corrupted by the interrupt of the channel program by a higher-priority channel (see **Page 11-151**).

11.20.3 Unused Registers as Global's or Constants

Registers R0 through R3 (for the Small Context Model), or R0 through R5 (for the Minimum Context Model) can be used to store constants such as addresses that are available to all channel programs. Hence, these registers hold global data, and no channel program is allowed to change them.

Since the GPRs of the PCP are not directly accessible from the FPI Bus, there does need to be an initial channel program that sets these values at or near boot time. There are

two choices here. A boot-time interrupt channel program can be invoked once to perform initialization, or there can be a program that routinely loads these values as a matter of course, and is invoked at boot time or as upon receipt of the very first interrupt.

11.20.4 Dispatch of Low Priority Tasks

A higher-priority channel program may wish to start a low-priority background task, or periodically pause and re-start itself later when there is no other action required at the moment. This can be accomplished in several ways:

- Post an SRPN to a free SRN on the FPI Bus, then EXIT.
- Perform an EXIT, posting the interrupt to the PCP, and indicating the channel number to be started.
- Use a single channel program as a list-driven or state-driven task dispatcher.

The first approach is straightforward to program, but uses a system SRN resource. Its advantage is that it allows continuous channel operation without using the interrupt queue, or risk blocking other uses of the PCP.

The second approach can be implemented by having a looping channel program continue operation in the background. It will also always be superseded by any higher-priority tasks.

The third approach uses a channel program to dispatch other non-interrupt-driven channel programs in an arbitrary order determined by the channel program dispatcher. In this way, multiple tasks could be continuously operated without over-using the PCP service-request queue. This approach would be useful when the aim is to poll for service requests in the peripheral SRNs rather than having them started by PCP hardware.

11.20.5 Code Reuse Across Channels (Call and Return)

A special jump instruction is included in the PCP instruction set to allow subroutines to be called from multiple channel programs. A routine may be jumped to directly, and then returned from using the JC.IA instruction. JC.IA allows a calling channel program to set aside a register for its return address, which will typically be the value of the next PC. The called subprogram can then execute a JC.IA, to the address stored in the register specified, causing a return-from-subroutine operation. The programmer must adopt and enforce a calling convention to determine which register holds the return address. Register R2 is normally used for this purpose.

For example:

```
Main Routine:                    Subroutine:
     LD.IL     R2,#RETURN            SUB:  MOV...
     JC.A      #SUB                        ADD...
RETURN: MOV    ...                         ...
     ...                                   JC.IA R2
```

11.20.6 Case-like Code Switches (Computed Go-To)

The JC.I instruction can be used to implement a multi-way branch for branch-on-bit or branch-on-state conditional branches. This instruction allows a conditional relative jump based on an index held in a register. If this instruction is combined with a table of jump addresses, a switch-type statement can be implemented. The default case, that is when the condition code = False, is the next instruction, as is the jump with register index = 0. The table can be any arbitrary length. The index register should be checked for range before the jump into the table is performed.

For Example:

```
           COMP  R3,#5      ;compare R3 to #5 - the number
                            ;of entries in the table
           JC.I  R3,cc_ULE
DEFAULT:   JL    #case_0    ;destination if R3 = 0 or
                            ;condition = false
           JL    #case_1    ;destination if R3 = 1
           JL    #case_2    ;destination if R3 = 2
           JL    #case_3    ;destination if R3 = 3
           JL    #case_4    ;destination if R3 = 4
           JL    #case_5    ;destination if R3 = 5
```

11.20.7 Simple DMA Operation

A simple interrupt-driven DMA requires at least the Small Context Model to operate properly. Its operation is consists of three stages:

- The device interrupts the PCP to indicate it can receive or provide data.
- The PCP moves the amount of data it is programmed to move.
- The PCP eventually finishes and interrupts the CPU to notify it that the DMA is complete.

There are two options for implementing a simple DMA operation, copy and burst copy.

11.20.7.1 COPY Instruction

A simple DMA channel program can consist of only two instructions. In the example below, a device interrupts the PCP to notify it that it has data in its output buffer, which is 4 words deep. The COPY instruction copies 4 words to memory at a time. It decrements CNT1 (which is initialized by the CPU in CR6_CNT1 context) after each 4 word transfer. The EXIT command then executes, and if CNT1 was decremented to 0, the condition code causes it to issue an interrupt with the value held R6_SRPN.

```
COPY  DST+,SRC,CNC=1,BRST=4,SIZE=32   ;do peripheral -> memory DMA
EXIT  EC=0,ST=0,INT=1,EP=0,cc_CNZ     ;transfer done, so exit
```

In the example above, the COPY instruction increments the destination held in R5 (DST+), and the source address is left constant in R4 (SRC). All permutations of decrement, increment or do not modify can be applied to either pointer register (R4 and R5) by use of the SRC and DST fields (SRC-, SRC+ or SRC and DST-, DST+ or DST).

Building on this basic DMA method, scatter-gather DMA channels can be created.

11.20.7.2 BCOPY Instruction (Burst Copy)

The BCOPY instruction is in principle similar to the COPY instruction except that it uses the FPI Burst mode to perform the transfers rather than performing individual reads/writes. As for the COPY instruction, the FPI Bus is locked between the burst read and burst write to ensure that a valid set of data is transferred. The BCOPY instruction allows support of all burst sizes supported by FPI Burst Mode except a burst size of 1 (i.e. 2, 4 or 8 words). The CNT0 field is used to control the burst size. Both the source and destination addresses (R4 and R5) must be correctly aligned for the burst size being used (see the FPI Bus description for details). If either address is incorrectly aligned, the PCP will generate an Illegal Operation Error Exit.

See also **Page 11-157** for TC1798 specific details of the BCOPY instruction.

11.21 PCP Programming Notes and Tips

This section discusses constraints on the use of the PCP and points out some non-obvious issues.

11.21.1 Notes on PCP Configuration

For configuring of the PCP, some notes should be regarded.

- Only one Context Model may be used at a time for all channels, and the PCP must remain in that Context Model once started and configured.
- In order for a specific channel program to be enabled, its context must have R7.CEN = 1. If R7.CEN = 0, the channel program will terminate when invoked, and cause a Disabled Channel Request error.
- The Channel Context Address from the FPI Bus as viewed during channel configuration is as follows:
- Full Context Model: PRAM Base + $20_H \times n$
- Small Context Model: PRAM Base + $10_H \times n$
- Minimum Context Model: PRAM Base + $08_H \times n$
  where n is the channel number.
- PCP_CS.RCB and context must be consistent. If RCB is configured to 0, then each channel program will start at the PC restored from its context. If the wrong address is pre-configured in the context, the channel program will not operate properly.
- The programmer of the PCP may lock PCP_CS by setting PCP_CS.EIE = 1. When the global ENDINIT bit is set, the PCP_CS register will no longer be writable, and attempting to do so will cause an FPI Bus error.
- An error condition will result in an interrupt being sent to the local FPI Bus master. The targeted interrupt service routine must be capable of dealing with the cause as recorded in PCP_ES, and, if required, it must be able to return the halted channel program to operation. The minimum required to do that is to set the context value of R7.CEN = 1.
- The only PCP Register bit that can be dynamically modified during PCP operation is the PCP_CS.EN bit. When writing to any other PCP Register bits, the user must ensure that the PCP is disabled (PCP_CS.EN = 0) and that the PCP is quiescent (PCP_CS.RS = 0).

11.21.2 General Purpose Register Use

When using the general purpose registers of the PCP, some notes should be regarded.

- The most significant 16 bits of R7 may not be written, and will always read back as 0. However, no error will occur if a write to the most significant 16 bits occurs.
- Care must be taken with the use of R6 as a general-use register to ensure that R6 contains the correct value prior to execution of the EXIT command. As R6 contains the CNT1 (counter used in COPY and optionally in EXIT instructions), SRPN and

TOS (service request number to use during optional interrupt at channel program EXIT) fields, R6 should not be used to pass values from one invocation of a channel program to the next invocation.

- If PRAM is to be accessed programmatically, then R7.DPTR must be configured properly as a pointer into the PRAM. This points to the 64-word segment that may be addressed by the xx.P instructions and the xx.PI instructions. It is not recommended to set R7.DTPR to point into the CSA. Special care must be taken that the Context PRAM is not overwritten.
- The programmer must be careful not to inadvertently clear R7.CEN when updating R7.DTPR (or any other field in R7). This would cause the channel program to generate a disabled channel interrupt to the CPU when the next interrupt request to the channel occurs.
- Any update to the Flags that is caused by an instruction (e.g. MOV R7, R0 which updates Z and N) takes precedence over any explicit bits that are moved to R7. See **Page 11-11**.
- The interrupt system assumes SRPN 0 is not a request. Full Context packing leaves the least significant 8 × 32-bit entries where channel 0 would normally be unused. That is, PRAM Base -> PRAM Base + 1 channel. In addition, for Small Context, the least significant 4 × 32-bit entries are unused, and for Minimum Context the least significant 2 × 32-bit entries are un-used. These “unused” entries should not be used by channel programs.
- If EP = 0 is used, or if PCP_CS.RCB = 1, a Channel Entry Table must be provided at the base of CMEM.
- If there is a plan to use the Small or Minimum Context Model, and the lower registers are to hold global values, then there needs to be an initial channel program that sets these values at or near boot time. There are at least two choices for implementing this. For instance, a boot interrupt channel program can be invoked once to perform initialization, or there can be a program that routinely loads these values as a matter of course, and it is invoked at boot time, or at the very first interrupt. See **Page 11-147**.
- When using Small or Minimum Context models and allowing a channel to be interrupted, care must be taken to ensure that the value of any registers that are not included in the context but are being used by a channel are not corrupted by interruption of the channel and subsequent operation of a higher-priority channel. Particular care must be taken when using instructions that use R0 implicitly. If necessary, critical instruction sequences should be protected by use of the R7.IEN bit (see **Page 11-153**).

11.21.3 Use of Channel Interruption

For channel interruption, the following note should be regarded.

- When a channel program consists of only a few instructions, it is best to configure the channel to be non-interruptible. This increases overall efficiency by removing the context save/restore overhead that would be incurred if the channel were to be interruptible.

11.21.3.1 Dynamic Interrupt Masking

A channel program can dynamically control whether it can be interrupted by use of the R7.IEN bit. When masking interrupts (by clearing R7.IEN), it must be noted that there is a delay of one instruction before the mask becomes effective. As a result the instruction that clears R7.IEN must be placed at least one instruction before the instruction sequence that is to be un-interruptible. As an example, consider the following sequence:

```
CLR   R7,IEN     ;Clear the R7.IEN bit
                 ;<< Interrupt can occur here
NOP
                 ;<< Interrupt can occur here
                 ;First instruction of non-interruptible
                 ;code sequence
```

11.21.3.2 Control of Channel Priority (CPPN)

The PCP has three extended Service Request Nodes (PCP_SRC9, PCP_SRC10 and PCP_SCR11) that allow storage of suspended channel interrupt requests. This allows interrupt nesting to a depth of four. This limit on the nesting depth carries the danger that a high-priority service request will not be serviced because the PCP's interrupt nesting depth has been exceeded.

It is recommended that a four-level "grouping" scheme should be adopted to avoid this problem. All PCP interrupt sources should be listed in order of their SRPNs.This list should then be subdivided into four contiguous groups, Group 0 being the lowest priority and Group 3 the highest. The CSA for each channel program should be configured such that CR6.CPPN contains the SRPN value of the highest channel program within the group to which the channel belongs. As each channel starts, the Operating Priority (CPPN) of the channel is loaded from the context. Using the scheme recommended above, any channel program will run with the priority of the highest SRPN within the group. As a result, the channel can only be interrupted by a service request from a higher-priority group (e.g. a Group 0 channel program can be interrupted by a new service request for a channel in any group from 1 to 3, a group 2 channel program can only be interrupted by a new service request for a channel in group 3).

Note: When using this scheme, each channel program must ensure prior to channel exit that the R6.CPPN field contains the appropriate value, so that when the channel is next invoked, it will run at the correct priority.

11.21.4 Implementing Divide Algorithms

As discussed in **Section 11.18.4**, a divide algorithm **must** always start with a DINIT instruction followed by a number of DSTEP instructions (up to four depending on the data width that is required). Prior to execution of any DSTEP instruction, R0 always contains either 0 (if this is the first DSTEP instruction in a divide sequence R0 contains 0 due to the preceding DINIT instruction, or the remainder from the previous DSTEP instruction). The dividend to be used in this step is generated in R0 by taking 256 × the remainder of the last DSTEP instruction (R0 << 8) and adding the most significant byte of Rb (Rb >> 24) as the LSB of the new dividend.

Since the remainder of the last DSTEP instruction is by definition always less than the divisor (Ra), it can be guaranteed that the result of the division of the dividend (calculated as above) by the divisor (Ra) can always be contained within an 8-bit result. The description given on **Page 11-114** only holds true under this condition. If the restrictions on the use of the DSTEP instruction (specified on **Page 11-105**) are adhered to, the above condition will always be met and this description of the instruction is correct. Failure to adhere to these conditions will lead to invalid results, which are outside the scope of this document.

During execution of a divide sequence, Rb is used both to compile the final divide result and to hold the remnants of the original dividend. For example, in a 32-/32-bit divide sequence (which consists of 4 DSTEP instructions - see below), Rb will have the following content:

- After the 1st DSTEP instruction:
  The least significant 3 bytes (24 bits) of the original 32-bit dividend (held in the most significant 3 bytes of Rb) and the most significant byte of the final result (held in the least significant byte of Rb).
- After the 2nd DSTEP instruction:
  The least significant 2 bytes (16 bits) of the original 32-bit dividend (held in the most significant 2 bytes of Rb) and the most significant 2 bytes of the final result (held in the least significant 2 bytes of Rb).
- After the 3rd DSTEP instruction:
  The least significant byte of the original 32-bit dividend (held in the most significant byte of Rb) and the most significant 3 bytes of the final result (held in the least significant 3 bytes of Rb).
- After the final DSTEP instruction:
  The 32 bit final result.

Note that the DSTEP instruction **always** uses the divisor as a 32 bit value. In any divide sequence, the dividend can be 8, 16, 24 or 32 bits (according to the number of DSTEP

instructions in the sequence) but the divisor is **always** 32 bits. Prior to the DINIT instruction, the dividend must always occupy the appropriate most significant bits within the 32-bit dividend register (Rb).

Divide Examples

Example of a 32/32 bit divide (R5 / R3):

```
DINIT     R5, R3     ;Initialize ready for the divide
JC        HANDLE_DIVIDE_BY_ZERO, cc_V     ;V flag was set
                     ;so jump to divide
                     ;by zero error handler
DSTEP     R5, R3     ;4 DSTEP instructions
                     ;(4 * 8 = 32 bit
DSTEP     R5, R3     ;divide)
DSTEP     R5, R3
DSTEP     R5, R3
```

After this sequence, R5 holds the result, R0 the remainder and R3 is unchanged.

Example of a 8/32 bit divide (R4 / R2):

```
RR        R4, 8      ;Rotate R4 right by 8 to move
                     ;least significant byte into
                     ;most significant byte
DINIT     R4, R2     ;Initialize ready for the divide
JC        HANDLE_DIVIDE_BY_ZERO, cc_V     ;V flag was set
                     ;so jump to divide
                     ;by zero error handler
DSTEP     R4, R2     ;DSTEP instruction
                     ;(1 * 8 = 8 bit divide)
```

After this sequence, R4 holds the result, R0 the remainder and R2 is unchanged.

Note that the above example is specified as being a 8/32 bit divide rather than an 8/8 bit divide (see comments above).

11.21.5 Implementing Multiply Algorithms

As discussed in **Section 11.18.4**, a multiply algorithm **must** always start with a MINIT instruction, followed by a number of MSTEP32 or MSTEP64 instructions. The MSTEP32 instruction is used to compile a multiplication result contained in 32 bits, discarding any overflows. The MSTEP64 instruction is used to compile a 64-bit multiplication result with the least significant 32 bits of the result contained in Rb and the most significant 32 bits of the result contained in R0.

Multiply Examples

Example of a 32 $\times$ 8 bit multiply (R4 $\times$ R1) yielding a 32 bit result (R4 = 32 bit, R1 = 8 bit):

```
RR        R1, 8      ;Rotate least significant byte of R1
                     ;to most significant byte
MINIT     R1, R4     ;Initialize ready for multiply
MSTEP32   R1, R4     ;Perform one MSTEP32 instruction
                     ;(8 bit multiply)
```

After this sequence, R0 holds the result, R1 is left unchanged (right rotated by RR instruction then left rotated by MSTEP32 instruction), and R4 is unchanged. The result is only valid if there is no overflow (i.e. the product of the 8-bit number in R1 multiplied by the 32-bit number in R4 can be contained within 32 bits). It is the user's responsibility to ensure that this is the case. The overflow condition cannot be detected after execution of the multiply sequence.

Example of a 32 × 16 bit multiply (R3 × R2) yielding a 32 bit result
(R3 = 32 bit, R2 = 16 bit):

```
RR        R2, 8      ;Perform two 8 bit rotations
                     ;(RR instructions) to get original
                     ;least significant 16 bits into
                     ;most significant 16 bits
RR        R2, 8
MINIT     R2, R3     ;Initialize ready for multiply
MSTEP32   R2, R3     ;Perform two MSTEP32 instructions
                     ;(16 bit multiply)
MSTEP32   R2, R3
```

After this sequence, R0 holds the result, R2 is left unchanged (right rotated by two RR instructions, then left rotated by two MSTEP32 instructions), R3 is unchanged. The comment above regarding overflow also applies to this sequence.

Example of a 32 × 32 bit multiply (R5 × R2) yielding a 64 bit result
(R5 = 32 bit, R2 = 32 bit):

```
MINIT     R2, R5     ;Initialize ready for multiply
MSTEP64   R2, R5     ;Perform 4 MSTEP64 instructions
                     ;(64-bit multiply)
MSTEP64   R2, R5
MSTEP64   R2, R5
MSTEP64   R2, R5
```

After this sequence R0 and R2 hold the result (most significant word in R0, least significant word in R2), R5 is unchanged. There is no possibility of overflow as the result of 32 × 32 bits can always be contained in 64 bits.

11.22 Implementation of the PCP in the TC1798

The addresses of the PCP registers and memories in the TC1798 are given in the following subsections:

11.22.1 PCP Memories

In the TC1798, the location of the registers and the memories sizes of the PRAM and the CMEM are given in **Table 11-19**.

Table 11-19 General Block Address Map

Unit		Address Range	Access Mode		Size
			Read	Write	
PCP	Reserved	$F004\ 0000_H$ - $F004\ 3EFF_H$	BE	BE	–
	PCP Registers	$F004\ 3F00_H$ - $F004\ 3FFF_H$	see **Page 11-67**		256 byte
	Reserved	$F004\ 4000_H$ - $F004\ FFFF_H$	BE	BE	–

Note: "BE" means that in case of an access to this address region a bus error is generated.

11.22.2 BCOPY Instruction

In the TC1798, the BCOPY instruction can be used to perform burst transfers (2, 4, or 8 words) with DMI memories (Local data RAM) and the PCP memories. Other internal and external memories can be accessed using a burst size of 2 words only (CNT0 = 10_B).

11.22.3 PCP Reset Operation

The PCP module can be reset by a system hardware signal (hard reset).

PCP Hard Reset

A PCP hard reset is always triggered if at least one of these TC1798 reset sources becomes active:

- Watchdog Timer Reset
- Hardware Reset
- Power-on Reset

Each of these reset sources forces a hardware reset of the functional blocks within the PCP module. The effect of hard reset within the PCP is to:

- Halt any operating channel
- Reset all control registers to their reset values
- Reset the PCP Processor Core to its default state
- Reset the FPI Bus interface

12 Direct Memory Access Controller (DMA)

This chapter describes the Direct Memory Access (DMA) Controller and the Memory Checker Module (MCHK) of the TC1798. It contains the following sections:

- Functional description of the DMA controller kernel (see **Section 12.2**)
- DMA controller module register description (see **Section 12.3**)
- TC1798 implementation-specific details of the DMA controller (interrupt control, address decoding, clock control, see **Section 12.4**)
- Functional description of the Memory Checker (MCHK) module (see **Section 12.5**)
- Memory Checker module register description (see **Section 12.5.2**)

*Note: The DMA kernel register names described in **Section 12.3** are referenced in the TC1798 User´s Manual by the module name prefix "DMA_".*

12.1 What is new

Major differences of the AudoMax DMA compared to AudoFuture:

- The AudoMax system architecture uses an SRI-XBAR in place of an LMB-BUS. The DMA LMB-Master is replaced by an SRI-Master.
- The LMB-Master 64-bit buffer to support read accesses to cached addresses (Segment 8) is replaced by an SRI-Master 256-bit buffer. In AudoFuture a Segment 8 read access was translated to a Single Data Transfer Double-Word (SDTD) access; in AudoMax it is translated to a 4-Transfer Block Transfer Request (BTR4) access.
- The access protection is extended from 32 to 64 fixed address ranges by the addition of a second Move Engine Access Enable Register. The number of programmable address range extensions is increased from 4 to 8 by the addition of a second Move Engine Access Range Register.

12.2 DMA Controller Kernel Description

The DMA Controller of the TC1798 transfers data from data source locations to data destination locations without intervention of the CPU or other on-chip devices. One data move operation is controlled by one DMA channel. Eight DMA channels are provided in one DMA Sub-Block. The Bus Switch provides the connection of the DMA Sub-Blocks to the two On Chip Bus interfaces and a DMA Peripheral interface. In the TC1798, the two On Chip Bus interfaces are connected to the System Peripheral Bus and the SRI Bus. The DMA Peripheral interface provides a connection to the Cerberus module, Micro Link Interface modules and other DMA-related devices (Memory Checker module in the TC1798). Clock control, address decoding, DMA request wiring, and DMA interrupt service request control are implementation-specific and are managed outside the DMA controller kernel.

The index “m” in the following block diagram refers to the DMA Sub-Block number (m = 0-1).

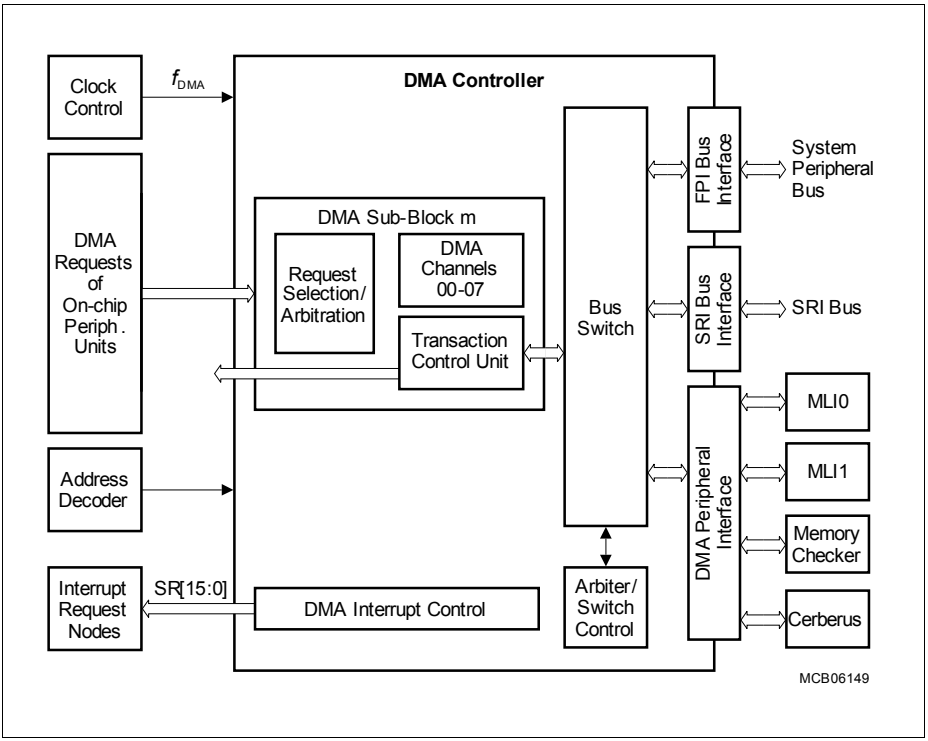


Figure 12-1 DMA Block Diagram

12.2.1 Features

The DMA controller is a fast and flexible DMA controller that has the following features:

- 16 independent DMA channels
  - 2 DMA Sub-Blocks with (8 DMA channels per DMA Sub-Block)
  - DMA Sub-Blocks with support of parallel channel execution (1 channel per Sub-Block, both Sub-Blocks in parallel)
  - Up to 16 selectable request inputs per DMA channel
  - 2-level programmable priority of DMA channels within the DMA Sub-Block
  - Software and hardware DMA request
  - Hardware requests by selected on-chip peripherals and external inputs
- 3-level programmable priority of the DMA Sub-Blocks on the chip bus interfaces
- Buffer capability for move actions on the buses (at least 1 move per bus is buffered)
- SRI Master Interface with 256-bit read buffer for read accesses to cached areas (Segment 8).
- Individually programmable operation modes for each DMA channel
  - Single Mode: stops and disables DMA channel after a predefined number of DMA transfers
  - Continuous Mode: DMA channel remains enabled after a predefined number of DMA transfers; DMA transaction can be repeated
  - Programmable address modification
  - Two shadow register modes (with / w/o automatic reset and direct write access).
- Full 32-bit addressing capability of each DMA channel
  - 4 Gbyte address range
  - Data block move > 32 Kbyte per DMA transaction
  - Circular buffer addressing mode with flexible circular buffer sizes
- Programmable data width of DMA transfer/transaction: 8-bit, 16-bit, or 32-bit
- Register set for each DMA channel
  - Source and destination address register
  - Channel control and status register
  - Transfer count register
- Flexible interrupt generation (the service request node logic for the MLI channels is also implemented in the DMA modules)
- DMA module is working on FPI frequency, SRI interface on SRI frequency.

Dependant on the target/destination address, Read/write requests from the Move Engines are directed to the FPI Bus, SRI Bus, MLIs or to the Cerberus module.

12.2.2 Definition of Terms

Some basic terms must be defined for the functional description of the DMA controller.

DMA Move

A DMA move is an operation that always consists of two parts:

1. A read move that loads data from a data source into the DMA controller
2. A write move that puts data from the DMA controller to a data destination

Within a DMA move, data is always moved from the data source via the DMA controller to the data destination. Data is temporarily stored in the DMA controller. The data widths of read move and write move are always identical (8-bit, 16-bit or 32-bit). Data assembly or disassembly is not supported.

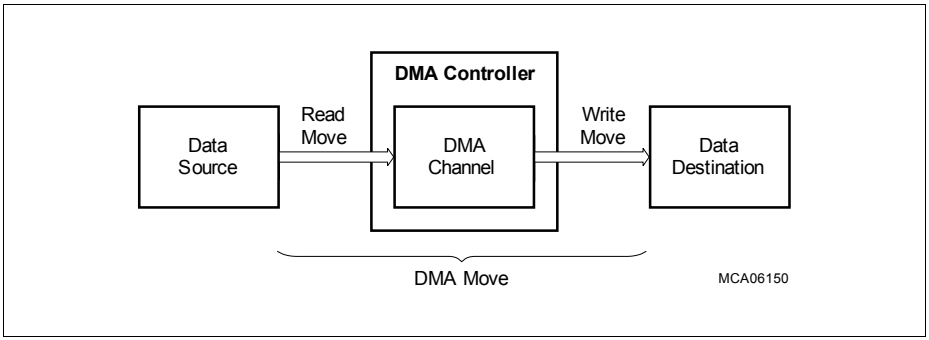


Figure 12-2 DMA Definition of Terms

DMA Transfer

A DMA transfer can be composed of 1, 2, 4, 8 or 16 DMA moves.

DMA Transaction

A DMA transaction is composed of several (at least one) DMA transfers. The Transfer Count determines the number of DMA transfers within one DMA transaction.

Example:
1024 word (32-bit wide) transactions can be composed of 256 transfers of four DMA word moves, or 128 transfers of eight DMA word moves.

12.2.3 DMA Principles

The DMA controller supports DMA moves from one address location to another one. DMA moves can be requested either by hardware or by software. DMA hardware requests are triggered by specific request lines from the peripheral modules or from other DMA channels (see **Figure 12-3**). The number of available DMA request lines from a peripheral module varies depending on the module functionality. Typically, the parallel occurrence of DMA requests and interrupts requests for DMA channels is possible. Therefore, the interrupt control unit and the DMA controller can react independently to interrupt and DMA requests that have been generated by one source.

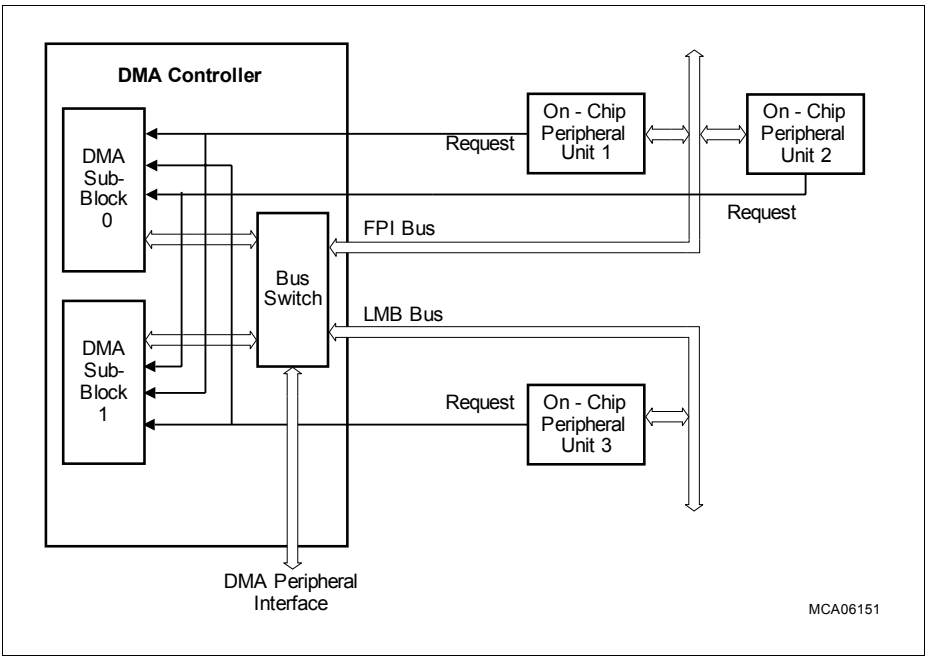


Figure 12-3 DMA Principle

The DMA controller mainly consists of two DMA Sub-Blocks and a Bus Switch. Once configured, the DMA Sub-Blocks are able to act as a master on the FPI Bus and on the SRI Bus.

12.2.4 DMA Channel Functionality

Each of the 16 DMA channels has one associated register set containing seven 32-bit registers. These registers are numbered by one index to indicate the related DMA Sub-Block and one index to indicate the related DMA channel: Index “m” refers to the DMA Sub-Block number (m = 0-1) and Index “n” refers to the channel number (n = 0-7) within the DMA Sub-Block.

Example: CHCR04 is the Control Register of DMA channel 4 in Sub-Block 0.

The register set of a DMA channel register contains the following registers:

- Channel mn Control Register CHCR0n (for details, see **Page 12-85**)
- Channel mn Status Register CHSR0n (for details, see **Page 12-89**)
- Channel mn Interrupt Control Register CHICR0n (for details, see **Page 12-90**)
- Channel mn Address Control Register ADRCR0n (for details, see **Page 12-92**)
- Channel mn Source Address Register SADR0n (for details, see **Page 12-97**)
- Channel mn Destination Address Register DADR0n (for details, see **Page 12-98**)
- Channel mn Shadow Address Register SHADR0n (for details, see **Page 12-99**)

12.2.4.1 Shadowed Source or Destination Address

As a typical application, an ASC module that receives data (fixed source address) has to deliver it to a memory buffer using a DMA transaction (variable destination address). After a certain amount of data has been transferred, a new DMA transaction should be initiated to deliver further ASC data into another memory buffer. While the destination address register is updated during a running DMA transaction with the actual destination address, a shadow mechanism allows programming of a new destination address without disturbing the content of the destination address register. In this case, the new destination address is written into a buffer register, i.e. the shadow address register. At the start of the next DMA transaction, the new address is transferred from this shadow address register to the destination address register without CPU intervention. This shadow mechanism avoids the CPU having to check for the end of a DMA transaction before reprogramming address registers.

The shadow address register can be used also to store a source address. However, it cannot store source and destination address at the same time. This means that the shadow mechanism makes it possible to automatically update either a new source address, or a new destination address at the start of a DMA transaction. If both address registers (for source and destination address) have to be updated for the next DMA transaction, a running DMA transaction for this channel must be finished. After that, source and destination address registers can be written before the next DMA transaction is started.

Figure 12-4 shows the actions that take place when a source address register is updated. The update of a destination register happens in an equivalent manner.

When writing a new address to the (address of) the source or destination address register and no DMA transaction is running, the new address value is directly written into the source or destination address register. In this case, no buffering of the address is required. When writing a new address to the (address of) the source or destination address register and a DMA transaction is running, no transfer to an address register can take place and SHADRmn holds the new address value that was written. For this operation, bit field ADRCRmn.SHCT must be set either to 01_B (address is a source address) or 10_B (new address is a destination address). At the start of the next DMA transaction, the shadow transfer takes place and the content of SHADRmn is written either into SADRmn or DADRmn (ADRCRmn.SHCT must be set accordingly). After the shadow transfer, SHADRmn is set to $0000\ 0000_H$ if the shadow register write enable bit is set to 0 (ADRCRmn.SHWEN = 0). In this case (ADRCRmn.SHWEN = 0), the software can check by reading the shadow address register whether or not the shadow transfer has already taken place.

Only one address register can be shadowed while a transaction is running, because the shadow register can only be assigned either to the source or to the destination address register. Note that the shadow address register transfer has the same behavior in Single and Continuous Mode. When the shadow mechanism is disabled (ADRCRmn.SHCT = 00_B), SHADRmn is always read as $0000\ 0000_H$.

If the shadow address register write enable bit is set to 1 (ADRCRmn.SHWEN = 1), the shadow register SHADRmn can be directly written. In this case (ADRCRmn.SHWEN = 1) the value stored in the SHADRmn is not modified when the shadow transfer takes place, and the shadow mechanism remains active and the shadow transfer will be repeated until Channel mn is reset or until the value in SHADR is $0000\ 0000_H$, is written into the shadow register (direct or indirect by writing to the source or destination address register according to the shadow control register ADRCRmn.SHCT).

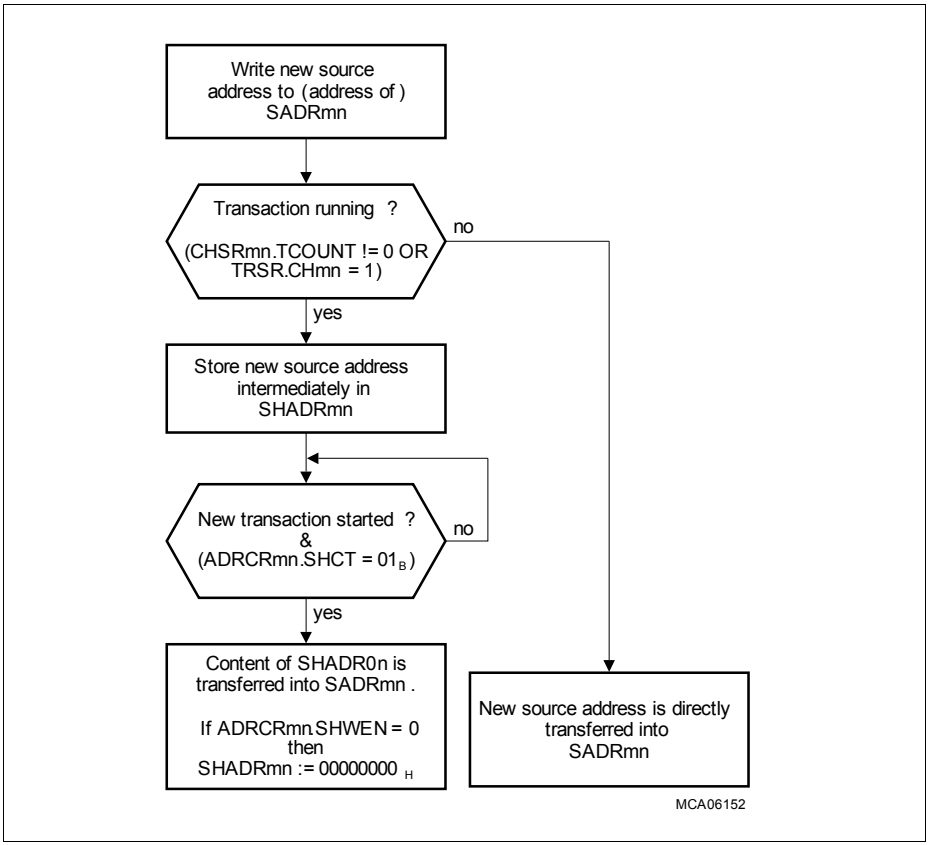


Figure 12-4 Source Address Update (m = 0-1)

The transfer count of a DMA transaction, stored in bit field CHCRmn.TREL, can also be programmed if the DMA transaction is running. At the start of a DMA transaction, TREL is transferred to bit field CHSRmn.TCOUNT, which is then updated during the DMA transaction.

No reload of address or counter will be done if TCOUNT is not equal to 0.

The reprogramming of channel specific values (except for the selected address shadow register) should be avoided while a DMA channel is active.

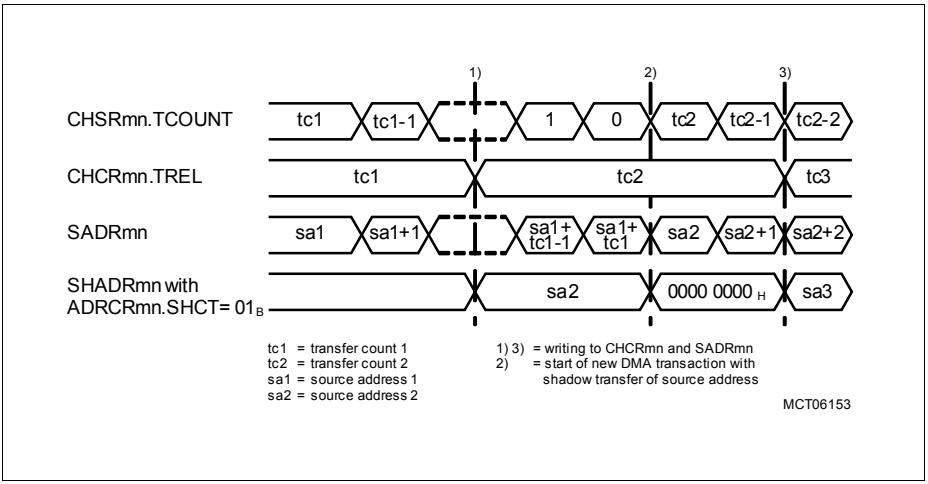


Figure 12-5 Shadow Source Address and Transfer Count Update with ADRCRmn.SHWEN = 0 (m = 0-1)

Figure 12-5 shows how the contents of the source address register SADRmn and the transfer count CHSRmn.TCOUNT are updated during two DMA transactions with a shadowed source address and transfer count update.

At reference point 2) the DMA transaction 1 is finished and DMA transaction 2 is started. At 1) the DMA channel is reprogrammed with two new parameters for the next DMA transaction: Transfer count tc2 and source address sa2. Source address sa2 is buffered in SADRmn and transferred to SADRmn when the new DMA transaction is started at 2). At this time, transfer count tc2 is also transferred to CHSRmn.TCOUNT. Note that the shadow address register is only reset by hardware to $0000\ 0000_H$ as shown in this example, if the write enable bit is set to 0 (ADRCRmn.SHWEN = 0).

12.2.4.2 DMA Channel Request Control

Figure 12-6 shows the control logic for DMA requests that is implemented for each DMA channel.

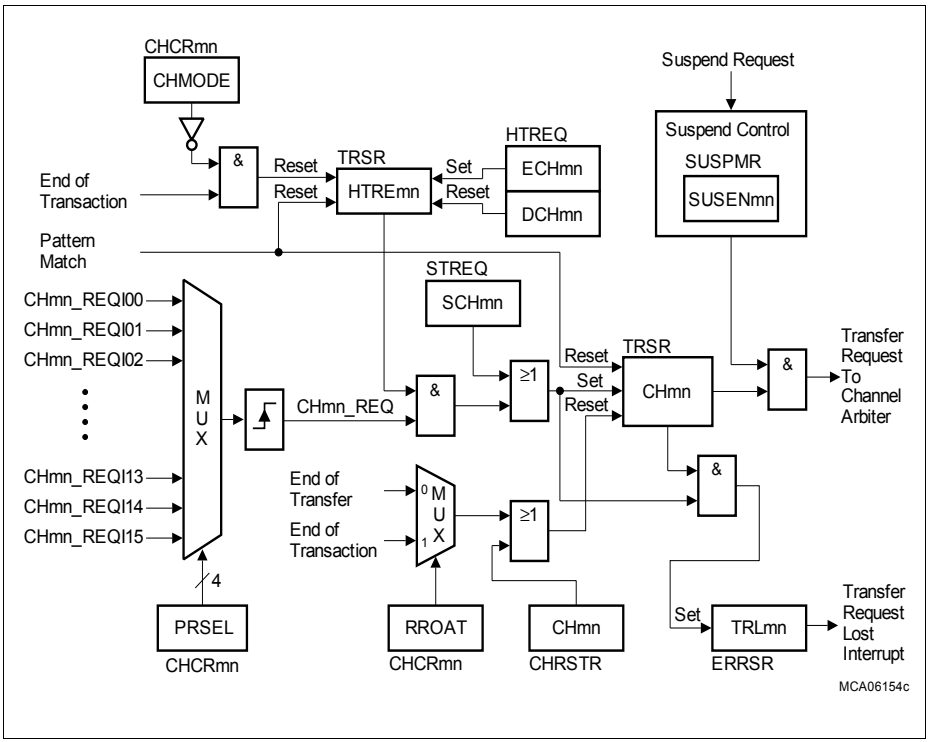


Figure 12-6 Channel Request Control (m = 0-1)

Two different types of DMA requests are possible:

- Hardware DMA requests
- Software DMA requests

The hardware request CHmn_REQ can be connected to one of sixteen possible hardware request input lines as selected by bit field CHCRmn.PRSEL. The hardware request input structure for CHCRmn.PRSEL includes a ´positive edge detector´ as the DMA channels requires single pulse requests.

Hardware requests are enabled/disabled by status bit TRSR.HTREmn. HTREmn can be set/reset by software or by hardware in Single Mode at the end of a DMA transaction. A software request can be generated by setting bit STREQ.SCHmn.

Status flag TRSR.CHmn indicates whether or not a software or hardware generated DMA request for DMA channel mn is pending. TRSR.CHmn can be reset by software or by hardware at the end of a DMA transfer (RROAT = 0) or at the end of a DMA transaction (RROAT = 1).

If a software or a hardware DMA request is detected for channel mn while TRSR.CHmn is set, a request lost event occurs. This error event indicates that the DMA is already processing a transfer and that another transfer has been requested before the end of the previous one. In this case, bit ERRSR.TRLmn will be set and a transfer lost interrupt can be generated.

12.2.4.3 DMA Channel Operation Modes

The operation mode of a DMA channel is individually programmable for each DMA channel mn. Basically, a DMA channel can operate in the following modes:

- Software controlled mode
- Hardware controlled mode, in Single or Continuous Mode

In software-controlled mode, a DMA channel request is generated by setting a control bit. In hardware-controlled mode, a DMA channel request is generated by request signals typically generated by on-chip peripheral units.

In hardware-controlled Single Mode, a DMA channel mn becomes disabled by hardware after the last DMA transfer of its DMA transaction. In hardware-controlled Continuous Mode, a DMA channel mn remains enabled after the last DMA transfer of its DMA transaction.

In hardware- and software-controlled mode, a DMA request signal can be configured to trigger a complete DMA transaction or one single transfer.

Software-controlled Modes

In software-controlled mode, one software request starts one complete DMA transaction or one single DMA transfer. Software-controlled modes are selected by writing HTREQ.DCHmn = 1. This forces status flag TRSR.HTREmn = 0 (hardware request of DMA channel mn is disabled).

The software-controlled mode that initiates one complete DMA transaction to be executed is selected for DMA channel mn by the following write operations:

- CHCRmn.RROAT = 1
- STREQ.SCHmn = 1

Setting STREQ.SCHmn to 1 (this is the software request) causes the DMA transaction of DMA channel mn to be started and TRSR.CHmn to be set. At the start of the DMA transaction, the value of CHCRmn.TREL is loaded into CHSRmn.TCOUNT (transfer count or tc) and the DMA transfers are executed. After each DMA transfer, TCOUNT becomes decremented and next source and destination addresses are calculated.

When TCOUNT reaches the 0, DMA channel mn becomes disabled and status flag TRSR.CHmn is reset. Setting STREQ.SCHmn again starts a new DMA transaction of DMA channel mn with the parameters as actually defined in the channel register set.

The software-controlled mode that initiates a single DMA transfer to be executed is selected for DMA channel mn by the following write operations:

- CHCRmn.RROAT = 0
- STREQ.SCHmn = 1, repeated for each DMA transfer

When CHCRmn.RROAT = 0, TRSR.CHmn becomes reset after each DMA transfer of the DMA transaction and a new software request (writing STREQ.SCHmn = 1) must be generated for starting the next DMA transfer.

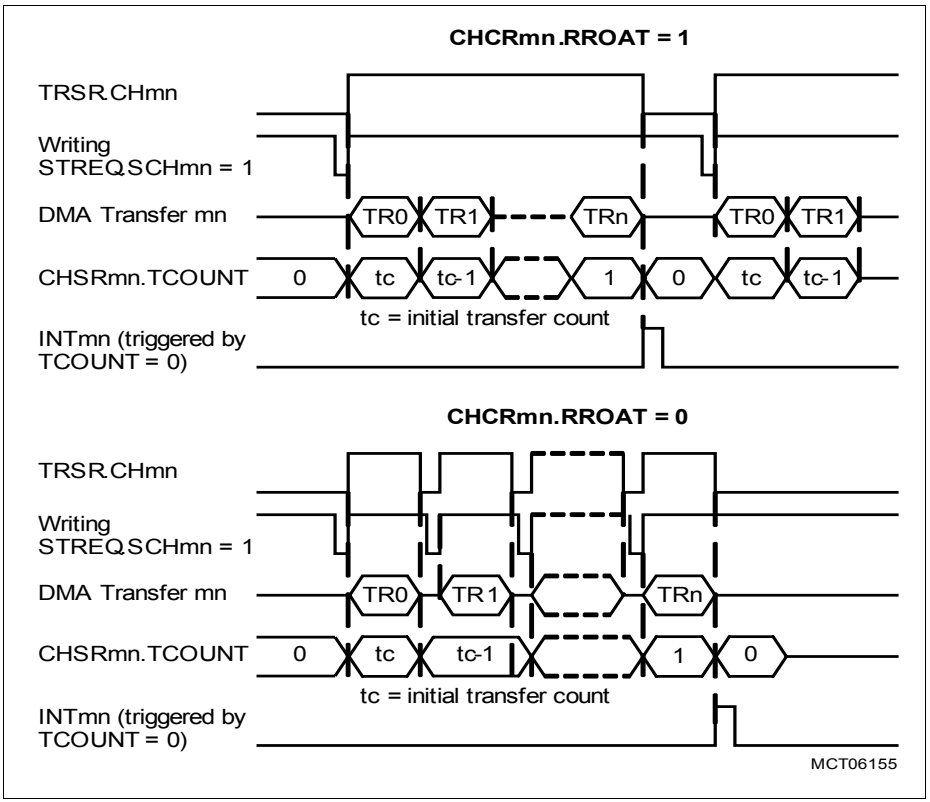


Figure 12-7 Software Controlled Mode Operation (m = 0-1)

Hardware-controlled Modes

In hardware-controlled modes, a hardware request signal starts a DMA transaction or a single DMA transfer. There are two hardware-controlled modes available:

- **Single Mode:**
  Hardware requests are disabled by hardware after a DMA transaction
- **Continuous Mode:**
  Hardware requests are not disabled by hardware after a DMA transaction

Hardware-controlled Single Mode

In hardware-controlled Single Modes, one hardware request starts one complete DMA transaction or one single DMA transfer. The hardware-controlled Single Mode that initiates one complete DMA transaction to be executed for DMA channel mn is selected by the following operations:

- CHCRmn.CHMODE = 0
- CHCRmn.RROAT = 1
- Selecting one of the sixteen hardware request inputs via CHCRmn.PRSEL
- HTREQ.ECHmn = 1

Setting HTREQ.ECHmn to 1 causes the hardware request CHmn_REQ of channel mn to be enabled (TRSR.HTREmn = 1). Whenever the hardware request CHmn_REQ becomes active, the value of CHCRmn.TREL is loaded into CHSRmn.TCOUNT and the DMA transaction is started by executing its first DMA transfer. After each DMA transfer, TCOUNT becomes decremented and next source and destination addresses are calculated. When TCOUNT reaches the 0, DMA channel 0n becomes disabled and status flags TRSR.CHmn and TRSR.HTREmn are reset. In order to start a new hardware-controlled DMA transaction, hardware requests must be enabled again by setting TRSR.HTREmn through HTREQ.ECHmn = 1. The hardware request disable function in Single Mode is typically needed when a reprogramming of the DMA channel register set (addresses, transfer count) is required before the next hardware triggered DMA transaction is started.

The hardware-controlled Single Mode in which each single DMA transfer has to be requested by a hardware request signal is selected as described above, with one difference:

- CHCRmn.RROAT = 0

In this operation mode, TRSR.CHmn becomes reset after each DMA transfer of the DMA transaction, and a new hardware request at CHmn_REQ must be generated for starting the next DMA transfer.

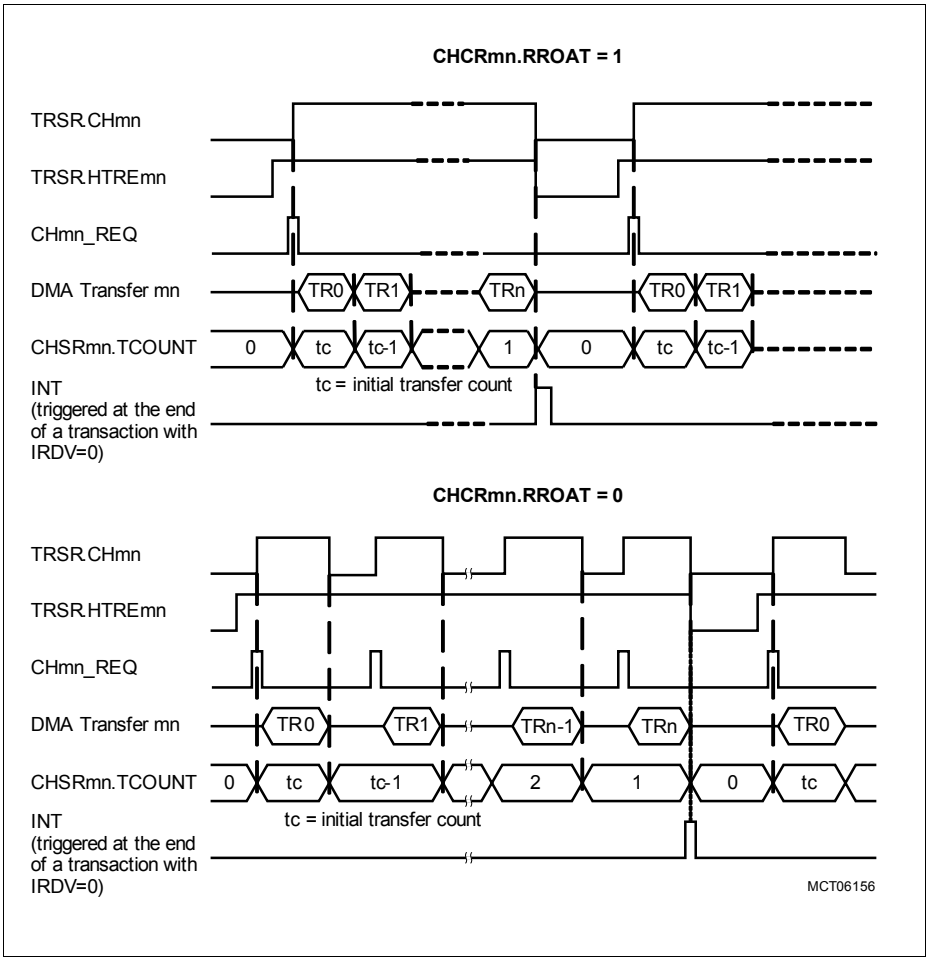


Figure 12-8 Hardware-controlled Single Mode Operation (m = 0-1)

Hardware-controlled Continuous Mode

In hardware-controlled Continuous Mode (CHCRmn.CHMODE = 1), the hardware transaction request enable bit HTREmn is not reset at the end of a DMA transaction. A new transaction of DMA channel mn with the parameters actually stored in the channel register set of DMA channel mn is started each time when CHSRmn.TCOUNT = 0 at the end of the DMA transaction. No software re-enable for a hardware request at CHmn_REQ is required.

Combined Software/Hardware-controlled Mode

Figure 12-9 shows how software- and hardware-controlled modes can be combined. In the example, the first DMA transfer is triggered by software when setting STREQ.SCHmn. Hardware requests are still disabled. After hardware requests have been enabled by setting HTREQ.ECHmn, subsequent DMA transfers are triggered now by hardware request coming from the CHmn_REQ line.

In the example, DMA channel mn operates in Single Mode (CHCRmn.CHMODE = 0). In this mode, TRSR.HTREmn becomes reset by hardware when CHSRmn.TCOUNT = 0 at the end of the DMA transaction.

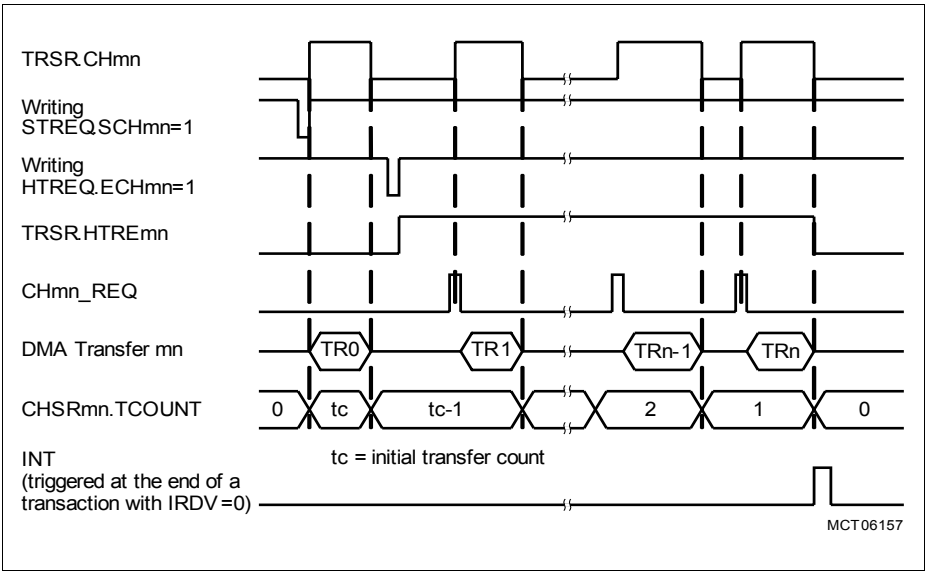


Figure 12-9 Transaction Start by Software, Continuation by Hardware (m = 0-1)

If a DMA channel is configured to be triggered by parallel hardware and software requests then if the requests collide in the same clock cycle then a Transaction/Transfer Request Lost event will be flagged in the DMA Error Status Register.

12.2.4.4 Error Conditions

The bus error flag ERRSR.FPIER indicates an FPI Bus error (SPB) that occurred during a source move (read or write) of a DMA module transaction. The bus error flag ERRSR.SRIER indicates an SRI Bus error that occurred during a source move (read or write) of a DMA module transaction.

The source error flags ERRSR.MEmSER indicates than an error occurred during source move (read) of a DMA transaction of DMA Sub-Block m.

The destination error flags ERRSR.MEmDER indicates than an error occurred during destination move (write) of a DMA transaction of DMA Sub-Block m
The transaction lost error flag ERRSR.TRLmn indicates if a DMA request for a DMA channel mn has been lost.

In the case of a read error, the write action is not executed, but the destination address is updated.

In the case of multiple errors, the error bits are set according to the error situations. This means that more than bus error flag can be set and that source/destination flags can be set.

12.2.4.5 Channel Reset Operation

A DMA transaction of DMA channel mn can be stopped (channel is reset) by setting bit CHRSTR.CHmn. When a read or write On Chip Bus transaction of DMA channel mn is executed at the time when CHRSTR.CH0n is set, this On Chip Bus transaction is finished normally. This behavior guarantees data consistency.

When CHRSTR.CHmn is set to 1:

- Bits TRSR.HTREmn, TRSR.CHmn, ERRSR.TRLmn, INTSR.ICHmn, INTSR.IPMmn, WRPSR.WRPDmn, WRPSR.WRPSmn, CHSRmn.LXO, and bit field CHSRmn.TCOUNT are reset.
- Source and destination address register will be set to the wrap boundary. SHADRmn will be cleared.
- All automatic functions are stopped for channel mn.

A user program must execute the following steps for resetting a DMA channel:

1. If hardware requests are enabled for the DMA channel mn, disable the DMA channel mn hardware requests by setting HTREQ.DCHmn = 1.
2. Writing a 1 to CHRSTR.CHmn.
3. Waiting (polling) until CHRSTR.CHmn = 0.

A user program should execute the following steps for restarting a DMA channel after it was reset:

1. Optionally (re-)configuring the address and other channel registers.
2. Restarting the DMA channel mn by setting HTREQ.ECHmn = 1 for hardware requests or STREQ.SCHmn = 1 for software requests.

The value of CHCRmn.TREL is copied to CHSRmn.TCOUNT when a new DMA transaction is requested and shadow address register contents is not equal $0000\ 0000_H$.

12.2.4.6 Transfer Count and Move Count

The move count determines the number of moves (consisting of one read and one write each) to be done in each transfer. It allows the user to indicate to the DMA the number of moves to be done after one request. The number of moves per transfer is selected by the block mode settings (CHCRmn.BLKM).

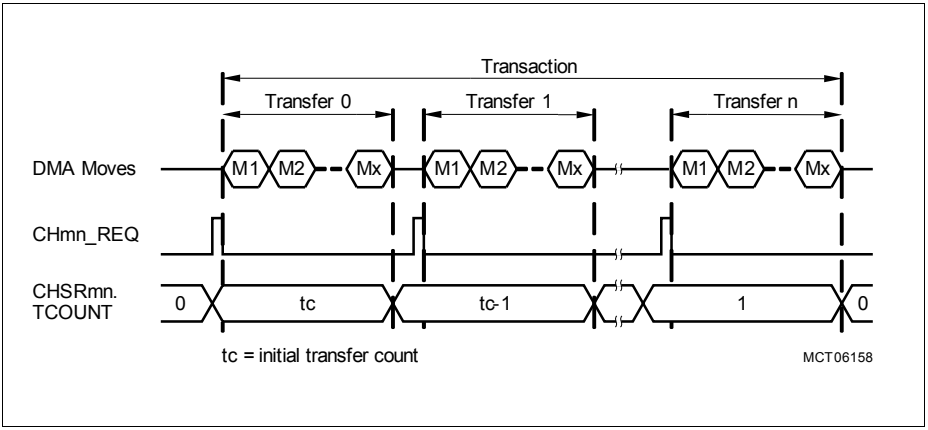


Figure 12-10 Transfer and Move Count (m = 0-1)

After a DMA move, the next source and destination addresses are calculated. Source and destination addresses are calculated independently of each other. The following address calculation parameters can be selected:

- The address offset, which is a multiple of the selected data width
- The offset direction: addition, subtraction, or none (unchanged address)

Control bits in address control register ADRCRmn determine how the addresses are incremented/decremented. Further, the data width as defined in CHCRmn.CHDW is taken into account for the address calculation.

Figure 12-11 and **Figure 12-12** show two examples of address calculation. In both examples, a data width of 16-bit (CHCRmn.CHDW = 01B) is assumed.

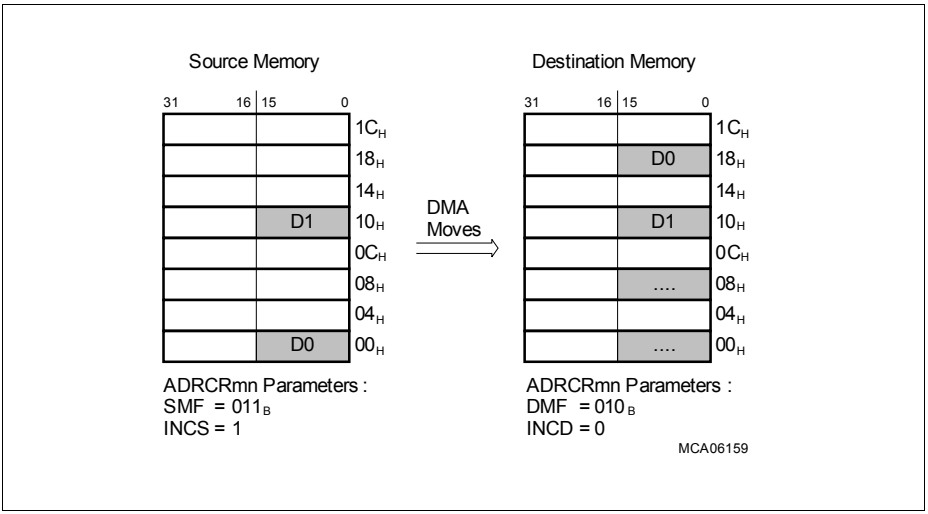


Figure 12-11 Programmable Address Modification - Example 1 (m = 0-1)

In **Figure 12-11**, 16-bit half-words are transferred from a source memory with an incrementing source address offset of 10_H to a destination memory with decrementing destination addresses offset of 08_H.

In **Figure 12-12**, 16-bit half-words are transferred from a source memory with an incrementing source address offset of 02_H to a destination memory with incrementing destination addresses offset of 04_H.

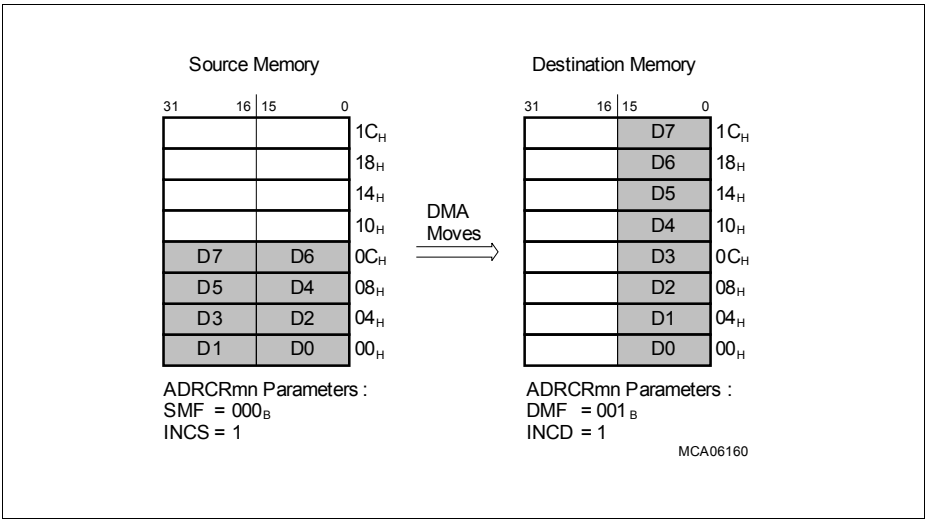


Figure 12-12 Programmable Address Modification - Example 2 (m = 0-1)

12.2.4.7 Circular Buffer

Destination and source address can be configured to build a circular buffer separately for source and destination data. Within this circular buffer, addresses are updated as defined in **Figure 12-11** and **Figure 12-12** with a wrap-around at the buffer limits. The circular buffer length is determined by bit fields ADRCRmn.CBLS (for the source buffer) and ADRCRmn.CBLD (for the destination buffer). These 4-bit wide bit fields determine which bits of the 32-bit address remain unchanged at an address update. Possible buffer sizes of the circular buffers can be 2^{CBLS} or 2^{CBLD} bytes (= 1, 2, 4, 8, 16, … up to 32k bytes).

When source or destination addresses are updated (incremented or decremented) after a DMA move, all upper bits [31:CBLS] of source address and [31:CBLD] of destination address are frozen and remain unchanged, even if a wrap-around from the lower address bits [CBLS:0] or [CBLD:0] occurred. This address-freezing mechanism always causes the circular buffers to be aligned to a multiple integer value of its size.

If the circular buffer size is less or equal than the selected address offset (see **Figure 12-9**), the same circular buffer address will always be accessed.

12.2.5 Transaction Control Engine

Each DMA Sub-Block has a Transaction Control Unit. The Transaction Control Unit in the DMA Sub-Block, as shown in the DMA Controller block diagram in **Figure 12-1**, contains a Channel Arbiter and a Move Engine.

The Channel Arbiter arbitrates the transfer requests of the DMA channels, and submits the transfers parameters of the DMA channel with the highest channel priority that are needed for a DMA transfer to the Move Engine. DMA channels within a DMA Sub-Block have a two-level programmable channel priority as defined by bit CHCRmn.CHPRIO. When two transfer requests of two different DMA channels with identical channel priority become active at the same time, the DMA channel with the lowest channel number (n) is serviced first.

The Move Engine handles the execution of a DMA transfer that has been detected by the Channel Arbiter to be the next one. The Move Engine requests the required buses and loads or stores data according to the parameters of a DMA transfer. It is able to wait if a targeted bus is not available. In the Move Engine, a DMA transfer of a DMA transaction cannot be interrupted and always get finished. This means that a DMA transfer, which can also be composed of several data moves (read move and write move), cannot be interrupted by a transfer of another DMA channel.

After a DMA transfer is finished, the Move Engine will send back the actualized address register information to the related DMA channel. Possible error conditions are also reported.

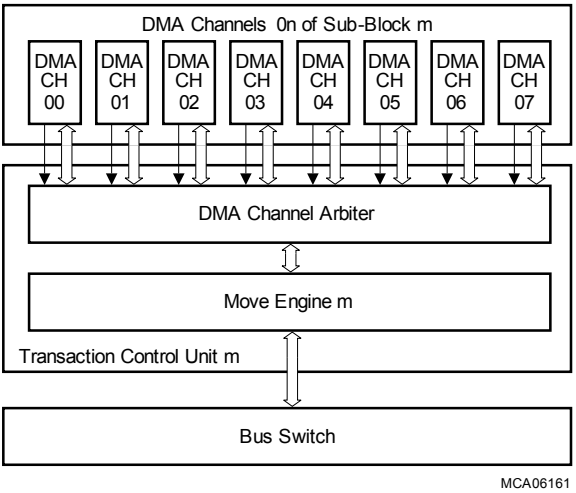


Figure 12-13 Transaction Control Engine (m = 0-1)

12.2.6 Bus Switch, Bus Switch Priorities

The Bus Switch of the DMA controller provides the connection from the DMA Sub-Blocks to the two On Chip Bus master interfaces (connected to System Peripheral Bus and SRI Bus) and to the DMA Peripheral Interface (see **Figure 12-14**).

The FPI Bus interface of the DMA includes a slave interface which provides the access to the DMA and the peripherals connected to the DMA Peripheral Interface (MLI, Cerberus and Memory Checker modules).

The SRI Bus interface of the DMA is a master interface.

The DMA module, the DMA Sub-Blocks as well as the MLI, the Memory Checker and the Cerberus module working frequencies are identical to the FPI Bus frequency. The working frequency of the SRI master interface is identical to the SRI/CPU working frequency.

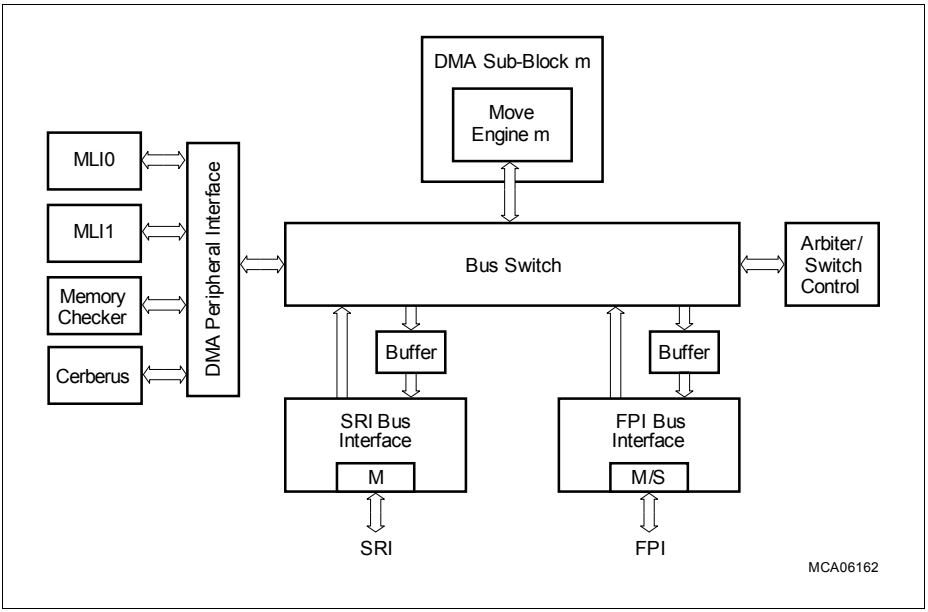


Figure 12-14 Bus Switch

One access can be buffered in the bus interfaces.

Note: The accesses of the DMA Move Engine's bus interfaces to the On Chip Bus interfaces are always done in Supervisor Mode.

The arbiter/switch control unit arbitrates the requests from the connected active interfaces (FPI Bus Interface, DMA Move Engines, MLIs, Cerberus,...) and grants the buses connected to the switch for data transfers. **Table 12-1** and **Table 12-2** define the Bus Switch priorities for requests to the same On Chip Bus Interface. The arbitration scheme is valid in case of a collision of requests from active peripherals connected to the DMA Bus Switch (Move Engine, MLIs, Cerberus) for the same resource (FPI Bus Interface, SRI Bus Interface, DMA Peripheral Interface, Move Engine). The arbitration is done for each Bus Switch request.

The general overview of the Bus Switch Priorities is given in **Table 12-1**. Additional detailed information about the Move Engine priorities for concurrent accesses on the Bus Switch is described in **Table 12-2**.

In case of a collision of the DMA Move Engine requests on the DMA Bus switch for the the same resource, a Move Engine Write has priority over a Move Engine Read. In case of a collision of both Move Engines with concurrent read requests or concurrent write requests for the same resource, the Move Engine number together with the

CHCRmn.DMAPRIO value determines the priority on the DMA Bus Switch (see Table 12-2).

Table 12-1 DMA Bus Switch Priorities

Priority	Agent Requests	Comment
Highest	Cerberus to On Chip Bus High	Priority selection by software in Cerberus.
	FPI Bus to DMA Peripheral Interface accesses	Reason: minimizing wait states on the FPI Bus.
	DMA Move Engine Write	The detailed Bus Switch priorities for the two Engines with concurrent reads or concurrent writes are listed in Table 12-2.
	DMA Move Engine Read	The detailed Bus Switch priorities for the two Engines with concurrent reads or concurrent writes are listed in Table 12-2.
	MLI0 access	–
	MLI1 access	–
Lowest	Cerberus to On Chip Bus Low	Priority selection by software in Cerberus.

Table 12-2 DMA Bus Switch Priorities of DMA Move Engines

Priority	DMA Move Engine Request	Comment
Highest	Move Engine 0 CHCR0x.DMAPRIO = “11” or CHCR0x.DMAPRIO = “01”	(x=7-0). x reflects the channel of Move 0 that won the Move Engine internal arbitration.
	Move Engine 1 CHCR1y.DMAPRIO = “11” or CHCR1y.DMAPRIO = “01”	(y=7-0). y reflects the channel of Move 1 that won the Move Engine internal arbitration.
	Move Engine 0 CHCR0x.DMAPRIO = “00”	(x=7-0). x reflects the channel of Move 0 that won the Move Engine internal arbitration.
Lowest	Move Engine 1 CHCR1x.DMAPRIO = “00”	(y=7-0). y reflects the channel of Move 1 that won the Move Engine internal arbitration.

12.2.7 DMA Module Priorities on On Chip Busses (FPI Bus, SRI Bus)

Every active peripheral connected to the DMA Bus Switch that requests for access to FPI Bus or SRI Bus has to go through two arbitration stages before accessing the On Chip

Bus: DMA Module internal arbitration at the DMA Bus Switch and DMA Module external arbitration at the On Chip Bus.

The DMA Module is connected to the FPI Bus and to the SRI Bus with master interfaces. The DMA SRI Master and the DMA FPI Master is each connected with three priorities to its On Chip Bus (low, medium and high priority), where it competes against the other bus masters connected to the On Chip Bus for bus access. The mapping of the Move Engines and the peripherals connected to the DMA Peripheral Interface to the DMA Module priorities on the FPI Bus and on the SRI Bus is described in **Table 12-3**.

The MLI modules are mapped to the low priority On Chip Bus requests of the DMA Module, while the mapping of the Cerberus and the Move Engines to the On Chip Bus requests is selected by software (control register bits).

The complete list of FPI master priorities can be found in the FPI Bus Control Unit Chapter.

The complete list of SRI master priorities can be found in the Shared Resource Interconnect Chapter.

Table 12-3 DMA Module Priorities on On Chip Busses

On Chip Bus Priority	DMA On Chip Bus Request	Comment
High	Cerberus High	Priority selection by SW in Cerberus.
	Move Engine m: CHCRmx.DMAPRIO = “11”	Priority selection by SW in Move Engine. (x=7-0) (m=1-0)
Medium	Move Engine m: CHCRmx.DMAPRIO = “01”	Priority selection by SW in Move Engine. (x=7-0) (m=1-0)
Low	Move Engine m: CHCRmx.DMAPRIO = “00”	Priority selection by SW in Move Engine. (x=7-0) (m=1-0)
	MLI0	-
	MLI1	-
	Cerberus Low	Priority selection by SW in Cerberus.

12.2.8 DMA Module: On Chip Bus Access Rights, RMW support

All accesses triggered by the DMA Move Engines, the MLI modules or the Cerberus module are always done in SV mode.

The DMA module does not support read/modify write instructions to the peripherals connected to the DMA Peripheral Interface (the MLI, Memory Checker and Cerberus modules).

12.2.9 DMA Module On Chip Bus Master Interfaces

This chapter describes the features of the DMA On Chip Bus Master Interfaces to the FPI Bus and to the SRI Bus.

The DMA FPI master interface supports:

- single data read and write transactions (8bit, 16bit, 32bit)
- generation of pipe lined FPI transactions from different sources (Move Engines, Cerberus, MLI´s)
- de-assertion of request after retry in order to prevent bus blocking.
- out of order transactions from different sources in order to avoid side effects (blocking) between the different sources (Move Engines, Cerberus, MLI´s)
- three dedicated FPI requests (medium, low, high priority. See **Table 12-3**)[1].

A single move engine supports only one transaction at a time. Due to the fact that the move engines do generate read - write sequences, it is unlikely that the DMA module generates permanent, pipeline, high priority requests.

The DMA SRI master interface supports:

- single data read and write transactions (8bit, 16bit, 32bit)
- 4-Transfer Burst Transfer (BTR4) for read accesses to Segment 8 (cached area)
- pipeline transactions from different sources (Move Engines, Cerberus, MLI´s)
- de-assertion of request after retry in order to prevent bus blocking.
- out of order transactions from different sources in order to avoid side effects (blocking) between the different sources (Move Engines, Cerberus, MLI´s)
- three dedicated SRI requests (medium, low, high priority. See **Table 12-3**)[2].

A single move engine supports only one transaction at a time. Due to the fact that the move engines do generate read - write sequences, it is unlikely that the DMA module generates permanent, pipeline, high priority requests.

DMA SRI Master Read Buffer:

The DMA SRI master interface includes a 256bit buffer for read accesses to cached addresses (Segment 8). The DMA SRI Master Interface contains a data read buffer for read accesses to cached addresses. The read buffer allows to read four double words (=256 bit) of data read from specific memory areas on SRI side (Segment 8: $8000\ 0000_H$ - $8FFF\ FFFF_H$)

A read request to an Segment 8 address (8bit, 16bit or 32bit) will be translated by the DMA SRI master interface into an SRI 4-Transfer Block Transfer Request. The DMA SRI master will forward the requested 8bit, 16bit or 32bit data to the DMA Bus switch and

1) The complete list of FPI master priorities can be found in the FPI Bus Control Unit Chapter.

2) The complete list of SRI master priorities can be found in the Shared Resource Interconnect Chapter.

save the 256bit read data together with the related 64bit aligned address in the DMA SRI master read buffer. If the next and subsequent read access to a segment 8 address is identical (64bit aligned) to the actual read buffer contents, the requested read data will be read from the read buffer by the DMA SRI master instead of reading it from the SRI bus.

If the next read to a read from a segment 8 address is not identical (64bit aligned) to the actual read buffer contents, the contents of the read buffer is invalidated. A 4-Transfer Block Transfer Request SRI read is generated by the DMA SRI master interface, the requested 8bit, 16bit or 32 bit data is forwarded to the DMA Bus switch and the read buffer is updated with the new 256bit data and its related address.

A DMA write to a segment 8 address (8bit, 16bit, 32bit write, 64bit write is not supported) invalidates the read buffer.

12.2.10 DMA Module Bridge Functionality

The DMA module includes bridge functionality:

- from the FPI Bus to the DMA Peripheral Interface
- from the DMA Peripheral Interface to the FPI Bus and SRI Bus.

FPI Bus -> SRI Bus

The DMA module does not forward transaction from the FPI Bus to the SRI Bus. The DMA module does not support / include bridge functionality between FPI Bus and SRI Bus.

FPI Bus -> DMA Peripheral Interface (MLI, Memory Check, Cerberus,...)

The DMA module forwards transactions from the FPI bus to the DMA Peripheral Interface (FPI -> MLI, Memory Check, Cerberus,...). The identification of the target module on the DMA Peripheral Interface is done by address decoding.

DMA Peripheral Interface -> On Chip Bus (FPI Bus, SRI Bus)

The DMA module forwards transactions from the active modules that are connected to the DMA Peripheral Interface (Cerberus, MLI,...) to the FPI Bus and SRI Bus. The identification of the target On Chip Bus is done by address decoding.

12.2.11 On-Chip Debug Capabilities

The DMA controller in the TC1798 provides some debugging capabilities. These debug features support:

- Soft-suspend Mode of DMA channels
- Break signal generation
- Trace signal generation

In Soft-suspend mode, the operations of DMA channels are stopped. Pending read or write transfers in the DMA module On Chip Bus Master Interfaces (SRI Master Interface, FPI Master Interface) are finished. Under certain conditions also a break signal is generated for the on-chip debug support logic. Further, DMA trace information can be output.

In Soft-suspend mode, the DMA module provides access to all control registers of the DMA module (inc. Move Engines and Memory Checker Module) and to the peripherals connected to the DMA Peripheral Interface.

12.2.11.1 Hard-suspend Mode

The Hard-Suspend Mode is controlled in the TC1798 DMA module CLC register but should not be used in order to guarantee access to the device via JTAG (Cerberus). Possible support of the Hard-suspend mode by the peripherals connected to the DMA Peripheral Interface is described in the related module chapters.

12.2.11.2 Soft-suspend Mode

The TC1798 on-chip debug control unit is able to generate a Soft-suspend Mode request (SUSREQ) for the DMA controller. When this soft-suspend request becomes active, the state of a DMA channel becomes frozen regarding hardware changes to ensure that the state of the DMA channels can be analyzed by reading the register contents. Pending read or write transfers in the DMA module On Chip Bus Master Interfaces (SRI Master Interface, FPI Master Interface) are finished. The DMA controller signals its soft suspend mode back to the on-chip debug control via an Soft-suspend acknowledge. The Soft-suspend acknowledge becomes active when all DMA channels mn that are enabled for the Soft-suspend Mode have set its suspend active status flag SUSPMR.SUSACmn.

Soft-suspend Mode of DMA channel mn is entered if its suspend enable bit SUSENmn in the Suspend Mode Register SUSPMR is set. When SUSREQ becomes active, the operation of all DMA channels mn that are enabled for Soft-suspend Mode is stopped automatically after its current DMA transfers have been finished in the transaction control unit. Afterwards, the suspend active status flag SUSPMR.SUSACmn is set, indicating that DMA channel mn is in Soft-suspend Mode. DMA channels that are disabled for Suspend Mode (SUSENmn = 0) continue with its normal operation.

In Soft-suspend Mode, register contents can be modified. These modifications are taken into account for further DMA transactions or DMA transfers of the related DMA channel

after Suspend Mode has been left again. Suspend Mode of DMA channel mn is left and its normal operation continues if either the SUSREQ signal becomes inactive, or if the enable bit SUSENmn is reset by software.

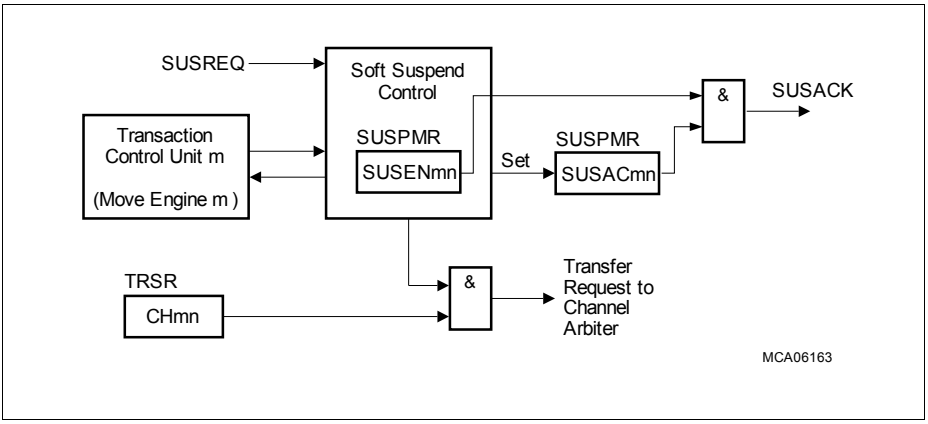


Figure 12-15 Soft-suspend Mode Control (m = 0-1)

12.2.11.3 Break Signal Generation

The DMA controller provides one BREAK output signal that is generated for the on-chip debug support logic (see **Figure 12-16**). The DMA sub-block is able to detect two break conditions:

- Transaction lost interrupt has occurred
- DMA request transitions, indicated by bits TRSR.CHmn

The output lines of the two break conditions in the DMA sub-block are OR-ed together to the BREAK output signal.

A transaction lost break condition occurs in DMA Sub-Block m whenever at least one of its eight transaction lost interrupts becomes active, and when enable bit OCDSR.BRL0 is set. The transaction lost interrupts do not generate a break condition if OCDSR.BRL0 = 0. Transaction interrupt control is described in **Section 12.2.12.2**.

The second break condition of DMA Sub-Block m becomes active when the transaction request bit TRSR.CHmn of one of its eight DMA channels n (as selected by OCDSR.BCHSn) indicates a transition of its state. The CHmn transition type (change from ´no request is pending´ to ´request is pending´, change from ´request is pending´ to ´no request is pending´, changes in both directions) is selected by bit field OCDSR.BTCRn.

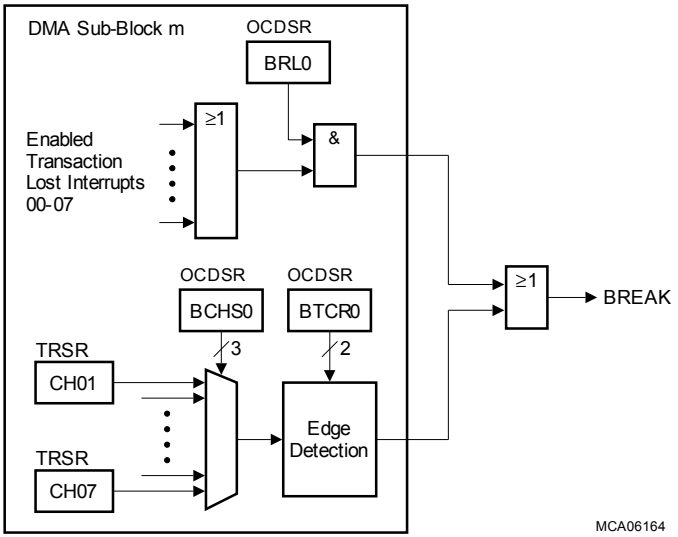


Figure 12-16 DMA Break Event Generation (m = 0-1)

12.2.12 Interrupts

The interrupt structure of the DMA controller is a very flexible control logic that allows an interrupt coming from an interrupt source within four interrupt source types to be connected to each of the sixteen interrupt outputs. This permits, for example, DMA channels that very rarely generate interrupts to share one interrupt node. The remaining interrupt nodes can be assigned to dedicated DMA channels to reduce the interrupt overhead for these channels. The four interrupt source types are:

- Channel interrupts
- Transaction lost interrupt
- Move Engine interrupts
- Wrap buffer interrupts

Some of the interrupt functions are common to all of the four interrupt source types. An interrupt event, internally generated as a request pulse, is always stored in an interrupt status flag. This interrupt status flag can be reset by software. Further, the interrupt event can be enabled or disabled. When an interrupt event is enabled, a 4-bit Interrupt Node Pointer determines which of the sixteen interrupt outputs will be activated.

The following sections describe each of the four interrupt source types in more detail.

12.2.12.1 Channel Interrupts

Each DMA channel mn has one associated channel interrupt. It can always be activated after a DMA transfer, or when CHSRmn.TCOUNT matches with the value of bit field CHICRmn.IRDV after it has been decremented after a DMA transfer. The pattern detection interrupts that are combined with the channel interrupts (one common Interrupt Node Pointer CHICRmn.INTP) are activated when the pattern detection interrupt of DMA channel mn becomes active (when enabled by CHCRmn.PATSEL not equal 00_B).

A channel interrupt of DMA channel mn is indicated when status flag INTSR.ICHmn is set. The status flags ICHmn and IPMmn can be reset together by software when setting bit INTCR.CICHmn (or CHRSTR.CHmn). The channel interrupt of DMA channel mn is enabled when bit CHICRmn.INTCT[1] is set. The channel interrupt pointer CHICRmn.INTP determines which of the interrupt outputs SR[15:0][1)] will be activated on an active channel interrupt or pattern detection interrupt. Note that the signal that is set signal for the ICHmn flag is available as CHmn_OUT signal at the DMA module boundary.

Bit CHICRmn.INTCT[0] selects these two types of interrupt sources. For the compare operation, bit field IRDV (4-bit) is zero-extended to 10-bit and then compared with the 10-bit TCOUNT value. This means that a TCOUNT match interrupt can be generated after one of the last 16 DMA transfers of a DMA transaction. Note that with

1) In the TC1798, only SR[7:0] are connected to interrupt nodes. SR[8:15] are used for DMA channel triggering/connections.

IRDV = 0000_B, the match interrupt is generated at the end of a DMA transaction (after the last DMA transfer).

The pattern detection interrupt is indicated when status flag INTSR.IPMmn is set. The status flags IPMmn and ICHmn can be reset together by software when setting bit INTCR.CICHmn (or CHRSTR.CHmn). The pattern detection interrupt of DMA channel mn is enabled when bit CHCRmn.PATSEL is set to a value not equal to 00_B. The channel interrupt pointer CHICRmn.INTP defines which of the interrupt outputs SR[15:0] will be activated on a pattern detection interrupt or the channel interrupt pointer CHICRmn.INTP determines which of the interrupt outputs SR[15:0][1] will be activated on a pattern detection or channel interrupt.

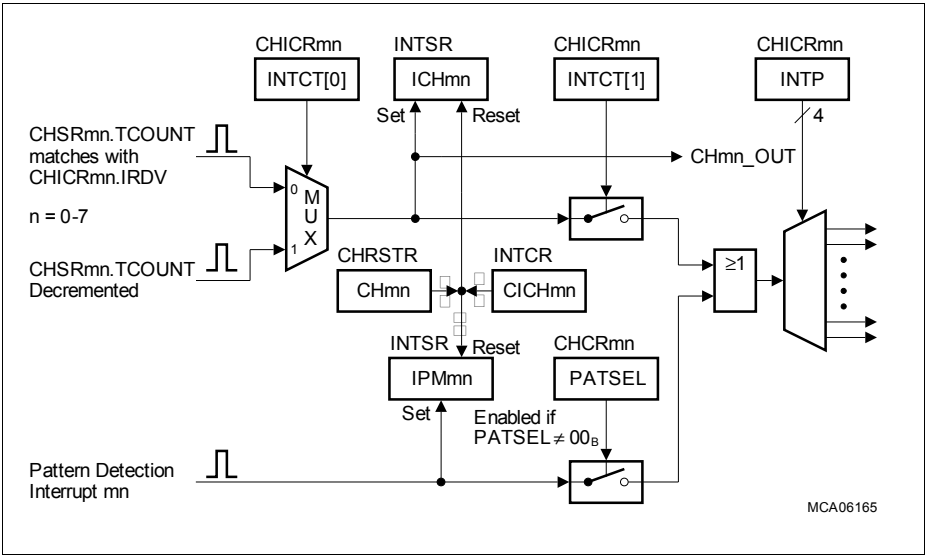


Figure 12-17 Channel Interrupts (m = 0-1)

1) In the TC1798, SR[7:0] are connected to interrupt nodes. SR[8:15] are used for DMA channel triggering/connections.

12.2.12.2 Transaction Lost Interrupt

Each DMA channel mn is able to detect a transaction request lost condition. This condition becomes true when a new hardware or software DMA request occurs while the previous transaction or transfer on DMA channel mn is not finished, indicated by TRSR.CHmn still set. If such a transaction request lost condition occurs, bit ERRSR.TRLmn is set. The transaction lost interrupts of all DMA channels are OR-ed together to one common transaction lost interrupt that can be directed to one of the interrupt outputs SR[15:0][1] by setting the transaction lost interrupt pointer EER.TRLINP with a corresponding value.

A transaction request lost condition of DMA channel mn is indicated by status flag ERRSR.TRLmn, which can be reset by setting bit CLRE.CTLmn or CHRSTR.CHmn. The transaction lost interrupt for DMA channel mn is enabled when bit EER.ETRLmn is set.

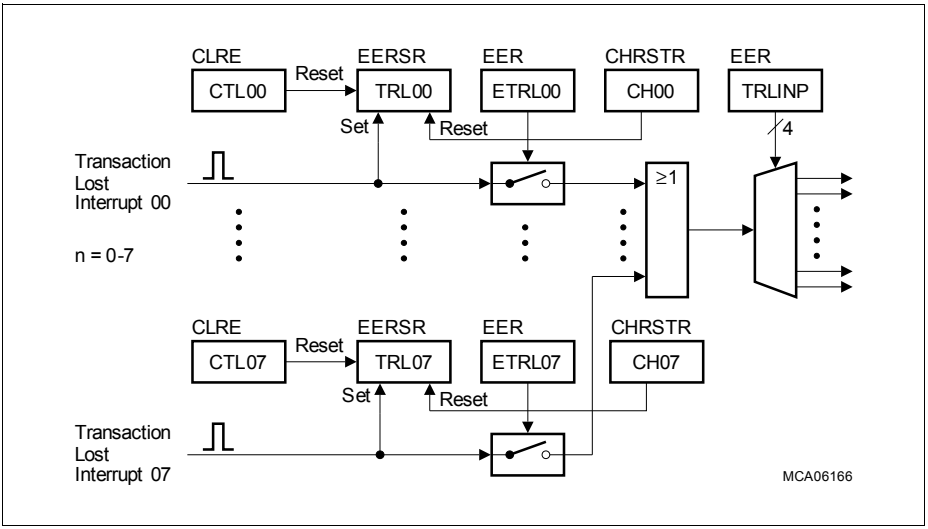


Figure 12-18 Transaction Lost Interrupt

1) In the TC1798 SR[7:0] are connected to interrupt nodes. SR[15:8] are used as DMA channel trigger signals.

12.2.12.3 Move Engine Interrupts

The Move Engine is able to detect error conditions that occur during accesses to the FPI Bus and SRI Bus interfaces of the Bus Switch (see **Figure 12-14**). Two error conditions can be detected:

- Source error
- Destination error

A source error indicates an FPI Bus or SRI Bus error that occurred during a read move from the data source. A destination error indicates an FPI Bus or SRI Bus error that occurred during a write move to the data destination.

A source error of Move Engine 0 is indicated by the status flag ERRSR.ME0SER. Status flag ME0SER can be reset by software when setting bit CLRE.CME0SER. The source error interrupt of Move Engine 0 is enabled when bit EER.EME0SER is set. Separate reset, status, and enable bits are available in the Move Engines for source error condition, as well as for destination error condition. The Move Engine's interrupts can be directed to one of the interrupt outputs SR[15:0][1] by setting the Move Engine interrupt pointer EER.ME0INP with a corresponding value.

Note that in case of a read move error, the write move is not executed but the destination address is updated.

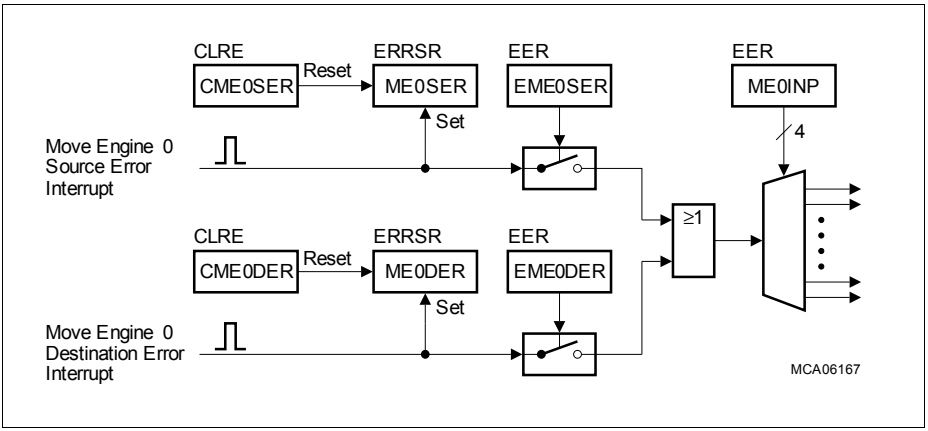


Figure 12-19 Move Engine Interrupts

1) In the TC1798 SR[7:0] are connected to interrupt nodes. SR[15:8] are used as DMA channel trigger signals.

When a Move Engine 0 source or destination error occurs, additional status bits and bit fields are provided in the error status register ERRSR to indicate the following two status conditions:

- At which On Chip Bus interface a Move Engine 0 error occurred (FPI or SRI)
- For which DMA channel a Move Engine 0 read or write move error was reported (LECME0)

These error status bits and bit fields are required by error handler software to detect in detail at which On Chip Bus interface and DMA channel the Move Engine error has been generated. ERRSR.FPIER or ERRSR.SRIER is reset when bits CLRE.CFPI0ER or CLRE.CFPI1ER is respectively set.

12.2.12.4 Wrap Buffer Interrupts

Each DMA channel mn is able to generate a wrap buffer interrupt for source buffer or destination buffer overflow. Further details on the pattern detection are described in **Section 12.2.13**.

A wrap source buffer interrupt of DMA channel mn is indicated by status flag WRPSR.WRPSmn. A wrap destination buffer interrupt of DMA channel mn is indicated by the status flag WRPSR.WRPDmn. Both interrupt status flags can be reset by software when bit INTCR.CWRPmn (or CHRSTR.CHmn becomes set). The wrap source buffer interrupt is enabled when bit CHICRmn.WRPSE is set. The wrap destination buffer interrupt is enabled when bit CHICRmn.WRPDE is set. The two interrupts for wrap source buffer and wrap destination buffer are OR-ed together to one common wrap buffer interrupt of DMA channel mn that can be directed to one of the interrupt outputs SR[15:0][1] by setting the wrap buffer interrupt pointer CHICRmn.WRPP with a corresponding value. Note that the pattern match should not be enabled while a wrap interrupt is enabled for the same channel.

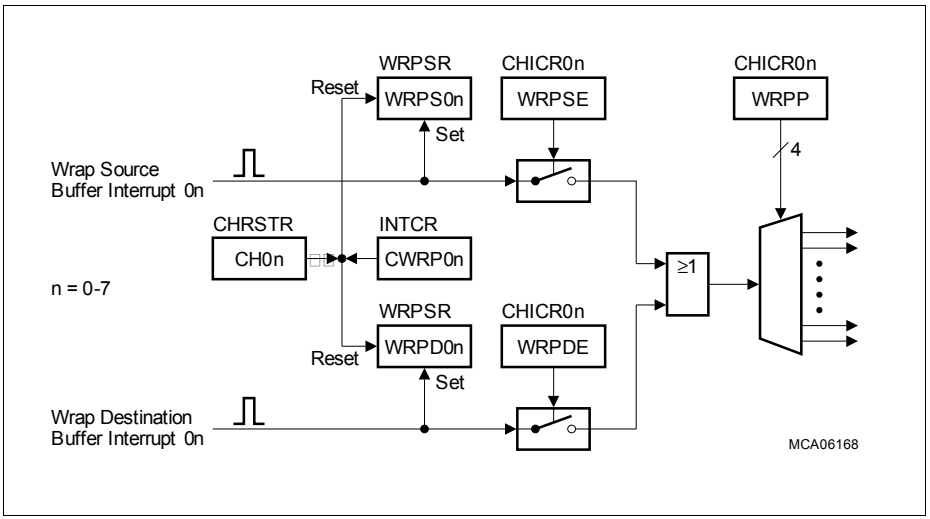


Figure 12-20 DMA Wrap Buffer Interrupts (m = 0-1)

1) In the TC1798 SR[7:0] are connected to interrupt nodes. SR[15:8] are used as DMA channel trigger signals.

12.2.12.5 Interrupt Request Compressor

The interrupt control logic of the DMA controller uses an interrupt compressing scheme that allows high flexibility in interrupt processing. The request compressor logic as shown in **Figure 12-21** condenses the 8 + 1 + 1 + 8 = 18 interrupt sources to the sixteen interrupt outputs. Each internal interrupt source can be directed to one of the sixteen interrupt outputs SR[15:0][1)] by using a 4-bit Interrupt Node Pointer. This also allows the connection of more than one interrupt source to one interrupt output SRx. Each interrupt output SR[15:0][1)] can also be activated by writing a 1 to the corresponding bit GINTR.SIDMAx.

1) In the TC1798 SR[7:0] are connected to interrupt nodes. SR[15:8] are used as DMA channel trigger signals.

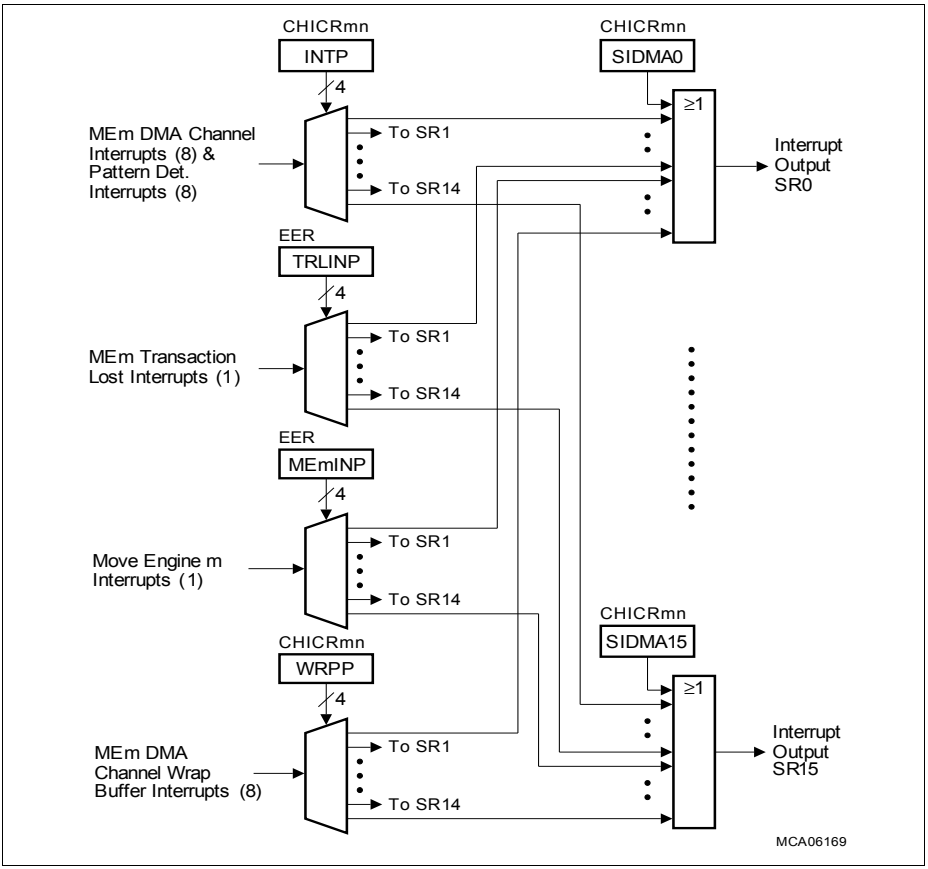


Figure 12-21 DMA Interrupt Request Compressor (m = 0-1)

12.2.13 Pattern Detection

The Move Engine in the DMA Sub-Block provides a register ME0R that contains the data that was read during the last read move. Parts of this read move data can be compared after the read move to data that is stored in the Move Engine pattern register ME0PR of DMA Sub-Block 0. The result of this pattern compare match is always stored in a bit (LXO) of the channel status register of the DMA channel mn that is currently executing the DMA move. Therefore, the pattern match result LXO of the previous read move can also be combined together with the pattern match result of the actual read move. ME0R is overwritten with each read move.

As the compare match patterns are stored in the Move Engine 0 (register ME0PR), its compare patterns are used for all DMA channels that are assigned to Move Engine 0 (all DMA channels of the DMA Sub-Block 0.

The configuration and capabilities of the pattern detection logic further depends on the settings of CHCRmn.CHDW. CHDW determines the data width for the read and write moves individually for each DMA channel mn. Another control bit, CHCRmn.PATSEL, selects among the different operating modes for a specific value of CHDW.

Depending on CHCRmn.PATSEL and on the positive result of the comparison, two actions follow (if CHCRmn.PATSEL=00, no action will be taken when a pattern match is detected, so the wrap interrupt can be used):

- The activation of the interrupt corresponding to the current active channel mn using the Interrupt Pointer defined in CHICRmn.INTP.
- Reset TRSR.HTREmn and TRSR.CHmn in order to stop the current transaction (Hardware and Software request enable). The value of CHSRmn.TCOUNT can be read out by the interrupt software.

The software will have to service the interrupt and to activate again the channel.

12.2.13.1 Pattern Compare Logic

Read move data and compare match patterns are compared on a bit-wise level. The logic as shown in **Figure 12-22** is implemented in each COMP block of **Figure 12-23**, **Figure 12-24**, and **Figure 12-25**. One COMP block controls either 8 bits or 16 bits of data and makes it possible to mask each data bit for the compare operation.

In the compare logic for one bit of the COMP block, a data bit from register ME0R is compared to the corresponding pattern bit stored in register ME0PR. If both bits are equal and a pattern mask bit stored in another part of register ME0PR is 0, the compare matched condition becomes active. When the pattern mask bit is set to 1, the compare matched condition is always active (set) for the related bit. When the compare matched conditions for each bit within a COMP block are true, the compare match output line of the COMP block becomes active.

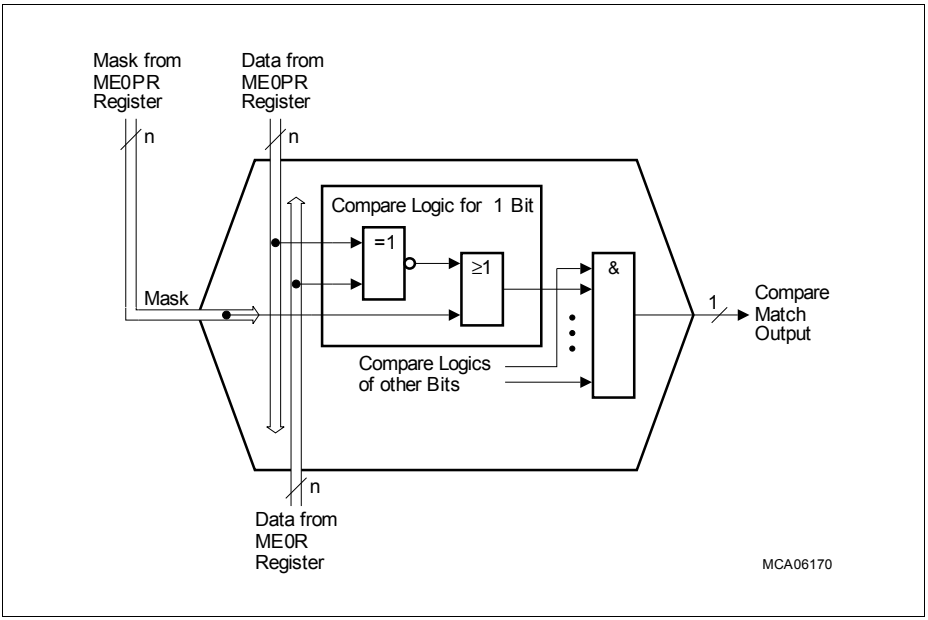


Figure 12-22 Pattern Compare Logic (COMP Block)

12.2.13.2 Pattern Detection for 8-bit Data Width

When 8-bit channel data width is selected (CHCRmn.CHDW = 00_B), the pattern detection logic is configured as shown in **Figure 12-23**. Three compare match configurations are possible.

Table 12-4 Pattern Detection for 8-bit Data Width

CHCRmn. PATSEL	Pattern Detection Operating Modes
00_B	Pattern detection disabled
01_B	Pattern compare of RD00 to PAT00, masked by PAT02
10_B	Pattern compare of RD00 to PAT01, masked by PAT03
11_B	Pattern compare of RD00 to PAT00, masked by PAT02 of the actual read move **and** Pattern compare of RD00 to PAT01, masked by PAT03 of the previous read move of DMA channel mn

When 8-bit channel data width is selected, the pattern detection logic allows the byte of one read move to be compared with two different patterns. Further, after each read move the pattern match result “RD00 with PAT01, masked by PAT03” is stored in bit CHCRmn.LXO. This operating mode allows, for example, two-byte sequences to be detected in an 8-bit data stream coming from a serial peripheral unit with 8-bit data width (e.g.: recognition of carriage-return, line-feed characters). A mask operation of each compared bit is possible.

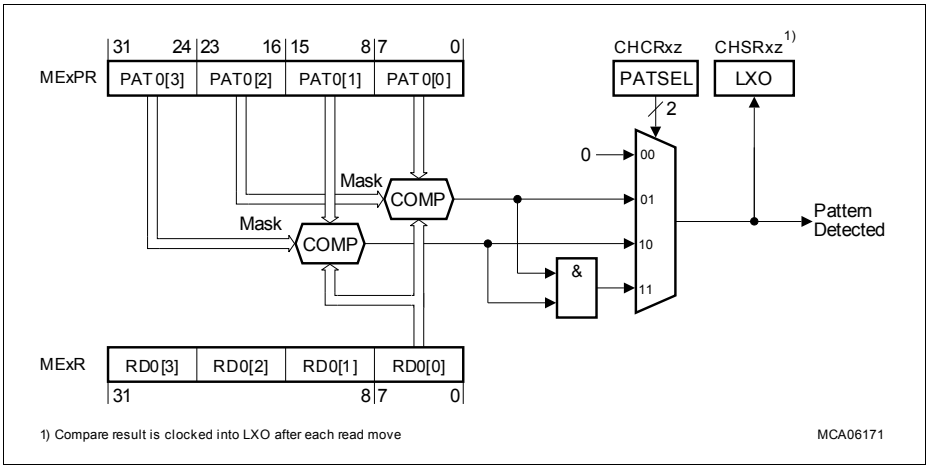


Figure 12-23 Pattern Detection for 8-bit Data Width (CHCRmn.CHDW = 00_B) (m = 0-

1)

12.2.13.3 Pattern Detection for 16-bit Data Width

When 16-bit channel data width is selected (CHCRmn.CHDW = 01_B) the pattern detection logic can be configured as shown in **Figure 12-24**. Three compare match configurations are possible.

Table 12-5 Pattern Detection for 16-bit Data Width

CHCRmn. **PATSEL**	**ADRCR**mn. **INCS**	**Pattern Detection Operating Modes**
00_B	–	Pattern detection disabled
01_B	–	**Aligned Mode:** Pattern compare of RD0[1:0] to PAT0[1:0], masked by PAT0[3:2]
10_B	0	**Unaligned Mode 1 (Source Address Decrement):** Pattern compare of RD01 to PAT00, masked by PAT02 of the actual read move **and** Pattern compare of RD00 to PAT01, masked by PAT03 (LXO) of the previous read move of DMA channel mn
	1	**Unaligned Mode 2 (Source Address Increment):** Pattern compare of RD00 to PAT01, masked by PAT03 of the actual read move **and** Pattern compare of RD01 to PAT00, masked by PAT02 (LXO) of the previous read move of DMA channel mn
11_B	0 or 1	**Combined Mode:** Pattern compare for aligned mode (PATSEL = 01_B) **or** unaligned modes (PATSEL = 10_B)

When 16-bit channel data width is selected, the pattern detection logic makes it possible to compare the complete half-word of one read move only (aligned mode) or to compare upper and lower byte of two consecutive read moves (unaligned modes). Both modes can be combined (combined mode) too. A mask operation of each compared bit is possible.

In unaligned mode 1 (source address decremented), the high byte (RD01) of the current and the low byte (RD00) of the previous 16-bit read move are compared.

In unaligned mode 2 (source address incremented), the low byte (RD00) of the current and the high byte (RD01) of the previous 16-bit read move are compared.

If it is not known on which byte boundary (even or odd address) the 16-bit pattern to be detected is located, the combined mode should be used. This mode is the most flexible

mode that combines the pattern search capability for aligned and unaligned 16-bit data searches.

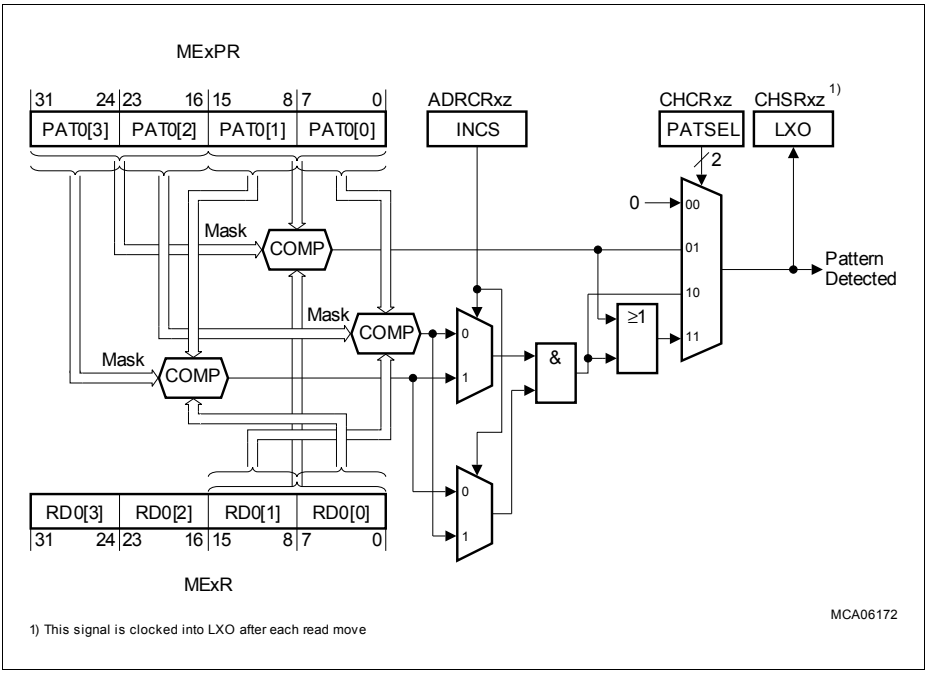


Figure 12-24 Pattern Detection for 16-bit Data Width (CHCRmn.CHDW = 01_B)
(m = 0-1)

12.2.13.4 Pattern Detection for 32-bit Data Width

When 32-bit channel data width is selected (CHCRmn.CHDW = 10_B) the pattern detection logic is configured as shown in **Figure 12-25**. Three compare match configurations are possible.

Table 12-6 Pattern Detection for 32-bit Data Width

CHCRmn. PATSEL	Pattern Detection Operating Modes
00_B	Pattern detection disabled
01_B	Unmasked pattern compare of RD0[1:0] to PAT0[1:0]
10_B	Unmasked pattern compare of RD0[3:2] to PAT0[3:2]
11_B	Unmasked pattern compare of RD0[3:0] to PAT0[3:0]

In 32-bit channel data width mode, the pattern detection logic makes it possible to compare the lower half-word only, the upper half-word only, or the complete 32-bit word with a pattern stored in the ME0PR register. A mask operation is not possible.

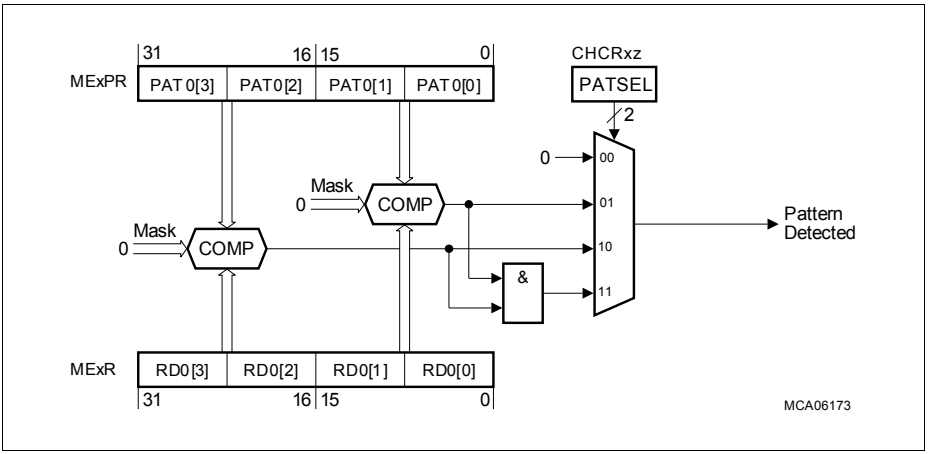


Figure 12-25 Pattern Detection for 32-bit Data Width (CHCRmn.CHDW = 10_B)
(m = 0-1)

12.2.14 Access Protection

The DMA controller provides an access protection logic that makes it possible to disable read and write accesses of the Move Engines to specific parts of the memory map. Each address of a read move and a write move is always checked to determine if it is within an address range that is enabled for read/write access. If no address range is valid for an actual move address, a Move Engine interrupt can be generated. Accesses outside of specific locations of the memory map (AEN address ranges) are invalid and will not be executed by the Move Engines or MLIs and will result in an access protection violation.

The access protection logic handles two levels of address range definitions:

- Fixed address range
- Programmable address range extension

There are 32 fixed address ranges available that can be individually enabled/disabled in the Move Engine by the address range enable bits AENx (x = 0-31): These bits are located in the Move Engine m Access Enable Registers MEmAENR0 and MEmAENR1. If bit AENx is set, read/write accesses to the associated address range x are allowed. If bit AENx is cleared (default after reset), read/write accesses to the associated address range x are not executed and a Move Engine interrupt for source or destination move is generated (see also **Section 12.2.12.3**).

Additionally eight programmable address range extensions are available for each of the two Move Engines that are fixed assigned to the Program Scratch SRAM, the Data Scratch SRAM, the LMU SRAM and PCP Data SRAM (see also **Section 12.4.2**). Each programmable address range extension makes it possible to define a sub-range within the corresponding address range where an access will be executed by the corresponding Move Engine if the address range is not disabled by the corresponding AENx bit. An access to the address range outside the defined sub-range will not be executed by the corresponding Move Engine. The parameters for the sub-ranges are stored in the Move Engine m Access Range Registers MEmARR0 and MEmARR1. The programmable address range extension is a feature that is applicable for memory access protection of memory blocks. In such an application, several memory sections are defined as sub-ranges of a complete memory block.

Figure 12-26 shows the two levels of address range definitions with the resulting address sub-ranges of the programmable address range extension. In a fixed address range, the width of fixed and variable address bits is constant. Number “a” determines the lowest bit position of the fixed address, and is fixed individually and product-specific for each of the 32 fixed address ranges. With the programmable address range extension, the variable address part of the fixed address range definition (as defined by AENx) is reduced by the definition of a programmable number (up to 32) of sub-ranges. Bit field MEmARR0.SIZE/MEmARR1.SIZE determines the sub-range size and bit field MEmARR0.SLICE/MEmARR1.SLICE determines which of the sub-ranges is currently

selected for access protection control. The two parameters (SIZE, SLICE) of the eight address range extensions of a move engine are numbered by index “n” (n = 0-3).

In the TC1798 the number “a” is defined in the following way:

- ARR0.SIZE0/ARR0.SLICE0 covering the Program Scratch SRAM, “a” = 16
- ARR0.SIZE1/ARR0.SLICE1 covering the LMU SRAM, “a” = 17
- ARR0.SIZE2/ARR0.SLICE2 covering the Data Scratch SRAM, “a” = 17
- ARR0.SIZE3/ARR0.SLICE3 covering the PCP Data SRAM, “a” = 16

Two sub-range examples (see **Figure 12-26**):

- 2^3 = 8 sub-ranges are available with SIZE = 100_B. SLICE[2:0] selects one out of the eight sub-ranges. SLICE[4:3] is “don’t care”.
- 2^7 = 128 sub-ranges are basically available with SIZEn = 000_B. SLICEn[4:0] selects one out of the lowest 32 sub-ranges. The upper 3 x 32 = 96 sub-ranges are not selectable (fixed address bits a-1 and a-2).

*Note: The definition of the fixed address ranges x and the assignment of each sub-range to one of the fixed address ranges is product-specific. The definitions of the address ranges for the DMA controller as implemented in the TC1798 are defined on **Page 12-111**.*

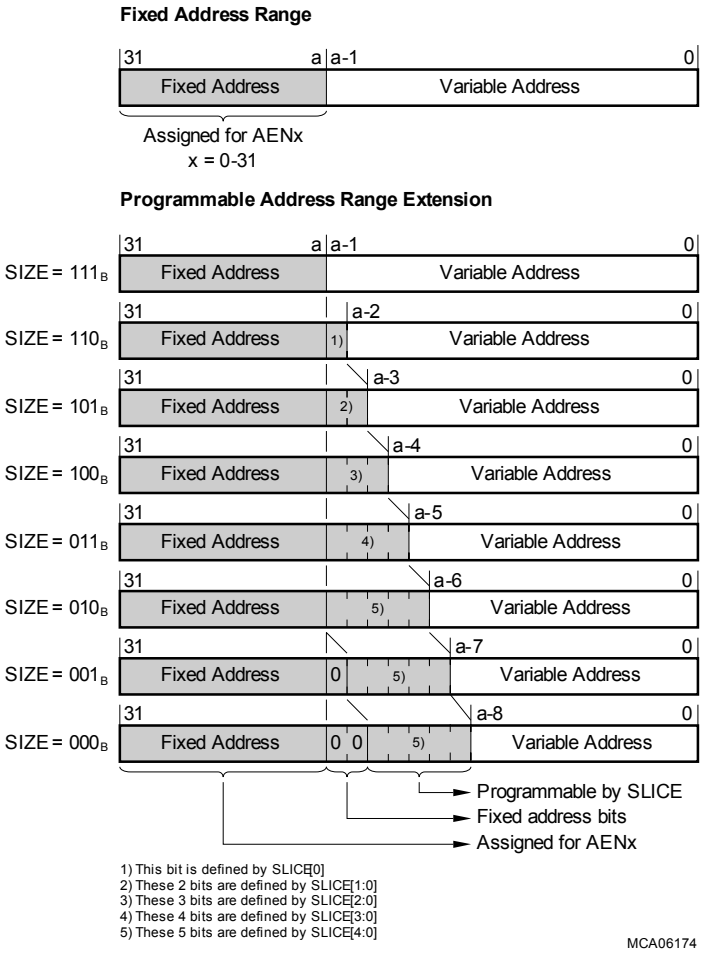


Figure 12-26 Access Protection Address Range Definitions

12.3 DMA Module Registers

Figure 12-27 and Table 12-8 show all registers associated with the DMA Controller Kernel. Additionally, Table 12-8 includes the DMA module specific registers. All DMA kernel register names described in this section are also referenced in other parts of the TC1798 User´s Manual by the module name prefix “DMA_”.

The registers are numbered by one index to indicate the related DMA Sub-Block and one index to indicate the related DMA channel: Index “m” refers to the DMA Sub-Block number (m = 0-1) and Index “n” or “x” refers to the channel number (n = 0-7 or x = 0-7) within the DMA Sub-Block.

DMA Registers Overview

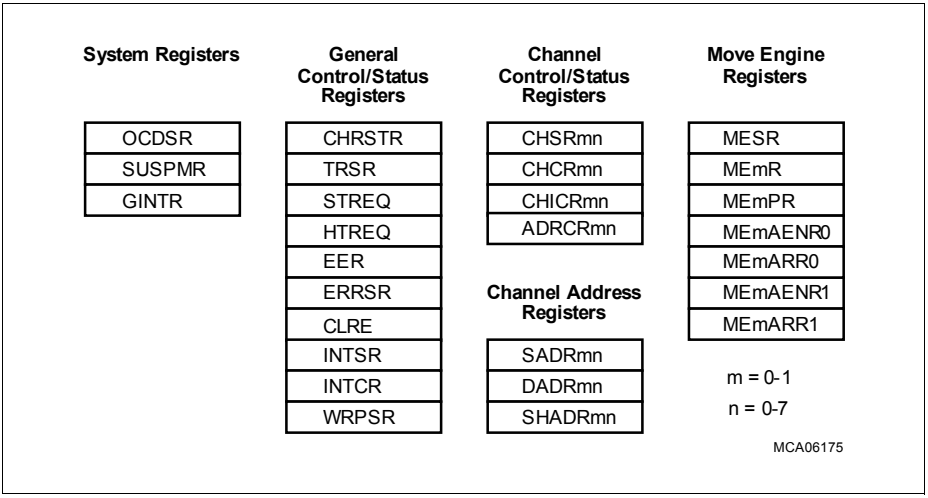


Figure 12-27 DMA Kernel Registers

Table 12-7 Registers Address Space - DMA Module

Module	Base Address	End Address	Note
DMA	$F000\ 3C00_H$	$F000\ 3EFF_H$	

Table 12-8 Registers Overview - DMA Control Registers

Short Name	Description	Offset Addr.[1)]	Access Mode		Reset Class	Description See
			Read	Write		
DMA_CLC	DMA Clock Control Register	000_H	U, SV	SV, E	3	Page 12-125
-	Reserved	004_H	nBE	SV	-	-
DMA_ID	DMA Module Identification Register Reserved	008_H	U, SV	BE	-	Page 12-53
-	Reserved	$00C_H$	BE	BE	-	-
DMA_CHRSTR	DMA Channel Reset Request Register	010_H	U, SV	SV	3	Page 12-59
DMA_TRSR	DMA Transaction Request State Register	014_H	U, SV	BE	3	Page 12-60
DMA_STREQ	DMA Software Transaction Request Register	018_H	U, SV	SV	3	Page 12-62
DMA_HTREQ	DMA Hardware Transaction Request Register	$01C_H$	U, SV	SV	3	Page 12-63
DMA_EER	DMA Enable Error Register	020_H	U, SV	SV	3	Page 12-65
DMA_ERRSR	DMA Error Status Register	024_H	U, SV	BE	3	Page 12-68
DMA_CLRE	DMA Clear Error Register	028_H	U, SV	SV	3	Page 12-71
DMA_GINTR	DMA Global Interrupt Set Register	$02C_H$	U, SV	SV	3	Page 12-58
DMA_MESR	DMA Move Engine Status Register	030_H	U, SV	BE	3	Page 12-78
DMA_ME0R	DMA Move Engine 0 Read Register	034_H	U, SV	BE	3	Page 12-80
DMA_ME1R	DMA Move Engine 1 Read Register	038_H	U, SV	BE	3	Page 12-80
DMA_ME0PR	DMA Move Engine 0 Pattern Register	$03C_H$	U, SV	SV	3	Page 12-80

Table 12-8 Registers Overview - DMA Control Registers

Short Name	Description	Offset Addr.[1]	Access Mode		Reset Class	Description See
			Read	Write		
DMA_ME1PR	DMA Move Engine 1 Pattern Register	040_H	U, SV	SV	3	Page 12-80
DMA_ME0AENR0	DMA Move Engine 0 Access Enable Register0	044_H	U, SV	SV, E	3	Page 12-81
DMA_ME0ARR0	DMA Move Engine 0 Access Range Register0	048_H	U, SV	SV, E	3	Page 12-83
DMA_ME1AENR0	DMA Move Engine 1 Access Enable Register0	$04C_H$	U, SV	SV, E	3	Page 12-81
DMA_ME1ARR0	DMA Move Engine 1 Access Range Register0	050_H	U, SV	SV, E	3	Page 12-83
DMA_INTSR	DMA Interrupt Status Register	054_H	U, SV	BE	3	Page 12-73
DMA_INTCR	DMA Interrupt Clear Register	058_H	U, SV	SV	3	Page 12-77
DMA_WRPSR	DMA Wrap Status Register	$05C_H$	U, SV	BE	3	Page 12-75
-	Reserved	060_H	BE	BE	-	-
DMA_OCDSR	DMA OCDS Register	064_H	U, SV	SV, E	1	Page 12-54
DMA_SUSPMR	DMA Suspend Mode Register	068_H	U, SV	SV, E	1	Page 12-56
DMA_ME0AENR1	DMA Move Engine 0 Access Enable Register 1	$06C_H$	U, SV	SV, E	3	Page 12-81
DMA_ME0ARR1	DMA Move Engine 0 Access Range Register 1	070_H	U, SV	SV, E	3	Page 12-83
DMA_ME1AENR1	DMA Move Engine 1 Access Enable Register 1	074_H	U, SV	SV, E	3	Page 12-81

Table 12-8 Registers Overview - DMA Control Registers

Short Name	Description	Offset Addr.[1)]	Access Mode		Reset Class	Description See
			Read	Write		
DMA_ME1_ARR1	DMA Move Engine 1 Access Range Register 1	078_H	U, SV	SV, E	3	Page 12-83
-	Reserved	$07C_H$	BE	BE		
DMA_CHSRmn	DMA Channel mn Status Register (n = 0-7, m = 0-1)	(n x 20_H) + (m x 100_H) + 080_H	U, SV	BE	3	Page 12-89
DMA_CHCRmn	DMA Channel mn Control Register (n = 0-7, m = 0-1)	(n x 20_H) + (m x 100_H) + 084_H	U, SV	SV	3	Page 12-85
DMA_CHICRmn	DMA Channel mn Interrupt Control Register (n = 0-7, m = 0-1)	(n x 20_H) + (m x 100_H) + 088_H	U, SV	SV	3	Page 12-90
DMA_ADRCRmn	DMA Channel mn Address Control Register (n = 0-7, m = 0-1)	(n x 20_H) + (m x 100_H) + $08C_H$	U, SV	SV	3	Page 12-92
DMA_SADRmn	DMA Channel mn Source Address Register (n = 0-7, m = 0-1)	(n x 20_H) + (m x 100_H) + 090_H	U, SV	SV	3	Page 12-97
DMA_DADRmn	DMA Channel mn Destination Address Register (n = 0-7, m = 0-1)	(n x 20_H) + (m x 100_H) + 094_H	U, SV	SV	3	Page 12-98

Table 12-8 Registers Overview - DMA Control Registers

Short Name	Description	Offset Addr.[1]	Access Mode		Reset Class	Description See
			Read	Write		
DMA_SHADRmn	DMA Channel mn Shadow Address Register (n = 0-7, m = 0-1)	(n x 20_H) + (m x 100_H) + 098_H	U, SV	BE / SV [2]	3	Page 12-99
-	Reserved (n = 0-7, m = 0-1)	(n x 20_H) + (m x 100_H) + $09C_H$	BE	BE	-	-
-	Reserved	280_H-$29C_H$	BE	BE	-	-
DMA_MLI0SRC3	DMA MLI0 Service Request Control Reg. 3	$2A0_H$	U, SV	SV	3	Page 12-127
DMA_MLI0SRC2	DMA MLI0 Service Request Control Reg. 2	$2A4_H$	U, SV	SV	3	Page 12-127
DMA_MLI0SRC1	DMA MLI0 Service Request Control Reg. 1	$2A8_H$	U, SV	SV	3	Page 12-127
DMA_MLI0SRC0	DMA MLI0 Service Request Control Reg. 0	$2AC_H$	U, SV	SV	3	Page 12-127
–	Reserved	$2B0_H$ - $2B4_H$	BE	BE	-	-
DMA_MLI1SRC1	DMA MLI1 Service Request Control Reg. 1	$2B8_H$	U, SV	SV	3	Page 12-127
DMA_MLI1SRC0	DMA MLI1 Service Request Control Reg. 0	$2BC_H$	U, SV	SV	3	Page 12-127
–	Reserved	$2C0_H$ - $2DC_H$	BE	BE	3	Page 12-127

Table 12-8 Registers Overview - DMA Control Registers

Short Name	Description	Offset Addr.[1]	Access Mode		Reset Class	Description See
			Read	Write		
DMA_SRC7	DMA Service Request Control Register 7	$2E0_H$	U, SV	SV	3	Page 12-126
DMA_SRC6	DMA Service Request Control Register 6	$2E4_H$	U, SV	SV	3	Page 12-126
DMA_SRC5	DMA Service Request Control Register 5	$2E8_H$	U, SV	SV	3	Page 12-126
DMA_SRC4	DMA Service Request Control Register 4	$2EC_H$	U, SV	SV	3	Page 12-126
DMA_SRC3	DMA Service Request Control Register 3	$2F0_H$	U, SV	SV	3	Page 12-126
DMA_SRC2	DMA Service Request Control Register 2	$2F4_H$	U, SV	SV	3	Page 12-126
DMA_SRC1	DMA Service Request Control Register 1	$2F8_H$	U, SV	SV	3	Page 12-126
DMA_SRC0	DMA Service Request Control Register 0	$2FC_H$	U, SV	SV	3	Page 12-126

1) The absolute register address is calculated as follows:
Module Base Address (Table 12-7) + Offset Address (shown in this column)
Further, the following ranges for parameters i, k, x, and n are valid: i = 0-7, k = 0-7, x = 0-1, n = 0-63.

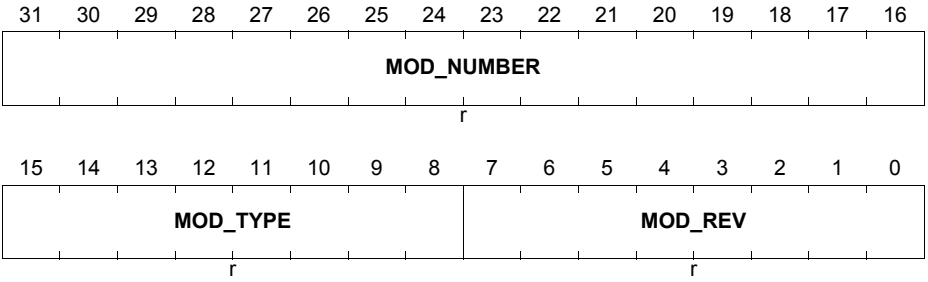
2) Write access mode to DMA_SHADRmn is controlled by the register bit DMA_ADRCRmn.SHWEN. DMA_ADRCRmn.SHWEN=´0´ -> Access Mode Write for DMA_SHADRmn is BE. DMA_ADRCRmn.SHWEN=´1´ -> Access Mode Write for DMA_SHADRmn is SV.

Note: Register bits marked “w” in the following register description are virtual registers and do not contain flip-flops. They are always read as 0.

12.3.1 System Registers

DMA Module Identification Register.

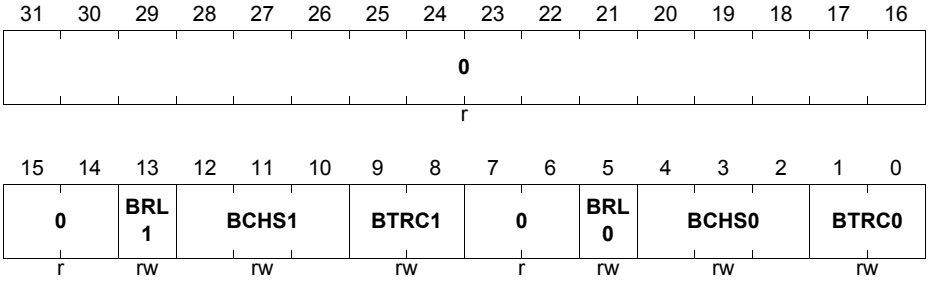
DMA_ID
Module Identification Register **(008_H)** **Reset Value: 001A C0XX$_H$**



Field	Bits	Type	Description
MOD_REV	[7:0]	r	**Module Revision Number** This bit field defines the module revision number. The value of a module revision starts with 01_H (first revision).
MOD_TYPE	[15:8]	r	**Module Type** The bit field is set to $C0_H$ which defines the module as a 32-bit module.
MOD_NUMBER	[31:16]	r	**Module Number Value** This bit field defines a module identification number. The value for the DMA module is $001A_H$.

The OCDS Register describes the break capability of the DMA module. OCDSR is only reset with the OCDS Reset.

DMA_OCDSR
DMA OCDS Register **(064_H)** **Reset Value: 0000 0000_H**



Field	Bits	Type	Description
BTRC0	[1:0]	rw	**Break Trigger Condition In Sub-Block 0** This bit field determines the transition type for the transaction request bit TRSR.CH0n that leads to a break condition in DMA Sub-Block 0. 00_B No break condition is generated 01_B A break condition is generated when TRSR.CH0n changes from 0 to 1 10_B A break condition is generated when TRSR.CH0n changes from 1 to 0 11_B A break condition is generated when TRSR.CH0n changes its state
BCHS0	[4:2]	rw	**Break Channel Select In Sub-Block 0** This bit field determines the DMA channel n of DMA Sub-Block 0 whose transaction request bit TRSR.CH0n is observed for signal transitions as defined by BTRC0. 000_B DMA channel 00 selected 001_B DMA channel 01 selected …$_B$ … 110_B DMA channel 06 selected 111_B DMA channel 07 selected

Field	Bits	Type	Description
BRL0	5	rw	**Break On Request Lost in Sub-Block 0** This bit field determines whether a BREAK signal is generated for DMA Sub-Block 0 when at least one of its eight transaction lost interrupts becomes active. 0_B No break condition is generated 1_B A break condition is generated for DMA Sub-Block 0 when at least one of its eight transaction lost interrupts becomes active
BTRC1	[9:8]	rw	**Break Trigger Condition In Sub-Block 1** This bit field determines the transition type for the transaction request bit TRSR.CH1n that leads to a break condition in DMA Sub-Block 1. 00_B No break condition is generated 01_B A break condition is generated when TRSR.CH1n changes from 0 to 1 10_B A break condition is generated when TRSR.CH1n changes from 1 to 0 11_B A break condition is generated when TRSR.CH1n changes its state
BCHS1	[12:10]	rw	**Break Channel Select In Sub-Block 1** This bit field determines the DMA channel n of DMA Sub-Block 1 whose transaction request bit TRSR.CH1n is observed for signal transitions as defined by BTRC1. 000_B DMA channel 10 selected 001_B DMA channel 11 selected ...B ... 110_B DMA channel 16 selected 111_B DMA channel 17 selected
BRL1	13	rw	**Break On Request Lost in Sub-Block 1** This bit field determines whether a BREAK signal is generated for DMA Sub-Block 1 when at least one of its eight transaction lost interrupts becomes active. 0_B No break condition is generated 1_B A break condition is generated for DMA Sub-Block 1when at least one of its eight transaction lost interrupts becomes active
0	[7:6], [31:14]	r	**Reserved** Read as 0; should be written with 0.

The Suspend Mode Register contains bits for each DMA channel that make it possible to enable/disable its Soft-suspend Mode capability and that indicate its suspend status.

DMA_SUSPMR
DMA Suspend Mode Register **(068_H)** **Reset Value: $0000\ 0000_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SUSAC17	**SUSAC16**	**SUSAC15**	**SUSAC14**	**SUSAC13**	**SUSAC12**	**SUSAC11**	**SUSAC10**	**SUSAC07**	**SUSAC06**	**SUSAC05**	**SUSAC04**	**SUSAC03**	**SUSAC02**	**SUSAC01**	**SUSAC00**
rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SUSEN17	**SUSEN16**	**SUSEN15**	**SUSEN14**	**SUSEN13**	**SUSEN12**	**SUSEN11**	**SUSEN10**	**SUSEN07**	**SUSEN06**	**SUSEN05**	**SUSEN04**	**SUSEN03**	**SUSEN02**	**SUSEN01**	**SUSEN00**
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
SUSEN0n (n = 0-7)	n	rw	**Suspend Enable for DMA Channel 1n** This bit enables the soft suspend capability individually for each DMA channel 0n. 0_B DMA channel 0n is disabled for Soft-suspend Mode. The DMA channel 0n does not react on an active suspend request signal SUSREQ. 1_B DMA channel 0n is enabled for Soft-suspend Mode. If the suspend request signal SUSREQ becomes active, a DMA transaction of DMA channel 0n is stopped after the current DMA transfer has been finished Soft-suspend Mode can be terminated when SUSEN0n is written with 0.

Field	Bits	Type	Description
SUSEN1n (n = 0-7)	8+n	rw	**Suspend Enable for DMA Channel 1n** This bit enables the soft suspend capability individually for each DMA channel 1n. 0_B DMA channel 1n is disabled for Soft-suspend Mode. The DMA channel 1n does not react on an active suspend request signal SUSREQ 1_B DMA channel 1n is enabled for Soft-suspend Mode. If the suspend request signal SUSREQ becomes active, a DMA transaction of DMA channel 1n is stopped after the current DMA transfer has been finished Soft-suspend Mode can be terminated when SUSENmn is written with 0.
SUSAC0n (n = 0-7)	16+n	rh	**Suspend Active for DMA Channel 0n** This status bit indicates whether DMA channel 0n is in Soft-suspend Mode or not. 0_B DMA channel 0n is not in Soft-suspend Mode or internal actions are not yet finished after the Soft-suspend Mode was requested 1_B DMA channel 0n is in Soft-suspend Mode
SUSAC1n (n = 0-7)	24+n	rh	**Suspend Active for DMA Channel 1n** This status bit indicates whether DMA channel 1n is in Soft-suspend Mode or not. 0_B DMA channel 1n is not in Soft-suspend Mode or internal actions are not yet finished after the Soft-suspend Mode was requested 1_B DMA channel 1n is in Soft-suspend Mode

Note: This register is only reset by the Debug reset.

The Global Interrupt Set Register allows the interrupt output lines of the DMA to be activated by software.

DMA_GINTR

DMA Global Interrupt Set Register (02C$_H$) Reset Value: 0000 0000$_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SIDMA15	SIDMA14	SIDMA13	SIDMA12	SIDMA11	SIDMA10	SIDMA9	SIDMA8	SIDMA7	SIDMA6	SIDMA5	SIDMA4	SIDMA3	SIDMA2	SIDMA1	SIDMA0
w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w

Field	Bits	Type	Description
SIDMAx (x = 0-15)	x	w	**Set DMA Interrupt Output Line x** 0_B No action 1_B DMA interrupt output line SRx will be activated. Reading this bit returns a 0
0	[31:16]	r	**Reserved** Read as 0; should be written with 0.

*Note: In the TC1798, SR[7:0] are connected to interrupt nodes. SR[15:8] are used as DMA channel request inputs (**Page 12-101**).*

12.3.2 General Control/Status Registers

The bits in the Channel Reset Request Register are used to reset DMA channel mn.

DMA_CHRSTR
DMA Channel Reset Request Register

(010_H) **Reset Value: $0000\ 0000_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CH 17	CH 16	CH 15	CH 14	CH 13	CH 12	CH 11	CH 10	CH 07	CH 06	CH 05	CH 04	CH 03	CH 02	CH 01	CH 00
rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh

Field	Bits	Type	Description
CH0n (n = 0-7)	n	rwh	**Channel 0n Reset** These bits force the DMA channel 0n to stop its current DMA transaction. Once set by software, this bit will be automatically cleared when the channel has been reset. Writing a 0 to CH0n has no effect. 0_B No action (write) or the requested channel reset has been reset (read). 1_B DMA channel 0n is stopped. More details see Page 12-16.
CH1n (n = 0-7)	8+n	rwh	**Channel 1n Reset** These bits force the DMA channel 1n to stop its current DMA transaction. Once set by software, this bit will be automatically cleared when the channel has been reset. Writing a 0 to CH1n has no effect. 0_B No action (write) or the requested channel reset has been reset (read). 1_B DMA channel 1n is stopped. More details see Page 12-16.
0	[31:16]	r	**Reserved** Read as 0; should be written with 0.

The bits in the Transaction Request State Register indicates which DMA channel is processing a request, and which DMA channel has hardware transaction requests enabled.

DMA_TRSR
DMA Transaction Request State Register

(014_H) **Reset Value: $0000\ 0000_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HTRE17	**HTRE16**	**HTRE15**	**HTRE14**	**HTRE13**	**HTRE12**	**HTRE11**	**HTRE10**	**HTRE07**	**HTRE06**	**HTRE05**	**HTRE04**	**HTRE03**	**HTRE02**	**HTRE01**	**HTRE00**
rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CH17	**CH16**	**CH15**	**CH14**	**CH13**	**CH12**	**CH11**	**CH10**	**CH07**	**CH06**	**CH05**	**CH04**	**CH03**	**CH02**	**CH01**	**CH00**
rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh

Field	Bits	Type	Description
CH0n (n = 0-7)	n	rh	**Transaction Request State of DMA Channel 0n** 0_B No DMA request is pending for channel 0n. 1_B A DMA request is pending for channel 0n.
CH1n (n = 0-7)	8+n	rh	**Transaction Request State of DMA Channel 1n** 0_B No DMA request is pending for channel 1n. 1_B A DMA request is pending for channel 1n.
HTRE0n (n = 0-7)	16+n	rh	**Hardware Transaction Request Enable State of DMA Channel 0n** 0_B Hardware transaction request for DMA Channel 0n is disabled. An input DMA request will not trigger the channel 0n. 1_B Hardware transaction request for DMA Channel 0n is enabled. The transfers of a DMA transaction are controlled by the corresponding channel request line of the DMA requesting source. HTRE0n is set to 0 when CHSR0n.TCOUNT is decremented and CHSR0n.TCOUNT = 0. HTRE0n can be enabled and disabled with HTREQ.ECH0n or HTREQ.DCH0n.

Field	Bits	Type	Description
HTRE1n (n = 0-7)	24+n	rh	**Hardware Transaction Request Enable State of DMA Channel 1n** 0_B Hardware transaction request for DMA Channel 1n is disabled. An input DMA request will not trigger the channel 1n. 1_B Hardware transaction request for DMA Channel 1n is enabled. The transfers of a DMA transaction are controlled by the corresponding channel request line of the DMA requesting source. HTRE1n is set to 0 when CHSR1n.TCOUNT is decremented and CHSR1n.TCOUNT = 0. HTRE1n can be enabled and disabled with HTREQ.ECH1n or HTREQ.DCH1n.

The bits in the Software Transaction Request Register are used to generate a DMA transaction request by software.

DMA_STREQ
DMA Software Transaction Request Register
(018_H) **Reset Value: $0000\ 0000_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SCH 17	SCH 16	SCH 15	SCH 14	SCH 13	SCH 12	SCH 11	SCH 10	SCH 07	SCH 06	SCH 05	SCH 04	SCH 03	SCH 02	SCH 01	SCH 00
w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w

Field	Bits	Type	Description
SCH0n (n = 0-7)	n	w	**Set Transaction Request for DMA Channel 0n** 0_B No action. 1_B A transaction for DMA channel 0n is requested. When setting SCH0n, TRSR.CH0n becomes set to indicate that a DMA request is pending for DMA channel 0n.
SCH1n (n = 0-7)	8+n	w	**Set Transaction Request for DMA Channel 1n** 0_B No action. 1_B A transaction for DMA channel 1n is requested. When setting SCH1n, TRSR.CH1n becomes set to indicate that a DMA request is pending for DMA channel 1n.
0	[31:16]	r	**Reserved** Read as 0; should be written with 0.

Note: Register bits marked with "w" are virtual and are not stored in flip-flops. Reading STREQ returns 0 when read.

The bits in the Hardware Transaction Request Register enable or disable DMA hardware requests.

DMA_HTREQ
DMA Hardware Transaction Request Register
($01C_H$) **Reset Value: $0000\ 0000_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DCH 17	DCH 16	DCH 15	DCH 14	DCH 13	DCH 12	DCH 11	DCH 10	DCH 07	DCH 06	DCH 05	DCH 04	DCH 03	DCH 02	DCH 01	DCH 00
w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ECH 17	ECH 16	ECH 15	ECH 14	ECH 13	ECH 12	ECH 11	ECH 10	ECH 07	ECH 06	ECH 05	ECH 04	ECH 03	ECH 02	ECH 01	ECH 00
w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w

Field	Bits	Type	Description
ECH0n (n = 0-7)	n	w	**Enable Hardware Transfer Request for DMA Channel 0n** see table below
ECH1n (n = 0-7)	8+n	w	**Enable Hardware Transfer Request for DMA Channel 1n** see table below
DCH0n (n = 0-7)	16+n	w	**Disable Hardware Transfer Request for DMA Channel 0n** see table below
DCH1n (n = 0-7)	24+n	w	**Disable Hardware Transfer Request for DMA Channel 1n** see table below

Table 12-9 Conditions to Set/Reset the Bits TRSR.HTREmn

HTREQ.ECHmn	HTREQ.DCHmn	Transaction Finishes[1)] for Channel mn	Modification of TRSR.HTREmn
0	0	0	Unchanged
1	0	0	Set

Table 12-9 Conditions to Set/Reset the Bits TRSR.HTREmn (cont'd)

HTREQ.ECHmn	HTREQ.DCHmn	Transaction Finishes[1] for Channel mn	Modification of TRSR.HTREmn
X	1	X	Reset
X	X	1	Reset

1) In Single Mode only. In Continuous Mode, the end of a transaction has no impact.

The Enable Error Register describes how the DMA controller reacts to errors. It enables the interrupts for the loss of a transaction request or Move Engine errors.

DMA_EER
DMA Enable Error Register **(020_H)** **Reset Value: 0000 0000$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TRLINP				ME1INP				ME0INP				E ME1 DER	E ME1 SER	E ME0 DER	E ME0 SER
rw				rw				rw				rw	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
E TRL 17	E TRL 16	E TRL 15	E TRL 14	E TRL 13	E TRL 12	E TRL 11	E TRL 10	E TRL 07	E TRL 06	E TRL 05	E TRL 04	E TRL 03	E TRL 02	E TRL 01	E TRL 00
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
ETRL0n (n = 0-7)	n	rw	**Enable Transaction Request Lost for DMA Channel 0n** This bit enables the generation of an interrupt when the set condition for ERRSR.TRL0n is detected. 0_B The interrupt generation for a request lost event for channel 0n is disabled. 1_B The interrupt generation for a request lost event for channel 0n is enabled.
ETRL1n (n = 0-7)	8+n	rw	**Enable Transaction Request Lost for DMA Channel 1n** This bit enables the generation of an interrupt when the set condition for ERRSR.TRL1n is detected. 0_B The interrupt generation for a request lost event for channel 1n is disabled. 1_B The interrupt generation for a request lost event for channel 1n is enabled.
EME0SER	16	rw	**Enable Move Engine 0 Source Error** This bit enables the generation of a Move Engine 0 source error interrupt. 0_B Move Engine 0 source error interrupt is disabled. 1_B Move Engine 0 source error interrupt is enabled.

Field	Bits	Type	Description
EME0DER	17	rw	**Enable Move Engine 0 Destination Error** This bit enables the generation of a Move Engine 0 destination error interrupt. 0_B Move Engine 0 destination error interrupt is disabled. 1_B Move Engine 0 destination error interrupt is enabled.
EME1SER	18	rw	**Enable Move Engine 1 Source Error** This bit enables the generation of a Move Engine 1 source error interrupt. 0_B Move Engine 1 source error interrupt is disabled. 1_B Move Engine 1 source error interrupt is enabled.
EME1DER	19	rw	**Enable Move Engine 1 Destination Error** This bit enables the generation of a Move Engine 0 destination error interrupt. 0_B Move Engine 1 destination error interrupt is disabled. 1_B Move Engine 1 destination error interrupt is enabled.
ME0INP	[23:20]	rw	**Move Engine 0 Error Interrupt Node Pointer** ME0INP determines the number n (n = 0-15) of the service request output SRn that becomes active on a Move Engine 0 source or destination interrupt. 0000_B SR0 selected for Move Engine 0 interrupt 0001_B SR1 selected for Move Engine 0 interrupt $\ldots_B$ … 1111_B SR15 selected for Move Engine 0 interrupt *Note: In the TC1798, SR[7:0] are connected to interrupt nodes. SR[15:8] are used as DMA channel request inputs (**Page 12-101**).*

Field	Bits	Type	Description
ME1INP	[27:24]	rw	**Move Engine 1 Error Interrupt Node Pointer** ME1INP determines the number n (n = 0-15) of the service request output SRn that becomes active on a Move Engine 1 source or destination interrupt. 0000_B SR0 selected for Move Engine 1 interrupt 0001_B SR1 selected for Move Engine 1 interrupt …$_B$ … 1111_B SR15 selected for Move Engine 1 interrupt *Note: In the TC1798, SR[7:0] are connected to interrupt nodes. SR[15:8] are used as DMA channel request inputs (**Page 12-101**).*
TRLINP	[31:28]	rw	**Transaction Lost Interrupt Node Pointer** TRLINP determines the number n (n = 0-15) of the service request output SRn that becomes active on a transaction lost interrupt. 0000_B SR0 selected for transaction lost interrupt 0001_B SR1 selected for transaction lost interrupt …$_B$ … 1111_B SR15 selected for transaction lost interrupt *Note: In the TC1798, SR[7:0] are connected to interrupt nodes. SR[15:8] are used as DMA channel request inputs (**Page 12-101**).*

The Error Status Register indicates if the DMA controller could not answer to a request because the previous request was not terminated (see **Section 12.2.4.4**). It indicates also the FPI Bus accesses that have been terminated with errors.

DMA_ERRSR
DMA Error Status Register **(024_H)** **Reset Value: 0000 0000$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MLI1	LEC ME1			MLI0	LEC ME0			0	CERBERUSER	SRIER	FPIER	ME1DER	ME1SER	ME0DER	ME0SER
rh	rh			rh	rh			r	rh	rh	rh	rh	rh	rh	rh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TRL17	TRL16	TRL15	TRL14	TRL13	TRL12	TRL11	TRL10	TRL07	TRL06	TRL05	TRL04	TRL03	TRL02	TRL01	TRL00
rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh

Field	Bits	Type	Description
TRL0n (n = 0-7)	n	rh	**Transaction/Transfer Request Lost of DMA Channel 0n** 0_B 0 No request lost event has been detected for channel 0n. 1_B 1 A new DMA request was detected while TRSR.CH0n=1 (request lost event). This bit is reset by software when writing a 1 to CLRE.CTL0n, or by a channel reset (writing CHRSTR.CH0n = 1).
TRL1n (n = 0-7)	8+n	rh	**Transaction/Transfer Request Lost of DMA Channel 1n** 0_B No request lost event has been detected for channel 1n. 1_B A new DMA request was detected while TRSR.CH1n=1 (request lost event). This bit is reset by software when writing a 1 to CLRE.CTL1n, or by a channel reset (writing CHRSTR.CH1n = 1).

Field	Bits	Type	Description
ME0SER	16	rh	**Move Engine 0 Source Error** This bit is set whenever a Move Engine 0 error occurred during a source (read) move of a DMA transfer, or a request could not been serviced due to the access protection. 0_B No Move Engine 0 source error has occurred. 1_B A Move Engine 0 source error has occurred.
ME0DER	17	rh	**Move Engine 0 Destination Error** This bit is set whenever a Move Engine 0 error occurred during a destination (write) move of a DMA transfer, or a request could not been serviced due to the access protection. 0_B No Move Engine 0 destination error has occurred. 1_B A Move Engine 0 destination error has occurred.
ME1SER	18	rh	**Move Engine 1 Source Error** This bit is set whenever a Move Engine 1 error occurred during a source (read) move of a DMA transfer, or a request could not been serviced due to the access protection. 0_B No Move Engine 1 source error has occurred. 1_B A Move Engine 1 source error has occurred.
ME1DER	19	rh	**Move Engine 1 Destination Error** This bit is set whenever a Move Engine 1 error occurred during a destination (write) move of a DMA transfer, or a request could not been serviced due to the access protection. 0_B No Move Engine 1 destination error has occurred. 1_B A Move Engine 1 destination error has occurred.
FPIER	20	rh	**SPB Error** This bit is set whenever a move that has been started by the DMA/MLI FPI master interface leads to an error on the FPI Bus. 0_B No error occurred. 1_B An error occurred on FPI Bus interface.

Field	Bits	Type	Description
SRIER	21	rh	**SRI Error** This bit is set whenever a move that has been started by the DMA/MLI SRI master interface leads to an error on the SRI Bus. 0_B No error occurred. 1_B An error occurred on SRI Bus interface.
CERBERUSER	22	rh	**Cerberus Error Source** This bit is set whenever an On Chip Bus error occurred due to an action of Cerberus. 0_B No On Chip Bus error occurred due to Cerberus. 1_B An On Chip Bus error occurred due to Cerberus.
LECME0	[26:24]	rh	**Last Error Channel Move Engine 0** This bit field indicates the channel number of the last channel of Move Engine 0 leading to an On Chip Bus error that has occurred.
MLI0	27	rh	**MLI0 Error Source** This bit is set whenever an On Chip Bus error occurred due to an action of MLI0. 0_B No On Chip Bus error occurred due to MLI0. 1_B An On Chip Bus error occurred due to MLI0.
LECME1	[30:28]	rh	**Last Error Channel Move Engine 1** This bit field indicates the channel number of the last channel of Move Engine 1 leading to an On Chip Bus error that has occurred.
MLI1	31	rh	**MLI1 Error Source** This bit is set whenever an On Chip Bus error occurred due to an action of MLI1. 0_B No On Chip Bus error occurred due to MLI1. 1_B An On Chip Bus error occurred due to MLI1.
0	23	r	**Reserved** Read as 0; should be written with 0.

The Clear Error contains bits that make it possible to clear the Transaction Request Lost flags or the Move Engine error flags.

DMA_CLRE
DMA Clear Error Register **(028_H)** **Reset Value: 0000 0000$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CLRMLI1		0		CLRMLI0		0			CLCERBERUS	CSRIER	CFPIER	CME1DER	CME1SER	CME0DER	CME0SER
w		w		w		w			w	w	w	w	w	w	w

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CTL17	CTL16	CTL15	CTL14	CTL13	CTL12	CTL11	CTL10	CTL07	CTL06	CTL05	CTL04	CTL03	CTL02	CTL01	CTL00
w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w

Field	Bits	Type	Description
CTL0n (n = 0-7)	n	w	**Clear Transaction Request Lost for DMA Channel 0n** 0_B No action 1_B Clear DMA channel 0n transaction request lost flag ERRSR.TRL0n
CTL1n (n = 0-7)	n+8	w	**Clear Transaction Request Lost for DMA Channel 1n** 0_B No action 1_B Clear DMA channel 1n transaction request lost flag ERRSR.TRL1n
CME0SER	16	w	**Clear Move Engine 0 Source Error** 0_B No action 1_B Clear source error flag ERRSR.ME0SER.
CME0DER	17	w	**Clear Move Engine 0 Destination Error** 0_B No action 1_B Clear destination error flag ERRSR.ME0DER.
CME1SER	18	w	**Clear Move Engine 1 Source Error** 0_B No action 1_B Clear source error flag ERRSR.ME1SER.

Field	Bits	Type	Description
CME1DER	19	w	**Clear Move Engine 1 Destination Error** 0_B No action 1_B Clear destination error flag ERRSR.ME1DER.
CFPIER	20	w	**Clear FPI Error** 0_B No action 1_B Clear error flag ERRSR.FPIER.
CSRIER	21	w	**Clear SRI Error** 0_B No action 1_B Clear error flag ERRSR.SRIER.
CLCERBERUS	22	w	**Clear Cerberus Error** 0_B No action 1_B Clear error flag ERRSR.Cerberus.
CLRMLI0	27	w	**Clear MLI0 Error** 0_B No action 1_B Clear error flag ERRSR.MLI0.
CLRMLI1	31	w	**Clear MLI1 Error** 0_B No action 1_B Clear error flag ERRSR.MLI1.
0	[26:23], [30:28]	r	**Reserved** Should be written with 0.

The Interrupt Status Register indicates if CHSRmn.TCOUNT matches with CHICRmn.IRDV, or if CHSRmn.TCOUNT has been decremented (depending on CHICRmn.INTCT[0]),or if a pattern has been detected. These conditions can also generate an interrupt if enabled (see **Figure 12-17** on **Page 12-31**).

DMA_INTSR

DMA Interrupt Status Register (054_H) Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
IPM 17	**IPM 16**	**IPM 15**	**IPM 14**	**IPM 13**	**IPM 12**	**IPM 11**	**IPM 10**	**IPM 07**	**IPM 06**	**IPM 05**	**IPM 04**	**IPM 03**	**IPM 02**	**IPM 01**	**IPM 00**
rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ICH 17	**ICH 16**	**ICH 15**	**ICH 14**	**ICH 13**	**ICH 12**	**ICH 11**	**ICH 10**	**ICH 07**	**ICH 06**	**ICH 05**	**ICH 04**	**ICH 03**	**ICH 02**	**ICH 01**	**ICH 00**
rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh

Field	Bits	Type	Description
ICH0n (n = 0-7)	n	rh	**Interrupt from Channel 0n** This bit indicates that channel 0n has raised an interrupt for TCOUNT = IRDV or if TCOUNT has been decremented (depending on CHICR.INTCT[0]. This bit (and IP0n) is reset by software when writing a 1 to INTCR.CICH0n or by a channel reset (writing CHRSTR.CH0n = 1). 0_B A channel interrupt has not been detected. 1_B A channel interrupt has been detected.
ICH1n (n = 0-7)	8+n	rh	**Interrupt from Channel 1n** This bit indicates that channel 1n has raised an interrupt for TCOUNT = IRDV or if TCOUNT has been decremented (depending on CHICR.INTCT[0]. This bit (and IP1n) is reset by software when writing a 1 to INTCR.CICH1n or by a channel reset (writing CHRSTR.CH1n = 1). 0_B A channel interrupt has not been detected. 1_B A channel interrupt has been detected.

Field	Bits	Type	Description
IPM0n (n = 0-7)	16+n	rh	**Pattern Detection from Channel 0n** This bit indicates that a pattern has been detected for channel 0n while the pattern detection has been enabled. This bit (and ICH0n) is reset by software when writing a 1 to INTCR.CICH0n or by a channel reset (writing CHRSTR.CH0n = 1). 0_B A pattern has not been detected. 1_B A pattern has been detected.
IPM1n (n = 0-7)	24+n	rh	**Pattern Detection from Channel 1n** This bit indicates that a pattern has been detected for channel 1n while the pattern detection has been enabled. This bit (and ICH1n) is reset by software when writing a 1 to INTCR.CICH1n or by a channel reset (writing CHRSTR.CH1n = 1). 0_B A pattern has not been detected. 1_B A pattern has been detected.

The Wrap Status Register gives information about the channels that did a wrap-around on their source or destination buffer(s). This condition can also lead to an interrupt if it is enabled.

DMA_WRPSR
DMA Wrap Status Register **($05C_H$)** **Reset Value: 0000 0000$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
WRPD17	WRPD16	WRPD15	WRPD14	WRPD13	WRPD12	WRPD11	WRPD10	WRPD07	WRPD06	WRPD05	WRPD04	WRPD03	WRPD02	WRPD01	WRPD00
rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WRPS17	WRPS16	WRPS15	WRPS14	WRPS13	WRPS12	WRPS11	WRPS10	WRPS07	WRPS06	WRPS05	WRPS04	WRPS03	WRPS02	WRPS01	WRPS00
rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh

Field	Bits	Type	Description
WRPS0n (n = 0-7)	n	rh	**Wrap Source Buffer for Channel 0n** These bits indicate which channels have done a wrap-around of their source buffer(s). 0_B No wrap-around occurred for channel 0n. 1_B A wrap-around occurred for channel 0n. This bit is reset by software by writing a 1 to INTCR.CWRP0n or CHRSTR.CH0n.
WRPS1n (n = 0-7)	8+n	rh	**Wrap Source Buffer for Channel 1n** These bits indicate which channels have done a wrap-around of their source buffer(s). 0_B No wrap-around occurred for channel 1n. 1_B A wrap-around occurred for channel 1n. This bit is reset by software by writing a 1 to INTCR.CWRP1n or CHRSTR.CH1n.
WRPD0n (n = 0-7)	16+n	rh	**Wrap Destination Buffer for Channel 0n** These bits indicate which channels have done a wrap-around of their destination buffer(s). 0_B No wrap-around occurred for channel 0n. 1_B A wrap-around occurred for channel 0n. This bit is reset by software by writing a 1 to INTCR.CWRP0n or CHRSTR.CH0n.

Field	Bits	Type	Description
WRPD1n (n = 0-7)	24+n	rh	**Wrap Destination Buffer for Channel 1n** These bits indicate which channels have done a wrap-around of their destination buffer(s). 0_B No wrap-around occurred for channel 1n. 1_B A wrap-around occurred for channel 1n. This bit is reset by software by writing a 1 to INTCR.CWRP1n or CHRSTR.CH1n.

The bits in the Interrupt Clear Register make it possible to reset the channel interrupt flags and the wrap buffer interrupt flags for DMA Channels mn.

DMA_INTCR
DMA Interrupt Clear Register **(058_H)** **Reset Value: 0000 0000$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CWRP17	**CWRP16**	**CWRP15**	**CWRP14**	**CWRP13**	**CWRP12**	**CWRP11**	**CWRP10**	**CWRP07**	**CWRP06**	**CWRP05**	**CWRP04**	**CWRP03**	**CWRP02**	**CWRP01**	**CWRP00**
w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CICH17	**CICH16**	**CICH15**	**CICH14**	**CICH13**	**CICH12**	**CICH11**	**CICH10**	**CICH07**	**CICH06**	**CICH05**	**CICH04**	**CICH03**	**CICH02**	**CICH01**	**CICH00**
w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w

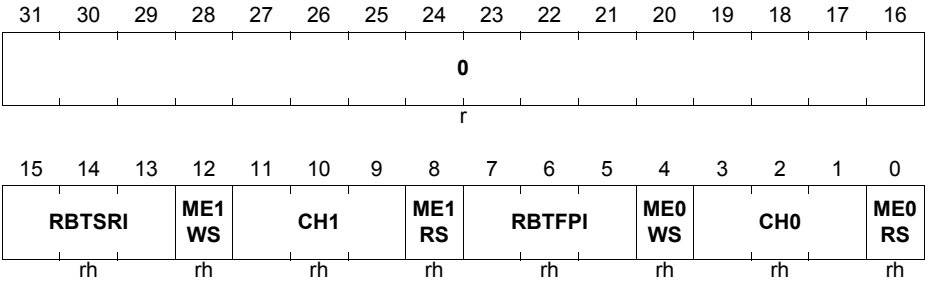
Field	Bits	Type	Description
CICH0n (n = 0-7)	n	w	**Clear Interrupt for DMA Channel 0n** These bits make it possible to reset the channel interrupt flags INTSR.ICH0n and INTSR.IPM0n of DMA channel 0n by software. 0_B No action. 1_B Bits INTSR.ICH0n and INTSR.IPM0n are reset.
CICH1n (n = 0-7)	8+n	w	**Clear Interrupt for DMA Channel 1n** These bits make it possible to reset the channel interrupt flags INTSR.ICH1n and INTSR.IPM1n of DMA channel 1n by software. 0_B No action. 1_B Bits INTSR.ICH1n and INTSR.IPM1n are reset.
CWRP0n (n = 0-7)	16+n	w	**Clear Wrap Buffer Interrupt for DMA Channel 0n** These bits make it possible to reset the wrap source buffer interrupt flag WRPSR.WRPS0n and the wrap destination buffer interrupt flag WRPSR.WRPD0n (both together) of DMA channel 0n by software. 0_B No action. 1_B Bits WRPSR.WRPS0n and WRPSR.WRPD0n are reset.

Field	Bits	Type	Description
CWRP1n (n = 0-7)	24+n	w	**Clear Wrap Buffer Interrupt for DMA Channel 1n** These bits make it possible to reset the wrap source buffer interrupt flag WRPSR.WRPS1n and the wrap destination buffer interrupt flag WRPSR.WRPD1n (both together) of DMA channel 1n by software. 0_B No action. 1_B Bits WRPSR.WRPS1n and WRPSR.WRPD1n are reset.

12.3.3 Move Engine Registers

The Move Engine Status Register is a read-only register that holds status information about the transaction handled by the Move Engines.

DMA_MESR
DMA Move Engine Status Register (030_H) Reset Value: $0000\ 0000_H$

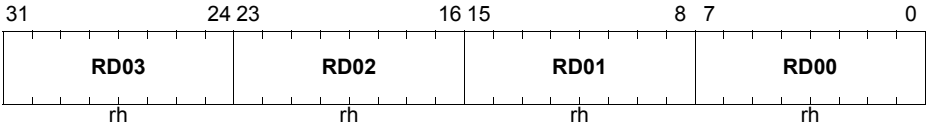


Field	Bits	Type	Description
ME0RS	0	rh	**Move Engine 0 Read Status** 0_B Move Engine 0 is not performing a read. 1_B Move Engine 0 is performing a read.
CH0	[3:1]	rh	**Reading Channel in Move Engine 0** This bit field indicates which channel number is currently being processed by the Move Engine 0.
ME0WS	4	rh	**Move Engine 0 Write Status** 0_B Move Engine 0 is not performing a write. 1_B Move Engine 0 is performing a write.

Field	Bits	Type	Description
RBTFPI	[7:5]	rh	**Read Buffer Trace for FPI Bus Interface** This bit field contains trace information from the buffer in the FPI Bus Interface. In the TC1798 it indicates the source of a bus access to the FPI Bus. 000_B Default value. 001_B DMA Move Engine 0 010_B DMA Move Engine 1 011_B MLI0 100_B MLI1 101_B Cerberus Other bit combinations are reserved. RBTFPI is useful for emulation purposes. It is not recommended to evaluate this bit field during normal operation of the TC1798.
ME1RS	8	rh	**Move Engine 1 Read Status** 0_B Move Engine 1 is not performing a read. 1_B Move Engine 1 is performing a read.
CH1	[11:9]	rh	**Reading Channel in Move Engine 1** These bit field indicates which channel number is currently being processed by the Move Engine 1.
ME1WS	12	rh	**Move Engine 1 Write Status** 0_B Move Engine 1 is not performing a write. 1_B Move Engine 1 is performing a write.
RBTSRI	[15:13]	rh	**Read Buffer Trace for SRI Bus Interface** This bit field contains trace information from the buffer in the SRI Bus Interface. In the TC1798, it indicates the source of a bus access to the SRI Bus. 000_B Default value 001_B DMA Move Engine 0 010_B DMA Move Engine 1 011_B MLI0 100_B MLI1 101_B Cerberus Other bit combinations are reserved. RBTSRI is useful for emulation purposes. It is not recommended to evaluate this bit field during normal operation of the TC1798.
0	[31:16]	r	**Reserved** Read as 0; should be written with 0.

The Move Engine 0 Read Register indicates the value that has just been read by Move Engine 0. The value in this register is compared to the bits in register ME0PR according to the bit fields CHCRmn.PATSEL.

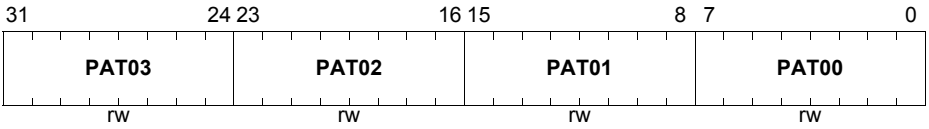
DMA_ME0R
DMA Move Engine 0 Read Register (034_H) **Reset Value: $0000\ 0000_H$**
DMA_ME1R
DMA Move Engine 1 Read Register (038_H) **Reset Value: $0000\ 0000_H$**



Field	Bits	Type	Description
RD00, RD01, RD02, RD03	[7:0], [15:8], [23:16], [31:24]	rh	**Read Value for Move Engine 0** Contains the 32-bit read data (four bytes RD0[3:0]) that is stored in the Move Engine 0 after each read move. The content of ME0R is overwritten after each read move of a DMA channel belonging to DMA Sub-block 0.

The Move Engine 0 Pattern Register contains the patterns (mask and/or compare bits) to be processed by the pattern detection logic in Move Engine 0.

DMA_ME0PR
DMA Move Engine 0 Pattern Register ($03C_H$) **Reset Value: $0000\ 0000_H$**
DMA_ME1PR
DMA Move Engine 1Pattern Register (040_H) **Reset Value: $0000\ 0000_H$**



Field	Bits	Type	Description
PAT00, PAT01, PAT02, PAT03	[7:0], [15:8], [23:16], [31:24]	rw	**Pattern for Move Engine 0** Determines up to four 8-bit compare patterns/mask patterns to be processed by the pattern detection logic in Move Engine 0. Depending on the pattern detection configuration (CHCR0n.PATSEL) and channel data width (CHCR0n.CHDW), the patterns are processed as bytes or half-words.

The DMA Move Engine 0 Access Enable Register controls the access protection. It enables/disables the address protection ranges x (x = 0-31) for Move Engine 0.

DMA_ME0AENR0
DMA Move Engine 0 Access Enable Register 0
(044_H) **Reset Value: $0000\ 0000_H$**

DMA_ME1AENR0
DMA Move Engine 1 Access Enable Register 0
($04C_H$) **Reset Value: $0000\ 0000_H$**

DMA_ME0AENR1
DMA Move Engine 0 Access Enable Register 1
($06C_H$) **Reset Value: $0000\ 0000_H$**

DMA_ME1AENR1
DMA Move Engine 1 Access Enable Register 1
(074_H) **Reset Value: $0000\ 0000_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
AEN 31	**AEN 30**	**AEN 29**	**AEN 28**	**AEN 27**	**AEN 26**	**AEN 25**	**AEN 24**	**AEN 23**	**AEN 22**	**AEN 21**	**AEN 20**	**AEN 19**	**AEN 18**	**AEN 17**	**AEN 16**
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AEN 15	**AEN 14**	**AEN 13**	**AEN 12**	**AEN 11**	**AEN 10**	**AEN 9**	**AEN 8**	**AEN 7**	**AEN 6**	**AEN 5**	**AEN 4**	**AEN 3**	**AEN 2**	**AEN 1**	**AEN 0**
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
AENx (x = 0-31)	x	rw	**Address Range x Enable** This bit enables the read and write capability of the DMA Move Engines for address range x (x = 0-31). 0_B DMA read and write moves to address range x are disabled 1_B DMA read and write moves to address range x are enabled If AENx = 0 for a read/write move to address range x, the read/write move is not executed and a source/destination Move Engine interrupt is generated.

*Note: See **Table 12-13** on **Page 12-111** for the TC1798-specific address range definition.*

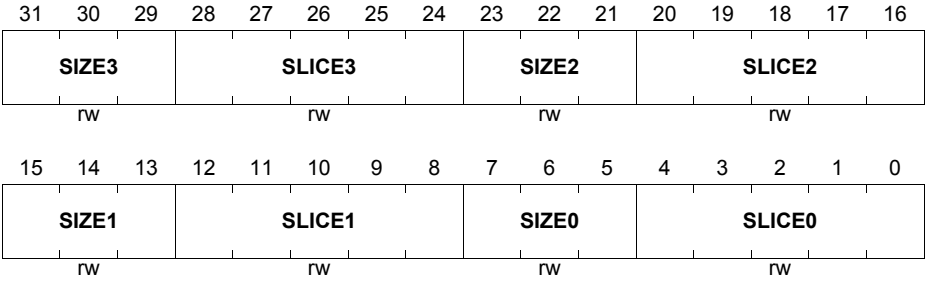
The DMA Move Engine 0 Access Range Register determines number and size of the sub-ranges for address range extension n (n = 0-3). See also **Figure 12-26** for bit field definitions.

DMA_ME0ARR0
DMA Move Engine 0 Access Range Register 0
(048_H) **Reset Value: 0000 0000_H**

DMA_ME1ARR0
DMA Move Engine 1 Access Range Register 0
(050_H) **Reset Value: 0000 0000_H**

DMA_ME0ARR1
DMA Move Engine 0 Access Range Register 1
(070_H) **Reset Value: 0000 0000_H**

DMA_ME1ARR1
DMA Move Engine 1 Access Range Register 1
(078_H) **Reset Value: 0000 0000_H**



Field	Bits	Type	Description
SLICE0	[4:0]	rw	**Address Slice 0** SLICE0 selects a specific sub-range within address range extension 0.
SIZE0	[7:5]	rw	**Address Size 0** SIZE0 determines the sub-range size within address range extension 0.
SLICE1	[12:8]	rw	**Address Slice 1** SLICE1 selects a specific sub-range within address range extension 1.
SIZE1	[15:13]	rw	**Address Size 1** SIZE1 determines the sub-range size within address range extension 1.

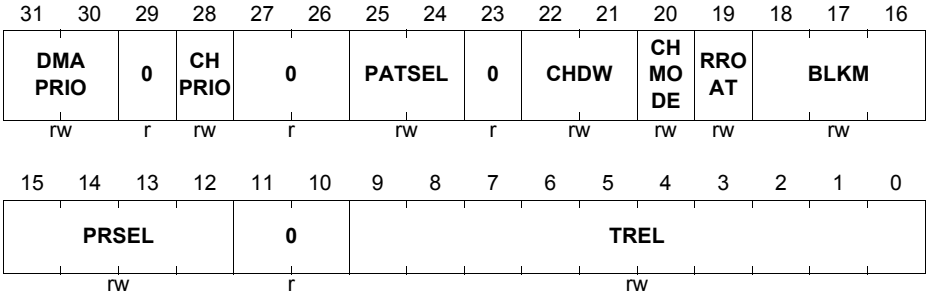
Field	Bits	Type	Description
SLICE2	[20:16]	rw	**Address Slice 2** SLICE2 selects a specific sub-range within address range extension 2.
SIZE2	[23:21]	rw	**Address Size 2** SIZE2 determines the sub-range size within address range extension 2.
SLICE3	[28:24]	rw	**Address Slice 3** SLICE3 selects a specific sub-range within address range extension 3.
SIZE3	[31:29]	rw	**Address Size 3** SIZE3 determines the sub-range size within address range extension 3.

*Note: See **Section 12.4.2** on **Page 12-111** for the TC1798-specific address range and address range extension definitions.*

12.3.4 Channel Control/Status Registers

The Channel Control Register for DMA channel mn contains its configuration and its control bits and bit fields.

DMA_CHCR0x (x = 0-7)
DMA Channel 0x Control Register (084_H+x*20_H) **Reset Value: 0000 0000_H**
DMA_CHCR1x (x = 0-7)
DMA Channel 1x Control Register (184_H+x*20_H) **Reset Value: 0000 0000_H**



Field	Bits	Type	Description
TREL	[9:0]	rw	**Transfer Reload Value** This bit field contains the number of DMA transfers for a DMA transaction of DMA channel mn. This10-bit transfer count value is loaded into CHSRmn.TCOUNT at the start of a DMA transaction (when TRSR.CHmn becomes set and CHSRmn.TCOUNT = 0). A write to CHSRmn.TREL during a running DMA transaction has no influence to the running DMA transaction. If CHSRmn.TREL = 0 or if CHSRmn.TREL = 1, CHSRmn.TCOUNT will be loaded with 1 when a new transaction is started (at least one DMA transfer must be executed per DMA transaction).

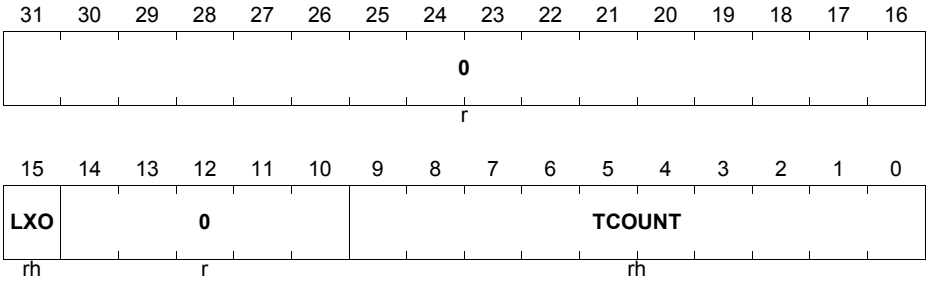
Field	Bits	Type	Description
PRSEL	[15:12]	rw	**Peripheral Request Select** This bit field controls the hardware request input multiplexer of DMA channel mn (see **Figure 12-6** on **Page 12-10**). 0000_B Input CHmn_REQI0 selected 0001_B Input CHmn_REQI1 selected 0010_B Input CHmn_REQI2 selected 0011_B Input CHmn_REQI3 selected 0100_B Input CHmn_REQI4 selected 0101_B Input CHmn_REQI5 selected 0110_B Input CHmn_REQI6 selected 0111_B Input CHmn_REQI7 selected 1000_B Input CHmn_REQI8 selected 1001_B Input CHmn_REQI9 selected 1010_B Input CHmn_REQI10 selected 1011_B Input CHmn_REQI11 selected 1100_B Input CHmn_REQI12 selected 1101_B Input CHmn_REQI13 selected 1110_B Input CHmn_REQI14 selected 1111_B Input CHmn_REQI15 selected
BLKM	[18:16]	rw	**Block Mode** BLKM determines the number of DMA moves executed during one DMA transfer. 000_B One DMA transfer has 1 DMA move 001_B One DMA transfer has 2 DMA move 010_B One DMA transfer has 4 DMA move 011_B One DMA transfer has 8 DMA move 100_B One DMA transfer has 16 DMA move Other bit combinations are reserved and must not be used. See also **Figure 12-10** on **Page 12-17**.
RROAT	19	rw	**Reset Request Only After Transaction** RROAT determines whether or not the TRSR.CHmn transfer request state flag is reset after each transfer. 0_B TRSR.CHmn is reset after each transfer. A transfer request is required for each transfer. 1_B TRSR.CHmn is reset when CHSRmn.TCOUNT = 0 after a transfer. One transfer request starts a complete DMA transaction

Field	Bits	Type	Description
CHMODE	20	rw	**Channel Operation Mode** CHMODE determines the reset condition for control bit TRSR.HTREmn of DMA channel mn. 0_B Single Mode operation is selected for DMA channel mn. After a transaction, DMA channel mn is disabled for further hardware requests (TRSR.HTREmn is reset by hardware) TRSR.HTREmn must be set again by software for starting a new transaction. 1_B Continuous Mode operation is selected for DMA channel mn. After a transaction, bit TRSR.HTREmn remains set
CHDW	[22:21]	rw	**Channel Data Width** CHDW determines the data width for the read and write moves of DMA channel mn. 00_B 8-bit (byte) data width for moves selected 01_B 16-bit (half-word) data width for moves selected 10_B 32-bit (word) data width for moves selected 11_B Reserved
PATSEL	[25:24]	rw	**Pattern Select** This bit field selects the mode of the pattern detection logic. Depending on the channel data width, PATSEL selects different pattern detection configurations. If pattern detection is enabled (PATSEL not equal 00_B), the pattern detection interrupt line will be activated on the selected pattern match. **8-bit channel data width (CHDW = 00_B):** Selected pattern detection configuration see **Table 12-4** on **Page 12-40**. **16-bit channel data width (CHDW = 01_B):** Selected pattern detection configuration see **Table 12-5** on **Page 12-41**. **32-bit channel data width (CHDW = 10_B):** Selected pattern detection configuration see **Table 12-6** on **Page 12-43**.

Field	Bits	Type	Description
CHPRIO	28	rw	**Channel Priority** CHPRIO determines the priority of DMA channel n for the Move Engine m internal channel arbitration. This priority is used for the case when multiple channels of Move Engine m are triggered in parallel. 0_B DMA channel mn has a low channel priority 1_B DMA channel mn has a high channel priority
DMAPRIO	[31:30]	rw	**DMA Priority** This bit determines the DMA the request priority that is used when a move operation related to channel mn is requesting an On Chip Bus. This bit has no effect in channel prioritization inside the Move Engine m in. 00_B Low priority selected 01_B Medium priority selected 10_B Reserved 11_B High priority selected
0	[11:10], 23, [27:26], 29	r	**Reserved** Read as 0; should be written with 0.

The Channel Status Register contains the current transfer count and a pattern detection compare result.

DMA_CHSR0x (x = 0-7)
DMA Channel 0x Status Register (080_H+x*20_H) **Reset Value: 0000 0000_H**
DMA_CHSR1x (x = 0-7)
DMA Channel 1x Status Register (180_H+x*20_H) **Reset Value: 0000 0000_H**

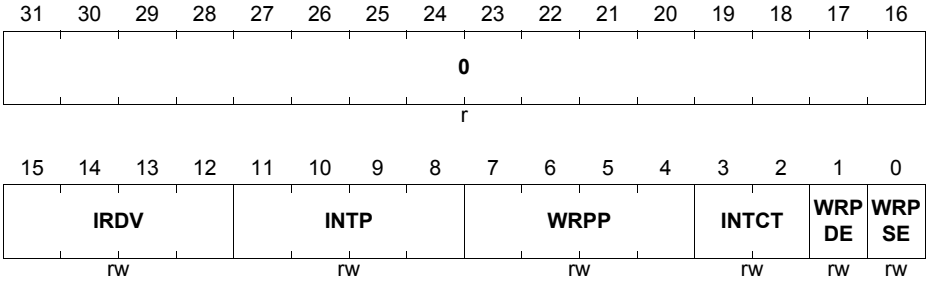


Field	Bits	Type	Description
TCOUNT	[9:0]	rh	**Transfer Count Status** TCOUNT holds the actual value of the DMA transfer count for DMA channel mx. TCOUNT is loaded with the value of CHCRmx.TREL when TRSR.CHmx becomes set (and TCOUNT = 0). After each DMA transfer, TCOUNT is decremented by 1.
LXO	15	rh	**Old Value of Pattern Detection** This bit contains the compare result of a pattern compare operation when 8-bit or 16-bit data width is selected. 8-bit data width: see **Table 12-4** and **Figure 12-23** 16-bit data width: see **Table 12-5** and **Figure 12-24** 0_B The corresponding pattern compare operation did not find a pattern match on the last move 1_B The corresponding pattern compare operation found a pattern match at the last move
0	[14:10], [31:16]	r	**Reserved** Read as 0; should be written with 0.

The Channel Interrupt Control Register controls the interrupts generation.

DMA_CHICR0x (x = 0-7)
DMA Channel 0x Interrupt Control Register
(088_H+x*20_H) **Reset Value: 0000 0000_H**

DMA_CHICR1x (x = 0-7)
DMA Channel 1x Interrupt Control Register
(188_H+x*20_H) **Reset Value: 0000 0000_H**



Field	Bits	Type	Description
WRPSE	0	rw	**Wrap Source Enable** 0_B Wrap source buffer interrupt disabled 1_B Wrap source buffer interrupt enabled
WRPDE	1	rw	**Wrap Destination Enable** 0_B Wrap destination buffer interrupt disabled 1_B Wrap destination buffer interrupt enabled
INTCT	[3:2]	rw	**Interrupt Control** 00_B No interrupt will be generated on changing the TCOUNT value. The bit INTSR.ICHmx is set when TCOUNT equals IRDV. 01_B No interrupt will be generated on changing the TCOUNT value. The bit INTSR.ICHmx is set when TCOUNT is decremented 10_B An interrupt is generated and bit INTSR.ICHmx is set each time TCOUNT equals IRDV 11_B Interrupt is generated and bit INTSR.ICHmx is set each time TCOUNT is decremented *Note: see **Figure 12-17**.*

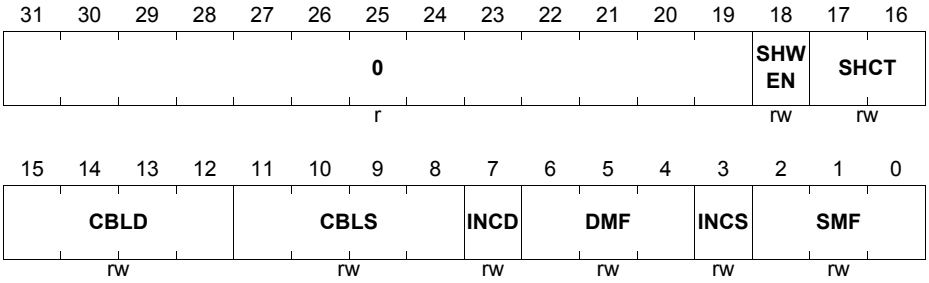
Field	Bits	Type	Description
WRPP	[7:4]	rw	**Wrap Pointer** WRPP determines the number n (n = 0-15) of the service request output SRn that becomes active on a wrap buffer interrupt. 0000_B SR0 selected for channel mx wrap buffer interrupt 0001_B SR1 selected for channel mx wrap buffer interrupt …$_B$ … 1111_B SR15 selected for channel mx wrap buffer interrupt *Note: In the TC1798, SR[7:0] are connected to interrupt nodes. SR[15:8] are used as DMA channel request inputs (**Page 12-101**).*
INTP	[11:8]	rw	**Interrupt Pointer** INTP determines the number n (n = 0-15) of the service request output SRn that becomes active on a channel interrupt. 0000_B SR0 selected for channel mx interrupt 0001_B SR1 selected for channel mx interrupt …$_B$ … 1111_B SR15 selected for channel mx interrupt *Note: In the TC1798, SR[7:0] are connected to interrupt nodes. SR[15:8] are used as DMA channel request inputs (**Page 12-101**).*
IRDV	[15:12]	rw	**Interrupt Raise Detect Value** These bits specify the value of CHSRmx.TCOUNT for which the Interrupt Threshold Limit should be raised.
0	[31:16]	r	**Reserved** Read as 0; should be written with 0.

Note: The interrupt node of the wrap-around interrupts is shared with the pattern match interrupt. In order to support interrupt generation in case of a pattern match, the wrap-around interrupt should be disabled. If the wrap-around interrupts are used, the pattern match interrupt should not be used. The settings are independent for each DMA channel.

The Address Control Register controls how source and destination addresses are updated after a DMA move. Furthermore, it determines whether or not a source or destination address register update is shadowed.

DMA_ADRCR0x (x = 0-7)
DMA Channel 0x Address Control Register
($08C_H$+x*20_H) **Reset Value: 0000 0000_H**

DMA_ADRCR1x (x = 0-7)
DMA Channel 1x Address Control Register
($18C_H$+x*20_H) **Reset Value: 0000 0000_H**



Field	Bits	Type	Description
SMF	[2:0]	rw	**Source Address Modification Factor** This bit field and the data width as defined in CHCRmx.CHDW determine an address offset value by which the source address is modified after each DMA move. See also **Table 12-10**. 000_B Address offset is 1 x CHCRmx.CHDW 001_B Address offset is 2 x CHCRmx.CHDW 010_B Address offset is 4 x CHCRmx.CHDW 011_B Address offset is 8 x CHCRmx.CHDW 100_B Address offset is 16 x CHCRmx.CHDW 101_B Address offset is 32 x CHCRmx.CHDW 110_B Address offset is 64 x CHCRmx.CHDW 111_B Address offset is 128 x CHCRmx.CHDW

Field	Bits	Type	Description
INCS	3	rw	**Increment of Source Address** This bit determines whether the address offset as selected by SMF will be added to or subtracted from the source address after each DMA move. The source address is not modified if CBLS = 0000_B. 0_B Address offset will be subtracted 1_B Address offset will be added.
DMF	[6:4]	rw	**Destination Address Modification Factor** This bit field and the data width as defined in CHCRmx.CHDW determines an address offset value by which the destination address is modified after each DMA move. The destination address is not modified if CBLD = 0000_B. See also **Table 12-10**. 000_B Address offset is 1 x CHDW 001_B Address offset is 2 x CHDW 010_B Address offset is 4 x CHDW 011_B Address offset is 8 x CHDW 100_B Address offset is 16 x CHDW 101_B Address offset is 32 x CHDW 110_B Address offset is 64 x CHDW 111_B Address offset is 128 x CHDW
INCD	7	rw	**Increment of Destination Address** This bit determines whether the address offset as selected by DMF will be added to or subtracted from the destination address after each DMA move. The destination address is not modified if CBLD = 0000_B. 0_B Address offset will be subtracted 1_B Address offset will be added

Field	Bits	Type	Description
CBLS	[11:8]	rw	**Circular Buffer Length Source** This bit field determines which part of the 32-bit source address register remains unchanged and is not updated after a DMA move operation (see also **Section 12.2.4.7**). Therefore, CBLS also determines the size of the circular source buffer. 0000_B Source address SADR[31:0] is not updated 0001_B Source address SADR[31:1] is not updated 0010_B Source address SADR[31:2] is not updated 0011_B Source address SADR[31:3] is not updated $\cdots_B$ ... 1110_B Source address SADR[31:14] is not updated 1111_B Source address SADR[31:15] is not updated
CBLD	[15:12]	rw	**Circular Buffer Length Destination** This bit field determines which part of the 32-bit destination address register remains unchanged and is not updated after a DMA move operation (see also **Page 12-19**). Therefore, CBLD also determines the size of the circular destination buffer. 0000_B Destination address DADR[31:0] is not updated 0001_B Destination address DADR[31:1] is not updated 0010_B Destination address DADR[31:2] is not updated 0011_B Destination address DADR[31:3] is not updated $\cdots_B$ ... 1110_B Destination address DADR[31:14] is not updated 1111_B Destination address DADR[31:15] is not updated

Field	Bits	Type	Description
SHCT	[17:16]	rw	**Shadow Control** This bit field determines whether an address is transferred into the shadow address register when writing to source or destination address register. 00_B Shadow address register not used. Source and destination address register are written directly 01_B Shadow address register used for source address buffering. When writing to SADRmx, the address is buffered in SHADRmx and transferred to SADRmx with the start of the next DMA transaction 10_B Shadow address register used for destination address buffering. When writing to DADRmx, the address is buffered in SHADRmx and transferred to DADRmx with the start of the next DMA transaction 11_B Reserved In case of SHCT = 01_B or 10_B, SHCT must not be changed until the next DMA transaction has been started.
SHWEN	18	rw	**Shadow Address Register Write Enable** This bit determines whether the shadow address register SHADRmx is read only and automatically set to 0000 0000_H or if the shadow register can also be directly written and not modified when and shadow transfer takes place. 0_B Shadow address register is read only and the value stored in the SHADRmx is automatically set to 0000 0000_H when the shadow transfer takes place 1_B Shadow address register SHADRmx can be read and can be directly written. The value stored in the SHADRmx is not automatically modified when the shadow transfer takes place
0	[31:19]	r	**Reserved** Read as 0; should be written with 0.

Table 12-10 shows the offset values that are added or subtracted to/from a source or destination address register after a DMA move. Bit field SMF and bit INCS determine the offset value for the source address. Bit field DMF and bit INCD determine the offset value for the destination address.

Table 12-10 Address Offset Calculation Table

CHCRmn.CHDW = 00_B (8-bit Data Width)			CHCRmn.CHDW = 01_B (16-bit Data Width)			CHCRmn.CHDW = 10_B (32-bit Data Width)		
SMF DMF	**INCS INCD**	**Address Offset**	**SMF DMF**	**INCS INCD**	**Address Offset**	**SMF DMF**	**INCS INCD**	**Address Offset**
000_B	0	-1	000_B	0	-2	000_B	0	-4
	1	+1		1	+2		1	+4
001_B	0	-2	001_B	0	-4	001_B	0	-8
	1	+2		1	+4		1	+8
010_B	0	-4	010_B	0	-8	010_B	0	-16
	1	+4		1	+8		1	+16
011_B	0	-8	011_B	0	-16	011_B	0	-32
	1	+8		1	+16		1	+32
100_B	0	-16	100_B	0	-32	100_B	0	-64
	1	+16		1	+32		1	+64
101_B	0	-32	101_B	0	-64	101_B	0	-128
	1	+32		1	+64		1	+128
110_B	0	-64	110_B	0	-128	110_B	0	-256
	1	+64		1	+128		1	+256
111_B	0	-128	111_B	0	-256	111_B	0	-512
	1	+128		1	+256		1	+512

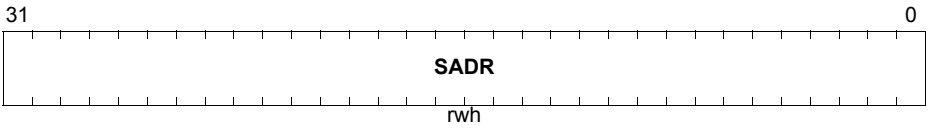
Note: CHCRmn.CHDW = 11_B is reserved and should not be used.

12.3.5 Channel Address Registers

The Source Address Register contains the 32-bit source address. If a DMA channel mn is active, SADRmn is updated continuously (if programmed) and shows the actual source address that is used for read moves within DMA transfers.

DMA_SADR0x (x = 0-7)
DMA Channel 0x Source Address Register
(090_H+x*20_H) **Reset Value: 0000 0000_H**

DMA_SADR1x (x = 0-7)
DMA Channel 1x Source Address Register
(190_H+x*20_H) **Reset Value: 0000 0000_H**



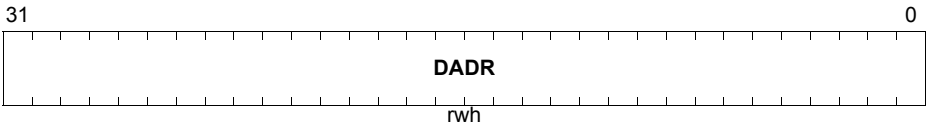
Field	Bits	Type	Description
SADR	[31:0]	rwh	**Source Start Address** This bit field holds the actual 32-bit source address of DMA channel mx that is used for read moves.

A write to SADRmn is executed directly only when the DMA channel mn is inactive (CHSRmn.TCOUNT = 0 and TRSR.CHmn = 0). If DMA channel mn is active when writing to SADRmn, the source address will not be written into SADRmn directly but will be buffered in the shadow register SHADRmn until the start of the next DMA transaction. During this shadowed address register operation, bit field ADRCRmn.SHCT must be set to 01_B.

The Destination Address Register contains the 32-bit destination address. If a DMA channel is active, DADRmn is updated continuously (if programmed) and shows the actual destination address that is used for write moves within DMA transfers.

DMA_DADR0x (x = 0-7)
DMA Channel 0x Destination Address Register
(094_H+x*20_H) **Reset Value: 0000 0000_H**

DMA_DADR1x (x = 0-7)
DMA Channel 1x Destination Address Register
(194_H+x*20_H) **Reset Value: 0000 0000_H**



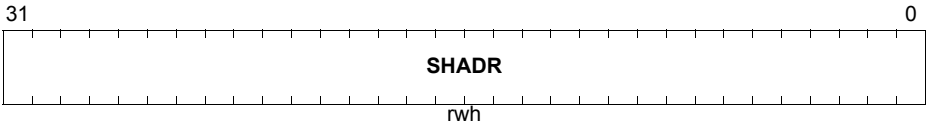
Field	Bits	Type	Description
DADR	[31:0]	rwh	**Destination Address** This bit field holds the actual 32-bit destination address of DMA channel mx that is used for write moves.

A write to DADRmn is executed directly only when the DMA channel mn is inactive (CHSRmn.TCOUNT = 0 and TRSR.CHmn = 0). If DMA channel mn is active when writing to DADRmn, the source address will not be written into DADRmn directly but will be buffered in the shadow register SHADRmn until the start of the next DMA transaction. During this shadowed address register operation, bit field ADRCRmn.SHCT must be set to 10_B.

The Shadow Address Register holds the shadowed source or destination address before it is written into the source or destination address register. SHADRmn can be read only.

DMA_SHADR0x (x = 0-7)
DMA Channel 0x Shadow Address Register
(098_H+x*20_H) **Reset Value: 0000 0000_H**

DMA_SHADR1x (x = 0-7)
DMA Channel 1x Shadow Address Register
(198_H+x*20_H) **Reset Value: 0000 0000_H**



Field	Bits	Type	Description
SHADR	[31:0]	rwh	**Shadowed Address** This bit field holds the shadowed 32-bit source or destination address of DMA channel mx.

SHADRmn is written when source or destination address buffering is selected (ADRCRmn.SHCT = 01_B or ADRCRmn.SHCT = 10_B) and a transaction is running. While the shadow mechanism is disabled, SHADR is set to 0000 0000_H.

If ADRCRmn.SHWEN = 0 the value stored in the SHADR is automatically set to 0000 0000_H when the shadow transfer takes place. The user can read the shadow register in order to detect if the shadow transfer has already taken place. If the value in SHADR is 0000 0000_H, no shadow transfer can take place and the corresponding address register is modified according to the circular buffer rules.

If ADRCRmn.SHWEN = 1 shadow register SHADRmn can be directly written. The value stored in the SHADRmn is not modified when the shadow transfer takes place, the shadow mechanism remains active and the shadow transfer will be repeated until Channel mn is reset or until the value in SHADR is 0000 0000_H, is written into the shadow register.

12.4 DMA Module Implementation

This section describes the TC1798 DMA module interfaces with the clock control, interrupt control, and address decoding.

Chapter 12-28 shows the TC1798-specific implementation details and interconnections of the DMA module. The DMA module is supplied with a separate clock control, address decoding, interrupt control, and the request input wiring matrix.

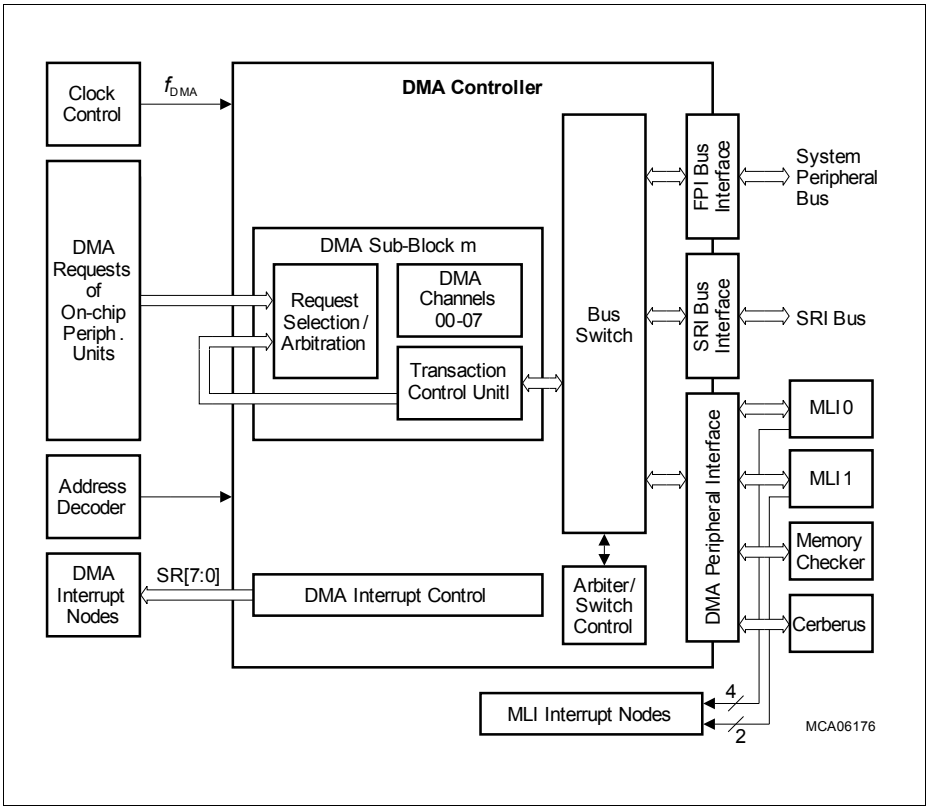


Figure 12-28 DMA Module Implementation and Interconnections

The request sources of the peripheral modules (ADC0, MSC0, MLI0/1, FADC, MultiCAN, and SCU) are associated with Interrupt Node Pointers and individual interrupt enable bits. As a result, each of the internal requests of a module can be routed independently to any of the interrupt output lines (INT_Ox) of the module.

12.4.1 DMA Request Wiring Matrix

The DMA request input lines of each DMA channel within DMA Sub-Block 0 and DMA Sub-Block 1 are connected to request output lines from the peripheral modules according to **Table 12-11**.

Table 12-11 DMA Request Assignment for DMA Sub-Block 0

DMA Channel	DMA Request Line	DMA Requesting Unit	Selected by
00	DMA_SR08	DMA(INT_O08)	CHCR00.PRSEL = 0000_B
	IOUT0	SCU (ERU)	CHCR00.PRSEL = 0001_B
	FADC_SR00	FADC	CHCR00.PRSEL = 0010_B
	ADC_SR00	ADC	CHCR00.PRSEL = 0011_B
	SSC0_RDR	SSC0	CHCR00.PRSEL = 0100_B
	ASC0_RDR	ASC0	CHCR00.PRSEL = 0101_B
	CAN_INT_O0	MultiCAN	CHCR00.PRSEL = 0110_B
	MLI0_SR4	MLI0	CHCR00.PRSEL = 0111_B
	STMIRQ0	STM	CHCR00.PRSEL = 1000_B
	GPTA_TRIG00	GPTA[1)]	CHCR00.PRSEL = 1001_B
	GPTA_TRIG10	GPTA[1)]	CHCR00.PRSEL = 1010_B
	INT1SRC	ERAY	CHCR00.PRSEL = 1011_B
	IBUSY	ERAY	CHCR00.PRSEL = 1100_B
	SSC2_RDR	SSC2	CHCR00.PRSEL = 1101_B
	Reserved[2)]	-	CHCR00.PRSEL = 1110_B
	MLI1_SR4	MLI1	CHCR00.PRSEL = 1111_B
01	DMA_SR09	DMA(INT_O09)	CHCR01.PRSEL = 0000_B
	IOUT1	SCU (ERU)	CHCR01.PRSEL = 0001_B
	FADC_SR01	FADC	CHCR01.PRSEL = 0010_B
	ADC_SR01	ADC	CHCR01.PRSEL = 0011_B
	SSC1_RDR	SSC1	CHCR01.PRSEL = 0100_B
	ASC1_RDR	ASC1	CHCR01.PRSEL = 0101_B
	CAN_INT_O1	MultiCAN	CHCR01.PRSEL = 0110_B
	MLI0_SR5	MLI0	CHCR01.PRSEL = 0111_B
	STMIRQ0	STM	CHCR01.PRSEL = 1000_B

Table 12-11 DMA Request Assignment for DMA Sub-Block 0 (cont'd)

DMA Channel	DMA Request Line	DMA Requesting Unit	Selected by
	GPTA_TRIG01	GPTA[1)]	CHCR01.PRSEL = 1001_B
	GPTA_TRIG11	GPTA[1)]	CHCR01.PRSEL = 1010_B
	TINT0SRC	ERAY	CHCR01.PRSEL = 1011_B
	Reserved[2)]	-	CHCR01.PRSEL = 1100_B
	CCU60_SR0	CCU60_SR0	CHCR01.PRSEL = 1101_B
	Reserved[2)]	-	CHCR01.PRSEL = 1110_B
	MLI1_SR5	MLI1	CHCR01.PRSEL = 1111_B
02	DMA_SR10	DMA(INT_O10)	CHCR02.PRSEL = 0000_B
	IOUT2	SCU (ERU)	CHCR02.PRSEL = 0001_B
	FADC_SR02	FADC	CHCR02.PRSEL = 0010_B
	ADC_SR02	ADC	CHCR02.PRSEL = 0011_B
	SSC0_TDR	SSC0	CHCR02.PRSEL = 0100_B
	ASC0_TDR	ASC0	CHCR02.PRSEL = 0101_B
	MSC0_SR2	MSC0	CHCR02.PRSEL = 0110_B
	MLI0_SR6	MLI0	CHCR02.PRSEL = 0111_B
	STMIRQ0	STM	CHCR02.PRSEL = 1000_B
	GPTA_TRIG02	GPTA[1)]	CHCR02.PRSEL = 1001_B
	GPTA_TRIG12	GPTA[1)]	CHCR02.PRSEL = 1010_B
	NDAT1SRC	ERAY	CHCR02.PRSEL = 1011_B
	ASC0_TBDR	ASC0	CHCR02.PRSEL = 1100_B
	SSC2_TDR	SSC2	CHCR02.PRSEL = 1101_B
	MSC1_SR2	MSC1	CHCR02.PRSEL = 1110_B
	MLI1_SR6	MLI1	CHCR02.PRSEL = 1111_B
03	DMA_SR11	DMA(INT_O11)	CHCR03.PRSEL = 0000_B
	IOUT3	SCU (ERU)	CHCR03.PRSEL = 0001_B
	FADC_SR03	FADC	CHCR03.PRSEL = 0010_B
	ADC_SR03	ADC	CHCR03.PRSEL = 0011_B
	SSC1_TDR	SSC1	CHCR03.PRSEL = 0100_B
	ASC1_TDR	ASC1	CHCR03.PRSEL = 0101_B
	MSC0_SR3	MSC0	CHCR03.PRSEL = 0110_B

Table 12-11 DMA Request Assignment for DMA Sub-Block 0 (cont'd)

DMA Channel	DMA Request Line	DMA Requesting Unit	Selected by
	MLI0_SR7	MLI0	CHCR03.PRSEL = 0111_B
	STMIRQ0	STM	CHCR03.PRSEL = 1000_B
	GPTA_TRIG03	GPTA[1)]	CHCR03.PRSEL = 1001_B
	GPTA_TRIG13	GPTA[1)]	CHCR03.PRSEL = 1010_B
	MBSC1SRC	ERAY	CHCR03.PRSEL = 1011_B
	ASC1_TBDR	ASC1	CHCR03.PRSEL = 1100_B
	Reserved[2)]	-	CHCR03.PRSEL = 1101_B
	MSC1_SR3	MSC1	CHCR03.PRSEL = 1110_B
	MLI1_SR7	MLI1	CHCR03.PRSEL = 1111_B
04	DMA_SR12	DMA(INT_O12)	CHCR04.PRSEL = 0000_B
	IOUT0	SCU (ERU)	CHCR04.PRSEL = 0001_B
	FADC_SR00	FADC	CHCR04.PRSEL = 0010_B
	ADC_SR04	ADC	CHCR04.PRSEL = 0011_B
	SSC0_TDR	SSC0	CHCR04.PRSEL = 0100_B
	ASC0_TDR	ASC0	CHCR04.PRSEL = 0101_B
	MSC0_SR2	MSC0	CHCR04.PRSEL = 0110_B
	MLI0_SR4	MLI0	CHCR04.PRSEL = 0111_B
	STMIRQ0	STM	CHCR04.PRSEL = 1000_B
	GPTA_TRIG04	GPTA[1)]	CHCR04.PRSEL = 1001_B
	GPTA_TRIG14	GPTA[1)]	CHCR04.PRSEL = 1010_B
	INT1SRC	ERAY	CHCR04.PRSEL = 1011_B
	ASC0_TBDR	ASC0	CHCR04.PRSEL = 1100_B
	OBUSY	ERAY	CHCR04.PRSEL = 1101_B
	MSC1_SR2	MSC1	CHCR04.PRSEL = 1110_B
	MLI1_SR4	MLI1	CHCR04.PRSEL = 1111_B
05	DMA_SR13	DMA(INT_O13)	CHCR05.PRSEL = 0000_B
	IOUT1	SCU (ERU)	CHCR05.PRSEL = 0001_B
	FADC_SR01	FADC	CHCR05.PRSEL = 0010_B
	ADC_SR05	ADC	CHCR05.PRSEL = 0011_B
	SSC1_TDR	SSC1	CHCR05.PRSEL = 0100_B

Table 12-11 DMA Request Assignment for DMA Sub-Block 0 (cont'd)

DMA Channel	DMA Request Line	DMA Requesting Unit	Selected by
	ASC1_TDR	ASC1	CHCR05.PRSEL = 0101_B
	MSC0_SR3	MSC0	CHCR05.PRSEL = 0110_B
	MLI0_SR5	MLI0	CHCR05.PRSEL = 0111_B
	STMIRQ0	STM	CHCR05.PRSEL = 1000_B
	GPTA_TRIG05	GPTA[1)]	CHCR05.PRSEL = 1001_B
	GPTA_TRIG15	GPTA[1)]	CHCR05.PRSEL = 1010_B
	TINT1SRC	ERAY	CHCR05.PRSEL = 1011_B
	ASC1_TBDR	ASC1	CHCR05.PRSEL = 1100_B
	CCU61_SR0	CCU61	CHCR05.PRSEL = 1101_B
	MSC1_SR3	MSC1	CHCR05.PRSEL = 1110_B
	MLI1_SR5	MLI1	CHCR05.PRSEL = 1111_B
06	DMA_SR14	DMA(INT_O14)	CHCR06.PRSEL = 0000_B
	IOUT2	SCU (ERU)	CHCR06.PRSEL = 0001_B
	FADC_SR02	FADC	CHCR06.PRSEL = 0010_B
	ADC_SR06	ADC	CHCR06.PRSEL = 0011_B
	SSC0_RDR	SSC0	CHCR06.PRSEL = 0100_B
	ASC0_RDR	ASC0	CHCR06.PRSEL = 0101_B
	CAN_INT_O0	MultiCAN	CHCR06.PRSEL = 0110_B
	MLI0_SR6	MLI0	CHCR06.PRSEL = 0111_B
	STMIRQ0	STM	CHCR06.PRSEL = 1000_B
	GPTA_TRIG06	GPTA[1)]	CHCR06.PRSEL = 1001_B
	GPTA_TRIG16	GPTA[1)]	CHCR06.PRSEL = 1010_B
	NDAT1SRC	ERAY	CHCR06.PRSEL = 1011_B
	SSC3_TDR	SSC3	CHCR06.PRSEL = 1100_B
	CCU62_SR0	CCU62	CHCR06.PRSEL = 1101_B
	ADC_SR08	ADC	CHCR06.PRSEL = 1110_B
	MLI1_SR6	MLI1	CHCR06.PRSEL = 1111_B
07	DMA_SR15	DMA(INT_O15)	CHCR07.PRSEL = 0000_B
	IOUT3	SCU (ERU)	CHCR07.PRSEL = 0001_B
	FADC_SR03	FADC	CHCR07.PRSEL = 0010_B

Table 12-11 DMA Request Assignment for DMA Sub-Block 0 (cont'd)

DMA Channel	DMA Request Line	DMA Requesting Unit	Selected by
	ADC_SR07	ADC	CHCR07.PRSEL = 0011_B
	SSC1_RDR	SSC1	CHCR07.PRSEL = 0100_B
	ASC1_RDR	ASC1	CHCR07.PRSEL = 0101_B
	CAN_INT_O1	MultiCAN	CHCR07.PRSEL = 0110_B
	MLI0_SR7	MLI0	CHCR07.PRSEL = 0111_B
	STMIRQ0	STM	CHCR07.PRSEL = 1000_B
	GPTA_TRIG07	GPTA[1)]	CHCR07.PRSEL = 1001_B
	GPTA_TRIG17	GPTA[1)]	CHCR07.PRSEL = 1010_B
	MBSC1SRC	ERAY	CHCR07.PRSEL = 1011_B
	SSC3_RDR	SSC3	CHCR07.PRSEL = 1100_B
	CCU63_SR0	CCU63	CHCR07.PRSEL = 1101_B
	ADC_SR09	ADC	CHCR07.PRSEL = 1110_B
	MLI1_SR7	MLI1	CHCR07.PRSEL = 1111_B

1) GPTA_TRIG signals are per default level sensitive signals while a DMA channel is activated with every active request signal cycle. The DMA internal positive edge detection will generate the channel request with the rising edge of the GPTA_TRIG signal, if selected. If channel requests for the positive and/or negative GPTA_TRIG signal is required, this can be realized either via the ERU (some GPTA_TRIG signals are mapped to it) or via GPTA programming by using additional GPTA cells.

2) Reserved PRSEL combinations do not result to DMA Channel requests.

Table 12-12 DMA Request Assignment for DMA Sub-Block 1

DMA Channel	DMA Request Line	DMA Requesting Unit	Selected by
10	DMA_SR08	DMA(INT_O08)	CHCR10.PRSEL = 0000_B
	IOUT0	SCU (ERU)	CHCR10.PRSEL = 0001_B
	FADC_SR00	FADC	CHCR10.PRSEL = 0010_B
	ADC_SR00	ADC	CHCR10.PRSEL = 0011_B
	SSC0_RDR	SSC0	CHCR10.PRSEL = 0100_B
	ASC0_RDR	ASC0	CHCR10.PRSEL = 0101_B
	CAN_INT_O0	MultiCAN	CHCR10.PRSEL = 0110_B
	MLI0_SR4	MLI0	CHCR10.PRSEL = 0111_B
	STMIRQ0	STM	CHCR10.PRSEL = 1000_B

Table 12-12 DMA Request Assignment for DMA Sub-Block 1 (cont'd)

DMA Channel	DMA Request Line	DMA Requesting Unit	Selected by
	GPTA_TRIG00	GPTA[1)]	CHCR10.PRSEL = 1001_B
	GPTA_TRIG10	GPTA[1)]	CHCR10.PRSEL = 1010_B
	INT1SRC	ERAY	CHCR10.PRSEL = 1011_B
	IBUSY	ERAY	CHCR10.PRSEL = 1100_B
	SSC2_RDR	SSC2	CHCR10.PRSEL = 1101_B
	Reserved[2)]	-	CHCR10.PRSEL = 1110_B
	MLI1_SR4	MLI1	CHCR10.PRSEL = 1111_B
11	DMA_SR09	DMA(INT_O09)	CHCR11.PRSEL = 0000_B
	IOUT1	SCU (ERU)	CHCR11.PRSEL = 0001_B
	FADC_SR01	FADC	CHCR11.PRSEL = 0010_B
	ADC_SR01	ADC	CHCR11.PRSEL = 0011_B
	SSC1_RDR	SSC1	CHCR11.PRSEL = 0100_B
	ASC1_RDR	ASC1	CHCR11.PRSEL = 0101_B
	CAN_INT_O1	MultiCAN	CHCR11.PRSEL = 0110_B
	MLI0_SR5	MLI0	CHCR11.PRSEL = 0111_B
	STMIRQ0	STM	CHCR11.PRSEL = 1000_B
	GPTA_TRIG01	GPTA[1)]	CHCR11.PRSEL = 1001_B
	GPTA_TRIG11	GPTA[1)]	CHCR11.PRSEL = 1010_B
	TINT0SRC	ERAY	CHCR11.PRSEL = 1011_B
	Reserved[2)]	-	CHCR11.PRSEL = 1100_B
	CCU60_SR0	CCU60	CHCR11.PRSEL = 1101_B
	Reserved[2)]	-	CHCR11.PRSEL = 1110_B
	MLI1_SR5	MLI1	CHCR11.PRSEL = 1111_B
12	DMA_SR10	DMA(INT_O10)	CHCR12.PRSEL = 0000_B
	IOUT2	SCU (ERU)	CHCR12.PRSEL = 0001_B
	FADC_SR02	FADC	CHCR12.PRSEL = 0010_B
	ADC_SR02	ADC	CHCR12.PRSEL = 0011_B
	SSC0_TDR	SSC0	CHCR12.PRSEL = 0100_B
	ASC0_TDR	ASC0	CHCR12.PRSEL = 0101_B
	MSC0_SR2	MSC0	CHCR12.PRSEL = 0110_B

Table 12-12 DMA Request Assignment for DMA Sub-Block 1 (cont'd)

DMA Channel	DMA Request Line	DMA Requesting Unit	Selected by
	MLI0_SR6	MLI0	CHCR12.PRSEL = 0111_B
	STMIRQ0	STM	CHCR12.PRSEL = 1000_B
	GPTA_TRIG02	GPTA[1)]	CHCR12.PRSEL = 1001_B
	GPTA_TRIG12	GPTA[1)]	CHCR12.PRSEL = 1010_B
	NDAT1SRC	ERAY	CHCR12.PRSEL = 1011_B
	ASC0_TBDR	ASC0	CHCR12.PRSEL = 1100_B
	SSC2_TDR	SSC2	CHCR12.PRSEL = 1101_B
	MSC1_SR2	MSC1	CHCR12.PRSEL = 1110_B
	MLI1_SR6	MLI1	CHCR12.PRSEL = 1111_B
13	DMA_SR11	DMA(INT_O11)	CHCR13.PRSEL = 0000_B
	IOUT3	SCU (ERU)	CHCR13.PRSEL = 0001_B
	FADC_SR03	FADC	CHCR13.PRSEL = 0010_B
	ADC_SR03	ADC	CHCR13.PRSEL = 0011_B
	SSC1_TDR	SSC1	CHCR13.PRSEL = 0100_B
	ASC1_TDR	ASC1	CHCR13.PRSEL = 0101_B
	MSC0_SR3	MSC0	CHCR13.PRSEL = 0110_B
	MLI0_SR7	MLI0	CHCR13.PRSEL = 0111_B
	STMIRQ0	STM	CHCR13.PRSEL = 1000_B
	GPTA_TRIG03	GPTA[1)]	CHCR13.PRSEL = 1001_B
	GPTA_TRIG13	GPTA[1)]	CHCR13.PRSEL = 1010_B
	MBSC1SRC	ERAY	CHCR13.PRSEL = 1011_B
	ASC1_TBDR	ASC1	CHCR13.PRSEL = 1100_B
	Reserved[2)]	-	CHCR13.PRSEL = 1101_B
	MSC1_SR3	MSC1	CHCR13.PRSEL = 1110_B
	MLI1_SR7	MLI1	CHCR13.PRSEL = 1111_B
14	DMA_SR12	DMA(INT_O12)	CHCR14.PRSEL = 0000_B
	IOUT0	SCU (ERU)	CHCR14.PRSEL = 0001_B
	FADC_SR00	FADC	CHCR14.PRSEL = 0010_B
	ADC_SR04	ADC	CHCR14.PRSEL = 0011_B
	SSC0_TDR	SSC0	CHCR14.PRSEL = 0100_B

Table 12-12 DMA Request Assignment for DMA Sub-Block 1 (cont'd)

DMA Channel	DMA Request Line	DMA Requesting Unit	Selected by
	ASC0_TDR	ASC0	CHCR14.PRSEL = 0101_B
	MSC0_SR2	MSC0	CHCR14.PRSEL = 0110_B
	MLI0_SR4	MLI0	CHCR14.PRSEL = 0111_B
	STMIRQ0	STM	CHCR14.PRSEL = 1000_B
	GPTA_TRIG04	GPTA[1)]	CHCR14.PRSEL = 1001_B
	GPTA_TRIG14	GPTA[1)]	CHCR14.PRSEL = 1010_B
	INT1SRC	ERAY	CHCR14.PRSEL = 1011_B
	ASC0_TBDR	ASC0	CHCR14.PRSEL = 1100_B
	OBUSY	ERAY	CHCR14.PRSEL = 1101_B
	MSC1_SR2	MSC1	CHCR14.PRSEL = 1110_B
	MLI1_SR4	MLI1	CHCR14.PRSEL = 1111_B
15	DMA_SR13	DMA(INT_O13)	CHCR15.PRSEL = 0000_B
	IOUT1	SCU (ERU)	CHCR15.PRSEL = 0001_B
	FADC_SR01	FADC	CHCR15.PRSEL = 0010_B
	ADC_SR05	ADC	CHCR15.PRSEL = 0011_B
	SSC1_TDR	SSC1	CHCR15.PRSEL = 0100_B
	ASC1_TDR	ASC1	CHCR15.PRSEL = 0101_B
	MSC0_SR3	MSC0	CHCR15.PRSEL = 0110_B
	MLI0_SR5	MLI0	CHCR15.PRSEL = 0111_B
	STMIRQ0	STM	CHCR15.PRSEL = 1000_B
	GPTA_TRIG05	GPTA[1)]	CHCR15.PRSEL = 1001_B
	GPTA_TRIG15	GPTA[1)]	CHCR15.PRSEL = 1010_B
	TINT1SRC	ERAY	CHCR15.PRSEL = 1011_B
	ASC1_TBDR	ASC1	CHCR15.PRSEL = 1100_B
	CCU61_SR0	CCU61	CHCR15.PRSEL = 1101_B
	MSC1_SR3	MSC1	CHCR15.PRSEL = 1110_B
	MLI1_SR5	MLI1	CHCR15.PRSEL = 1111_B
16	DMA_SR14	DMA(INT_O14)	CHCR16.PRSEL = 0000_B
	IOUT2	SCU (ERU)	CHCR16.PRSEL = 0001_B
	FADC_SR02	FADC	CHCR16.PRSEL = 0010_B

Table 12-12 DMA Request Assignment for DMA Sub-Block 1 (cont'd)

DMA Channel	DMA Request Line	DMA Requesting Unit	Selected by
	ADC_SR06	ADC	CHCR16.PRSEL = 0011_B
	SSC0_RDR	SSC0	CHCR16.PRSEL = 0100_B
	ASC0_RDR	ASC0	CHCR16.PRSEL = 0101_B
	CAN_INT_O0	MultiCAN	CHCR16.PRSEL = 0110_B
	MLI0_SR6	MLI0	CHCR16.PRSEL = 0111_B
	STMIRQ0	STM	CHCR16.PRSEL = 1000_B
	GPTA_TRIG06	GPTA[1)]	CHCR16.PRSEL = 1001_B
	GPTA_TRIG16	GPTA[1)]	CHCR16.PRSEL = 1010_B
	NDAT1SRC	ERAY	CHCR16.PRSEL = 1011_B
	SSC3_TDR	SSC3	CHCR16.PRSEL = 1100_B
	CCU62_SR0	CCU62	CHCR16.PRSEL = 1101_B
	ADC_SR08	ADC	CHCR16.PRSEL = 1110_B
	MLI1_SR6	MLI1	CHCR16.PRSEL = 1111_B
17	DMA_SR15	DMA(INT_O15)	CHCR17.PRSEL = 0000_B
	IOUT3	SCU (ERU)	CHCR17.PRSEL = 0001_B
	FADC_SR03	FADC	CHCR17.PRSEL = 0010_B
	ADC_SR07	ADC	CHCR17.PRSEL = 0011_B
	SSC1_RDR	SSC1	CHCR17.PRSEL = 0100_B
	ASC1_RDR	ASC1	CHCR17.PRSEL = 0101_B
	CAN_INT_O1	MultiCAN	CHCR17.PRSEL = 0110_B
	MLI0_SR7	MLI0	CHCR17.PRSEL = 0111_B
	STMIRQ0	STM	CHCR17.PRSEL = 1000_B
	GPTA_TRIG07	GPTA[1)]	CHCR17.PRSEL = 1001_B
	GPTA_TRIG17	GPTA[1)]	CHCR17.PRSEL = 1010_B
	MBSC1SRC	ERAY	CHCR17.PRSEL = 1011_B
	SSC3_RDR	SSC3	CHCR17.PRSEL = 1100_B
	CCU63_SR0	CCU63	CHCR17.PRSEL = 1101_B
	ADC_SR09	ADC	CHCR17.PRSEL = 1110_B
	MLI1_SR7	MLI1	CHCR17.PRSEL = 1111_B

1) GPTA_TRIG signals are per default level sensitive signals while a DMA channel is activated with every active request signal cycle. The DMA internal positive edge detection will generate the channel request with the rising edge of the GPTA_TRIG signal, if selected. If channel requests for the positive and/or negative GPTA_TRIG signal is required, this can be realized either via the ERU (some GPTA_TRIG signals are mapped to it) or via GPTA programming by using additional GPTA cells.
2) Reserved PRSEL combinations do not result to DMA Channel requests.

12.4.2 Access Protection Assignment

DMA access protection as described on Page 12-44 requires the assignment of 32 fixed address range. Table 12-13 shows this address range assignment as implemented in the TC1798 (see also: Page 12-81, Page 12-81).

Table 12-13 DMA Access Protection Address Ranges for DMA_MEmAENR0

Access Protection Range			Related Module(s)
No. n	**Enable Bit in MEmAENR**	**Selected Address Range**	
0	AEN0	F000 0500$_H$ - F000 06FF$_H$	SCU, WDT
1	AEN1	F000 0100$_H$ - F000 01FF$_H$	SBCU
2	AEN2	F000 0200$_H$ - F000 02FF$_H$	STM
3	AEN3	F000 0400$_H$ - F000 04FF$_H$	OCDS
4	AEN4	F000 0800$_H$ to F000 08FF$_H$	MSC0
5	AEN5	F000 0A00$_H$ to F000 0AFF$_H$	ASC0
6	AEN6	F000 0B00$_H$ to F000 0BFF$_H$	ASC1
7	AEN7	F000 0C00$_H$ - F000 17FF$_H$	Port 0 - Port 11
8	AEN8	F030 0000$_H$ - F030 06FF$_H$	Port 12 - Port 18
9	AEN9	F000 1800$_H$ - F000 2FFF$_H$	GPTA0, GPTA1, LTCA2
10	AEN10	F000 3C00$_H$ - F000 3EFF$_H$	DMA
11	AEN11	F000 4000$_H$ - F000 7FFF$_H$	MultiCAN
12	AEN12	F004 0000$_H$ - F004 FFFF$_H$	PCP Registers
13	AEN13	F005 0000$_H$ - F005 FFFF$_H$	PCP Data SRAM (PRAM)
14	AEN14	F006 0000$_H$ - F007 FFFF$_H$	PCP Code SRAM (CMEM)
15	AEN15	F031 0000$_H$ - F031 01FF$_H$ F031 0800$_H$ - F031 09FF$_H$ F031 0A00$_H$ - F031 0BFF$_H$	SSC0, SSC1 SSCG0 SSCG1
16	AEN16	F031 0200$_H$ - F031 03FF$_H$ F031 0C00$_H$ - F031 0DFF$_H$ F031 0E00$_H$ - F010 0FFF$_H$	SSC2, SSC3 SSCG2 SSCG3
17	AEN17	F010 0400$_H$ - F010 05FF$_H$	FADC
18	AEN18	F010 1000$_H$ - F010 1FFF$_H$	ADC0, ADC1, ADC2, ADC3
19	AEN19	F010 C000$_H$ - F010 C0FF$_H$ F01E 0000$_H$ - F01E 7FFF$_H$ F020 0000$_H$ - F023 FFFF$_H$	MLI0 Module, MLI0 Small TWs, MLI0 Large TWs

Table 12-13 DMA Access Protection Address Ranges for DMA_MEmAENR0

Access Protection Range			Related Module(s)
No. n	**Enable Bit in MEmAENR**	**Selected Address Range**	
20	AEN20	F010 C100$_H$ - F010 C1FF$_H$ F01E 8000$_H$ - F01E FFFF$_H$ F024 0000$_H$ - F027 FFFF$_H$	MLI1, MLI1 Small TWs, MLI1 Large TWs
21	AEN21	F7E0 FF00$_H$ - F7E0 FFFF$_H$ F7E1 0000$_H$ - F7E1 FFFF$_H$	CPS CPU Core SFRs & GPRs
22	AEN22	F800 0000$_H$ - F800 03FF$_H$	EBU
23	AEN23	8000 0000$_H$ - 82FF FFFF$_H$ A000 0000$_H$ - A2FF FFFF$_H$	PFLASH0, PFLASH1
24	AEN24	8300 0000$_H$ - 8EFF FFFF$_H$ A300 0000$_H$ - AEFF FFFF$_H$	External EBU Space
25	AEN25	8F00 0000$_H$ - 8F0F FFFF$_H$ AF00 0000$_H$ - AF0F FFFF$_H$	DFLASH0, DFLASH1
26	AEN26	9F00 0000$_H$ - 9F1F FFFF$_H$ BF00 0000$_H$ - BF1F FFFF$_H$	Emulation Device Memory Space
27	AEN27	8FFF C000$_H$ - 8FFF FFFF$_H$ AFFF C000$_H$ - AFFF FFFF$_H$	Boot ROM
28	AEN28	F001 0000$_H$ - F001 7FFF$_H$	ERAY
29	AEN29	9000 0000$_H$ - 9001 FFFF$_H$ B000 0000$_H$ - B001 FFFF$_H$	LMU SRAM
30	AEN30	D000 0000$_H$ - D001 FFFF$_H$ D800 0000$_H$ - D801 FFFF$_H$	DMI (Data Scratch SRAM)
31	AEN31	C000 0000$_H$ - C000 7FFF$_H$ C800 0000$_H$ - C800 7FFF$_H$	PMI (Program Scratch SRAM)

Table 12-14 DMA Access Protection Address Ranges for DMA_MEmAENR1

Access Protection Range			Related Module(s)
No. n	**Enable Bit in MEmAENR**	**Selected Address Range**	
0	AEN0	F010 C200$_H$ - F010 C2FF$_H$	MEMCHK
1	AEN1		
2	AEN2		

Table 12-14 DMA Access Protection Address Ranges for DMA_MEmAENR1

Access Protection Range			Related Module(s)
No. n	**Enable Bit in MEmAENR**	**Selected Address Range**	
3	AEN3		
4	AEN4	F000 0900$_H$ to F000 09FF$_H$	MSC1
5	AEN5		
6	AEN6		
7	AEN7		
8	AEN8		
9	AEN9		
10	AEN10	F000 3000$_H$ - F000 31FF$_H$ F000 3400$_H$ - F000 34FF$_H$	CCU60, CCU61 GPT120
11	AEN11	F000 3200$_H$ - F000 33FF$_H$ F000 3500$_H$ - F000 35FF$_H$	CCU62, CCU63 GPT121
12	AEN12	F000 3800$_H$ - F000 3AFF$_H$	SDMA
13	AEN13	F032 0000$_H$ - F032 00FF$_H$	FCE
14	AEN14	F032 0200$_H$ - F032 02FF$_H$	SHE
15	AEN15	F032 1000$_H$ - F032 19FF$_H$	SENT
16	AEN16	F032 3000$_H$ - F032 31FF$_H$	BMU Registers
17	AEN17	F870 0800$_H$ - F870 08FF$_H$	LMU
18	AEN18	F800 0500$_H$ - F86F FFFF$_H$	PMU, Flash Registers
19	AEN19	F870 0000$_H$ - F870 04FF$_H$	XBAR
20	AEN20		
21	AEN21		
22	AEN22		
23	AEN23		
24	AEN24		
25	AEN25		
26	AEN26	F032 4000$_H$ - F032 7FFF$_H$	BMURAM
27	AEN27		
28	AEN28		
29	AEN29		

Table 12-14 DMA Access Protection Address Ranges for DMA_MEmAENR1

Access Protection Range			Related Module(s)
No. n	**Enable Bit in MEmAENR**	**Selected Address Range**	
30	AEN30	$D820\ 0000_H$ - $D820\ 3FFF_H$	DCACHE
31	AEN31	$C820\ 0000_H$ - $C820\ 3FFF_H$	PCACHE

In the TC1798, four internal memory areas (Program Scratch SRAM, Data Scratch SRAM, LMU SRAM and PCP Data SRAM) are protected by an address range verification in addition to the access enable bits. The address range verification is based on the bit fields SIZEx and SLICEx (x = 3-0), which are located in the registers MEmARR0 and MEmARR1 (m = 1-0). An access to one of these four memory areas is only processed if it is enabled by the corresponding AENx bit and if the address is inside the sub-range defined by the corresponding SIZEx and SLICEx. If the address is outside of the defined sub-range, the transfer will not be processed and an error interrupt is generated (indicated by the corresponding MExDER, MExSER bit). If a protected memory is available from DMA under multiple address ranges (SRI, FPI, cached and or un-cached segments), the access protection is valid for all memory views in parallel, starting always with the base address of the memory views, ending always with the end address of the address range.

The address ranges described by SLICEx and SIZEx are defined as follows:

- MEmARR0.SLICE0, MEmARR0.SIZE0:
  32-KB Program Scratch SRAM, assigned to address range 31 (AEN31). The sub-ranges are controlled by bit fields MEmARR0.SIZE0 and ME0ARR0.SLICE0 with a minimum granularity of 0,5 KB (see **Table 12-15**).
- MEmARR0.SIZE1 and MEmARR0.SLICE1:
  128-KB LMU SRAM, assigned to address range 29 (AEN29). The sub-ranges are controlled by bit fields MEmARR0.SIZE1 and MEmARR0.SLICE1 with a minimum granularity of 1 KB (see **Table 12-16**).
- MEmARR0.SIZE2 and MEmARR0.SLICE2:
  128-KB Data Scratch SRAM, assigned to address range 30 (AEN30). The sub-ranges are controlled by bit fields MEmARR0.SIZE2 and MEmARR0.SLICE2 with a minimum granularity of 1 KB (see **Table 12-17**).
- MEmARR0.SIZE3 and MEmARR0.SLICE3:
  16-Kbyte PCP Data SRAM, assigned to address range 13 (AEN13). The sub-range is controlled by bit fields MEmARR0.SIZE3 and MEmARR0.SLICE3 with a minimum granularity of 0,5 KB (see **Table 12-18**).
- MEmARR1.SIZE0 and MEmARR1.SLICE0:
  Reserved.
- MEmARR1.SIZE1 and MEmARR1.SLICE1:
  Reserved.
- MEmARR1.SIZE2 and MEmARR1.SLICE2:
  Reserved.
- MEmARR1.SIZE3 and MEmARR1.SLICE3:
  Reserved.

DMA_MEmARR0.SIZE0 and DMA_MEmARR0.SLICE0 bit fields: Program Scratch SRAM sub-range access protection

Bit fields SIZE0 and SLICE0 for the PMI memory sub-range access protection (32 KB PSPR) as shown in **Table 12-15**.

The PMI memory is protected with a min. granularity of 0,5 KB up to the end address Cx00 $FFFF_H$.

PMI address ranges that are protected by the bit fields SIZE0 and SLICE0:

- C000 0000_H - C000 $7FFF_H$ (Program Scratch RAM)
- C800 0000_H - C800 $7FFF_H$ (Program Scratch RAM)

Table 12-15 Program Scratch SRAM Address Protection Sub-Range Definition

SIZE0	Sub-Ranges	SLICE0	Selected Address Range
000_B	32 sub-ranges of 512 bytes	00000_B 00001_B … 11111_B	xxx0 0000_H - xxx0 $01FF_H$ xxx0 0200_H - xxx0 $03FF_H$ … xxx0 $3E00_H$ - xxx0 $3FFF_H$
001_B	32 sub-ranges of 1 Kbyte	00000_B 00001_B … 11111_B	xxx0 0000_H - xxx0 $03FF_H$ xxx0 0400_H - xxx0 $07FF_H$ … xxx0 $7C00_H$ - xxx0 $7FFF_H$
010_B	32 sub-ranges of 2 Kbytes	00000_B 00001_B … 11111_B	xxx0 0000_H - xxx0 $07FF_H$ xxx0 0800_H - xxx0 $0FFF_H$ … xxx0 $F800_H$ - xxx0 $FFFF_H$
011_B	16 sub-ranges of 4 Kbytes	$X0000_B$ $X0001_B$ … $X1111_B$	xxx0 0000_H - xxx0 $0FFF_H$ xxx0 1000_H - xxx0 $1FFF_H$ … xxx0 $F000_H$ - xxx0 $FFFF_H$
100_B	8 sub-ranges of 8 Kbytes	$XX000_B$ $XX001_B$ … $XX111_B$	xxx0 0000_H - xxx0 $1FFF_H$ xxx0 2000_H - xxx0 $3FFF_H$ … xxx0 $E000_H$ - xxx0 $FFFF_H$
101_B	4 sub-ranges of 16 Kbytes	$XXX00_B$ $XXX01_B$ $XXX10_B$ $XXX11_B$	xxx0 0000_H - xxx0 $3FFF_H$ xxx0 4000_H - xxx0 $7FFF_H$ xxx0 8000_H - xxx0 $BFFF_H$ xxx0 $C000_H$ - xxx0 $FFFF_H$

Table 12-15 Program Scratch SRAM Address Protection Sub-Range Definition

SIZE0	Sub-Ranges	SLICE0	Selected Address Range
110_B	2 sub-ranges of 32 Kbytes	$XXXX0_B$ $XXXX1_B$	xxxx 0000_H - xxxx $7FFF_H$ xxxx 8000_H - xxxx $FFFF_H$
111_B	64 Kbytes	$XXXXX_B$	xxxx 0000_H - xxxx $FFFF_H$

DMA_MEmARR0.SIZE1 and DMA_MEmARR0.SLICE1 bit fields: LMU SRAM sub-range access protection

Bit fields SIZE1 and SLICE1 for the LMU SRAM sub-range access protection (128 KB) are coded as shown in **Table 12-16**.

The 128 KB LMU SRAM memory is protected with a minimum granularity of 1 KB up to the end address x001 $FFFF_H$.

OVRAM address ranges that are protected by the bit fields SIZE1 and SLICE1:

- $9000\ 0000_H$ - $9001\ FFFF_H$ (LMU SRAM)
- $B000\ 0000_H$ - $B001\ FFFF_H$ (LMU SRAM)

Table 12-16 LMU SRAM Address Protection Sub-Range Definition

SIZE1	Sub-Ranges	SLICE1	Selected Address Range
000_B	32 sub-ranges of 1 Kbytes	00000_B 00001_B … 11111_B	xxx0 0000_H - xxx0 $03FF_H$ xxx0 0400_H - xxx0 $07FF_H$ … xxx0 $7C00_H$ - xxx0 $7FFF_H$
001_B	32 sub-ranges of 2 Kbyte	00000_B 00001_B … 11111_B	xxx0 0000_H - xxx0 $07FF_H$ xxx0 0800_H - xxx0 $0FFF_H$ … xxx0 $F800_H$ - xxx0 $FFFF_H$
010_B	32 sub-ranges of 4Kbytes	00000_B 00001_B … 11111_B	xxx0 0000_H - xxx0 $0FFF_H$ xxx0 1000_H - xxx0 $1FFF_H$ … xxx1 $F000_H$ - xxx1 $FFFF_H$
011_B	16 sub-ranges of 8 Kbytes	$X0000_B$ $X0001_B$ … $X1111_B$	xxx0 0000_H - xxx0 $1FFF_H$ xxx0 2000_H - xxx0 $3FFF_H$ … xxx1 $E000_H$ - xxx1 $FFFF_H$
100_B	8 sub-ranges of 16 Kbytes	$XX000_B$ $XX001_B$ … $XX111_B$	xxx0 0000_H - xxx0 $3FFF_H$ xxx0 4000_H - xxx0 $7FFF_H$ .... xxx1 $C000_H$ - xxx1 $FFFF_H$

Table 12-16 LMU SRAM Address Protection Sub-Range Definition (cont'd)

SIZE1	Sub-Ranges	SLICE1	Selected Address Range
101_B	4 sub-ranges of 32 Kbytes	$XXX00_B$ $XXX01_B$ $XXX10_B$ $XXX11_B$	xxx0 0000_H - xxx0 $7FFF_H$ xxx0 8000_H - xxx0 $FFFF_H$ xxx1 0000_H - xxx1 $7FFF_H$ xxx1 8000_H - xxx1 $FFFF_H$
110_B	2 sub-ranges of 64 Kbytes	$XXXX0_B$ $XXXX1_B$	xxx0 0000_H - xxx0 $FFFF_H$ xxx1 0000_H - xxx1 $FFFF_H$
111_B	128 Kbytes	$XXXXX_B$	xxx0 0000_H - xxx1 $FFFF_H$

DMA_MEmARR0.SIZE2 and DMA_MEmARR0.SLICE2 bit fields: Data Scratch SRAM sub-range access protection

Bit fields SIZE2 and SLICE2 for the Data Scratch SRAM sub-range access protection. These bit fields are covering the 128 KB Data Scratch SRAM.

The Data Scratch SRAM is protected with a min. granularity of 1 KB (**Table 12-17**) up to the end address Dx01 $FFFF_H$.

Data Scratch SRAM address ranges that are protected by the bit fields SIZE2 and SLICE2:

- D000 0000_H - D001 $FFFF_H$ (Data Scratch SRAM)
- D800 0000_H - D801 $FFFF_H$ (Data Scratch SRAM)

Table 12-17 Data Scratch SRAM Address Protection Sub-Range Definitions

SIZE2	Sub-Ranges	SLICE2	Selected Address Range
000_B	32 sub-ranges of 1 Kbytes	00000_B 00001_B … 11111_B	xxx0 0000_H - xxx0 $03FF_H$ xxx0 0400_H - xxx0 $07FF_H$ … xxx0 $7C00_H$ - xxx0 $7FFF_H$
001_B	32 sub-ranges of 2 Kbyte	00000_B 00001_B … 11111_B	xxx0 0000_H - xxx0 $07FF_H$ xxx0 0800_H - xxx0 $0FFF_H$ … xxx0 $F800_H$ - xxx0 $FFFF_H$
010_B	32 sub-ranges of 4Kbytes	00000_B 00001_B … 11111_B	xxx0 0000_H - xxx0 $0FFF_H$ xxx0 1000_H - xxx0 $1FFF_H$ … xxx1 $F000_H$ - xxx1 $FFFF_H$

Table 12-17 Data Scratch SRAM Address Protection Sub-Range Definitions

SIZE2	Sub-Ranges	SLICE2	Selected Address Range
011_B	16 sub-ranges of 8 Kbytes	$X0000_B$ $X0001_B$ … $X1111_B$	xxx0 0000_H - xxx0 $1FFF_H$ xxx0 2000_H - xxx0 $3FFF_H$ … xxx1 $E000_H$ - xxx1 $FFFF_H$
100_B	8 sub-ranges of 16 Kbytes	$XX000_B$ $XX001_B$ … $XX111_B$	xxx0 0000_H - xxx0 $3FFF_H$ xxx0 4000_H - xxx0 $7FFF_H$ .... xxx1 $C000_H$ - xxx1 $FFFF_H$
101_B	4 sub-ranges of 32 Kbytes	$XXX00_B$ $XXX01_B$ $XXX10_B$ $XXX11_B$	xxx0 0000_H - xxx0 $7FFF_H$ xxx0 8000_H - xxx0 $FFFF_H$ xxx1 0000_H - xxx1 $7FFF_H$ xxx1 8000_H - xxx1 $FFFF_H$
110_B	2 sub-ranges of 64 Kbytes	$XXXX0_B$ $XXXX1_B$	xxx0 0000_H - xxx0 $FFFF_H$ xxx1 0000_H - xxx1 $FFFF_H$
111_B	128 Kbytes	$XXXXX_B$	xxx0 0000_H - xxx1 $FFFF_H$

DMA_MEmARR0.SIZE3 and DMA_MEmARR0.SLICE3 bit fields: PCP Data SRAM sub-range access protection

Bit fields SIZE3 and SLICE3 for the PCP Data SRAM sub-range access protection. These bit fields are covering PCP Data SRAM memory.

The PCP Data SRAM memory is protected with a min. granularity of 0,5 KB (**Table 12-18**) up to the end address F005 $FFFF_H$ (16KB PRAM and 48KB Reserved Address Space).

PCP Data SRAM address range that is protected by the bit fields SIZE3 and SLICE3:

- F005 0000_H - F005 $3FFF_H$ (PCP Data SRAM on FPI Bus, 16 KB)

Table 12-18 PCP Data SRAM SIZE3 and SLICE3 Address Protection Sub-Range Definition Scheme

SIZE3	Sub-Ranges	SLICE3	Selected Address Range
000_B	32 sub-ranges of 512 bytes	00000_B 00001_B … 11111_B	$F005\ 0000_H$ - $F005\ 01FF_H$ $F005\ 0200_H$ - $F005\ 03FF_H$ … $F005\ 3E00_H$ - $F005\ 3FFF_H$
001_B	32 sub-ranges of 1 Kbyte	00000_B 00001_B … 11111_B	$F005\ 0000_H$ - $F005\ 03FF_H$ $F005\ 0400_H$ - $F005\ 07FF_H$ … $F005\ 7C00_H$ - $F005\ 7FFF_H$
010_B	32 sub-ranges of 2 Kbytes	00000_B 00001_B … 11111_B	$F005\ 0000_H$ - $F005\ 07FF_H$ $F005\ 0800_H$ - $F005\ 0FFF_H$ … $F005\ F800_H$ - $F005\ FFFF_H$
011_B	16 sub-ranges of 4 Kbytes	$X0000_B$ $X0001_B$ … $X1111_B$	$F005\ 0000_H$ - $F005\ 0FFF_H$ $F005\ 1000_H$ - $F005\ 1FFF_H$ … $F005\ F000_H$ - $F005\ FFFF_H$
100_B	8 sub-ranges of 8 Kbytes	$XX000_B$ $XX001_B$ … $XX111_B$	$F005\ 0000_H$ - $F005\ 1FFF_H$ $F005\ 2000_H$ - $F005\ 3FFF_H$ … $F005\ E000_H$ - $F005\ FFFF_H$
101_B	4 sub-ranges of 16 Kbytes	$XXX00_B$ $XXX01_B$ $XXX10_B$ $XXX11_B$	$F005\ 0000_H$ - $F005\ 3FFF_H$ $F005\ 4000_H$ - $F005\ 7FFF_H$ $F005\ 8000_H$ - $F005\ BFFF_H$ $F005\ C000_H$ - $F005\ FFFF_H$
110_B	2 sub-ranges of 32 Kbytes	$XXXX0_B$ $XXXX1_B$	$F005\ 0000_H$ - $F005\ 7FFF_H$ $F005\ 8000_H$ - $F005\ FFFF_H$
111_B	64 Kbytes	$XXXXX_B$	$F005\ 0000_H$ - $F005\ FFFF_H$

DMA_MEmARR1.SIZE0 and DMA_MEmARR1.SLICE0 bit fields

Table 12-19 Address Protection Sub-Range Definition

SIZE0	Sub-Ranges	SLICE0	Selected Address Range
000_B			
001_B			
010_B			
011_B			
100_B			
101_B			
110_B			
111_B			

DMA_MEmARR1.SIZE1 and DMA_MEmARR1.SLICE1 bit fields

Table 12-20 Address Protection Sub-Range Definition

SIZE1	Sub-Ranges	SLICE1	Selected Address Range
000_B			
001_B			
010_B			
011_B			
100_B			
101_B			
110_B			
111_B			

DMA_MEmARR1.SIZE2 and DMA_MEmARR1.SLICE2 bit fields

Table 12-21 Address Protection Sub-Range Definition

SIZE2	Sub-Ranges	SLICE2	Selected Address Range
000_B			
001_B			
010_B			
011_B			

Table 12-21 Address Protection Sub-Range Definition (cont'd)

SIZE2	Sub-Ranges	SLICE2	Selected Address Range
100_B			
101_B			
110_B			
111_B			

DMA_MEmARR1.SIZE3 and DMA_MEmARR1.SLICE3 bit fields

Table 12-22 Address Protection Sub-Range Definition

SIZE3	Sub-Ranges	SLICE3	Selected Address Range
000_B			
001_B			
010_B			
011_B			
100_B			
101_B			
110_B			
111_B			

12.4.3 Implementation-specific DMA Registers

The DMA controller as implemented in the TC1798 contains the following additional registers:

- DMA clock control register
- Service request control registers for DMA controller interrupts (DMA_SRCx)
- Service request control registers for MLI module interrupts (DMA_MLI0ySRC.x)

Figure 12-29 provides an overview of these registers.

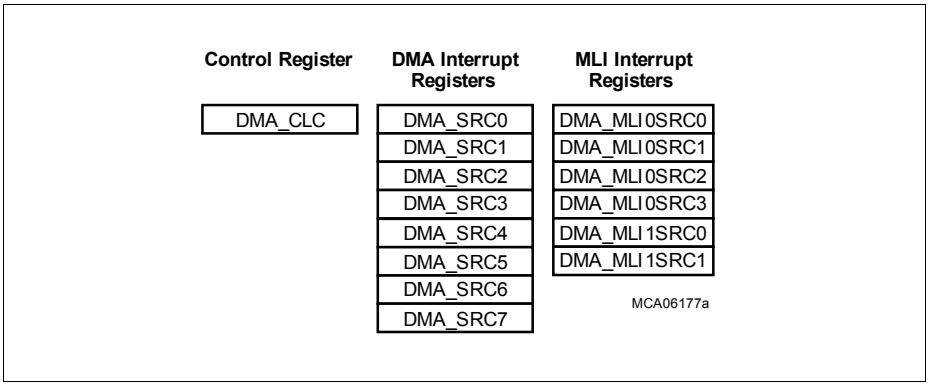


Figure 12-29 DMA Implementation-specific Registers

Note: Further details on interrupt handling and processing are described in the "Interrupt System" chapter of the TC1798 System Units User´s Manual.

The clock generation and interrupt control configuration as implemented in the DMA controller module is shown in **Figure 12-29**.

The DMA controller, the Cerberus and the two MLI modules (MLI0 and MLI1) are supplied from a common module clock f_{DMA} that has the frequency of the system clock f_{FPI} and is controlled via the DMA_CLC clock control register. The MLI modules nor the Cerberus module do not have their own clock control registers. Their input clock is derived from the DMA clock divided by separate fractional divider registers.

The control of the suspend and break features is done independently inside each module.

The DMA controller module contains in total 14 interrupt request nodes with its interrupt service request control registers:

- Eight interrupt requests SR[7:0] = INT_O[7:0] from the DMA controller; upper eight interrupt requests of the DMA controller INT_O[15:8] are used ad DMA channel trigger inputs.
- Four interrupt requests SR[3:0] = INT_O[3:0] from the MLI0 module; upper four interrupt requests of the MLI0 module INT_O[7:4] are not connected.
- Two interrupt requests SR[1:0] = INT_O[1:0] from the MLI1 module; upper six interrupt requests of the MLI1 module INT_O[7:2] are not connected.

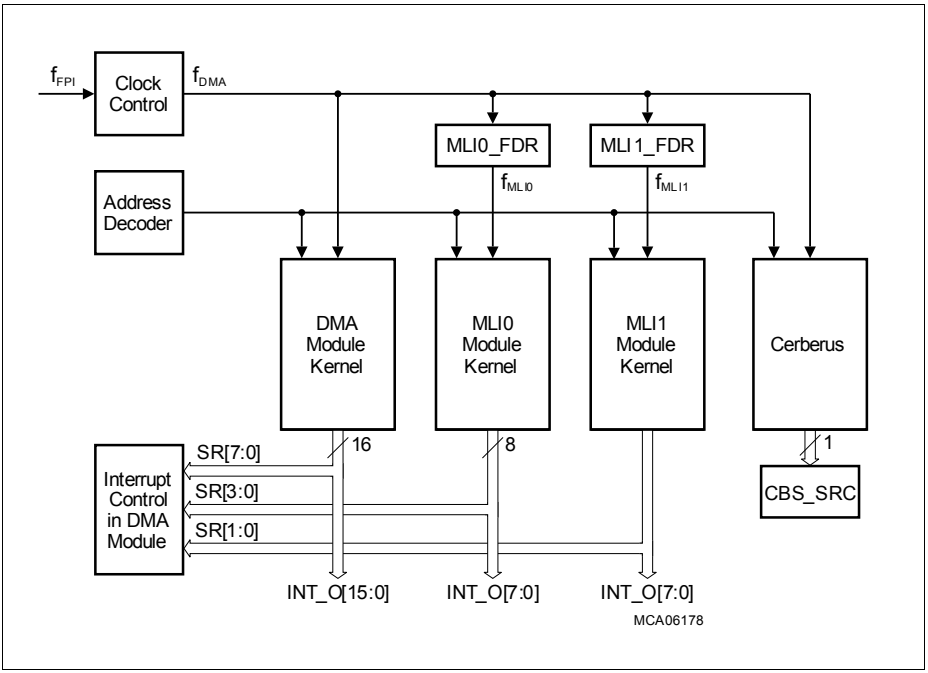
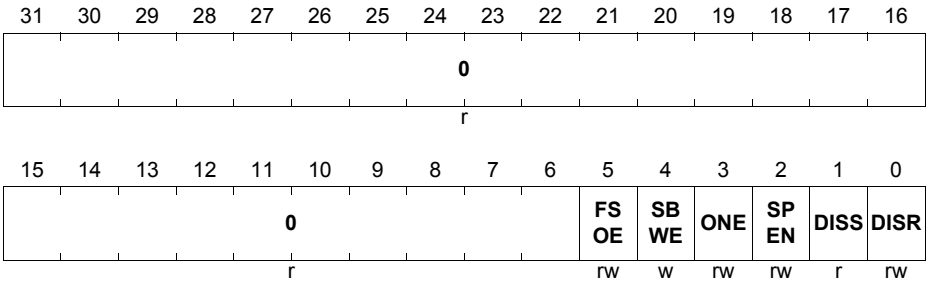


Figure 12-30 Implementation of the DMA Module and the MLI Modules

12.4.3.1 Clock Control Register

The Clock Control Register controls the DMA module internal f_{DMA} clock signal. This clock is also used for the MLI modules as a common clock that can be individually divided for the MLI modules.

DMA_CLC
DMA Clock Control Register **(000_H)** **Reset Value: 0000 0008$_H$**



Field	Bits	Type	Description
DISR	0	rw	**Module Disable Request Bit** Used for enable/disable control of the module
DISS	1	r	**Module Disable Status Bit** Bit indicates the current status of the module
SPEN	2	rw	**Module Suspend Enable for OCDS** Used to enable the Suspend Mode
ONE	3	rw	**Reserved;** returns 1 if read; must be written with 1.
SBWE	4	w	**Module Suspend Bit Write Enable for OCDS** Determines whether SPEN and FSOE are write-protected.
0	5	rw	**Reserved;** returns 0 if read; must be written with 0.
0	[31:6]	r	**Reserved** Read as 0; should be written with 0.

Note: After a hardware reset operation, the DMA module is enabled.

Note: The suspend mode does not modify any of the registers.

12.4.3.2 DMA Interrupt Registers

In the TC1798, the lower eight DMA controller interrupts SR[7:0] are connected to service request control registers. The upper eight DMA controller interrupt outputs SR[15:8] are used as DMA channel request inputs (Page 12-101).

DMA_SRCx (x = 0-7)
DMA Service Request Control Register x
($2FC_H$ - x*4_H) **Reset Value: 0000 0000_H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SETR	CLRR	SRR	SRE	0	TOS	0		SRPN							
w	w	rh	rw	r	rw	r		rw							

Field	Bits	Type	Description
SRPN	[7:0]	rw	**Service Request Priority Number**
TOS	10	rw	**Type of Service Control** 0_B CPU service is initiated 1_B PCP request is initiated
SRE	12	rw	**Service Request Enable**
SRR	13	rh	**Service Request Flag**
CLRR	14	w	**Request Clear Bit**
SETR	15	w	**Request Set Bit**
0	[9:8], 11, [31:16]	r	**Reserved** Read as 0; should be written with 0.

12.4.3.3 MLI Interrupt Registers

The Service Request Control Registers of the MLI module are located inside the DMA address area, because the MLI module does not have its own FPI Bus interfaces. The MLI modules shares one FPI Bus slave interface with the DMA controller.

The MLI0 module has eight interrupt output lines. Only four of them [3:0] are controlled by the MLI0 service request registers. The MLI1 module has also eight interrupt output lines, but only two of them [1:0] are controlled by the MLI1 service request registers.

DMA_MLI0SRCx (x = 0-3)
DMA MLI0 Service Request Control Register x
($2AC_H$ - x*4_H) **Reset Value: 0000 0000_H**

DMA_MLI1SRCy (y = 0-1)
DMA MLI1 Service Request Control Register y
($2BC_H$ - y*4_H) **Reset Value: 0000 0000_H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SETR	CLRR	SRR	SRE	0	TOS	0		SRPN							
w	w	rh	rw	r	rw	r		rw							

Field	Bits	Type	Description
SRPN	[7:0]	rw	**Service Request Priority Number**
TOS	10	rw	**Type of Service Control** 0_B CPU service is initiated 1_B PCP request is initiated
SRE	12	rw	**Service Request Enable**
SRR	13	rh	**Service Request Flag**
CLRR	14	w	**Request Clear Bit**
SETR	15	w	**Request Set Bit**
0	[9:8], 11, [31:16]	r	**Reserved** Read as 0; should be written with 0.

Note: The bit coding of the MLI0/MLI1 service request registers is identical to that of the DMA Service Request Control Registers shown on the previous page.

12.4.4 Address Map

The DMA controller register block address map is shown in **Figure 12-31**. It shows how the different register blocks are arranged and adds the absolute address information.

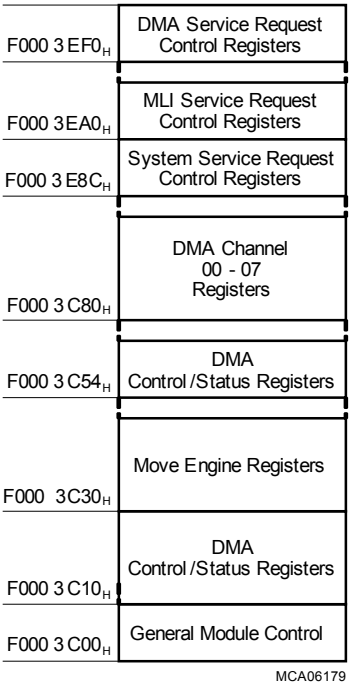


Figure 12-31 DMA Controller Register Block Address Map

12.5 Memory Checker Module

The Memory Checker Module (MCHK) supports the checking of data consistency in memories. It includes two parallel Cyclic Redundancy Checkers (CRCs) that can be used to check the data consistency of two memories in parallel. Each CRC block contains two algorithm engines:

1. A legacy data compaction algorithm based on a Multiple Input Shift Register (MISR) implementation.
2. A CRC-32 ethernet polynomial implementation.

Both algorithm engines use a common input register and simultaneously compute a checksum.

12.5.1 Functional Description

The Memory Checker module is connected to the DMA Peripheral Interface and can be accessed via the SPB. Preferable the module is used in combination with the DMA as it as described hereafter: a DMA channel can be used to read 8-bit, 16-bit, or 32-bit data from an address area and to write the data in one of the two memory checker input register. With each write operation to the chosen memory checker input register a polynomial checksum calculation is triggered and the result of the calculation is stored in the corresponding memory checker result register. The MISR algorithm engine supports 8-bit, 16-bit and 32-bit read data accesses. The CRC-32 ethernet polynomial is limited to 32-bit accesses.

In order to start a memory check sequence, the memory checker MISR and CRC-32 Ethernet polynomial result registers must be initialized (e.g. written with $FFFFFFFF_H$ or with a desired start value) and a DMA transaction must be set up (start address, length, etc.). When programming the DMA channel for the memory checker with CHCRmn.RROAT = 1, one DMA transfer request (software or hardware triggered) starts the DMA transaction.

During the read move operations of the DMA transaction, data is always read from the memory and then written into the memory checker input register for the polynomial checksum calculation. At the end of the transaction (CHSRmn.TCOUNT = 0), an interrupt can be generated by the DMA channel (if CHCRmn.RROAT = 1), and the memory checker result register can be read out by software.

Both the MISR and CRC-32 memory checkers use the IEEE 802.3 Standard polynomial, which is given by:

$$G^{32} = x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1 \quad (12.1)$$

Note: Although the polynomial above is used for generation, the generation algorithm differs from the one that is used by the Ethernet protocol.

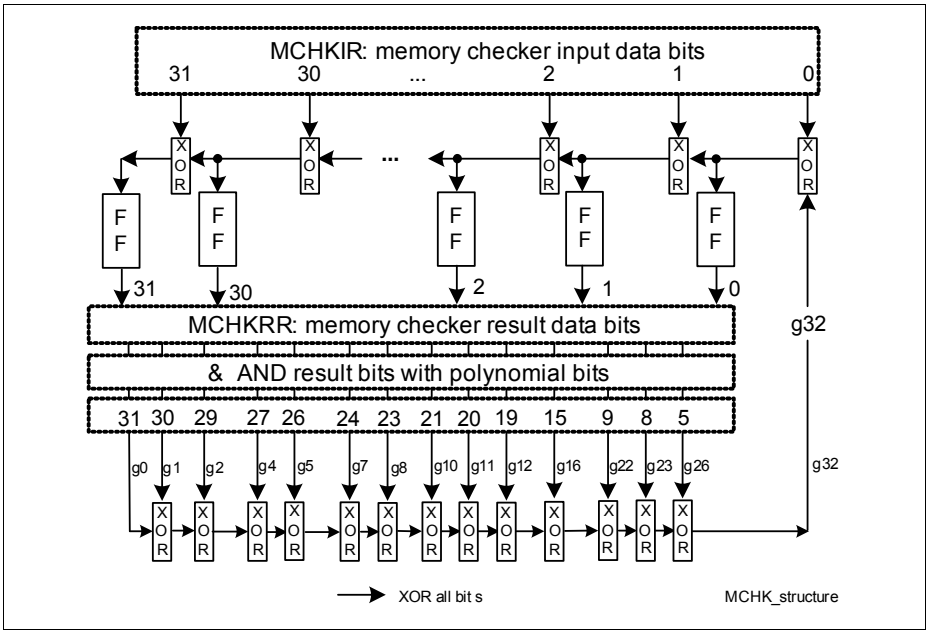


Figure 12-32 Implementation of the Multiple Input Shift Register

12.5.1.1 Ethernet CRC-32 Endianness

In order to comply with the Ethernet CRC-32 standard the endianness of the input word needs to be big endian. This is important only when the input stream is made up of bytes, because each CPU architecture may have a different endianness.

TriCore is little endian, and when a byte pointer (to a byte array) is cast into a 32-bit word pointer, the compiler packs the bytes in little endian format and therefore the CRC-32 checksum result provided by the MCHK Ethernet CRC-32 hardware differs from that generated by an Ethernet CRC-32 software model using a byte stream. In order to generate a checksum compliant with the Ethernet CRC-32 checksum then the software must swap the order of the bytes.

12.5.2 Memory Checker Module Registers

This section describes the kernel registers of the Memory Checker module.

MCHK Register Overview

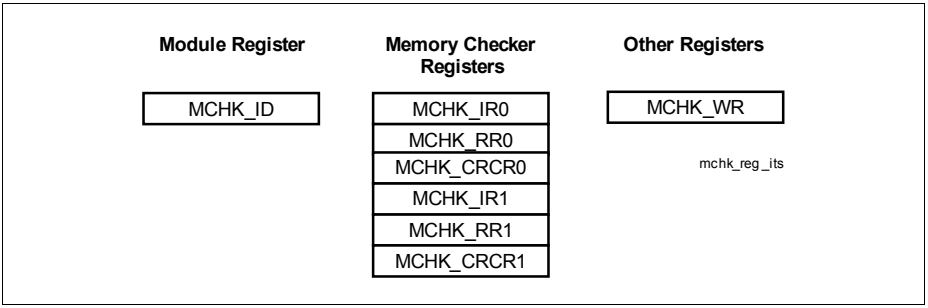


Figure 12-33 Memory Checker Registers

Table 12-23 Registers Address Space - Memory Checker Module Address Space

Module	Base Address	End Address	Note
MCHK	$F010\ C200_H$	$F010\ C2FF_H$	

Table 12-24 Registers Overview - Memory Checker Module Control Registers

Short Name	Description	Offset Addr.[1]	Access Mode		Reset Class	Description See
			Read	Write		
-	Reserved	000_H - 004_H	BE	BE	-	-
MCHK_ID	Module Identification Register	008_H	US, V	BE	-	Page 12-133
-	Reserved	$00C_H$	BE	BE	-	-
MCHK_IR0	Memory Checker Input Register	010_H	U, SV	U, SV	3	Page 12-135
MCHK_RR0	Memory Checker Result Register	014_H	U, SV	U, SV	3	Page 12-135
MCHK_IR1	Memory Checker Input Register	018_H	U, SV	U, SV	3	Page 12-135
MCHK_RR1	Memory Checker Result Register	$01C_H$	U, SV	U, SV	3	Page 12-135

Table 12-24 Registers Overview - Memory Checker Module Control Registers

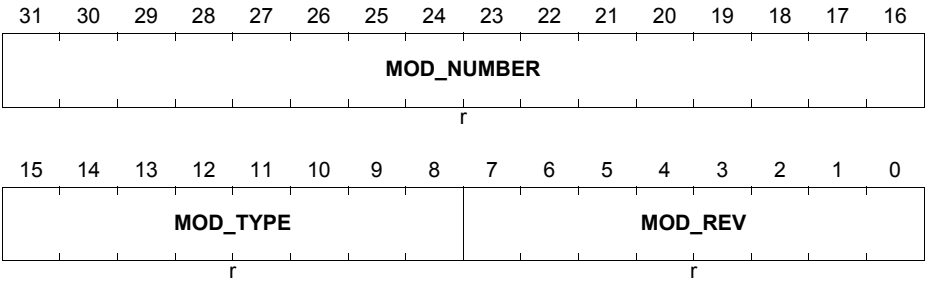
Short Name	Description	Offset Addr.[1]	Access Mode		Reset Class	Description See
			Read	Write		
MCHK_WR	Memory Checker Write Register	020_H	U, SV	U, SV	3	Page 12-136
MCHK_CRCR0	Memory Checker Result Register	024_H	U, SV	U, SV, 32	3	Page 12-136
MCHK_CRCR1	Memory Checker Result Register	028_H	U, SV	U, SV, 32	3	Page 12-136
-	Reserved	$02C_H$ - $2FF_H$	BE	BE	-	-

1) The absolute register address is calculated as follows:
Module Base Address (Table 12-23) + Offset Address (shown in this column)

12.5.2.1 Memory Checker Module Control Registers

The identification register allows the programmer version-tracking of the module. The table below shows the identification register which is implemented in the MCHK module.

MCHK_ID
Module Identification Register (008_H) Reset Value: 001B C0XX$_H$

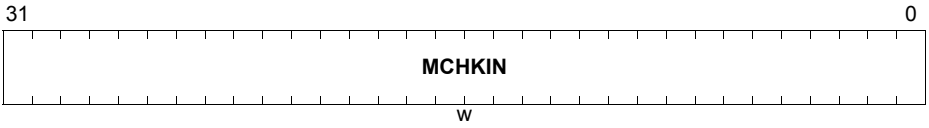


Field	Bits	Type	Description
MOD_REV	[7:0]	r	**Module Revision Number** This bit field defines the module revision number. The value of a module revision starts with 01_H (first revision).

Field	Bits	Type	Description
MOD_TYPE	[15:8]	r	**Module Type** The bit field is set to $C0_H$ which defines the module as a 32-bit module.
MOD_NUMBER	[31:16]	r	**Module Number Value** This bit field defines a module identification number. The value for the Memory Checker module is $001B_H$.

A Memory Checker Input Register is used during write moves of a memory checker related DMA transaction as data destination with its fixed register address. If the DMA moves to register, for example MCHK_IR0 are 8-bit or 16-bit wide, the unused register bits of the 32-bit MCHKIN0 value are taken as 0s for the current result calculation.

MCHK_IRx (x = 0-1)
Memory Checker Input Register (010_H+x*08_H) Reset Value: 0000 0000_H

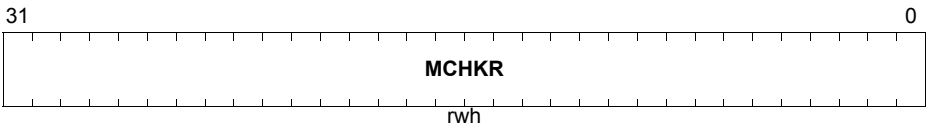


Field	Bits	Type	Description
MCHKIN	[31:0]	w	**Memory Checker Input** The value written to MCHKIN is used for the next checksum calculation. Any read action will deliver 0.

Note: MCHK_IR is a write-only register. Any read action will deliver 0000 0000_H.

A Memory Checker Result Register contains the result of the memory check operation. Before starting a checksum calculation operation, it should be written with an initial checksum calculation value.

MCHK_RRx (x = 0-1)
Memory Checker Result Register (014_H+x*08_H) Reset Value: 0000 0000_H

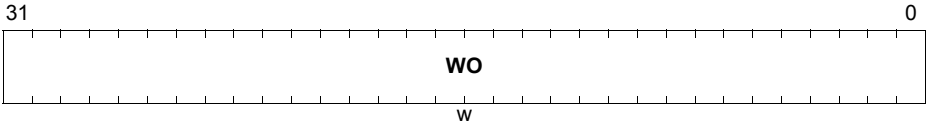


Field	Bits	Type	Description
MCHKR	[31:0]	rwh	**Memory Checker Result** This bit field contains the current result of the memory checksum calculation operation.

The Memory Checker Write Register is a dummy write-only register that is located within the memory checker address range.

The Memory Checker Write Register can be used as dummy write register at the write back action of the DMA or MLI controller Move Engine when the pattern detection feature of the DMA controller is used. Accessing MCHK_WR with the Move Engine of the MLI or DMA controller via the Bus Switch of the DMA controller (see) does not request the two FPI buses of the TC1798, SPB and DMA, because it is near the MLI modules address ranges.

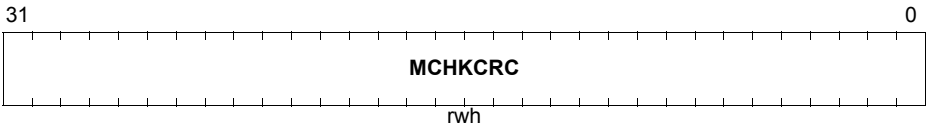
MCHK_WR
Memory Checker Write Register (020_H) Reset Value: 0000 0000_H



Field	Bits	Type	Description
WO	[31:0]	w	**Write-Only** This write-only bit field is used to write dummy data during DMA pattern detection. The data written to WO is not taken into account for any action. Any read action of WO will deliver 0000 0000_H.

The CRC Registers store the working CRC32 ethernet polynomial checksum. Only 32-bit word accesses are permitted to the CRC registers. In order to start a CRC32 sequence the CRC register must be initialised (e.g. written with 00000000_H or with a desired start value) and a DMA transaction set up (start address, length, etc.). When data is written to MCHK_IRx then a polynomial checksum calculation is performed and MCHK_CRCx is updated.

MCHK_CRCx (x = 0-1)
Memory Checker CRC Register (024_H+x*04_H) Reset Value: 0000 0000_H



Field	Bits	Type	Description
MCHKCRC	[31:0]	rwh	**Memory Checker CRC** This bit field contains the working CRC32 ethernet polynomial checksum. The stored value is inverted and reflected prior to a read. Therefore if the register is written with all 1’s then the output will be all 0’s.

13 Safe Direct Memory Access Controller (SDMA)

This chapter describes the Safe Direct Memory Access (SDMA) Controller of the TC1798. It contains the following sections:

- Functional description of the SDMA controller kernel (see **Section 13.2**)
- SDMA controller module register description (see **Section 13.3**)
- TC1798 implementation-specific details of the SDMA controller (interrupt control, address decoding, clock control, see **Section 13.4**)

*Note: The SDMA kernel register names described in **Section 13.3** are referenced in the TC1798 User´s Manual by the module name prefix "SDMA_".*

13.1 What is new

SDMA is based on the DMA peripheral. SDMA has additional features to support safety critical applications. The principal differences are:

- Upper and lower address boundary checking of the source and destination address.
- Generation of unique CRC checksums for source and destination addresses.
- Generation of in-line CRC checksum for read data.

13.2 SDMA Controller Kernel Description

The SDMA Controller of the TC1798 transfers data from data source locations to data destination locations without intervention of the CPU or other on-chip devices. One data move operation is controlled by one SDMA channel. Eight SDMA channels are provided in one SDMA Sub-Block. The Bus Switch provides the connection of the SDMA Sub-Block to the On Chip Bus interfaces and a SDMA Peripheral interface. In the TC1798, the two On Chip Bus interfaces are connected to the System Peripheral Bus. Clock control, address decoding, SDMA request wiring, and SDMA interrupt service request control are implementation-specific and are managed outside the SDMA controller kernel.

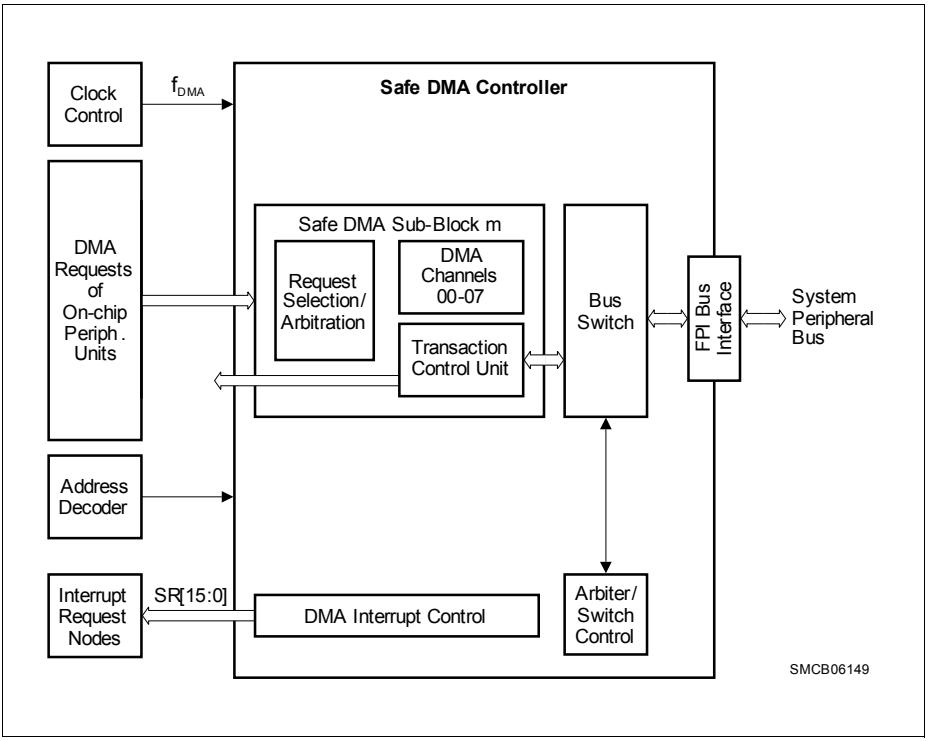


Figure 13-1 SDMA Block Diagram

13.2.1 Features

The SDMA controller has the following features:

- 8 independent SDMA channels
  - 1 SDMA Sub-Block with 8 SDMA channels
  - Parallel channel execution
  - Up to 16 selectable request inputs per SDMA channel
  - 2-level programmable priority of SDMA channels within the SDMA Sub-Block
  - Software and hardware SDMA request
  - Hardware requests by selected on-chip peripherals and external inputs
- Individually programmable operation modes for each SDMA channel
  - Single Mode: stops and disables SDMA channel after a predefined number of SDMA transfers
  - Continuous Mode: SDMA channel remains enabled after a predefined number of SDMA transfers; SDMA transaction can be repeated
  - Programmable address modification
  - Two shadow register modes (with / w/o automatic reset and direct write access).
- Full 32-bit addressing capability of each SDMA channel
  - 4 Gbyte address range
  - Data block move > 32 Kbyte per SDMA transaction
  - Circular buffer addressing mode with flexible circular buffer sizes
- Programmable data width of SDMA transfer/transaction: 8-bit, 16-bit, or 32-bit
- Register set for each SDMA channel
  - Source and destination address register
  - Channel control and status register
  - Transfer count register
- SDMA module is working on FPI frequency.
- Read/write requests from the Move Engine are directed to the FPI Bus.

13.2.2 Definition of Terms

Some basic terms must be defined for the functional description of the SDMA controller.

SDMA Move

A SDMA move is an operation that always consists of two parts:

1. A read move that loads data from a data source into the SDMA controller
2. A write move that puts data from the SDMA controller to a data destination

Within a SDMA move, data is always moved from the data source via the SDMA controller to the data destination. Data is temporarily stored in the SDMA controller. The data widths of read move and write move are always identical (8-bit, 16-bit or 32-bit). Data assembly or disassembly is not supported.

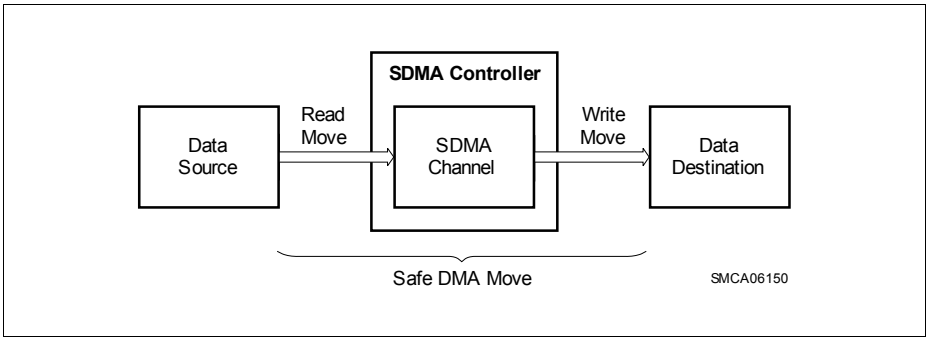


Figure 13-2 SDMA Definition of Terms

SDMA Transfer

A SDMA transfer can be composed of 1, 2, 4, 8 or 16 SDMA moves.

SDMA Transaction

A SDMA transaction is composed of several (at least one) SDMA transfers. The Transfer Count determines the number of SDMA transfers within one SDMA transaction.

Example:
1024 word (32-bit wide) transactions can be composed of 256 transfers of four SDMA word moves, or 128 transfers of eight SDMA word moves.

13.2.3 SDMA Principles

The SDMA controller supports SDMA moves from one address location to another one. SDMA moves can be requested either by hardware or by software. SDMA hardware requests are triggered by specific request lines from the peripheral modules or from other SDMA channels (see **Figure 13-3**). The number of available SDMA request lines from a peripheral module varies depending on the module functionality. Typically, the parallel occurrence of SDMA requests and interrupts requests for SDMA channels is possible. Therefore, the interrupt control unit and the SDMA controller can react independently to interrupt and SDMA requests that have been generated by one source.

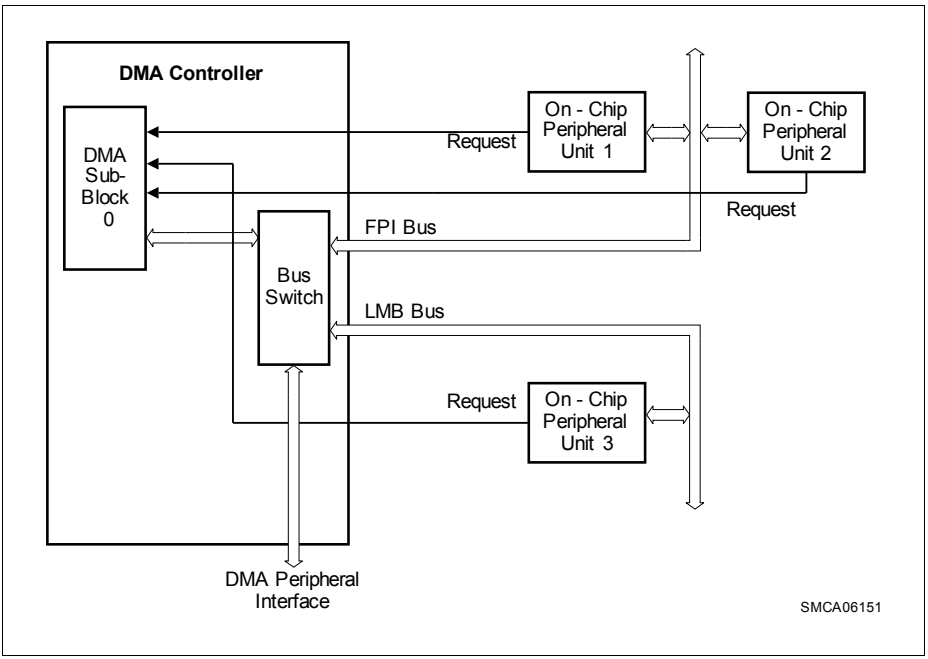


Figure 13-3 SDMA Principle

The SDMA controller mainly consists of a SDMA Sub-Block and a Bus Switch. Once configured, the SDMA Sub-Block is able to act as a master on the FPI Bus.

13.2.4 SDMA Channel Functionality

Each of the 8 SDMA channels has one associated register set containing ten 32-bit registers. These registers are numbered by one index to indicate the related SDMA channel: Index “n” refers to the channel number (n = 0-7) within the SDMA Sub-Block.

Example: CHCR04 is the Control Register of SDMA channel 4 in Sub-Block 0.

The register set of a SDMA channel register contains the following registers:

- Channel 0n Control Register CHCR0n (for details, see **Page 13-65**)
- Channel 0n Status Register CHSR0n (for details, see **Page 13-69**)
- Channel 0n Interrupt Control Register CHICR0n (for details, see **Page 13-70**)
- Channel 0n Address Control Register ADRCR0n (for details, see **Page 13-72**)
- Channel 0n Source Address Register SADR0n (for details, see **Page 13-77**)
- Channel 0n Destination Address Register DADR0n (for details, see **Page 13-78**)
- Channel 0n Shadow Address Register SHADR0n (for details, see **Page 13-79**)

13.2.4.1 Shadowed Source or Destination Address

As a typical application, an ASC module that receives data (fixed source address) has to deliver it to a memory buffer using a SDMA transaction (variable destination address). After a certain amount of data has been transferred, a new SDMA transaction should be initiated to deliver further ASC data into another memory buffer. While the destination address register is updated during a running SDMA transaction with the actual destination address, a shadow mechanism allows programming of a new destination address without disturbing the content of the destination address register. In this case, the new destination address is written into a buffer register, i.e. the shadow address register. At the start of the next SDMA transaction, the new address is transferred from this shadow address register to the destination address register without CPU intervention. This shadow mechanism avoids the CPU having to check for the end of a SDMA transaction before reprogramming address registers.

The shadow address register can be used also to store a source address. However, it cannot store source and destination address at the same time. This means that the shadow mechanism makes it possible to automatically update either a new source address, or a new destination address at the start of a SDMA transaction. If both address registers (for source and destination address) have to be updated for the next SDMA transaction, a running SDMA transaction for this channel must be finished. After that, source and destination address registers can be written before the next SDMA transaction is started.

Figure 13-4 shows the actions that take place when a source address register is updated. The update of a destination register happens in an equivalent manner.

When writing a new address to the (address of) the source or destination address register and no SDMA transaction is running, the new address value is directly written into the source or destination address register. In this case, no buffering of the address

is required. When writing a new address to the (address of) the source or destination address register and a SDMA transaction is running, no transfer to an address register can take place and SHADR0n holds the new address value that was written. For this operation, bit field ADRCR0n.SHCT must be set either to 01_B (address is a source address) or 10_B (new address is a destination address). At the start of the next SDMA transaction, the shadow transfer takes place and the content of SHADR0n is written either into SADR0n or DADR0n (ADRCR0n.SHCT must be set accordingly). After the shadow transfer, SHADR0n is set to 0000 0000_H if the shadow register write enable bit is set to 0 (ADRCR0n.SHWEN = 0). In this case (ADRCR0n.SHWEN = 0), the software can check by reading the shadow address register whether or not the shadow transfer has already taken place.

Only one address register can be shadowed while a transaction is running, because the shadow register can only be assigned either to the source or to the destination address register. Note that the shadow address register transfer has the same behavior in Single and Continuous Mode. When the shadow mechanism is disabled (ADRCR0n.SHCT = 00_B), SHADR0n is always read as 0000 0000_H.

If the shadow address register write enable bit is set to 1 (ADRCR0n.SHWEN = 1), the shadow register SHADR0n can be directly written. In this case (ADRCR0n.SHWEN = 1) the value stored in the SHADR0n is not modified when the shadow transfer takes place, and the shadow mechanism remains active and the shadow transfer will be repeated until Channel 0n is reset or until the value in SHADR is 0000 0000_H, is written into the shadow register (direct or indirect by writing to the source or destination address register according to the shadow control register ADRCR0n.SHCT).

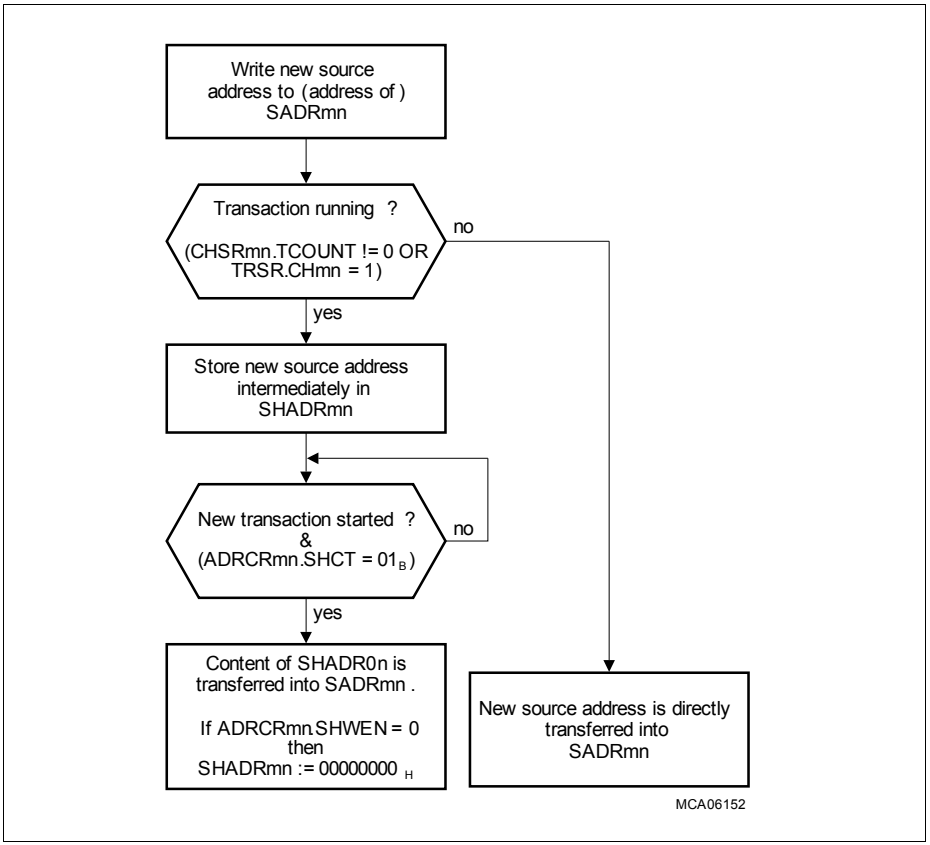


Figure 13-4 Source Address Update (m=0)

The transfer count of a SDMA transaction, stored in bit field CHCR0n.TREL, can also be programmed if the SDMA transaction is running. At the start of a SDMA transaction, TREL is transferred to bit field CHSR0n.TCOUNT, which is then updated during the SDMA transaction.

No reload of address or counter will be done if TCOUNT is not equal to 0.

The reprogramming of channel specific values (except for the selected address shadow register) should be avoided while a SDMA channel is active.

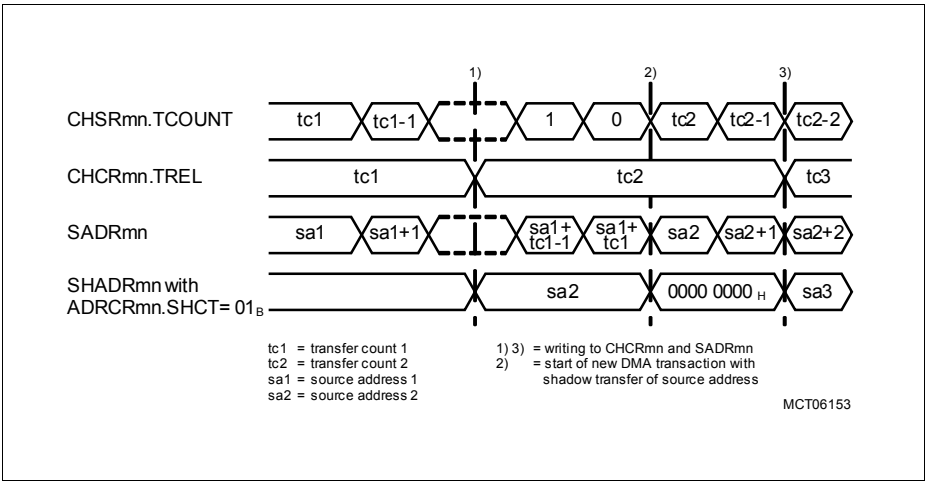


Figure 13-5 Shadow Source Address and Transfer Count Update with ADRCR0n.SHWEN = 0 (m = 0)

Figure 13-5 shows how the contents of the source address register SADR0n and the transfer count CHSR0n.TCOUNT are updated during two SDMA transactions with a shadowed source address and transfer count update.

At reference point 2) the SDMA transaction 1 is finished and SDMA transaction 2 is started. At 1) the SDMA channel is reprogrammed with two new parameters for the next SDMA transaction: Transfer count tc2 and source address sa2. Source address sa2 is buffered in SADR0n and transferred to SADR0n when the new SDMA transaction is started at 2). At this time, transfer count tc2 is also transferred to CHSR0n.TCOUNT. Note that the shadow address register is only reset by hardware to 0000 0000_H as shown in this example, if the write enable bit is set to 0 (ADRCR0n.SHWEN = 0).

13.2.4.2 SDMA Channel Request Control

Figure 13-6 shows the control logic for SDMA requests that is implemented for each SDMA channel.

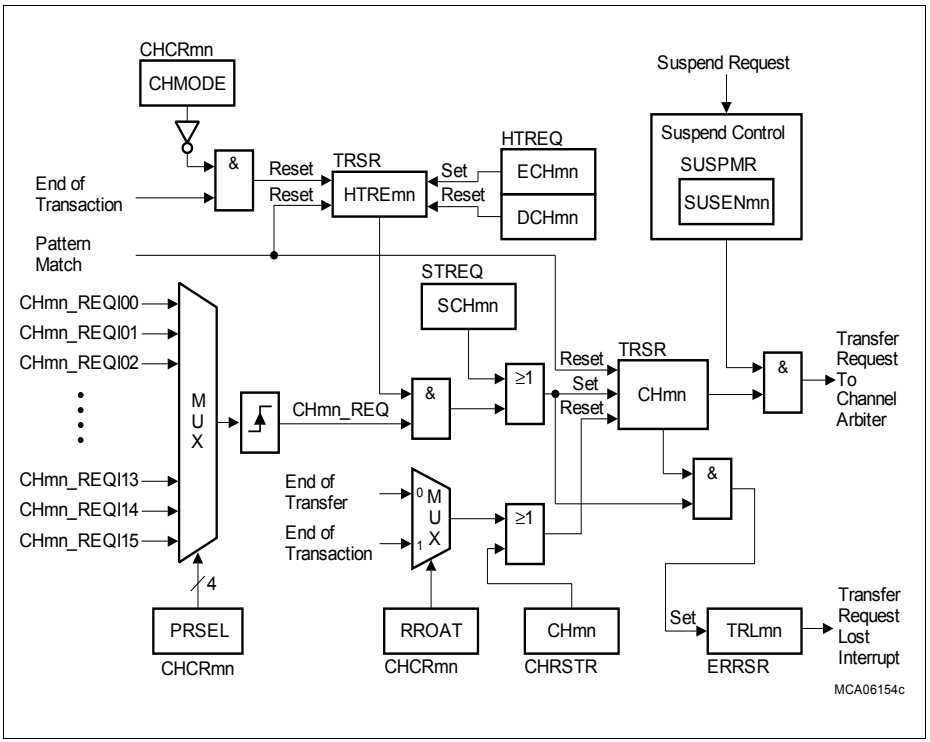


Figure 13-6 Channel Request Control(m = 0)

Two different types of SDMA requests are possible:

- Hardware SDMA requests
- Software SDMA requests

The hardware request CH0n_REQ can be connected to one of sixteen possible hardware request input lines as selected by bit field CHCR0n.PRSEL. The hardware request input structure for CHCR0n.PRSEL includes a ´positive edge detector´ as the SDMA channels requires single pulse requests.

Hardware requests are enabled/disabled by status bit TRSR.HTRE0n. HTRE0n can be set/reset by software or by hardware in Single Mode at the end of a SDMA transaction. A software request can be generated by setting bit STREQ.SCH0n.

Status flag TRSR.CH0n indicates whether or not a software or hardware generated SDMA request for SDMA channel 0n is pending. TRSR.CH0n can be reset by software or by hardware at the end of a SDMA transfer (RROAT = 0) or at the end of a SDMA transaction (RROAT = 1).

If a software or a hardware SDMA request is detected for channel 0n while TRSR.CH0n is set, a request lost event occurs. This error event indicates that the SDMA is already processing a transfer and that another transfer has been requested before the end of the previous one. In this case, bit ERRSR.TRL0n will be set and a transfer lost interrupt can be generated.

13.2.4.3 SDMA Channel Operation Modes

The operation mode of a SDMA channel is individually programmable for each SDMA channel n. Basically, a SDMA channel can operate in the following modes:

- Software controlled mode
- Hardware controlled mode, in Single or Continuous Mode

In software-controlled mode, a SDMA channel request is generated by setting a control bit. In hardware-controlled mode, a SDMA channel request is generated by request signals typically generated by on-chip peripheral units.

In hardware-controlled Single Mode, a SDMA channel n becomes disabled by hardware after the last SDMA transfer of its SDMA transaction. In hardware-controlled Continuous Mode, a SDMA channel n remains enabled after the last SDMA transfer of its SDMA transaction.

In hardware- and software-controlled mode, a SDMA request signal can be configured to trigger a complete SDMA transaction or one single transfer.

Software-controlled Modes

In software-controlled mode, one software request starts one complete SDMA transaction or one single SDMA transfer. Software-controlled modes are selected by writing HTREQ.DCH0n = 1. This forces status flag TRSR.HTRE0n = 0 (hardware request of SDMA channel 0n is disabled).

The software-controlled mode that initiates one complete SDMA transaction to be executed is selected for SDMA channel 0n by the following write operations:

- CHCR0n.RROAT = 1
- STREQ.SCH0n = 1

Setting STREQ.SCH0n to 1 (this is the software request) causes the SDMA transaction of SDMA channel 0n to be started and TRSR.CH0n to be set. At the start of the SDMA transaction, the value of CHCR0n.TREL is loaded into CHSR0n.TCOUNT (transfer count or tc) and the SDMA transfers are executed. After each SDMA transfer, TCOUNT becomes decremented and next source and destination addresses are calculated.

When TCOUNT reaches the 0, SDMA channel 0n becomes disabled and status flag TRSR.CH0n is reset. Setting STREQ.SCH0n again starts a new SDMA transaction of SDMA channel 0n with the parameters as actually defined in the channel register set.

The software-controlled mode that initiates a single SDMA transfer to be executed is selected for SDMA channel 0n by the following write operations:

- CHCR0n.RROAT = 0
- STREQ.SCH0n = 1, repeated for each SDMA transfer

When CHCR0n.RROAT = 0, TRSR.CH0n becomes reset after each SDMA transfer of the SDMA transaction and a new software request (writing STREQ.SCH0n = 1) must be generated for starting the next SDMA transfer.

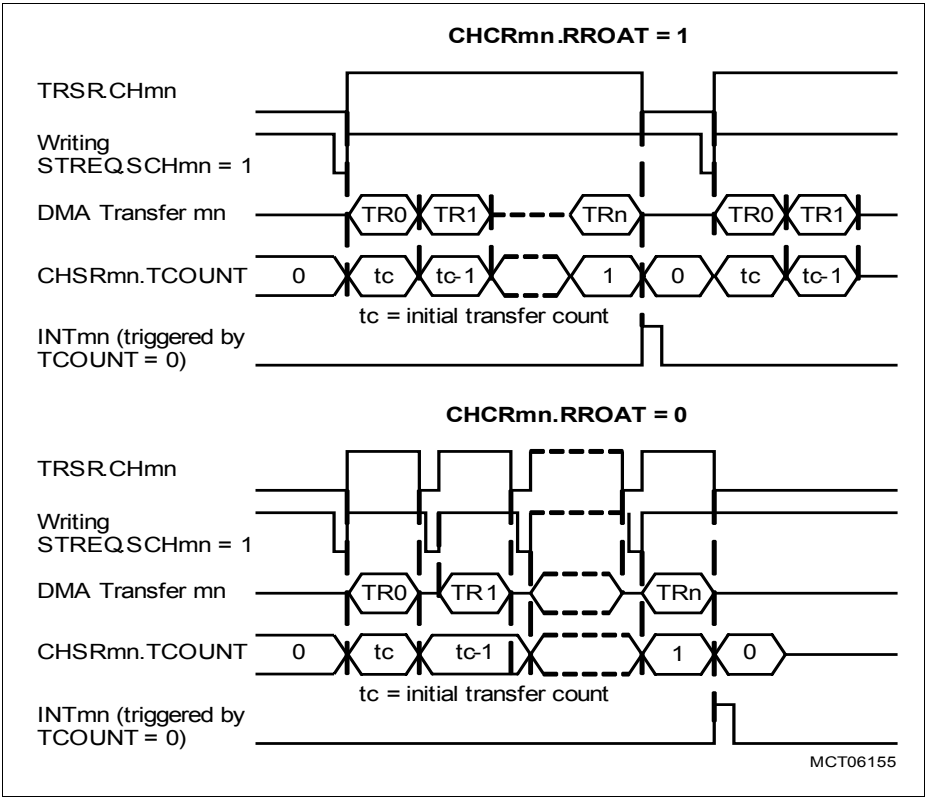


Figure 13-7 Software Controlled Mode Operation (m = 0)

Hardware-controlled Modes

In hardware-controlled modes, a hardware request signal starts a SDMA transaction or a single SDMA transfer. There are two hardware-controlled modes available:

- **Single Mode:**
  Hardware requests are disabled by hardware after a SDMA transaction
- **Continuous Mode:**
  Hardware requests are not disabled by hardware after a SDMA transaction

Hardware-controlled Single Mode

In hardware-controlled Single Modes, one hardware request starts one complete SDMA transaction or one single SDMA transfer. The hardware-controlled Single Mode that initiates one complete SDMA transaction to be executed for SDMA channel 0n is selected by the following operations:

- CHCR0n.CHMODE = 0
- CHCR0n.RROAT = 1
- Selecting one of the sixteen hardware request inputs via CHCR0n.PRSEL
- HTREQ.ECH0n = 1

Setting HTREQ.ECH0n to 1 causes the hardware request CH0n_REQ of channel 0n to be enabled (TRSR.HTRE0n = 1). Whenever the hardware request CH0n_REQ becomes active, the value of CHCR0n.TREL is loaded into CHSR0n.TCOUNT and the SDMA transaction is started by executing its first SDMA transfer. After each SDMA transfer, TCOUNT becomes decremented and next source and destination addresses are calculated. When TCOUNT reaches the 0, SDMA channel 0n becomes disabled and status flags TRSR.CH0n and TRSR.HTRE0n are reset. In order to start a new hardware-controlled SDMA transaction, hardware requests must be enabled again by setting TRSR.HTRE0n through HTREQ.ECH0n = 1. The hardware request disable function in Single Mode is typically needed when a reprogramming of the SDMA channel register set (addresses, transfer count) is required before the next hardware triggered SDMA transaction is started.

The hardware-controlled Single Mode in which each single SDMA transfer has to be requested by a hardware request signal is selected as described above, with one difference:

- CHCR0n.RROAT = 0

In this operation mode, TRSR.CH0n becomes reset after each SDMA transfer of the SDMA transaction, and a new hardware request at CH0n_REQ must be generated for starting the next SDMA transfer.

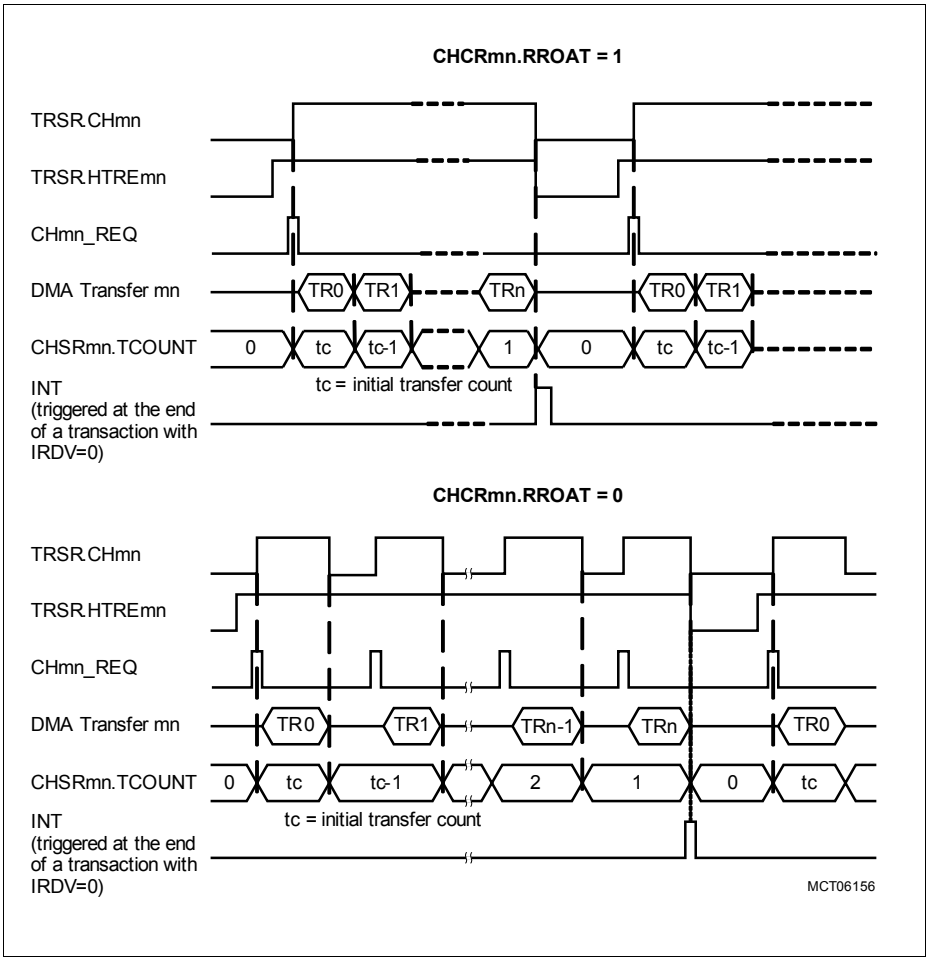


Figure 13-8 Hardware-controlled Single Mode Operation (m = 0)

Hardware-controlled Continuous Mode

In hardware-controlled Continuous Mode (CHCR0n.CHMODE = 1), the hardware transaction request enable bit HTRE0n is not reset at the end of a SDMA transaction. A new transaction of SDMA channel 0n with the parameters actually stored in the channel register set of SDMA channel 0n is started each time when CHSR0n.TCOUNT = 0 at the end of the SDMA transaction. No software re-enable for a hardware request at CH0n_REQ is required.

Combined Software/Hardware-controlled Mode

Figure 13-9 shows how software- and hardware-controlled modes can be combined. In the example, the first SDMA transfer is triggered by software when setting STREQ.SCH0n. Hardware requests are still disabled. After hardware requests have been enabled by setting HTREQ.ECH0n, subsequent SDMA transfers are triggered now by hardware request coming from the CH0n_REQ line.

In the example, SDMA channel 0n operates in Single Mode (CHCR0n.CHMODE = 0). In this mode, TRSR.HTRE0n becomes reset by hardware when CHSR0n.TCOUNT = 0 at the end of the SDMA transaction.

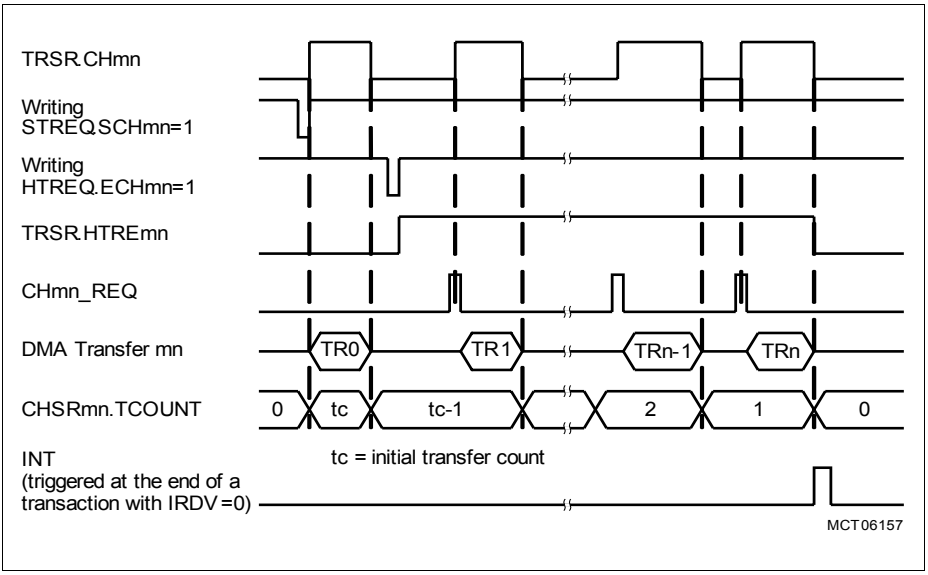


Figure 13-9 Transaction Start by Software, Continuation by Hardware (m = 0)

If an SDMA channel is configured to be triggered by parallel hardware and software requests then if the requests collide in the same clock cycle then a Transaction/Transfer Request Lost event will be flagged in the SDMA Error Status Register.

13.2.4.4 Error Conditions

The bus error flag ERRSR.FPIER indicates an FPI Bus error (SPB) that occurred during a source move (read or write) of a SDMA module transaction.

The source error flag ERRSR.ME0SER indicates than an error occurred during source move (read) of a SDMA transaction of SDMA Sub-Block 0.

The destination error flag ERRSR.ME0DER indicates than an error occurred during destination move (write) of a SDMA transaction of SDMA Sub-Block 0
The transaction lost error flag ERRSR.TRL0n indicates if a SDMA request for a SDMA channel 0n has been lost.

In the case of a read error, the write action is not executed, but the destination address is updated.

In the case of multiple errors, the error bits are set according to the error situations. This means that more than bus error flag can be set and that source/destination flags can be set.

13.2.4.5 Channel Reset Operation

A SDMA transaction of SDMA channel 0n can be stopped (channel is reset) by setting bit CHRSTR.CH0n. When a read or write On Chip Bus transaction of SDMA channel 0n is executed at the time when CHRSTR.CH0n is set, this On Chip Bus transaction is finished normally. This behavior guarantees data consistency.

When CHRSTR.CH0n is set to 1:

- Bits TRSR.HTRE0n, TRSR.CH0n, ERRSR.TRL0n, INTSR.ICH0n, INTSR.IPM0n, WRPSR.WRPD0n, WRPSR.WRPS0n, CHSR0n.LXO, and bit field CHSR0n.TCOUNT are reset.
- Source and destination address register will be set to the wrap boundary. SHADR0n will be cleared.
- All automatic functions are stopped for channel 0n.

A user program must execute the following steps for resetting a SDMA channel:

1. If hardware requests are enabled for the SDMA channel 0n, disable the SDMA channel 0n hardware requests by setting HTREQ.ECH0n = 0.
2. Writing a 1 to CHRSTR.CH0n.
3. Waiting (polling) until CHRSTR.CH0n = 0.

A user program should execute the following steps for restarting a SDMA channel after it was reset:

1. Optionally (re-)configuring the address and other channel registers.
2. Restarting the SDMA channel 0n by setting HTREQ.ECH0n = 1 for hardware requests or STREQ.SCH0n = 1 for software requests.

The value of CHCR0n.TREL is copied to CHSR0n.TCOUNT when a new SDMA transaction is requested and shadow address register contents is not equal $0000\ 0000_H$.

13.2.4.6 Transfer Count and Move Count

The move count determines the number of moves (consisting of one read and one write each) to be done in each transfer. It allows the user to indicate to the SDMA the number of moves to be done after one request. The number of moves per transfer is selected by the block mode settings (CHCR0n.BLKM).

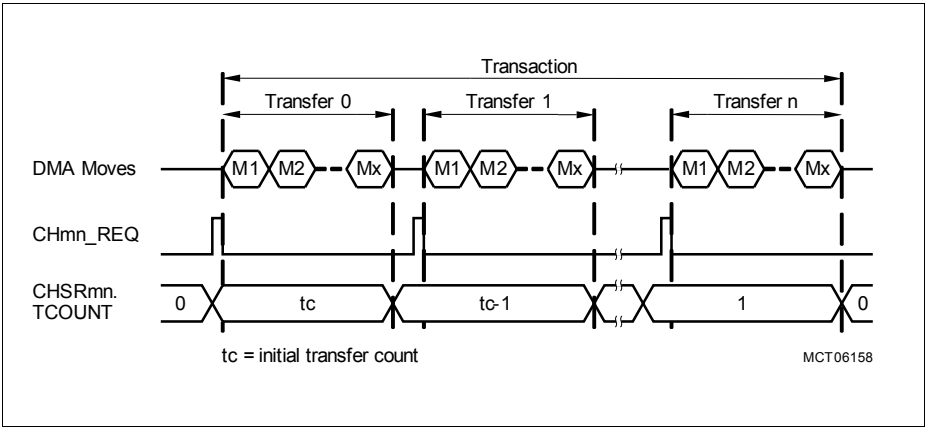


Figure 13-10 Transfer and Move Count (m = 0)

After a SDMA move, the next source and destination addresses are calculated. Source and destination addresses are calculated independently of each other. The following address calculation parameters can be selected:

- The address offset, which is a multiple of the selected data width
- The offset direction: addition, subtraction, or none (unchanged address)

Control bits in address control register ADRCR0n determine how the addresses are incremented/decremented. Further, the data width as defined in CHCR0n.CHDW is taken into account for the address calculation.

Figure 13-11 and **Figure 13-12** show two examples of address calculation. In both examples, a data width of 16-bit (CHCR0n.CHDW = 01_B) is assumed.

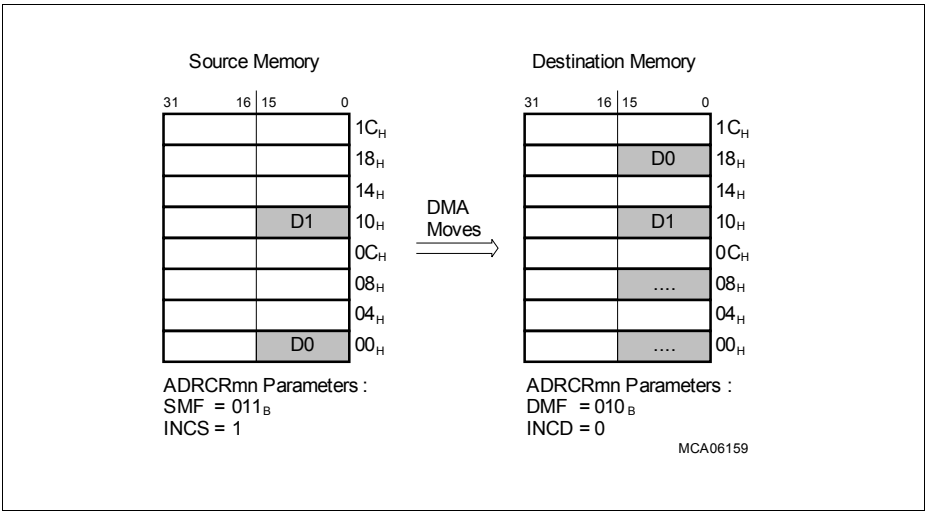


Figure 13-11 Programmable Address Modification - Example 1 (m = 0)

In **Figure 13-11**, 16-bit half-words are transferred from a source memory with an incrementing source address offset of 10_H to a destination memory with decrementing destination addresses offset of 08_H.

In **Figure 13-12**, 16-bit half-words are transferred from a source memory with an incrementing source address offset of 02_H to a destination memory with incrementing destination addresses offset of 04_H.

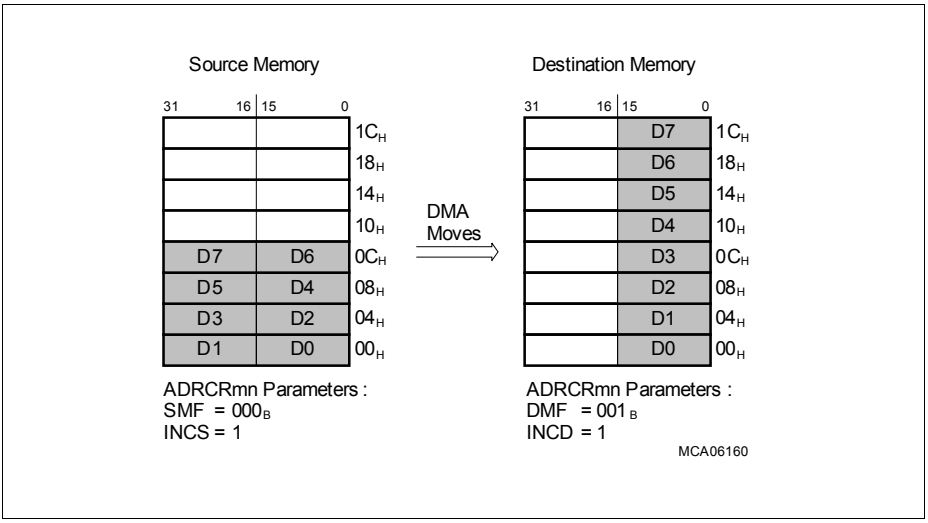


Figure 13-12 Programmable Address Modification - Example 2 (m = 0)

13.2.4.7 Circular Buffer

Destination and source address can be configured to build a circular buffer separately for source and destination data. Within this circular buffer, addresses are updated as defined in **Figure 13-11** and **Figure 13-12** with a wrap-around at the buffer limits. The circular buffer length is determined by bit fields ADRCR0n.CBLS (for the source buffer) and ADRCR0n.CBLD (for the destination buffer). These 4-bit wide bit fields determine which bits of the 32-bit address remain unchanged at an address update. Possible buffer sizes of the circular buffers can be 2^{CBLS} or 2^{CBLD} bytes (= 1, 2, 4, 8, 16, … up to 32k bytes).

When source or destination addresses are updated (incremented or decremented) after a SDMA move, all upper bits [31:CBLS] of source address and [31:CBLD] of destination address are frozen and remain unchanged, even if a wrap-around from the lower address bits [CBLS:0] or [CBLD:0] occurred. This address-freezing mechanism always causes the circular buffers to be aligned to a multiple integer value of its size.

If the circular buffer size is less or equal than the selected address offset (see **Table 13-7**), the same circular buffer address will always be accessed.

13.2.5 Transaction Control Engine

The Transaction Control Unit in the SDMA Sub-Block, as shown in the SDMA Controller block diagram in **Figure 13-1**, contains a Channel Arbiter and a Move Engine.

The Channel Arbiter arbitrates the transfer requests of the SDMA channels, and submits the transfers parameters of the SDMA channel with the highest channel priority that are needed for a SDMA transfer to the Move Engine. SDMA channels within a SDMA Sub-Block have a two-level programmable channel priority as defined by bit CHCR0n.CHPRIO. When two transfer requests of two different SDMA channels with identical channel priority become active at the same time, the SDMA channel with the lowest channel number (n) is serviced first.

The Move Engine handles the execution of a SDMA transfer that has been detected by the Channel Arbiter to be the next one. The Move Engine requests the required buses and loads or stores data according to the parameters of a SDMA transfer. It is able to wait if a targeted bus is not available. In the Move Engine, a SDMA transfer of a SDMA transaction cannot be interrupted and always get finished. This means that a SDMA transfer, which can also be composed of several data moves (read move and write move), cannot be interrupted by a transfer of another SDMA channel.

After a SDMA transfer is finished, the Move Engine will send back the actualized address register information to the related SDMA channel. Possible error conditions are also reported.

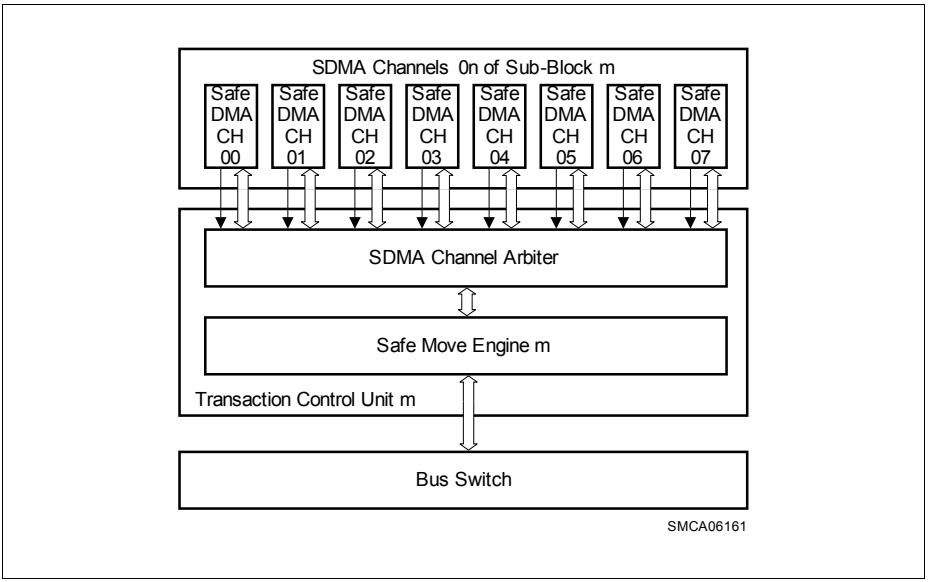


Figure 13-13 Transaction Control Engine (m = 0)

13.2.6 Bus Switch, Bus Switch Priorities

The Bus Switch of the SDMA controller provides the connection from the SDMA Sub-Block to the On Chip Bus System Peripheral Bus master interface and to the SDMA Peripheral Interface (see **Figure 13-14**).

The SDMA module working frequency is identical to the FPI Bus frequency.

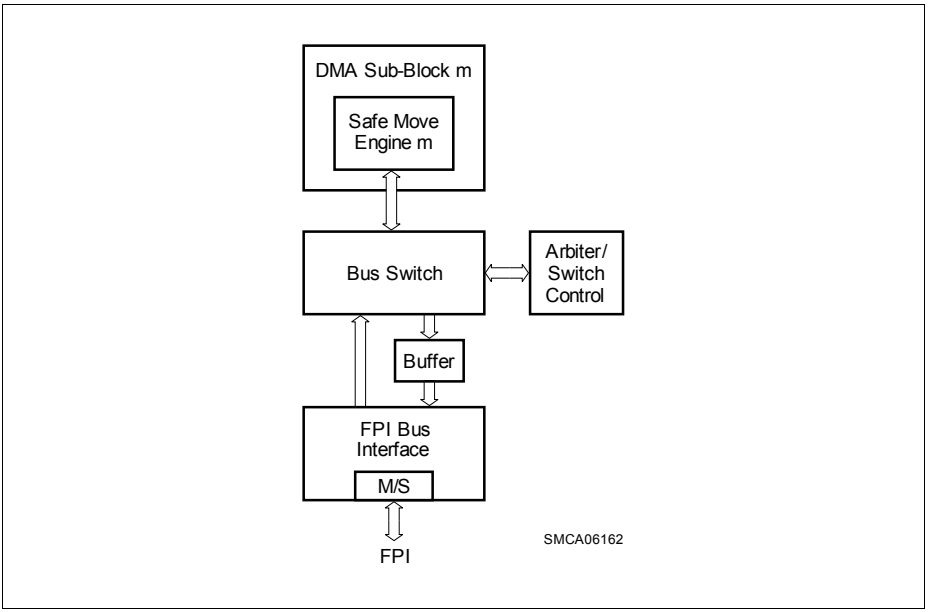


Figure 13-14 Bus Switch

One access can be buffered in the bus interface.

Note: The accesses of the SDMA Move Engine's bus interfaces to the On Chip Bus interfaces are always done in Supervisor Mode.

A Move Engine Write has priority over a Move Engine Read.

13.2.7 SDMA Module: On Chip Bus Access Rights, RMW support

All accesses triggered by the SDMA Move Engine are always done in SV mode.

The SDMA module does not support read/modify write instructions.

13.2.8 SDMA On Chip Bus FPI Master Interface

The SDMA On Chip Bus FPI Master Interfaces supports:

- single data read and write transactions (8bit, 16bit, 32bit)
- de-assertion of request after retry in order to prevent bus blocking.

The move engine generates read - write sequences and supports only one transaction at a time.

13.2.9 On-Chip Debug Capabilities

The SDMA controller in the TC1798 provides some debugging capabilities. These debug features support:

- Soft-suspend Mode of SDMA channels
- Break signal generation
- Trace signal generation

In Soft-suspend mode, the operations of SDMA channels are stopped. Pending read or write transfers in the SDMA module On Chip Bus Master Interface are finished. Under certain conditions also a break signal is generated for the on-chip debug support logic. Further, SDMA trace information can be output.

In Soft-suspend mode, the SDMA module provides access to all control registers of the SDMA module.

13.2.9.1 Hard-suspend Mode

The Hard-Suspend Mode is controlled in the TC1798 SDMA module CLC register.

13.2.9.2 Soft-suspend Mode

The TC1798 on-chip debug control unit is able to generate a Soft-suspend Mode request (SUSREQ) for the SDMA controller. When this soft-suspend request becomes active, the state of a SDMA channel becomes frozen regarding hardware changes to ensure that the state of the SDMA channels can be analyzed by reading the register contents. Pending read or write transfers in the SDMA module On Chip Bus FPI Master Interface are finished. The SDMA controller signals its soft suspend mode back to the on-chip debug control via an Soft-suspend acknowledge. The Soft-suspend acknowledge becomes active when all SDMA channels 0n that are enabled for the Soft-suspend Mode have set its suspend active status flag SUSPMR.SUSAC0n.

Soft-suspend Mode of SDMA channel 0n is entered if its suspend enable bit SUSEN0n in the Suspend Mode Register SUSPMR is set. When SUSREQ becomes active, the operation of all SDMA channels 0n that are enabled for Soft-suspend Mode is stopped automatically after its current SDMA transfers have been finished in the transaction control unit. Afterwards, the suspend active status flag SUSPMR.SUSAC0n is set, indicating that SDMA channel 0n is in Soft-suspend Mode. SDMA channels that are disabled for Suspend Mode (SUSEN0n = 0) continue with its normal operation.

In Soft-suspend Mode, register contents can be modified. These modifications are taken into account for further SDMA transactions or SDMA transfers of the related SDMA channel after Suspend Mode has been left again. Suspend Mode of SDMA channel 0n is left and its normal operation continues if either the SUSREQ signal becomes inactive, or if the enable bit SUSEN0n is reset by software.

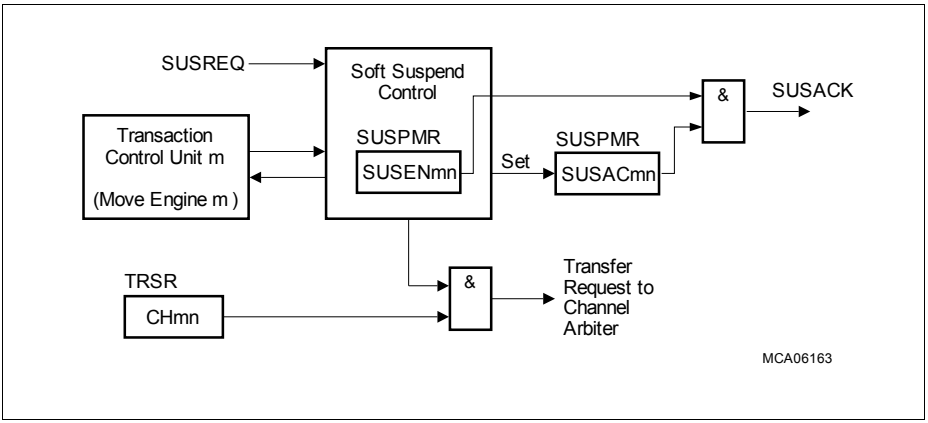


Figure 13-15 Soft-suspend Mode Control (m = 0)

13.2.9.3 Break Signal Generation

The SDMA controller provides one BREAK output signal that is generated for the on-chip debug support logic (see **Figure 13-16**). The SDMA sub-block is able to detect two break conditions:

- Transaction lost interrupt has occurred
- SDMA request transitions, indicated by bits TRSR.CH0n

The output lines of the two break conditions in the SDMA sub-block are OR-ed together to the BREAK output signal.

A transaction lost break condition occurs in SDMA Sub-Block whenever at least one of its eight transaction lost interrupts becomes active, and when enable bit OCDSR.BRL0 is set. The transaction lost interrupts do not generate a break condition if OCDSR.BRL0 = 0. Transaction interrupt control is described in **Section 13.2.10.2**.

The second break condition of SDMA Sub-Block becomes active when the transaction request bit TRSR.CH0n of one of its eight SDMA channels n (as selected by OCDSR.BCHSn) indicates a transition of its state. The CH0n transition type (change from ´no request is pending´ to ´request is pending´, change from ´request is pending´ to ´no request is pending´, changes in both directions) is selected by bit field OCDSR.BTCRn.

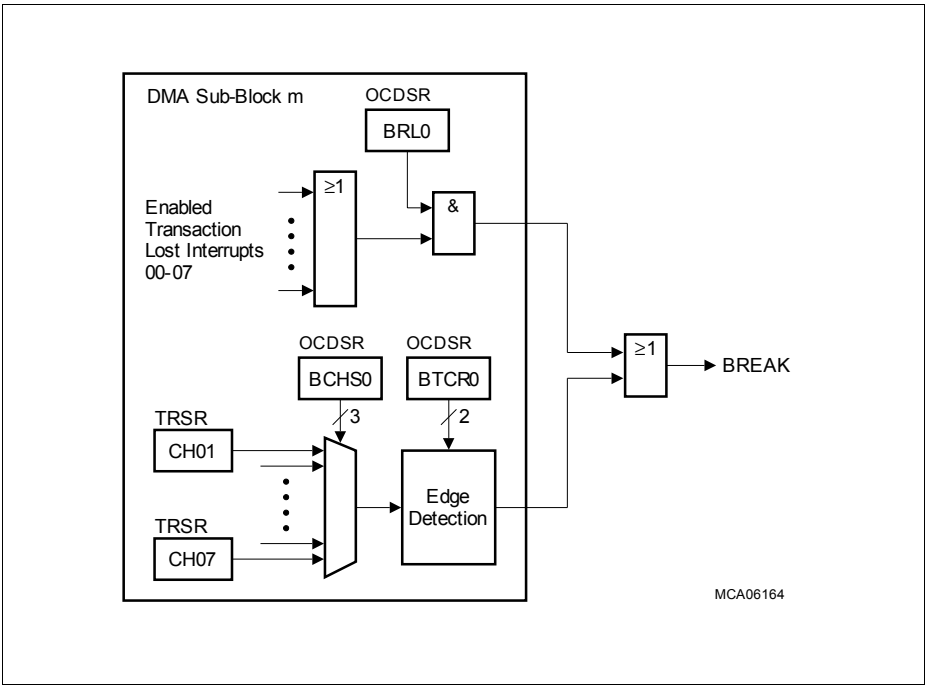


Figure 13-16 SDMA Break Event Generation (m = 0)

13.2.10 Interrupts

The interrupt structure of the SDMA controller is a very flexible control logic that allows an interrupt coming from an interrupt source within four interrupt source types to be connected to each of the sixteen interrupt outputs. This permits, for example, SDMA channels that very rarely generate interrupts to share one interrupt node. The remaining interrupt nodes can be assigned to dedicated SDMA channels to reduce the interrupt overhead for these channels. The four interrupt source types are:

- Channel interrupts
- Transaction lost interrupt
- Move Engine interrupts
- Wrap buffer interrupts

Some of the interrupt functions are common to all of the four interrupt source types. An interrupt event, internally generated as a request pulse, is always stored in an interrupt status flag. This interrupt status flag can be reset by software. Further, the interrupt event can be enabled or disabled. When an interrupt event is enabled, a 4-bit Interrupt Node Pointer determines which of the sixteen interrupt outputs will be activated.

The following sections describe each of the four interrupt source types in more detail.

13.2.10.1 Channel Interrupts

Each SDMA channel 0n has one associated channel interrupt. It can always be activated after a SDMA transfer, or when CHSR0n.TCOUNT matches with the value of bit field CHICR0n.IRDV after it has been decremented after a SDMA transfer. The pattern detection interrupts that are combined with the channel interrupts (one common Interrupt Node Pointer CHICR0n.INTP) are activated when the pattern detection interrupt of SDMA channel 0n becomes active (when enabled by CHCR0n.PATSEL not equal 00_B).

A channel interrupt of SDMA channel 0n is indicated when status flag INTSR.ICH0n is set. The status flags ICH0n and IPM0n can be reset together by software when setting bit INTCR.CICH0n (or CHRSTR.CH0n). The channel interrupt of SDMA channel 0n is enabled when bit CHICR0n.INTCT[1] is set. The channel interrupt pointer CHICR0n.INTP determines which of the interrupt outputs SR[15:0][1)] will be activated on an active channel interrupt or pattern detection interrupt. Note that the signal that is set signal for the ICH0n flag is available as CH0n_OUT signal at the SDMA module boundary.

Bit CHICR0n.INTCT[0] selects these two types of interrupt sources. For the compare operation, bit field IRDV (4-bit) is zero-extended to 10-bit and then compared with the 10-bit TCOUNT value. This means that a TCOUNT match interrupt can be generated after one of the last 16 SDMA transfers of a SDMA transaction. Note that with

1) In the TC1798, only SR[7:0] are connected to interrupt nodes. SR[8:15] are used for SDMA channel triggering/connections.

IRDV = 0000_B, the match interrupt is generated at the end of a SDMA transaction (after the last SDMA transfer).

The pattern detection interrupt is indicated when status flag INTSR.IPM0n is set. The status flags IPM0n and ICH0n can be reset together by software when setting bit INTCR.CICH0n (or CHRSTR.CH0n). The pattern detection interrupt of SDMA channel 0n is enabled when bit CHCR0n.PATSEL is set to a value not equal to 00_B. The channel interrupt pointer CHICR0n.INTP defines which of the interrupt outputs SR[15:0] will be activated on a pattern detection interrupt or the channel interrupt pointer CHICR0n.INTP determines which of the interrupt outputs SR[15:0][1] will be activated on a pattern detection or channel interrupt.

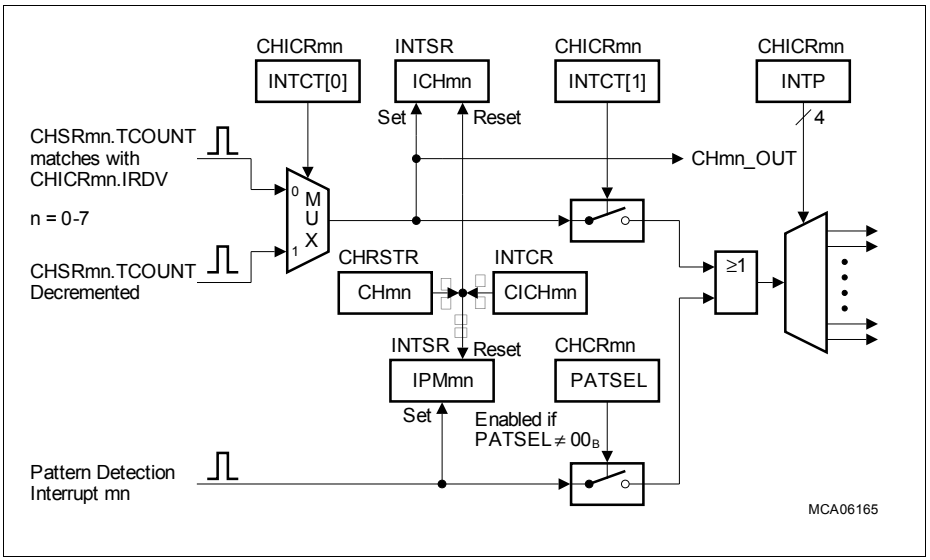


Figure 13-17 Channel Interrupts (m = 0)

1) In the TC1798, SR[7:0] are connected to interrupt nodes. SR[8:15] are used for SDMA channel triggering/connections.

13.2.10.2 Transaction Lost Interrupt

Each SDMA channel 0n is able to detect a transaction request lost condition. This condition becomes true when a new hardware or software SDMA request occurs while the previous transaction or transfer on SDMA channel 0n is not finished, indicated by TRSR.CH0n still set. If such a transaction request lost condition occurs, bit ERRSR.TRL0n is set. The transaction lost interrupts of all SDMA channels are OR-ed together to one common transaction lost interrupt that can be directed to one of the interrupt outputs SR[15:0][1] by setting the transaction lost interrupt pointer EER.TRLINP with a corresponding value.

A transaction request lost condition of SDMA channel 0n is indicated by status flag ERRSR.TRL0n, which can be reset by setting bit CLRE.CTL0n or CHRSTR.CH0n. The transaction lost interrupt for SDMA channel 0n is enabled when bit EER.ETRL0n is set.

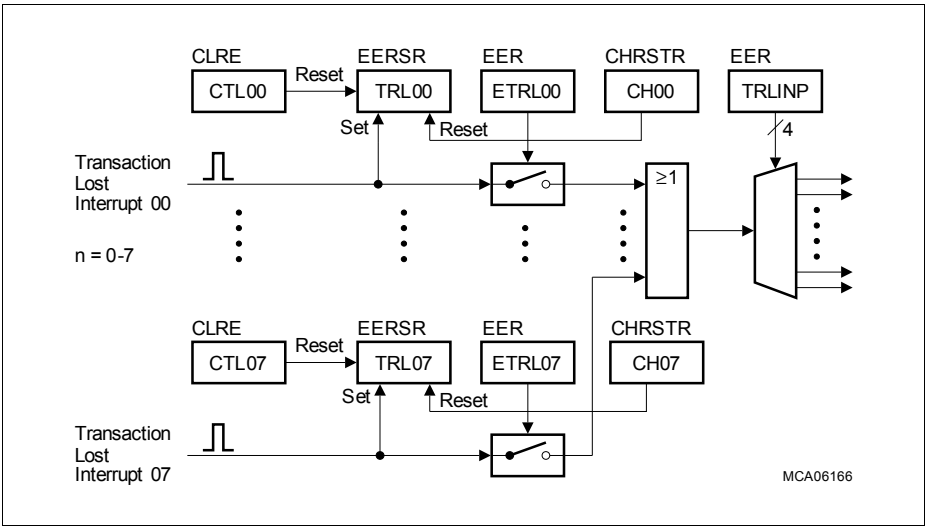


Figure 13-18 Transaction Lost Interrupt

1) In the TC1798 SR[7:0] are connected to interrupt nodes. SR[15:8] are used as SDMA channel trigger signals.

13.2.10.3 Move Engine Interrupt

The Move Engine is able to detect error conditions that occur during accesses to the FPI Bus interfaces of the Bus Switch (see **Figure 13-14**). Two error conditions can be detected:

- Source error
- Destination error

A source error indicates an FPI Bus error that occurred during a read move from the data source. A destination error indicates an FPI Bus error that occurred during a write move to the data destination.

A source error of Move Engine 0 is indicated by the status flag ERRSR.ME0SER. Status flag ME0SER can be reset by software when setting bit CLRE.CME0SER. The source error interrupt of the Move Engine 0 is enabled when bit EER.EME0SER is set. Separate reset, status, and enable bits are available in the Move Engine for source error condition, as well as for destination error condition. The Move Engine's interrupts can be directed to one of the interrupt outputs SR[15:0][1)] by setting the Move Engine interrupt pointer EER.ME0INP with a corresponding value.

Note that in case of a read move error, the write move is not executed but the destination address is updated.

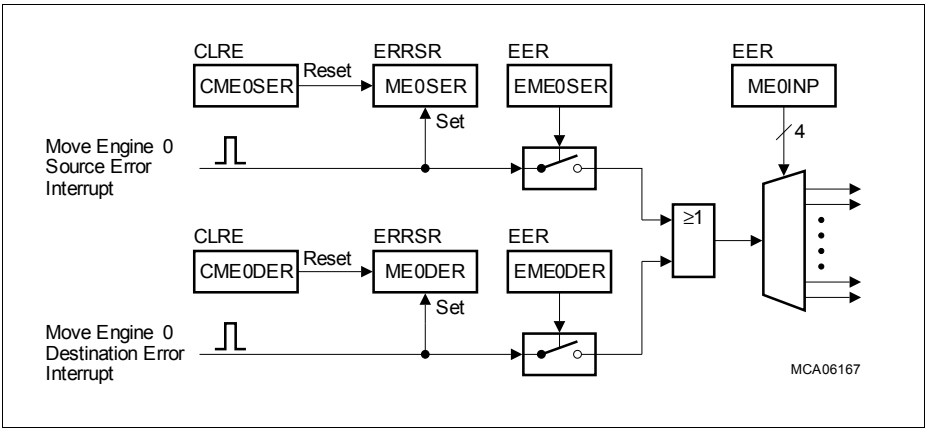


Figure 13-19 Move Engine Interrupts

1) In the TC1798 SR[7:0] are connected to interrupt nodes. SR[15:8] are used as SDMA channel trigger signals.

13.2.10.4 Wrap Buffer Interrupts

Each SDMA channel 0n is able to generate a wrap buffer interrupt for source buffer or destination buffer overflow. Further details on the pattern detection are described in **Section 13.2.11**.

A wrap source buffer interrupt of SDMA channel 0n is indicated by status flag WRPSR.WRPS0n. A wrap destination buffer interrupt of SDMA channel 0n is indicated by the status flag WRPSR.WRPD0n. Both interrupt status flags can be reset by software when bit INTCR.CWRP0n (or CHRSTR.CH0n becomes set). The wrap source buffer interrupt is enabled when bit CHICR0n.WRPSE is set. The wrap destination buffer interrupt is enabled when bit CHICR0n.WRPDE is set. The two interrupts for wrap source buffer and wrap destination buffer are OR-ed together to one common wrap buffer interrupt of SDMA channel 0n that can be directed to one of the interrupt outputs SR[15:0][1] by setting the wrap buffer interrupt pointer CHICR0n.WRPP with a corresponding value. Note that the pattern match should not be enabled while a wrap interrupt is enabled for the same channel.

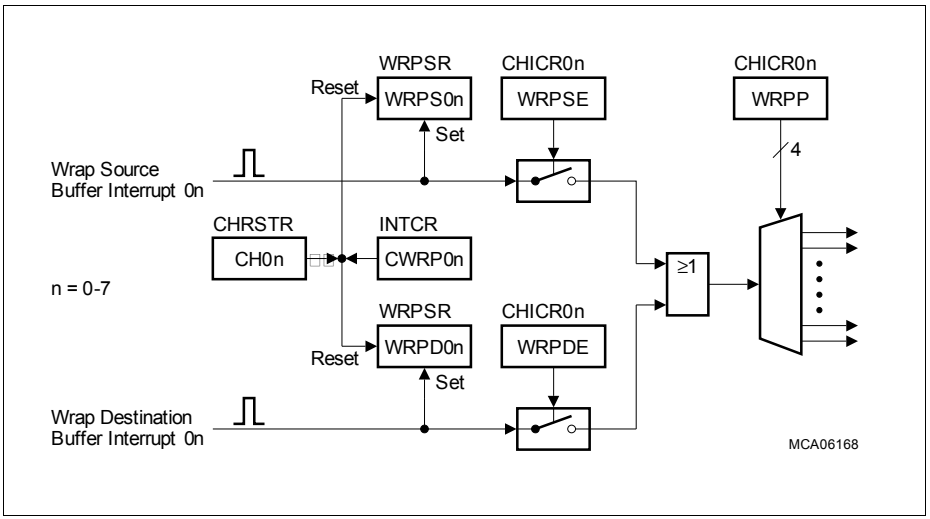


Figure 13-20 SDMA Wrap Buffer Interrupts (m = 0)

1) In the TC1798 SR[7:0] are connected to interrupt nodes. SR[15:8] are used as SDMA channel trigger signals.

13.2.10.5 Interrupt Request Compressor

The interrupt control logic of the SDMA controller uses an interrupt compressing scheme that allows high flexibility in interrupt processing. The request compressor logic as shown in **Figure 13-21** condenses the 8 + 1 + 1 + 8 = 18 interrupt sources to the sixteen interrupt outputs. Each internal interrupt source can be directed to one of the sixteen interrupt outputs SR[15:0][1)] by using a 4-bit Interrupt Node Pointer. This also allows the connection of more than one interrupt source to one interrupt output SRx. Each interrupt output SR[15:0][1)] can also be activated by writing a 1 to the corresponding bit GINTR.SIDMAx.

1) In the TC1798 SR[7:0] are connected to interrupt nodes. SR[15:8] are used as SDMA channel trigger signals.

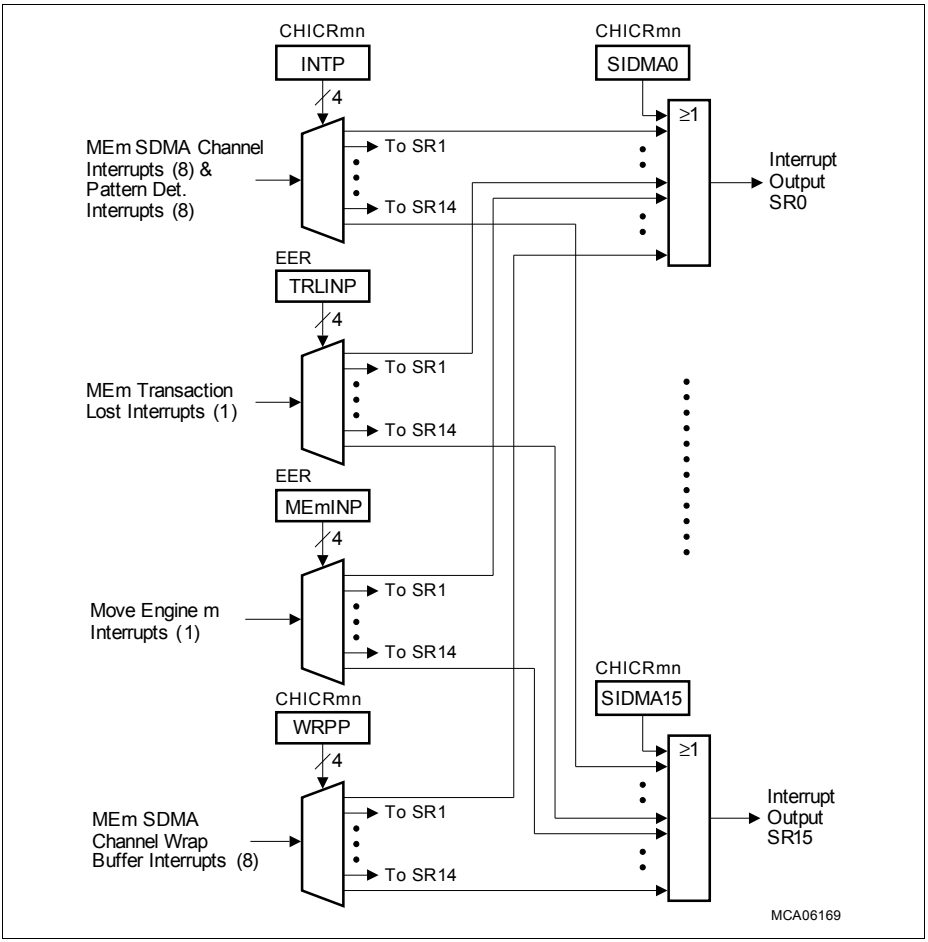


Figure 13-21 SDMA Interrupt Request Compressor (m = 0)

13.2.11 Pattern Detection

The Move Engine in the SDMA Sub-Block provides a register ME0R that contains the data that was read during the last read move. Parts of this read move data can be compared after the read move to data that is stored in the Move Engine pattern register ME0PR of SDMA Sub-Block 0. The result of this pattern compare match is always stored in a bit (LXO) of the channel status register of the SDMA channel 0n that is currently executing the SDMA move. Therefore, the pattern match result LXO of the previous read

move can also be combined together with the pattern match result of the actual read move. ME0R is overwritten with each read move.

As the compare match patterns are stored in the Move Engine 0 (register ME0PR), its compare patterns are used for all SDMA channels that are assigned to Move Engine 0 (all SDMA channels of the SDMA Sub-Block 0).

The configuration and capabilities of the pattern detection logic further depends on the settings of CHCR0n.CHDW. CHDW determines the data width for the read and write moves individually for each SDMA channel 0n. Another control bit, CHCR0n.PATSEL, selects among the different operating modes for a specific value of CHDW.

Depending on CHCR0n.PATSEL and on the positive result of the comparison, two actions follow (if CHCR0n.PATSEL=00, no action will be taken when a pattern match is detected, so the wrap interrupt can be used):

- The activation of the interrupt corresponding to the current active channel 0n using the Interrupt Pointer defined in CHICR0n.INTP.
- Reset TRSR.HTRE0n and TRSR.CH0n in order to stop the current transaction (Hardware and Software request enable). The value of CHSR0n.TCOUNT can be read out by the interrupt software.

The software will have to service the interrupt and to activate again the channel.

13.2.11.1 Pattern Compare Logic

Read move data and compare match patterns are compared on a bit-wise level. The logic as shown in **Figure 13-22** is implemented in each COMP block of **Figure 13-23**, **Figure 13-24**, and **Figure 13-25**. One COMP block controls either 8 bits or 16 bits of data and makes it possible to mask each data bit for the compare operation.

In the compare logic for one bit of the COMP block, a data bit from register ME0R is compared to the corresponding pattern bit stored in register ME0PR. If both bits are equal and a pattern mask bit stored in another part of register ME0PR is 0, the compare matched condition becomes active. When the pattern mask bit is set to 1, the compare matched condition is always active (set) for the related bit. When the compare matched conditions for each bit within a COMP block are true, the compare match output line of the COMP block becomes active.

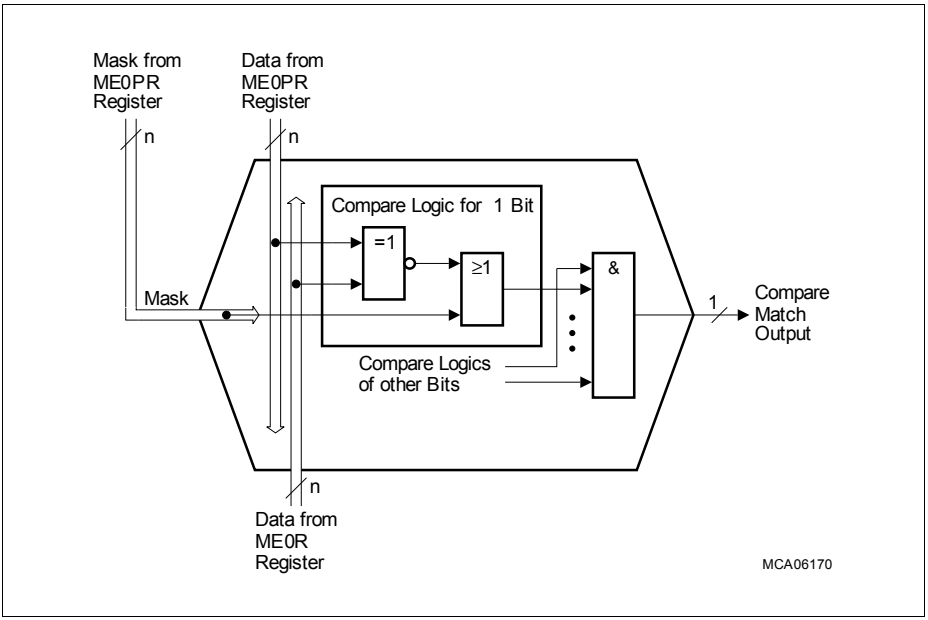


Figure 13-22 Pattern Compare Logic (COMP Block)

13.2.11.2 Pattern Detection for 8-bit Data Width

When 8-bit channel data width is selected (CHCR0n.CHDW = 00_B), the pattern detection logic is configured as shown in **Figure 13-23**. Three compare match configurations are possible.

Table 13-1 Pattern Detection for 8-bit Data Width

CHCR0n. PATSEL	Pattern Detection Operating Modes
00_B	Pattern detection disabled
01_B	Pattern compare of RD00 to PAT00, masked by PAT02
10_B	Pattern compare of RD00 to PAT01, masked by PAT03
11_B	Pattern compare of RD00 to PAT00, masked by PAT02 of the actual read move **and** Pattern compare of RD00 to PAT01, masked by PAT03 of the previous read move of SDMA channel 0n

When 8-bit channel data width is selected, the pattern detection logic allows the byte of one read move to be compared with two different patterns. Further, after each read move the pattern match result “RD00 with PAT01, masked by PAT03” is stored in bit CHCR0n.LXO. This operating mode allows, for example, two-byte sequences to be detected in an 8-bit data stream coming from a serial peripheral unit with 8-bit data width (e.g.: recognition of carriage-return, line-feed characters). A mask operation of each compared bit is possible.

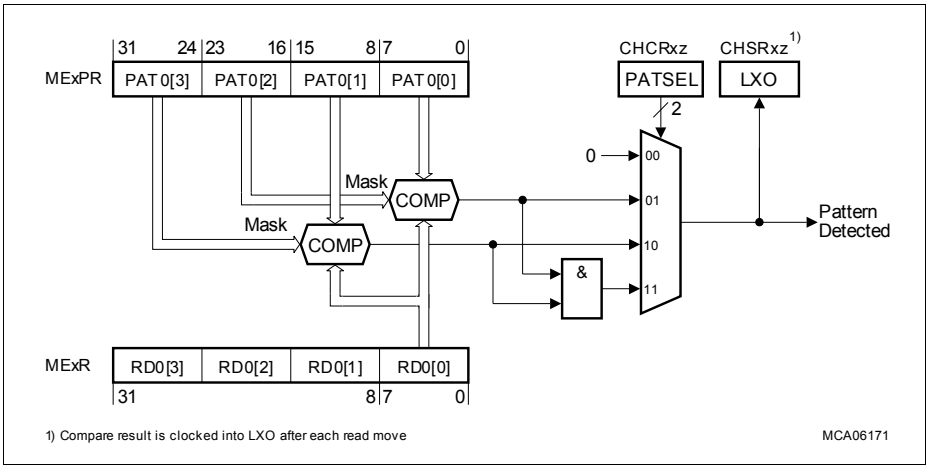


Figure 13-23 Pattern Detection for 8-bit Data Width (CHCRmn.CHDW = 00_B)

(m = 0)

13.2.11.3 Pattern Detection for 16-bit Data Width

When 16-bit channel data width is selected (CHCR0n.CHDW = 01B) the pattern detection logic can be configured as shown in **Figure 13-24**. Three compare match configurations are possible.

Table 13-2 Pattern Detection for 16-bit Data Width

CHCR0n. PATSEL	ADRCR0n. INCS	Pattern Detection Operating Modes
00_B	–	Pattern detection disabled
01_B	–	**Aligned Mode:** Pattern compare of RD0[1:0] to PAT0[1:0], masked by PAT0[3:2]
10_B	0	**Unaligned Mode 1 (Source Address Decrement):** Pattern compare of RD01 to PAT00, masked by PAT02 of the actual read move **and** Pattern compare of RD00 to PAT01, masked by PAT03 (LXO) of the previous read move of SDMA channel 0n
	1	**Unaligned Mode 2 (Source Address Increment):** Pattern compare of RD00 to PAT01, masked by PAT03 of the actual read move **and** Pattern compare of RD01 to PAT00, masked by PAT02 (LXO) of the previous read move of SDMA channel 0n
11_B	0 or 1	**Combined Mode:** Pattern compare for aligned mode (PATSEL = 01_B) **or** unaligned modes (PATSEL = 10_B)

When 16-bit channel data width is selected, the pattern detection logic makes it possible to compare the complete half-word of one read move only (aligned mode) or to compare upper and lower byte of two consecutive read moves (unaligned modes). Both modes can be combined (combined mode) too. A mask operation of each compared bit is possible.

In unaligned mode 1 (source address decremented), the high byte (RD01) of the current and the low byte (RD00) of the previous 16-bit read move are compared.

In unaligned mode 2 (source address incremented), the low byte (RD00) of the current and the high byte (RD01) of the previous 16-bit read move are compared.

If it is not known on which byte boundary (even or odd address) the 16-bit pattern to be detected is located, the combined mode should be used. This mode is the most flexible

mode that combines the pattern search capability for aligned and unaligned 16-bit data searches.

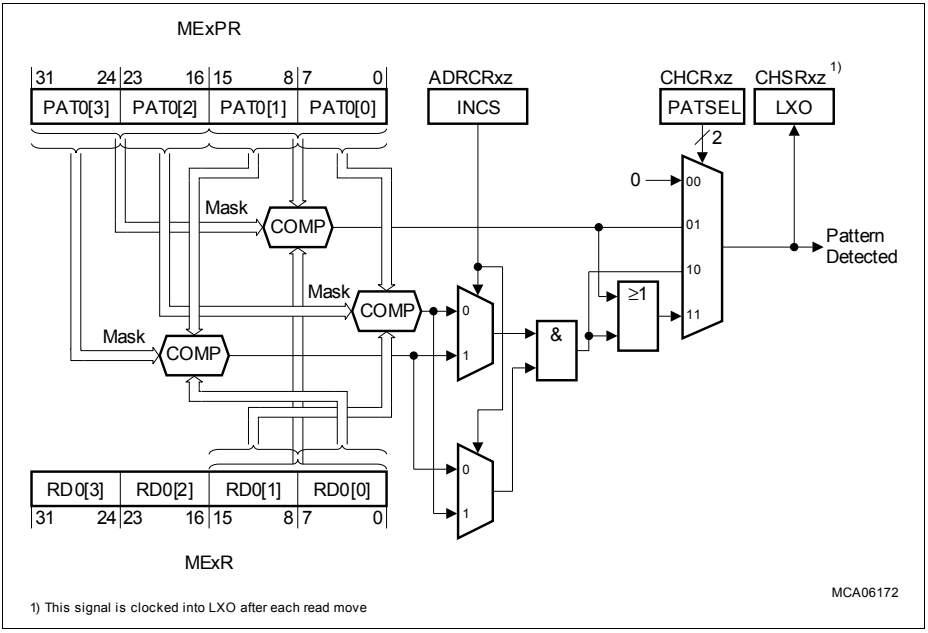


Figure 13-24 Pattern Detection for 16-bit Data Width (CHCRmn.CHDW = 01_B) (m = 0)

13.2.11.4 Pattern Detection for 32-bit Data Width

When 32-bit channel data width is selected (CHCR0n.CHDW = 10_B) the pattern detection logic is configured as shown in **Figure 13-25**. Three compare match configurations are possible.

Table 13-3 Pattern Detection for 32-bit Data Width

CHCR0n. PATSEL	Pattern Detection Operating Modes
00_B	Pattern detection disabled
01_B	Unmasked pattern compare of RD0[1:0] to PAT0[1:0]
10_B	Unmasked pattern compare of RD0[3:2] to PAT0[3:2]
11_B	Unmasked pattern compare of RD0[3:0] to PAT0[3:0]

In 32-bit channel data width mode, the pattern detection logic makes it possible to compare the lower half-word only, the upper half-word only, or the complete 32-bit word with a pattern stored in the ME0PR register. A mask operation is not possible.

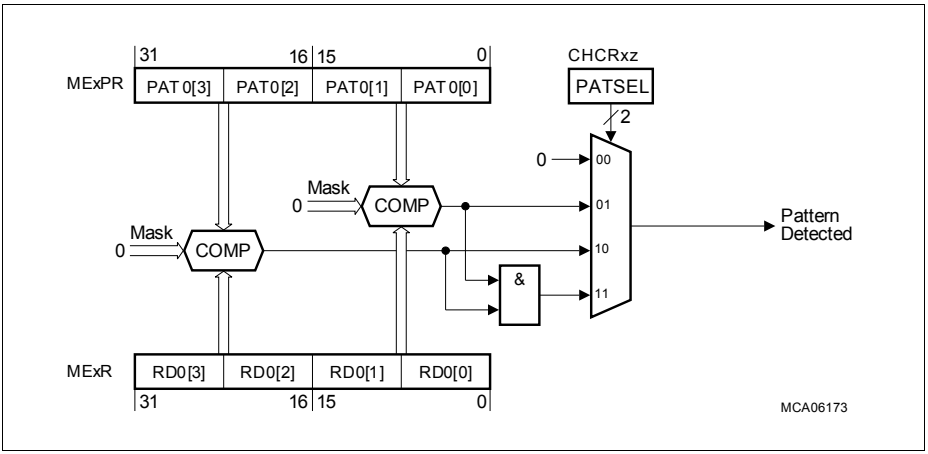


Figure 13-25 Pattern Detection for 32-bit Data Width (CHCRmn.CHDW = 10_B) (m = 0)

13.2.12 Memory Protection

The SDMA controller provides a memory protection system that makes it possible to disable read and write accesses of the Move Engine to specific parts of the memory map. Each address of a read move and write move is checked to determine if it is within the

lower and upper range limits that are enabled for the read/write access. If no address range is valid for an actual move address, a Move Engine interrupt can be generated.

Each channel has lower and upper source and destination address boundary registers. Memory protection within a channel is permanently enabled. The lower boundary register is reset to 00000000_H and the upper boundary is reset to $FFFFFFFF_H$.

13.2.13 SDMA Checksums

THE SDMA controller uses the CRC-32 IEEE 802.3 Standard polynomial to generate unique checksum calculations for the source address, destination address and read data. The source and destination address checksums are used to verify that the correct address sequence was followed. The read data checksum is calculated as a read move loads data from a data source into the SDMA controller. The checksum is used to verify the integrity of data transfers.

In order to start the generation of a checksum sequence the CRC register(s) must be initialized (e.g. written with 00000000_H or with a desired start value) and a SDMA transaction must be set up (start address, length, etc.).

The address checkums are calculated as the source or destination address changes. The read data checksum is calculated as the value in the Read Value in the Move Engine Read Register is refreshed. The checksum calculation is limited to 32-bit accesses.

13.3 SDMA Module Registers

Figure 13-26 and Table 13-5 show all registers associated with the SDMA Controller Kernel. Additionally, Table 13-5 includes the SDMA module specific registers that are shown in Figure 13-26. All SDMA kernel register names described in this section are also referenced in other parts of the TC1798 User´s Manual by the module name prefix “SDMA_”.

The registers are numbered by one index to indicate the related SDMA Sub-Block and one index to indicate the related SDMA channel: Index “m” refers to the SDMA Sub-Block number (m = 0) and Index “n” or “x” refers to the channel number (n = 0-7 or x = 0-7) within the SDMA Sub-Block.

SDMA Registers Overview

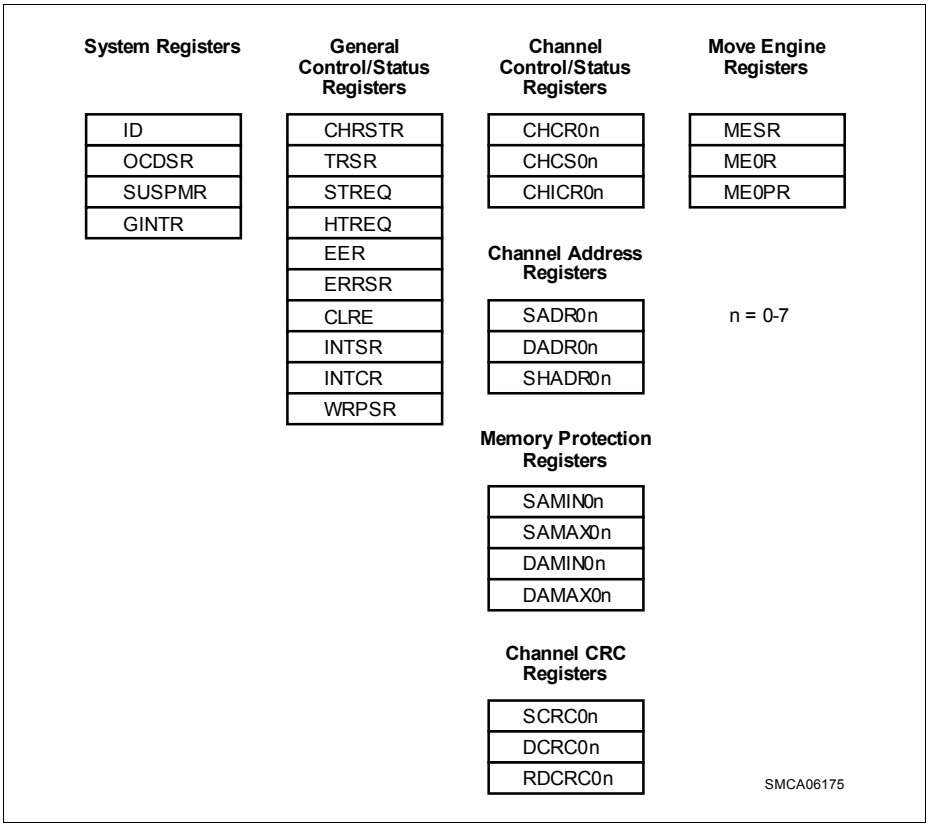


Figure 13-26 SDMA Kernel Registers

Table 13-4 Registers Address Space - SDMA Module

Module	Base Address	End Address	Note
SDMA	$F000\ 3800_H$	$F000\ 3AFF_H$	

Table 13-5 Registers Overview - SDMA Control Registers

Short Name	Description	Offset Addr.[1]	Access Mode		Reset Class	Description See
			Read	Write		
SDMA_CLC	SDMA Clock Control Register	000_H	U, SV	SV, E	3	Page 13-92
-	Reserved	004_H	nBE	SV	-	-
SDMA_ID	SDMA Module Identification Register	008_H	U, SV	BE	-	Page 13-46
-	Reserved	$00C_H$	BE	BE	-	-
SDMA_CHRSTR	SDMA Channel Reset Request Register	010_H	U, SV	SV	3	Page 13-51
SDMA_TRSR	SDMA Transaction Request State Register	014_H	U, SV	BE	3	Page 13-52
SDMA_STREQ	SDMA Software Transaction Request Register	018_H	U, SV	SV	3	Page 13-53
SDMA_HTREQ	SDMA Hardware Transaction Request Register	$01C_H$	U, SV	SV	3	Page 13-54
SDMA_EER	SDMA Enable Error Register	020_H	U, SV	SV	3	Page 13-55
SDMA_ERRSR	SDMA Error Status Register	024_H	U, SV	BE	3	Page 13-57
SDMA_CLRE	SDMA Clear Error Register	028_H	U, SV	SV	3	Page 13-59
SDMA_GINTR	SDMA Global Interrupt Set Register	$02C_H$	U, SV	SV	3	Page 13-50
SDMA_MESR	SDMA Move Engine Status Register	030_H	U, SV	BE	3	Page 13-63
SDMA_ME0R	SDMA Move Engine 0 Read Register	034_H	U, SV	BE	3	Page 13-64

Table 13-5 Registers Overview - SDMA Control Registers (cont'd)

Short Name	Description	Offset Addr.[1)]	Access Mode		Reset Class	Description See
			Read	Write		
-	Reserved	038_H	BE	BE	-	-
SDMA_ME0PR	SDMA Move Engine 0 Pattern Register	$03C_H$	U, SV	SV	3	Page 13-64
-	Reserved	040_H-050_H	BE	BE	-	-
SDMA_INTSR	SDMA Interrupt Status Register	054_H	U, SV	BE	3	Page 13-60
SDMA_INTCR	SDMA Interrupt Clear Register	058_H	U, SV	SV	3	Page 13-62
SDMA_WRPSR	SDMA Wrap Status Register	$05C_H$	U, SV	BE	3	Page 13-61
-	Reserved	060_H	BE	BE	-	-
SDMA_OCDSR	SDMA OCDS Register	064_H	U, SV	SV, E	1	Page 13-47
SDMA_SUSPMR	SDMA Suspend Mode Register	068_H	U, SV	SV, E	1	Page 13-49
-	Reserved	$06C_H$-$07C_H$	BE	BE	-	-
SDMA_CHSR0n	SDMA Channel 0n Status Register (n = 0-7)	(n x 20_H) + 080_H	U, SV	BE	3	Page 13-69
SDMA_CHCR0n	SDMA Channel 0n Control Register (n = 0-7)	(n x 20_H) + 084_H	U, SV	SV	3	Page 13-65
SDMA_CHICR0n	SDMA Channel 0n Interrupt Control Register (n = 0-7)	(n x 20_H) + 088_H	U, SV	SV	3	Page 13-70
SDMA_ADRCR0n	SDMA Channel 0n Address Control Register (n = 0-7)	(n x 20_H) + $08C_H$	U, SV	SV	3	Page 13-72

Table 13-5 Registers Overview - SDMA Control Registers (cont'd)

Short Name	Description	Offset Addr.[1]	Access Mode		Reset Class	Description See
			Read	Write		
SDMA_SADR0n	SDMA Channel 0n Source Address Register (n = 0-7)	(n x 20_H) + 090_H	U, SV	SV	3	Page 13-77
SDMA_DADR0n	SDMA Channel 0n Destination Address Register (n = 0-7)	(n x 20_H) + 094_H	U, SV	SV	3	Page 13-78
SDMA_SHADR0n	SDMA Channel 0n Shadow Address Register (n = 0-7)	(n x 20_H) + 098_H	U, SV	BE / SV [2]	3	Page 13-79
-	Reserved (n = 0-7)	(n x 20_H) + $09C_H$	BE	BE	-	-
SDMA_SAMIN0n	SDMA Channel 0n Source Address Lower Boundary Register (n = 0-7)	(n x 20_H) + 180_H	U, SV, 32	SV, 32	3	Page 13-80
SDMA_SAMAX0n	SDMA Channel 0n Source Address Upper Boundary Register (n = 0-7)	(n x 20_H) + 184_H	U, SV, 32	SV, 32	3	Page 13-80
SDMA_DAMIN0n	SDMA Channel 0n Destination Address Lower Boundary Register (n = 0-7)	(n x 20_H) + 188_H	U, SV, 32	SV, 32	3	Page 13-81
SDMA_DAMAX0n	SDMA Channel 0n Destination Address Upper Boundary Register (n = 0-7)	(n x 20_H) + $18C_H$	U, SV, 32	SV, 32	3	Page 13-81
SDMA_SRCC0n	SDMA Channel 0n Source Address CRC Checksum Register	(n x 20_H) + 190_H	U, SV, 32	SV, 32	3	Page 13-82

Table 13-5 Registers Overview - SDMA Control Registers (cont'd)

Short Name	Description	Offset Addr.[1)]	Access Mode		Reset Class	Description See
			Read	Write		
SDMA_DCRC0n	SDMA Channel 0n Destination Address CRC Checksum Register	(n x 20_H) + 194_H	U, SV, 32	SV, 32	3	Page 13-82
SDMA_RDCRC0n	SDMA Channel 0n Read Data CRC Checksum Register	(n x 20_H) + 198_H	U, SV, 32	SV, 32	3	Page 13-83
-	Reserved (n = 0-7)	(n x 20_H) + $19C_H$	BE	BE	-	
-	Reserved	280_H-$2DC_H$	BE	BE	-	-
SDMA_SRC7	SDMA Service Request Control Register 7	$2E0_H$	U, SV	SV	3	Page 13-94
SDMA_SRC6	SDMA Service Request Control Register 6	$2E4_H$	U, SV	SV	3	Page 13-94
SDMA_SRC5	SDMA Service Request Control Register 5	$2E8_H$	U, SV	SV	3	Page 13-94
SDMA_SRC4	SDMA Service Request Control Register 4	$2EC_H$	U, SV	SV	3	Page 13-94
SDMA_SRC3	SDMA Service Request Control Register 3	$2F0_H$	U, SV	SV	3	Page 13-94
SDMA_SRC2	SDMA Service Request Control Register 2	$2F4_H$	U, SV	SV	3	Page 13-94

Table 13-5 Registers Overview - SDMA Control Registers (cont'd)

Short Name	Description	Offset Addr.[1]	Access Mode		Reset Class	Description See
			Read	Write		
SDMA_ SRC1	SDMA Service Request Control Register 1	$2F8_H$	U, SV	SV	3	Page 13-94
SDMA_ SRC0	SDMA Service Request Control Register 0	$2FC_H$	U, SV	SV	3	Page 13-94

1) The absolute register address is calculated as follows:
Module Base Address (Table 13-4) + Offset Address (shown in this column)
Further, the following ranges for parameters i, k, x, and n are valid: i = 0-7, k = 0-7, x = 0-1, n = 0-63.

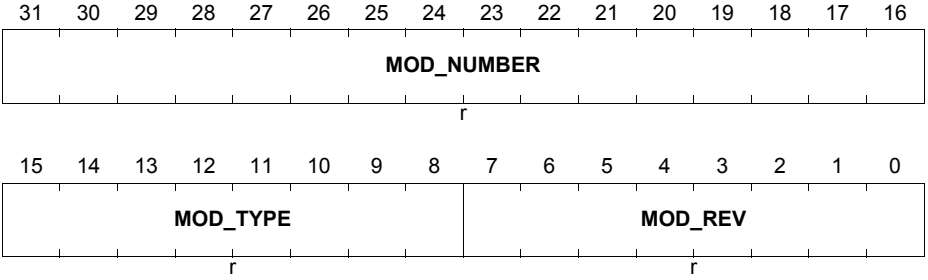
2) Write access mode to SDMA_SHADR0n is controlled by the register bit SDMA_ADRCR0n.SHWEN. SDMA_ADRCR0n.SHWEN=´0´ -> Access Mode Write for SDMA_SHADR0n is BE. SDMA_ADRCR0n.SHWEN=´1´ -> Access Mode Write for SDMA_SHADR0n is SV.

Note: Register bits marked "w" in the following register description are virtual registers and do not contain flip-flops. They are always read as 0.

13.3.1 System Registers

SDMA Module Identification Register.

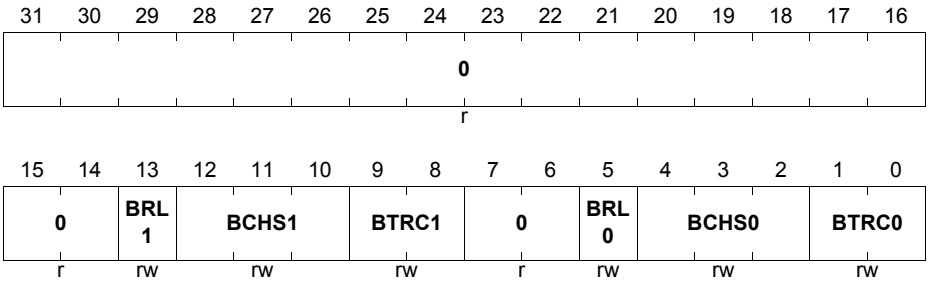
SDMA_ID
Module Identification Register **(008_H)** **Reset Value: 0087 C0XX$_H$**



Field	Bits	Type	Description
MOD_REV	[7:0]	r	**Module Revision Number** This bit field defines the module revision number. The value of a module revision starts with 01_H (first revision).
MOD_TYPE	[15:8]	r	**Module Type** The bit field is set to $C0_H$ which defines the module as a 32-bit module.
MOD_NUMBER	[31:16]	r	**Module Number Value** This bit field defines a module identification number. The value for the SDMA module is 0087_H.

The OCDS Register describes the break capability of the SDMA module. OCDSR is only reset with the OCDS Reset.

SDMA_OCDSR
SDMA OCDS Register **(064_H)** **Reset Value: 0000 0000$_H$**



Field	Bits	Type	Description
BTRC0	[1:0]	rw	**Break Trigger Condition In Sub-Block 0** This bit field determines the transition type for the transaction request bit TRSR.CH0n that leads to a break condition in SDMA Sub-Block 0. 00_B No break condition is generated 01_B A break condition is generated when TRSR.CH0n changes from 0 to 1 10_B A break condition is generated when TRSR.CH0n changes from 1 to 0 11_B A break condition is generated when TRSR.CH0n changes its state
BCHS0	[4:2]	rw	**Break Channel Select In Sub-Block 0** This bit field determines the SDMA channel n of SDMA Sub-Block 0 whose transaction request bit TRSR.CH0n is observed for signal transitions as defined by BTRC0. 000_B SDMA channel 00 selected 001_B SDMA channel 01 selected …$_B$ … 110_B SDMA channel 06 selected 111_B SDMA channel 07 selected

Field	Bits	Type	Description
BRL0	5	rw	**Break On Request Lost in Sub-Block 0** This bit field determines whether a BREAK signal is generated for SDMA Sub-Block 0 when at least one of its eight transaction lost interrupts becomes active. 0_B No break condition is generated 1_B A break condition is generated for SDMA Sub-Block 0 when at least one of its eight transaction lost interrupts becomes active
BTRC1	[9:8]	rw	**Break Trigger Condition In Sub-Block 1** This bit field determines the transition type for the transaction request bit TRSR.CH1n that leads to a break condition in SDMA Sub-Block 1. 00_B No break condition is generated 01_B A break condition is generated when TRSR.CH1n changes from 0 to 1 10_B A break condition is generated when TRSR.CH1n changes from 1 to 0 11_B A break condition is generated when TRSR.CH1n changes its state
BCHS1	[12:10]	rw	**Break Channel Select In Sub-Block 1** This bit field determines the SDMA channel n of SDMA Sub-Block 1 whose transaction request bit TRSR.CH1n is observed for signal transitions as defined by BTRC1. 000_B SDMA channel 10 selected 001_B SDMA channel 11 selected ...$_B$ ... 110_B SDMA channel 16 selected 111_B SDMA channel 17 selected
BRL1	13	rw	**Break On Request Lost in Sub-Block 1** This bit field determines whether a BREAK signal is generated for SDMA Sub-Block 1 when at least one of its eight transaction lost interrupts becomes active. 0_B No break condition is generated 1_B A break condition is generated for SDMA Sub-Block 1when at least one of its eight transaction lost interrupts becomes active
0	[7:6], [31:14]	r	**Reserved** Read as 0; should be written with 0.

The Suspend Mode Register contains bits for each SDMA channel that allow the enabling/disabling of its soft suspend mode capability and to indicate its suspend status.

SDMA_SUSPMR
SDMA Suspend Mode Register **(068_H)** **Reset Value: $0000\ 0000_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0								SUSAC07	SUSAC06	SUSAC05	SUSAC04	SUSAC03	SUSAC02	SUSAC01	SUSAC00
r								rh	rh	rh	rh	rh	rh	rh	rh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0								SUSEN07	SUSEN06	SUSEN05	SUSEN04	SUSEN03	SUSEN02	SUSEN01	SUSEN00
rw								rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
SUSEN0n (n = 0-7)	n	rw	**Suspend Enable for SDMA Channel 0n** This bit enables the soft suspend capability individually for each SDMA channel 0n. 0_B SDMA channel 0n is disabled for Soft-suspend Mode. The SDMA channel 0n does not react on an active suspend request signal SUSREQ 1_B SDMA channel 0n is enabled for Soft-suspend Mode. If the suspend request signal SUSREQ becomes active, a SDMA transaction of SDMA channel 0n is stopped after the current SDMA transfer has been finished Soft-suspend Mode can be terminated when SUSEN0n is written with 0.
SUSAC0n (n = 0-7)	n + 16	rh	**Suspend Active for SDMA Channel 0n** This status bit indicates whether or not SDMA channel 0n is in Soft-suspend Mode. 0_B SDMA channel 0n is not in Soft-suspend Mode or internal actions are not yet finished after the Soft-suspend Mode was requested 1_B SDMA channel 0n is in Soft-suspend Mode
0	[15:8]	rw	**Reserved** Read as 0; must be written with 0.

Field	Bits	Type	Description
0	[31:24]	r	**Reserved** Read as 0; should be written with 0.

Note: Register SUSPMR is only reset by the OCDS reset.

The Global Interrupt Set Register allows the interrupt output lines of the SDMA to be activated by software.

SDMA_GINTR

SDMA Global Interrupt Set Register (02C$_H$) **Reset Value: 0000 0000$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SIDMA15	**SIDMA14**	**SIDMA13**	**SIDMA12**	**SIDMA11**	**SIDMA10**	**SIDMA9**	**SIDMA8**	**SIDMA7**	**SIDMA6**	**SIDMA5**	**SIDMA4**	**SIDMA3**	**SIDMA2**	**SIDMA1**	**SIDMA0**
w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w

Field	Bits	Type	Description
SIDMAx (x = 0-15)	x	w	**Set SDMA Interrupt Output Line x** 0_B No action 1_B DMA interrupt output line SRx will be activated. Reading this bit returns a 0
0	[31:16]	r	**Reserved** Read as 0; should be written with 0.

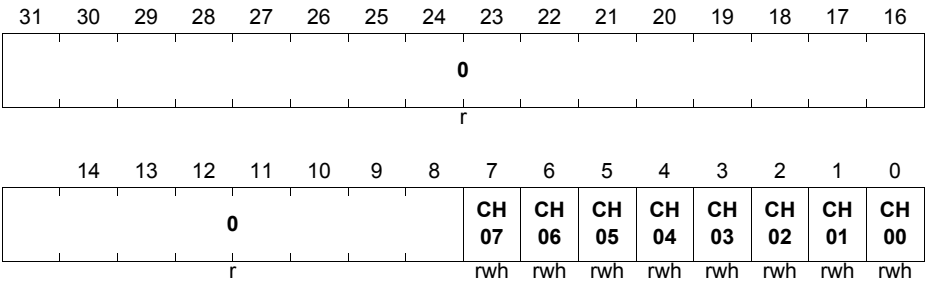
Note: In the TC1798, SR[7:0] are connected to interrupt nodes. SR[15:8] are used as SDMA channel request inputs.

13.3.2 General Control/Status Registers

The bits in the Channel Reset Request Register are used to reset SDMA channel mn.

SDMA_CHRSTR
SDMA Channel Reset Request Register

(010_H) **Reset Value: $0000\ 0000_H$**



Field	Bits	Type	Description
CH0n (n = 0-7)	n	rwh	**Channel 0n Reset** These bits force the SDMA channel 0n to stop its current SDMA transaction. Once set by software, this bit will be automatically cleared when the channel has been reset. Writing a 0 to CH0n has no effect. 0_B No action (write) or the requested channel reset has been reset (read). 1_B SDMA channel 0n is stopped. More details see Page 13-16.
0	[31:8]	r	**Reserved** Read as 0; should be written with 0.

The bits in the Transaction Request State Register indicates which SDMA channel is processing a request, and which SDMA channel has hardware transaction requests enabled.

SDMA_TRSR
SDMA Transaction Request State Register
(014_H) **Reset Value: $0000\ 0000_H$**

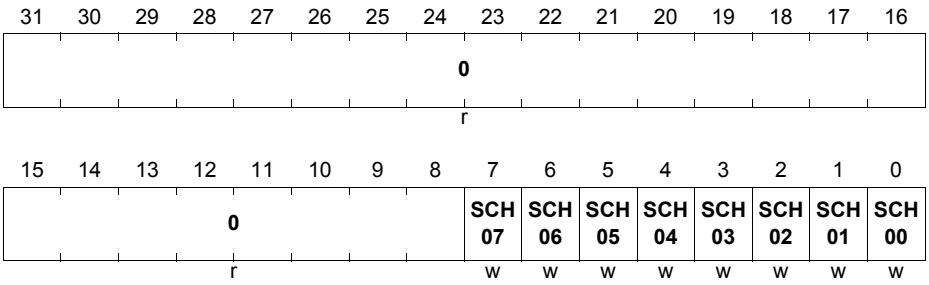
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0								HTRE07	HTRE06	HTRE05	HTRE04	HTRE03	HTRE02	HTRE01	HTRE00
r								rh	rh	rh	rh	rh	rh	rh	rh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0								CH07	CH06	CH05	CH04	CH03	CH02	CH01	CH00
r								rh	rh	rh	rh	rh	rh	rh	rh

Field	Bits	Type	Description
CH0n (n = 0-7)	n	rh	**Transaction Request State of SDMA Channel 0n** 0_B No SDMA request is pending for channel 0n. 1_B A SDMA request is pending for channel 0n. CH0n is reset when a pattern match is detected.
HTRE0n (n = 0-7)	n+16	rh	**Hardware Transaction Request Enable State of SDMA Channel 0n** 0_B Hardware transaction request for SDMA Channel 0n is disabled. An input SDMA request will not trigger the channel 0n. 1_B Hardware transaction request for SDMA Channel 0n is enabled. The transfers of a SDMA transaction are controlled by the corresponding channel request line of the SDMA requesting source. HTRE0n is set to 0 when CHSR0n.TCOUNT is decremented and CHSR0n.TCOUNT = 0. HTRE0n can be enabled and disabled with HTREQ.ECH0n or HTREQ.DCH0n. HTRE0n is reset when a pattern match is detected.
0	[31:24], [15:8]	r	**Reserved** Read as 0; should be written with 0.

The bits in the Software Transaction Request Register are used to generate a SDMA transaction request by software.

SDMA_STREQ
SDMA Software Transaction Request Register
(018_H) **Reset Value: $0000\ 0000_H$**



Field	Bits	Type	Description
SCH0n (n = 0-7)	n	w	**Set Transaction Request for SDMA Channel 0n** 0_B No action. 1_B A transaction for SDMA channel 0n is requested. When setting SCH0n, TRSR.CH0n becomes set to indicate that a SDMA request is pending for SDMA channel 0n.
0	[31:8]	r	**Reserved** Read as 0; should be written with 0.

Note: Register bits marked with "w" are virtual and are not stored in flip-flops. Reading STREQ returns 0 when read.

The bits in the Hardware Transaction Request Register enable or disable SDMA hardware requests.

SDMA_HTREQ
SDMA Hardware Transaction Request Register
($01C_H$) **Reset Value: $0000\ 0000_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0								DCH 07	DCH 06	DCH 05	DCH 04	DCH 03	DCH 02	DCH 01	DCH 00
r								w	w	w	w	w	w	w	w

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0								ECH 07	ECH 06	ECH 05	ECH 04	ECH 03	ECH 02	ECH 01	ECH 00
r								w	w	w	w	w	w	w	w

Field	Bits	Type	Description
ECH0n (n = 0-7)	n	w	**Enable Hardware Transfer Request for SDMA Channel 0n** see table below
DCH0n (n = 0-7)	16+n	w	**Disable Hardware Transfer Request for SDMA Channel 0n** see table below
0	[31:24], [15:8]	r	**Reserved** Read as 0; should be written with 0.

Table 13-6 Conditions to Set/Reset the Bits TRSR.HTREmn

HTREQ.ECHmn	HTREQ.DCHmn	Transaction Finishes[1] for Channel mn	Modification of TRSR.HTREmn
0	0	0	Unchanged
1	0	0	Set
X	1	X	Reset
X	X	1	Reset

1) In Single Mode only. In Continuous Mode, the end of a transaction has no impact.

The Enable Error Register describes how the SDMA controller reacts to errors. It enables the interrupts for the loss of a transaction request or Move Engine errors.

SDMA_EER
SDMA Enable Error Register (020_H) Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TRLINP				0				ME0INP				0		EME0DER	EME0SER
rw				r				rw				r		rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0								ETRL07	ETRL06	ETRL05	ETRL04	ETRL03	ETRL02	ETRL01	ETRL00
r								rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
ETRL0n (n = 0-7)	n	rw	**Enable Transaction Request Lost for SDMA Channel 0n** This bit enables the generation of an interrupt when the set condition for ERRSR.TRL0n is detected. 0_B The interrupt generation for a request lost event for channel 0n is disabled. 1_B The interrupt generation for a request lost event for channel 0n is enabled.
EME0SER	16	rw	**Enable Move Engine 0 Source Error** This bit enables the generation of a Move Engine 0 source error interrupt. 0_B Move Engine 0 source error interrupt is disabled. 1_B Move Engine 0 source error interrupt is enabled.
EME0DER	17	rw	**Enable Move Engine 0 Destination Error** This bit enables the generation of a Move Engine 0 destination error interrupt. 0_B Move Engine 0 destination error interrupt is disabled. 1_B Move Engine 0 destination error interrupt is enabled.

Field	Bits	Type	Description
ME0INP	[23:20]	rw	**Move Engine 0 Error Interrupt Node Pointer** ME0INP determines the number n (n = 0-15) of the service request output SRn that becomes active on a Move Engine 0 source or destination interrupt. 0000_B SR0 selected for Move Engine 0 interrupt 0001_B SR1 selected for Move Engine 0 interrupt $\ldots_B$ … 1111_B SR15 selected for Move Engine 0 interrupt *Note: In the TC1798, SR[7:0] are connected to interrupt nodes. SR[15:8] are used as SDMA channel request inputs.*
TRLINP	[31:28]	rw	**Transaction Lost Interrupt Node Pointer** TRLINP determines the number n (n = 0-15) of the service request output SRn that becomes active on a transaction lost interrupt. 0000_B SR0 selected for transaction lost interrupt 0001_B SR1 selected for transaction lost interrupt $\ldots_B$ … 1111_B SR15 selected for transaction lost interrupt *Note: In the TC1798, SR[7:0] are connected to interrupt nodes. SR[15:8] are used as SDMA channel request inputs.*
0	[15:8], [19:18], [27:24]	r	**Reserved** Read as 0; should be written with 0.

The Error Status Register indicates if the SDMA controller could not answer to a request because the previous request was not terminated (see **Section 13.2.4.4**). It indicates also the FPI Bus accesses that have been terminated with errors.

SDMA_ERRSR
SDMA Error Status Register **(024_H)** **Reset Value: 0000 0000$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0						LEC ME0		0			FPIER	0	0	ME0DER	ME0SER
r						rh		r			rh	r	r	rh	rh

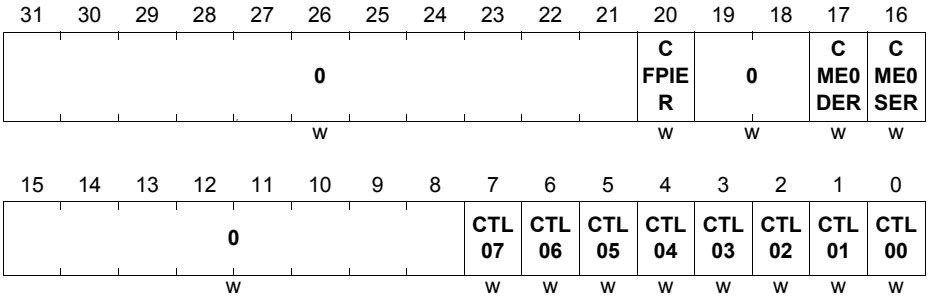
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0								TRL07	TRL06	TRL05	TRL04	TRL03	TRL02	TRL01	TRL00
r								rh	rh	rh	rh	rh	rh	rh	rh

Field	Bits	Type	Description
TRL0n (n = 0-7)	n	rh	**Transaction/Transfer Request Lost of SDMA Channel 0n** 0_B 0 No request lost event has been detected for channel 0n. 1_B 1 A new SDMA request was detected while TRSR.CH0n=1 (request lost event). This bit is reset by software when writing a 1 to CLRE.CTL0n, or by a channel reset (writing CHRSTR.CH0n = 1).
ME0SER	16	rh	**Move Engine 0 Source Error** This bit is set whenever a Move Engine 0 error occurred during a source (read) move of a SDMA transfer, or a request could not been serviced due to the access protection. 0_B No Move Engine 0 source error has occurred. 1_B A Move Engine 0 source error has occurred.

Field	Bits	Type	Description
ME0DER	17	rh	**Move Engine 0 Destination Error** This bit is set whenever a Move Engine 0 error occurred during a destination (write) move of a SDMA transfer, or a request could not been serviced due to the access protection. 0_B No Move Engine 0 destination error has occurred. 1_B A Move Engine 0 destination error has occurred.
FPIER	20	rh	**SPB Error** This bit is set whenever a move that has been started by the SDMA FPI master interface leads to an error on the FPI Bus. 0_B No error occurred. 1_B An error occurred on FPI Bus interface.
LECME0	[26:24]	rh	**Last Error Channel Move Engine 0** This bit field indicates the channel number of the last channel of Move Engine 0 leading to an On Chip Bus error that has occurred.
0	[15:8], [19:18], [23:21], [31:27]	r	**Reserved** Read as 0; should be written with 0.

The Clear Error contains bits that make it possible to clear the Transaction Request Lost flags or the Move Engine error flags.

SDMA_CLRE
SDMA Clear Error Register **(028_H)** **Reset Value: 0000 0000$_H$**



Field	Bits	Type	Description
CTL0n (n = 0-7)	n	w	**Clear Transaction Request Lost for SDMA Channel 0n** 0_B No action 1_B Clear SDMA channel 0n transaction request lost flag ERRSR.TRL0n
CME0SER	16	w	**Clear Move Engine 0 Source Error** 0_B No action 1_B Clear source error flag ERRSR.ME0SER.
CME0DER	17	w	**Clear Move Engine 0 Destination Error** 0_B No action 1_B Clear destination error flag ERRSR.ME0DER.
CFPIER	20	w	**Clear FPI Error** 0_B No action 1_B Clear error flag ERRSR.FPIER.
0	[15:8], [19:18], [31:21]	r	**Reserved** Should be written with 0.

The Interrupt Status Register indicates if CHSR0n.TCOUNT matches with CHCR0n.IRDV, or if CHSR0n.TCOUNT has been decremented (depending on CHICR0n.INTCT[0]), or if a pattern has been detected. These conditions can also generate an interrupt if enabled (see **Figure 13-17** on **Page 13-27**).

SDMA_INTSR
SDMA Interrupt Status Register (054_H) Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0								IPM 07	IPM 06	IPM 05	IPM 04	IPM 03	IPM 02	IPM 01	IPM 00
r								rh	rh	rh	rh	rh	rh	rh	rh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0								ICH 07	ICH 06	ICH 05	ICH 04	ICH 03	ICH 02	ICH 01	ICH 00
r								rh	rh	rh	rh	rh	rh	rh	rh

Field	Bits	Type	Description
ICH0n (n = 0-7)	n	rh	**Interrupt from Channel 0n** This bit indicates that channel 0n has raised an interrupt for TCOUNT = IRDV or if TCOUNT has been decremented (depending on CHICR.INTCT[0]. This bit (and IP0n) is reset by software when writing a 1 to INTCR.CICH0n or by a channel reset (writing CHRSTR.CH0n = 1). 0_B A channel interrupt has not been detected. 1_B A channel interrupt has been detected.
IPM0n (n = 0-7)	n + 16	rh	**Pattern Detection from Channel 0n** This bit indicates that a pattern has been detected for channel 0n while the pattern detection has been enabled. This bit (and ICH0n) is reset by software when writing a 1 to INTCR.CICH0n or by a channel reset (writing CHRSTR.CH0n = 1). 0_B A pattern has not been detected. 1_B A pattern has been detected.
0	[15:8], [31:24]	r	**Reserved** Read as 0; should be written with 0.

The Wrap Status Register provides information on the channels that perform a wraparound on their source or destination buffer(s). This condition can also lead to an interrupt if it is enabled.

SDMA_WRPSR
SDMA Wrap Status Register (05C$_H$) Reset Value: 0000 0000$_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0								WRPD07	WRPD06	WRPD05	WRPD04	WRPD03	WRPD02	WRPD01	WRPD00
r								rh	rh	rh	rh	rh	rh	rh	rh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0								WRPS07	WRPS06	WRPS05	WRPS04	WRPS03	WRPS02	WRPS01	WRPS00
r								rh	rh	rh	rh	rh	rh	rh	rh

Field	Bits	Type	Description
WRPS0n (n = 0-7)	n	rh	**Wrap Source Buffer for Channel 0n** These bits indicate which channels have done a wrap-around of their source buffer(s). 0_B No wrap-around occurred for channel 0n. 1_B A wrap-around occurred for channel 0n. Note: This bit is reset by software by writing a 1 to INTCR.CWRP0n or CHRSTR.CH0n.
WRPD0n (n = 0-7)	n+16	rh	**Wrap Destination Buffer for Channel 0n** These bits indicate which channels have done a wrap-around of their destination buffer(s). 0_B No wrap-around occurred for channel 0n. 1_B A wrap-around occurred for channel 0n. Note: This bit is reset by software by writing a 1 to INTCR.CWRP0n or CHRSTR.CH0n.
0	[15:8], [31:24]	r	**Reserved** Read as 0; should be written with 0.

The bits in the Interrupt Clear Register allow the channel interrupt flags and the wrap buffer interrupt flags for SDMA Channels 0n to be reset.

SDMA_INTCR
SDMA Interrupt Clear Register (058$_H$) Reset Value: 0000 0000$_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0								CWRP07	CWRP06	CWRP05	CWRP04	CWRP03	CWRP02	CWRP01	CWRP00
r								w	w	w	w	w	w	w	w

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0								CICH07	CICH06	CICH05	CICH04	CICH03	CICH02	CICH01	CICH00
r								w	w	w	w	w	w	w	w

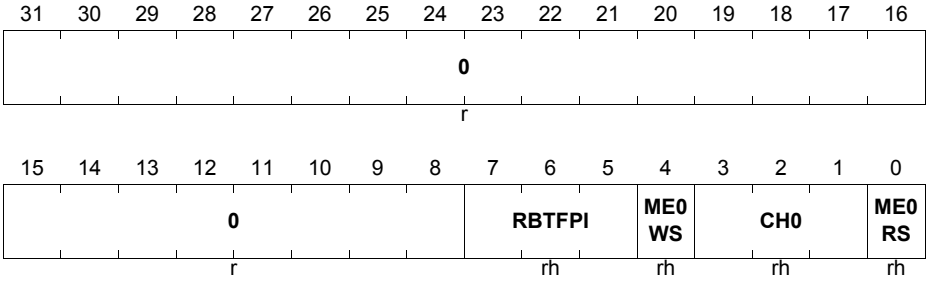
Field	Bits	Type	Description
CICH0n (n = 0-7)	n	w	**Clear Interrupt for SDMA Channel 0n** These bits allow the channel interrupt flags INTSR.ICH0n and INTSR.IPM0n of SDMA channel 0n to be reset by software. 0_B No action. 1_B Bits INTSR.ICH0n and INTSR.IPM0n are reset.
CWRP0n (n = 0-7)	n + 16	w	**Clear Wrap Buffer Interrupt for SDMA Channel 0n** These bits allow the wrap source buffer interrupt flag WRPSR.WRPS0n and the wrap destination buffer interrupt flag WRPSR.WRPD0n (both together) of SDMA channel 0n to be reset by software. 0_B No action. 1_B Bits WRPSR.WRPS0n and WRPSR.WRPD0n are reset.
0	[15:8], [31:24]	r	**Reserved** Read as 0; should be written with 0.

13.3.3 Move Engine Registers

The Move Engine Status Register is a read-only register that holds status information about the transaction handled by the Move Engines.

SDMA_MESR

SDMA Move Engine Status Register (030$_H$) **Reset Value: 0000 0000$_H$**

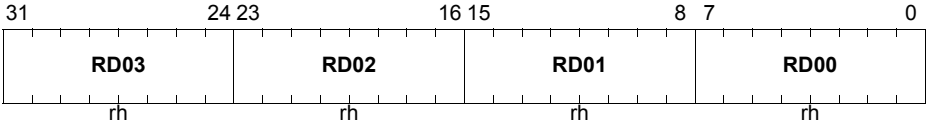


Field	Bits	Type	Description
ME0RS	0	rh	**Move Engine 0 Read Status** 0_B Move Engine 0 is not performing a read. 1_B Move Engine 0 is performing a read.
CH0	[3:1]	rh	**Reading Channel in Move Engine 0** This bit field indicates which channel number is currently being processed by the Move Engine 0.
ME0WS	4	rh	**Move Engine 0 Write Status** 0_B Move Engine 0 is not performing a write. 1_B Move Engine 0 is performing a write.
RBTFPI	[7:5]	rh	**Read Buffer Trace for FPI Bus Interface** This bit field contains trace information from the buffer in the FPI Bus Interface. In the TC1798 it indicates the source of a bus access to the FPI Bus. 000_B SDMA Move Engine 0 Other bit combinations are reserved. RBTFPI is useful for emulation purposes. It is not recommended to evaluate this bit field during normal operation of the TC1798.
0	[31:8]	r	**Reserved** Read as 0; should be written with 0.

The Move Engine 0 Read Register indicates the value that has just been read by Move Engine 0. The value in this register is compared to the bits in register ME0PR according to the bit fields CHCR0n.PATSEL.

SDMA_ME0R

SDMA Move Engine 0 Read Register (034_H) **Reset Value: $0000\ 0000_H$**

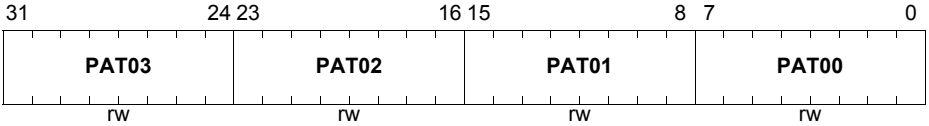


Field	Bits	Type	Description
RD00, RD01, RD02, RD03	[7:0], [15:8], [23:16], [31:24]	rh	**Read Value for Move Engine 0** Contains the 32-bit read data (four bytes RD0[3:0]) that is stored in the Move Engine after each read move. The content of ME0R is overwritten after each read move of a SDMA channel belonging to SDMA Sub-block.

The Move Engine 0 Pattern Register contains the patterns (mask and/or compare bits) to be processed by the pattern detection logic in Move Engine 0.

SDMA_ME0PR

SDMA Move Engine 0 Pattern Register($03C_H$) **Reset Value: $0000\ 0000_H$**



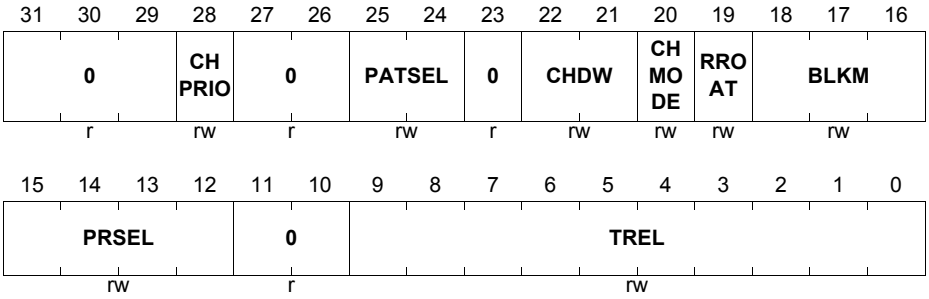
Field	Bits	Type	Description
PAT00, PAT01, PAT02, PAT03	[7:0], [15:8], [23:16], [31:24]	rw	**Pattern for Move Engine 0** Determines up to four 8-bit compare patterns/mask patterns to be processed by the pattern detection logic in Move Engine 0. Depending on the pattern detection configuration (CHCR0n.PATSEL) and channel data width (CHCR0n.CHDW), the patterns are processed as bytes or half-words.

13.3.4 Channel Control/Status Registers

The Channel Control Register for SDMA channel 0n contains its configuration and its control bits and bit fields.

SDMA_CHCR0x (x = 0-7)

SDMA Channel 0x Control Register(084_H+x*20_H) **Reset Value: 0000 0000_H**



Field	Bits	Type	Description
TREL	[9:0]	rw	**Transfer Reload Value** This bit field contains the number of SDMA transfers for a SDMA transaction of SDMA channel 0n. This10-bit transfer count value is loaded into CHSR0n.TCOUNT at the start of a SDMA transaction (when TRSR.CH0n becomes set and CHSR0n.TCOUNT = 0). A write to CHSR0n.TREL during a running SDMA transaction has no influence to the running SDMA transaction. If CHSR0n.TREL = 0 or if CHSR0n.TREL = 1, CHSR0n.TCOUNT will be loaded with 1 when a new transaction is started (at least one SDMA transfer must be executed per SDMA transaction).

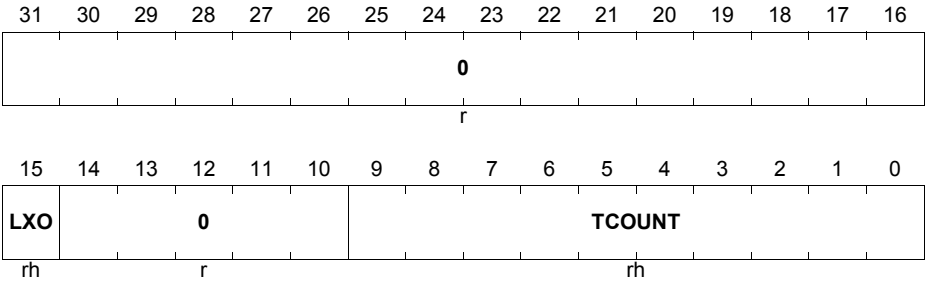
Field	Bits	Type	Description
PRSEL	[15:12]	rw	**Peripheral Request Select** This bit field controls the hardware request input multiplexer of SDMA channel 0n (see **Figure 13-6** on **Page 13-10**). 0000_B Input CH0n_REQI0 selected 0001_B Input CH0n_REQI1 selected 0010_B Input CH0n_REQI2 selected 0011_B Input CH0n_REQI3 selected 0100_B Input CH0n_REQI4 selected 0101_B Input CH0n_REQI5 selected 0110_B Input CH0n_REQI6 selected 0111_B Input CH0n_REQI7 selected 1000_B Input CH0n_REQI8 selected 1001_B Input CH0n_REQI9 selected 1010_B Input CH0n_REQI10 selected 1011_B Input CH0n_REQI11 selected 1100_B Input CH0n_REQI12 selected 1101_B Input CH0n_REQI13 selected 1110_B Input CH0n_REQI14 selected 1111_B Input CH0n_REQI15 selected
BLKM	[18:16]	rw	**Block Mode** BLKM determines the number of SDMA moves executed during one SDMA transfer. 000_B One SDMA transfer has 1 SDMA move 001_B One SDMA transfer has 2 SDMA move 010_B One SDMA transfer has 4 SDMA move 011_B One SDMA transfer has 8 SDMA move 100_B One SDMA transfer has 16 SDMA move Other bit combinations are reserved and must not be used. See also **Figure 13-10** on **Page 13-17**.
RROAT	19	rw	**Reset Request Only After Transaction** RROAT determines whether or not the TRSR.CH0n transfer request state flag is reset after each transfer. 0_B TRSR.CH0n is reset after each transfer. A transfer request is required for each transfer. 1_B TRSR.CH0n is reset when CHSR0n.TCOUNT = 0 after a transfer. One transfer request starts a complete SDMA transaction

Field	Bits	Type	Description
CHMODE	20	rw	**Channel Operation Mode** CHMODE determines the reset condition for control bit TRSR.HTRE0n of SDMA channel 0n. 0_B Single Mode operation is selected for SDMA channel 0n. After a transaction, SDMA channel 0n is disabled for further hardware requests (TRSR.HTRE0n is reset by hardware) TRSR.HTRE0n must be set again by software for starting a new transaction. 1_B Continuous Mode operation is selected for SDMA channel 0n. After a transaction, bit TRSR.HTRE0n remains set
CHDW	[22:21]	rw	**Channel Data Width** CHDW determines the data width for the read and write moves of SDMA channel 0n. 00_B 8-bit (byte) data width for moves selected 01_B 16-bit (half-word) data width for moves selected 10_B 32-bit (word) data width for moves selected 11_B Reserved
PATSEL	[25:24]	rw	**Pattern Select** This bit field selects the mode of the pattern detection logic. Depending on the channel data width, PATSEL selects different pattern detection configurations. If pattern detection is enabled (PATSEL not equal 00_B), the pattern detection interrupt line will be activated on the selected pattern match. **8-bit channel data width (CHDW = 00_B):** Selected pattern detection configuration see **Table 13-1** on **Page 13-35**. **16-bit channel data width (CHDW = 01_B):** Selected pattern detection configuration see **Table 13-2** on **Page 13-36**. **32-bit channel data width (CHDW = 10_B):** Selected pattern detection configuration see **Table 13-3** on **Page 13-38**.

Field	Bits	Type	Description
CHPRIO	28	rw	**Channel Priority** CHPRIO determines the priority of SDMA channel n for the Move Engine 0 internal channel arbitration. This priority is used for the case when multiple channels of Move Engine 0 are triggered in parallel. 0_B SDMA channel 0n has a low channel priority 1_B SDMA channel 0n has a high channel priority
0	[11:10], 23, [27:26], [31:29]	r	**Reserved** Read as 0; should be written with 0.

The Channel Status Register contains the current transfer count and a pattern detection compare result.

SDMA_CHSR0x (x = 0-7)
SDMA Channel 0x Status Register (080_H+x*20_H) **Reset Value: 0000 0000_H**



Field	Bits	Type	Description
TCOUNT	[9:0]	rh	**Transfer Count Status** TCOUNT holds the actual value of the SDMA transfer count for SDMA channel 0x. TCOUNT is loaded with the value of CHCR0x.TREL when TRSR.CH0x becomes set (and TCOUNT = 0). After each SDMA transfer, TCOUNT is decremented by 1.
LXO	15	rh	**Old Value of Pattern Detection** This bit contains the compare result of a pattern compare operation when 8-bit or 16-bit data width is selected. 8-bit data width: see **Table 13-1** and **Figure 13-23** 16-bit data width: see **Table 13-2** and **Figure 13-24** 0_B The corresponding pattern compare operation did not find a pattern match on the last move 1_B The corresponding pattern compare operation found a pattern match at the last move
0	[14:10], [31:16]	r	**Reserved** Read as 0; should be written with 0.

The Channel Interrupt Control Register controls the interrupts generation.

SDMA_CHICR0x (x = 0-7)
SDMA Channel 0x Interrupt Control Register
(088_H+x*20_H) **Reset Value: 0000 0000_H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IRDV				INTP				WRPP				INTCT		WRPDE	WRPSE
rw				rw				rw				rw		rw	rw

Field	Bits	Type	Description
WRPSE	0	rw	**Wrap Source Enable** 0_B Wrap source buffer interrupt disabled 1_B Wrap source buffer interrupt enabled
WRPDE	1	rw	**Wrap Destination Enable** 0_B Wrap destination buffer interrupt disabled 1_B Wrap destination buffer interrupt enabled
INTCT	[3:2]	rw	**Interrupt Control** 00_B No interrupt will be generated on changing the TCOUNT value. The bit INTSR.ICH0x is set when TCOUNT equals IRDV. 01_B No interrupt will be generated on changing the TCOUNT value. The bit INTSR.ICH0x is set when TCOUNT is decremented 10_B An interrupt is generated and bit INTSR.ICH0x is set each time TCOUNT equals IRDV 11_B Interrupt is generated and bit INTSR.ICH0x is set each time TCOUNT is decremented *Note: see **Figure 13-17**.*

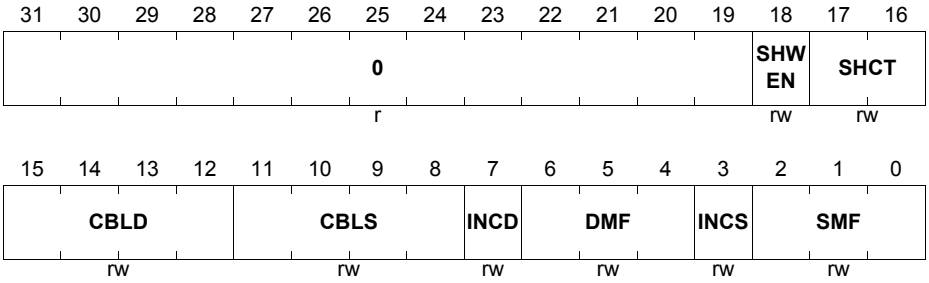
Field	Bits	Type	Description
WRPP	[7:4]	rw	**Wrap Pointer** WRPP determines the number n (n = 0-15) of the service request output SRn that becomes active on a wrap buffer interrupt. 0000_B SR0 selected for channel 0x wrap buffer interrupt 0001_B SR1 selected for channel 0x wrap buffer interrupt …$_B$ … 1111_B SR15 selected for channel 0x wrap buffer interrupt *Note: In the TC1798, SR[7:0] are connected to interrupt nodes. SR[15:8] are used as SDMA channel request inputs.*
INTP	[11:8]	rw	**Interrupt Pointer** INTP determines the number n (n = 0-15) of the service request output SRn that becomes active on a channel interrupt. 0000_B SR0 selected for channel 0x interrupt 0001_B SR1 selected for channel 0x interrupt …$_B$ … 1111_B SR15 selected for channel 0x interrupt *Note: In the TC1798, SR[7:0] are connected to interrupt nodes. SR[15:8] are used as SDMA channel request inputs.*
IRDV	[15:12]	rw	**Interrupt Raise Detect Value** These bits specify the value of CHSR0x.TCOUNT for which the Interrupt Threshold Limit should be raised.
0	[31:16]	r	**Reserved** Read as 0; should be written with 0.

Note: The interrupt node of the wrap-around interrupts is shared with the pattern match interrupt. In order to support interrupt generation in case of a pattern match, the wrap-around interrupt should be disabled. If the wrap-around interrupts are used, the pattern match interrupt should not be used. The settings are independent for each SDMA channel.

The Address Control Register controls how source and destination addresses are updated after a SDMA move. Furthermore, it determines whether or not a source or destination address register update is shadowed.

SDMA_ADRCR0x (x = 0-7)
SDMA Channel 0x Address Control Register

($08C_H$+x*20_H) **Reset Value: 0000 0000_H**



Field	Bits	Type	Description
SMF	[2:0]	rw	**Source Address Modification Factor** This bit field and the data width as defined in CHCRx.CHDW determine an address offset value by which the source address is modified after each SDMA move. See also **Table 13-7**. 000_B Address offset is 1 x CHCR0x.CHDW 001_B Address offset is 2 x CHCR0x.CHDW 010_B Address offset is 4 x CHCR0x.CHDW 011_B Address offset is 8 x CHCR0x.CHDW 100_B Address offset is 16 x CHCR0x.CHDW 101_B Address offset is 32 x CHCR0x.CHDW 110_B Address offset is 64 x CHCR0x.CHDW 111_B Address offset is 128 x CHCR0x.CHDW
INCS	3	rw	**Increment of Source Address** This bit determines whether the address offset as selected by SMF will be added to or subtracted from the source address after each SDMA move. The source address is not modified if CBLS = 0000_B. 0_B Address offset will be subtracted 1_B Address offset will be added.

Field	Bits	Type	Description
DMF	[6:4]	rw	**Destination Address Modification Factor** This bit field and the data width as defined in CHCR0x.CHDW determines an address offset value by which the destination address is modified after each SDMA move. The destination address is not modified if CBLD = 0000_B. See also **Table 13-7**. 000_B Address offset is 1 x CHDW 001_B Address offset is 2 x CHDW 010_B Address offset is 4 x CHDW 011_B Address offset is 8 x CHDW 100_B Address offset is 16 x CHDW 101_B Address offset is 32 x CHDW 110_B Address offset is 64 x CHDW 111_B Address offset is 128 x CHDW
INCD	7	rw	**Increment of Destination Address** This bit determines whether the address offset as selected by DMF will be added to or subtracted from the destination address after each SDMA move. The destination address is not modified if CBLD = 0000_B. 0_B Address offset will be subtracted 1_B Address offset will be added
CBLS	[11:8]	rw	**Circular Buffer Length Source** This bit field determines which part of the 32-bit source address register remains unchanged and is not updated after a SDMA move operation (see also **Section 13.2.4.7**). Therefore, CBLS also determines the size of the circular source buffer. 0000_B Source address SADR[31:0] is not updated 0001_B Source address SADR[31:1] is not updated 0010_B Source address SADR[31:2] is not updated 0011_B Source address SADR[31:3] is not updated $\ldots_B$ ... 1110_B Source address SADR[31:14] is not updated 1111_B Source address SADR[31:15] is not updated

Field	Bits	Type	Description
CBLD	[15:12]	rw	**Circular Buffer Length Destination** This bit field determines which part of the 32-bit destination address register remains unchanged and is not updated after a SDMA move operation (see also Page 13-19). Therefore, CBLD also determines the size of the circular destination buffer. 0000_B Destination address DADR[31:0] is not updated 0001_B Destination address DADR[31:1] is not updated 0010_B Destination address DADR[31:2] is not updated 0011_B Destination address DADR[31:3] is not updated $\ldots_B$ ... 1110_B Destination address DADR[31:14] is not updated 1111_B Destination address DADR[31:15] is not updated
SHCT	[17:16]	rw	**Shadow Control** This bit field determines whether an address is transferred into the shadow address register when writing to source or destination address register. 00_B Shadow address register not used. Source and destination address register are written directly 01_B Shadow address register used for source address buffering. When writing to SADR0x, the address is buffered in SHADR0x and transferred to SADR0x with the start of the next SDMA transaction 10_B Shadow address register used for destination address buffering. When writing to DADR0x, the address is buffered in SHADR0x and transferred to DADR0x with the start of the next SDMA transaction 11_B Reserved In case of SHCT = 01_B or 10_B, SHCT must not be changed until the next SDMA transaction has been started.

Field	Bits	Type	Description
SHWEN	18	rw	**Shadow Address Register Write Enable** This bit determines whether the shadow address register SHADR0x is read only and automatically set to 0000 0000_H or if the shadow register can also be directly written and not modified when and shadow transfer takes place. 0_B Shadow address register is read only and the value stored in the SHADR0x is automatically set to 0000 0000_H when the shadow transfer takes place 1_B Shadow address register SHADR0x can be read and can be directly written. The value stored in the SHADR0x is not automatically modified when the shadow transfer takes place
0	[31:19]	r	**Reserved** Read as 0; should be written with 0.

Table 13-7 shows the offset values that are added or subtracted to/from a source or destination address register after a SDMA move. Bit field SMF and bit INCS determine the offset value for the source address. Bit field DMF and bit INCD determine the offset value for the destination address.

Table 13-7 Address Offset Calculation Table

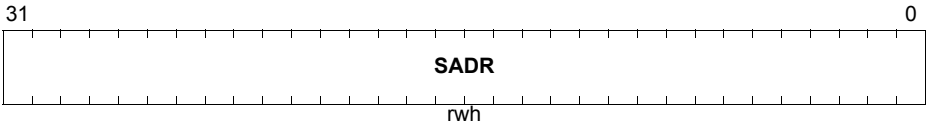
CHCR0n.CHDW = 00_B (8-bit Data Width)			CHCR0n.CHDW = 01_B (16-bit Data Width)			CHCR0n.CHDW = 10_B (32-bit Data Width)		
SMF DMF	**INCS INCD**	**Address Offset**	**SMF DMF**	**INCS INCD**	**Address Offset**	**SMF DMF**	**INCS INCD**	**Address Offset**
000_B	0	-1	000_B	0	-2	000_B	0	-4
	1	+1		1	+2		1	+4
001_B	0	-2	001_B	0	-4	001_B	0	-8
	1	+2		1	+4		1	+8
010_B	0	-4	010_B	0	-8	010_B	0	-16
	1	+4		1	+8		1	+16
011_B	0	-8	011_B	0	-16	011_B	0	-32
	1	+8		1	+16		1	+32
100_B	0	-16	100_B	0	-32	100_B	0	-64
	1	+16		1	+32		1	+64
101_B	0	-32	101_B	0	-64	101_B	0	-128
	1	+32		1	+64		1	+128
110_B	0	-64	110_B	0	-128	110_B	0	-256
	1	+64		1	+128		1	+256
111_B	0	-128	111_B	0	-256	111_B	0	-512
	1	+128		1	+256		1	+512

Note: CHCR0n.CHDW = 11_B is reserved and should not be used.

13.3.5 Channel Address Registers

The Source Address Register contains the 32-bit source address. If a SDMA channel 0n is active, SADR0n is updated continuously (if programmed) and shows the actual source address that is used for read moves within SDMA transfers.

SDMA_SADR0x (x = 0-7)
SDMA Channel 0x Source Address Register
(090_H+x*20_H) **Reset Value: 0000 0000_H**

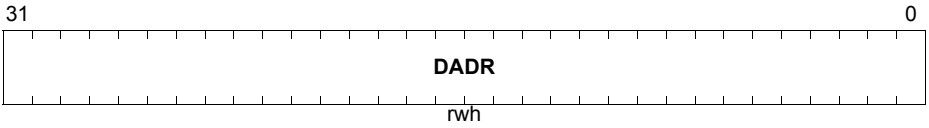


Field	Bits	Type	Description
SADR	[31:0]	rwh	**Source Start Address** This bit field holds the actual 32-bit source address of SDMA channel 0x that is used for read moves.

A write to SADR0n is executed directly only when the SDMA channel 0n is inactive (CHSR0n.TCOUNT = 0 and TRSR.CH0n = 0). If SDMA channel 0n is active when writing to SADR0n, the source address will not be written into SADR0n directly but will be buffered in the shadow register SHADR0n until the start of the next SDMA transaction. During this shadowed address register operation, bit field ADRCR0n.SHCT must be set to 01_B.

The Destination Address Register contains the 32-bit destination address. If a SDMA channel is active, DADR0n is updated continuously (if programmed) and shows the actual destination address that is used for write moves within SDMA transfers.

SDMA_DADR0x (x = 0-7)
SDMA Channel 0x Destination Address Register
(094_H+x*20_H) **Reset Value: 0000 0000_H**

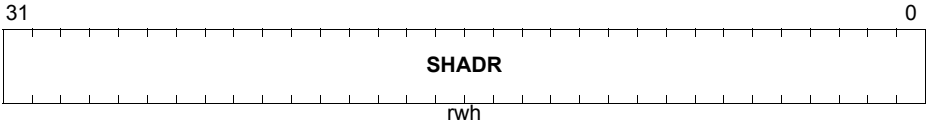


Field	Bits	Type	Description
DADR	[31:0]	rwh	**Destination Address** This bit field holds the actual 32-bit destination address of SDMA channel 0x that is used for write moves.

A write to DADR0n is executed directly only when the SDMA channel 0n is inactive (CHSR0n.TCOUNT = 0 and TRSR.CH0n = 0). If SDMA channel 0n is active when writing to DADR0n, the source address will not be written into DADR0n directly but will be buffered in the shadow register SHADR0n until the start of the next SDMA transaction. During this shadowed address register operation, bit field ADRCR0n.SHCT must be set to 10_B.

The Shadow Address Register holds the shadowed source or destination address before it is written into the source or destination address register. SHADR0n can be read only.

SDMA_SHADR0x (x = 0-7)
SDMA Channel 0x Shadow Address Register
(098_H+x*20_H) **Reset Value: 0000 0000_H**



Field	Bits	Type	Description
SHADR	[31:0]	rwh	**Shadowed Address** This bit field holds the shadowed 32-bit source or destination address of SDMA channel x.

SHADR0n is written when source or destination address buffering is selected (ADRCR0n.SHCT = 01_B or ADRCR0n.SHCT = 10_B) and a transaction is running. While the shadow mechanism is disabled, SHADR is set to 0000 0000_H.

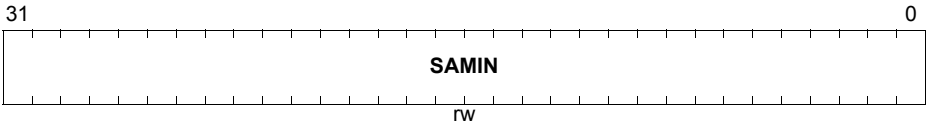
If ADRCR0n.SHWEN = 0 the value stored in the SHADR is automatically set to 0000 0000_H when the shadow transfer takes place. The user can read the shadow register in order to detect if the shadow transfer has already taken place. If the value in SHADR is 0000 0000_H, no shadow transfer can take place and the corresponding address register is modified according to the circular buffer rules.

If ADRCR0n.SHWEN = 1 shadow register SHADR0n can be directly written. The value stored in the SHADR0n is not modified when the shadow transfer takes place, the shadow mechanism remains active and the shadow transfer will be repeated until Channel 0n is reset or until the value in SHADR is 0000 0000_H, is written into the shadow register.

13.3.6 Memory Protection Registers

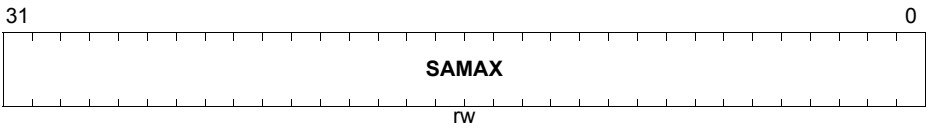
The Memory Protection Registers control the lower and upper source and destination address boundaries. Only 32-bit word accesses are permitted to the memory protection registers. Byte and half word accesses will return a bus error.

SDMA_SAMIN0x (x = 0-7)
SDMA Channel 0x Source Address Lower Boundary Register
(180_H+x*20_H) Reset Value: 0000 0000_H



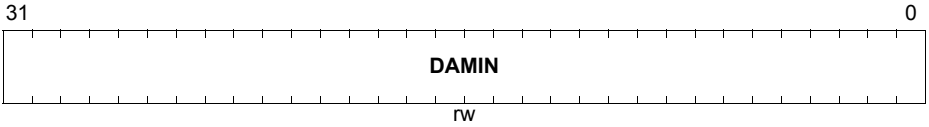
Field	Bits	Type	Description
SAMIN	[31:0]	rw	**Source Address Lower Boundary** This bit field holds the 32-bit source address lower boundary value of SDMA channel 0x that is used for read moves.

SDMA_SAMAX0x (x = 0-7)
SDMA Channel 0x Source Address Lower Boundary Register
(184_H+x*20_H) Reset Value: FFFF $FFFF_H$



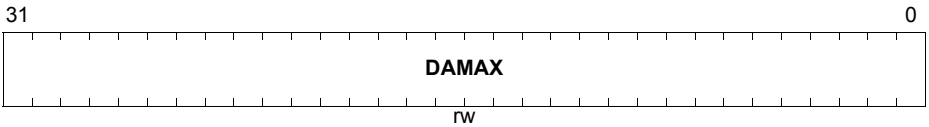
Field	Bits	Type	Description
SAMAX	[31:0]	rw	**Source Address Upper Boundary** This bit field holds the 32-bit source address upper boundary value of SDMA channel 0x that is used for read moves.

SDMA_DAMIN0x (x = 0-7)
SDMA Channel 0x Destination Address Lower Boundary Register
(188_H+x*20_H) **Reset Value: 0000 0000_H**



Field	Bits	Type	Description
DAMIN	[31:0]	rw	**Destination Address Lower Boundary** This bit field holds the 32-bit destination address lower boundary value of SDMA channel 0x that is used for write moves.

SDMA_DAMAX0x (x = 0-7)
SDMA Channel 0x Destination Address Upper Boundary Register
($18C_H$+x*20_H) **Reset Value: FFFF $FFFF_H$**



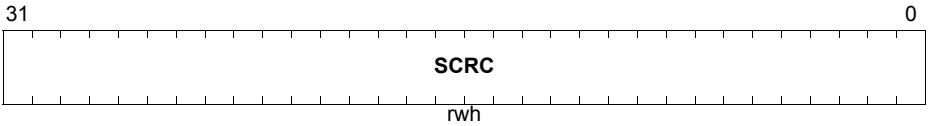
Field	Bits	Type	Description
DAMAX	[31:0]	rw	**Destination Address Upper Boundary** This bit field holds the 32-bit destination address upper boundary value of SDMA channel 0x that is used for write moves.

13.3.7 Channel CRC Registers

The Channel CRC Registers store the working CRC32 ethernet polynomial checksum. Only 32-bit word accesses are permitted to the CRC registers. Byte and half word accesses will return a bus error.

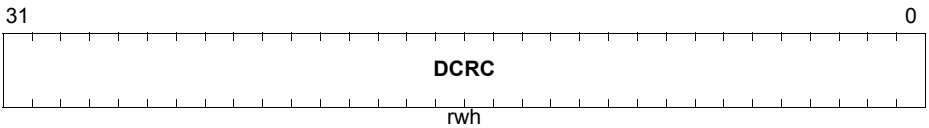
In order to start a CRC32 sequence the CRC registers must be initialized (e.g. written with 00000000_H or with a desired start value) and an SDMA transaction must be set up (start address, length, etc.). During each SDMA Move a read move loads data from a data source to the SDMA Controller and a write move puts data from the SDMA controller to a DMA destination. During an SDMA Move each CRC register will perform one polynomial checksum calculation.

SDMA_SCRC0x (x = 0-7)
SDMA Channel 0x Source Address CRC Register
(190_H+x*20_H) **Reset Value: 0000 0000_H**



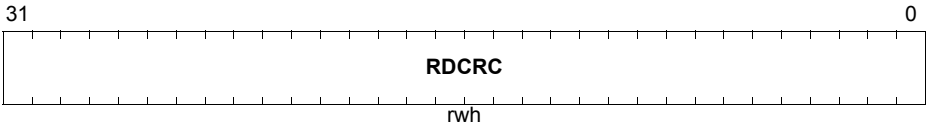
Field	Bits	Type	Description
SCRC	[31:0]	rwh	**Source Address CRC** This bit field contains the working CRC32 ethernet polynomial checksum for the source address.

SDMA_DCRC0x (x = 0-7)
SDMA Channel 0x Destination Address CRC Register
(194_H+x*20_H) **Reset Value: 0000 0000_H**



Field	Bits	Type	Description
DCRC	[31:0]	rwh	**Destination Address CRC** This bit field contains the working CRC32 ethernet polynomial checksum for the destination address.

SDMA_RDCRC0x (x = 0-7)
SDMA Channel 0x Read Data CRC Register
(198_H+x*20_H) **Reset Value: 0000 0000_H**



Field	Bits	Type	Description
RDCRC	[31:0]	rwh	**Read Data CRC** This bit field contains the working CRC32 ethernet polynomial checksum for read data.

13.4 SDMA Module Implementation

This section describes the TC1798 SDMA module interfaces with the clock control, interrupt control, and address decoding.

Figure 13-27 shows the TC1798-specific implementation details and interconnections of the SDMA module. The SDMA module is supplied with a separate clock control, address decoding, interrupt control, and the request input wiring matrix.

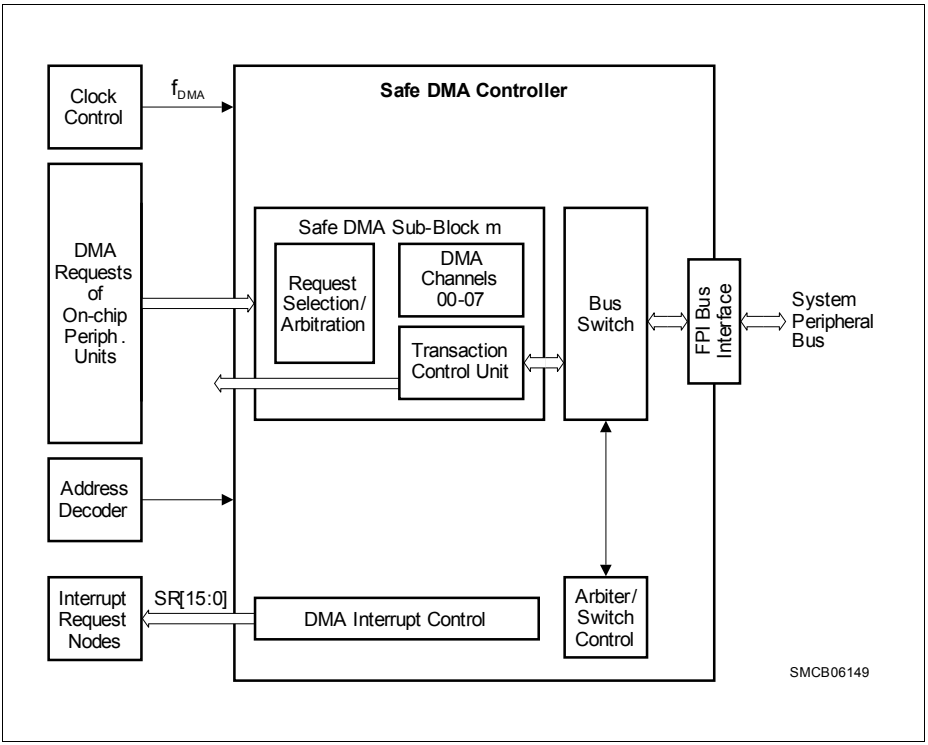


Figure 13-27 SDMA Module Implementation and Interconnections

The request sources of the peripheral modules (ADC0, MultiCAN, and SCU) are associated with Interrupt Node Pointers and individual interrupt enable bits. As a result, each of the internal requests of a module can be routed independently to any of the interrupt output lines (INT_Ox) of the module.

13.4.1 SDMA Request Wiring Matrix

The SDMA request input lines of each SDMA channel within the SDMA Sub-Block are connected to request output lines from the peripheral modules according to **Table 13-8**.

Table 13-8 SDMA Request Assignment for SDMA Sub-Block

SDMA Channel	SDMA Request Line	SDMA Requesting Unit	Selected by
00	SDMA_SR08	SDMA(INT_O08)	CHCR00.PRSEL = 0000_B
	IOUT0	SCU (ERU)	CHCR00.PRSEL = 0001_B
	SENT_TRIG0	SENT	CHCR00.PRSEL = 0010_B
	ADC_SR02	ADC	CHCR00.PRSEL = 0011_B
	SSC0_RDR	SSC0	CHCR00.PRSEL = 0100_B
	ASC0_RDR	ASC0	CHCR00.PRSEL = 0101_B
	FADC_SR00	FADC	CHCR00.PRSEL = 0110_B
	MIL0_SR4	MIL0	CHCR00.PRSEL = 0111_B
	MISC0_SR2	MSC0	CHCR00.PRSEL = 1000_B
	GPTA_TRIG00	GPTA	CHCR00.PRSEL = 1001_B
	-	-	CHCR00.PRSEL = 1010_B
	INT1SRC	ERAY	CHCR00.PRSEL = 1011_B
	IBUSY	ERAY	CHCR00.PRSEL = 1100_B
	-	-	CHCR00.PRSEL = 1101_B
	-	-	CHCR00.PRSEL = 1110_B
	-	-	CHCR00.PRSEL = 1111_B
01	SDMA_SR09	SDMA(INT_O09)	CHCR01.PRSEL = 0000_B
	IOUT1	SCU (ERU)	CHCR01.PRSEL = 0001_B
	SENT_TRIG1	SENT	CHCR01.PRSEL = 0010_B
	ADC_SR03	ADC	CHCR01.PRSEL = 0011_B
	SSC0_TDR	SSC0	CHCR01.PRSEL = 0100_B
	ASC1_RDR	ASC1	CHCR01.PRSEL = 0101_B
	FADC_SR01	FADC	CHCR01.PRSEL = 0110_B
	MIL0_SR5	MIL0	CHCR01.PRSEL = 0111_B
	MSC0_SR3	MSC0	CHCR01.PRSEL = 1000_B
	GPTA_TRIG01	GPTA	CHCR01.PRSEL = 1001_B
	-	-	CHCR01.PRSEL = 1010_B
	TINT0SRC	ERAY	CHCR01.PRSEL = 1011_B
	-	-	CHCR01.PRSEL = 1100_B

Table 13-8 SDMA Request Assignment for SDMA Sub-Block (cont'd)

SDMA Channel	SDMA Request Line	SDMA Requesting Unit	Selected by
	-	-	CHCR01.PRSEL = 1101_B
	-	-	CHCR01.PRSEL = 1110_B
	-	-	CHCR01.PRSEL = 1111_B
02	SDMA_SR10	SDMA(INT_O10)	CHCR02.PRSEL = 0000_B
	IOUT2	SCU (ERU)	CHCR02.PRSEL = 0001_B
	SENT_TRIG2	SENT	CHCR02.PRSEL = 0010_B
	ADC_SR04	ADC	CHCR02.PRSEL = 0011_B
	SSC1_RDR	SSC1	CHCR02.PRSEL = 0100_B
	ASC0_TDR	ASC0	CHCR02.PRSEL = 0101_B
	ASC0_TBDR	ASC0	CHCR02.PRSEL = 0110_B
	MIL0_SR6	MIL0	CHCR02.PRSEL = 0111_B
	MSC0_SR2	MSC0	CHCR02.PRSEL = 1000_B
	GPTA_TRIG02	GPTA	CHCR02.PRSEL = 1001_B
	CCU60_SR0	CCU60	CHCR02.PRSEL = 1010_B
	NDAT1SRC	ERAY	CHCR02.PRSEL = 1011_B
	-	-	CHCR02.PRSEL = 1100_B
	-	-	CHCR02.PRSEL = 1101_B
	-	-	CHCR02.PRSEL = 1110_B
	-	-	CHCR02.PRSEL = 1111_B
03	SDMA_SR11	SDMA(INT_O11)	CHCR03.PRSEL = 0000_B
	IOUT3	SCU (ERU)	CHCR03.PRSEL = 0001_B
	SENT_TRIG3	SENT	CHCR03.PRSEL = 0010_B
	ADC_SR05	ADC	CHCR03.PRSEL = 0011_B
	SSC1_TDR	SSC1	CHCR03.PRSEL = 0100_B
	ASC1_TDR	ASC1	CHCR03.PRSEL = 0101_B
	ASC1_TBDR	ASC1	CHCR03.PRSEL = 0110_B
	MIL0_SR7	MIL0	CHCR03.PRSEL = 0111_B
	MSC0_SR3	MSC0	CHCR03.PRSEL = 1000_B
	GPTA_TRIG03	GPTA	CHCR03.PRSEL = 1001_B
	CCU61_SR0	CCU61	CHCR03.PRSEL = 1010_B

Table 13-8 SDMA Request Assignment for SDMA Sub-Block (cont'd)

SDMA Channel	SDMA Request Line	SDMA Requesting Unit	Selected by
	MBSC1SRC	ERAY	CHCR03.PRSEL = 1011_B
	-	-	CHCR03.PRSEL = 1100_B
	-	-	CHCR03.PRSEL = 1101_B
	-	-	CHCR03.PRSEL = 1110_B
	-	-	CHCR03.PRSEL = 1111_B
04	SDMA_SR12	SDMA(INT_O12)	CHCR04.PRSEL = 0000_B
	STMIRQ0	STM	CHCR04.PRSEL = 0001_B
	SENT_TRIG4	SENT	CHCR04.PRSEL = 0010_B
	ADC_SR06	ADC	CHCR04.PRSEL = 0011_B
	SSC2_RDR	SSC2	CHCR04.PRSEL = 0100_B
	ASC0_TDR	ASC0	CHCR04.PRSEL = 0101_B
	ASC0_TBDR	ASC0	CHCR04.PRSEL = 0110_B
	MIL0_SR4	MIL0	CHCR04.PRSEL = 0111_B
	MSC1_SR2	MSC1	CHCR04.PRSEL = 1000_B
	GPTA_TRIG10	GPTA	CHCR04.PRSEL = 1001_B
	-	-	CHCR04.PRSEL = 1010_B
	INT1SRC	ERAY	CHCR04.PRSEL = 1011_B
	OBUSY	ERAY	CHCR04.PRSEL = 1100_B
	-	-	CHCR04.PRSEL = 1101_B
	-	-	CHCR04.PRSEL = 1110_B
	-	-	CHCR04.PRSEL = 1111_B
05	SDMA_SR13	SDMA(INT_O13)	CHCR05.PRSEL = 0000_B
	STMIRQ0	STM	CHCR05.PRSEL = 0001_B
	SENT_TRIG5	SENT	CHCR05.PRSEL = 0010_B
	ADC_SR07	ADC	CHCR05.PRSEL = 0011_B
	SSC2_TDR	SSC2	CHCR05.PRSEL = 0100_B
	ASC1_TDR	ASC1	CHCR05.PRSEL = 0101_B
	ASC1_TBDR	ASC1	CHCR05.PRSEL = 0110_B
	MIL0_SR5	MIL0	CHCR05.PRSEL = 0111_B
	MSC1_SR3	MSC1	CHCR05.PRSEL = 1000_B

Table 13-8 SDMA Request Assignment for SDMA Sub-Block (cont'd)

SDMA Channel	SDMA Request Line	SDMA Requesting Unit	Selected by
	GPTA_TRIG11	GPTA	CHCR05.PRSEL = 1001_B
	-	-	CHCR05.PRSEL = 1010_B
	TINT1SRC	ERAY	CHCR05.PRSEL = 1011_B
	-	-	CHCR05.PRSEL = 1100_B
	-	-	CHCR05.PRSEL = 1101_B
	-	-	CHCR05.PRSEL = 1110_B
	-	-	CHCR05.PRSEL = 1111_B
06	SDMA_SR14	SDMA(INT_O14)	CHCR06.PRSEL = 0000_B
	CAM_INT_O0	MultiCAN	CHCR06.PRSEL = 0001_B
	SENT_TRIG6	SENT	CHCR06.PRSEL = 0010_B
	ADC_SR08	ADC	CHCR06.PRSEL = 0011_B
	SSC2_RDR	SSC2	CHCR06.PRSEL = 0100_B
	ASC0_RDR	ASC0	CHCR06.PRSEL = 0101_B
	FADC_SR00	FADC	CHCR06.PRSEL = 0110_B
	MIL0_SR6	MIL0	CHCR06.PRSEL = 0111_B
	MSC1_SR2	MSC1	CHCR06.PRSEL = 1000_B
	GPTA_TRIG12	GPTA	CHCR06.PRSEL = 1001_B
	CCU62_SR0	CCU62	CHCR06.PRSEL = 1010_B
	NDAT1SRC	ERAY	CHCR06.PRSEL = 1011_B
	-	-	CHCR06.PRSEL = 1100_B
	-	-	CHCR06.PRSEL = 1101_B
	-	-	CHCR06.PRSEL = 1110_B
	-	-	CHCR06.PRSEL = 1111_B
07	SDMA_SR15	SDMA(INT_O15)	CHCR07.PRSEL = 0000_B
	CAM_INT_O1	MultiCAN	CHCR07.PRSEL = 0001_B
	SENT_TRIG7	SENT	CHCR07.PRSEL = 0010_B
	ADC_SR09	ADC	CHCR07.PRSEL = 0011_B
	SSC2_TDR	SSC2	CHCR07.PRSEL = 0100_B
	ASC1_RDR	ASC1	CHCR07.PRSEL = 0101_B
	FADC_SR01	FADC	CHCR07.PRSEL = 0110_B

Table 13-8 SDMA Request Assignment for SDMA Sub-Block (cont'd)

SDMA Channel	SDMA Request Line	SDMA Requesting Unit	Selected by
	MIL0_SR7	MIL0	CHCR07.PRSEL = 0111_B
	MSC1_SR3	MSC1	CHCR07.PRSEL = 1000_B
	GPTA_TRIG13	GPTA	CHCR07.PRSEL = 1001_B
	CCU63_SR0	CCU63	CHCR07.PRSEL = 1010_B
	MBSC1SRC	ERAY	CHCR07.PRSEL = 1011_B
	-	-	CHCR07.PRSEL = 1100_B
	-	-	CHCR07.PRSEL = 1101_B
	-	-	CHCR07.PRSEL = 1110_B
	-	-	CHCR07.PRSEL = 1111_B

13.4.2 Implementation-specific SDMA Registers

The SDMA controller as implemented in the TC1798 contains the following additional registers:

- SDMA clock control register
- Service request control registers for SDMA controller interrupts (SDMA_SRCx)

Figure 13-28 provides an overview of these registers.

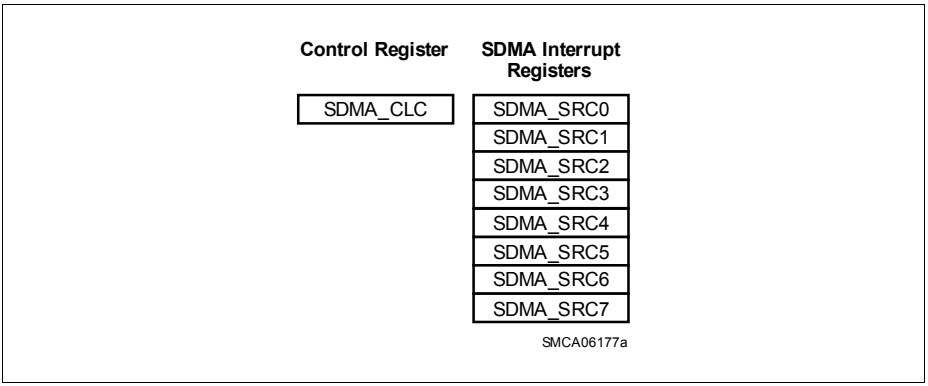


Figure 13-28 SDMA Implementation-specific Registers

Note: Further details on interrupt handling and processing are described in the "Interrupt System" chapter of the TC1798 System Units User´s Manual.

The clock generation and interrupt control configuration as implemented in the SDMA controller module is shown in **Figure 13-29**.

The SDMA controller is supplied from a common module clock f_{SDMA} that has the frequency of the FPI-Bus clock f_{FPI} and is controlled via the SDMA_CLC clock control register.

The SDMA controller module contains in total 8 interrupt request nodes with its interrupt service request control registers:

- Eight interrupt requests SR[7:0] = INT_O[7:0] from the SDMA controller; upper eight interrupt requests of the SDMA controller INT_O[15:8] are used as SDMA channel trigger inputs.

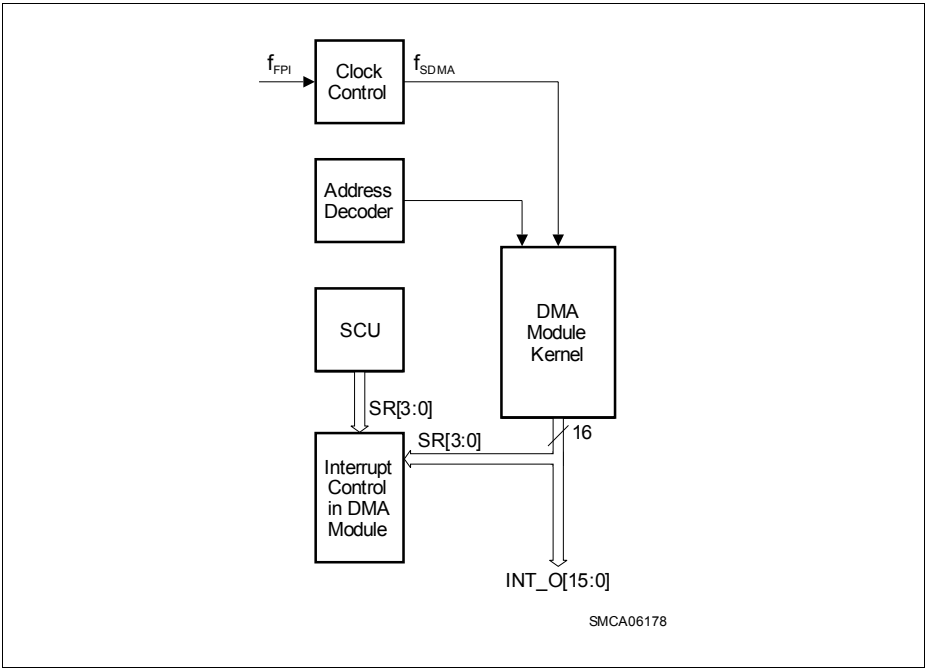
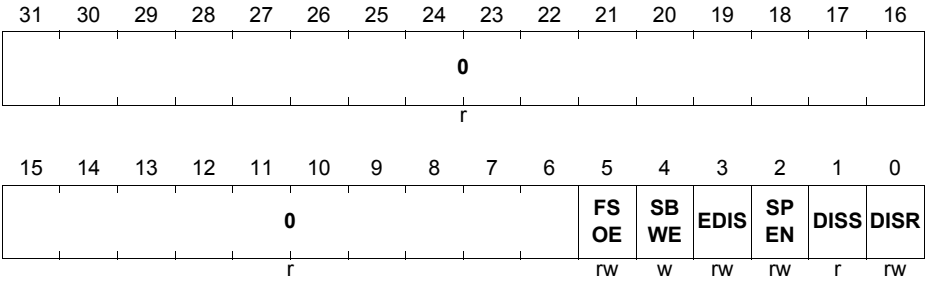


Figure 13-29 Implementation of the SDMA Module

13.4.2.1 Clock Control Register

The Clock Control Register controls the SDMA module internal f_{SDMA} clock signal.

SDMA_CLC
SDMA Clock Control Register (000_H) Reset Value: 0000 0000_H



Field	Bits	Type	Description
DISR	0	rw	**Module Disable Request Bit** Used for enable/disable control of the module
DISS	1	r	**Module Disable Status Bit** Bit indicates the current status of the module
SPEN	2	rw	**Module Suspend Enable for OCDS** Used to enable the Suspend Mode
EDIS	3	rw	**Sleep Mode Enable Control** Used for module sleep mode control. 0_B Sleep mode request is regarded. Module is enabled to go into sleep mode. 1_B Sleep mode request is disregarded. Sleep mode cannot be entered on a request.
SBWE	4	w	**Module Suspend Bit Write Enable for OCDS** Determines whether SPEN and FSOE are write-protected.

Field	Bits	Type	Description
FSOE	5	rw	**Fast Switch Off Enable** Used for fast clock switch-off in Suspend Mode. 0_B Clock switch-off in Suspend Mode via Disable Control Feature (Secure Clock Switch Off) selected 1_B Fast clock switch off in Suspend Mode selected This bit can be written only if SBWE is set during the same write operation.
0	[31:6]	r	**Reserved** Read as 0; should be written with 0.

Note: After a hardware reset operation, the SDMA module is enabled.

Note: The suspend mode does not modify any of the registers.

13.4.2.2 SDMA Interrupt Registers

In the TC1798, the lower eight SDMA controller interrupts SR[7:0] are connected to service request control registers. The upper eight SDMA controller interrupt outputs SR[15:8] are used as SDMA channel request inputs.

SDMA_SRCx (x = 0-7)
SDMA Service Request Control Register x
($2FC_H$ - x*4_H) **Reset Value: 0000 0000_H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SETR	CLRR	SRR	SRE	0	TOS	0		SRPN							
w	w	rh	rw	r	rw	r		rw							

Field	Bits	Type	Description
SRPN	[7:0]	rw	**Service Request Priority Number**
TOS	10	rw	**Type of Service Control** 0_B CPU service is initiated 1_B PCP request is initiated
SRE	12	rw	**Service Request Enable**
SRR	13	rh	**Service Request Flag**
CLRR	14	w	**Request Clear Bit**
SETR	15	w	**Request Set Bit**
0	[9:8], 11, [31:16]	r	**Reserved** Read as 0; should be written with 0.

13.4.3 Address Map

The SDMA controller register block address map is shown in **Figure 13-30**. It shows how the different register blocks are arranged and adds the absolute address information.

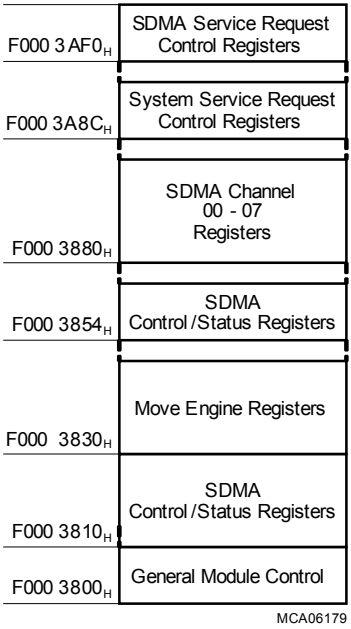


Figure 13-30 SDMA Controller Register Block Address Map

14 Flexible CRC Engine (FCE)

This document describes the Flexible CRC Engine (FCE) module. The FCE provides a parallel implementation of one or more Cyclic Redundancy Code (CRC) algorithms. The current FCE version for the TC1798 microcontroller implements the IEEE 802.3 ethernet CRC32 and the Castagnoli CRC32C polynomials. FCE's generic structure enables it to be extended with multiple CRC polynomials. The primary target of FCE is to be used as an hardware acceleration engine for software applications or operating systems services (compatible with Autosar CRC "specification of CRC Routines") using CRC signatures. CRC algorithms are commonly used to calculate unique message signatures that can be used to check message integrity during transport over communication channels like internal busses or interfaces between micro-controllers. CRC signatures are also suitable to sign blocks of data residing in variable or invariable storage elements. Signatures computed based on polynomial division provide a very high bit error detection capability. The FCE operates as a standard FPI bus slave peripheral and is fully controlled through a set of configuration and control registers.

This chapter is structured as follows:

- **"FCE Features" on Page 14-3**
- **"Operational overview" on Page 14-4**
- **"FCE Functional Description" on Page 14-6**
- **"FCE Module Registers" on Page 14-14**
- **"Interfaces of the FCE Module" on Page 14-13**
- **"Programming Guide" on Page 14-28**
- **"Properties of CRC code" on Page 14-31**

*Note: The FCE kernel register names described in **"FCE Module Registers" on Page 14-14** are referenced in a product User´s Manual by the module name prefix "FCE_".*

Note: The FCE may in the future be used as well in a 16-bit microcontroller. There is no such requirement currently, but this possible extension can already be considered during the development phase.

14.1 Related documentation

Input documents

- [D1] A painless guide to CRC Error Detection Algorithms, Ross N. Williams
- [D2] Autosar R3.1 Rev 0001, Specification of CRC Routines V3.0.2
- [D3] 32-Bit Cyclic Redundancy Codes for Internet Applications, Philip Koopman, International Conference on Dependable Systems and Networks (DSN), 2002

Related standards and norms

- [S1] IEEE 802.3 Ethernet 32-bits CRC

14.2 FCE Features

The FCE provides the following features:

- Architecture supports up to 4 different CRC polynomials. Current FCE version implements:
  - IEEE 802.3 CRC32 ethernet polynomial: 0x82608EDB[1)] (crc kernel 0)
  - CRC32C Castagnoli polynomial: 0x8F6E37A0 (crc kernel 1)
- Parallel CRC implementation (32-bits wide)
  - Data blocks to be computed by FCE shall be a multiple of 32-bits
  - Start address of Data blocks to be computed by FCE shall be at least 32-bits aligned
- Only 32-bit write accesses are allowed to the kernel input register.
  - 8 or 16-bit write accesses to the configuration registers are supported.
- Register Interface compliant with Autosar specification for CRC routines. Enables to support reentrant software routines via a software-based save/restore mechanism.
- Extended register interface to control reliability of FCE execution.
- Critical Registers controlling the FCE operation are implemented redundant to capture transient errors
- Error notification scheme via dedicated interrupt node for:
  - transient error detection: error interrupt generation (maskable) with local status register (cleared by software)
  - Checksum failure: error interrupt generation (maskable) with local status register (cleared by software)
- FCE implements its own Interrupt Service Node

1) The polynomial hexadecimal representation covers the coefficients 32 down to 1 (x^0 is implicit) enabling to use 32-bits to characterize the polynomial.

14.3 Operational overview

The FCE is a standard FPI slave module. The FCE is fully synchronous with the FPI bus and runs with a 1:1 clock ratio. It connects to the FPI peripheral bus of a micro-controller.

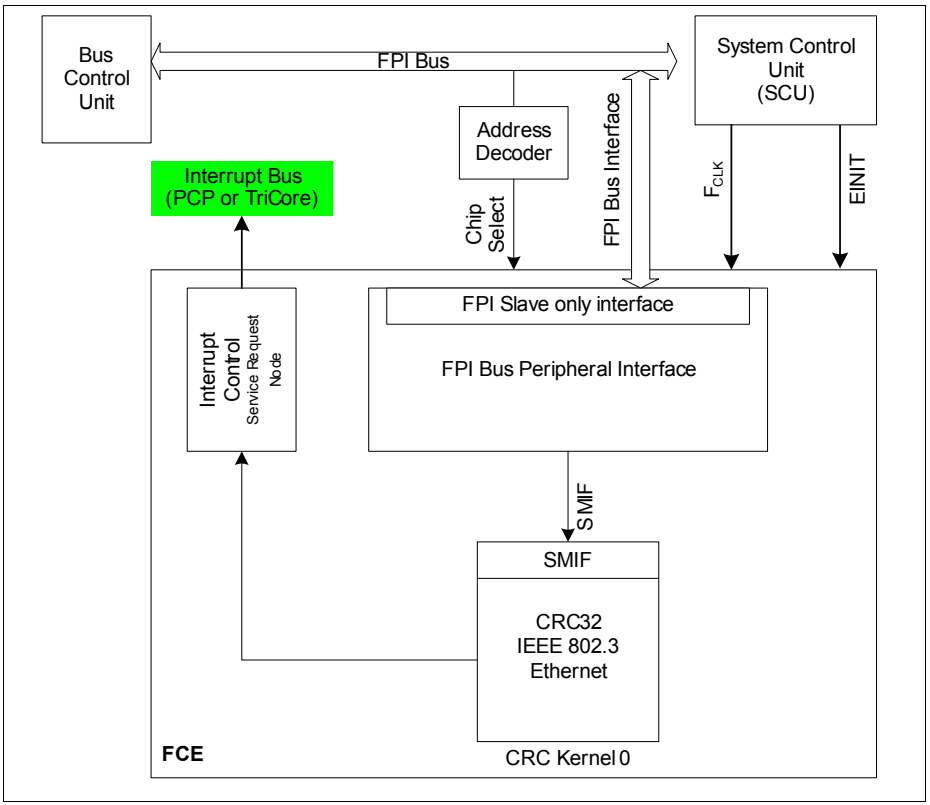


Figure 14-1 FCE system integration: single CRC kernel

The FCE operation is controlled over a set of memory mapped registers. The main purpose is to serve as hardware acceleration for software applications requiring CRC checksum computation. The register set has been designed to enable the FCE. Depending on the hardware configuration the FCE may implement more crc kernels with different CRC polynomials. The specific configuration for a product will be described into the product customizing chapter. Every crc kernel will present the same hardware and software architecture. The rest of this document will focus only on the description of the generic CRC kernel architecture. The **Figure 14-2** shows a multi kernel configuration.

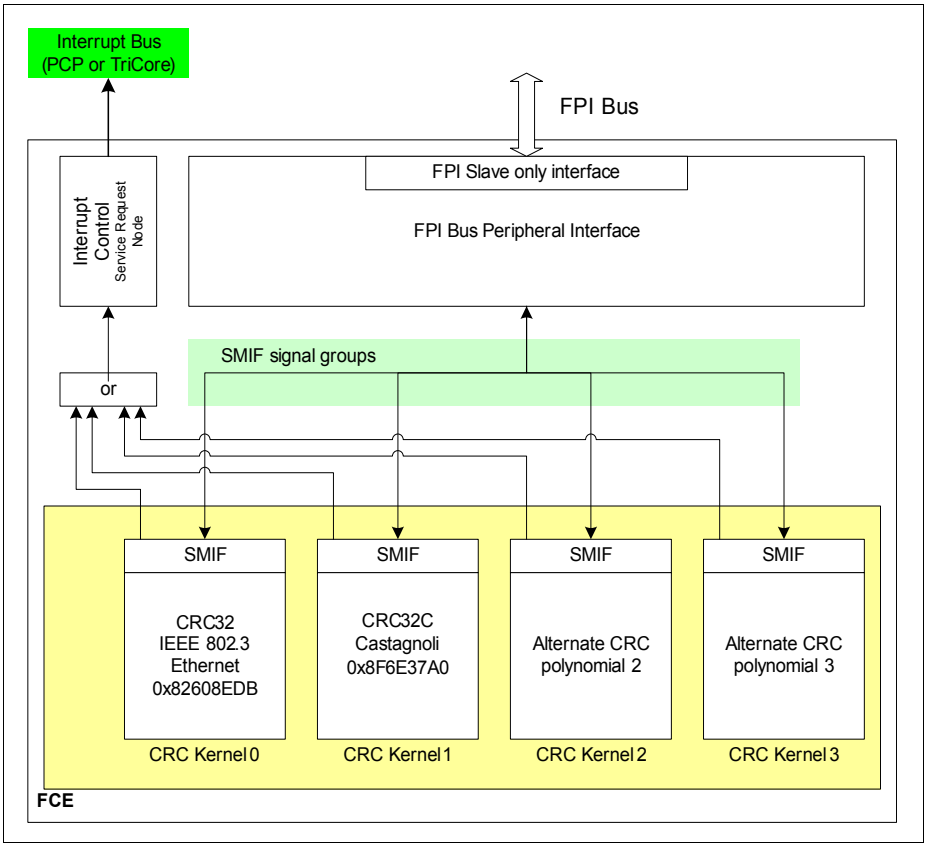


Figure 14-2 FCE system integration: multi-crc kernels

In a multi-kernel implementation the interrupt lines are ored together, the FCE only present a single interrupt node to the system. Each crc kernel implements a status register that enables the software to identify which interrupt source is active. Please refer to the STS register description for a detailed description of the status and interrupt handling.

14.4 FCE Functional Description

.

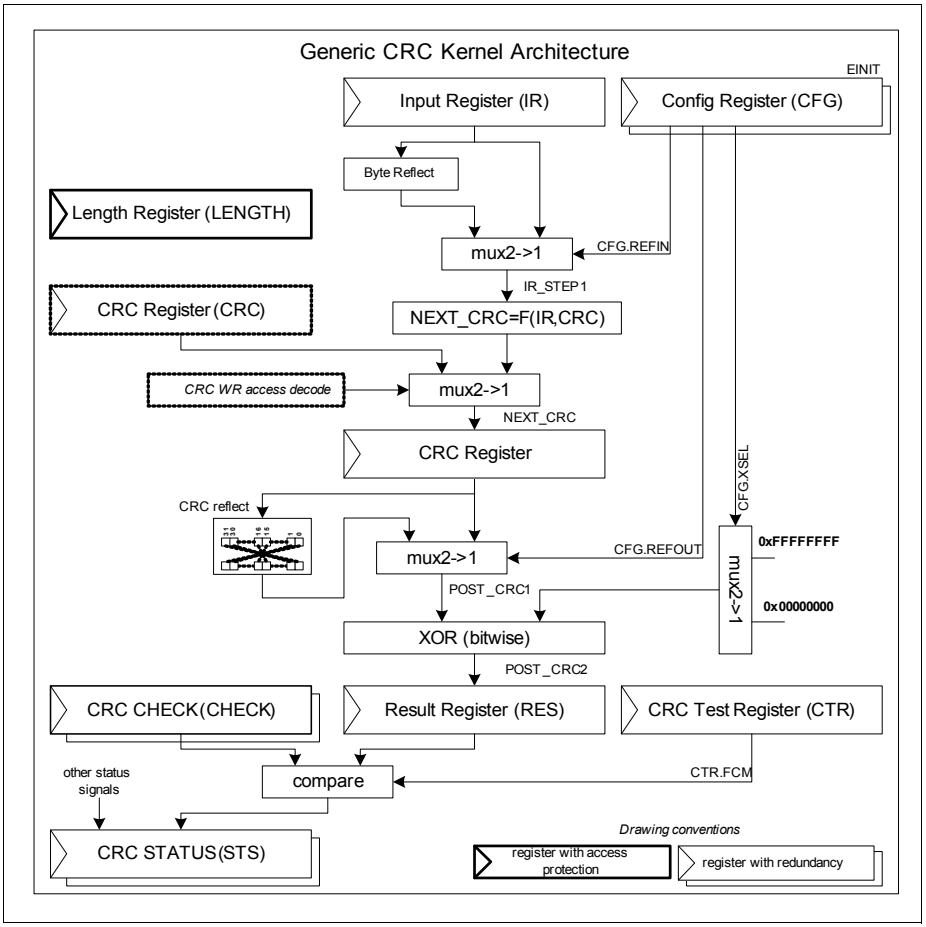


Figure 14-3 CRC kernel architecture

A checksum algorithm based on CRC polynomial division is characterized by the following properties:

- [1] polynomial degree (e.g. 32, that represents the highest power of two of the polynomial)
- [2] polynomial (e.g. 0x04C11DB7: the 33rd bit is omitted because always equal to 1)
- [3] init value: the initial value of the CRC register

- [4] input data reflected: indicates if each byte of the input parallel data is reflected before being used to compute the CRC
- [4] result data reflected: indicates if the final CRC value is reflected or not
- [5] XOR value: indicates if a final XOR operation is done before returning the CRC result

All the properties are static once a polynomial has been chosen. However the FCE provides the capability to control the two reflection steps and the final xor as depicted in **Figure 14-3** through the CFG register. The reset values are compatible with the implemented algorithm. The final xor control enables to select either 0xFFFFFFFF or 0x00000000 to be xored with the POST_CRC1 (see **Figure 14-3**) value. These two values are those used by the most common CRC polynomials.

Note: The reflection steps and final XOR do not modify the properties of the CRC algorithm in terms of error detection, only the CRC final signature is affected.

CRC operation

Software must first ensure that the CRC kernel is properly configured, especially the initial CRC register value written via the **CRC** register. If the software whishes to use the automatic signature check at the end of a message, the LENGTH register and CHECK registers must be configured with respectively the length (as number of 32-bit words) of the message and the expected signature (**CHECK**). The **CHECK** value takes into account the final CRC reflection and XOR operation. The self check is enable by the **CFG.CCE** bit field.

Property:
If the input message M1 consists of a message M0 appended with the CRC signature of M0, then the CRC signature of M1 shall be 0.

The software writes as many times as necessary into the **IR** register according to the length of the message. If **CFG.CCE** bit field is set, every time the IR register is written, the LENGH register is decremented by one. If **LENGTH** is already at zero but software still writes to **IR** (by mistake) every bit of the **LENGTH** should be set to 1 and hold this value until software initializes it again for the processing of a new message. In such case the STS.MLF (Message Length Flag) should be set and an interrupt generated if the CFG.MLE (Message length Error) is set. The hardware monitors the transition of the **LENGTH** register from 1 to 0 to detect the end of the message and proceed with the comparison of the POST_CRC2 (see **Figure 14-3**) value with the **CHECK** register value.

The next two figures provides an overview of the control and status features of a CRC kernel.

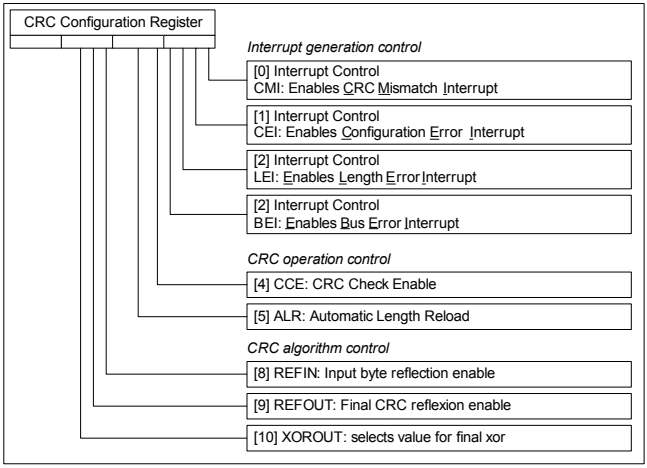


Figure 14-4 CRC kernel configuration register

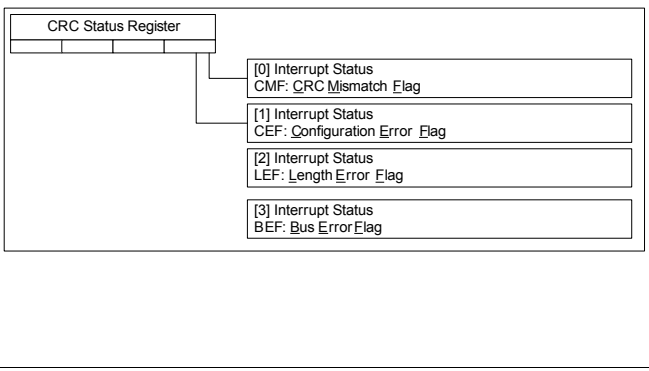


Figure 14-5 CRC kernel status register

Register Protection and Monitoring methods

Register Monitoring: applied to CFG and CHECK registers

Because CFG and CHECK registers are critical to the CRC operation, some mechanisms to detect and log transient errors are provided. Early detection of transient failures enables to improve the failure detection time and asses the severity of the failure. The monitoring mechanisms are implemented using two redundant instances as presented in **Figure 14-6**.

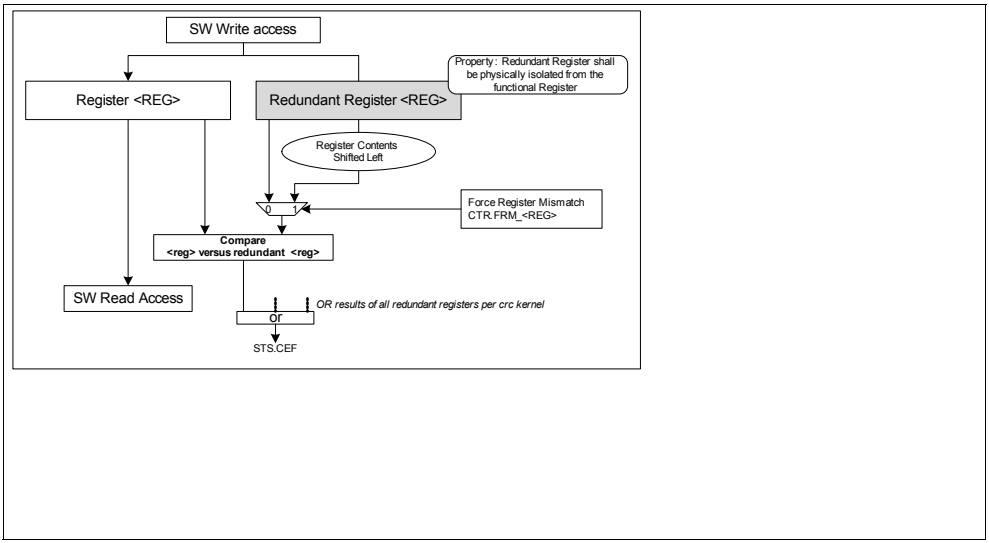


Figure 14-6 Register monitoring scheme

Let <REG> designate either CFG or CHECK registers. When a write to <REG> takes place a copy of the redundant register is also updated. **Redundant registers are not visible to software**. Bits of <REG> reserved have no storage and are not used for redundancy. A compare logic continuously compares the two stored values and provides a signal that indicates if the compare is successful or not. The result of all compare blocks are ored together to provide a single flag information. If a mismatch is detected the **STS.CEF** (Configuration Error Flag) bit is set. For run-time validation of the compare logic a Force Register Mismatch bit field (**CTR.FRM_<REG>**) is provided. When set to 1 by software the contents of the redundant register is shifted left by one bit position (redundant bit 0 position is always replaced by a logical 0 value) and is given to the compare logic instead of the redundant register value. This enables to check the compare logic is functional. Using a walking bit pattern, the software can completely check the full operation of the compare logic.

Register Access Protection: applies to LENGTH and CHECK registers

In order to reduce the probability of a mis-configuration of the CHECK and LENGTH registers (in the case the automatic check is used), the write access to the CHECK and LENGTH registers must follow the procedure depicted in **Figure 14-7**:

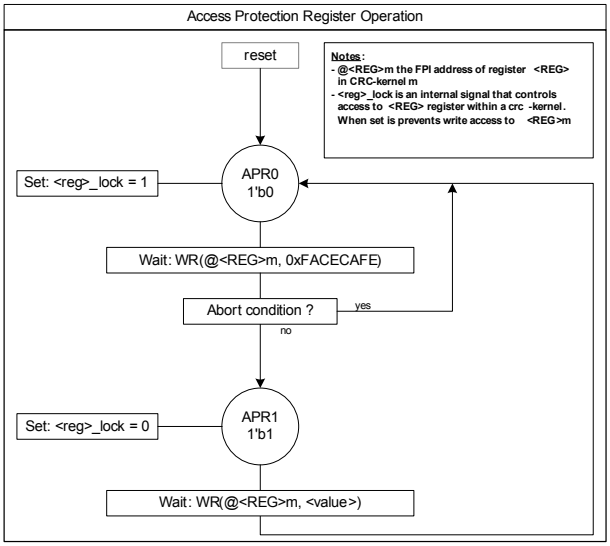


Figure 14-7 Access control to CHECK register

Let **<REG>** designate **CHECK** or **LENGTH** registers. Before being able to configure a new <value> value into the CHECK register of a crc kernel, software must first write the 0xFACECAFE value to the CHECK address. The 0xFACECAFE is not written into the CHECK register. The next write access will proceed as a normal FPI write access. This procedure will then be repeated every time software wants to configure a new <REG> value. If software reads the CHECK register just after writing 0xFACECAFE it returns the current <REG> contents and not 0xFACECAFE. **A read access to <REG> has no effect on the protection mechanism**.

FCE interrupts

Each FCE crc kernel provides one internal interrupt source. The interrupt lines from each crc kernel are ored together to be sent to the FCE interrupt control block that implements the standard interrupt node logic and register. When multiple crc kernels are present within a FCE, the interrupt lines from each crc kernel are ored together to provide a single interrupt source to the interrupt control block. If the interrupt from the FCE is arbitrated, the FCE interrupt handler must use the status information located within the **STS** status register of each crc kernel.

Each crc kernel provides the following interrupt sources:

- CRC Mismatch Interrupt controlled by **CFG.CMI** bit field and observable via the status bit field **STS.CMF** (CRC Mismatch Flag).
- Configuration Error Interrupt controlled by **CFG.CEI** bit field and observable via the status bit field **STS.CEF** (Configuration Error Flag).
- Length Error Interrupt controlled by **CFG.LEI** bit field and observable via the status bit field **STS.LEF** (Length Error Flag).
- FPI Error Interrupt controlled by **CFG.FEI** bit field and observable via the status bit field **STS.FEF** (FPI Error Flag).

Interrupt generation rules

- A status flag shall be cleared by software by writing a **1** to the corresponding bit position.
- If an status flag is set and a new hardware condition occurs, no new interrupt is generated by the kernel: the STS.<FLAG> bit field masks the generation of a new interrupt from the same source. If a SW access to clear the interrupt status bit takes place and in the same cycle the hardware wants to set the bit, the hardware condition wins the arbitration.

As all the interrupts are caused by an error condition, the interrupt shall be handled by a Error Management software layer. The software services using the FCE as acceleration engine may not directly deal with error conditions but let the upper layer using the service to deal with the error handling.

14.5 Interfaces of the FCE Module

The FCE module implements its own interrupt node, therefore implements an interface to the TriCore and PCP interrupt controllers. For protection purposes it uses the EINIT information to control the configuration of critical resources. The EINIT protection is described in the register chapter.

Table 14-1 Generic FCE Digital Connections

Signal	from/to Module	I/O to FCE
EINIT	SCU	I

14.6 FCE Module Registers

Figure 14-8 and Table 14-3 show all registers associated with a FCE crc-kernel. All FCE kernel register names are described in this section. They should get the prefix “FCE_” when used in the context of a product specification.

The registers are numbered by one index to indicate the related FCE CRC Kernel (m = 0-1).

FCE Registers Overview

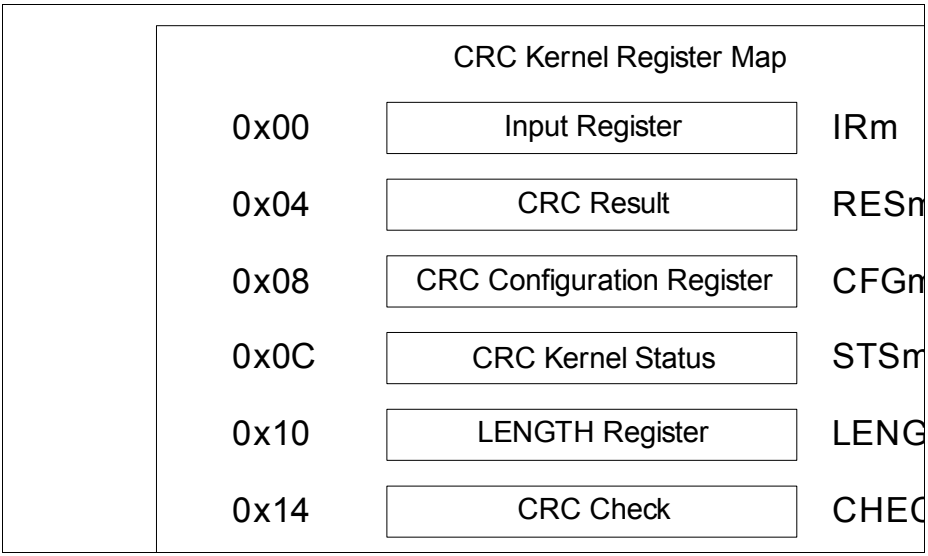


Figure 14-8 FCE Kernel Registers

Figure 14-9 shows the FCE module register map. The system registers region comprises the interrupt service request node and module identifier registers.

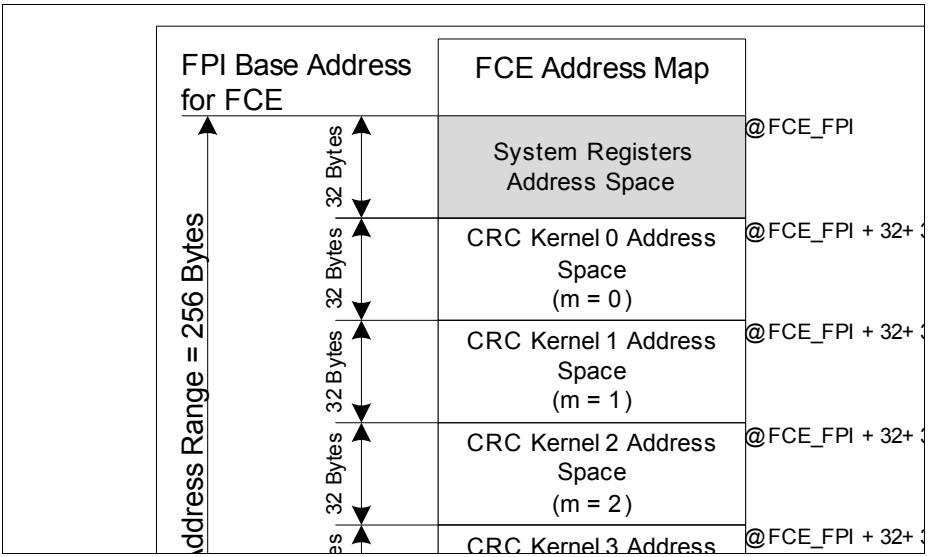


Figure 14-9 FCE Register Map

Table 14-2 Registers Address Space - FCE Module

Module	Base Address	End Address	Note
FCE	$F032\ 0000_H$	$F032\ 00FF_H$	

Table 14-3 Registers Overview - CRC Kernel Registers

Short Name	Description	Offset Addr.[1)]	Access Mode		Reset Class	Description See
			Read	Write		
FCE_CLC	Clock Control Register	00_H	U, SV	**E, SV**	3	**Page 14-17**
FCE_ID	Module Identification Register	08_H	U, SV	BE	3	**Page 14-20**
IRm	Input Register m	$20_H + m*20_H$	U, SV	U, SV	3	**Page 14-21**
RESm	CRC Result Register m	$24_H + m*20_H$	U, SV	BE	3	**Page 14-21**
CFGm	CRC Configuration Register m	$28_H + m*20_H$	U, SV	**E, SV**	3	**Page 14-22**

Table 14-3 Registers Overview - CRC Kernel Registers

Short Name	Description	Offset Addr.[1)]	Access Mode		Reset Class	Description See
			Read	Write		
STSm	CRC Status Register m	$2C_H$ + m*20_H	U, SV	U, SV	3	Page 14-24
LENGTHm	CRC Length Register m	30_H + m*20_H	U, SV	U, SV	3	Page 14-25
CHECKm	CRC Check Register m	34_H + m*20_H	U, SV	U, SV	3	Page 14-25
CRCm	CRC Register m	38_H + m*20_H	U, SV	U, SV	3	Page 14-26
CTRm	CRC Test Register m	$3C_H$ + m*20_H	U, SV	U, SV	3	Page 14-27
FCE_SRC	Service Request Control Register	FC_H	U, SV	SV	3	Page 14-18

1) The absolute register byte address for each crc kernel m is calculated as follows:
CRC kernel register base Address (Table 14-2) + m*20H, m = 0-1

Access Mode Rules

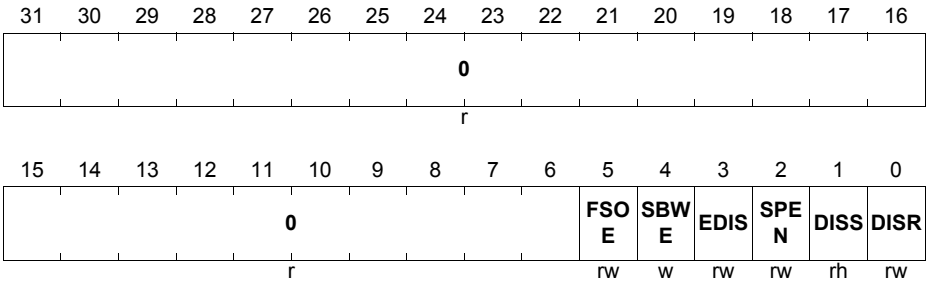
The Table 14-3 “Registers Overview - CRC Kernel Registers” on Page 14-15 uses the standard access mode conventions.

- **E** indicates that an access is only possible if the **end of initialization** signal from the System Control Unit is active. In this case Supervisor Mode (SV) is also mandatory.
- When U, SV are both listed it means that a read or write access can be done either in user mode (U) or supervisor mode (V).
- BE stands for Bus Error, NSC stands for No Special Condition.

14.6.1 System Registers

FCE Module Clock Control Register. This register is global to FCE and not part of a crc kernel. FCE does not implement a fractional divider, the FCE kernel (when enabled) always runs with the peripheral bus clock.

FCE_CLC
Control Clock Register **(00_H)** **Reset Value: 0000 0003$_H$**



Field	Bits	Type	Description
DISR	0	rw	**Module Disable Bit Request** Used for enable/disable control of the module 0_B Module disable is not requested 1_B Module disable is requested
DISS	1	rh	**Module Disable Bit Status** Bit indicates the current status of the module 0_B Module is enabled 1_B Module is disabled
SPEN	2	rw	**Module Suspend Enable** Used for enabling the Suspend Mode. 0_B Module cannot be suspended (suspend is disabled) 1_B Module can be suspended (suspend is enabled) This bit can be written only if SBWE is set during the same write operation.

Field	Bits	Type	Description
EDIS	3	rw	**Sleep Mode Enable Control** Used for module Sleep Mode control. 0_B Sleep Mode request is regarded. Module is enabled to go into Sleep Mode. 1_B Sleep Mode request is disregarded: Sleep Mode cannot be entered on a request.
SBWE	4	w	**Module Suspend Bit Write Enable for OCDS** Determines whether SPEN and FSOE are write-protected. 0_B Bits SPEN and FSOE are write-protected 1_B Bits SPEN and FSOE are overwritten by respective value of SPEN or FSOE Reading this bit returns always 0.
FSOE	5	rw	**Fast Switch Off Enable** Used for fast clock switch-off in Suspend Mode. 0_B Clock switch-off in Suspend Mode via Disable Control Feature (Secure Clock Switch Off) selected 1_B Fast clock switch off in Suspend Mode selected This bit can be written only if SBWE is set during the same write operation.
0	[31:6]	r	**Reserved** Read as 0; should be written with 0.

FCE_SRC

Service Request Control Register (FC_H) Reset Value: 0000 0000$_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

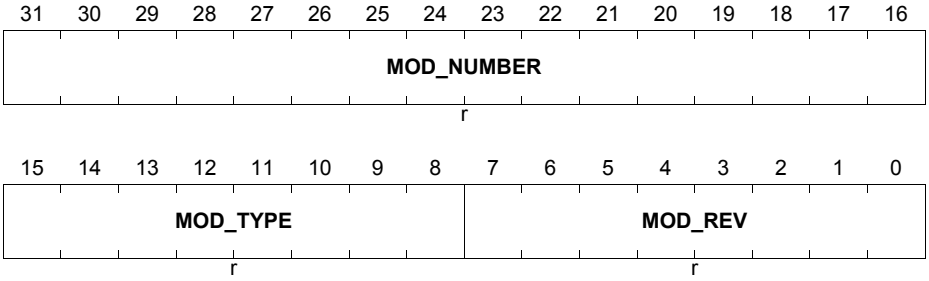
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SETR	CLRR	SRR	SRE	0	TOS	0		SRPN							
w	w	rwh	rw	r	rw	r		rw							

Field	Bits	Type	Description
SRPN	[7:0]	rw	**Service Request Priority Number** 00_H Service request is never serviced 01_H Service request is on lowest priority ... FF_H Service request is on highest priority
TOS	10	rw	**Type of Service Control** 0_B CPU service is initiated 1_B PCP service is initiated
SRE	12	rw	**Service Request Enable** 0_B Service request is disabled 1_B Service request is enabled
SRR	13	rwh	**Service Request Flag** 0_B No service request is pending 1_B A service request is pending[1)]
CLRR	14	w	**Request Clear Bit** CLRR is required to clear SRR. 0_B No action 1_B Clear SRR; bit value is not stored; read always returns 0; no action if SETR is set also.
SETR	15	w	**Request Set Bit** SETR is required to set SRR. 0_B No action 1_B Set SRR; bit value is not stored; read always returns 0; no action if CLRR is set also.
0	[9:8], 11, [31:16]	r	**Reserved** Read as 0; should be written with 0.

1) The bit field SRR is automatically cleared by hardware at the end of an interrupt arbitration round if the node was the winner, therefore this information is not suitable for interrupt plausibility checks.

FCE Module Identification Register. This register is global to FCE and not part of a crc kernel.

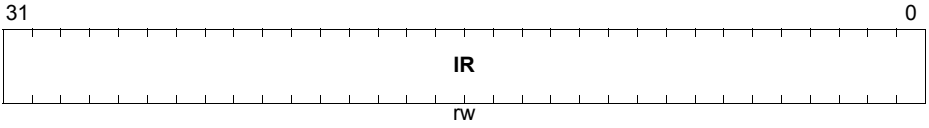
FCE_ID
Module Identification Register (08$_H$) Reset Value: 008A C001$_H$



Field	Bits	Type	Description
MOD_REV	[7:0]	r	**Module Revision Number** This bit field defines the module revision number. The value of a module revision starts with 01$_H$ (first revision).
MOD_TYPE	[15:8]	r	**Module Type** The bit field is set to C0$_H$ which defines the module as a 32-bit module.
MOD_NUMBER	[31:16]	r	**Module Number Value** This bit field defines a module identification number. The value for the FCE module is 008A$_H$.

14.6.2 CRC Kernel Control/Status Registers

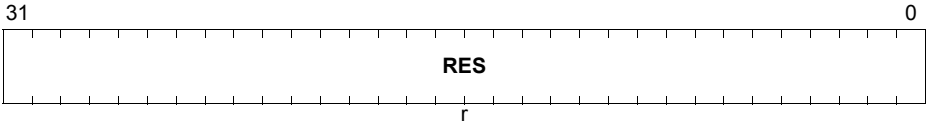
IRm (m = 0-1)
Input Register m **(20_H + m*20_H)** **Reset Value: 0000 0000_H**



Field	Bits	Type	Description
IR	[31:0]	rw	**Input Register** This bit field holds the 32-bit data to be computed

A write to IRm triggers the CRC kernel to update the message checksum according to the IR contents and to the current CRC register contents. Only 32-bit write transactions are allowed to IRm registers, any other FPI write transaction will lead to a Bus Error.

RESm (m = 0-1)
CRC Result Register m **(24_H + m*20_H)** **Reset Value: FFFF $FFFF_H$**



Field	Bits	Type	Description
RES	[31:0]	r	**Result Register** Returns the final CRC value including CRC reflection and final XOR according to the CFG register configuration. Writing to this register has no effect.

CFGm (m = 0-1)
CRC Configuration Register m

(28_H + m*20_H) **Reset Value: 0000 0700_H**

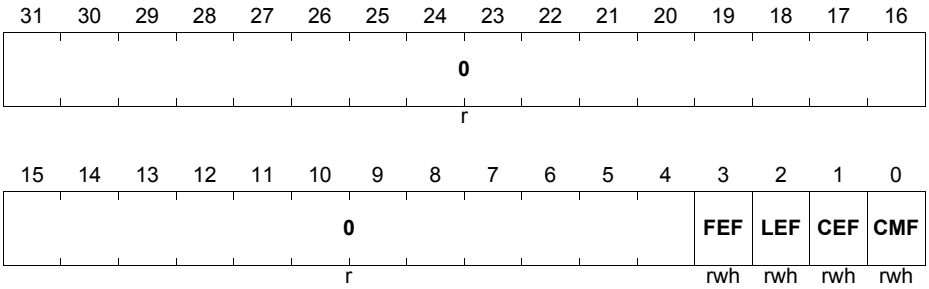
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0					X SEL	REF OUT	REF IN	0			CCE	FEI	LEI	CEI	CMI
r					rw	rw	rw	r			rw	rw	rw	rw	rw

Field	Bits	Type	Description
CMI	0	rw	**CRC Mismatch Interrupt** 0_B CRC Mismatch Interrupt is disabled 1_B CRC Mismatch Interrupt is enabled
CEI	1	rw	**Configuration Error Interrupt** When enabled, an Configuration Error Interrupt is generated whenever a mismatch is detected in the CFG and CHECK redundant registers. 0_B Configuration Error Interrupt is disabled 1_B Configuration Error Interrupt is enabled
LEI	2	rw	**Length Error Interrupt** When enabled, an Length Error Interrupt is generated if software writes to IR register with LENGTH equal to 0 and CFG.CCE is set to 1. 0_B Length Error Interrupt is disabled 1_B Length Error Interrupt is enabled
FEI	3	rw	**FPI Error Interrupt** When enabled, an interrupt is generated if a FPI write transaction other than 32-bits is issued to the Input register. 0_B FPI Error Interrupt is disabled 1_B FPI Error Interrupt is enabled

Field	Bits	Type	Description
CCE	4	rw	**CRC Check Comparison** 0_B CRC check comparison at the end of a message is disabled 1_B CRC check comparison at the end of a message is enabled
REFIN	8	rw	**IR Byte Wise Reflection** 0_B IR Byte Wise Reflection is disabled 1_B IR Byte Wise Reflection is enabled
REFOUT	9	rw	**CRC 32-Bit Wise Reflection** 0_B CRC 32-bit wise is disabled 1_B CRC 32-bit wise is enabled
XSEL	10	rw	**Selects the value to be xored with the final CRC** 0_B 0x00000000 1_B 0xFFFFFFFF
0	[7:5], [31:11]	r	**Reserved** Read as 0; should be written with 0.

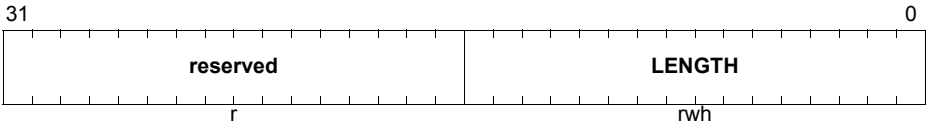
STSm (m = 0-1)
CRC Status Register m **($2C_H$ + m*20_H)** **Reset Value: 0000 0000_H**



Field	Bits	Type	Description
CMF	0	rwh	**CRC Mismatch Flag** This bit is set per hardware only. To clear this bit, software must write a 1 to this bit field location. Writing 0 per software has no effect. If this bit is equal to 1 and a new interrupt is raised by hardware, it will not be propagated to the FCE interrupt service node.
CEF	1	rwh	**Configuration Error Flag** This bit is set per hardware only. To clear this bit, software must write a 1 to this bit field location. Writing 0 per software has no effect. If this bit is equal to 1 and a new interrupt is raised by hardware, it will not be propagated to the FCE interrupt service node.
LEF	2	rwh	**Length Error Flag** This bit is set per hardware only. To clear this bit, software must write a 1 to this bit field location. Writing 0 per software has no effect. If this bit is equal to 1 and a new interrupt is raised by hardware, it will not be propagated to the FCE interrupt service node.
FEF	3	rwh	**FPI Error Flag** This bit is set per hardware only. To clear this bit, software must write a 1 to this bit field location. Writing 0 per software has no effect. If this bit is equal to 1 and a new interrupt is raised by hardware, it will not be propagated to the FCE interrupt service node.

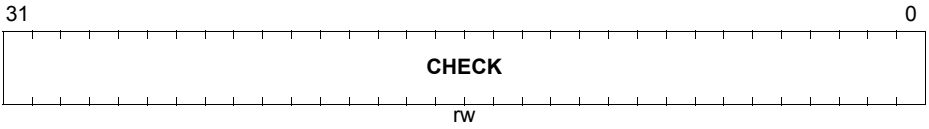
Field	Bits	Type	Description
0	[31:4]	r	**Reserved** Read as 0; should be written with 0.

LENGTHm (m = 0-1)
CRC Length Register m **(30_H + m*20_H)** **Reset Value: 0000 0000_H**



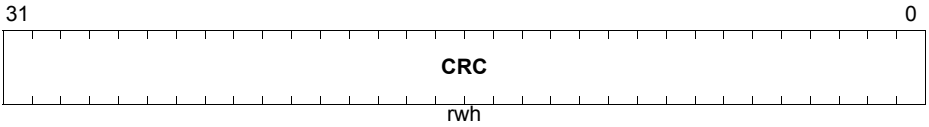
Field	Bits	Type	Description
LENGTH	[15:0]	rwh	**Message Length Register** Number of 32-bits words building the message over which the CRC checksum is calculated. This bit field is modified by the hardware: every write to the IR register decrements the value of the LENGTH bit field.
0	[31:16]	r	**Reserved** Read as 0; should be written with 0.

CHECKm (m = 0-1)
CRC Check Register m **(34_H + m*20_H)** **Reset Value: 0000 0000_H**



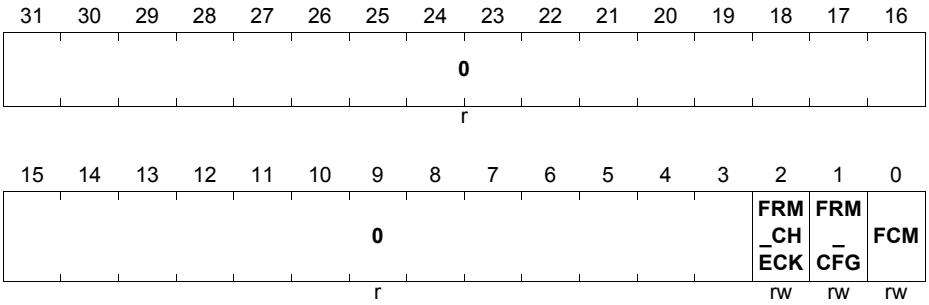
Field	Bits	Type	Description
CHECK	[31:0]	rw	**CHECK Register** Expected CRC value to be checked by the hardware upon detection of a 1 to 0 transition of the LENGTH register. The comparison is enabled by the CFG.CCE bit field

CRCm (m = 0-1)
CRC Register m **(38_H + m*20_H)** **Reset Value: 0000 0000_H**



Field	Bits	Type	Description
CRC	[31:0]	rwh	**CRC Register** This register enables to directly access the internal CRC register

CTRm (m = 0-1)
CRC Test Register m **($3C_H$ + m*20_H)** **Reset Value: 0000 0000_H**



Field	Bits	Type	Description
FCM	0	rw	**Force CRC Mismatch** Forces the CRC compare logic to issue an error regardless of the CHECK and CRC values. The hardware detects a 0 to 1 transition of this bit field and triggers a CRC Mismatch interrupt
FRM_CFG	1	rw	**Force CFG Register Mismatch** This field is used to control the error injection mechanism used to check the compare logic of the redundant CFG registers. This is a one shot operation. When the hardware detects a 0 to 1 transition of this bit field it triggers a Configuration Mismatch interrupt (if enabled by the corresponding CFGm register).
FRM_CHECK	2	rw	**Force Check Register Mismatch** This field is used to control the error injection mechanism used to check the compare logic of the redundant CHECK registers. This is a one shot operation. The hardware detects a 0 to 1 transition of this bit field and triggers a Check Register Mismatch interrupt (if enabled by the corresponding CFGm register).
0	[31:3]	r	**Reserved** Read as 0; should be written with 0.

14.7 Programming Guide

This section provides some guidelines showing how the FCE configuration features can be mapped to the AUTOSAR API for CRC32 routines.

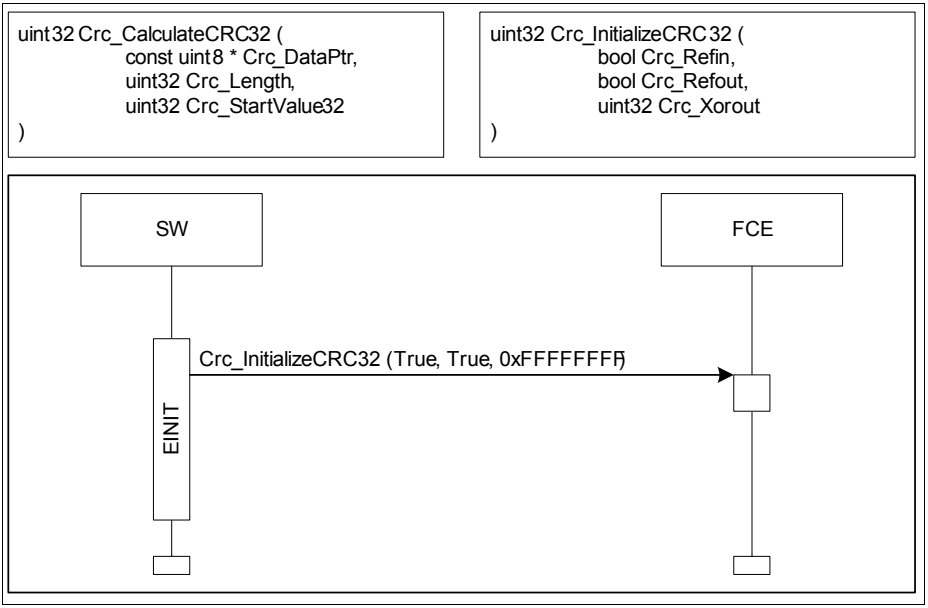


Figure 14-10 Autosar initialization API

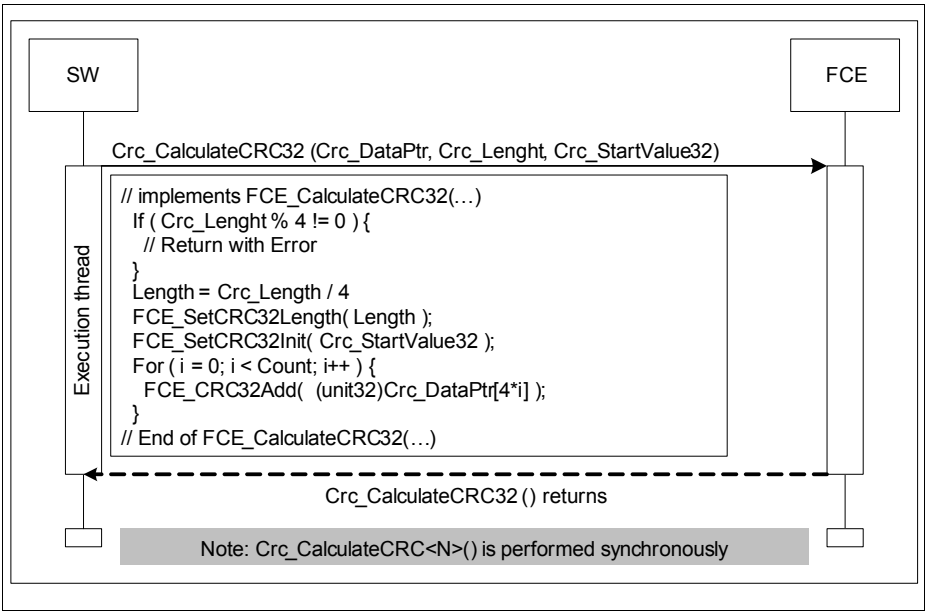


Figure 14-11 Autosar CRC_calculate API

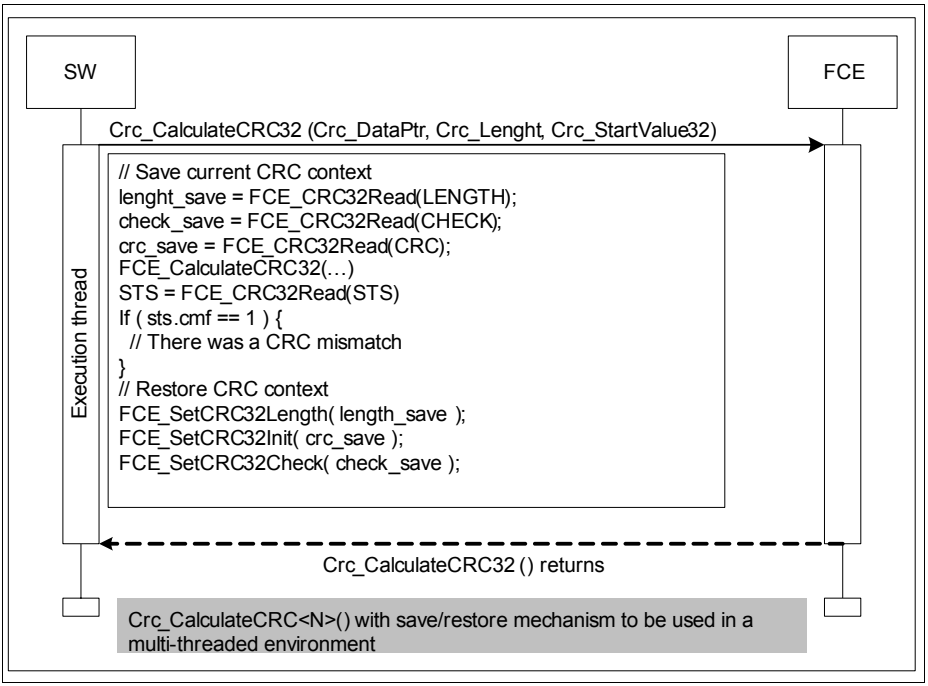


Figure 14-12 Autosar CRC_calculate API with save/restore

14.8 Properties of CRC code

Hamming Distance

The Hamming distance defines the error detection capability of a CRC polynomial. A cyclic code with a Hamming Distance of D can detect all D-1 bit errors. **Table 14-4 "Hamming Distance as a function of message length (bits)" on Page 14-31** shows the dependency of the Hamming Distance with the length of the message.

Table 14-4 Hamming Distance as a function of message length (bits)[1)]

Hamming Distance	IEEE CRC32	Castagnoli
15	8 - 10	
14	8 - 10	
13	8 - 10	
12	11 - 12	8 - 17
11	13 - 21	18 - 21
10	22 - 34	22 - 27
9	35 - 57	22 - 27
8	58 - 91	28 - 58
7	92 - 171	59 - 81
6	172 - 268	82 - 1060
5	269 - 2974	1061 - 65504
4	2973 - 91607	1061 - 65504
3	91607 - 131072	65506 - 131072

1) Data from technical paper "32-Bit Cyclic Redundancy Codes for Internet Applications" by Philip Koopman, Carnegie Mellon University, 2002

15 SRI External Bus Unit (EBU)

The External Bus Unit (EBU), TC1798 controls the transactions between external memories or peripheral units, and the internal memories and peripheral units. The basic interfaces of the EBU are shown in **Figure 15-1**.

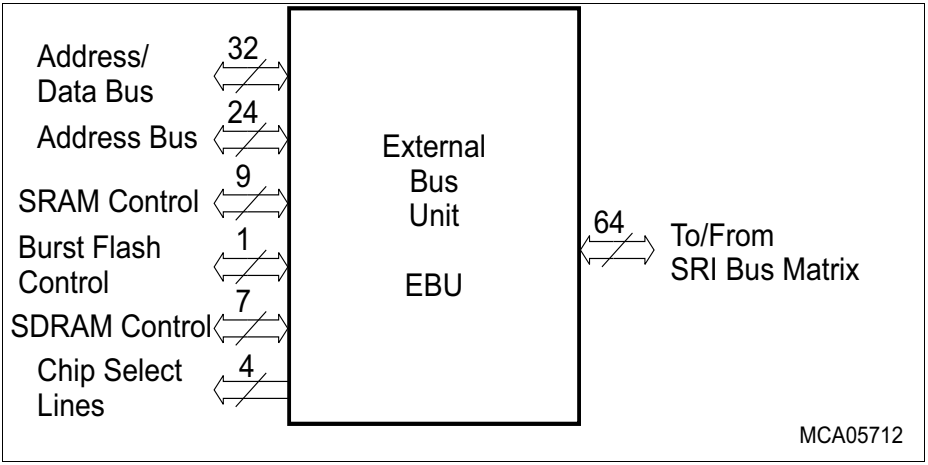


Figure 15-1 EBU Interface Diagram

The EBU is internally connected to the SRI Bus Matrix by a single slave interface.

15.1 Overview

The Memory Controller module for SRI-based systems connects on-chip controller cores (e.g. Tricore CPU, DMA Controller) to external resources such as memories and peripherals. **Figure 15-2** shows Memory Controller within a typical system.

Any SRI master can (in conjunction with an SRI Matrix) access external memories through the Memory Controller.

15.2 References

The EBU complies with the requirements of the following specifications when generating accesses to external memories:

- JESD21-C revision 18A, sections relating to SDRAM & LPSDRAM (3.11.5.1)
- JESD21-C revision 18A, section relating to LPDDR NVM (3.6.3).
- JESD209, Low Power Double Data Rate (LPDDR) SDRAM Standard
- Open NAND Flash Interface Specification. Revision 2.0, 27-February-2008
- Intel™, PC SDRAM Specification, revision 1.7, November 1999.

15.3 Feature List

Features supported in the Memory Controller:-

- Highly programmable access parameters.
- Intel-style peripheral/device support.
- Burst FLASH support (see **Section 15.17** for specific device types).
- Cellular RAM support (see **Section 15.17** for specific device types).
- NAND flash
- Multiplexed access (address & data on the same bus)
- Data Buffering: Two read buffers. Single write buffer in the SRI interface.
- Four programmable address regions.
- External bus frequency: Module frequency:flash clock = 1:1, 1:2, 1:3 or 1:4.
- JEDEC 42.4 LPDDR NVM support
- DDR burst flash support.
- SDRAM support (see **Section 15.18** for specific device types).
- DDRAM support (see **Section 15.18** for specific device types).
- ONFI 2.0 NAND flash support
- Configurable clock generation and edge recovery logic using a programmable DLL (Delay Locked Loop) to control clock phase and edge positioning
- External bus frequency: Module frequency:DDR device clock = 1:1, 1:2, or 1:4.

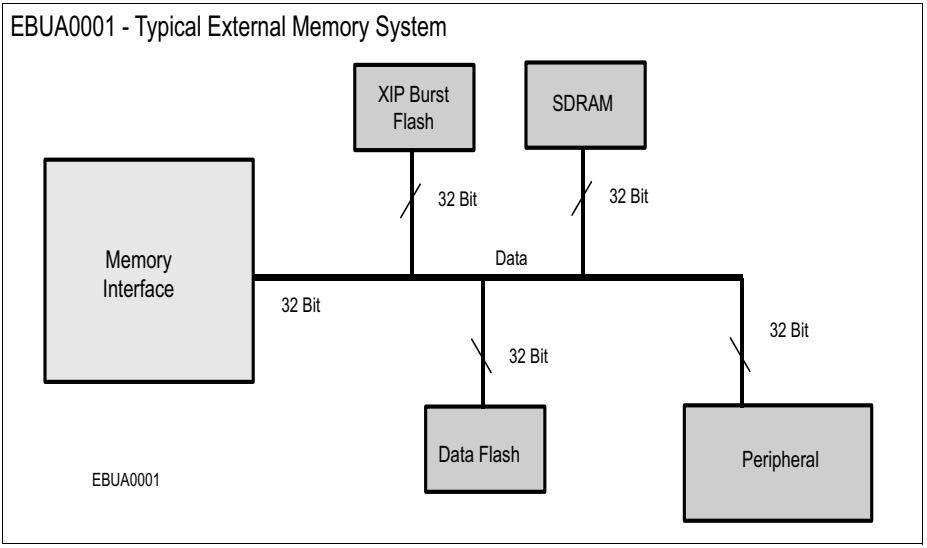


Figure 15-2 Typical External Memory System

15.4 Differences between Audo-Future and Audo-Max EBUs

The clocking scheme of the EBU has been upgraded. A DLL has been added to allow reconstruction of a 50% duty cycle clock and the generation of phase shifted clocks for DDR device support. This has added a new register, **EBU_DLLCON**, to the EBU register space.

The EBU can now also be configured to run at half the CPU frequency or asynchronously to the CPU using the Flexray PLL as its clock source. The features are programmed using the **SYNC** and **DIV2** fields in **EBU_CLC**.

New features have been added to the **EBU_MODCON** register:

- **BUSSTATE**, a monitor bit which is set to 1_B when the EBU owns the external bus
- **FAST_SRI**, The normal address process decode takes 2 clock cycles. If the SRI clock frequency is 180 MHz or lower, then this bit can be set to reduce the decode time to 1 clock cycle.
- **FIFO_BYPASS**, a control bit for the data read mode for devices using an SDRAM protocol or DDR data transfer protocol. Under normal circumstances the read data from these devices is considered to be asynchronous and is resynchronised to the EBU clock using a data FIFO. If the external bus frequency is low enough, this bit can be set to load the data directly into the internal read buffers. This will remove one external bus clock from the access latency.

To make space for these, the four bit GLOBALCS field previously in MODCON has been made region specific and moved to individual **GLOBALCS** fields for each $\overline{CS}$ in **EBU_ADDRSELx (x = 0-3).**

Support for three new memory protocols has been added. All of these can be grouped under the heading DDR flash:

- LPDDR-NVM (JEDEC 42.4). This is a DDR memory protocol based on the PC100 SDRAM standard. Adding this protocol also allows the EBU to support DDRAM and SDRAM (where environmental conditions allow).
  - The following registers have been added to the EBU to allow configuration of the new protocol: **EBU_SDRMCON**; **EBU_SDRMOD**; **EBU_SDRMREF**; **EBU_SDRSTAT**; **EBU_DDRNCON**; **EBU_DDRNMOD**; **EBU_DDRNMOD2**; **EBU_DDRNSRR**; **EBU_DDRNPRLD** and **EBU_DDRNTAGx (x=0-3)**
  - The EBU will now also recognise values of 8_D (SDRAM), 10_D (LPDDR-NVM) and 12_D (DDRAM) as being valid for the **AGEN** fields in **EBU_BUSRCONx (x = 0-3)** and **EBU_BUSWCONx (x = 0-3)**
  - A new differential clock output (DDRCLKO & $\overline{DDRCLKO}$), new control signals ($\overline{RAS}$, $\overline{CAS}$, CKE), and data strobes (DQS[3:0]) have been added to the EBU pinout. The byte control signals (BC[3:0]) now have an alternate function as data modifiers (DQM[3:0]).
- Spansion 29DS032J. (1.8v I/O mode only) This is a hybrid device using a standard flash command protocol and DDR transfer of read data. Support for this device is configured using an **AGEN** value of 9_D.

- ONFI 2.0. DDR interface protocol for NAND flash memories. Support for this device type is configured using an **AGEN** value of 13_D. Adding this device has required the following changes to the EBU:
  - The **PORTW** field in **EBU_BUSRCONx (x = 0-3)** now takes 00_B as a valid value configuring an 8 bit device. This is valid for all values of **AGEN** except 8_D, 9_D, 10_D and 12_D.
  - NAND flash control signals ALE and CRE are now output on ADV and BAA respectively. This applies to **AGEN** value 2_D as well as 13_D.
  - The timing of the MR/$\overline{W}$ signal has been changed for accesses to memories configured using **AGEN** values 2_D and 13_D. For these accesses the timing of MR/$\overline{W}$ will follow the standard RD/$\overline{WR}$ signal.

Additional fields have also been added to the **EBU_USERCON** register to provide finer control of switching pins between EBU and GPIO functions. This will now allow individual high order address bits to be reallocated for GPIO if not required by attached memory devices and also address bits 15 down to 0 to be allocated for GPIO if all attached memories have multiplexed address and data connections.

15.5 EBU Interface Signals

The external EBU interface signals are listed in Table 15-1 below. In many case, the EBU pins have multiple functions depending on the memory devices configured and being accessed. In these cases, the primary designation of the pin is emphasised.

Table 15-1 EBU Interface Signals

Signal/Pin	Type	Function
AD[31:0]	O	Multiplexed Address/Data bus lines 0-31
A[27:0]	O	Address bus lines 0-27.
DQS[3:0]	I/O	data strobe lines for DDR devices. Can also be used as A[27:24] if DDR devices are not attached to the EBU. DQS[3]->A[24], DQS[2]->A[25], DQS[1]->A[26], DQS[0]->A[27]
A[27:24]	O	
$\overline{\text{CS}}$[3:0]	O	Chip select 0-3
$\overline{\text{CSCOMB}}$	O	Combined chip select for global select
$\overline{\text{RD}}$	O	Read control line
RD/$\overline{\text{WR}}$	O	Write control line
$\overline{\text{ADV}}$	O	Address valid output. Can be inverted for use as Address Latch Enable. Also used as ALE for NAND flash.
ALE	O	
$\overline{\text{BC}}$[3:0]	O	Byte control lines 3 to 0 Alternatively, these pins are used as Data Mask outputs when accessing JEDEC 42.4 LPDDR-NVM Memory, DDRAM orSDRAM
DQM[3:0]	O	
BFCLKO	O	Clock Output for Synchronous Accesses
BFCLKI	I	Feedback clock input for Synchronous Accesses
DDRCLKO	O	Clock Output for JEDEC 42.4 LPDDR-NVM Memory Accesses & DDRAM Memory Accesses. Alternately, SDRAM clock output.
SDCLKO	O	
$\overline{\text{DDRCLKO}}$	O	Negative phase of balanced DDRCLKO signal Alternatively, can also be used as the negative phase of BFCLKO if a DDR NOR flash memory is attached or the feedback Clock for SDCLKO.
SDCLKI	I	
$\overline{\text{BFCLKO}}$	O	
CKE	O	Clock Enable Output for JEDEC 42.4 LPDDR-NVM Memory, DDRAM and SDRAM
$\overline{\text{RAS}}$	O	Row Address Strobe for JEDEC 42.4 LPDDR-NVM Memory, DDRAM and SDRAM

Table 15-1 EBU Interface Signals (cont'd)

Signal/Pin	Type	Function
CAS	O	Column Address Strobe for JEDEC 42.4 LPDDR-NVM Memory, DDRAM and SDRAM
WAIT	I	Wait input
MR/W	O	Write Control line with timing suitable for Motorola Peripherals. ONFI 2.0 flash clock output
OCLKO	O	
BAA	O	Burst address advance output. Also Control Register Enable (CRE) for NAND flash accesses
CRE	O	
HOLD	I	Hold request input
HLDA	O	Hold acknowledge output
BREQ	O	Bus request output

15.5.1 Address/Data Bus, AD[31:0]

This bus transfers address and data information. The width of this bus is 32 bits. External devices with 8, 16 or 32 bits of data width can be connected to the data bus.

The EBU adjusts the data on the data bus to the width of the external device, according to the programmed parameters in its control registers. The byte control signals BC[3:0] specify which parts of the data bus carry valid data.

15.5.2 Address Bus, A[27:0]

The total address bus of the EBU consists of 24 address output lines, giving a directly addressable range of 64 Mbytes (2^{24}, 32 bit words). An external device can be selected via one of the chip select lines. Since there are four chip select lines, four such devices with up to 256 Mbytes of address range can be used in the external system.

15.5.3 Global Chip Select, CSCOMB

The EBU provides a combined or global chip select line. This can be programmed to be asserted with any combination of the normal chip selects CS[3:0]. See **Chapter 15.13.7** for more details.

15.5.4 Chip Selects, CS[3:0]

The EBU provides four chip select outputs, CS0, CS1, CS2 and CS3. The address ranges for which these chip selects are generated are programmed separately for each chip select line in a very flexible way via the address select registers EBU_ADDRSELx. More details are described on **Page 15-53**.

15.5.5 Read/Write Control Lines, $\overline{RD}$, RD/$\overline{WR}$

Two lines are provided to trigger the read ($\overline{RD}$) and write (RD/$\overline{WR}$) operations of external devices. While some read/write devices require both signals, there are devices with only one control input. The RD/$\overline{WR}$ line is then used for these devices. This line will go to an active-low level on a write, and will stay inactive high on a read. The external device should only evaluate this signal in conjunction with an active chip select. Thus, an active chip select in combination with a high level on the RD/$\overline{WR}$ line indicates a read access to this device.

15.5.6 Address Valid, $\overline{ADV}$

The address valid signal, $\overline{ADV}$, validates the address lines A[23:0] (and also the address placed on the data bus AD[31:0] when attaching multiplexed address/data devices). It can be used to latch these addresses externally. The polarity can be inverted to allow use as a positive logic Address Latch Enable signal (ALE).

It is also used as ALE when accessing NAND flash. In this case, the timing will be adjusted so that it is stable for the entire access.

15.5.7 Byte Controls, $\overline{BC[3:0]}$

The byte control signals $\overline{BC[3:0]}$ select the appropriate byte lanes of the data bus for both read and write accesses. **Table 15-2** shows the activation on access to a 16-bit or 8-bit external device. Please note that this scheme supports little-endian devices.

Table 15-2 Byte Control Pin Usage

Width of External Device	$\overline{BC3}$	$\overline{BC2}$	$\overline{BC1}$	$\overline{BC0}$
32-bit device with byte write capability	D[31:24]	D[23:16]	D[15:8]	D[7:0]
16-bit device with byte write capability	inactive (high)	inactive (high)	D[15:8]	D[7:0]
8-bit device	inactive (high)	inactive (high)	inactive (high)	D[7:0]

Signals BCx can be programmed for different timing. The available modes cover a wide range of external devices, such as RAM with separate byte write-enable signals, and RAM with separate byte chip select signals. This allows external devices to connect without any external “glue” logic.

Table 15-3 Byte Control Signal Timing Options

Mode	EBU_BUSCONx. BCGEN	Description
Chip Select Mode	00_B	$\overline{BCx}$ signals have the same timing as the generated chip select $\overline{CS}$.
Control Mode	01_B	$\overline{BCx}$ signals have the same timing as the generated control signals $\overline{RD}$ or RD/$\overline{WR}$.
Write Enable Mode	10_B	$\overline{BCx}$ signals have the same timing as the generated control signal RD/$\overline{WR}$.
DQM Mode	11_B	$\overline{BCx}$ signals are used as DQM for SDRAM/DDRAM.

15.5.8 Burst Flash Clock Output/Input, BFCLKO/$\overline{BFCLKO}$/BFCLKI

The flash clock output signal of the EBU is provided at pin BFCLKO. It is used for timing purposes (timing reference) during Burst Mode accesses. BFCLKO is, by default, only generated during synchronous accesses.

The clock input BFCLKI of the EBU is used to latch read data into the EBU. Normally BFCLKI is directly fedback and connected to BFCLKO. This feedback path can be configured externally to maximize the operating fiuency for a given Flash device or to compensate the BFCLKO clock pad delay. More details are given on **Page 15-91**.

DDR flash devices require a differential clock. If a DDR flash device is configured, then $\overline{BFCLKO}$ will be generated on the $\overline{DDRCLKO}$ pin.

15.5.9 Wait Input, $\overline{WAIT}$

This is an input signal to the EBU that is used to dynamically insert wait states into read or write data cycles controlled by the device on the external bus.

15.5.10 Burst Address Advance, $\overline{BAA}$

The Burst Address Advance output, $\overline{BAA}$, is provided for advancing the addresses during a Burst Flash read cycle. This signal is not asserted for burst flash writes.

This pin also functions as the Control Register Enable (CRE) for accesses to NAND flash.

15.5.11 Motorola Peripheral Write Signal, MR/$\overline{W}$

A write control signal held valid for the duration of an access (from chip select asserted to chip select negated).

15.5.12 ONFI 2.0 clock Output, OCLKO

The ONFI 2.0 devices require a clock input when working as a synchronous, DDR memory. The input pin on the device is also used as the write input, WR, when the device is operating in asynchronous mode. To enable the device to be successfully connected, a copy of the BFCLKO signal will be generated on the MR/W pin as OCLCKO when a region is configured for ONFI 2.0 memory.

15.5.13 DDR Clock Output/Input DDRCLKO/DDRCLKO/SDCLKI

The EBU provides a clock output for SDRAM devices on the SDCLKO pin. SDCLKO is, by default, a continuously running signal but can also be configured to switch off between accesses to conserve power.

The feedback clock input, SDCLKI, is used as a timing reference for the capture of read data on SDRAM accesses. It should be connected via a PCB trace to the clock pin of the SDRAM device.

For DDR devices a differential clock is required but the use of DQS lines to clock read data means that SDCLKI is not necessary. In this case, the negative phase clock, SDCLKO, is output on the SDCLKI pin.

If the combined clock mode is selected, SDCLKO will be output on the BFCLKO pin.

15.5.14 LPDDR-NVM, DDRAM, SDRAM Control Signals, CKE, CAS and RAS

These signals implement, along with the RD/WR signal, the command interface for an attached memory device using an PC100 SDRAM type control protocol.

15.5.15 DDR Data Strobes, DQS[3:0]

The DQS signals are used as clocks for data being transferred using DDR protocols. They are driven by the EBU on write accesses and by the attached memory device on read accesses.

15.5.16 Bus Arbitration Signals, HOLD, HLDA, and BREQ

The HOLD input signal is the external bus arbitration signal that indicates to the EBU when an external bus master requests to obtain ownership of the external bus.

The HLDA output signal is the external bus arbitration signal that indicates to a external bus master that it has obtained ownership of the external bus from the EBU.

The BREQ output signal is the external bus arbitration signal that is asserted by the EBU when it requests to obtain back the ownership of the external bus.

15.5.17 EBU Reset

The EBU is asynchronously initialised by the application reset.

15.5.17.1 Allocation of Unused Signals as GPIO

The EBU will allow pins not required for its programmed configuration to be allocated for use as GPIO. The signals required are as defined below:

Table 15-4 EBU Interface Signals Required by Operating Mode

Signal/Pin	When Needed by EBU
AD[15:0]	Always needed when the EBU is enabled. EBU_MODCON.ARBMODE != 00_B [1)]
$\overline{RD}$	
RD/$\overline{WR}$	
MR/$\overline{W}$	
$\overline{BC}$[1:0]	
A[18:16]	
$\overline{WAIT}$	This signal is required by the EBU when any enable region is configured to use WAIT by setting the BUSCONx.WAIT field to a value other than 00_B (EBU_MODCON.ARBMODE != 00_B) AND (EBU_ADDRSELx.REGENAB=1_B OR EBU_ADDRSELx.ALTENAB=1_B) AND (BUSRCONx.WAIT != 00_B)
A[27:19]	These address bits can be indvidually enabled for use as GPIO by setting the relevant enable bit in the USERCON register. Setting EBU_MODCON.ARBMODE = 00_B will also enable for GPIO. If DDR devices are connected, then the 4 MSBs of the address are used for DQS and will be enabled regardless of the state of the USERCON bits.
A[15:0]	These address bits are not required if the only devices connected have a multiplexed address/data bus. In this case they will be made available for GPIO if USERCON.ADDRLSW=1_B. Setting EBU_MODCON.ARBMODE = 00_B will also enable for GPIO.
$\overline{ADV}$	The ADV output can be made available for GPIO by setting the **ADVIO** bit in the USERCON register to 1_B. Setting EBU_MODCON.ARBMODE = 00_B will also enable for GPIO.

Table 15-4 EBU Interface Signals Required by Operating Mode (cont'd)

Signal/Pin	When Needed by EBU
BFCLKO BFCLKI $\overline{\text{BAA}}$	These signals are required by the EBU when the EBU is enabled and an enabled region is configured for burst device support (EBU_MODCON.ARBMODE != 00_B) AND (((EBU_ADDRSELx.REGENAB=1_B) OR (EBU_ADDRSELx.ALTENAB=1_B) OR (BUSRCONx.BFCMSEL=0_B)) AND (BUSCONx.AGEN = 1_H OR 3_H OR 6_H OR 5_H OR 7_H OR 9_H OR B_H)) OR (MODCON.CLKCOMB = 1_B))
$\overline{\text{RAS}}$ $\overline{\text{CAS}}$ CKE DDRCLKO $\overline{\text{DDRCLKO}}$	These signals are required by the EBU when the EBU is enabled and an enabled region is configured for SDRAM, DDRAM or LPDDR-NVM support. (DDRCLKO is also required if DDR burst flash is connected and will additionally be enabled in this case) (EBU_MODCON.ARBMODE != 00_B) AND ((EBU_ADDRSELx.REGENAB=1_B OR EBU_ADDRSELx.ALTENAB=1_B) AND (BUSRCONx.AGEN = 8_D OR 10_D OR 12_D)
$\overline{\text{HOLD}}$ $\overline{\text{BREQ}}$ $\overline{\text{HLDA}}$	These signals are required by the EBU when the EBU is configured to arbitrate for the external bus. e.g. EBU_MODCON.ARBMODE = 01_B or 10_B
AD[31:16] DQS[3:2] $\overline{\text{BC}}$[3:2]	These signals are required by the EBU when the EBU is enabled and an enabled region is configured for accessing 32 bit memory (EBU_MODCON.ARBMODE != 00_B) AND ((EBU_ADDRSELx.REGENAB=1_B OR EBU_ADDRSELx.ALTENAB=1_B) AND (BUSRCONx.PORTW = 10_B or 11_B)
$\overline{\text{CS}}$[3:0]	The Chip select lines are individually controlled and will be required for EBU operation when the associated memory region is enabled. (EBU_MODCON.ARBMODE != 00_B) AND (EBU_ADDRSELx.REGENAB=1_B OR EBU_ADDRSELx.ALTENAB=1_B)
$\overline{\text{CSCOMB}}$	The Global Chip Select line is required by the EBU when any EBU_ADDRSEL.**GLOBALCS** != 0_B and the EBU is enabled (EBU_MODCON.ARBMODE != 00_B)

1) If the EBU is disabled by writing 00 to the EBUCON.ARBMODE field, there will be a delay before the signals become available for GPIO usage as the EBU will wait for all pending external memory accesses to be completed and the arbitration logic to return to the "nobus" state before releasing the signals.

15.6 Bus State During Reset

The state of the various bus signals is controlled by Memory Controller during reset as follows:-

Table 15-5 Memory Controller External Bus pin states during reset

Pin Name	State during Reset[1)]	State during Idle[2)]	State during "no bus" mode
AD(31:16)	GPIO	High Impedance - pull ups enabled to pull to '1'.	GPIO
AD(15:0)	High impedance pull to '1' (high).	High Impedance - pull ups enabled to pull to '1'.	High Impedance - pull ups enabled to pull to '1' (High).
A(27:19)	GPIO	Driven to '0' after reset, otherwise last used address	GPIO
A(19:0)	High impedance pull to '1' (high).	Driven to '1' (High) at reset, last used address when idle	High impedance pull to '1' (high).
$\overline{CS}$(0)	High impedance pull to '1' (high).	Driven to '1' (High).	High impedance pull to '1' (high).
$\overline{CS}$(3:1)	GPIO	Driven to '1' (High).	GPIO
$\overline{RD}$	High impedance pull to '1' (high).	Driven to '1' (High).	High impedance pull to '1' (high).
$\overline{WR}$	High impedance pull to '1' (high).	Driven to '1' (High).	High impedance pull to '1' (high).
$\overline{CAS}$	GPIO	Driven to '1' (High).	GPIO
$\overline{RAS}$	GPIO	Driven to '1' (High).	GPIO
CKE	GPIO	Dependant on SDRAM clocking/power save mode	GPIO
$\overline{ADV}$	GPIO	Driven to '1' (High).	GPIO
DDRCLKO	GPIO	Driven to '0' (Low).	GPIO

Table 15-5 Memory Controller External Bus pin states during reset (cont'd)

Pin Name	State during Reset[1)]	State during Idle[2)]	State during "no bus" mode
$\overline{\text{DDRCLKO}}$	GPIO	High Impedance	GPIO
BFCLKI	GPIO	High Impedance	GPIO
BFCLKO	GPIO	Driven to '0' (Low).	GPIO
$\overline{\text{BC}}$(3:2)	GPIO	Driven to '1' (High).	GPIO
$\overline{\text{BC}}$(1:0)	High impedance pull to '1' (high).	Driven to '1' (High).	High impedance pull to '1' (high).
$\overline{\text{WAIT}}$	GPIO	Always an input (must have a pull-resistor to inactive state).	GPIO
$\overline{\text{CSCOMB}}$	GPIO	Driven to '1' (High).	GPIO
$\overline{\text{HOLD}}$	GPIO	depends on state of bus arbitration logic	GPIO
$\overline{\text{HLDA}}$	GPIO		GPIO
$\overline{\text{BREQ}}$	GPIO		GPIO
MR/$\overline{\text{W}}$	GPIO	Driven to '1' (High).	GPIO
$\overline{\text{BAA}}$	GPIO	Driven to '1' (High).	GPIO

1) GPIO controlled pins should be high impedance with pull up during reset.

2) Assuming that the pins have not been made available as GPIO.

Applicable reset is cgu_con_clk_rst_n_i.

15.7 Memory Controller Structure

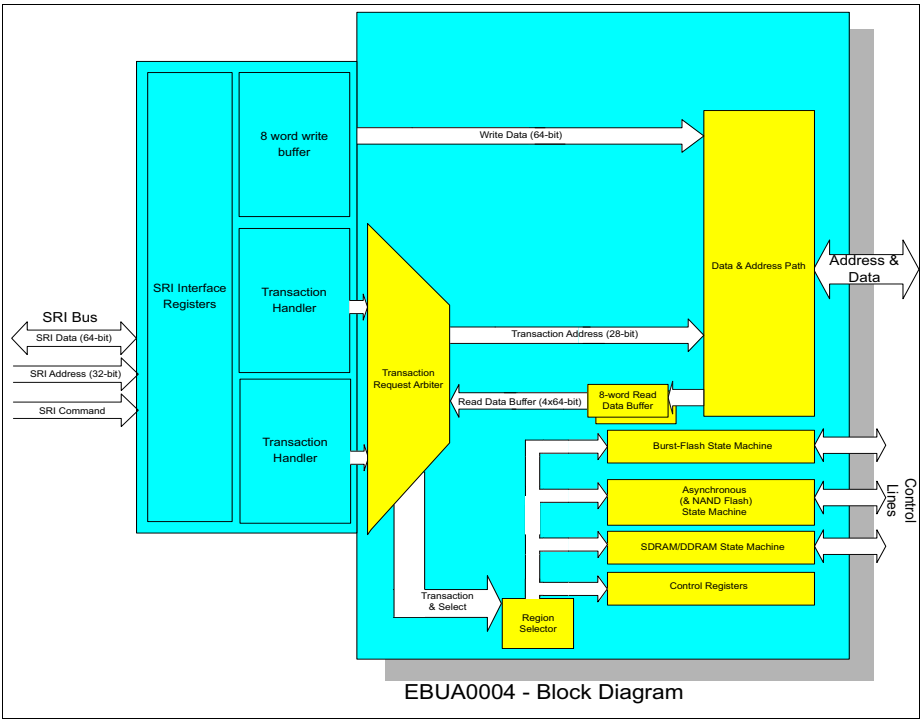


Figure 15-3 Memory Controller Block Diagram

The SRI interface translates SRI transactions from the ports into appropriate transaction requests which can be transferred to the arbiter. The interface can handle two transactions simultaneously as required by the SRI protocol which has a two deep, command pipeline. The interface will also generate an ECC code for all read data returned and will check ECC codes received along with each SRI transaction. In the event of a transaction failing the ECC check, an error will be flagged to the system for further processing and the transaction will be terminated with an SRI error.

The arbiter looks at the transaction requests and schedules corresponding requests to the relevant state machine. Only one state machine can be active at any time and the arbiter is designed to prevent out-of-order execution. The dedicated state machines are used to sequence control signals and to co-ordinate accesses to each of the different external memory/device types and also the internal registers.

If two consecutive accesses are to the same state machine, the second access will be queued before the first has completed. This allows accesses to run “back-to-back” on the external bus and maximises bandwidth utilisation.

15.8 Memory Controller Read Architecture

The memory controller contains two, identical read buffers each with a capacity of 4, 64 bit words. A read access will be allowed to proceed if one of the buffers is flagged as available. The data read from the external memory will be stored in the read buffer and the outputs from the read buffer will be multiplexed to the SRI port. Once the SRI port signals that all data has been returned to the requesting SRI master, the read buffer will again be flagged as available.

This architecture allows reads to be in progress simultaneously, as a second read can be running while the first read is still waiting for data to be returned to the SRI master.

15.9 Access Arbitration

Arbitration of SRI accesses is handled by the SRI matrix. The EBU will only ensure that accesses are processed in the order that they arrive at the SRI port

15.9.1 Programming Sequence Locking

Programming sequences for some Burst Flash devices require that the source of the programming transactions has exclusive access to the external memory device for the duration of the write sequence. If such devices are used and can be accessed by multiple transaction sources then the “Locked Programming Sequence” feature can be enabled via register bit EBU_BUSWCONx.LOCKCS.

A programming sequence is considered to start when the processor data port carries out an initial write transaction.

Note: It has been assumed that the processor data port is the only port that will ever attempt programming operations to a NOR flash.

A programming sequence is considered to have ended when the processor data port carries out a subsequent read transaction to a CS which it has locked, or when the processor data port, which has locked CSx, carries out a write to CSy resulting in the locking of CSy, or when an internal fail-safe timeout expires.

A programming sequence lock is aborted if an access is attempted from the processor instruction port to the locked device. An aborted sequence will be flagged by the status bit. LCKABRT, in the EBU_MODCON register. This flag will be cleared by writing 1_B to the LCKABRT field.

Note: This is to prevent a system livelock in the event that the code running the programming sequence is interrupted.

If programming sequence locking is enabled for $\overline{CSx}$, then once a write transaction to $\overline{CSx}$ is accepted from the processor data port, the SRI interface automatically “locks” ownership of the device on $\overline{CSx}$ to that port. Any transaction requests (read or write) to the same $\overline{CSx}$ from other transaction sources wil be errored until the end of the

programming sequence. Accesses to other $\overline{CS}$y or $\overline{CS}$z devices from the other initiators will be permitted.

Sequence “locking” takes place in the SRI interface block.

The fail-safe timeout timer defaults to a count of 255 and is decremented at a frequency of EBU_CLK/16. It commences counting from the preload value every time a write completes. The default value can be changed by writing to the EBU_BUSCON.LOCKTIMEOUT register field.

15.9.2 Source Access Inhibit

Transactions not initiated by the processor can be temporarily denied access to external memory by setting the EBU_MODCON.access_inh bit. This is to allow reprogramming of access parameters for external memory by the processor while preventing the other potential masters from attempting to access with invalid settings. While this bit is set accesses which do not originate from one of the processor ports will be errored. Port Access Inhibit will be enabled after reset.

Note: If a DLL relock is trigged while access inhibit is active, then access inhibit should not be removed until a DLL relock has completed.

15.10 Clocking Strategy and Local Clock Generation

The Memory Controller can be configured to operate from several possible clock sources. The clock generation logic is used to select between these clock sources and generate the internal clock used for the memory controller, EBU_CLK.

15.10.1 Clocking Modes

The bridges can be operated in one of two modes using one of two clocks:-

- Asynchronous mode: The SRI clock and Memory Controller internal clock (EBU_CLK) are assumed to be asynchronous. EBU_CLK is derived from the Flexray PLL output.
- Synchronous mode: The EBU_CLK is derived from the controller (SRI) clock. The EBU_CLK and SRI interface clocks have aligned edges (although pulse swallowing can be used on the EBU_CLK clock, so that the EBU core can run at a lower frequency than the SRI bus matrix).
- Synchronous or Asynchronous mode at half of SRI clock: The EBU clock is running at half the frequency of the processor clock. The EBU clock is edge aligned with the processor and SRI interface clocks.

The clock for the SRI interface of the memory controller, is always be derived from the same synchronous source (the processor clock, .

Operation of the bridge in Asynchronous mode provides maximum flexibility in clocking different domains at different frequencies. This is, however, at the cost of additional latency (for signal resynchronisation) through the bridge.

Operation of the bridge in synchronous mode minimises the latency through the bridge at the cost of forcing the SRI and EBU_CLK domains to run from the same source clock (the processor clock).

The mode of operation of the bridge is controlled by the **EBU_CLC.SYNC** register field. The **EBU_CLC.SYNCACK** field will be updated to report the current operating mode.

The **EBU_CLC.SYNC** register field can be used (dynamically) to switch between these two modes. The Memory Controller contains internal control logic to sequence the switching between modes to ensure that external bus accesses are not corrupted as a result of switching clocking modes. The Memory Controller updates the **EBU_CLC.SYNCACK** to signal the status of the bridge (‘1’ = operating in Synchronous Mode, ‘0’ = operating in Asynchronous Mode).

If **EBU_CLC.DIV2** is set to 0_B, then **EBU_CLC.SYNC** also controls the clock input and switches it between the processor clock and the Flexray PLL output.

However, if **EBU_CLC.DIV2** is set to 1_B, then EBU clock source is forced to be half the frequency of the processor clock and **EBU_CLC.SYNC** only enables and disables the resynchronisation stages necessary for asynchronous operation. Setting **EBU_CLC.SYNC** to 0_B will only activate the resynchronisation stages, the EBU clock will remain fixed at half the processor clock frequency . The value of **DIV2** in use by the memory controller is stored in the **EBU_CLC.DIV2ACK** field.

15.10.2 Local Clock Divider

A local divider can be used to reduce the frequency of EBU_CLK. The divider can be programmed to for divide ratios of 1:1, 2:1, 3:1 or 4:1 using the **EBU_CLC.EBUDIV** register field. The ratio currently in use is provided in the **EBU_CLC.EBUDIVACK** register field.

The purposes of the divider is to allow the memory controller core to operate synchronously at an integer divide ratio of the SRI clock.

By also setting the **EBU_CLC.DIV2** bitfield, the available divide ratios between the SRI clock and the EBU_CLK become 1:2, 1:4, 1:6 and 1:8

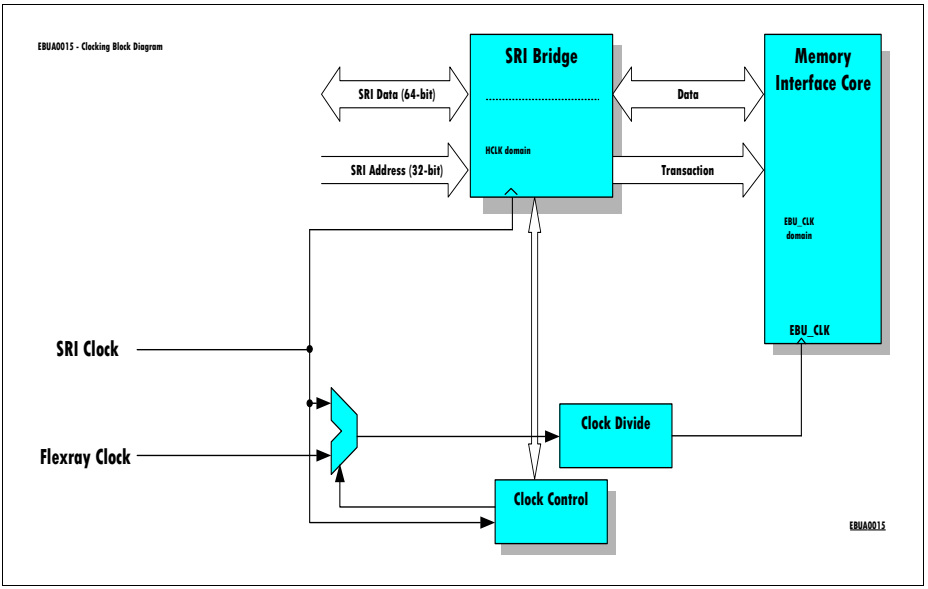


Figure 15-4 SRI/Memory Controller Clock Domains

If a divide ratio of 1:3 is selected using the local clock divider and a memory device is being used at a 1:1 or 1:3 external clock ratio, then the device clock outputs, BFCLKO and SDCLKO, will not have a 50% duty cycle unless the DLL is used to correct the duty cycle. This is because the local divider operates by pulse swallowing the module input clock to generate EBU_CLK.

For all clock ratios other than 1:3 the negative phase clock can be generated using a shifted pulse swallowing control signal but accurate positioning of the negative edge of a 1:3 clock is not possible.[1)]

1) All clock duty cycle ratios are nominal and will be affected by PLL jitter and pad rise/fall asymmetry

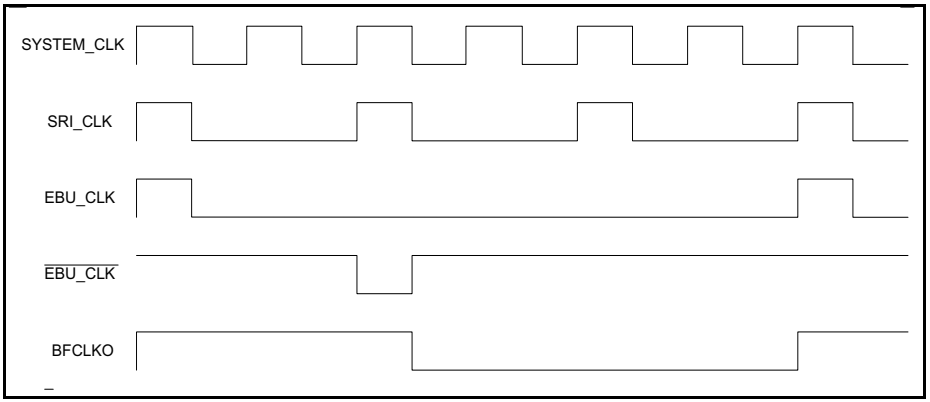


Figure 15-5 Example of BFCLKO Generation using 1:3 case

The figure above shows an example of external bus clock generation.

- Firstly, the system clock is divided to generate the SRI clock
- Then the EBU local clock divider divides the SRI clock to generate the EBU internal clock
- An $\overline{\text{EBU\_CLK}}$ signal is also generated from the SRI clock by shifting the pulse swallowing control signal and inverting the signal if required
  - For 1:1 division, there is no phase shift and the clock is inverted only
  - For 1:2 division, the phase shift is one period of the SRI clock and there is no inversion
  - For 1:3 division, the phase shift is one period of the SRI clock and the signal is inverted
  - For 1:4 division, the phase shift is two periods of the SRI clock and there is no inversion.
  - For 1:6 division, the phase shift is three periods of the SRI clock and there is no inversion.
  - For 1:8 division, the phase shift is four periods of the SRI clock and there is no inversion.
- The inverted clock signal is used to position the negative edge of the external bus clock in 1:1 EBU_CLK:BFCLKO mode (BUSCONx.**EXTCLOCK**=00_B) and also the edges of control signals shifted by one half of an EBU_CLK period (See **Chapter 15.16.4** and **Chapter 15.17.8**).

15.10.3 Standby Mode

The Memory Controller can be configured to disable its internal clock and enter standby mode by writing a logic ‘1’ to the **EBU_CLC.DISR** register field.

Once the register field is written, the Memory Controller will wait for any running accesses to finish and will then disable the clock to the core logic of the Memory Controller (EBU_CLK). As this will also disable the refresh counters, it is necessary to set the **EBU_SDRMREF.AUTOSELFR** register field if this mode is to be used with SDRAM. This will instruct the MEMCTRL to place any attached SDRAM into self refresh mode before allowing clock mode switching or standby.

Exit from standby mode is triggered by writing 0_B to the **EBU_CLC.DISR** field

An access arriving on any of the Memory Controller, SRI interfaces will trigger an automatic exit from standby mode to service the access request. This condition may also prevent standby mode being entered at all depending upon when the new access arrives at the SRI interface

Note: Once a pending SRI access has triggered an exit from standby mode, if all pending SRI accesses have been serviced and the standby request is still active, the memory controller will not return to standby mode.

An automatic exit from standby mode will not clear the **EBU_CLC.DISR** field. If automatic exit is used, then the **EBU_CLC.DISR** field will have to be cleared by an explicit write of 0_B before standby mode can be used again.

15.10.4 DLL Operation

The DLL is required for the following reasons:

- It is used to delay the DQS signals from the external DDR memory and enable read data to be successfully transferred between the DDR SDRAM and the memory controller. This is enabled by setting **EBU_DLLCON.RD_EN** to 1_B.
- It is used to delay the write data output from the memory controller to the DDR memory device and enable the correct relationship between the DQ, DQM and DQS lines to be estabilised when the external bus clock is running at the same frequency as EBU_CLK. (For signal timing with other clock ratios see **"Generation of DDR Control Signals without using the DLL" on Page 15-24**). This is enabled by setting **EBU_DLLCON.WR_EN** to 1_B.
- It is used to adjust the duty cycle of the clocks to external memory to the optimum 50% when the ratio between internal and external clock is 1:1. This is enabled by setting **EBU_DLLCON.DCC_EN** to 1_B

The calibrated delay value used by the slave delay lines will only be updated when it is safe to do so.

- The delays affecting write data (DQ and DQM) will only be updated when a DDR write is not taking place
- The delays affecting the DQS inputs will only be updated when a DDR read is not taking place
- The delays used to compensate the duty cycle will be continuously updated but using a clocking signal that is phase shifted so that glitches cannot occur on the output.

15.10.4.1 Locking the DLL

Once enabled by setting **EBU_DLLCON.DLL_DIS** to 0_B, the DLL can be initialised by writing 1_B to **EBU_DLLCON.DLL_RST**. This will trigger the DLL to lock to the current DDR clock frequency. If the EBU_CLK frequency is modified, then this field should be rewritten to lock the DLL to the new frequency.

A status bit is provided, **EBU_DLLCON.DLL_LCK**. This will be set when The DLL successfully locks to the current EBU_CLK frequency.

It will be cleared after reset and when either

- 1_B is written to **EBU_DLLCON.DLL_RST**
- The DLL loses lock with EBU_CLK.

Once initial lock has been achieved, the DLL will continually update its lock point. This behaviour will be inhibited when **EBU_DLLCON.DLL_DIS** is set to logic one.

The DLL will only flag "loss of lock" by setting **EBU_DLLCON.DLL_LCK** to 0_B if the input frequency is sufficiently low that the master delay line has too few delay line elements to enable a lock point to be achieved. In all other cases, the delay line will attempt to track the input frequency. If the input frequency is changed using the CGU control logic, signal positioning will be incorrect while the delay line tries to relock. However the lock signal will remain set unless the new frequency is out of range. For this reason, it is recommended that frequency changes are always performed using the clock source control logic. See **“Clocking Modes” on Page 15-16**.

After reset, the DLL will be disabled with **EBU_DLLCON.DLL_DIS** set to logic ’1’.

The DLL has two possible locking algorithms selected by the **EBU_DLLCON.ALGO** bit. when set to 0_B, the DLL will use a fast locking algorithm to rapidly scan the delay setting using intervals of four delay cells from zero to just past the lock point. It will then adjust the delay back down incrementally until the lock point is reached.

If **EBU_DLLCON.ALGO** is set to 1, the DLL will use a slow locking algorithm where the delay is scanned using increments of one delay cell until the lock point is passed. This mode has a lesser risk of spurious errors if the clock period is sufficiently small that the four delay cell increments of the fast locking mode are a significant proportion of the clock period.

15.10.4.2 DLL Operating Modes

The DLL is only designed to lock at frequencies between 80 MHz and 180 MHz. At lower frequencies, the DLL can be operated unlocked with a a static delay programmed by the **EBU_DLLCON.DLL_VALUE** register field.

In this mode, ’1’ should be written to **EBU_DLLCON.DLL_DIS**. This will prevent the DLL from trying to lock. The DLL value will then remain at the value written to the **EBU_DLLCON.DLL_VALUE** register field (permitted values 0 to 425).

This preprogrammed value should therefore provide sufficient margin between clock and delayed DQS edges for the interface to operate.

Note: Each delay element should have a delay of between 35ps and 120ps depending on the operating conditions of the device.

*Note: The master delay line can add 425 delay elements to the input clock and the logic is therefore designed to cope with a master delay line output of 0 to 425. Writing a larger value than 425_D to **EBU_DLLCON.DLL_VALUE** when **EBU_DLLCON.DLL_DIS** is set will cause arithmetic overflows in the slave delay elements and cause the delayed signals to be disabled*

15.10.4.3 DLL Related Access Error Conditions

Accesses to DDR memory will return an SRI error if:

- **EBU_DLLCON.DLL_LCK** is 0_B and
- **EBU_DLLCON.DLL_DIS** is 0_B and
- **EBU_DLLCON.WR_EN** is 1_B or **EBU_DLLCON.RD_EN** is 1_B

Accesses to any external memory will return an error if:

- **EBU_DLLCON.DLL_LCK** is 0_B and
- **EBU_DLLCON.DLL_DIS** is 0_B and
- **EBU_DLLCON.DCC_EN** is 1_B

15.10.4.4 DQ and DQM Outputs (EBU_DLLCON.WR_EN=1_B)

The DQ and DQM outputs will be delayed by 25% of a clock cycle. There will be two delay elements adjusting the clocks of the flipflops driving the DQ and DQM outputs (one for positive edge and one for negative edge). The optimum value can be adjusted manually by up to +3/64 and -4/64 of a clock cycle by writing the appropriate signed value to the **EBU_DLLCON.WR_D_ADJ** register field[1)].

The delay lines will only be allowed to update when a write is not in progress.

15.10.4.5 DQS Inputs (EBU_DLLCON.RD_EN=1_B)

The DQS inputs will be individually delayed by 25% of a clock period (EBU_CLK) before being used as the capture clock for the read data (one delay per byte lane). The optimum value can be adjusted manually by up to +3/64 and -4/64 of a clock cycle by writing the appropriate signed value to the **EBU_DLLCON.RD_DQS_ADJ** register field1).

The setpoint of the delay lines can only be updated when a read is not in progress. This is not a problem for DDR devices using the synchronous state machine where the device protocols enforce a gap on the databus between “back-to-back” reads but can be an

1) The field allows for a signed number with a value between -4 and +3..

issue for devices using the SDRAM state machine where reads can be aggressively pipelined. See **Chapter 15.19** and **Chapter 15.20** for more information on managing updates of the slave delay lines.

15.10.4.6 Duty Cycle Correction

The negative clock edge is used to clock the flipflops used to generate the negative edge of the external memory clocks when 1:1 clock ratio is selected. It also clocks the flipflops generating those control signals generated on the negative edge of the internal clock. If EBU_CLK does not have a 50% duty cycle then the edges will deviate for the nominal position.

The duty cycle correction delay is used to compensate for the duty cycle distortion caused by the pulse swallowing circuit used to locally divide the input clock to generate EBU_CLK. A delay line with a nominal value of 50% of clock period is used to generate a clock edge at the same position in the clock cycle as the negative edge of a 50% duty cycle clock of the same period.

If duty cycle correction is disabled by setting the **EBU_DLLCON.DCC_EN** register bit to 0_B, the negative edge flipflops are connected directly to an anti-phase version of the EBU_CLK clock signal. See **"Local Clock Divider" on Page 15-17** for information on how this anti-phase clock is generated.

Note: This is intended to allow the correct generation of the external interface signals at lower frequencies of the memory controller input clock (outside the DLL lock range) when the duty cycle is 50% and the local clock division circuit is set to 1:1.

15.10.5 DLL Drift detector

The DLL contains a modified phase detector with an expanded detection window intended to detect when the drift rate of the locking point has exceeded the tracking limit of the DLL.

This circuit is enabled when the following conditions are true:

- The DLL has achieved lock.
- 1_B is written to the **EBU_DLLCON.WIN_EN** bitfield.

Once enabled the drift detector will monitor the phase of the DLL input and output clocks. If the phase variation of the input and output clocks exceeds the window of the detector, all accesses to DDR memory will be stalled by the EBU and the **EBU_SDRSTAT.DRIFT_WARN** bitfield will be set to 1_B. Once the drift detector registers that the phase variation has decreased to within the window, the stalled accesses will be allowed to proceed. **EBU_SDRSTAT.DRIFT_WARN** will not clear until written with 0_B.

The size of the window is set to be ±6 delay elements.

The principle of operation is that the error on the lockpoint should never exceed one delay element if the DLL control logic can keep up with the current rate of drift.

If this feature is to be relied on to prevent data corruption, it must be ensured that the operating frequency of the DDR interface is limited so that the worst case signal positioning error does not cause a timing violation.

15.10.6 Generation of DDR Control Signals without using the DLL

The previous section covered the principles of using the DLL to generate the correct signal timing for DDR signals when the internal to external clock ratio is 1:1.

If the ratio of the internal to external clocks is not 1:1, then the internal clock is used to generate the necessary signal timing for outputs without the use of the DLL. For this to work correctly, the shifting of write DQ and DQM by the DLL must be disabled (**EBU_DLLCON.WR_EN** must be 0_B)

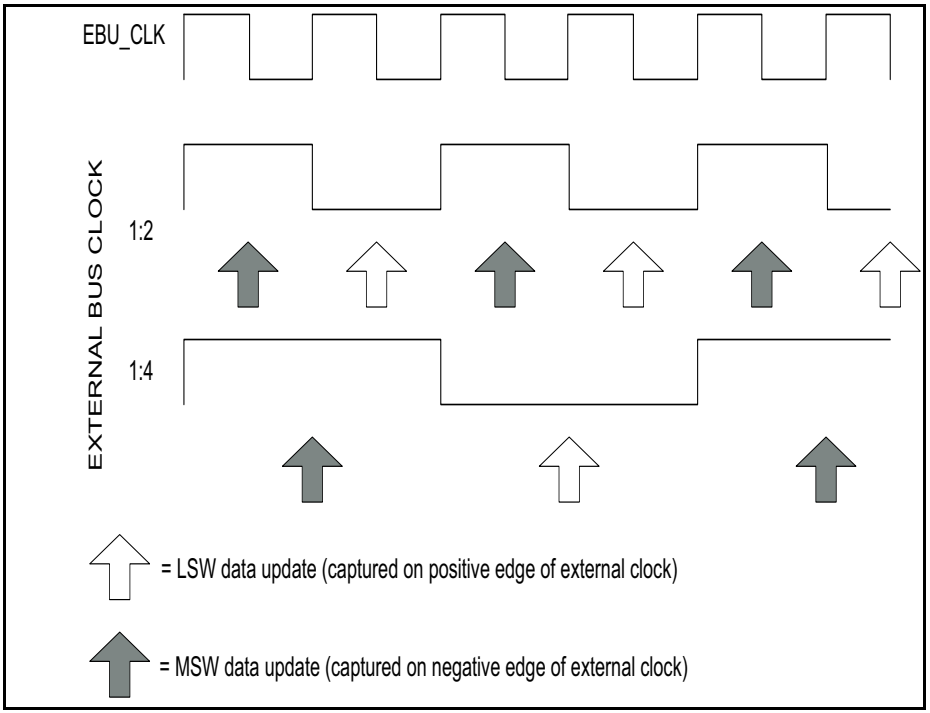


Figure 15-6 Write Data Update Points

15.10.7 Read Data Capture for DDR Devices

The EBU has two possible methods of capturing the data read from DDR devices:

15.10.7.1 Read Data FIFO

The read data FIFO is clocked by the DQS signals generated by the DDR memory device. As the memory device will generate DQS edges aligned with data changes, the DQS signals have to be phase shifted using the delay lines to guarantee safe capture of the data. See **"DQS Inputs (EBU_DLLCON.RD_EN=1B)" on Page 15-22** for the method used to generate a fixed delay of 25% of an EBU_CLK period (nominal). This method can be used at any setting of the EBU_CLK to external clock ratio provided that 25% of an EBU_CLK period provides sufficient setup time to successfully capture the data.

If the DLL is not locked, then a fixed delay value can be written into **EBU_DLLCON.DLL_VALUE**. This will insert a fixed number of delay cells into the DQS input path (**DLL_VALUE**/4). As there is no feedback mechanism in this mode to compensate for changes in operating conditions, the value of the delay inserted will vary as voltage and temperature of the device changes.

This method treats the DQS inputs as asynchronous clocks and the data is resynchronised to EBU_CLK.

15.10.7.2 FIFO Bypass Mode

At lower frequencies it is possible to capture the read data from DDR memories without using the data FIFO to resynchronise it to the internal clock domain. This allows DDR memories to be accessed without requiring the DLL. For this mode to work correctly, the following constraints must be met:

- The rising edge of the feedback clock must be guaranteed not to coincide with the rising edge of the internal clock. For the TC1798, this is possible up to a maximum external bus frequency frequency of 45 MHz.
- The external bus frequency must be sufficiently low to allow the DQS & DQ to be generated from one clock edge and reach a stable state before the next clock edge.
- The first DQS/DQ transition must be triggered by a rising clock edge
- Once the first DQS/DQ transition has occurred all clock edges must trigger a DQS/DQ transition until the access completes.

In this mode $\overline{\text{DDRCLKO}}$ will be used as the feedback clock and both edges of the feedback clock will be used to register DQ (data) and DQS lines from the memory. A change in state of the DQS will cause the sampled data to be transferred into the read FIFO.

FIFO bypass mode is enabled by writing 1_B to the **EBU_MODCON.FIFO_BYPASS** bitfield.

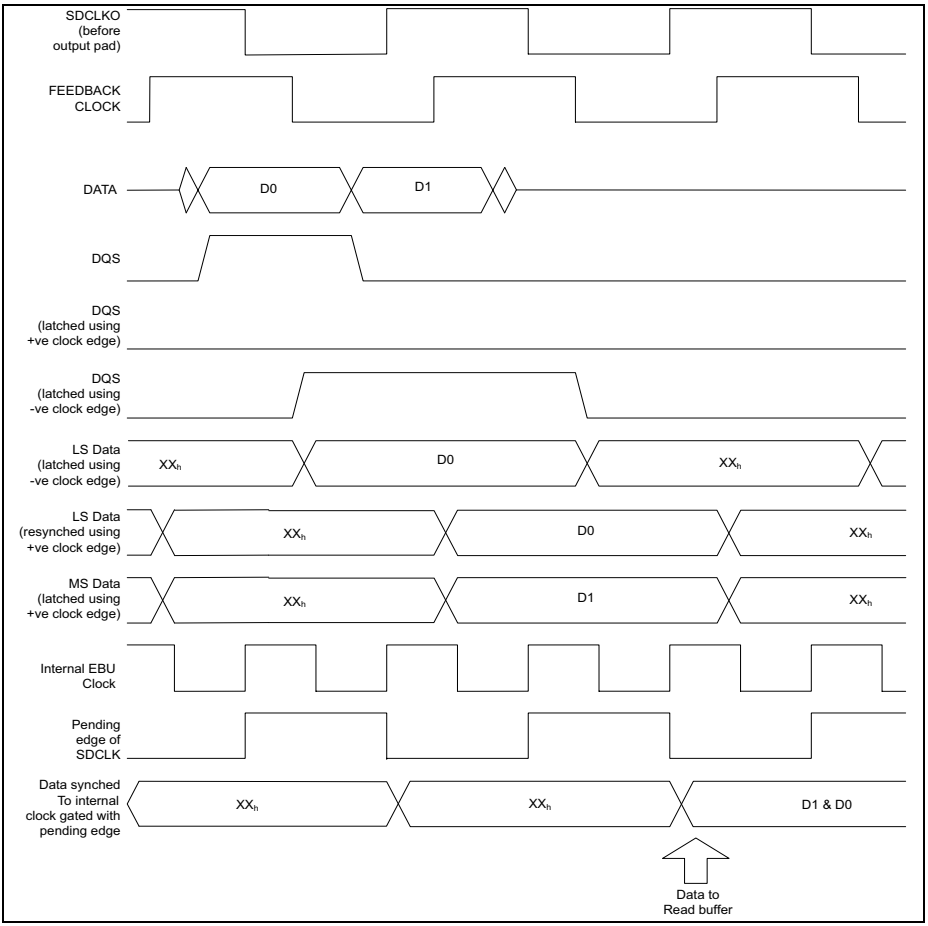


Figure 15-7 Data Read Timing for Accesses bypassing the FIFO

15.10.8 External Bus Clock Generation

The memory controller can generate two external bus clocks.

One of these is intended for use with SDRAM/DDRAM type devices controlled by the SDRAM state machine[1)] and is output on DDRCLKO (and $\overline{\text{DDRCLKO}}$ if a differential clock is required). See **"SDRAM External Bus Clock Generation" on Page 15-117**

1) See **"Programmable Device Types" on Page 15-54** for the device types supported by the EBU and the state machines used to control them

The other is intended for use with other synchronous memories such as burst flash and is output on BFCLKO (and DDRCLKO if a differential clock is required). See **"Burst Flash Clock" on Page 15-91**

For devices without DQS outputs, clock feedback is used to correct for pad output and PCB track delays and each clock output therefore has an equivalent clock input. These are SDCLKI (DDRCLKO alternate function) and BFCLKI respectively. If a device does have DQS outputs, these are used to time read data capture (for the only exception see **"FIFO Bypass Mode" on Page 15-25**).

If a DDR memory is attached to the EBU, it will normally require a differential clock. For devices using the SDRAM control state machine this is DDRCLK & DDRCLK. For devices using the burst flash control state machine, the differential clock will be BFCLKO and DDRCLK.

The clocking mode will be determined by the **AGEN** fields of the configured memory regions.

- If any region is configured for LPDDR NVM (**AGEN** = 10_D) or DDRAM (**AGEN** = 12_D), then the differential DDRCLK will be output on DDRCLK and DDRCLK.
- If any region is configured for DDR burst flash (**AGEN** = 9_D) or ONFI 2 DDR flash (**AGEN** = 13_D), the differential DDRCLK will be output on BFCLKO and DDRCLK.
- Configuring both of the above conditions will force the DDRCLK and BFCLKO outputs to use identical settings, In this case both regions must be configured with identical **EXTCLOCK** and **SDCMSEL**/**BFCMSEL** settings. If this is not done, the the EBU contains logic which will try and configure sensible clock settings as follows:
  - the frequency of the output clock will be set by the **EXTCLOCK** setting of the highest priority region configured for DDR memory[1].
  - BFCLKO and SDCLKO will both output the positive phase of DDRCLK
  - If an enabled region configured as DDR burst flash has **BFCMSEL** set to 0_B or an enabled region is configured for DDRAM or LPDDR NVM with **SDCMSEL** set to 0_B then the clock will run continuously at the frequency specified by the **EXTCLOCK** setting of that region.
  - Clock feedback for both memory types (if required) will be taken from the SDCLKI pin.
- Setting the **CLK_COMB** bit in the **EBU_MODCON** register will have an identical effect to configuring both types of DDR memory. This is not dependent on having any DDR memory configured. (e.g. this could be used to run SDRAM off the BFCLKO clock output.)

Note: All attached DDR memories use the same DQS signals and read/write datapaths. Due to the practical difficulties of dynamically switching the clock frequency of a DDR interface, this effectively forces all DDR devices attached to the EBU to be run at the same clock frequency.

1) region 0 has the highest priority and region 3 the lowest

15.11 External Bus Arbitration

External bus arbitration is provided to allow the EBU to share its external bus with other master devices. This capability allows other external master devices to obtain ownership of the external bus, and to use the bus to access external devices connected to this bus. The scheme provided by the EBU is compatible with other TriCore and XC2XXX devices and therefore allows the use of such devices as (external bus) masters together with the TC1798.

*Note: In this section, the term "external master" is used to denote a device which is located on the **external** bus and is capable of generating accesses across the external bus (i.e. is capable of driving the external bus). An external master is not able to access units that are located inside the TC1798.*

15.11.1 External Bus Modes

The EBU can be in one of two bus states on the external bus:

- Owner State
- Hold State

When in Owner State, the EBU operates as the master of the external bus. In other words, the EBU drives the external bus as required in order to access devices located on the external bus. While the EBU is in Owner State it is not possible for any other master to perform any accesses on the external bus. When the EBU is in Owner State, **EBU_MODCON.BUSSTATE** is set to 1_B.

In Hold State, the EBU tri-states the appropriate signal on the external bus in order to allow another external bus master to perform accesses on the external bus (i.e. to allow another master to drive the various external bus signals without contention with EBU). When the EBU is in Hold State, **EBU_MODCON.BUSSTATE** is set to 0_B.

15.11.2 Arbitration Signals and Parameters

The arbitration scheme consists of an external bus master that is responsible for controlling the allocation of the external bus. This master is referred to as the "Arbiter" within this document. The other external bus master (termed Participant within this document) requests ownership of the bus, and when necessary, from the Arbiter. The EBU can be programmed to operate either as an Arbiter or as a Participant (see **Page 15-30**). The following three lines are used by the EBU to arbitrate the external bus.

Table 15-6 EBU External Bus Arbitration Signals

Signal	Direction	Function
$\overline{\text{HOLD}}$	In	$\overline{\text{HOLD}}$ is asserted (low) by an external bus master when the external bus master requests to obtain ownership of the external bus from the EBU.
$\overline{\text{HLDA}}$	In/Out[1)]	$\overline{\text{HLDA}}$ is asserted (low) by the Arbiter to signal that the external bus is available for use by the Participant (i.e. the bus is not being used by the Arbiter). $\overline{\text{HLDA}}$ is sampled by the Participant to detect when it may use the external bus.
$\overline{\text{BREQ}}$	Out	$\overline{\text{BREQ}}$ is asserted (low) by the EBU when the EBU requests to obtain ownership of the external bus.

1) The direction of this signal depends upon the mode in which the EBU is operating (see Page 15-30).

Two components that are equipped with the EBU arbitration protocol can be directly connected together (without additional external logic) as shown below:

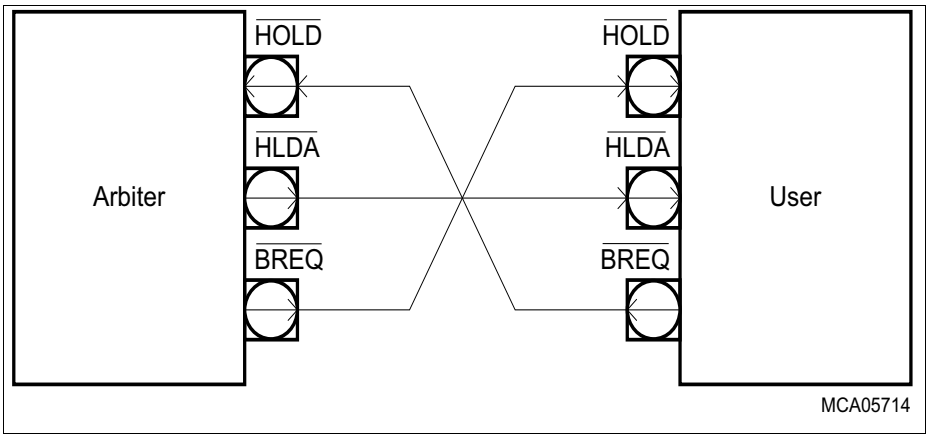


Figure 15-8 Connection of Bus Arbitration Signals

*Note: In the example of **Figure 15-8**, it is possible for the EBU to perform the function or either Arbiter or Participant (or indeed both the Arbiter and Participant may be the EBU).*

Table 15-7 lists the programmable parameters for the external bus arbitration.

Table 15-7 External Bus Arbitration Programmable Parameters

Parameter	Function	Description See
EBU_MODCON.ARBMODE	Arbitration mode selection	Page 15-30
EBU_MODCON.ARBSYNC	Arbitration input signal sampling control	
EBU_MODCON.EXTLOCK	External bus ownership locking control	
EBU_MODCON.TIMEOUTC	External bus time-out control	

15.11.3 Arbitration Modes

The arbitration mode of the EBU can be selected through configuration pins during reset or by programming the EBU_MODCON.ARBMODE bit field (see Page 15-30) after reset. Four different modes are available:

- No Bus Mode
- Sole Master Mode
- Arbiter Mode
- Participant Mode

15.11.3.1 No Bus Arbitration Mode

All accesses of the EBU to devices on the external bus are prohibited and will generate an SRI bus error. The EBU is in hold state all the time. The HOLD and HLDA arbitration inputs are ignored and BREQ arbitration output remains at high (inactive) level.

No Bus Mode is selected by EBU_MODCON.ARBMODE = 00_B.

15.11.3.2 Sole Master Arbitration Mode

The EBU is the only master on the external bus; therefore no arbitration is necessary and the EBU has access to the external bus at any time. The EBU is in owner state all the time. The HOLD arbitration input is ignored, and the HLDA and BREQ arbitration outputs remain at high (inactive) level.

Sole Master Mode is selected by EBU_MODCON.ARBMODE = 11_B.

15.11.3.3 Arbiter Mode Arbitration Mode

The EBU is the default owner of the external bus (e.g. applicable when operating from external memory). Arbitration is performed if an external master (e.g. second TriCore) needs to access the external bus.

The EBU is cooperative in relinquishing ownership of the external bus while operating in Arbiter Mode. When the HOLD input is active, the EBU will generate delay any attempt to access the external bus from the internal SRI. However, the EBU is aggressive in

regaining ownership of the external bus while operating in Arbiter Mode. The EBU, having yielded ownership of the bus, will always request return of ownership even if there is no EBU external bus access pending.

Arbiter Mode is selected by EBU_MODCON.ARBMODE = 01_B.

Table 15-8 and **Figure 15-9** show the functionality of the arbitration signals in Arbiter Mode.

Table 15-8 Function of Arbitration Pins in Arbiter Mode

Pin	Type	Pin Function in Arbiter Mode
$\overline{\text{HOLD}}$	In	In owner state (EBU is the owner of the external bus), a low level at $\overline{\text{HOLD}}$ indicates a request for bus ownership from the external master. In hold state (EBU is not the owner of the external bus), a high level at $\overline{\text{HOLD}}$ indicates that the external master has relinquished bus ownership, which causes the EBU to exit hold state.
$\overline{\text{HLDA}}$	Out	While $\overline{\text{HLDA}}$ is high, the EBU is operating in owner state. A high-to-low transition indicates that the EBU has entered hold state and that the external bus is available to the external master. While $\overline{\text{HLDA}}$ is low, the EBU is operating in hold state. A low-to-high transition indicates that the EBU has exited hold state, and has retaken ownership of the external bus.
$\overline{\text{BREQ}}$	Out	$\overline{\text{BREQ}}$ is high during normal operation. The EBU drives $\overline{\text{BREQ}}$ low two EBU clock cycles after entering hold state (after asserting $\overline{\text{HLDA}}$ low). $\overline{\text{BREQ}}$ returns high one clock cycle after the EBU has exited hold state (after driving $\overline{\text{HLDA}}$ high).

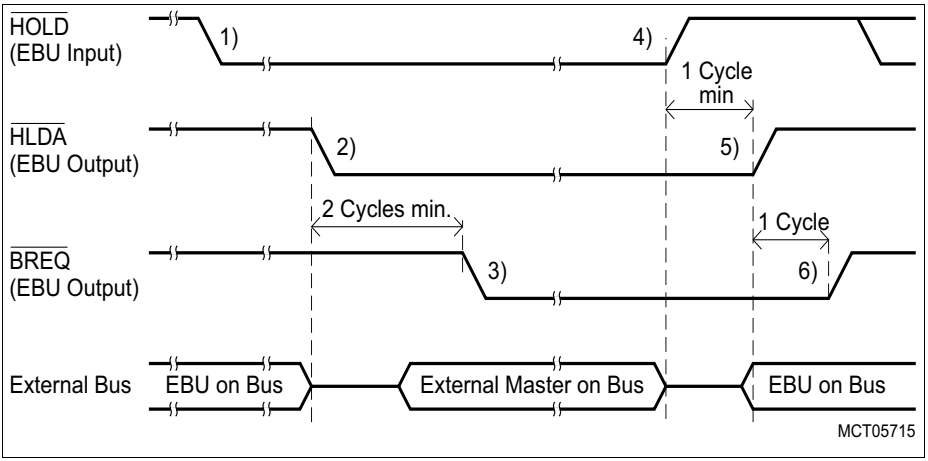


Figure 15-9 Arbitration Sequence with the EBU in Arbiter Mode

In Arbiter Mode, the arbitration sequence starts with the EBU as owner of the external bus.

1. The external master wants to perform an external bus access by asserting a low signal on the HOLD input.
2. When the EBU is able to release bus ownership, it enters hold state by tri-stating its bus interface lines and drives HLDA = 0 to indicate that it has released the bus. At this point, the external master ia allowed to drive the bus.
3. Two clock (EBU_CLK) cycles minimum after issuing HLDA low, the EBU drives BREQ low in order to regain bus ownership. This bus request is issued whether or not the EBU has a pending external bus access. However, the external master will ignore this signal until it has finished its bus access. This scheme assures that the external master can perform at least one complete external bus access.
4. When the external master has completed its access, it tri-states its bus interface and sets HOLD to inactive (high) level to signal that it has released the bus back to the EBU.
5. When the EBU detects that the bus has been released, it returns HLDA to high level and returns to owner state by actively driving the bus interface lines. There is always at least one clock (EBU_CLK) cycle delay from the release of the HOLD input to the EBU driving the bus.
6. Finally, the EBU deactivates the BREQ signal a minimum of one clock (EBU_CLK) cycle after deactivation of HLDA. Now (and not earlier) the external master can generate a new hold request to the EBU.

This sequence assures that the EBU can perform at least one complete bus cycle before it re-enters hold state as a result of a request from the external master.

The conditions that cause change of bus ownership when the EBU is operating in Arbiter Mode are shown in **Figure 15-10**.

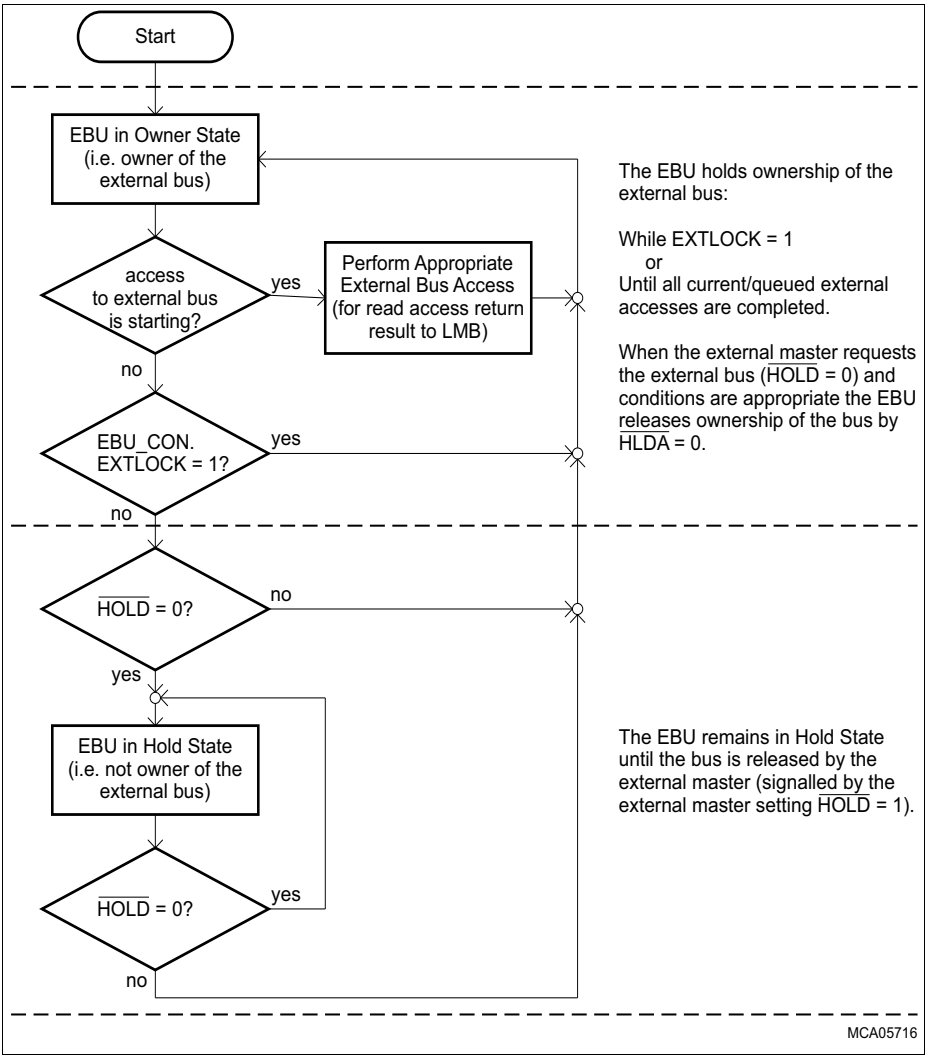


Figure 15-10 Bus Ownership Control in Arbiter Mode

15.11.3.4 “Participant Mode” Arbitration Mode

The EBU tries to gain bus ownership only in case of pending transfers (e.g. when operating from internal memory and performing stores to external memory). While the EBU is not the owner of the external bus (default state), any SRI access to the external bus will be delayed by the EBU. Any such access will cause the EBU to arbitrate for ownership of the external bus.

Once the access has been completed, the EBU will continue to accept requests from the SRI bus until the external master asserts $\overline{HOLD}$ = 0. After the external master has asserted $\overline{HOLD}$ = 0, the EBU will respond by delaying subsequent SRI accesses to external memory and will return ownership of the bus to the external master once any ongoing transaction is complete.

The use of the arbitration signals in Participant Mode is:

Table 15-9 Function of Arbitration Pins in Participant Mode

Pin	Type	Pin Function in Participant Mode
$\overline{HOLD}$	In	When the EBU is not in hold state ($\overline{HLDA}$ = 0) and has completely taken over control of the external bus, a low level at $\overline{HOLD}$ requests the EBU to return to hold state.
$\overline{HLDA}$	In	When the $\overline{HLDA}$ signal is high, the EBU is in hold state. When the EBU has requested ownership of the bus, the EBU is released from hold state by a high-to-low transition at $\overline{HLDA}$.
$\overline{BREQ}$	Out	$\overline{BREQ}$ remains high as long as the EBU does not need to access the external bus. When the EBU detects that an external access is required, it sets $\overline{BREQ}$ = 0 and waits for signal $\overline{HLDA}$ to become low. When the EBU has completed the external bus access (and has re-entered hold state), it will set $\overline{BREQ}$ = 1 to signal that it has relinquished ownership of the external bus.

Participant Mode arbitration mode is selected by EBU_CON.ARBMODE = 10_B.

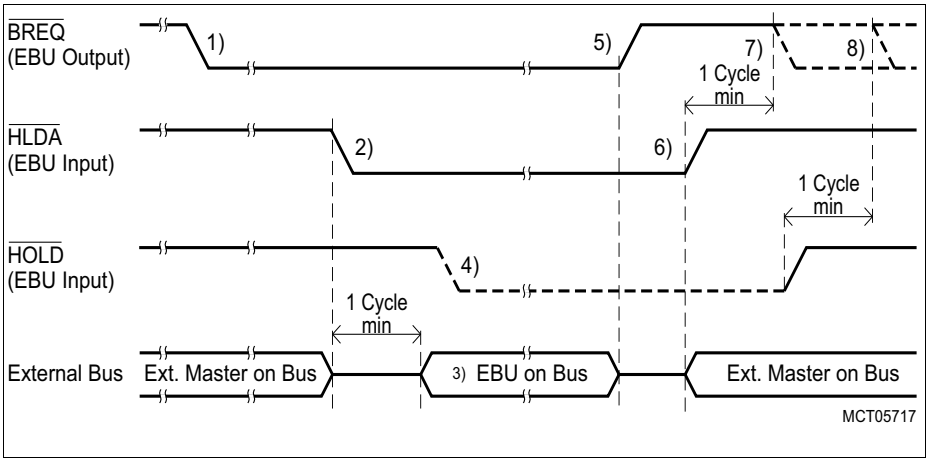


Figure 15-11 Arbitration Sequence with the EBU in Participant Mode

In Participant Mode, the arbitration sequence starts with the EBU in hold state.

1. The EBU detects that it has to perform an external bus access by asserting a low signal on the $\overline{\text{BREQ}}$ output.
2. When the external master is able to release bus ownership, the external master releases the external bus by tri-stating its bus interface lines and drives the $\overline{\text{HLDA}}$ = 0.
3. At least one clock (EBU_CLK) cycle after detecting $\overline{\text{HLDA}}$ = 0, the EBU will start to drive the external bus.
4. When the EBU is in owner state, the external master may optionally drive $\overline{\text{HOLD}}$ = 0 to signal that it wants to regain ownership of the external bus.
5. When the criterias are met for the EBU to release the bus ownership, the EBU enters hold state and drives $\overline{\text{BREQ}}$ = 1 output high to signal that it has released the bus.
6. When the external master detects that the EBU has released the bus ($\overline{\text{BREQ}}$ = 1), it returns $\overline{\text{HLDA}}$ to high level and takes ownership of the external bus.
7. The EBU will not request ownership of the external bus again ($\overline{\text{BREQ}}$ = 0) at least one clock (EBU_CLK) cycle after $\overline{\text{HLDA}}$ has been driven high).
8. In owner state, the EBU will not request ownership of the external bus $\overline{\text{BREQ}}$ = 0) for at least one clock (EBU_CLK) cycle after its $\overline{\text{HOLD}}$ input has been driven high.

The conditions that cause change of bus ownership when the EBU is operating in Participant Mode is shown in **Figure 15-10**.

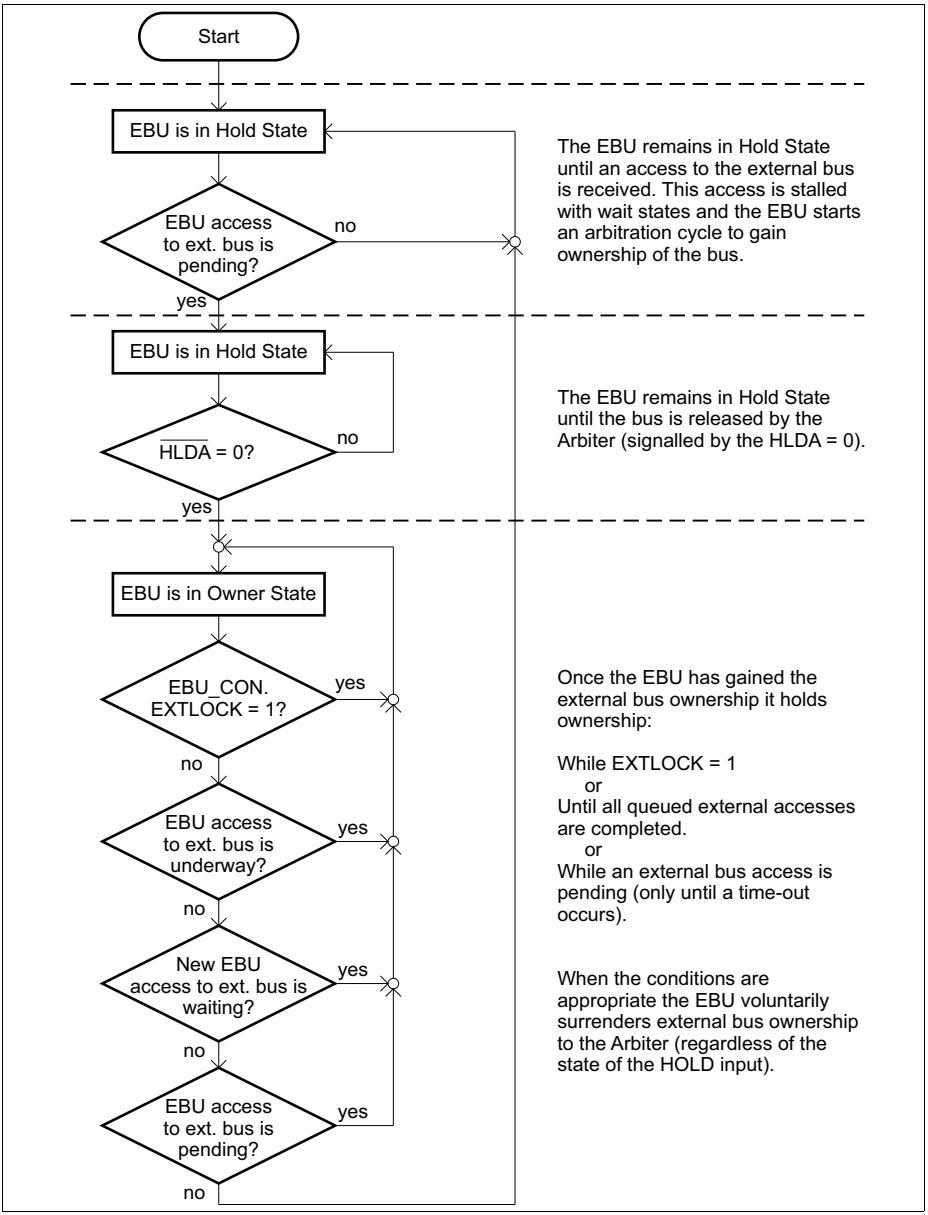


Figure 15-12 Bus Ownership Control with the EBU in Participant Mode

15.11.4 Switching Arbitration Modes

The arbitration logic will allow arbitration modes to be switched “on-the-fly” and will switch between modes as described in the following sections. However it is recommended that the arbitration mode is set as soon as possible after power on and that it is then not modified.

If this is not possible, then changes in arbitration mode should use “no bus” mode as an intermediate state with the arbiter in participant mode being placed in no bus mode first. Once both arbiters are in no bus mode, then the new modes can be set.

Note: It should be remembered that the arbitration logic drives the HLDA pin in arbiter or sole master modes and that having both sets of logic in one of these modes should be avoided to prevent contention on the signal.

15.11.4.1 Exiting No Bus Mode

As arbitration is disabled in this mode, there will be no attempt to gain or release the bus when exiting the mode. A transfer to participant mode will occur immediately and the arbitration logic will directly enter the hold state.

Transfers to sole master or arbiter mode will occur immediately and will result in the arbitration logic entering the owner state directly.

If an attached SDRAM is configured for automatic self refresh, the SDRAM will be taken out of self refresh as part of the transition to owner state.

15.11.4.2 Exiting Sole Master Mode

The arbitration logic will switch directly from sole master to arbiter mode remaining in the owner state.

The arbitration logic will exit sole master mode and transfer to no bus or participant modes only when in the hold state. If the arbitration logic is in owner state when the request to change mode is made, then the arbitration logic will release the bus before entering the new mode.

15.11.4.3 Exiting Arbiter Mode

The arbitration logic will exit arbiter mode and transfer to sole master mode only when in the owner state. If the arbitration logic is in hold state when the request to change mode is made, then the arbitration logic will request the bus and wait until ownership is granted before switching mode.

The arbitration logic will exit arbiter mode and transfer to no bus or participant modes only when in the hold state. If the arbitration logic is in owner state when the request to change mode is made, then the arbitration logic will release the bus before entering the new mode.

Note: If a transfer to participant mode results in both arbiters being in participant mode then there is a high possibility of a system deadlock. Any attempt to access external memory will result in the bus being requested. However, neither arbiter can drive HLDA so the bus cannot be granted. The external memory access will therefore stall indefinitely, blocking any further attempt to write to the EBU_MODCON register to change arbitration mode.

15.11.4.4 Exiting Participant Mode

The arbitration logic will exit participant mode and transfer to no bus mode only when in the hold state. If the arbitration logic is in owner state when the request to change mode is made, then the arbitration logic will release the bus before switching mode.

The arbitration logic will exit participant mode and transfer to sole master or arbiter modes only when in the owner state. If the arbitration logic is in hold state when the request to change mode is made, then the arbitration logic will request the bus and wait until ownership is granted before entering the new mode.

Note: As switching to sole master or arbiter mode requires ownership of the bus, it follows that the other arbiter in the system must be in arbiter mode to grant the bus. This will result in contention on the HLDA signal when the mode change completes.

15.11.5 Arbitration Input Signal Sampling

The sampling of the arbitration inputs can be programmed for two modes:

- Synchronous Arbitration
- Asynchronous Arbitration

When synchronous arbitration signal sampling is selected (ARBSYNC = 0), the arbitration input signals are sampled and evaluated in the same clock cycle. This mode provides the least overhead during arbitration (i.e. when changing bus ownership). The disadvantage is that the input signals must adhere to setup and hold times with respect to EBU_CLK to prevent the propagation of meta-stable signals in the EBU.

When asynchronous arbitration signal sampling is selected (ARBSYNC = 1), the arbitration signals are sampled and then fed to an additional register to be evaluated in the cycle following that in which they were sampled. This provides the EBU with good immunity to signals changing state at or around the time at which they are sampled. The disadvantage is the introduction of additional latency during arbitration (i.e. when changing bus ownership).

15.11.6 Locking the External Bus

The external bus can be locked to allow the EBU to perform uninterrupted sequences of external bus accesses. The EBU allows two methods of locking the external bus:

- Locked SRI accesses (i.e Read-Modify-Write)
- Lock bit EXTLOCK

When the EBU has ownership of the external bus and is performing external bus accesses in response to a locked SRI access sequence, the ownership of the external bus will not be relinquished until the locked SRI access sequence has been completed.

When lock bit EXTLOCK = 1, the EBU will hold the ownership of the external bus until EXTLOCK is subsequently cleared. If EXTLOCK is written to 1 while the EBU is the owner of the external bus, the EBU is immediately prevented from responding to requests for the external bus until EXTLOCK is cleared[1]. If EXTLOCK is written to 1 while the EBU is not the owner of the external bus, the EBU will immediately attempt to gain ownership. When the EBU gains the ownership of the external bus the next time, the external master is prevented from regaining ownership of the external bus until EXTLOCK is again cleared.

Note: There is no time-out mechanism available for the EXTLOCK bit. When the EBU is owner of the external bus with EXTLOCK bit set, the external master will remain locked off the bus until the EXTLOCK bit is cleared by software.

15.11.7 Interaction with Debug System

The EBU monitors the OCDS suspend signal used to freeze peripheral state when the system receives a break command. If the EBU detects a break it will request the external bus (if it is not the current owner). Once the EBU owns the bus, it will refuse any further arbitration requests until the suspend is released. This allows the external memories to be read by the attached debugger.

If this behaviour is not required, setting the **EBU_MODCON.OCDS_SUSP_DIS** bitfield will cause ecternal bus arbitration to continue to operate normally during a break.

15.11.8 Arbitrating SDRAM control signals

Normally, the memory controller will not surrender control of a connected SDRAM type device[2] when arbitrating the external bus. This is because the memory controller needs to keep track of which pages are open in the SDRAM and also because of restrictions on the SDRAM clock.

However, the memory controller can be programmed to tri-state the SDRAM control signals SDCLKO, CKE, $\overline{RAS}$ and $\overline{CAS}$ by setting the EBU_MODCON.SDTRI bit to 1_B. When this bit is set, SDRAM can be shared with another controller provided certain conditions are met by both memory controllers.

1) Requests for the external bus already pending when EXTLOCK is set will not be cancelled so the EBU can give up control of the external bus after EXTLOCK is set provided that the request occurs before the EXTLOCK bit is set.

2) SDRAM, DDRAM & LPDDR-NVM devices

- The SDRAM must be in self refresh mode with the clock safely stopped before ownership of the external bus is transferred. This ensures that all pages in the SDRAM are closed and that the CKE signal is at logic zero. This can be achieved for the memory controller by setting the SDRMREF.AUTOSELFR to 1_B.
- The SDRAM CKE input must have a pull down sufficient to ensure that there is a guaranteed logic zero on the input while bus ownership is being transferred.

15.12 Start-Up/Boot Process

During reset, the EBU will be in “nobus” mode and all pins will be controlled by the Port I/O logic. After reset is removed, the EBU will check to see if external boot has been requested. If external boot is required, then the EBU will set the BUSCONx.PORTW and BUSRCONx.AGEN fields to the appropriate values and enable the necessary pins for use by the EBU. If external boot is not requested then the EBU will remain in “nobus” mode until configured by software.

15.12.1 Disabled (arbitration mode is “nobus”)

The EBU will come up with access to the external bus disabled after reset (i.e. no access from SRI to external memory is possible without EBU re-configuration).

15.12.2 External Boot Mode

The External Boot Mode of the EBU allows the EBU to boot (i.e. run all start-up code) from external memory. Immediately after reset a system may have no knowledge as to the type of memory connected to the external bus. When external boot mode is selected, the EBU will exit reset with the registers configures to allow slow (safe) accesses to both mexed and non-muxed asynchronous memories.

When External Boot Mode is selected, the EBU will be configured to automatically read a 32-bit Boot Configuration Value from an external memory (connected to $\overline{CS0}$, chip select region 0). The Boot Configuration Value in the external boot memory makes it possible to initialize the EBU with more appropriate configuration values for the external boot memory. These configuration values will, in turn, be used for the subsequent read accesses from the external boot memory (i.e. instruction fetches).

The boot configuration fetch can be triggered using two methods:

- Setting the SYSCON.SETEXTBEN bit and then resetting the EBU. In this case all accesses to the EBU will be held while the configuration fetch is in progress
- Writing 1_B to the EBU_EXTBOOT.EBUCFG bit before the end of system boot[1)]. In this case the EBU_EXTBOOT.CFGEND bit should be polled to determine when the fetch has ended and the registers updated.

1) This is determined by the state of the BOOT_ACTIVE flag generated by the SCU.

In both cases the EBU_EXTBOOT.CFGERR bit will be set if the configuration word fetch fails to retrieve valid data. See **"Configuration Word Fetch Process" on Page 15-42** for a full description of the configuration process.

Note: External boot cannot be used if an SDRAM/DDRAM or LPDDR_NVM is connected. This is because these devices do not have an external reset input and will therefore be in an indeterminate state after a reset of the EBU. This state could cause the memory device to drive the databus and, as the DDRCLKO output is disabled after reset, the memory device will remain in this state during the external boot process and interfere with the reads from the boot memory.

15.12.2.1 Configuration Word Fetch Process

If an External Boot configuration fetch is enabled, the EBU will perform one external bus read access to external bus address 000004_H of the memory device attached to chip select line $\overline{CS0}$. As it is assumed by the that the attached memory device has a 32 bit data bus, this is equivalent to a SRI or byte address of 000010_H because of the address translation implemented in the EBU (see **Chapter 15.13.4** on **Page 15-52**).

The data read by this read access is used to configure the EBU with parameters (see **Page 15-44**). The boot read access itself is performed as an asynchronous access cycle with all timing parameters set to their maximum values. This access scheme supports ROMs, EPROMs or Flash memories with both separate address and data connections and also multiplexed address and data connections. **Figure 15-13** shows a timing example of booting from a standard demultiplexed asynchronous memory device.

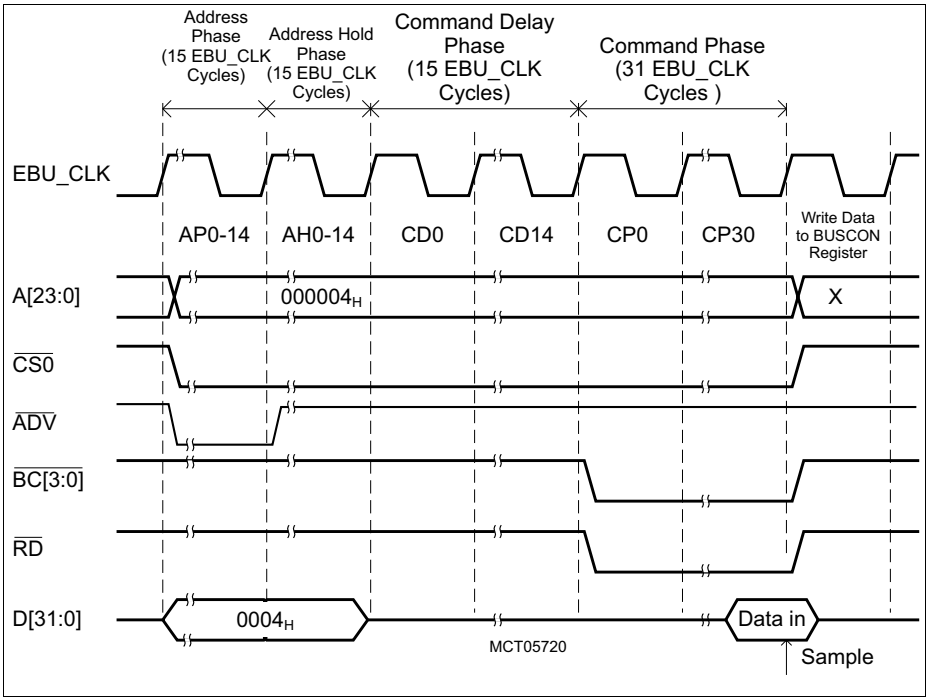


Figure 15-13 Boot Read Access Cycle

When a configuration fetch is triggered, the EBU waits 256 EBU_CLK clock cycles until the access is initiated, as shown in **Figure 15-13**. This gap is inserted to fulfill the recovery times needed by external synchronous devices such as Flash ROMs. During the read access, the maximum number of programmable EBU_CLK cycles is inserted (WAITRDC = 31), and the evaluation of the $\overline{\text{WAIT}}$ signal is inhibited.

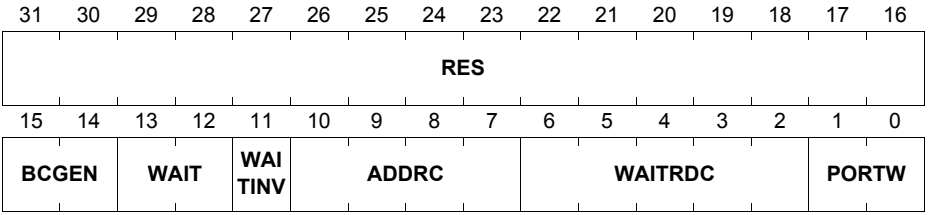
Note: The boot memory must be connected to chip select line $\overline{CS0}$. The EBU assumes that the boot memory is 32-bits wide and, therefore, always reads a 32-bit configuration word at the "Data in" point shown above.

*Note: If $FFFF_H$ is returned as on bits 15 downto 0 of the configuration word during the boot read cycle (e.g. by reading the configuration word from an erased external boot memory device), the arbitration mode is set to No Bus Mode (ARBMODE = 00_B, see **"No Bus Arbitration Mode" on Page 15-30**). However since a value for the BCGEN field of 11_B is not legal for boot, at least one bit of the fetched word will be 0_B for valid data*

15.12.2.2 Boot Configuration Value

The EBU supports boot operation from 32-bit wide memories. The format of the Boot Configuration Value is as follows (Bits 31 to 16 are reserved for future expansion):

Boot Configuration Value



Field	Bits	Description
PORTW	1:0	**Port Width** 00_B external memory is 8 bit 01_B external memory is 16 bit 10_B external memory is two 16 bit memories in parallel to make a 32 bit memory 11_B external memory is 32 bit
WAITRDC	[6:2]	**Number of Wait States for Read Accesses** Loaded into EBU_BUSRAP0.WAITRDC.
ADDRC	[10:7]	**Number of Cycles in the Address Phase** Loaded into EBU_BUSRAP0.ADDRC.
WAITINV	11	**WAIT Input Polarity Control** Loaded into EBU_BUSRCON0.WAITINV.
WAIT	[13:12]	**External Wait State Control** Loaded into EBU_BUSRCON0.WAIT.
BCGEN	[15:14]	**Byte Control Signal Control** Loaded into EBU_BUSRCON0.BCGEN.
RES	[31:16]	**Reserved** This bit field is reserved for future use. In the TC1798, RES should always be set to 0_H.

15.13 Accessing the External Bus

Each internal SRI master can access external devices via the EBU. The EBU provides four user-programmable external memory regions. Each of these regions is provided with a set of registers that determine the parameters of the external bus transaction and one chip select signal. An SRI transaction that matches one of these user-programmable external memory regions is translated by the EBU to the appropriate external access(es).

In the TC1798, the EBU responds to the address ranges as defined in **Table 15-10**.

Table 15-10 EBU External Address Ranges

Address Range	Description	Action
$8300\ 0000_H$ - $8EFF\ FFFF_H$	External memory space (cached area)	compare
$A300\ 0000_H$ - $AEFF\ FFFF_H$	External memory space (non-cached area)	
$F800\ 0000_H$ - $F800\ 03FF_H$	EBU Registers	access registers

The “compare” action means that the EBU compares the supplied SRI address to all its external regions. If a match is found, the EBU performs the appropriate external bus access. Otherwise, the EBU generates an SRI Error Acknowledge.

The “access registers” action means that the EBU is selected for a control/status register access. The EBU performs the requested register access (or generates an SRI Error Acknowledge if there is no register at the supplied address).

For all address ranges that not listed in **Table 15-10** the EBU is not selected and SRI requests are ignored.

15.13.1 External Memory Regions

Each of the external memory regions has its own associated chip select output $\overline{CS}[3:0]$ and a set of control registers to specify the type of memory/peripheral device and the access parameters.

The access parameters for each of the regions can be programmed individually to accommodate different types of external devices. Separate control registers are available to control read and write accesses. This allows optimal access types, speeds and parameters to be chosen. Access type is configured via BUSRCONx and BUSWCONx. Access parameters are configured via BUSRAPx and BUWAPx.

Throughout this document the generic term EBU_BUSCONx is used when either of BUSRCONx or BUSWCONx is applicable and EBU_BUSAPx is used when either of BUSRAPx or BUSWAPx is applicable.

Table 15-11 EBU Address Regions, Registers and Chip Selects

Region	Associated Chip Select	Address Select Registers	Bus Configuration Registers	Bus Access Parameters Registers
Region 0	$\overline{CS0}$	EBU_ADDRSEL0	EBU_BUSRCON0 EBU_BUSWCON0	EBU_BUSRAP0 EBU_BUSWAP0
Region 1	$\overline{CS1}$	EBU_ADDRSEL1	EBU_BUSRCON1 EBU_BUSWCON1	EBU_BUSRAP1 EBU_BUSWAP1
Region 2	$\overline{CS2}$	EBU_ADDRSEL2	EBU_BUSRCON2 EBU_BUSWCON2	EBU_BUSRAP2 EBU_BUSWAP2
Region 3	$\overline{CS3}$	EBU_ADDRSEL3	EBU_BUSRCON3 EUB_BUSWCON3	EBU_BUSRAP3 EBU_BUSWAP3

Table 15-12 lists the programmable parameters that are available for the four external regions (regions 0 to 3) independent of the attached memory device.

Table 15-12 Programmable Parameters of Regions

Register	Parameter (Bit/Bit field)	Function
EBU_ADDRSELx	ALTSEG	Alternate segment of region to be compared to SRI address bits [31:28].
	BASE	Region base address to be compared with SRI address in conjunction with the MASK parameter.
	MASK	Address mask for each external region. Specifies the number of right-most bits in the base address starting from bit 26.
	WPROT	Write Protect bit for each region.
	ALTENAB	Alternate segment enable of a region. Determines whether or not parameter ALTSEG is always compared to SRI address.
	REGENAB	Enable bit for each region. A disabled region will always generate a miss during address comparison.
EBU_BUSCONx	AGEN	Region access type: See **Section 15.14.1**

15.13.2 Address Comparison

Address Comparison is implemented in addition to the address decoding in the SRI bus matrix and is used to map SRI addresses to the EBU regions. The address comparison operation will, by default, take two clock cycles. If the frequency of the SRI bus is set to be less than or equal to 180 MHZ, then the SRI interface of the EBU can be set to use single cycle decode. This is controlled by the **EBU_MODCON.FAST_SRI** bitfield. When set to 1_B, the SRI interface will use a single cycle for address decode.

Note: As the FAST_SRI bit modifies the SRI interface behaviour dynamically, some care is needed when changing the mode of operation. When setting or clearing the bit, time should be allowed after writing the register for the setting to take effect before attempting a read from the EBU. To ensure the new setting has taken effect, it is suggested that the EBU_MODCON register is written twice with the new setting. This is because internal architecture constraints mean that the data from the first write must have been transferred to the register before the second write can proceed.

15.13.2.1 Operation Address Comparison

Each of the four EBU regions can be programmed for independent base addresses and lengths by bits and bit fields in registers EBU_ADDRSELx.

- Bit REGEN is the enable control of a region. If the region is disabled (REGEN = 0), no address comparison will take place for the region.
- Bit field BASE specifies address bits A[31:12] of region x, where A[31:28] must only point to segments 8, 10, 13, and 14 (see **Table 15-13** on **Page 15-50**).[1)]
- Bit field MASK determines the length of a region. It specifies how many bits of anSRI SRI address must match the contents of the BASE(x) bit field (to a maximum of 15, starting with A[26]). Note that address bits A[31:27] must always match.
- Bit WPROT write protects a region. If the region is protected (WPROT = 1), no address comparison will take place for that region on a write access[2)]
- Bit field ALTSEG determines the number of an alternate segment that can be used for address comparison with A[31:28] (if enabled by ALTENAB = 1).
- Bit ALTENAB determines whether an additional alternate segment number as defined by ALTSEG is used for address comparison.

1) There is no hardware lockout preventing other values being written to A[31:28], but in most cases this will result in an inaccessible memory. Enabling a memory region at segment $F8_H$ will result in the memory region conflicting with the registers. The EBU will not work correctly if this is done.

2) The WPROT bit also appiles to the read phase of a read modify write, SRI transaction. This is to prevent two possible error conditions. The first would be where the read phase was accepted and the write phase errored. This is an SRI protocol violation. The second would be where the read and write accesses occurred to different memory addresses (if the read took place to a write protected region and there was an unprotected, lower priority, region mapped to the same address space).

The address comparison scheme is shown in **Figure 15-14**.

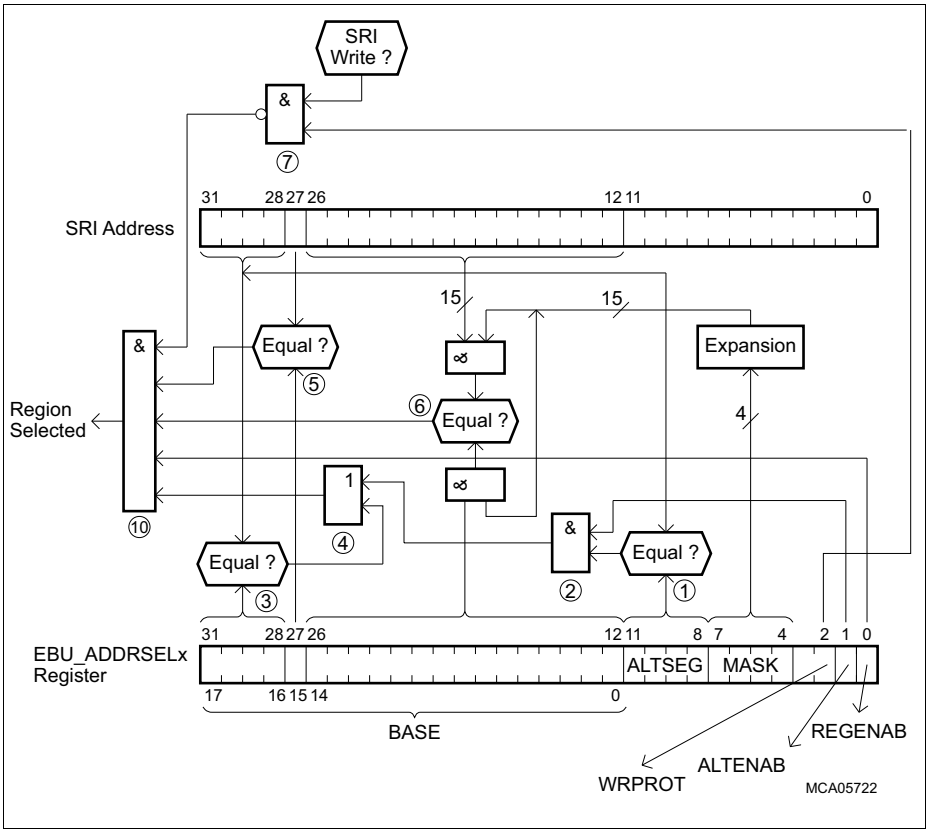


Figure 15-14 Address Comparison to Detect Access to External Region

When the EBU is processing an SRI access, the address is compared in parallel to the parameters of all four regions. The address comparison process for one region is shown in **Figure 15-14**. This process is as follows:

1. The most significant four bits of the SRI address are compared with the ALTSEG bit field (“alternate” segment address). The result of the comparison (1 if equal, otherwise 0) is fed to an AND gate.
2. If ALTENAB = 0, the alternate segment function is disabled and the output of the AND gate is 0. With ALTENAB = 1, the alternate segment function is enabled, and the result of the comparison between ALTSEG and the segment part of the SRI address is fed to an OR gate.

3. The most significant four bits of the SRI address (“main” segment address) are compared to the most significant four bits of the BASE bit field. The result of the comparison (1 if equal, otherwise 0) is fed to the OR gate.
4. The OR gate combines the result of the “main” and “alternate” segment comparisons generates a 1 if the SRI address is in the selected segment(s) for the region, otherwise it generates 0. The output of the OR gate is fed to the final AND gate.
5. Bit 27 of the SRI address is (unconditionally) compared with bit 15 of the BASE bit field. The result of the comparison (1 if equal, otherwise 0) is fed to the final AND gate.
6. The appropriate number of SRI address bits from bit 26 downwards is compared with the corresponding bits from bit field BASE bit 14 downwards. The number of bits used for the comparison is controlled by the MASK bit field. The result of the comparison (1 if the appropriate bits are equal, otherwise 0) is fed to the final AND gate.
7. The NAND gate delivers a 0 if a write is performed to a read-only region (WRPROT=1), and prevents the region from being selected. The output of the NAND gate is fed to the final AND gate.
8. The final AND gate delivers a 1 if a match occurs at the address comparison, and the region x is enabled by REGENAB = 1, and the access is not a write access when the region is defined as read-only access.

This address decoding scheme has the following effects:

- The smallest possible address region is 2^{12} bytes (4 Kbyte)
- The largest possible address region is 2^{27} bytes (128 Mbyte)
- The start address of a region depends on the size of the region. It must be at an address that is a multiple of the size of a region; for example, the smallest region can be placed on any 4-Kbyte boundary, while the largest region can be placed on 8-Mbyte boundaries only.

Table 15-13 shows the possible region sizes and start granularity, as determined by the programming of the MASK bit field. The range of the offset address within such a region is also given.

Table 15-13 EBU Address Regions Size and Start Address Relations

MASK	No. of Address Bits compared to BASE[26:12]	Range of Address Bits compared to BASE[26:12]	Region Size and Start Address Granularity	Range of Offset Address Bits within Region
1111_B	15	A[26:12]	4 Kbyte	A[11:0]
1110_B	14	A[26:13]	8 Kbyte	A[12:0]
1101_B	13	A[26:14]	16 Kbyte	A[13:0]
1100_B	12	A[26:15]	32 Kbyte	A[14:0]
1011_B	11	A[26:16]	64 Kbyte	A[15:0]

Table 15-13 EBU Address Regions Size and Start Address Relations (cont'd)

MASK	No. of Address Bits compared to BASE[26:12]	Range of Address Bits compared to BASE[26:12]	Region Size and Start Address Granularity	Range of Offset Address Bits within Region
1010_B	10	A[26:17]	128 Kbyte	A[16:0]
1001_B	9	A[26:18]	256 Kbyte	A[17:0]
1000_B	8	A[26:19]	512 Kbyte	A[18:0]
0111_B	7	A[26:20]	1 Mbyte	A[19:0]
0110_B	6	A[26:21]	2 Mbyte	A[20:0]
0101_B	5	A[26:22]	4 Mbyte	A[21:0]
0100_B	4	A[26:23]	8 Mbyte	A[22:0]
0011_B	3	A[26:24]	16 Mbyte	A[23:0]
0010_B	2	A[26:25]	32 Mbyte	A[24:0]
0001_B	1	A[26]	64 Mbyte	A[25:0]
0000_B	0	–	128 Mbyte	A[26:0]

The EBU uses the four region select outputs from the above scheme, in conjunction with its own address decode logic, to react to SRI accesses as follows:

1. **Address is in the EBU register space:**
   An EBU register access is executed, and in case of a illegal register address, SRI Error Acknowledge is returned.
2. **Address matches exactly one enabled external region:**
   The requested access is performed to external memory.
3. **Address matches more than one enabled region (overlapping regions):**
   The requested access is performed using the parameters from the region with highest priority. Region 0 has the highest priority and region 3 the lowest priority.
4. **Address matches disabled region(s) or no address match:**
   The EBU returns an SRI Error Acknowledge.

When defining mirrored segments, the user is responsible for ensuring that there is no collision. There is no checking mechanism in hardware that ensures that each segment defined (either in BASE[31:28] or ALTSEG[11:8] or both) is exclusive. Therefore, the user must ensure that each mapping from region 0 to 3 does not interfere with any other; otherwise, only the mapping with the highest priority will take effect.

15.13.3 SRI Bus Width Translation

If the SRI access size is wider than the external bus width specified for the selected external region, the internal access is split in the EBU into several external accesses. For example, if the SRI requests to read a 64-bit word and the external device is only 16-bit

wide, the EBU will automatically perform four external 16-bit accesses. When multiple accesses are generated in this way, external bus arbitration is blocked until the multiple access is complete. This means that the EBU remains the owner of the external bus for the duration of the access sequence. The external accesses are performed in ascending SRI address order.

15.13.4 Address Alignment During Bus Accesses

During an external bus access, the EBU will align the internal byte address to generate the appropriate external word or half-word address aligned to the external address pins. The address alignment will be done as follows:

- For 8 bit memory accesses
  - AD[15:0] will be driven with the value from A_{SRI}[15:0] (mutiplexed accesses only)
  - A[27:0] will be driven with the value from A_{SRI}[27:0]
- For 16 bit memory accesses
  - AD[15:0] will be driven with the value from A_{SRI}[16:1] (mutiplexed accesses only)
  - A[27:0] will be driven with the value from A_{SRI}[28:1]
- For 32 bit memory accesses
  - AD[15:0] and AD[31:16] will both be driven with the value from A_{SRI}[17:2] (accesses to paired 16-bit multiplexed devices only)
  - AD[31:0] will be driven with the right-justified and zero-padded value from A_{SRI}[31:2] (accesses to paired 32-bit multiplexed devices only)
  - A[27:0] will be driven with the value from A_{SRI}[28:2]

15.13.5 SRI Data Buffering

The data for all SRI writes are “posted” into a buffer in the SRI interface before the access is passed to the state machine blocks for execution. This means that all the write data is available to the state machine before the access starts independent of the relative clock frequencies of the internal and external buses and that the write completes at the initiating master before the data is written to the external memory.

15.13.6 Chip Select Control

The EBU generates four chip select signals, $\overline{CSx}$, which are all available at dedicated chip select outputs. Each chip select is associated exclusively with an EBU region. See **"External Memory Regions" on Page 15-45** for a complete description....

15.13.7 Combined Chip Select ($\overline{CSCOMB}$)

The EBU can also generate a combined, global chip select. This is controlled using the EBU_ADDRSELx.GLOBALCS register fields. If this is set to 1_B in a register, then the $\overline{CSCOMB}$ chip select is asserted whenever the associated normal chip select is asserted. Multiple GLOBALCS fields can be set simultaneously.

15.14 Connecting External Memories

The EBU supports interconnection to a wide variety of memory/peripheral devices with flexible programming of the access parameters. In the following sections, the basic features for these access modes are described. The types of external access cycles provided by the EBU are:

- Asynchronous accesses with multiplexed or demultiplexed address and data bus
  - ROMs, EPROMs
  - NOR flash devices
  - NAND flash devices
  - Static RAMs and PSRAMs
- Synchronous accesses with multiplexed or demultiplexed address and data bus
  - NOR flash devices (operating in burst mode)
  - DDR flash devices
  - PSRAMs
  - Page mode flash[1)]
- Accesses using SDRAM Type Command Protocol
  - Mobile SDRAM
  - Mobile DDRAM
  - LPDDR-NVM

Note: Not all memory types supported by the memory controller are known to be available in all quality grades and temperature ranges.

Each type of access is controlled by a state machine in the EBU kernel. See **Table 15-14** for a list of the access types supported and the controlling state machine.

SDRAM type accesses comply with the relevant protocol and have limited programmability. Asynchronous and Synchronous accesses use the concept of access

1) Page mode flash devices are not synchronous but have in common with synchronous devices the ability to return multiple data words for each supplied address. They are therefore handled by the synchronous state machine of the EBU

phases of programmable duration and are more fully described in **“Phases for Asynchronous and Synchronous Accesses” on Page 15-62**

15.14.1 Programmable Device Types

Each CS region (0 to 3) can be individually configured using the BUSCONx.AGEN register field, to be connected to one of the following external memory/device types:

Table 15-14 agen description

agen value	Device Type	State Machine
0	Muxed Asynchronous Type (default after reset)	Asynchronous
1	Muxed Burst Type	Synchronous
2	NAND flash (page optimised)	Asynchronous
3	Muxed Cellular RAM	Synchronous
4	Demuxed Asynchronous Type	Asynchronous
5	Demuxed Burst Type	Synchronous
6	Demuxed Page Mode	Synchronous
7	Demuxed Cellular RAM	Synchronous
8	SDRAM	SDRAM
9	DDR Burst Flash (Spansion protocol)	Synchronous
10	LPDDR NVM (Jedec 42.4 DDR non-volatile memory)	SDRAM
11	reserved	-
12	DDRAM	SDRAM
13	ONFI 2.0 NAND flash	Synchronous
14	reserved	-
15	reserved	-

The AGEN fields for the BUSRCONx and BUSWCONx can, in most cases, be set independently. This allows devices such as burst flash, which require synchronous reads and asynchronous writes to be supported efficiently.

There are device types where this capability does not confer any advantage. In these cases, writing to the BUSRCONx.AGEN field will also update the BUSWCONx.AGEN field.

The AGEN values which trigger the automatic BUSWCONx.AGEN update are:

- SDRAM: 8_D
- LPDDR NVM: 10_D

- DDRAM: 12_D

While the BUSRCONx.AGEN field is set to one of these values, any attempt to set the value of the related BUSWCONx.AGEN field will be ignored.

15.14.2 Support for Multiplexed Device Configurations

Memory Controller supports a number of configurations of Multiplexed memory/peripheral devices using different values of the EBU_BUSRCONx.PORTW bit-field. The EBU_BUSWCONx registers also contain the PORTW field but in this case the field is read only and reflects the value set in the related one of the EBU_BUSRCONx registers. The values set in the EBU_BUSRCONx registers are used for both read and write accesses.

Note: When using multiplexed devices a non-zero recovery phase is mandatory for all devices to prevent read data from one access conflicting with the address for the next access to the multiplexed memory.

Table 15-15 Pins used to connect Multiplexed Devices to Memory Controller

Memory Device Configuration	Memory Controller Pins			Section
	A(27:0)[1]	AD(31:16)	AD(15:0)	
8-bit MUX	A(27:0)	-	A(7:0)/ D(7:0)	8-bit Multiplexed Memory/Peripheral Configuration
16-bit MUX	A(27:0)	-	A(15:0)/ D(15:0)	16-bit Multiplexed Memory/Peripheral Configuration
Twin 16-bit MUX	A(27:0)	A(15:0)/ D(31:16)	A(15:0)/ D(15:0)	Twin 16-bit Multiplexed Device Configuration
32-bit MUX	-	A(31:16)/ D(31:16)	A(15:0)/ D(15:0)	32-bit Multiplexed Memory/Peripheral Configuration

1) These pins are always outputs which are connected to address pins on the Multiplexed device(s)

Table 15-16 Selection of Multiplexed Device Configuration

PORTW value	
00_B	8-bit multiplexed (deprecated)[1]
01_B	16-bit multiplexed[2]

Table 15-16 Selection of Multiplexed Device Configuration (cont'd)

PORTW value	
10_B	Twin, 16-bit Multiplexed[3)]
11_B	32 bit multiplexed[4)]

1) 8-bit port width is only intended for NAND flash and ONFI devices which do not require particular values on the address bus. Correct operation of multiplexed addressing is not verified or guaranteed.

2) Address will only be driven onto AD(15:0) during the address and address hold phases. A(15:0) will be driven with address for duration of access

3) Lower 16 bits of address will be driven onto both A(15:0) and AD(15:0) during the address and address hold phases

4) Full address will be driven onto A(15:0) and AD(15:0) during the address and address hold phases

15.14.2.1 Twin 16-bit Multiplexed Device Configuration

This mode allows the use of two 16-bit multiplexed devices to create a 32-bit wide bus. Throughout the complete external bus cycle the address[1)] is driven onto Memory Controller pins A(27:0). During the address phase the low 16 bits of the address are driven (in parallel) to Memory Controller pins AD(15:0) and AD(31:16). This ensures that both multiplexed devices are issued with the same address during the address phase. Data (32-bit) is written to/read from the AD(31:16) pins for MSW and the AD(15:0) pins for LSW during the data phase. The interconnect between Memory Controller and two 16-bit Multiplexed devices in this mode is shown below (note: for clarity only the address/data signals are shown):-

1) This address is pre-aligned according to the bus width as detailed in **Section 15.13.4**.

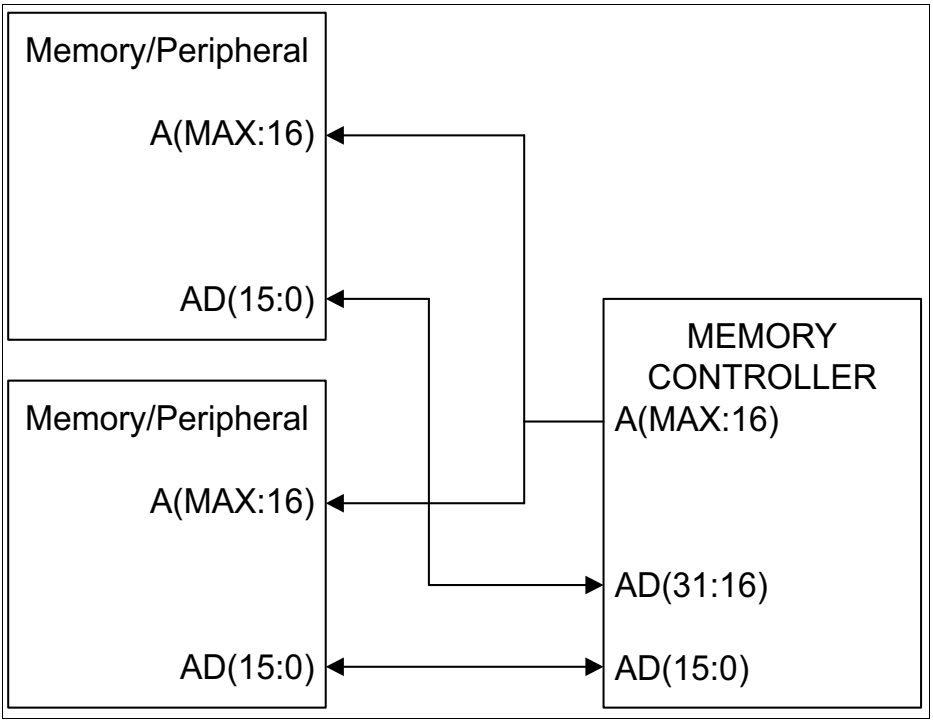


Figure 15-15 Connection of twin 16-bit Multiplexed Device's to Memory Controller

15.14.2.2 16-bit Multiplexed Memory/Peripheral Configuration

Throughout the complete external bus cycle the address[1)] is driven onto Memory Controller pins A(27:0). During the address phase the low 16 bits of the address are driven to Memory Controller pins AD(15:0). Data (16-bit) is driven to/read back from the AD(15:0) pins during the data phase. The interconnect between Memory Controller and a 16-bit Multiplexed device in this mode is shown below (note: for clarity only the address/data signals are shown):-

1) This address is pre-aligned according to the bus width as detailed in **Section 15.13.4**.

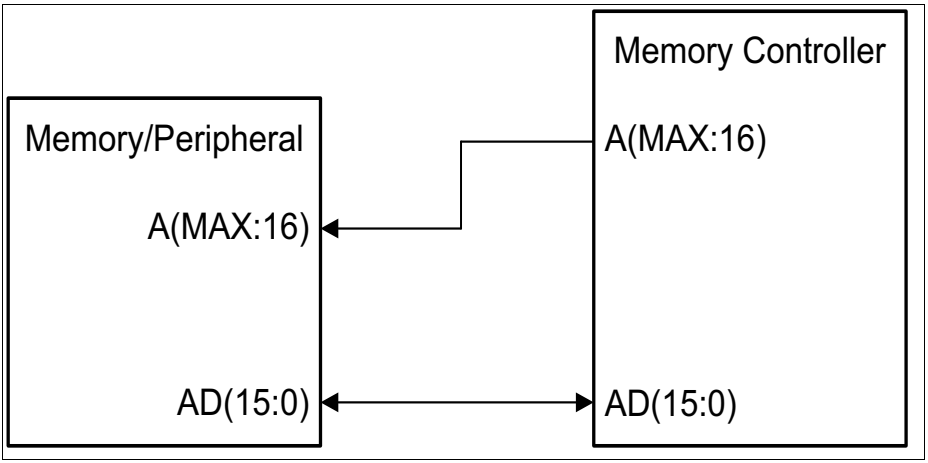


Figure 15-16 Connection of a 16-bit Multiplexed Device to Memory Controller

15.14.2.3 8-bit Multiplexed Memory/Peripheral Configuration

The EBU drives signals for 8 bit devices in an identical manner to 16 bit devices. AD(15:0) are driven for address and write data and BC(1:0) are enabled. However valid write data only appears on AD(7:0) and BC(1) is always inactive. Read data is only sampled from AD(7:0).

15.14.2.4 32-bit Multiplexed Memory/Peripheral Configuration

During the address phase the lower 16 bits of the 25 bit address are driven to Memory Controller pins AD(15:0), the most significant 9 bits of the address are driven to pins AD(24:16) and pins AD(31:17) are driven with 0 (zero). Data (32-bit) is driven to/read from the AD(31:0) pins during the data phase. The interconnect between Memory Controller and a 32-bit Multiplexed device in this mode is shown below (note: for clarity only the address/data signals are shown):-

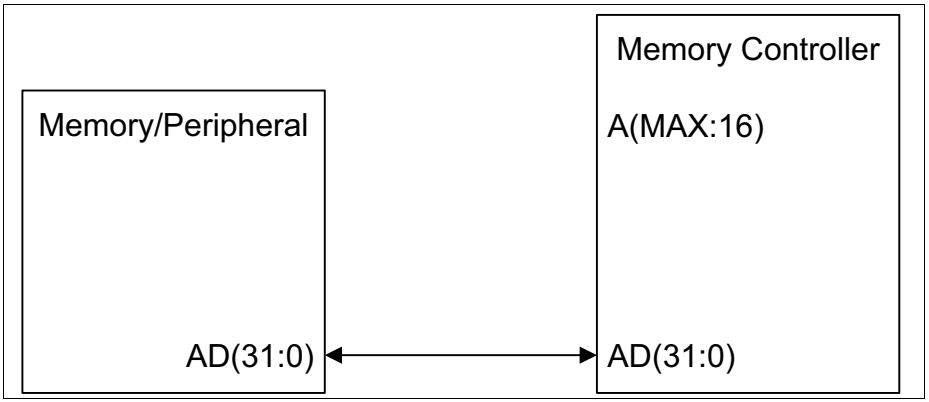


Figure 15-17 Connection of a 32-bit Multiplexed Device to Memory Controller

15.14.3 Support for Non-Multiplexed Device Configurations

The Memory Controller supports 16-bit and 32-bit non-multiplexed memory devices.

Table 15-17 Pins used to connect non-multiplexed Devices to Memory Controller

Memory Device Configuration	Memory Controller Pins			Section
	A(27:0)	AD(31:16)	AD(15:0)	
8-bit non-MUX	A(27:0)	-	D(7:0)	8-bit non-Multiplexed Memory/Peripheral Configuration
16-bit non-MUX	A(27:0)	-	D(15:0)	16-bit non-Multiplexed Memory/Peripheral Configuration
twin, 16-bit non-MUX	A(27:0)	D(31:16)	D(15:0)	32-bit non-Multiplexed Memory/Peripheral Configuration
32-bit non-MUX	A(27:0)	D(31:16)	D(15:0)	32-bit non-Multiplexed Memory/Peripheral Configuration

Table 15-18 Selection of non-Multiplexed Device Configuration

PORTW value	
00_B	8-bit[1)]
01_B	16-bit
10_B	Twin 16-bit
11_B	32-bit

1) 8-bit port width is only intended for NAND flash and ONFI devices which do not require particular values on the address bus. Correct operation of addressing for other device types is not verified or guaranteed

15.14.3.1 16-bit non-Multiplexed Memory/Peripheral Configuration

Throughout the complete external bus cycle the address[1)] is driven onto Memory Controller pins A(27:0). Data (16-bit) is driven to/read back from the AD(15:0) pins during the data phase. The interconnect between Memory Controller and a 16-bit non-Multiplexed device in this mode is shown below (note: for clarity only the address/data signals are shown):-

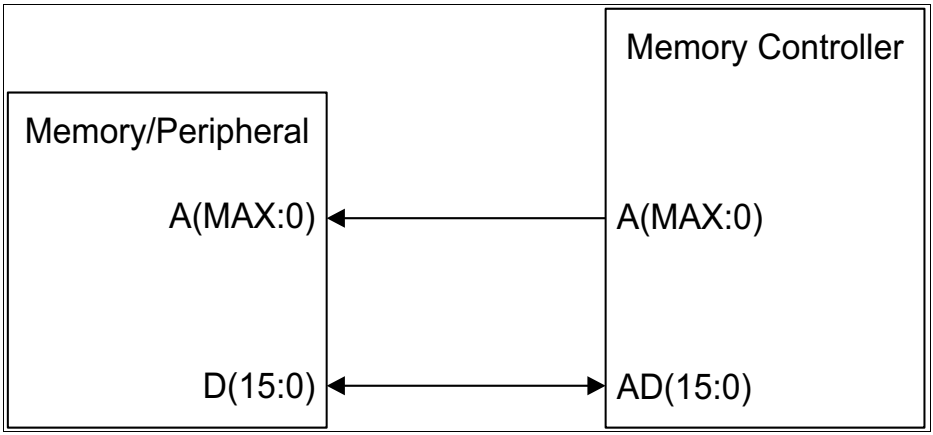


Figure 15-18 Connection of a 16-bit non-Multiplexed Device to Memory Controller

15.14.3.2 8-bit non-Multiplexed Memory/Peripheral Configuration

The EBU drives signals for 8 bit devices in an identical manner to 16 bit devices. AD(15:0) are driven for address and write data and BC(1:0) are enabled. However valid

1) This address is pre-aligned according to the bus width as detailed in **Section 15.13.4**.

write data only appears on AD(7:0) and BC(1) is always inactive. Read data is only sampled from AD(7:0).

15.14.3.3 32-bit non-Multiplexed Memory/Peripheral Configuration

Throughout the complete external bus cycle the address[1] is driven onto Memory Controller pins A(27:0). Data (32-bit) is driven to/read back from the AD(31:0) pins during the data phase. The interconnect between Memory Controller and a 16-bit non-Multiplexed device in this mode is shown below (note: for clarity only the address/data signals are shown):-

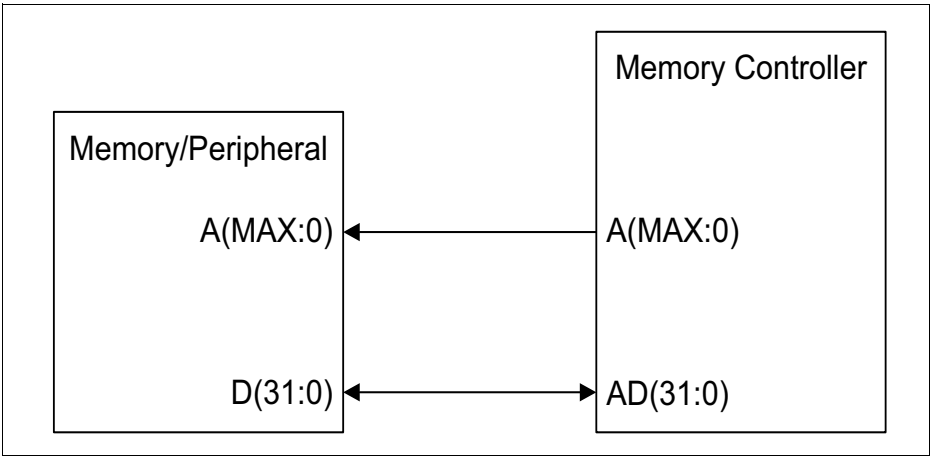


Figure 15-19 Connection of a 32-bit non-Multiplexed Device to Memory Controller

15.14.3.4 Twin, 16-bit non-Multiplexed Memory/Peripheral Configuration

Throughout the complete external bus cycle the address[2] is driven onto Memory Controller pins A(27:0). Data (32-bit) is driven to/read back from the AD(31:0) pins during the data phase. The interconnect between Memory Controller and two, 16-bit non-Multiplexed devices in this mode is shown below (note: for clarity only the address/data signals are shown):-

1) This address is pre-aligned according to the bus width as detailed in **Section 15.13.4**.

2) This address is pre-aligned according to the bus width as detailed in **Section 15.13.4**.

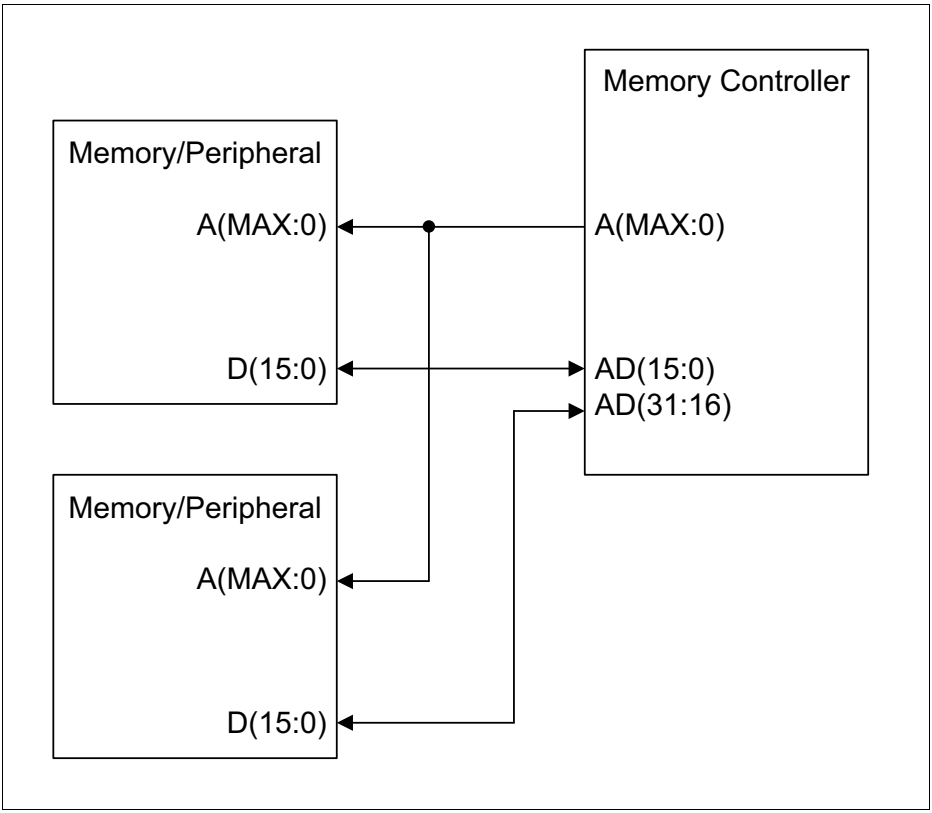


Figure 15-20 Connection of two 16-bit non-Multiplexed Devices to the Memory Controller

This mode primarily affects the mode register and status register operations for SDRAM, DDRAM and LPDDR-NVM devices. If the region is configured as twin, 16-bit, then the mode register data will be replicated on both halves of the 32 bit data bus to ensure that both the connected devices are written with an identical configuration.

15.15 Phases for Asynchronous and Synchronous Accesses

Accesses to asynchronous and synchronous devices are composed of a number of standard access phases (according to the type of device and the type of access). Each output signal for the EBU is active in defined phases. The length of the phases can be programmed to adjust the pulse width and timing relationships of the output signals

There are six access phases defined:

- Address Phase AP (mandatory for read and write cycles of both device types)
- Command Delay Phase CD (optional)
- Command Phase CP (mandatory)
- Burst Phase BP (Synchronous Accesses only)
- Control Hold CH (optional, Synchronous Accesses to DDR NOR flash only)
- Data Hold Phase DH (optional, only applies to write cycles)
- Recovery Phase RP (optional)

Throughout the remainder of this document, a short-hand notation is adopted to represent any clock cycle in any phase. This notation consists of two or three letters followed by a number. The letters identify the access phase within which the clock cycle is located (e.g. AP for Address Phase). The number denotes the number of EBU_CLK clock cycles within the phase (i.e. 1 = first, etc.). In the case of delays that can be extended by external control inputs the lower case letters “e” and “i” are inserted following the two letter phase identifier to differentiate between internally (“i”) and externally (“e”) generated delays. For example, AP2 identifies the second clock in the Address Phase. CPe3 identifies the third clock in the Command Phase which is being extended by external wait-states.

15.15.1 Address Phase (AP)

The Address Phase is mandatory. It always consists of at least one or more EBU_CLK cycles. The phase can be optionally extended to accommodate slower devices.

At the start of the Address Phase, the EBU:

- Selects the device to be accessed by asserting the appropriate $\overline{\text{CSx}}$ signal,
- Issues the address which is to be accessed on the address bus,
- For multiplexed devices, drives the address onto the muliplexed address/data bus,
- Asserts the $\overline{\text{ADV}}$ signal low,[1)]
- Asserts the appropriate $\overline{\text{BCx}}$ signals if these are programmed to be asserted with the $\overline{\text{CSx}}$ signal,
- Asserts the MR/$\overline{\text{W}}$ signal according to the type of access to be performed (low in the case of a write access, not used in burst read cycles). This level is retained until the start of the next Address Phase.
- At the end of the Address Phase the EBU returns the $\overline{\text{ADV}}$ signal to high.

The length (number of EBU_CLK cycles) of the Address Phase is programmed via the EBU_BUSAPx.ADDRC bit field parameter.

1) If an active high, ALE, signal is required, the polarity of the $\overline{\text{ADV}}$ output can be inverted by setting the ALE field of the EBU_MODCON register.

15.15.2 Address Hold Phase (AH)

The Address Hold Phase is optional. It consists of zero or more EBU_CLK cycles. It is intended to provide hold time for the multiplexed address bits after the ADV signal has returned to the inactive state.

At the end of the address hold phase, the multiplexed address can be removed from the bus:

- During a read access, the multiplexed address/data bus can return to the high impedance condition to allow the read data to be driven by the external memory
- During a write access, the write data can be driven onto the multiplexed address/data bus

15.15.3 Command Delay Phase (CD)

The Command Delay phase is optional. This means that it can also be programmed for a length of zero EBU_CLK clock cycles. The CD phase allows for the insertion of a delay between Address Phase (or optional Address Hold phase) and Command Phase(s). This phase accommodates devices that are not fast enough to receive commands immediately after getting the address or multiplexed devices which require a bus turnaround delay on reads.

The length (number of EBU_CLK cycles) of the Command Delay phase is programmed via the EBU_BUSAPx.CMDDELAY bit field. This parameter makes it possible to select between zero to seven Command Delay phases.

15.15.4 Command Phase (CP)

The Command Phase is mandatory for asynchronous devices. It always consists of at least one or more EBU_CLK cycles. The phase can optionally be extended to accommodate slower devices.

The length (number of EBU_CLK cycles) of the Command Phase is separately programmable for read and write accesses. Bit field EBU_BUSAPx.WAITRDC determines the basic length of Command Phases during read cycles and bit field EBU_BUSAPx.WAITWRC determines the basic length of Command Phases during write cycles.

Additionally, when accessing asynchronous devices, a Command Phase can also be extended externally using the WAIT signal when the region being accessed is programmed for external command delay control via bit EBU_BUSCONx.WAIT or EBU_EMUBC.WAIT.

The Command Phase is further subdivided into:

- CPi (= internally-programmed Command Phase)
- CPe (= externally-prolonged Command Phase, i.e. prolonged by the assertion of the WAIT signal).

At the start of the Command Phase, the EBU:

- Asserts the appropriate control signal $\overline{RD}$ or RD/$\overline{WR}$ low according to the access type (read or write),
- Issues the data to be written on the data bus AD[15:0] (in the case of a write cycle),
- Asserts the appropriate $\overline{BCx}$ low (in the case where $\overline{BCx}$ is programmed to be asserted with the $\overline{RD}$ or RD/$\overline{WR}$ signals).

At the end of the Command Phase during an asynchronous access, the EBU:

- Returns the appropriate control signal $\overline{RD}$ or RD/$\overline{WR}$ high according to the type of access type (read or write),
- Latches the data from the data bus AD[15:0] (in the case of a read cycle),
- Returns the appropriate $\overline{BCx}$ high (in the case where $\overline{BCx}$ is programmed to be asserted with the $\overline{RD}$ or RD/$\overline{WR}$ signals).

At the end of the Command Phase during a synchronous access, the $\overline{RD}$ or RD/$\overline{WR}$ signals hold their state and the state machine transfers to the Burst Phase. Transition to Burst Phase will always occur synchrnously with a rising edge of BFCLKO. If necessary, the Command Phase will be extended to ensure that this happens.

15.15.5 Data Hold Phase (DH)

The Data Hold phase is optional. This means that it can also be programmed for a length of zero EBU_CLK clock cycles. Furthermore, it is only available for asynchronous write accesses (with two exceptions, see below). The Data Hold phase extends the amount of time for which data is still held on the bus after the rising edge of the RD/$\overline{WR}$ signal occurred. The Data Hold phase is used to accommodate external devices that require a data hold time after the rising edge of the RD/$\overline{WR}$ signal. The length (number of EBU_CLK cycles) of the Data Hold phase is programmed via the EBU_BUSAPx.DATAC bit field.

15.15.5.1 Exceptional use of Data Hold

In two cases, signals other than the data bus may need to have a hold time maintained relative to RD/$\overline{WR}$ or $\overline{RD}$. These cases occur when $\overline{ADV}$ and $\overline{BAA}$ are being used as NAND flash control signals which happens for AGEN settings of 2_D or 13_D. For these two settings, the Data Hold Phase will apply to both reads and writes.

15.15.6 Burst Phase (BP)

The Burst Phase is mandatory during burst accesses. At the end of the Burst Phase the EBU reads data from the data bus or updates the write data. During a burst access, Burst Phases are repeated as many times as required in order to read or write the required amount of data from or to the external memory device.

At the start of the first Burst Phase during a burst read access, the EBU:

- Drives the $\overline{BAA}$ signal low to cause the Burst Flash device to advance the address with each subsequent BFCLKO positive edge.

The first burst phase of an access will always start on arising edge of BFCLKO. If necessary, the length of the previous phase will be extended to ensure that this happens.

At the end of the last Burst Phase during a burst access, the EBU:

- Returns the $\overline{BAA}$ signal high,
- Returns the $\overline{CSx}$ signal high,
- Returns the $\overline{RD}$ signal high.
- Returns the RD/$\overline{WR}$ signal high

provided that a Control Hold phase has not been programmed.

During accesses to Burst Flash devices the length of the Burst Phase will be programmed such that the end of the Burst Phase always coincides with a positive edge of the appropriate BFCLKO (Burst Flash Clock) signal.

A Burst Phase is always at least one clock cycle in length. The length of each Burst Phase (i.e. the number of EBU_CLK cycles) is derived from the value of the EXTCLOCK and EXTDATA fields in the EBU_BUSAPx register. The length of the burst phase will be either be:

- one period of BFCLKO if EXTDATA is 00_B,
- two periods of BFCLKO if EXTDATA is 01_B.
- four periods of BFCLKO if EXTDATA is 10_B.
- eight periods of BFCLKO if EXTDATA is 11_B.

15.15.7 Control Hold (CH)

The Control Hold phase applies to synchronous reads to DDR burst flash (BUSRCONx.AGEN = 9_D and BUSRCONx.AGEN = 13_D). The length of this phase will be forced to zero clocks for write accesses.

It is an optional phase designed to allow for a variable delay between the memory device clock input and the device outputs. For DDR memories, this can potentially be more than a device clock cycle.

Programming a Control Hold phase allows the active state of the RD, BAA and CSx signals to maintained while the device completes the read access.

The length of the Control Hold phase is controlled using the EBU_BUSRAPx.DATAC bitfield.

If an Control Hold phase is programmed for an ONFI 2.0 device (BUSRCONx.AGEN = 13_D), then an additional cycle of BFCLKO will be added at the end of the programmed length with $\overline{CS}$ active and all other control signals inactive. This is needed to ensure that the memory device registers an IDLE command at the end of the access and returns the DQS and AD lines to a high impedance state.

15.15.8 Recovery Phase (RP)

The Recovery Phase is optional (although for access types which would cause a bus contention a single cycle of recovery is normally forced by the memory controller logic). This means that it can also be programmed for a length of zero EBU_CLK clock cycles. This phase allows the insertion of a delay following an external bus access that delays the start of the Address Phase for the next external bus access. This permits flexible adjustment of the delay between accesses to the various external devices. The following individually programmable delays are provided on a region by region basis for the following conditions:

- Bit fields EBU_BUSAPx.RDRECOVC determine the basic length of the Recovery Phase after a read access.
- Bit fields EBU_BUSAPx.WRRECOVC determine the basic length of the Recovery Phase after a write access.
- Bit fields EBU_BUSAPx.DTACS determine the length (basic number of EBU_CLK clock cycles) of the Recovery Phase after a read/write access of one region that is followed by a read/write access of another region or a read to one region is followed by a write to the same region (BUSRAPx.DTACS) or a write to one region is followed by a read to the same region (BUSWAPx.DTACS).

The EBU implements a “highest wins” algorithm to ensure that the longest applicable recovery delay is always used between consecutive accesses to the external bus. **Table 15-19** shows the scheme for determining this delay for all possible circumstances. For example, if a read access to a region associated with $\overline{CS1}$ is followed by a write to a region associated with $\overline{CS2}$, the delay will be the highest of BUSRAP1.DTACS and BUSRAP1.RDRECOVC. In this case, if BUSRAP1.DTACS is greater than BUSRAP1.RDRECOVC, then the number of recovery cycles between the two accesses is BUSRAP1.DTACS clock cycles (minimum).

Table 15-19 Parameters for Recovery Phase

Case			Parameter(s) used to calculate "Highest Wins" Recovery Phase
Region	**Current Access**	**Next Access**	
Same $\overline{CSn}$	Read	Read	RDRECOVC
	Write	Write	WRRECOVC
	Read	Write	BUSRAPx.DTACS
	Write	Read	BUSWAPx.DTACS
Different $\overline{CSn}$	Read	Read	BUSRAPx.DTACS, RDRECOVC
	Write	Write	BUSWAPx.DTACS, WRRECOVC
	Read	Write	BUSRAPx.DTACS, RDRECOVC
	Write	Read	BUSWAPx.DTACS, WRRECOVC

15.16 Asynchronous Read/Write Accesses

Asynchronous read/write access of the EBU support the following features:

- EBU_CLK clock-synchronous signal generation
- Support for 8-bit, 16-bit and 32-bit bus width
  Performing an SRI access with a data size greater than that of the external device automatically triggers a sequence of the appropriate number of external accesses to match the SRI access width.
- Demultiplexed address/data lines
- Programmable access parameters
  - Internal control of command delay cycles
  - External and/or internal control of wait states
  - Variable data hold cycles for write operation (to allow flexible hold time adjustment)
  - Variable inactive/recovery cycles when:
    Switching between different memory regions (CS),
    Switching between read and write operations,
    After each read cycle,
    After each write cycle.

Software driver routines are required in order to support Nand Flash devices using asynchronous device accesses. A single Nand Flash access sequence is performed by generating the appropriate sequence of discrete asynchronous device accesses in software.

15.16.1 Signal List

The following signals of the EBU are used for asynchronous accesses:

Table 15-20 Asynchronous Mode Signal List

Signal/Pin	Type	Function
AD[31:0]	O	Address/Data bus lines 0-31
A[27:0]	O	Address bus lines 0-27
$\overline{\text{CS}}$[3:0]	O	Chip select 0-3
$\overline{\text{RD}}$	O	Read control line
RD/$\overline{\text{WR}}$	O	Write control line
$\overline{\text{BC}}$[3:0]	O	Byte control lines 0-3
$\overline{\text{WAIT}}$	I	Wait input
MR/$\overline{\text{W}}$	O	Read/Write signal with timimg for Motorola peripherals

15.16.2 Standard Asynchronous Access Phases

Accesses to asynchronous devices are composed of a subset of the standard access phases which are detailed in **Section 15.15**. The standard access phases for asynchronous devices are:

- AP: Address Phase (compulsory - see **Page 15-63**)
- AH: Address Hold Phase (Optional - see **Page 15-64**)
- CD: Command Delay Phase (optional - see **Page 15-64**)
- CP: Command Phase (compulsory - see **Page 15-64**)
- DH: Data Hold Phase (optional - see **Page 15-65**)
- RP: Recovery Phase (optional - see **Page 15-67**)

Figure 15-21 above shows an example of an access to a non-multiplexed device and **Figure 15-22** an example of an access to a multiplexed device.

15.16.3 Example Waveforms

The following figures show example waveforms for asynchronous accesses

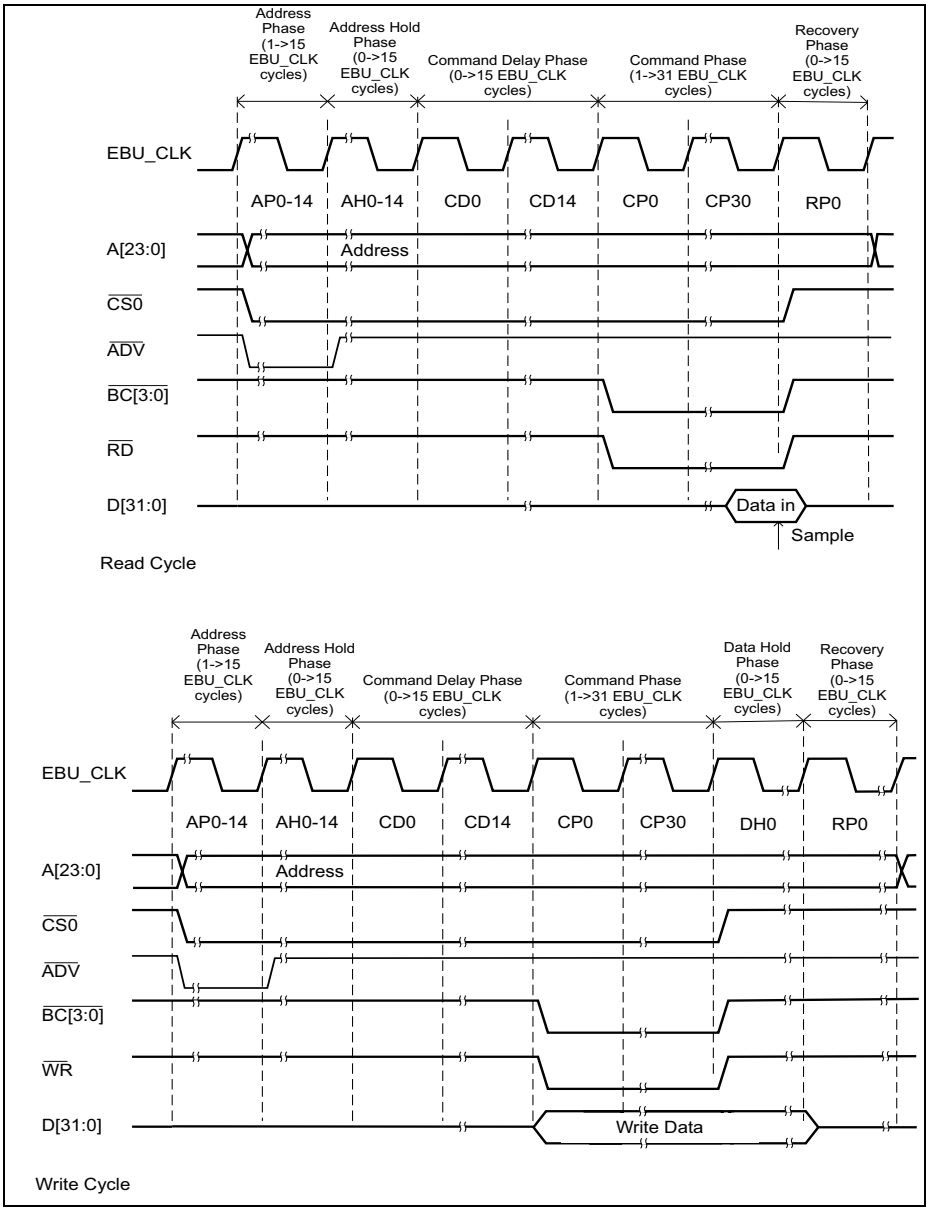


Figure 15-21 Asynchronous non-muxed Access

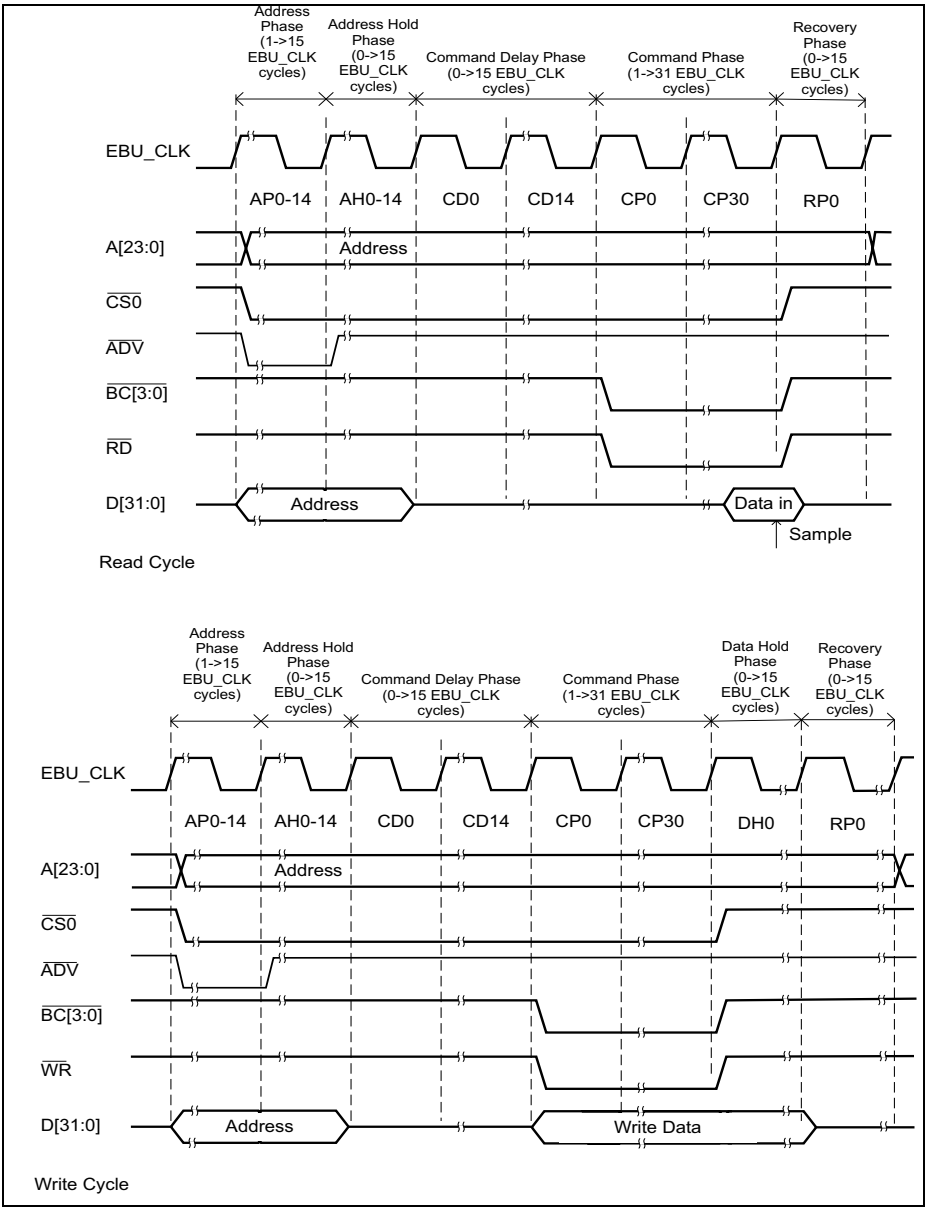


Figure 15-22 Asynchronous muxed Access

15.16.4 Control of $\overline{ADV}$ & Other Signal Delays During Asynchronous Accesses

For asynchronous accesses, the Memory Controller output signals: $\overline{ADV}$, $\overline{CS}$, $\overline{RD}$, RD/$\overline{WR}$, and $\overline{BC}$ signals can be delayed with respect to the start of the access phases they are asserted in. The amount by which the signal is delayed depends on the setting of the EBU_BUSRAPx.EXTCLOCK field of the region being addressed for read accesses and the EBU_BUSWAPx.EXTCLOCK field of the region being addressed for writes:-

- When EXTCLOCK is set to 00_B, control signals are asserted on the negative edge of EBU_CLK. i.e. they are in effect delayed by an EBU_CLK high pulse width (T_{PH})with respect to the other signals.
- When EXTCLOCK is not set to 00_B, control signals are asserted on the next positive edge of EBU_CLK. i.e. they are in effect delayed by an EBU_CLK cycle (T_{CLK}) with respect to the other signals.

The Memory Controller allows these delays to be enabled and disabled independently via the register bits EBU_BUSCONx.EBSE for $\overline{ADV}$ and EBU_BUSCONCx.ECSE for the other control signals. The default setting after reset has the delay disabled.

Table 15-21 $\overline{ADV}$ Signal Timing

EXTCLOCK is set to	ADV Falling Edge Position		ADV Rising Edge Position	
	Delay Disabled[1)]	Delay Enabled	Delay Disabled[1)]	Delay Enabled
00_B	Start of AP1	Start of AP1 + T_{PH}	Start of AP1	Start of AP1 + T_{PH}
01_B, 10_B, 11_B	Start of AP1	End of AP1	Start of AP1	End of AP1

1) See **Figure 15-21** for details of this signal positioning.

Table 15-22 $\overline{RD}$ and RD/$\overline{WR}$ Signal Timing

EXTCLOCK is set to	Set at:		Cleared at:	
	Delay Disabled[1)]	Delay Enabled	Delay Disabled[1)]	Delay Enabled
00_B	Start of CP1	Start of CP1 + T_{PH}	End of CPn[2)]	End of CPn + T_{PH}
01_B, 10_B, 11_B	Start of CP1	End of CP1	End of CPn	End of CPn + T_{CLK}

1) See **Figure 15-21** for details of this signal positioning.

2) CPn indicates the final Command Phase.

Table 15-23 $\overline{CS}$ Signal Timing

EXTCLOCK is set to	Set at:		Cleared at:	
	Delay Disabled[1)]	Delay Enabled	Delay Disabled[1)]	Delay Enabled
00_B	Start of AP1	Start of AP1 + T_{PH}	End of DHn[2)]	End of DHn + T_{PH}
01_B, 10_B, 11_B	Start of AP1	End of AP1	End of DHn	End of DHn + T_{CLK}

1) See **Figure 15-21** for details of this signal positioning.

2) DHn indicates the final Data Hold Phase. This is replaced by CPn, the final Command Phase, if the programmed Data Hold phase length is zero clocks.

The byte control signals, $\overline{BC}$x, can either use the timing in **Table 15-22** if EBU_BUSCONx.BCGEN is set to 01_B or 10_B or the timing in **Table 15-23** if EBU_BUSCONx.BCGEN is set to 00_B. A EBU_BUSCONx.BCGEN value of 11_B is not valid for asynchronous accesses.

Write data is handled differently to the other signals. Delays are never applied to the write data.

Note: If the control signals are delayed a recovery phase must be used to prevent conflicts between accesses as the rising edge of the control signals will be delayed past the end of the command phase. If a multiplexed access is used without a recovery phase, the address for the next access will be delayed by one clock cycle to enforce a bus turnaround time on the data bus, resulting in the valid address being driven one clock after $\overline{ADV}$ is asserted.

15.16.5 Programmable Parameters

Table 15-24 lists the programmable parameters for asynchronous accesses.

Table 15-24 Asynchronous Access Programmable Parameters

Register	Parameter (Bit/Bit field)	Function
EBU_BUSAPx	ADDRC	Number of cycles in address phase
	CMDDELAY	Number of programmed command delay cycles[1].
	AHOLD	Number of Cycles in Address Hold Phase[1]
	WAITRDC	Number of programmed wait states for read accesses.
	WAITWRC	Number of programmed wait states for write accesses.
	DATAC	Number of Data Hold cycles.
EBU_BUSAPx	RDRECOVC	Number of minimum recovery cycles after a read access.
	WRRECOVC	Number of minimum recovery cycles after a write access.
	DTARDWR	Number of minimum recovery cycles between a read access and a write access.
	DTACS	Number of minimum recovery cycles when the next access going to a different memory region.
EBU_BUSCONx	WAIT	External Wait State control (OFF, asynchronous, synchronous)
	WAITINV	Reversed polarity at $\overline{\text{WAIT}}$: active low or active high

1) This phase can be programmed for devices without multiplexed address and data busses but serves no purpose other than extending the access

15.16.6 Asynchronous Access Control

In general, there are only two critical phase during accesses to asynchronous devices with separate address and data buses. These phases are:

- **Command Phase** (see **Page 15-64**) which is used to control the widths of the Output Enable and Write Enable pulses. The length of the Command Phase is set by the bit fields EBU_BUSRAPx.WAITRDC and EBU_BUSWAPx.WAITWRC.
- **Data Hold Phase** (see **Page 15-65**) which is used to ensure that the write data is stable long enough to allow it to be successfully latched into the device. The length of the Command Phase is set by the bit field EBU_BUSWAPx.DATAC

As the “address to data valid” and the “chip select to data” valid parameters of asynchronous devices are usually greater than “output enable to data valid” parameter,

the lengths of the “Address”, “Address Hold” and “Command Delay” phases can be used to extend the time between the start of the access when the address and chip select are driven and the end of the Command Phase when the read or write event occurs.

For devices with a multiplexed address and data buses two additional phases control the latching of the address into the device and also critical:

- **Address Phase** (see **Page 15-63**) which is used to control the width of the $\overline{ADV}$ pulse. The length of the Address Phase is available via bit fields EBU_BUSAPx.**ADDRC**
- **Address Hold Phase** (see **Page 15-64**) which is used to ensure that the address is stable long enough to allow it to be successfully latched into the device. The length of the Address Phase is available via bit fields EBU_BUSAPx.**AHOLDC**

15.16.6.1 External Extension of the Command Phase by WAIT

The $\overline{WAIT}$ input can be used to cause the EBU to extend the Command Phase by inserting additional cycles prior to deactivation of the $\overline{RD}$ and RD/$\overline{WR}$ lines. This signal can be programmed separately for each region to be ignored or sampled either synchronously or asynchronously (selected via the EBU_BUSCONx.WAIT bit field). Additionally, the polarity of $\overline{WAIT}$ can be programmed for active low (default after reset) or active high function via bit EBU_BUSCONx.WAITINV. The signal will only take effect after the programmed number of Command Phase cycles has passed. This means that the signal can only be used to extend the phase, not to shorten it.

Table 15-25 Operation of WAIT input

Value of BUSCONx.WAIT	Mode of the $\overline{WAIT}$ input
0_D	OFF (default after reset).
1_D	Asynchronous input at WAIT.
2_D	Synchronous input at WAIT.
3_D	reserved

When programmed for synchronous operation, $\overline{WAIT}$ is sampled on every rising edge of EBU_CLK during the Command Phase. The sampled value is then used on the next rising edge of EBU_CLK to decide whether to prolong the Command Phase or to start the next phase. **Figure 15-23** shows an example of $\overline{WAIT}$ used in Synchronous Mode.

Note: Due to the one-cycle delay in Synchronous Mode between the sampling of the $\overline{WAIT}$ input and its evaluation by the EBU, the Command Phase must always be programmed to be at least one EBU_CLK cycle (via EBU_BUSAPx.WAITRDC or EBU_BUSAPx.WAITWRC) in this mode.

When programmed for asynchronous operation, WAIT is also sampled at each rising edge of EBU_CLK during the Command Phase. However, an extra synchronization cycle is inserted prior to the use of the sampled value. This means that the sampled value is not used until the second following rising edge of EBU_CLK. **Figure 15-24** shows an example of WAIT used in Asynchronous Mode.

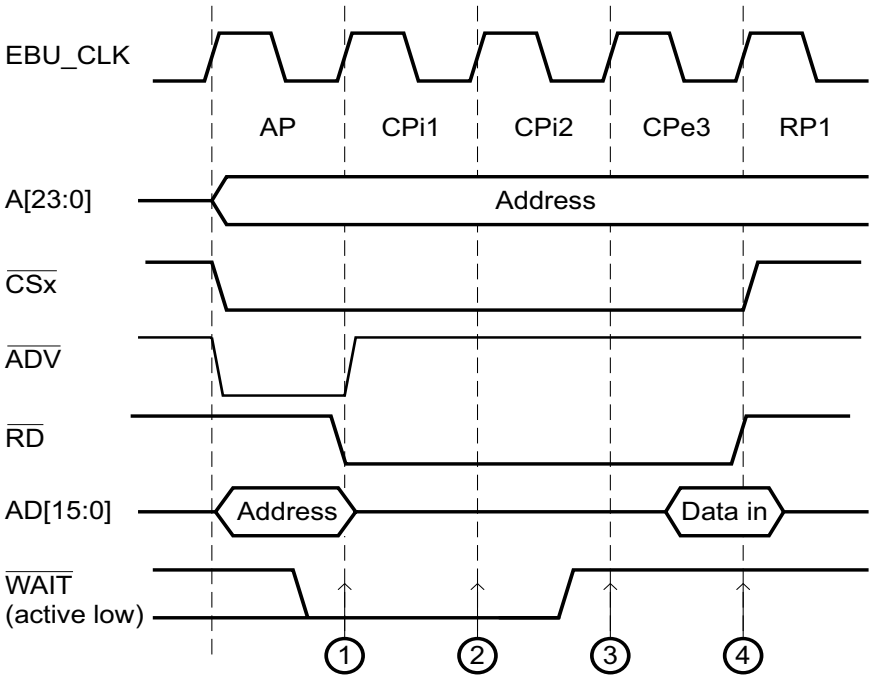
Note: Due to the two-cycle delay in Asynchronous Mode between the sampling of the WAIT input and its evaluation by the EBU, the Command Phase must always be programmed to be at least two EBU_CLK cycles (via EBU_BUSAPx.WAITRDC or EBU_BUSAP.WAITWRC) in this mode.

Figure 15-23 shows an example of the extension of the Command Phase through the WAIT input in synchronous mode:

- At EBU_CLK edge 1 (at the end of the Address Phase), the EBU samples the WAIT input as low and starts the first cycle of the Command Phase (CPi1 - internally programmed).
- At EBU_CLK edge 2, the EBU samples the WAIT input as low and starts an additional Command Phase cycle (CPe2 - externally generated) as a result of the WAIT input sampled as low at EBU_CLK edge 1.
- At EBU_CLK edge 3, the EBU samples the WAIT input as high and starts an additional Command Phase cycle (CPe3 - externally generated) as a result of the WAIT input sampled as low at EBU_CLK edge 2.
- Finally at EBU_CLK edge 4, as a result of the WAIT input sampled as high at point 3, the EBU terminates the Command Phase, reads the input data from D[31:0] and starts the Recovery Phase.

Note: Synchronous operation means that even though access to the device may be asynchronous, the control logic generating the control signals must meet setup and hold time requirements with respect to EBU_CLK.

Read Access with Synchronous $\overline{\text{WAIT}}$



Note: In the example above, the Command Delay phase is internally programmed to zero EBU_CLK cycles (no Command Delay phase).
The Command Phase is internally programmed to one EBU_CLK cycle. All other phases are programmed for one EBU_CLK cycle.

Figure 15-23 External Wait Insertion (Synchronous Mode)

Figure 15-24 shows an example of the extension of the Command Phase through the $\overline{\text{WAIT}}$ input in asynchronous mode:

- At EBU_CLK edge 1 (at the end of the Address Phase), the EBU samples the $\overline{\text{WAIT}}$ input as low and starts the first cycle of the Command Phase (CPi1 - internally programmed).

- At EBU_CLK edge 2, the EBU samples the $\overline{\text{WAIT}}$ input as low and starts the second cycle of the Command Phase (CPi2 - internally programmed).
- At EBU_CLK edge 3, the EBU samples the $\overline{\text{WAIT}}$ input as high and starts an additional Command Phase cycle (CPe3 - externally generated) as a result of the $\overline{\text{WAIT}}$ input sampled as low at EBU_CLK edge 1.
- At EBU_CLK edge 4, the EBU starts an additional Command Phase cycle (CPe4 - externally generated) as a result of the $\overline{\text{WAIT}}$ input sampled as low at EBU_CLK edge 2.
- Finally at EBU_CLK edge 5, as a result of the $\overline{\text{WAIT}}$ input sampled as high at EBU_CLK edge 3, the EBU terminates the Command Phase, reads the input data from AD[15:0],and starts the Recovery Phase.

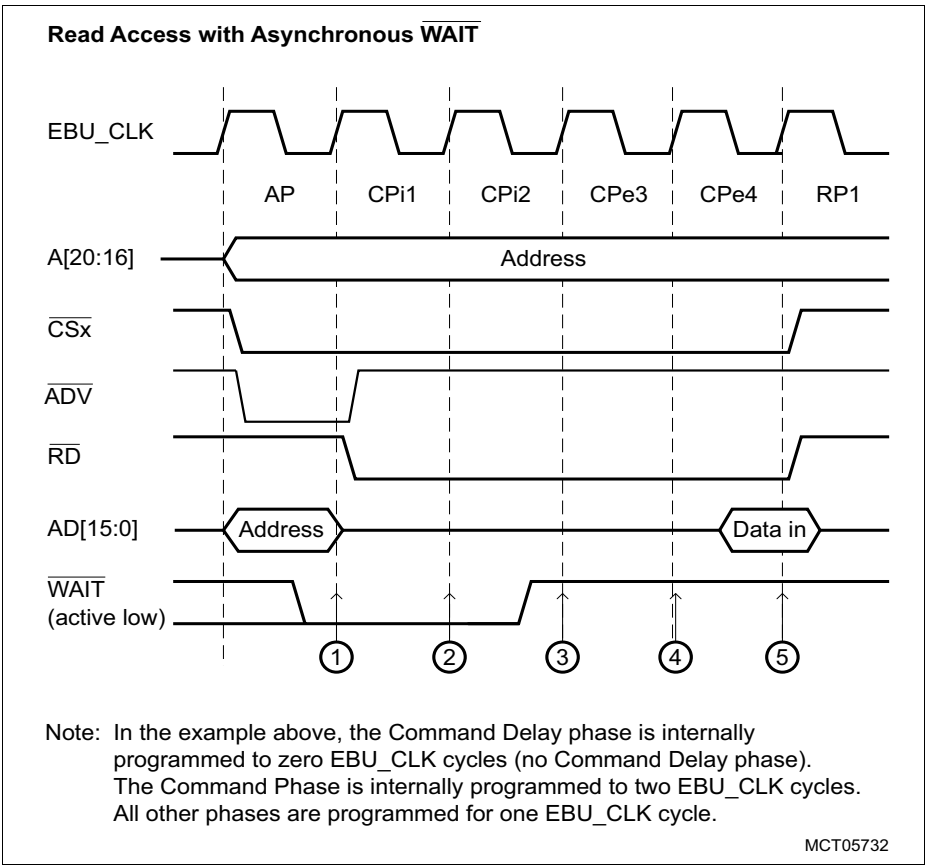


Figure 15-24 External Wait Insertion (Asynchronous Mode)

15.16.7 Interaction with DDR Signal Timing

If a DDR device is attached and **EBU_DLLCON.WR_EN** is enabled, then the write data and byte control signal timing will be affected. The storage elements used to drive the signal outputs will be operating off a shifted clock controlled by the DLL. This will shift the outputs relative to the expected timing.

For these reasons, asynchronous writes to single data rate devices when **EBU_DLLCON.WR_EN** is enabled will require additional data hold time. The recommendation is to allow an extra two clock cycles of Data Hold phase.

15.16.8 Interfacing to Asynchronous Nand Flash Devices

The memory controller provides support for specific Nand Flash devices. The required access sequences (read or write) are generated by connecting the Nand Flash device as an Asynchronous Device and using appropriate processor generated access sequences to emulate the NAND flash commands. **Figure 15-25** Shows an example of Memory Controller connected to a Nand Flash device:-

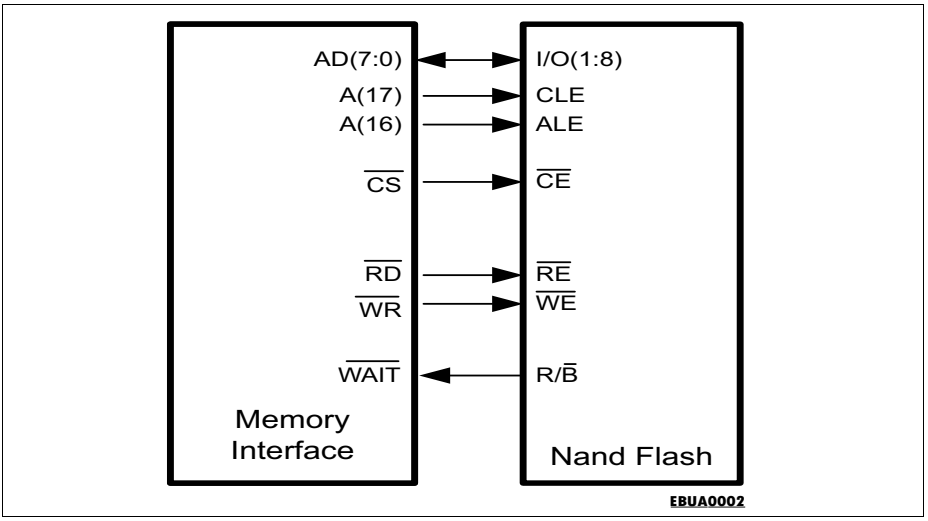


Figure 15-25 Example of interfacing a Nand Flash device to the Memory Controller

The R/$\overline{B}$ input from the NAND flash is connected to the memory controller $\overline{WAIT}$ input and is available as the EBU_MODCON.STS. This enables a NAND flash to be driven by software from the processor.

In the instance shown above two address lines are connected to the Nand Flash, and rather than being connected to address inputs, they are connected to control inputs. This allows access to three “registers” in the Nand Flash as follows:-

Table 15-26 Nand Flash "Registers" (8 bit device)

SRI Address	"Register"	Comment
Base + 00000_H	Data Register	Read/Write: Used to read data from and write data to the device.
Base + 10000_H	Address Register	Write only: Used to write the required access address to the device.
Base + 20000_H	Command Register	Write only: Used to write the required command to the device.

Note: SRI addresses are byte addresses and addresses on the external bus are word addresses. The SRI address of the virtual register will depend on the port width. of the addressed memory region. See ***"SRI Bus Width Translation" on Page 15-51***

15.16.8.1 NAND flash page mode

NAND flash memories are page oriented devices capable of extended read operations with a single setup phase for command signals at the beginning of the access. The asynchronous controller of the Memory Controller will split a large transfer into multiple accesses to external memory but each of these accesses will have the overhead of the initial setup phase. Enabling page mode, by setting the agen field in EBU_BUSCONx to 2_D, will cause the standard flow of the controller to be modified as follows:

- For a read, if data remains to be fetched at the end of a command phase, the controller will start a new command delay phase, instead of a new address phase or recovery phase and the address will not be incremented. If EBU_BUSRAPx.cmddelay is set to zero, the command delay phase will have a duration of one clock cycle but in this case the command delay phase is mandatory to ensure that the $\overline{RD}$ and RD/$\overline{WR}$ signals return to the high state.
- For a write, if data remains to be written at the end of a data hold phase (or command phase if the length of data hold is zero), the controller will start a new command phase, instead of a new address phase or recovery phase and the address will not be incremented. If EBU_BUSWAPx.datac is set to zero, the data hold phase will have a duration of one clock cycle as in this case the data hold phase is mandatory to ensure that the $\overline{RD}$ and RD/$\overline{WR}$ signals return to the high state. The command phase will be forced to have a minimum length of two clocks.

Enabling NAND flash page mode will also reconfigure the EBU signals used for ALE and CLE. While A(17:16) can still be used directly, the same values will also be output on $\overline{ADV}$ and $\overline{BAA}$.

- $\overline{ADV}$ will be used as ALE and will output the value of A(16).
- $\overline{BAA}$ will be used as CRE and will output the value of A(17).

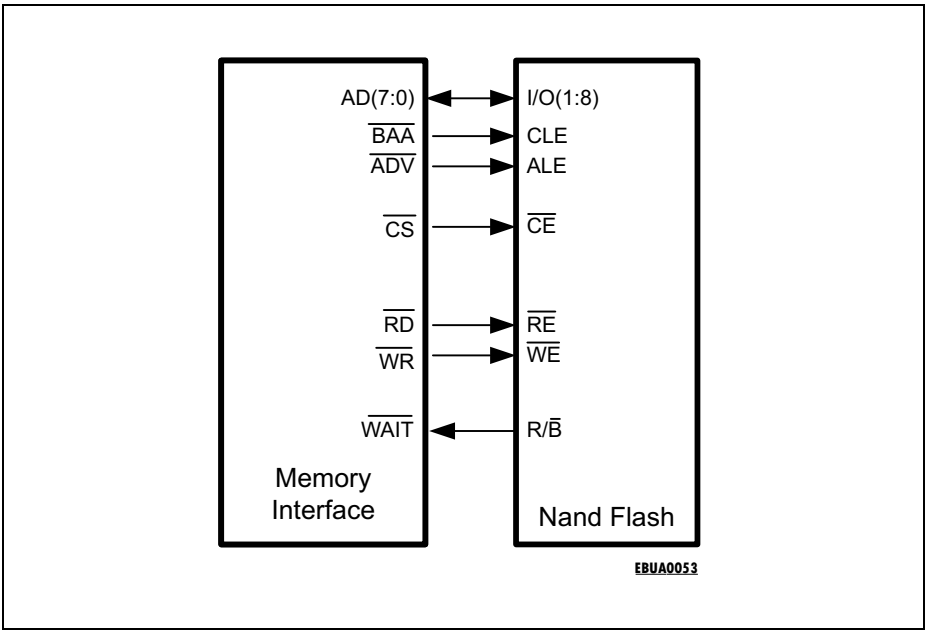


Figure 15-26 NAND Flash Connection for AGEN=3_D

To allow accesses to run consecutively without violating $\overline{\text{ADV}}$ and $\overline{\text{BAA}}$ timing restrictions, both signals will be set inactive (1_B) at the beginning of the recovery phase of the access.

See **Figure 15-27** for example waveforms.

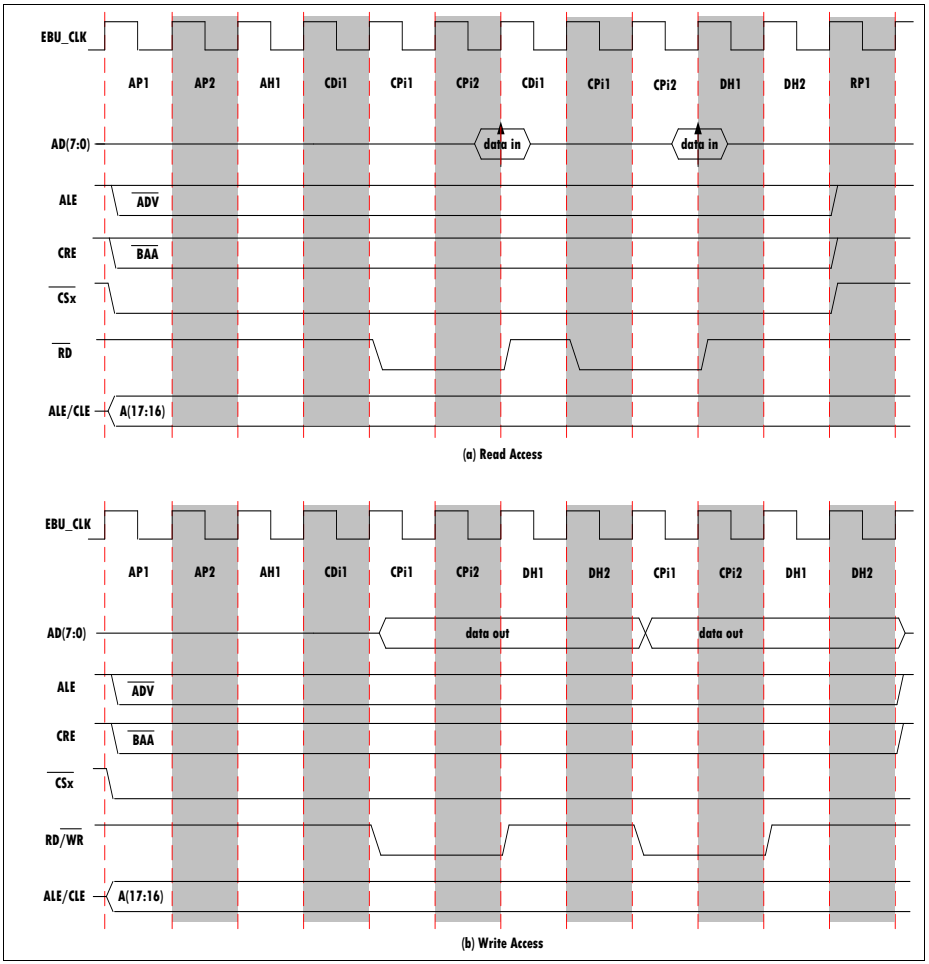


Figure 15-27 NAND Flash Page Mode Accesses

Example Nand Flash Read Sequence

Figure 15-28 shows an example of how the processor can generate a Nand Flash read access sequence given this configuration:-

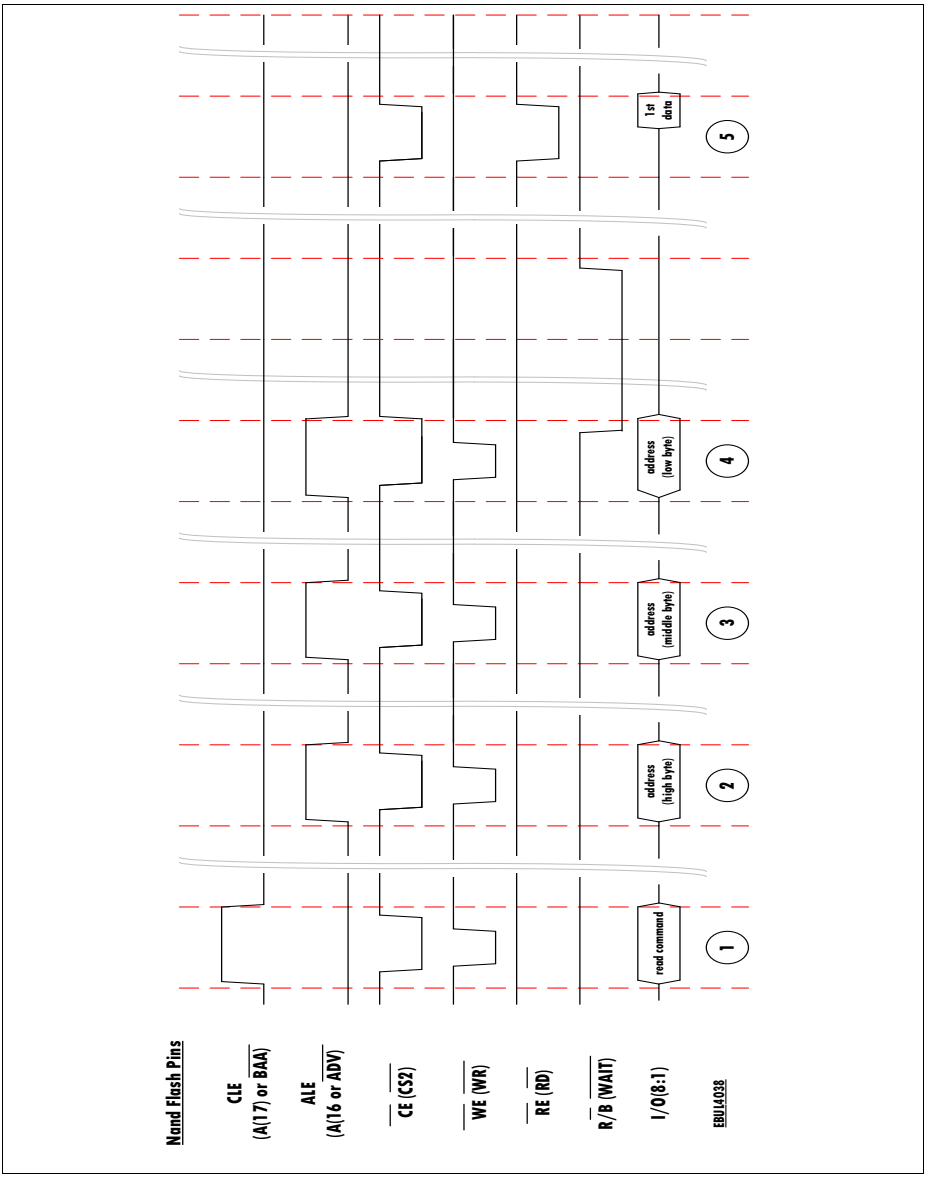


Figure 15-28 Example of an Memory Controller Nand Flash access sequence (read)

1. In the cycle marked ‘1’ in **Figure 15-28** the processor initiates a read sequence by writing the “Read Command” value to address “NAND_FLASH_BASE + 0x20000”. This generates a write sequence with CLE (A(17)) driven high and ALE (A(16)) driven low.
2. In the cycle marked ‘2’ the processor loads the most significant byte of the read address by writing to address “NAND_FLASH_BASE + 0x10000”. This generates a write sequence with CLE (A(17)) driven low and ALE (A(16)) driven high.
3. In the cycle marked ‘3’ the processor loads the middle significant byte of the read address by repeating the access specified in ‘2’ above.
4. In the cycle marked ‘4’ the processor loads the least significant byte of the read address by repeating the access specified in ‘2’ above. The Nand Flash responds to this final address byte by driving it’s R/$\overline{B}$ output low. The processor monitors this pin (using the EBU_MODCON.sts bit) until the Nand Flash has completed it’s internal data fetch.
5. In the cycle marked ‘5’ the processor reads the first byte of data by reading address “NAND_FLASH_BASE + 0x00000”. The processor can subsequently read any additionally required (sequential) data bytes by repeating cycle ‘5’.

Note: A similar scheme can be used to generate write access sequences.

15.17 Synchronous Read/Write Accesses

The Memory Controller is designed to generate waveforms compatible with the burst modes of:

1. INTEL and compatible burst flash devices
2. SPANSION and compatible burst flash devices
3. INFINEON and MICRON cellular RAM
4. Fujitsu and Compatible FCRAM/uTRAM/CosmoRAM
5. Samsung OneNAND burst capable NAND flash and compatible devices
6. M-Systems DiskOnchipG3 and compatible devices
7. GSI SSRAM
8. DDR burst flash (XIP)
9. ONFI 2.0 NAND flash

Note: Not all of the supported synchronous memory types are known to be available in automotive grade

Features

The Synchronous Access Controller is primarily designed to perform burst mode read and write cycles for an external instruction memories, external Cellular RAM and FCRAM data memories. In general, the features are:-

- Fully synchronous timing with flexible programmable timing parameters (address cycles, read wait cycles, data cycles).
- Programmable $\overline{WAIT}$ function.

- Programmable burst (mode and length)
- 8-bit device width.
- 16-bit device width.
- 32-bit device width
- Page mode read accesses.
- Resynchronisation of read data to a feedback clock to maximise the frequency of operation (optional).
- DDR device support

15.17.1 Signals

The following signals are used for the Burst FLASH interface:-

Table 15-27 Burst Flash Signal List

Signal	Type	Function
AD(31:0)	I/O	Multiplexed Address/Data bus
$\overline{RD}$	O	Read control
$\overline{WR}$	O	Write control
A(27:0)	O	Address bus
$\overline{ADV}$	O	Address valid strobe
$\overline{WAIT}$	I	Wait/terminate burst control
$\overline{CS}$(3:0)	O	Chip select
BFCLKO	O	Burst FLASH Clock, running equal to, 1/2, 1/3 or 1/4 of the frequency of EBU_CLK.
BFCLKI	I	Burst FLASH Clock Feedback.
$\overline{DDRCLKO}$	O	Negative phase of differential DDR clock
$\overline{BAA}$	O	Advance Burst Address
STS	I	Burst FLASH Status Input (Optional, value of $\overline{WAIT}$ pin available through status register)
MR/$\overline{W}$	O	Read/Write signal for Motorola type peripherals
OCLKO	O	Clock signal for ONFI2 memory devices. Output on the $\overline{WR}$ pin

15.17.2 Support for four Burst FLASH device types

Support is provided for a maximum of four different Burst FLASH configurations on the external bus - i.e. one on each external chip select.

Bit-fields EBU_BUSCONx.EBSE, EBU_BUSCONx.ECSE, EBU_BUSCONx.wait, EBU_BUSCONx.FBBMSEL, EBU_BUSCONx.BFCMSEL and

EBU_BUSCONx.FETBLEN are used to configure specific characteristics for burst access cycles.

15.17.3 Typical Burst Flash Connection

The figure below shows a typical burst flash connection.

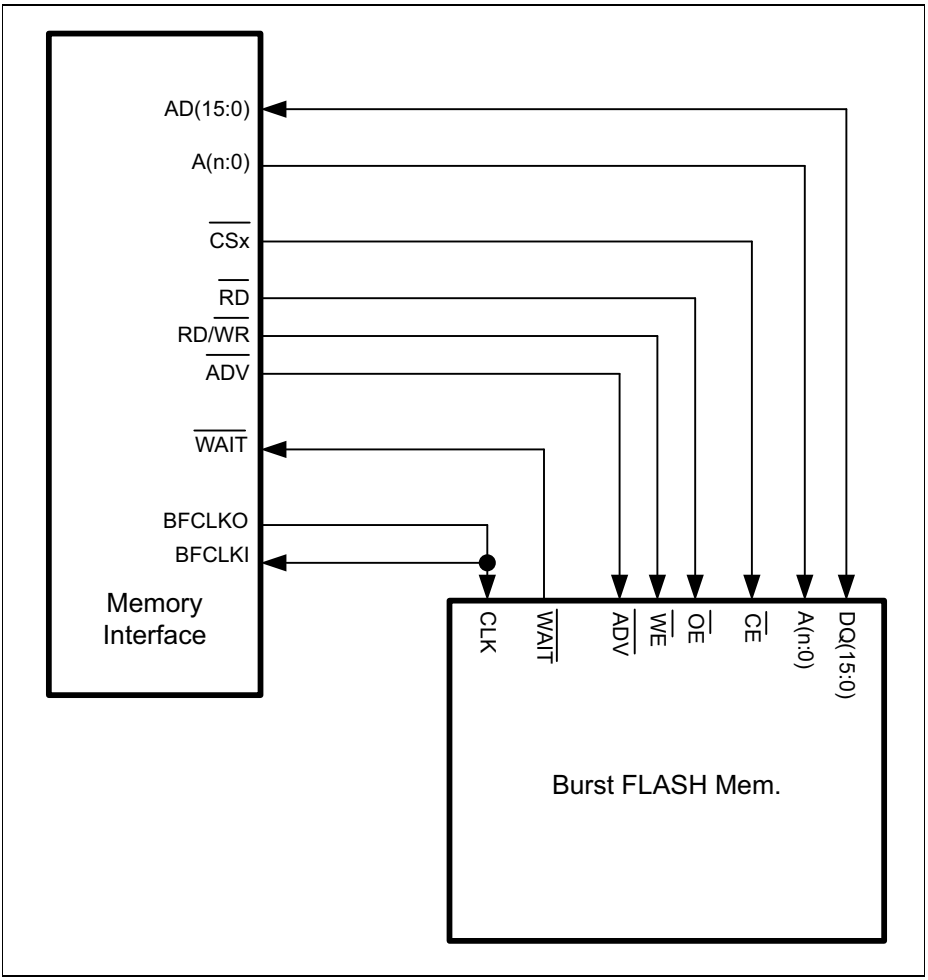


Figure 15-29 Typical Burst Flash Connection

15.17.4 Standard Access Phases

Accesses to burst FLASH devices are composed of a number of “Standard Access Phases” (which are detailed in **Section 15.15**). The Standard Access Phases for Burst FLASH devices are:-

- AP: Address Phase (compulsory - see **“Address Phase (AP)” on Page 15-63**).
- AH: Address Hold Phase (optional see **“Address Hold Phase (AH)” on Page 15-64**).
- CD: Command Delay Phase (optional - see **“Command Delay Phase (CD)” on Page 15-64**).
- CP: Command Phase (optional - see **“Command Phase (CP)” on Page 15-64**).
- BP: Burst Phase (compulsory - see **“Burst Phase (BP)” on Page 15-65**).
- CH: Command Hold Phase (optional - see **“Control Hold (CH)” on Page 15-66**)
- RP: Recovery Phase (optional - see **“Recovery Phase (RP)” on Page 15-67**).

Note: During a burst access the Burst Phase (BP) is repeated the required number of times to complete the burst length.

See **Figure 15-30** for an example synchronous access to a non-multiplexed device and **Figure 15-31** for an example synchronous access to a multiplexed device.

15.17.5 Example Waveforms

The following figures show example waveforms for synchronous accesses

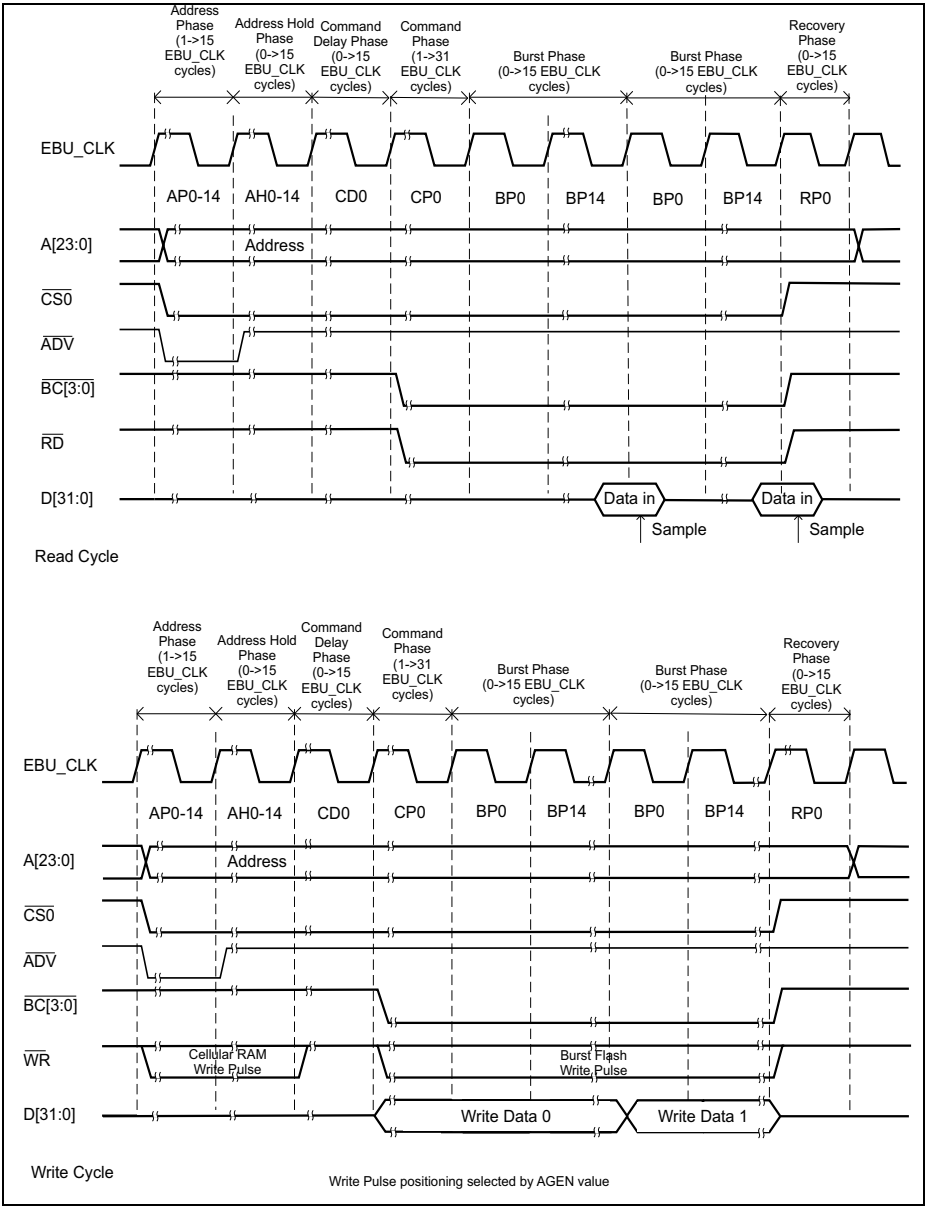


Figure 15-30 Synchronous non-muxed Access

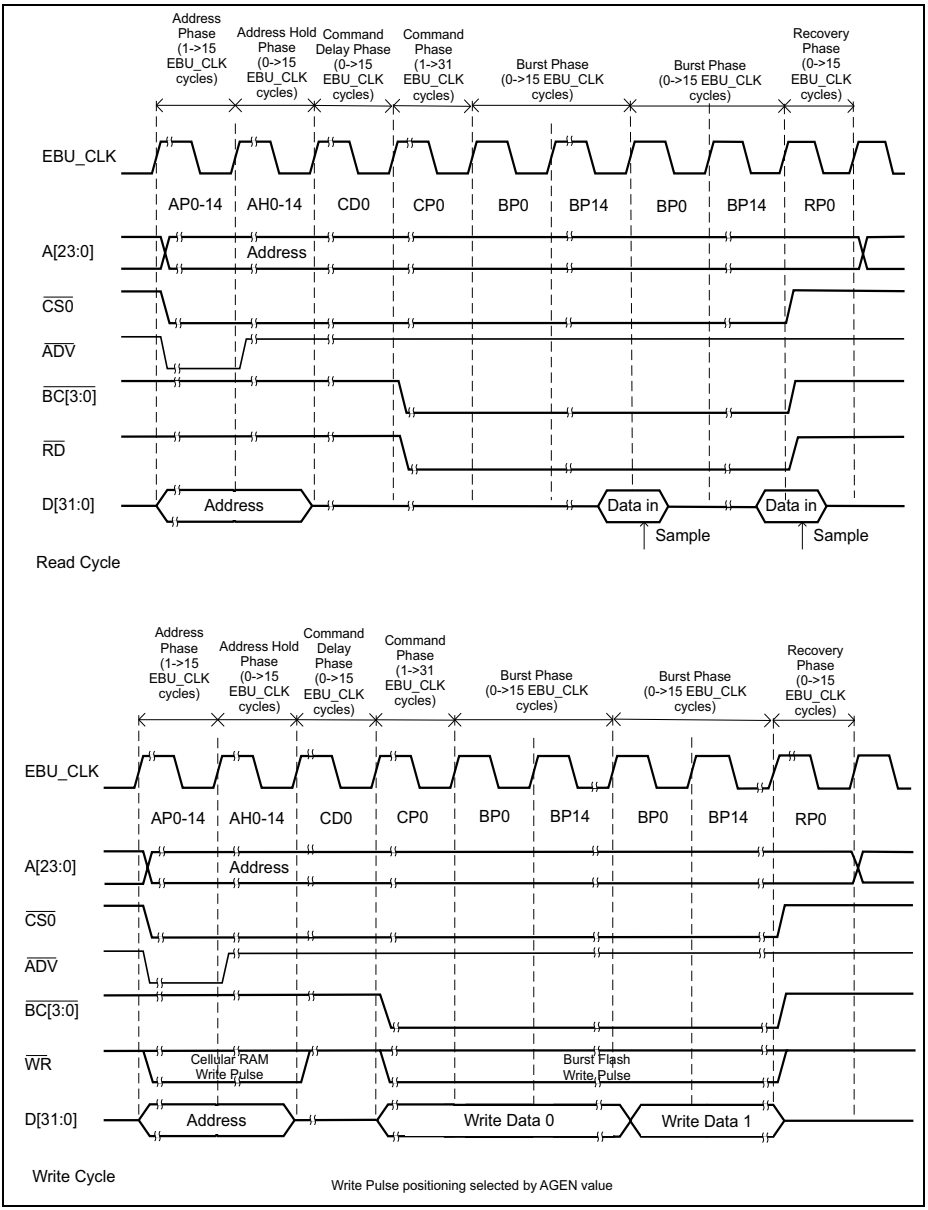


Figure 15-31 Synchronous muxed Access

15.17.6 Burst Length Control

The maximum number of valid data samples that can be generated by a flash device in a single read access is set by the EBU_BUSCONx.FBBMSEL bit and the EBU_BUSCONx.FETBLEN bit field.

The EBU_BUSCONx.FBBMSEL bit is used to select Continuous Burst Mode where there is no limit to the number of data samples in a burst read access.

The EBU_BUSCONx.FBBMSEL and EBU_BUSCONx.FETBLEN bit-fields are used to select the maximum number of data samples in a single access. Where an SRI request exceeds the amount of data that can be fetched or stored by the programmed number of data samples, the EBU will automatically generate the appropriate number of burst accesses to transfer the required amount of data.

Note: Selection of Continuous Burst Mode (by use of the 'FBBMSEL' bit) overrides the maximum burst setting (specified by the FETBLEN bit-field).

15.17.7 Burst Flash Clock

Since the EBU_CLK can run too fast for clocking Burst FLASH devices, the Memory Controller provides an additional clock source (BFCLKO). This signal is generated by a programmable clock divider driven by EBU_CLK and allows EBU_CLK to BFCLKO ratios of 1:1, 2:1, 3:1 and 4:1 to be selected. The frequency of the signal is determined by bit-field EBU_BUSRP.EXTCLOCK. Note that it is possible to set a different clock rate for synchronous writes to the same device by programming EBU_BUSWP.EXTCLOCK to a different value.

If a continuously running BFCLKO is required, then the BUSRCONx.BFCMSEL field can be used to enable an ungated flash clock. This bit is normally set to 1_B in all the BUSRCONx registers after reset. If cleared, the related BUSRAPx.EXTCLOCK field will be used to generate a stable BFCLKO. If multiple BUSRCONx.BFCMSEL fields are set to 0_B, then the highest priority (lowest index) BUSRAPx.EXTCLOCK field will be used.

During a burst access to a synchronous device, BFCLKO will generate correctly aligned clock edges as shown in **Figure 15-32**. The BFCLKO signal is gated to ensure that it is low (zero) at all other times (including asynchronous read/writes of/to synchronous devices). This provides power savings and ensures correct asynchronous accesses to Burst FLASH device(s).

The start of the address and burst phases are synchronised, by hardware, to the rising edge of BFCLKO. Exiting from a phase extended by the WAIT input will also be synchronised to the rising edge of BFCLKO.

Attaching DDR memory devices to the memory controller will impose additional restrictions on external bus clock generation. See **"External Bus Clock Generation" on Page 15-26**

Note: The length of the standard accesses phases during Burst FLASH accesses are programmed as a multiple of EBU_CLK independent of the BFCLKO frequency. It is the users responsibility to program the access phases to ensure that the sampling of data by Memory Controller guarantees valid sampling of the data from the Burst FLASH device.

The EBU uses the EBU_CLK clock to generate all external bus access sequences.

Table 15-28 EXTCLOCK to clock ratio mapping

EXTCLOCK value	BFCLKO divide ratio
00	1:1
01	1:2
10	1:3
11	1:4

Unless documented elsewhere, all outputs to the external bus are generated of the rising edge of EBU_CLK.

The BFCLKO phase is controlled so that control signal changes will normally occur at the rising edge of BFCLKO unless configured otherwise by register settings.

15.17.8 Control of $\overline{\text{ADV}}$ & Control Signal Delays During Synchronous Accesses

The Memory Controller output signals: $\overline{\text{ADV}}$, $\overline{\text{CS}}$, $\overline{\text{RD}}$, RD/$\overline{\text{WR}}$, $\overline{\text{BC}}$ and AD signals can be delayed with respect to the BFCLKO clock signal.

The delays can be enabled and disabled by the register bits EBU_BUSCONx.EBSE for the $\overline{\text{ADV}}$ signal and by EBU_BUSCON.ECSE for the $\overline{\text{CS}}$, $\overline{\text{RD}}$, RD/$\overline{\text{WR}}$, $\overline{\text{BAA}}$ and write data signals

The amount by which the signal is delayed depends on the ratio of EBU_CLK to the Burst FLASH clock as follows:-

- When the ratio of EBU_CLK to BFCLKO is 1:1, signals are asserted on the negative edge of EBU_CLK. i.e. it is in effect delayed by an EBU_CLK high pulse width (T_{PH}) with respect to BFCLKO.
- When the ratio of EBU_CLK to BFCLKO is 1:2 or 1:3, control signals are asserted on the next positive edge of EBU_CLK. i.e. it is in effect delayed by an EBU_CLK cycle (T_{CLK}) with respect to BFCLKO.
- When the ratio of EBU_CLK to BFCLKO is 1:4, control signals are asserted on the negative edge of BFCLKO. i.e. it is in effect delayed by two EBU_CLK cycles (2*T_{CLK}) with respect to BFCLKO.

- If the access is to a Cellular RAM (BUSWCONx.AGEN=3_D or 7_D), then the RD/$\overline{WR}$ signal is treated as a qualifier to the address and its timing will therefore not be affected by the setting of EBU.BUSWCON.ECSE.

For read accesses the EXTCLOCK field used will be from the BUSRAPx register of the region being accessed. For write accesses the EXTCLOCK field used will be from the BUSWAPx register of the region being accessed. However if a continuous BFCLKO is being generated (BUSRCONx.BFCMSEL=0_B), for all accesses, the EXTCLOCK value from the register with BFCMSEL set to 0_B will be used when calculating delays. This ensures that the signals are always delayed correclty relative to the clock on the BFLCKO output.

The default setting after reset has the delays disabled.

If the delay is disabled, then the signals will not be delayed in 1:1 mode (except for ADV which will be guaranteed to be after the edge of BFCLKO). In 2:1, 3:1 and 4:1 mode, the signals will be delayed by an EBU_CLK high pulse width (T_{PH}) from the start of the cycle in which they are asserted.

Table 15-29 $\overline{ADV}$ Signal Timing

EXTCLOCK is set to	$\overline{ADV}$ Falling Edge position		$\overline{ADV}$ Rising Edge position	
	Delay Disabled[1]	Delay Enabled	Delay Disabled[1]	Delay Enabled
00_B	Start of AP1	Start of AP1+T_{PH}	End of APn	End of APn+T_{PH}
01_B, 10_B	Start of AP1+T_{PH}	End of AP1	End of APn+T_{PH}	End of APn+ T_{CLK}
11_B	Start of AP1+T_{PH}	End of AP1 + T_{CLK}	End of APn+T_{PH}	End of APn + 2*T_{CLK}

1) See **Figure 15-30** for details of this signal positioning.

Table 15-30 $\overline{RD}$ and RD/$\overline{WR}$ Signal Timing

EXTCLOCK is set to	Set at:		Cleared at:	
	Delay Disabled[1]	Delay Enabled	Delay Disabled	Delay Enabled
00_B	Start of CP1	Start of CP1 + T_{PH}	End of CPn[2]	End of CPn + T_{PH}

Table 15-30 $\overline{RD}$ and RD/$\overline{WR}$ Signal Timing (cont'd)

EXTCLOCK is set to	Set at:		Cleared at:	
	Delay Disabled[1)]	**Delay Enabled**	**Delay Disabled**	**Delay Enabled**
01_B, 10_B	Start of CP1 + T_{PH}	End of CP1	End of CPn + T_{PH}	End of CPn + T_{CLK}
11_B	Start of CP1 + T_{PH}	End of CP1 + T_{CLK}	End of CPn + T_{PH}	End of CPn + 2*T_{CLK}

1) See **Figure 15-30** for details of this signal positioning.

2) CPn indicates the final Command Phase.

Table 15-31 $\overline{CS}$ Data Signal Timing

EXTCLOCK is set to	Set at:		Cleared at:	
	Delay Disabled[1)]	**Delay Enabled**	**Delay Disabled**	**Delay Enabled**
00_B	Start of AP1	Start of AP1 + T_{PH}	End of DHn[2)]	End of DHn + T_{PH}
01_B, 10_B	Start of AP1 + T_{PH}	End of AP1	End of DHn + T_{PH}	End of DHn + T_{CLK}
11_B	Start of AP1 + T_{PH}	End of AP1 + T_{CLK}	End of DHn + T_{PH}	End of DHn + 2*T_{CLK}

1) See **Figure 15-30** for details of this signal positioning.

2) DHn indicates the final Data Hold Phase. This is replaced by CPn if the programmed Data Hold phase length is zero clocks.

The byte control signals, $\overline{BC}$x, can either use the timing in **Table 15-30** if EBU_BUSCONx.BCGEN is set to 01_B or 10_B or the timing in **Table 15-31** if EBU_BUSCONx.BCGEN is set to 00_B. A EBU_BUSCONx.BCGEN value of 11_B is not valid for synchronous accesses.

Table 15-32 Write Data Signal Timing

EXTCLOCK is set to	Data Driven at:		Data Cleared at:		Data Changes at:	
	Delay Disabled[1)]	Delay Enabled	Delay Disabled	Delay Enabled	Delay Disabled	Delay Enabled
00_B	Start of CP1	Start of CP1 + T_{PH}	End of DHn[2)]	End of DHn + T_{PH}	Start of BP1	Start of BP1 + T_{PH}
01_B, 10_B	Start of CP1 + T_{PH}[3)]	End of CP1[3)]	End of DHn + T_{PH}	End of DHn + T_{CLK}	Start of BP1 + T_{PH}	End of BP1
11_B	Start of CP1 + T_{PH}[3)]	End of CP1 + T_{CLK}[3)]	End of DHn + T_{PH}	End of DHn + 2*T_{CLK}	Start of BP1 + T_{PH}	End of BP1 + T_{CLK}

1) See **Figure 15-30** for details of this signal positioning.

2) DHn indicates the final Data Hold Phase. This is replaced by CPn if the programmed Data Hold phase length is zero clocks.

3) Data bus will be enabled at the start of CP1

These delay options apply to write data only. Addresses which are output on the data bus to support devices with multiplexed address and data connections are not delayed.

Note: If the control signals are delayed a recovery phase must be used to prevent conflicts between accesses as the rising edge of the control signals will be delayed past the end of the command phase. If a multiplexed access is used without a recovery phase, the address for the next access will be delayed by one clock cycle to enforce a bus turnaround time on the data bus, resulting in the valid address being driven one clock after ADV is asserted.

15.17.9 Interaction with DDR Signal Timing

If a DDR device is attached and **EBU_DLLCON.WR_EN** is enabled, then the write data and byte control signal timing will be affected. The storage elements used to drive the signal outputs will be operating off a shifted clock controlled by the DLL. This will degrade the timing margins relative to the BFCLKO output and may shift the outputs by a complete clock cycle due to the different resynchronisation stages used.

For these reasons, correct operation of synchronous writes to single data rate devices when **EBU_DLLCON.WR_EN** is enabled cannot be guaranteed and this combination of settings should be avoided.

15.17.10 Burst Flash Clock Feedback

The Memory Controller can be configured to use clock feedback to optimise the operating frequency for a given flash device. This is enabled by setting the EBU_BUSCONx.FDBKEN bit to one. With this bit enabled the first sampling stage for read data has its own clock (PD_BFCLKFEEDBK_I). This will be derived from the BFCLKO output by using a second pad (BFCLKI) to monitor the BFCLKO signal after the output pad delay.

Clock feedback should be used whenever possible as it allows the best possible performance

A side effect of using this mode is an increase in data latency by one BFCLKO cycle compared with not using clock feedback.

Note: Clock feedback will be automatically disabled for burst writes as the additional latency on the $\overline{WAIT}$ input would prevent correct operation of the memory controller.

15.17.11 Asynchronous Address Phase

As operating frequency increases, it becomes increasingly hard to avoid violating some timing parameters. The asynchronous address phase allows the address to be latched into the flash memory using the ADV signal before the clock is enabled. This is only possible if explicitly allowed by the flash data sheet.

If the EBU_BUSCONx.AAP is set, then the clock will not start until the end of the address hold phase of the access. The rising edge of the clock will always be co-incident with the transition from the address hold phase. If the address hold phase has zero length then the first rising edge of the clock will coincide with the tranistion from the address phase. If this mode is enabled a recovery phase of one BFCLK period will be enforced at the end of the previous transaction to ensure that the clock has time to turn off before the start of the next access.

Setting this mode for any region will force the clocks on all synchronous accesses to be disabled in the recovery phase. Only one clock pulse will occur during the recovery phase.

AAP mode is incompatible with the continuous clock mode and will be disabled automatically if continuous clocking is enabled by setting any BUSRCONx.BFCMSEL bit to 0_B.

15.17.12 Critical Word First Read Accesses

In the default case, the memory controller will always start a burst at the lowest address possible and wrapping of the burst data is handled internally to the memory controller. However, some burst devices implement a wrapping feature which is compatible with the wrapped bursts used by the processor cache fill requests. If this is the case, there is an

advantage to using the wrapping mode in the device as the instruction required by the processor (the critical word) can be fetched first from the external memory.

The mode is enabled by setting the EBU_BUSCONx.dba bit for the appropriate region. Once enabled, the memory controller will not align the start address for the burst and the device will be relied on to return data in the correct order. The memory controller must fetch all the data in a single burst. If the transaction is split into multiple accesses on the external bus by use of the FETBLEN field, the issued addresses will be incorrect.

Note: The cache line fill will use an SRI, BTR4 transfer. This translates to a 16 word burst for a 16 bit device. The device must therefore support a 16 word wrap setting. A 32 bit memory must support a 8 word wrap setting. The memory controller supports a 16 word burst using the continuous burst setting for FBBMSEL. Other burst opcodes must not be generated for accesses to the external memory by the system if this mode is enabled, otherwise data corruption will occur.

15.17.13 Example Burst Flash Access Cycle

The figure below shows an example burst flash access without clock feedback configured.

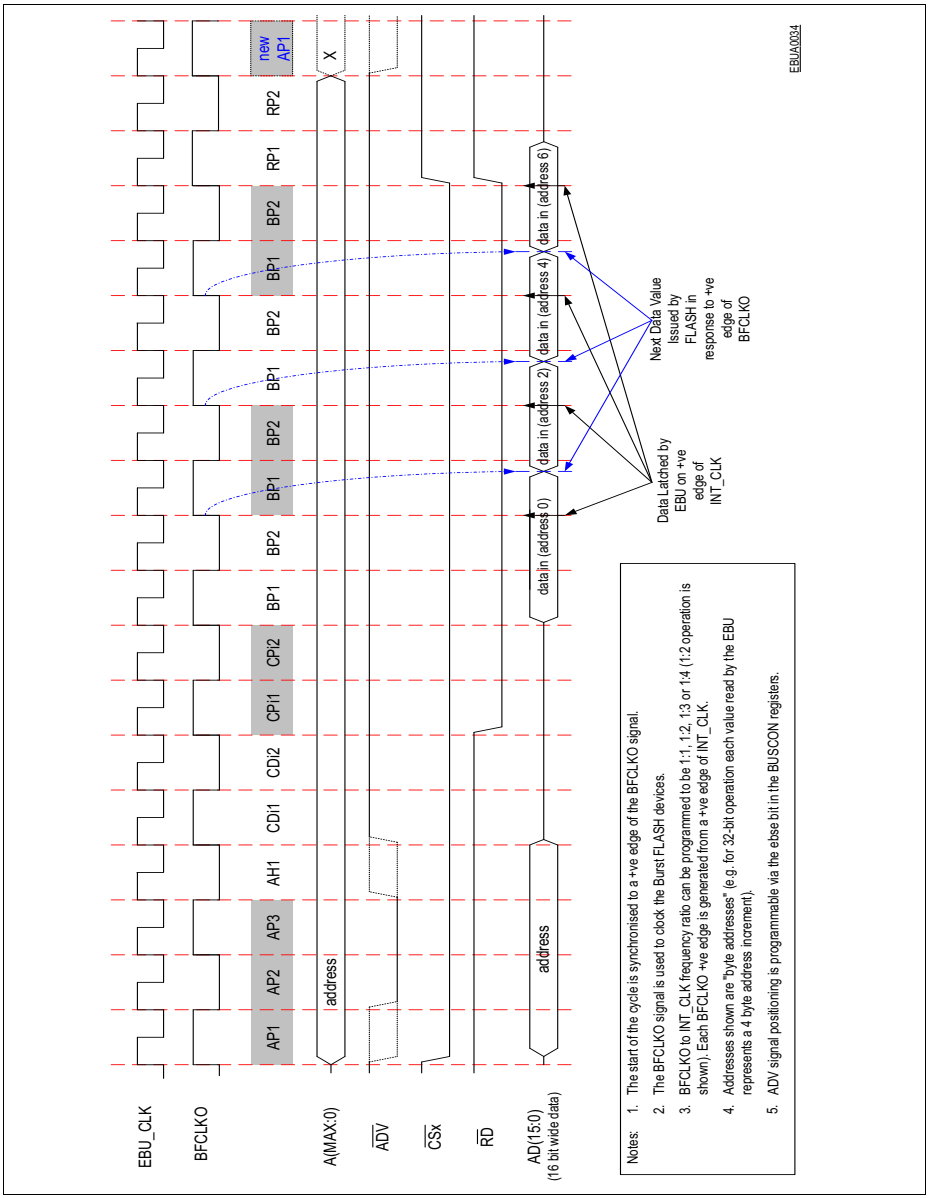


Figure 15-32 Burst FLASH Read without Clock Feedback (burst length of 4)

Figure 15-32 shows an example of a burst read access (burst length of four) to a Burst FLASH device with WAIT and clock feedback functions disabled.

Programmability of the length of the Address, Command Delay and Command phases allows flexible configuration to meet the initial read access time of a Burst FLASH device.

Data is sampled at the end of each Burst Phase cycle. The Burst Phase is repeated the appropriate number of times for the programmed burst length (programmable for lengths of 1, 2, 4 or 8 via the EBU_BUSCONx.FETBLEN bit-field).

Figure 15-32 shows an access cycle with the following settings:-

- Clock Feedback disabled.
- Address Phase length = 3 EBU_CLK cycles (see ADDRC and **"Address Phase (AP)" on Page 15-63**).
- Command Delay Phase length = 3 EBU_CLK cycles (see CMDDELAY and **"Command Delay Phase (CD)" on Page 15-64**).
- Command Phase length = 2 EBU_CLK cycles (see WAITRDC and **"Command Phase (CP)" on Page 15-64**).
- Burst Phase length = 2 EBU_CLK cycles (see EXTCLOCK, EXTDATA and **"Burst Phase (BP)" on Page 15-65**).
- Recovery Phase length = 2 EBU_CLK cycles (see **"Recovery Phase (RP)" on Page 15-67**).
- Burst Length = 4 (see FETBLEN).
- BFCLKO frequency = 1/2 of EBU_CLK frequency (see EXTCLOCK).

15.17.14 External Cycle Control via the WAIT Input

Memory Controller provides control of the Burst FLASH device via the WAIT input. This allows Memory Controller to support operation of Burst FLASH while crossing Burst FLASH page boundaries. During a Burst FLASH access the WAIT input operates in one of four modes:-

- Disabled
- Early Wait for Page Load.
- Wait for Page Load.
- Abort and Retry Access.

Selection of the mode in which the WAIT input operates during Burst FLASH reads is selected via the EBU_BUSCONx.WAIT bits.

Table 15-33 Operation of WAIT input

Value of BUSCONx.WAIT	Mode of the WAIT input
0_D	OFF (default after reset).
1_D	Wait for page load (Early WAIT).

Table 15-33 Operation of WAIT input (cont'd)

Value of BUSCONx.WAIT	Mode of the $\overline{\text{WAIT}}$ input
2_D	Wait for page load (WAIT with data).
3_D	reserved

Note: Selection of "Disabled" via the wait bit-field prevents the $\overline{WAIT}$ input having any effect on a Burst FLASH access cycle

Wait for Page Load Mode

This mode supports devices which assert a $\overline{\text{WAIT}}$ output for the duration of clock cycles in which the data output by the device is invalid or, alternatively, one clock cycle earlier than the data output is invalid. This includes Intel and AMD Burst FLASH devices (and compatibles) configured for Early Wait Generation Mode (EBU_BUSCONX.wait=01_B) and standard wait generation (EBU_BUSCONx.wait=10_B).

In operation, the burst flash controller loads a counter with the required number of samples at the start of each burst. At the end of each burst phase, the burst flash controller samples the $\overline{\text{WAIT}}$ input and the data bus at the end of each Burst phase. If $\overline{\text{WAIT}}$ is inactive, the sample is valid, the sample counter is decremented and the sampled data is passed to the datapath of the Memory Controller. This synchronous sampling means that the validity of the sample can not be determined until the clock cycle after the end of the burst phase. The Burst Flash controller will therefore overrun and generate extra burst phases until the sample counter is decremented to zero. Extra data samples returned after the sample counter is zero will be discarded.

The only difference if early wait is used is that the validity of data in burst phase "n" is determined by the value of $\overline{\text{WAIT}}$ in burst phase "n-1".

This mode of operation is compatible with the use of clock feedback as, with feedback enabled, $\overline{\text{WAIT}}$ is fed through the same resynchronisation signals as the data bus. The only effect on operation is that the number of overrun cycles will increase as the decrementing of the sample counter will be lagged by the resynchronisation stages.

During the initial phases of an access, $\overline{\text{WAIT}}$ is sampled on every edge of EBU_CLK. This is so the first burst phase is working with an accurate value for the $\overline{\text{WAIT}}$ signal. To ensure this is the case, the command phase should be of sufficient length to allow the device to drive $\overline{\text{WAIT}}$ and for the signal to propagate to the controller.

Abort and Retry Access

In this mode, the $\overline{\text{WAIT}}$ input is polled during the address and address hold phases only. If an active state on $\overline{\text{WAIT}}$ is detected, the address phase of the access will be restarted after the end of the address hold phase.

In this mode $\overline{\text{WAIT}}$ cannot be used to extend the command phase of an access.

15.17.15 Flash Non-Array Access Support

Several types of flash memories will assert $\overline{\text{WAIT}}$ permanently during an access which is not directed to the memory array. An example of this would be polling the status register to check if a programming operation has completed. If the BUSRCON[3:0].NAA field is set, then an access to the region with SRI A(26) set will proceed as if the appropriate wait field in BUSRCON[3:0] or BUSWCON[3:0] was set to 00_B and $\overline{\text{WAIT}}$ was disabled. When set, this field affects both read and write accesses.

15.17.16 Termination of a Burst Access

A burst read operation is terminated by de-asserting $\overline{\text{CSx}}$ signal followed by the appropriate length Recovery Phase. **Figure 15-33** shows an example of termination of a burst access following the read of two locations (i.e. two Burst Phases) from a 16-bit non-multiplexed Burst FLASH device.

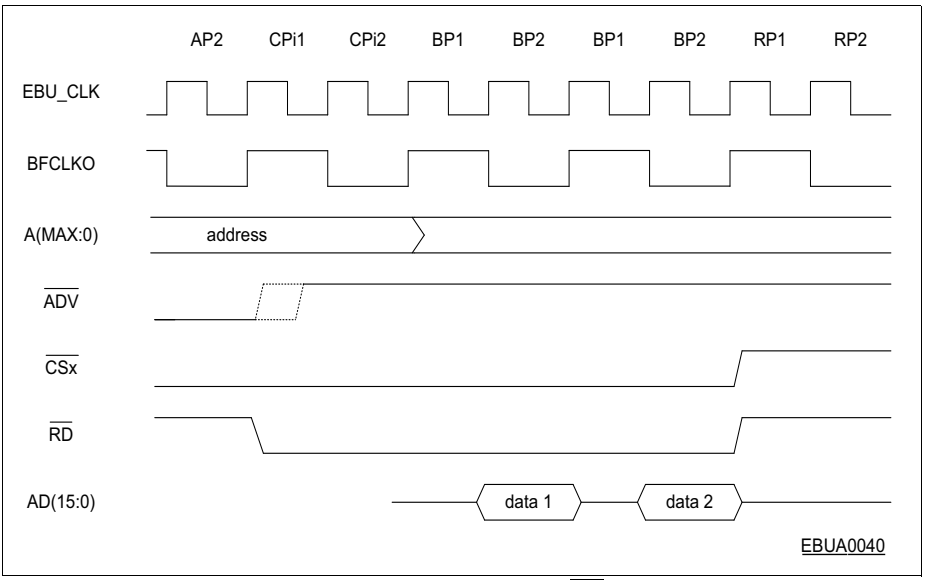


Figure 15-33 Terminating a Burst by de-asserting $\overline{\text{CS}}$

15.17.17 Burst Flash Device Programming Sequences

Programming sequences for some Burst Flash devices must not be interrupted by other read/write operations to the same device. There is an optional hardware lock feature to

guarantee that programming sequences are not interrupted. See **Section 15.9.1** for details.

15.17.18 Cellular RAM

Cellular RAM devices have been designed to meet the growing memory and bandwidth demands of modern cellular phone designs. The devices have been designed with a “multi-protocol” interface to allow use of the devices with existing memory interfaces (i.e. by re-use of existing memory protocols). The supported interface protocols supported by Cellular RAM devices are:-

1. SRAM (Asynchronous Read and Write).
2. NOR Flash (Synchronous Burst Read, Asynchronous Write).
3. Synchronous (Synchronous Burst Read and Write).

In principle, when using previous versions of Memory Controller, the first two of the above modes (1 and 2 above) provided Cellular RAM support. For maximum performance, the Memory Controller now supports Synchronous Mode (3 above) for Cellular RAM (Synchronous Burst Read and Write).

As Cellular RAM Synchronous Mode consists of a Burst FLASH compatible Burst Read access, Cellular RAM support has been provided by enhancing the Burst FLASH interface by the inclusion of a Burst Write capability. For this reason Cellular RAM is treated as a special type of Burst FLASH device.

Cellular RAM support is selected by programming the desired region as cellular RAM via the EBU_BUSCONx.AGEN bit-field.

Synchronous Read Access

A Synchronous Cellular RAM Burst Read Access is compatible with a Burst FLASH Burst Read Access. As a result preceding sections applying to Burst FLASH devices apply and should be consulted for details of Cellular RAM Burst Read Accesses.

15.17.18.1Synchronous Write Access

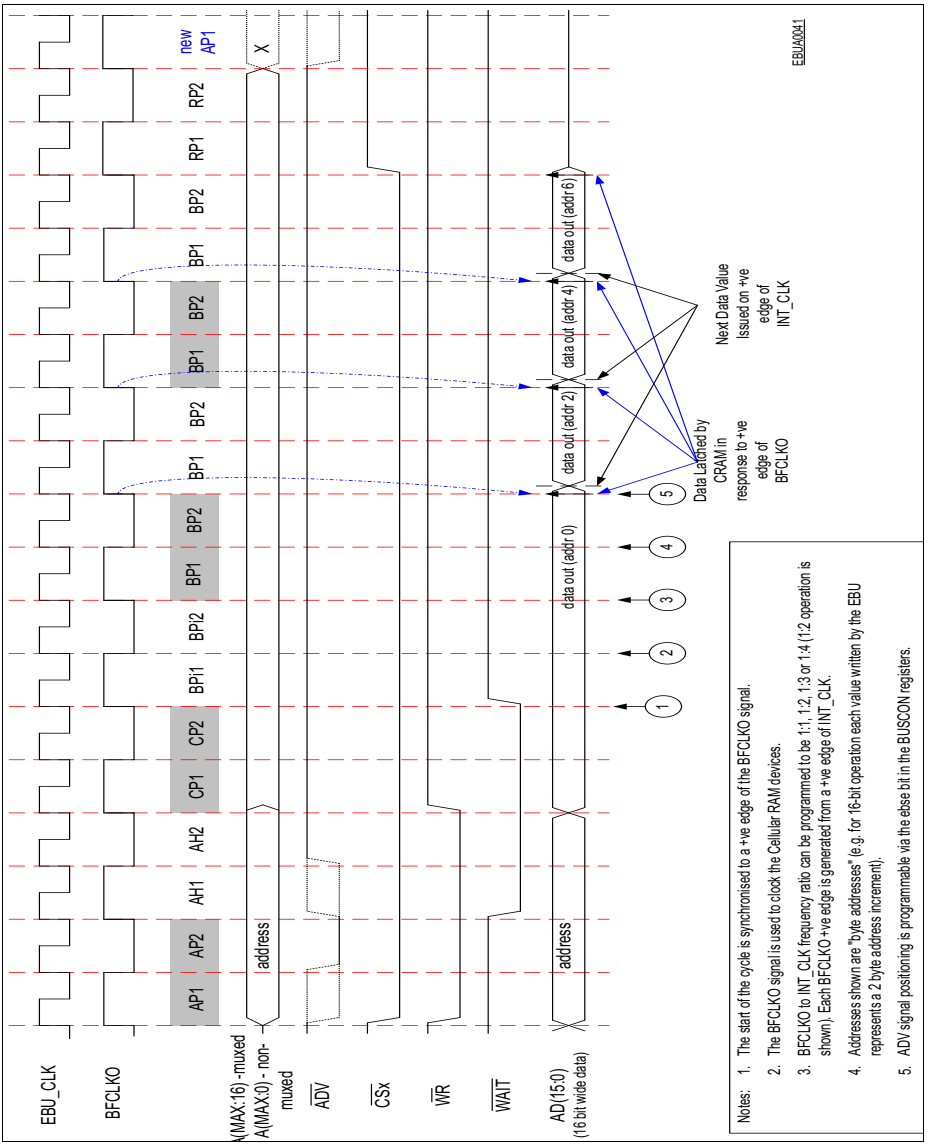


Figure 15-34 Burst Cellular RAM Burst Write Access (burst length of 4)

Figure 15-34 shows an example of a Cellular RAM burst write access.

*Note: **Figure 15-34** shows operation with a BFCLKO to EBU_CLK ratio of 1:2.*

The Start of the access cycle is the same as for a Synchronous Read access (see **Figure 15-32**) except that the WR signal is treated as an address phase signal (i.e. it is asserted active during the Address Phase and Address Hold Phase and is then deasserted). See **"Fujitsu FCRAM Support (burst write with WR active during data phase)" on Page 15-104** for alternative WR timing during burst write.

The remaining sequence is as follows (with reference to the figure above):-

1. At the positive edge of EBU_CLK labelled as '1' above the first Burst Phase starts. As the state machine is currently in the command phase, the interface samples the WAIT input. This is sampled as "active". By coincidence, in this example, the Cellular RAM also deasserts it's WAIT output as a response to this clock edge to signal that it will start to take the data from the data bus on the BFCLKO rising clock edge after the next (i.e. the rising edge of BFCLKO labelled as '5' above) - this need not be the case.
2. At the positive edge of EBU_CLK labelled as '2' above the second programmed EBU_CLK period of the Burst Phase begins.
3. At the positive edge of EBU_CLK labelled as '3' above the Burst FLASH evaluates the WAIT sample from '1' above. As this sample was "active" the write data is not updated. As this clock edge is coincident with the end of a burst phase the WAIT input is resampled. The value of this new WAIT sample is "inactive".
4. At the positive edge of EBU_CLK labelled as '5' above the Burst FLASH again evaluates the WAIT sample from '3' above. As this sample was "in-active", and the edge is coincident with the end of a burst phase, the next data value is issued to the AD(15:0) pins and the next Burst Phase is started.

This process continues until all the data is written.

15.17.18.2 Fujitsu FCRAM Support (burst write with WR active during data phase)

The FCRAM device type can be supported in two ways. Later FCRAMs have a compatibility bit in the device configuration register which programmes the device to expect the WR signal to be active with the address and to be latched with the ADV signal. In this mode, FCRAM can be treated as an Infineon/Micron cellular RAM.

Alternatively, if a write is attempted to a region configured as a burst flash, the memory controller will generate a burst write with the WR signal asserted with the write data. This should be directly compatible with an FCRAM operating in its native mode.

15.17.19 DDR Burst Flash Support

The memory controller includes features which allow the support of flash memories using a DDR data bus protocol. The memory types supported are:

- DDR NOR flash memory, supporting DDR read and write accesses

- ONFI 2.0 NAND flash

Configuring a region to support either of the memory types will enable the requisite number of DQS lines to support the attached memory.

The DQS lines will be multiplexed onto the most significant address lines as these will not be required for the supported DDR memories. Once enabled as DQS, the address lines will not be available as addresses for any devices attached to the EBU.

It is recommended that DDR flash is only used with other DDR memories due to the critical load matching requirements on the DQ/DQS/DQM lines. Mixing memory types may limit the supportable operating frequency.

DDR flash support using an BUSCONx.EXTCLOCK setting of 00_B (1:1 internal to external clock ratio) requires the use of the memory controller DLL. Other clock ratios are supported using edges of the internal clock signal to generate the signal waveforms (See **“Generation of DDR Control Signals without using the DLL” on Page 15-24**).

15.17.19.1 DDR NOR Burst Flash

DDR NOR burst flash support is configured by setting the **AGEN** fields of the BUSCONx register to 9_D. However, at present there are no devices that are known to support writes using this protocol so it is expected that the device will be configured for DDR reads and asynchrnonous writes.

Configuring support for this type of device will enable the differential BFCLK clock (See **“External Bus Clock Generation” on Page 15-26**). It will also enable the generation of addresses on the AD bus to allow support multiplexed address/data memories.

DDR NOR burst flash can have an internal PLL. If this is the case, the clock must be set to continuous mode by setting the **BFCMSEL** field of the BUSRCON register to 0_B.

Note: Once the differential clock has been enabled, there will be a delay while the PLL locks. During this delay, the device cannot be accessed synchronously.

For accesses to DDR NOR flash, the reading of data will be handled in the same way as for DDRAM. See **Chapter 15.10.4** and **Chapter 15.10.6** for a full description of the methods available.

Due to uncertainty in the read signal output timing of the attached device, read accesses will always use the full burst length programmed in the **FETBLEN** bitfield. Continuous burst mode is not available. Setting continuous burst mode using the **FBBMSEL** bitfield will result in a burst length of sixteen being programmed.

For read accesses, any unused data words will be discarded.

As the burst length of the EBU is defined in cycles of BFCLKO and the burst length of the flash may be defined in data words, there may be a mismatch for DDR devices. If the device burst length is defined in data words per read then the programmed EBU burst length must be half the burst length programmed into the device configuration register. The EBU will expect two data words per Burst Phase when accessing DDR devices.

DDR NOR flash read accesses should be extended using a Control Hold phase (**“Control Hold (CH)” on Page 15-66**). This is used to prevent the device outputs being disabled before the last data word can be output by the device. This is necessary as the worst case timing delay between the clock input to the device and the output of the DQS and data word may be great enough to move the output signals into the next clock period. Cancelling the control signals at the end of the burst phase may therefore diable the device outputs before the last data can be latched into the EBU.

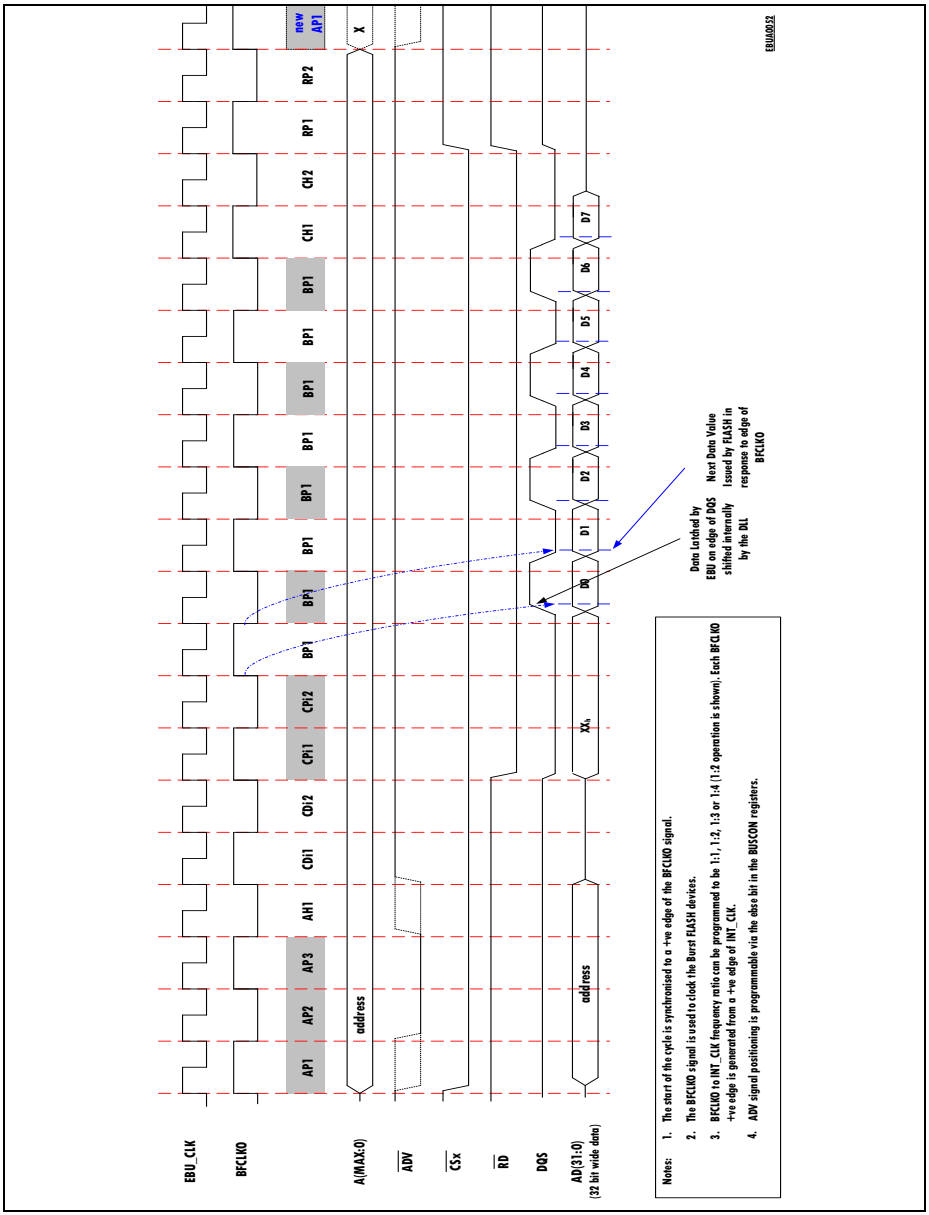


Figure 15-35 DDR NOR Burst Flash Read Cycle

15.17.19.2 ONFI 2.0 NAND Flash

The EBU can interface to NAND flash memories complying with the ONFI 2.0 specification. Initial, asynchronous, operation is handled using the AGEN value 2_D (NAND flash page mode). Once configured for synchronous operation, the AGEN field should be set to 13_D.

Connection of an eight bit device is as in below. Connection of 16 and 32 bit devices is the same with the additional AD and DQS connections. A 16 bit device will need AD(15:8) and DQS(1). A 32 bit device will also need AD(31:16) and DQS(3:2). Multiple devices can also be connected in parallel to make up a large word width.

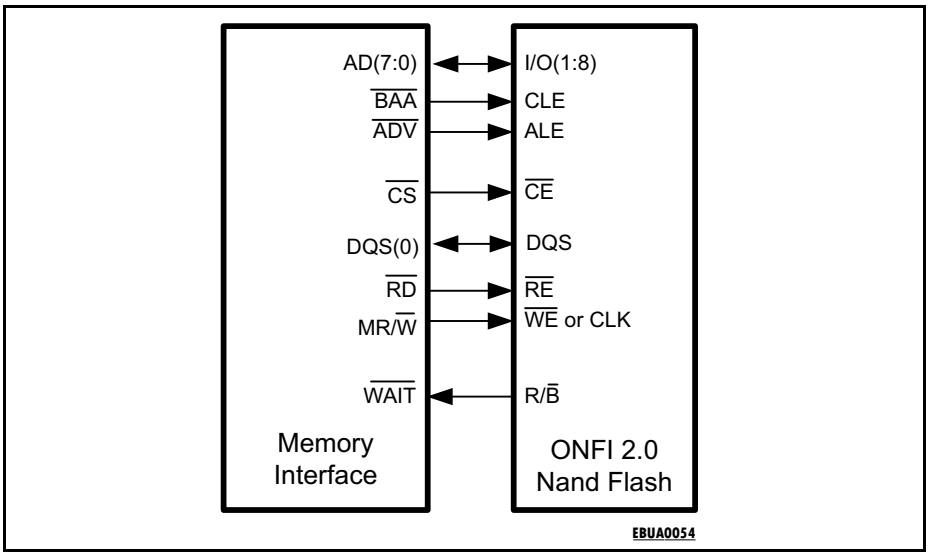


Figure 15-36 Connection of 8 bit ONFI 2.0 NAND Flash

While AGEN is set to 2_D, the state of the DQS signal(s) on a write access will be determined by A(18) of the access. This is equivalent to A_{SRI}(18) for 8 bit devices.

When AGEN is set to 13_D, the state of the DQS signal(s) during a write access will be determined by A(18) unless both A(17) ands A(16) are set to 1_B.

If A_{EBU}(17:16) is set to 11_B, a data transfer (as defined in the ONFI specification) is in progress and the DQS lines will be used to clock the data.

If AGEN is 13_D and a data transfer is not in progress then the burst length of all transfers to the device should be restricted by software to a single data phase. This is to enable the successful writes of command and address data.

Write data will be transferred at single data rate if a data transfer is not in progress as the attached device will use the clock to latch the write data and will not expect DQS.

Table 15-34 ONFI 2.0 Nand Flash Command SIgnal Control (8 bit device)

SRI Address	Signal(s) set	Asynchronous mode usage	Synchronous Mode Usage
Base + 00000_H	No command signals set	Read/Write: Used to read data from and write data to the device.	Bus Idle.[1]
Base + 10000_H	ALE	Write only: Used to write the required access address to the device.	
Base + 20000_H	CRE	Write only: Used to write the required command to the device.	
Base + 30000_H	ALE+CRE	Invalid	Data Transfer
Base + 40000_H	DQS	Read/Write: Use Base + 0000_H instead	Bus Idle
Base + 50000_H	ALE+DQS	Write only: Used to write the required access address to the device. Use Base + 10000_H instead.	
Base + 60000_H	CRE+DQS	Write only: Used to write the “set features” command to the device.	
Base + 70000_H	ALE+CRE	Invalid	Data Transfer

1) If used on a read access, the EBU will stall indefinitely waiting for read data.

Example waveforms for the ONFI 2.0 interface protocol are shown below.

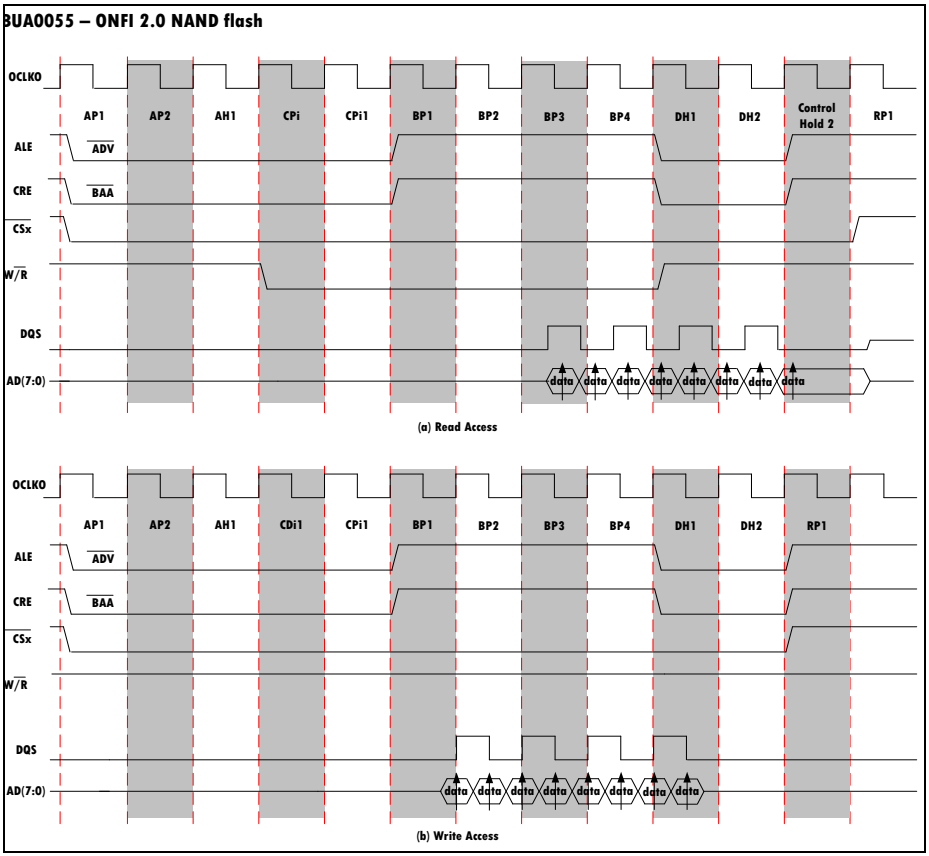


Figure 15-37 ONFI 2.0 NAND Flash: Data Transfer Cycles

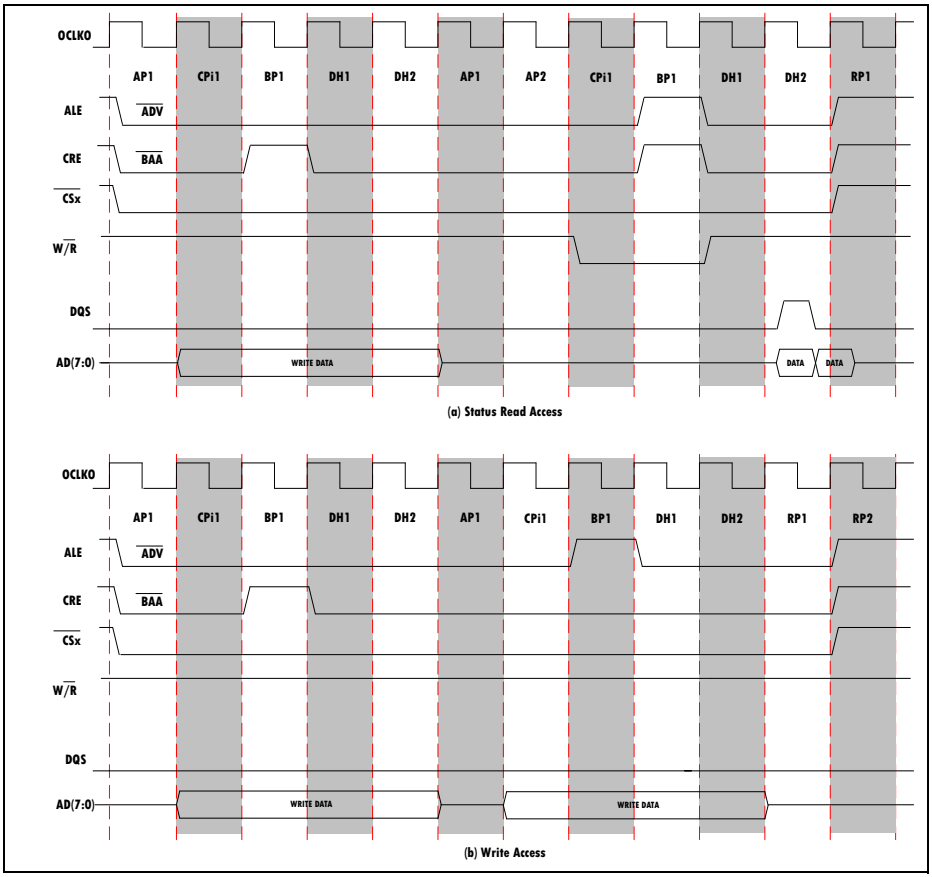


Figure 15-38 ONFI 2.0 Command Cycles

Note: The ONFI 2.0 specification does not support byte transfers to/from 16 or 32 bit devices in source synchronous mode. The EBU will translate requests for byte reads into a word read and discard the extra data. Writes, however, will always transfer 16 bits of data to the device (the superfluous data will not be masked).

15.17.20 Programmable Parameters

The following table lists the programmable parameters for burst flash accesses. These parameters only apply when the EBU_BUSCONx.agen parameter for a particular memory region is set for access to synchronous burst devices (page mode or otherwise).

Table 15-35 Burst Flash Access Programmable Parameters

Parameter	Function	Register
ADDRC	Number of cycles in Address Phase.	EBU_BUSAPx
AHOLDC	Number of cycles in Address Hold.	EBU_BUSAPx
CMDDELAY	Number of programmed Command Delay cycles.	EBU_BUSAPx
WAITRDC	Number of programmed wait states for read accesses.	EBU_BUSAPx
WAITWRC	Number of programmed wait states for write accesses.	EBU_BUSWAPx
EXTDATA	Extended data	EBU_BUSAPx
RDRECOVC	Number of minimum recovery cycles after a read access when the next access is to the same region.	EBU_BUSRAPx
WRRECOVC	Number of minimum recovery cycles after a write access when the next access is to the same region.	EBU_BUSWAPx
RDDTACS	Number of minimum recovery cycles after a read access when the next access is to a different region.	EBU_BUSRAPx
WRDTACS	Number of minimum recovery cycles after a write access when the next access is to a different region.	EBU_BUSWAPx
WAIT	Sampling of $\overline{\text{WAIT}}$ input: OFF, SYNCHRONOUS, ASYNCHRONOUS or WAIT_CELLULAR_RAM	EBU_BUSCONx
FBBMSEL	Flash synchronous burst mode: CONTINUOUS or DEFINED (as in FETBLEN)	EBU_BUSCONX
FETBLEN	Synchronous burst length: SINGLE, BURST2, BURST4 or BURST8	EBU_BUSCONx
BFCMSEL	Flash Clock Mode, continuous or gated	EBU_BUSRCONx

Table 15-35 Burst Flash Access Programmable Parameters (cont'd)

Parameter	Function	Register
EXTCLOCK	Frequency of external clock at pin OCLKO: equal, 1/2 or 1/4 of EBU_CLK	EBU_BUSAPx
EBSE	delay $\overline{ADV}$ output to improve hold margin	EBU_BUSCONx
ECSE	delay $\overline{CS}$, $\overline{WR}$ and write data outputs to improve hold margin	EBU_BUSCONx
LOCKCS	enable locked write sequences for this region	EBU_BUSWCONx
FDBKEN	enable clock feedback to improve read data margins	EBU_BUSRCONx
DBA	disable alignment of read bursts on external bus	EBU_BUSRCONx
AAP	enable the "asynchronous address phase" mode.	EBU_BUSCONx
PORTW	memory port width	EBU_BUSRCONx

Note: datac is not used for burst write accesses

15.18 SDRAM Interface

The SDRAM interface supports 16 and 32 bit bit SDRAM configurations with four banks at densities up to 1 GBit.

Please see the Intel™ PC100 specification for signalling waveforms for this interface.

The Memory Controller can support a single SDRAM region. To enable SDRAM support the **AGEN** fields of a single register pair of EBU_BUSRCON and EBU_BUSWCON must be set to "8_D".

*Note: Programming the **AGEN** fields of multiple regions for SDRAM and connecting multiple SDRAMs will result in data corruption as the "page open" tags in the SDRAM controller will be applied indiscriminately to all connected devices.*

15.18.1 Features

- Compatible with mobile PC133 memories at 125 MHz (if maximum bus load is not exceeded) when used with optimised pads.
- Mobile SDRAM support.

- Support for 64, 128, 256, 512 MBit and 1 GBit SDRAM devices.
- Auto-refresh mode support.
- Support for 16 and 32 bit bus widths.
- Power-on/mode-set sequence triggered by SRI write to **EBU_SDRMOD** configuration register.
- Programmable refresh rate.
- Programmable timing parameters (row-to-column delay, row-precharge time, mode-register setup time, initialization refresh cycles, refresh periods).
- Multiple power save modes supported
  - Clock Stop
  - power down without precharge
  - power down with Auto-precharge
  - power down with precharge
  - self refresh

15.18.2 Signal List

The following signals are used for the SDRAM interface:-

Table 15-36 SDRAM Signal List (16 bit support)

Signal	Type	Function
AD(15:0)	I/O	Data bus
A(27:0)	O	Address bus
RD/$\overline{WR}$	O	Read and write control
CKE	O	Clock enable
CS(3:0)	O	Chip select
SDCLK0	O/I	External SDRAM Clock.
SDCLKI	I	External SDRAM Clock Feedback
RAS	O	Row Address Strobe for SDRAM accesses.
CAS	O	Column Address Strobe for SDRAM accesses.
DQM(3:0)	O	Data Qualifiers (output on $\overline{BC}$(3:0))

Table 15-37 SDRAM Signal List (32 bit support)

Signal	Type	Function
AD(31:16)	I/O	Data bus MSW
AD(15:0)	I/O	Data bus LSW
A(15:0)	O	Address bus (A(27:16) not needed for SDRAM)

Table 15-37 SDRAM Signal List (32 bit support) (cont'd)

Signal	Type	Function
RD/$\overline{WR}$	O	Read and write control
CKE[1)]	O	Clock enable
CS(3:0)	O	Chip select
SDCLK0	O/I	External SDRAM Clock
SDCLKI	I	External SDRAM Clock Feedback
RAS	O	Row Address Strobe for SDRAM accesses.
CAS	O	Column Address Strobe for SDRAM accesses.
DQM(3:0)	O	Data Qualifiers (output on $\overline{BC}$(3:0))

1) Pull down resistor required to maintain a valid logic level when the EBU is not driving the bus. See **Chapter 15.18.3**

15.18.3 External Interface

The external interface can be directly connected to DRAM chips without any glue-logic. Special board layout and timing constraints may apply when additional memory/peripherals (in addition to SDRAM devices) are directly connected to the bus.

16 and 32 bit devices are supported. Additionally, two 16 bit devices connected in parallel to make a 32 bit device are also supported. In this case, the memory controller region should be configured to support a 32 bit device but with the BUSCON PORTW fields set to 10_B to indicate a twin, 16 bit configuration.

Note: The memory controller always resets to "no bus" arbitration mode and will then synchronously transition to the appropriate mode and enable the required pins based on the register settings. This means that the SDRAM specific pins will be under the control of the ports I/O logic after reset. CKE must either be driven to an appropriate value for the application by the reset value of the ports logic or held to a valid state by a pull resistor on the PCB.

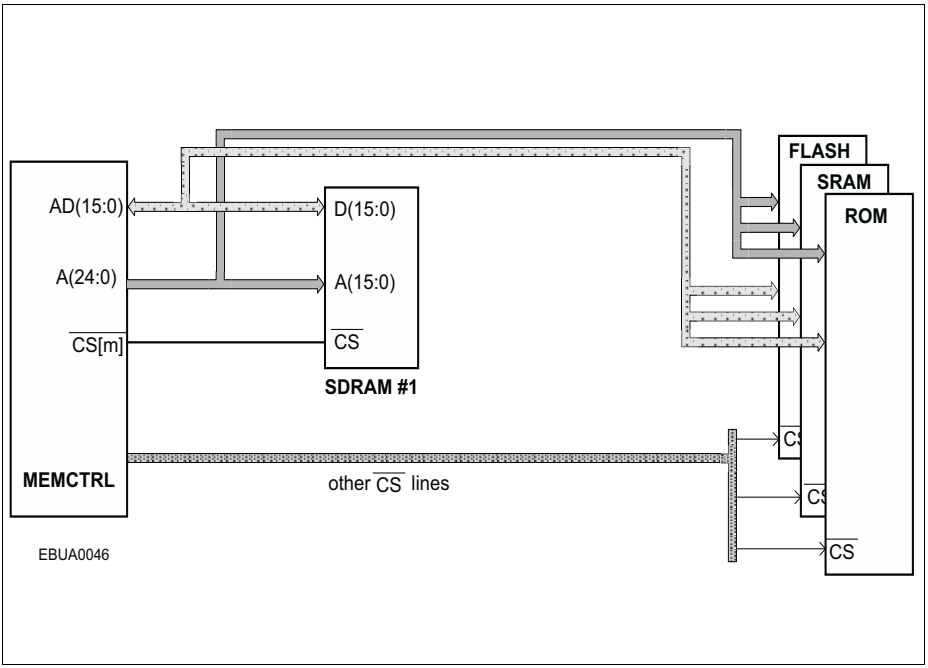


Figure 15-39 Connectivity for 16 bit SDRAM

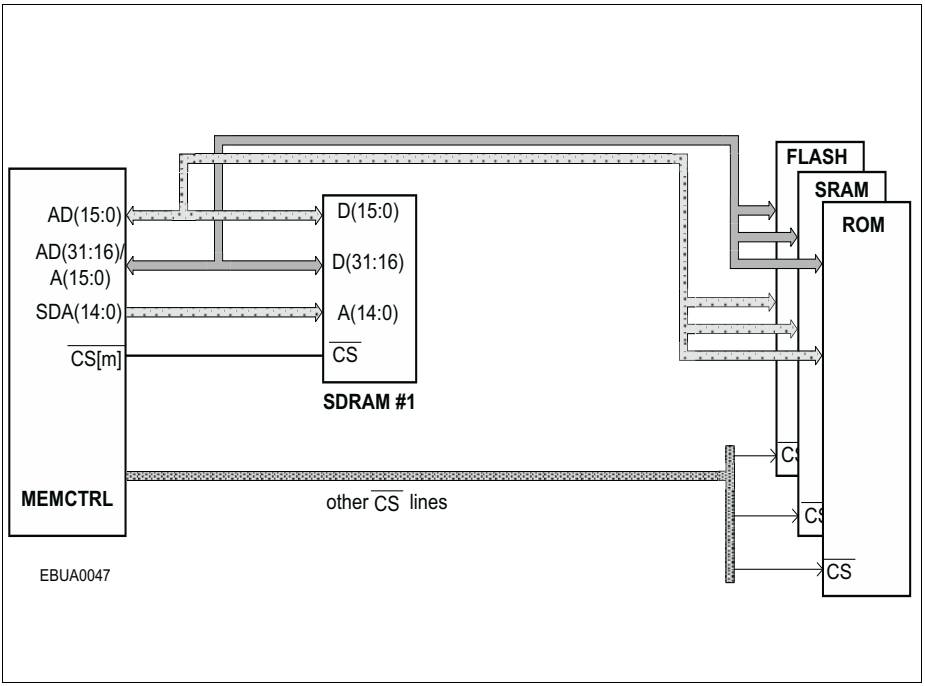


Figure 15-40 Connectivity for 32 bit SDRAM

15.18.4 SDRAM External Bus Clock Generation

The Memory Controller uses the EBU_CLK clock as a reference to generate all external bus access sequences.

SDCLKO is required by SDRAM memories and the frequency of this output is controlled by the EBU_BUSRAP.EXTCLOCK field of the highest priority (lowest region number) region which has EBU_BUSRCON.AGEN set to 8_D, 10_D or 12_D which are the values used to select the SDRAM state machine. EBU_BUSWAP.EXTCLOCK has no effect for SDRAM.

Unless documented elsewhere, all outputs to the external bus are generated synchronously to the falling edge of SDCLKO. This means that the SDRAM memory device sees control signal changes occur on the negative clock edge.

Connecting DDR memories to the EBU will impose additional constaints on the external bus clocks. See **“External Bus Clock Generation” on Page 15-26**.

Table 15-38 EXTCLOCK to clock ratio mapping

EXTCLOCK value	SDCLKO divide ratio
00	1:1
01	1:2
10	1:4
11	1:4

15.18.5 SDRAM Characteristics

SDRAMs are synchronous DRAMs with burst read/write capability which are controlled by a set of commands at the pins $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DQM and A10. As for standard DRAMs, a periodic refresh must be performed.

SDRAM devices are subdivided into “banks”. Each bank is subdivided into a number of “rows[1)]”. Each row is, in turn, subdivided into a number of “columns”. The number of banks and the size of a row varies from one SDRAM device to another. A specific location (half-word) within a device is specified by supplying a bank, row and column address. Devices supported by Memory Controller must conform to the following criteria:-

- **Number of Banks:** 2 or 4 only.
- **Row Size:** 256, 512 or 1024 only.

SDRAM devices produce high speed data transfer rates by use of the bank and row architecture. When an initial access is made to a specific row within a specific bank then Memory Controller must issue a “row” address to specifiy which row in which bank is to accessed. In response to this the SDRAM device loads the entire row to a local (high speed) buffer area. At this point (i.e. when the local buffer associated with a bank contains data from the main SDRAM array) the bank is said to be “open”. Memory Controller then issues a “column” address to specifiy which location(s) within the row are to be accessed. Subsequent accesses to locations within the same row can then be performed at high speed (with Memory Controller supplying only a column address) since the appropriate data is already contained within the local buffer and there is no requirement for the SDRAM to fetch data from the main SDRAM array. Prior to accessing a location in a different row Memory Controller must issue a “precharge” command so that the local buffer is written back to the main SDRAM array.

An SDRAM device provides a local buffer for each bank within the device, thus it is simultaneously possible for each of the banks to be “open”, this is termed “Multibanking”. Multibanking is supported in order to allow interleaved bank accesses. Comparison of

1) Previous Memory Controller documentation uses the term “page” to refer to a “row”. Where possible this has been changed to reflect the more commonly used term “row”.

banks is done prior to initiating external memory accesses (see **"SDRAM Bank Management" on Page 15-131**).

15.18.6 Supported SDRAM commands

Table 15-39 lists the supported SDRAM commands, how they are triggered and which signals are activated:-

Table 15-39 Supported SDRAM commands

Command	Event	CKE (n-1)	CKE (n)	CS	RAS	CAS	RD/ WR	See Section 15.18.17 for Memory Controller pins			
								A12[1] A11	A10	A (9:0)	BA (1:0)
Device deselect	region not sel'ted	H	-	H	-	-	-	-	-	-	-
Nop	idle	H	-	L	H	H	H	-	-	-	-
Bank activate	open a closed bank	H	-	L	L	H	H	valid address			
Read	read access	H	-	L	H	L	H	valid addr	L	valid address	
Write	write access	H	-	L	H	L	L	valid addr	L	valid address	
Read with autoprecharge	read access	H	-	L	H	L	H	valid addr	H	valid address	
Write with autoprecharge	write access	H	-	L	H	L	L	valid addr	H	valid address	
Precharge selective	bank or row miss	H	-	L	L	H	L	-	L	-	bank
Precharge all	refresh is due or going into power down	H	-	L	L	H	L	-	H	-	-

Table 15-39 Supported SDRAM commands (cont'd)

Command	Event	CKE (n-1)	CKE (n)	CS	RAS	CAS	RD/ WR	See Section 15.18.17 for Memory Controller pins			
								A12[1)] A11	A10	A (9:0)	BA (1:0)
Autorefresh	refresh is due, after precharge all is done	H	H	L	L	L	H	-	-	-	-
Self refresh entry	going into power down after precharge all is done	H	L	L	L	L	H	-	-	-	-
Self refresh exit	coming out of power down	L	H	H	-	-	-	-	-	-	-
Mode register set	during initialization	H	-	L	L	L	L	valid mode (see register EBU_SDRMOD)			00_B
Extended Mode register set	during initialization	H	-	L	L	L	L	valid mode (see register EBU_SDRMOD)			10_B[2)]

1) A12 is required by larger memories

2) 10_B is default value for SDRAM. This can be changed using the **EBU_SDRMOD.XBA** field

15.18.7 SDRAM device size

The Memory Controller supports SDRAM's with the following sizes:-

- **Size**[1)]**:** 64MBit, 128MBit, 256MBit, 512MBit and 1Gbit.

1) In addition verified support is limited to specific SDRAM device geometries (number of banks and row size). Support for other sizes/geometries may be possible but this has not been verified.

15.18.8 Power Up Sequence

During power-up the SDRAM should be initialized with the proper sequence. This includes the requirement of bringing up the VDD, VDDQ and the stable clock (minimum 200 µs before any accesses to SDRAM) and $\overline{CS}$ remains inactive.

15.18.9 Initialization sequence

SDRAMs must be initialised before being used. Application of power must be followed by 200 µs pause (timed by software) with a stable clock. Then a Precharge All Banks command must be issued. Following this, the device must go through Auto Refresh Cycles (the number of refresh commands is programmable through **Crfsh** in SDRMCON registers and the number of NOP cycles in between is programmable through **Crc**). At the end of it, the Mode Register must be programmed through the address lines. Following that some number of NOP cycles programmable through **Crsc** in EBU_SDRMCON.

Note: This sequence will be referred to as a "cold start",and is necessary when both the memory and the memory controller have just had power applied. Conversely a "warm start" will be required when the memory controller has just been powered up but data has been retained in the external memory by the use of self refresh mode.

The SDRAM controller will power up with the SDRAM clock disabled and CKE high.

Care must be taken during software configuration of Memory Controller to ensure the correct SDRAM initialisation sequence is generated for both cold start and warm start.

15.18.9.1 Cold Start Initialisation

The recomended sequence for Memory Controller register initialisation after a cold start when using SDRAM devices is as follows:-

1. If the EBU is in “no bus” arbitration mode, write to EBU_MODCON to switch to an arbitration mode which allows external bus accesses
2. Write to BUSCON to define which region has SDRAM connected and the required divide ratio for the SDRAM clock.
3. Write to EBU_SDRMCON to configure the controller for the attached SDRAM device(s) and to enable the SDRAM clock. (**SDCMSEL** = $0_B$and **CLKDIS**=0_B.)
4. Initialise all other Memory Controller registers except SDRAM specific registers (i.e. other than those listed below).
5. Wait for 200µs (or the appropriate initialisation delay required by the attached device)
6. Write to EBU_SDRMOD with the "**COLDSTART**" bit set to precharge tall banks in he device, perform the required refresh commands and write the mode register values to the SDRAM mode register.
7. Write to EBU_SDRMREF to configure refresh rate. (see **“Refresh Cycles” on Page 15-133**.)

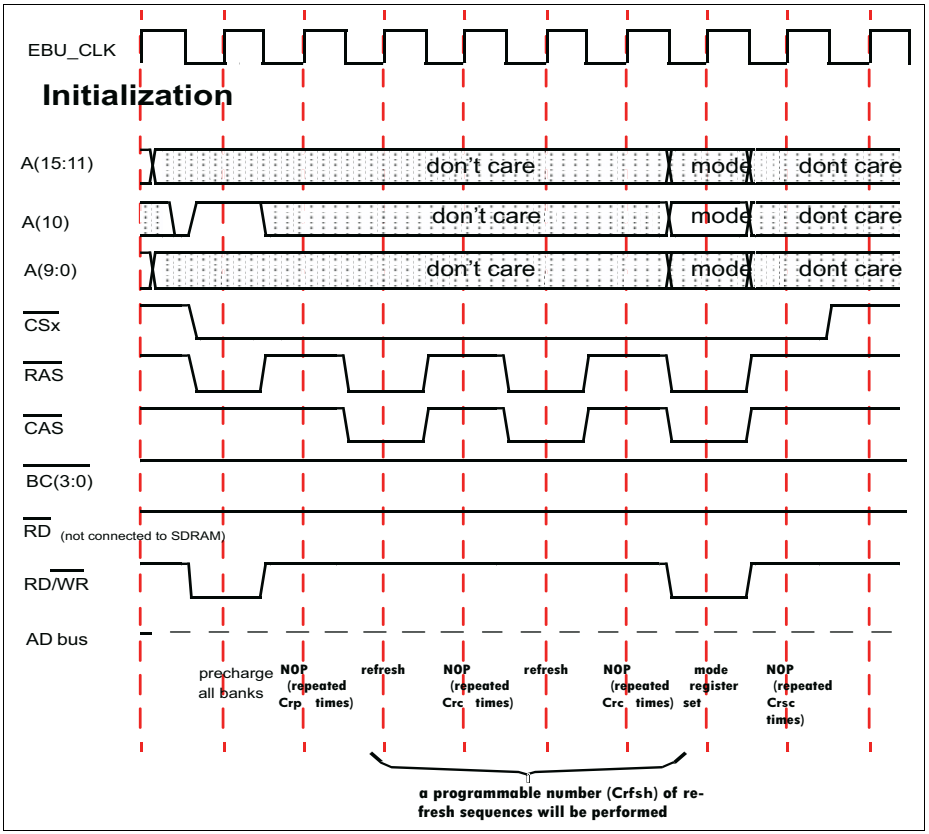


Figure 15-41 SDRAM Initialization

The sequence is triggered by a write to the SDRAM mode register SDRMOD. A device attached to a region having **agen** in BUSCONx set to '1000_B' will be configured with the mode from SDRMOD. While this sequence is being executed, **sdrmbusy** flag in the SDRMSTAT status register will be set accordingly.

Note: As no other accesses are permitted in the current implementation while the SDRAM initialisation sequence is running, it will not be possible to poll the sdrmbusy bit at '1' unless there has been a failure in the controller logic.

The user has to make sure that the SDRAM is programmed in the following way:

Table 15-40 SDRAM Mode Register Setting

Field	Value	Meaning	SDRMOD Position	Corresponding Address Pins
Burst length	"100" “011” “010” “001” "000"	bursts of length 16 bursts of length 8 bursts of length 4 bursts of length 2 bursts of length 1	**burstl**[2:0]	A[2:0]
Burst type	‘0’	sequential bursts	**btyp**[3]	A[3]
$\overline{\text{CAS}}$ latency	“001” “010” “011” “1xx”	reserved latency 2 latency 3 reserved	**caslat**[6:4]	A[6:4]
Operation Mode	all ‘0’	burst read and burst write	**opmode** [13:7]	A[12:7]

The Memory Controller uses the $\overline{\text{CAS}}$ latency value and burst length to adjust the burst read timing. All other fields have no influence on the Memory Controller, which means only a single value is accepted for those fields.

The complete initialization sequence described will only be issued on the first write (since reset) to the **EBU_SDRMOD** register with the **COLDSTART** field set to logic ’1’. On subsequent writes with the **COLDSTART** field set to logic ’1’, the SDRAM device does not need to be initialized, so a simple mode register set command can be issued to refresh the contents of the registers in the SDRAM. A precharge-all command needs to be issued to the SDRAM before this can happen.

An initialisation sequence will write to both the mode register and the extended mode register (if the extended mode register has been enabled).

A write to the **EBU_SDRMOD** register with the **COLDSTART** cleared will update the EBU register and will also write to the config registers of the SDRAM but will not execute the refresh cycles which are part of the full initialisation required at cold start.

15.18.9.2 Warm Start Initialisation

The recomended sequence for Memory Controller register initialisation after a warm start when using SDRAM devices requires a pull-down resistor on the CKE pin and is as follows:

1. If the EBU is in “no bus” arbitration mode, write to EBU_MODCON to switch to an arbitration mode which allows external bus accesses

2. Write to EBU_BUSRCON to define which region has SDRAM connected and the required divide ratio for the SDRAM clock.
3. Write to **EBU_SDRMCON** to configure the controller for the attached SDRAM device(s) and to enable the SDRAM clock. (**SDCMSEL**=0_B and **CLKDIS**=0_B.)
4. Write to **EBU_SDRMREF** to configure refresh rate.
5. All other Memory Controller registers except SDRAM specific registers (i.e. other than those listed below).
6. Write to **EBU_SDRMOD** with the "**COLDSTART**" bit cleared to update the mode register values.

The SDRAM will be taken out of self-refresh when step two is completed. Auto-refresh by the EBU will start at the completion of step 4 when the refresh counters in the SDRAM controller expire. Care should be taken when setting the registers to ensure that the maximum refresh period is not exceeded.

15.18.10 Mobile SDRAM Support

Mobile SDRAMs include an “Extended Mode Register”. This is accessed using a similar mechanism to the existing PC-133 Mode Register but with an additional select code on the SDRAM device BA pins.

The **EBU_SDRMOD.XBA** bits are used to select “Mobile” SDRAM support for each of the SDRAM devices. If this field is non-zero, then the Extended Mode Register will be automatically written during the Initialization phase (immediately after the “standard” Mode Register write). In addition writes to the Extended Mode Register(s) will be triggered by writes to the **EBU_SDRMOD** register (i.e. whenever the “standard” Mode Register is written). The **EBU_SDRMOD.XOPM** bit-field is used to program the value that is to be written to the Extended Mode Register. The **EBU_SDRMOD.XBA** bit-field is used to program the logic levels asserted on the device BA(1:0) pins (i.e. to program the specific command used to access the extended mode register).

Note: In order to cater for possible future device variations the Memory Controller allows the user to select the logic levels issued on the BA(1:0) pins during an Extended Mode Register. Care should be taken in programming this bit field since it is possible to generate an unwanted “standard” Mode Register write by use of this bit field.

15.18.11 Burst Accesses

The Memory Controller supports SDRAM burst lengths of 1, 2, 4, 8 and 16. Bursts of other lengths are supported but are implemented using data-masking. Burst length 16 is currently not supported by available SDR memories.

15.18.12 Short Burst Accesses and Byte Writes

The Memory Controller can be configured to generate SDRAM bursts lengths of either one, two, four, eight or sixteen via the EBU_SDRMOD.**BURSTL** bit fields. When configured for burst lengths of four or eight the interface will use data masking to support shorter write accesses. However, when configured for a burst length of one data masking is not used. **Figure 15-42** shows how short burst write accesses are handled. During the write access data masking is activated (with zero clock latency) to prevent unwanted write operation. Data masking is activated through the $\overline{BCx}$ outputs (connected to $\overline{DQM}$ on the SDRAM device) during a write cycle.

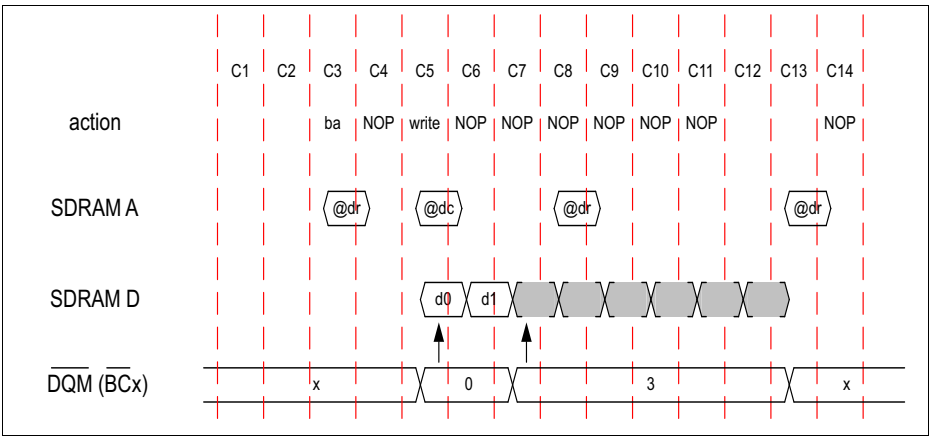


Figure 15-42 Short Burst Write Access through Data Masking

The figure shows how a two beat burst write is translated to an eight beat burst write with data masking. During the first two data cycles (C5 and C6) the $\overline{BC0}$ and $\overline{BC1}$ outputs are driven low to cause the SDRAM device to write the required data. In cycle C7 the $\overline{BC0}$ and $\overline{BC1}$ outputs are driven high to mask subsequent data writes.

When performing byte writes, the DQM signals on $\overline{BC[3:0]}$ signals are used to mask the byte lines not required for the write in progress.

15.18.13 SDRAM Addressing Scheme

SDRAM devices use a multiplexed address issued as “bank”, “row” and “column” addresses.

The bank address is used to qualify row and column addresses and is used to divide the addressed memory into physically indpendent regions. An SDRAM bank will have its own sense amplifiers and row buffer which operate independently of the sense amplifiers and row buffers of the other banks in the device.

The row address determines which row is being accessed within a bank and is placed on the bus during a “bank activate command”. The bank activate command loads to contents of the row into one of the row buffers of the SDRAM device. Once in the row buffer it can be modified by write commands or transferred to the memory controller by read commands. The row buffer used is determined by the bank address bits.

The column address determines which location is being accessed within a row. The column address is placed on the bus during read or write commands.

Since the number of rows per bank and the row sizes can differ from one SDRAM device to another it is necessary to provide a programmable address multiplexing scheme. Selection of the multiplexing scheme is via the **EBU_SDRMCON.AWIDTH** and **EBU_SDRMCON.BANKM** bit-fields.

The SRI address (A_{SRI}) is mapped to the SDRAM as follows:

- A_{SRI}(n:0) are used as the column address, where n is defined using the **AWIDTH** field. See **“Column Address Multiplexing” on Page 15-127**
- A_{SRI}(m-1:n+1) are used as the row address, where m is defined using the **BANKM** field. See **“Row Address Multiplexing” on Page 15-128**
- A_{SRI}(m+1:m) are used as the bank address. See **“Bank Address Multiplexing” on Page 15-126**

15.18.14 Bank Address Multiplexing

A bank address is always issued whenever either a row or column address is issued. As a result the Bank Address multiplexing must be the same regardless of whether a row or column address is being issued.

Note: The Memory Controller uses it’s address output pins to select the bank being accessed (rather than having dedicated Bank Select outputs).

The SDRAM Bank Select pin(s) (BA[1:0]) must be connected to the Memory Controller A[15:14] address pins. The **EBU_SDRMCON.BANKM** bit-field must be set correctly to ensure that they are driven by the appropriate SRI Address (according to the SDRAM geometry).

The "EBU_SDRMCON.**BANKM**" (bank mask) bit-field must be set to the appropriate value to set the SRI address bit range used to detect which bank is being accessed. The value to be written to this bit-field is determined by the device size setting (see **“SDRAM device size” on Page 15-120**) and the number of banks in the device.

- When the device has 2 banks then the "**BANKM**" value must be set to include the most significant address bit of the SRI address range occupied by the SDRAM device (i.e. region) - see **Table 15-45** and **Table 15-46**.
- When the device has 4 banks then the "bankm" value must be set to include the most significant two address bits of the SRI address range occupied by the SDRAM device (i.e. region) - see **Table 15-45** and **Table 15-46**.

The following settings must be used:

Table 15-41 “BANKM” Selection

“BANKM” setting	SRI Address Bits used for BA[1:0]	Comment
0	none	Reserved - do not use (default after reset).
1	A_{SRI}[21 to 20]	Bank Size = 8MBit
2	A_{SRI}[22 to 21]	Bank Size = 16MBit
3	A_{SRI}[23 to 22]	Bank Size = 32MBit
4	A_{SRI}[24 to 23]	Bank Size = 64MBit
5	A_{SRI}[25 to 24]	Bank Size = 128MBit
6	A_{SRI}[26 to 25]	Bank Size = 256MBit.
7	A_{SRI}[27 to 26]	not supported for SDRAM/DDRAM

15.18.15 Column Address Multiplexing

When a column address is issued:

- The most significant Memory Controller address outputs (A[27:16]) are driven with '0' (zero).
- The least significant ten address outputs (A[9:0]) are driven with the (correctly aligned) column address. This address alignment is a one bit right shift of the SRI address if the SDRAM is 16 bit or a two bit shift if the SDRAM is 32 bit. This address alignment is performed according to the device row size specified by the "AWIDTH" bit-field and the “PORTW” field (see **Table 15-42**). Note that all 10 possible column address lines are always driven regardless of the row size of the device. Superfluous address bits will be ignored by the attached memory
- Address output ten (A[10]) is driven with a “command” value (used by the SDRAM in conjunction with the other control signals to determine which command is to be executed.
- The address outputs (A[15:14]) are driven with the bank address signals, BA[1:0] (see **“Bank Address Multiplexing” on Page 15-126**).

The "EBU_SDRMCOM.**AWIDTH**" bit-field sets row size of the attached memory and therefore the number of address bits the memory device require for the column address. The value to be written to this bit-field is as follows:

Table 15-42 Selection of address multiplexing

AWIDTH	Row size	16 bit DRAM PORTW="01"	32 bit DRAM PORTW="11"
00_B	Reserved; do not use	-	-
01_B	256 words	A_{SRI}(8:0) (512 bytes)	A_{SRI}(9:0) (1024 bytes)
10_B	512 words	A_{SRI}(9:0) (1024 bytes)	A_{SRI}(10:0) (2048 bytes)
11_B	1024 words	A_{SRI}(10:0) (2048 bytes)	A_{SRI}(11:0) (4096 bytes)

Table 15-43 Column Address Generation for SDRAM/DDRAM

16 bit, PORTW="01" Address Generation (at Memory Controller pins)	32 bit, PORTW="11" Address Generation (at Memory Controller pins)
A[27:16] = '0' A[15:14] = BA[1:0] A[10] = Command A[9:0] = A_{SRI}[10:1]	A[26:16] = '0' A[15:14] = BA[1:0] A[10] = Command A[9:0] = A_{SRI}[11:2]

15.18.16 Row Address Multiplexing

When a row address is issued as follows:-

- The most significant Memory Controller address outputs not required by the SDRAM (A[27:16]) are driven with '0' (zero).
- A[15:14] are driven with the bank address signals, BA[1:0]
- The least significant fourteen address outputs (A[13:0]) are driven with the correctly aligned row address. This address alignment is performed according to the device row size specified by the "AWIDTH" bit-field and the "PORTW" field (see **Table 15-44**). Note that all 14 possible row address lines are always driven regardless of the number of rows in the device. Superfluous address bits will be ignored by the attached memory.

During the issue of a row address the following address multiplexing is used:-

Table 15-44 Row address generation for 16 bit SDRAM

AWIDTH	16 bit, PORTW="01" Address Generation (at Memory Controller pins)	32 bit, PORTW="11" Address Generation (at EBU pins)
01_B	A[13:0] = A_{SRI}[22:9]	A[13:0] = A_{SRI}[23:10]
10_B	A[13:0] = A_{SRI}[23:10]	A[13:0] = A_{SRI}[24:11]
11_B	A[13:0] = A_{SRI}[24:11]	A[13:0] = A_{SRI}[25:12]

15.18.17 Supported SDRAM Configurations

The following SDRAM types can be connected to Memory Controller:

Table 15-45 Example Supported Configurations for 16-bit wide data bus

SDRAM portw = 01_B (16-bit)			Signal Mapping	Memory Controller Pins unused bits at MSB(s) of fields				AWIDTH
Size Mbit		Add		A(15:14)	A(13:11)	A(10)	A(9:0)	
1024	64Mx16	row	SDRAM	BA(1:0)	RA(13:11)	RA(10)	RA(9:0)	11
			A_{SRI} signals	(26:25)	(24:22)	(21)	(20:11)	
		col	SDRAM	BA(1:0)		CMD	CA(9:0)	
			A_{SRI} signals	(26:25)		CMD	(10:1)	
512	32Mx16	row	SDRAM	BA(1:0)	RA(12:11)	RA(10)	RA(9:0)	11
			A_{SRI} signals	(25:24)	(23:22)	(21)	(20:11)	
		col	SDRAM	BA(1:0)		CMD	CA(9:0)	
			A_{SRI} signals	(25:24)		CMD	(10:1)	
256	16Mx16	row	SDRAM	BA(1:0)	RA(12:11)	RA(10)	RA(9:0)	10
			A_{SRI} signals	(24:23)	(22:21)	(20)	(19:10)	
		col	SDRAM	BA(1:0)		CMD	CA(8:0)	
			A_{SRI} signals	(24:23)		CMD	(9:1)	
128	8Mx16	row	SDRAM	BA(1:0)	RA(11)	RA(10)	RA(9:0)	10
			A_{SRI} signals	(23:22)	(21)	(20)	(19:10)	
		col	SDRAM	BA(1:0)		CMD	CA(8:0)	
			A_{SRI} signals	(23:22)		CMD	(9:1)	

Table 15-45 Example Supported Configurations for 16-bit wide data bus (cont'd)

SDRAM portw = 01_B (16-bit)			Signal Mapping	Memory Controller Pins unused bits at MSB(s) of fields				AWI DTH
Size Mbit		**Add**		**A(15:14)**	**A(13:11)**	**A(10)**	**A(9:0)**	
64	16Mx 4[1]	row	SDRAM	BA(1:0)	RA(11)	RA(10)	RA(9:0)	11
			A_{SRI} signals	(24:23)	(22)	(21)	(20:11)	
		col	SDRAM	BA(1:0)		CMD	CA(9:0)	
			A_{SRI} signals	(24:23)		CMD	(10:1)	
	8Mx8 [2]	row	SDRAM	BA(1:0)	RA(11)	RA(10)	RA(9:0)	10
			A_{SRI} signals	(23:22)	(21)	(20)	(19:10)	
		col	SDRAM	BA(1:0)		CMD	CA(8:0)	
			A_{SRI} signals	(23:22)		CMD	(9:1)	
	4Mx 16	row	SDRAM	BA(1:0)	RA(11)	RA(10)	RA(9:0)	01
			A_{SRI} signals	(22:21)	(20)	(19)	(18:9)	
		col	SDRAM	BA(1:0)		CMD	CA(7:0)	
			A_{SRI} signals	(22:21)		CMD	CA(8:1)	
16	4Mx4 [3]	row	SDRAM	BA(0)[4]		RA(10)	RA(9:0)	11
			A_{SRI} signals	(22)		(21)	(20:11)	
		col	SDRAM	BA(0)		CMD	CA(9:0)	
			A_{SRI} signals	(22)		CMD	(10:1)	
	2Mx8 [5]	row	SDRAM	BA(0)[6]		RA(10)	RA(9:0)	10
			A_{SRI} signals	(21)		(20)	(19:10)	
		col	SDRAM	BA(0)		CMD	CA(8:0)	
			A_{SRI} signals	(21)		CMD	(9:1)	
	1Mx 16	row	SDRAM	BA(0)[7]		RA(10)	RA(9:0)	01
			A_{SRI} signals	(20)		(19)	(18:9)	
		col	SDRAM	BA(0)		CMD	(8:1)	
			A_{SRI} signals	(20)		CMD	(8:1)	

1) deprecated, 4 devices in parallel needed to make a 16Mx16 configuration

2) 2 devices in parallel needed to make an 8Mx16 configuration

3) deprecated, 4 devices in parallel needed to make a 4Mx16 configuration

4) 2 bank device. Accessing device with $A_{SRI}(23)$ set will cause page tag corruption and access errors

5) 2 devices in parallel needed to make an 2Mx16 configuration

6) 2 bank device. Accessing device with $A_{SRI}(22)$ set will cause page tag corruption and access errors

7) 2 bank device. Accessing device with $A_{SRI}(21)$ set will cause page tag corruption and access errors

Notes:

- RA: row address
- BA: bank select (MSB of row address)
- CA: column address
- CMD: auto pre-charge command is currently not supported
- Areas in shades are not recommended for SDRAM configurations, in order to minimize loads on the pads.

Table 15-46 Example Supported Configurations for 32-bit wide data bus

SDRAM portw = 11_B (32-bit)			Signal Mapping	Memory Controller Pins unused bits at MSB(s) of fields				AWI DTH
Size Mbit		**Add**		**A(15:14)**	**A(13:11)**	**A(10)**	**A(9:0)**	
1024	32Mx32	row	SDRAM	BA(1:0)	RA(12:11)	RA(10)	RA(9:0)	11
			A_{SRI} signals	(26:25)	(24:23)	(23)	(21:12)	
		col	SDRAM	BA(1:0)		CMD	CA(9:0)	
			A_{SRI} signals	(26:25)		CMD	(11:2)	
512	16Mx32	row	SDRAM	BA(1:0)	RA(12:11)	RA(10)	RA(9:0)	10
			A_{SRI} signals	(25:24)	(23:22)	(21)	(20:11)	
		col	SDRAM	BA(1:0)		CMD	CA(8:0)	
			A_{SRI} signals	(25:24)		CMD	(10:2)	
256	8Mx32	row	SDRAM	BA(1:0)	RA(11)	RA(10)	RA(9:0)	10
			A_{SRI} signals	(24:23)	(22)	(21)	(20:11)	
		col	SDRAM	BA(1:0)		CMD	CA(8:0)	
			A_{SRI} signals	(24:23)		CMD	(10:2)	
128	4Mx 32	row	SDRAM	BA(1:0)	RA(11)	RA(10)	RA(9:0)	01
			A_{SRI} signals	(23:22)	(21)	(20)	(19:10)	
		col	SDRAM	BA(1:0)		CMD	CA(8:0)	
			A_{SRI} signals	(23:22)		CMD	(9:2)	

15.18.18 SDRAM Bank Management

The EBU maintains a page tag register for each bank of the SDRAM device. This is updated with the row tag of the opened page when a “bank activate” occurs.

It is flagged as valid every time a row is opened in the bank and invalidated when the row is precharged (the bank is “closed”).

The EBU contains four page tag registers. This allows devices with up to four banks to be supported.

The "EBU_SDRMCON.**AWIDTH**" bit-field is used to set the lower bound of the SRI address range of the page tag. The upper end of the address range is determined by the **BANKM** setting.

The row tag is the address range between the most-significant column address width as determined by **AWIDTH** and the least significant bank address bit as determined by **BANKM**.

When a read or write transaction is addressed to the SDRAM, The bank address bits will decoded from the SRI address. This will be used to select the appropriate page tag. If the page tag is valid (bank hit) and the row tag of the current access matches the row tag stored in the page tag register, then a “row hit” will be flagged.

The other options, invalidated page tag register (bank miss) and unmatched page tag (row miss) are used to determine the necessary controller actions needed to complete the access.

15.18.18.1Decisions over “row hit”

When a row hit occurs, the memory controller can continue the access operation using data already in the SDRAM row buffer and without updating the stored page tag.

The absence of a “row hit” can result in several other activities.

- If the absence of a “row hit” is due to the bank being accessed not having an open row (“bank miss”), then the memory controller does not have to issue a precharge operation but can activate the bank, update the appropriate page tag to reflect the new bank status (i.e. to “open” with the specified row address) and continue the access operation.
- If a “row miss” occurs without a “bank miss”, then the memory controller has to close the open row in the bank being accessed, (i.e. do a precharge). This is then followed by re-activating the bank, updating the appropriate page tag to reflect the new bank status (i.e. “open” with the new page address) and continuing the access operation.

15.18.19 Banks Precharge

The system is required to precharge a bank under one of the following conditions:

1. When the next access to a bank is to a different row to the previous access within the bank, the affected bank will be selectively precharged to enable the new row to be opened. This is triggered as detailed in **“Bank Address Multiplexing” on Page 15-126**.
2. When an SRI request cannot be completed before the row active time $t_{RAS\ max}$ is due, then the bank must explicitly be closed and opened again for the current request. Since $t_{RAS\ max}$ (of the order of 100 µs) is usually much greater compared to the refresh

period (distributed refresh is in order of 15 µs for 4096 rows) this is generally fulfilled by systematically carrying out refresh to the SDRAMs (see '3' below).
3. All banks must also be pre-charged, when a refresh cycle is due as explained next. See **"Refresh Cycles" on Page 15-133**.
4. All banks must also be pre-charged, prior to issuing Self Refresh Entry command. See **"Self-Refresh Mode" on Page 15-133**.

15.18.20 Refresh Cycles

The refresh sequence is controlled by the EBU hardware and is periodically triggered by an internal refresh counter with programmable rate. The rate is set using the **ERFSHC** and **REFRESHC** fields in the EBU_SDRMREF register. These fields are combined to create an eight bit value (**ERFSHC** as MSBs). This value is then multiplied by 64 and used as the number of EBU_CLK cycles between refresh operations being requested.

All SDRAM banks will be pre-charged using a single "precharge all" command before any refresh commnads are issued. After the "precharge all" command, the EBU will insert NOP commands on the external bus to allow the precharge command to be completed by the memory device. The number of NOPs will be determined by the **EBU_SDRMCON.CRP** bitfield.

The specific refresh command issued is Auto Refresh (CBR) command, in which the device keeps track of the row addresses to be refreshed. The number of commands issued for each refresh sequence is programmable through **REFRESHR** in **EBU_SDRMREF**. After each refresh command, the EBU will issue NOP commands on the external bus to allow time for the device to complete the refresh operation before another command is issued. The number of NOPs will be determined by the **EBU_SDRMCON.CRC** bitfield.

A refresh request has precedence over an SRI access to SDRAM, i.e. if both occur at the same time the refresh sequence is entered and the SRI access is delayed.

A refresh error occurs when a previous refresh request has not been satisfied and another refresh request occurs. An error flag (**REFERR**) in the **EBU_SDRSTAT** status register will be set accordingly.

15.18.21 Self-Refresh Mode

SDRAM devices provide a Self-Refresh Mode. In this mode the SDRAM automatically performs internal refresh sequences in response to an on-chip timer. Self Refresh Mode is entry command is asserted with RAS, CAS, and CKE low and $\overline{WE}$ high. In Self-Refresh Mode all external control signals except CKE (but including the clock) are disabled). Returning CKE to high enables the clock and initiates the Self-Refresh Mode exit operation. After the exit command, at least one tRC delay is required prior to any access command. This delay can be configured using the **EBU_SDRMREF.SELFREX_DLY** bitfield.

Low Power SDRAMs provide additional power saving features such as:-

Programmable refresh period of the on-chip timer such that the refresh period can be optimised (maximised) by taking the device operating temperature in to account.

Partial array self-refresh mode such that only selected banks will be refreshed. Data written to the non-selected banks will be lost (due to lack of refresh to the bank) after a period defined by t_{REF}.

These additional features are programmed by issuing an Extended Mode Register write (see **"Mobile SDRAM Support" on Page 15-124**).

To activate Self-Refresh Mode, software must write '1' to bit **SELFREN** in **EBU_SDRMREF** register. Memory Controller will then:

1. precharge all the banks, and
2. issue a self refresh command (see **Table 15-39**) to the attached SDRAM device.

In completion of this command all SDRAM devices will ignore all inputs but CKE signal. The read-only bit **SELFRENST** reflects the status of issuing this command. When the command is completed, power-down can be safely entered. The devices would perform low-current self refresh during the power down. When exiting from power-down and before doing any accesses to SDRAM, software must write '1' to bit **SELFREX** in EBU_SDRMREF registers. Memory Controller will then assert the CKE signal for all the SDRAM devices to get out of the self-refresh mode. The read-only bit **SELFREXST** reflects the completion of this command, upon which an access to SDRAMs can be performed.

Two additional fields affect the method the memory controller uses to exit self refresh.

1. After CKE is taken high (self refresh exit command), a single NOP cycle is generated. The **EBU_SDRMREF.ARFSH** field is checked. If set to one a single auto refresh command is output to the memory.
2. After step 1, the **EBU_SDRMREF.SELFREX_DLY** field is checked. If the field is non-zero, the value in the field is used to generate a sequence of NOP instructions to the memory. This allows between 1 and 255 NOPs to be inserted before the device sees a non-null command.

For predictable operation of the device during warm start, both the **EBU_SDRMREF.ARFSH** and **EBU_SDRMREF.SELFREX_DLY** fields should be set to 0 before triggering the warm start.

15.18.22 Power Down Mode

In order to reduce standby power consumption SDRAM devices provide a Power Down Mode. All banks can optionally be precharged before the device enters Power Down mode. Once Power Down mode is initiated by holding CKE low, all receiver circuits except for CLK and CKE are gated off. Power Down mode does not perform any refresh operations in the way that self refresh mode does, therefore to prevent loss of data, the device must not remain in Power Down mode longer than the Refresh period (tREF) of

the device. Taking the device out of power down to perform autoreresh is handled automatically by the SDRAM controller. Exit from this mode is performed by taking CKE “high”. One clock cycle delay is required for power down mode entry and exit.

The Memory Controller provides automatic support for Power Down Mode via the EBU_SDRMCON.SDCMSEL (SDRAM clock mode select) bit. When this bit is ‘0’ Power Down mode will not be used and the SDRAM clock will always be present at the SDCLKO pin. When the bit is ‘1’ the device will automatically be placed into Power Down Mode when there are no SDRAM accesses pending. In this case the SDRAM clock will only be present during an Memory Controller-generated SDRAM access (data, refresh, bank/row open etc) and will be gated off at all other times.

When a refresh is required (at the programmed rate) Memory Controller will automatically take the device out of Power Down Mode, issue the required refresh and will then return the device to Power Down Mode (providing no other SDRAM accesses are pending following the refresh).

By default, the Memory Controller automatically issues the “Pre-Charge All” command sequence and closes all pages prior to entry into Power Down Mode (EBU_SDRMCON.PWR_MODE set to 00_B).

The memory controller can also be configured to use the auto-precharge option when running a command (EBU_SDRMCON.PWR_MODE set to 01_B) or not to precharge banks at all (active power down mode) with EBU_SDRMCON.PWR_MODE set to 10_B.

As a final option, "clock stop" power down mode is also supported. In this case, the clock is disabled between accesses with no preparatory command cycles (EBU_SDRMCON.PWR_MODE set to 11_B).

The default reset state of Memory Controller is Power Down Mode disabled (EBU_SDRMCON.SDCMSEL = ‘0’).

Note: The programmer should be very careful about the use of this feature as some external devices may require this clock to be running in some modes. There are restrictions within the PC-133 specification about when the clock can be disabled, especially if the SDRAMs are operated in self-refresh mode.

A separate field **EBU_SDRMREF.RES_DLY** is provided to allow a delay to be programmed after exiting the power down mode. This field is the delay, in external clock cycles (NOPs), after CKE is taken high on exiting power down mode before another command is permitted.

An additional bit EBU_SDRMCON.CLKDIS is provided to allow the clock output to be completely disabled. Setting this bit will allow a self refresh exit to be performed to enable CKE without starting the clock.

15.18.23 SDRAM Recovery Phases

15.18.23.1Recovery after SDRAM Command

A recovery phase can be programmed to increase the minimum gap between an SDRAM access and an access to another connected memory.

For write cycles, the minimum value for this gap is two periods of the internal clock between last command/data driven and the next access starting (for DDR the gap for data is one cycle). This can be increased by setting the BUSWAP.WRDTACS field to the required number of internal clock cycles.

For read accesses, the gap can also be increased using the BUSRAP.RDDTACS field in the same way. However, the counter is started when the last read command is issued by the controller and the controller does not permit another device to be accessed until two clock cycles after the last data has been read into the read buffers. As the read data is significantly delayed by the latency through the read synchronisation logic (minimum latency is 2 clock cycles CAS latency plus 2 clock cycles internal latency), setting this for read accesses is unlikely to make a significant difference unless very large values are used.

15.18.23.2Write Recovery Time (T_{WRC})

SDRAMs require a write recovery time after the last data is written before the next command can be processed. The usual value for this is one cycle of the SDRAM clock and this value is hard coded into the controlling state machine. Some devices require more delay and this can be programmed using the **WRRECOVC** field of the BUSWAPx register. Values of 0_H or 1_H (corresponding to zero or one cycle of recovery) have no effect because of the hardcoded lower limit of one clock cycle of recovery but programming larger values will set the number of clock cycles of write recovery time to the number programmed into the field.

The programmed value will set the number of SDRAM clock (SDCLKO) cycles of write recovery used rather than the number of EBU_CLK cycles.

15.18.24 Status Register Definition

The **EBU_SDRSTAT** register contains four bits which can be used to interrogate the status of EBU functions critical for SDRAM accesses. where these bits report an error condition, they will latch at 1_B until reset by writing 0_B to the register bit.

15.18.24.1Refresh Error (REFERR)

The SDRAM controller will schedule a refresh operation to an attached SDRAM memory at an interval set by the **EBU_SDRMREF**.**REFRESHR** bitfield. The **REFERR** bit is set if the scheduled refresh has not occurred by the time the next refresh becomes due. If this error condition occurs, then the refresh operations are not keeping up with the device reaquirements and data loss is likely. This bit latches and must be cleared by software.

15.18.24.2SDRAM Controller Busy (SDRMBUSY)

This bit is set while the controller is performing the initialisation sequence of an attached memory. It will clear once the initialisation is complete. This bit can be polled to ensure that other EBU functions (such as clock switching) are not performed while an initialisation is in progress.

15.18.24.3SDRAM Read Error (SDERR)

The **SDERR** bit is set when the control logic detects an error has occurred transferring data from an attached memory device using the SDRAM data path. This bit will latch. The bit will set under the following conditions:

- The addressed memory does not respond within sixteen clock cycles of the external bus clock
- The device returns more data than is expected by the controller.
- The device does not return enough data to complete the access.
- FIFO bypass mode is enabled and the controller detects that a DDR device is not returning data within half a clock period

15.18.24.4DLL Drift Detected (DRIFT_WARN)

See **“DLL Drift detector” on Page 15-23**.

15.18.25 Programmable Parameters

The following table lists programmable parameters for SDRAM accesses. These parameters are only effective when parameter **AGEN** (in BUSCONx registers) for a particular memory region is set to "8_D".

Table 15-47 SDRAM Access Programmable Parameters

Parameter	Function	Register
Address Mapping		
BANKM	Map SRI address bits to the bank address bits.	EBU_SDRMCON
AWIDTH	Number of address bits to be used for column address	EBU_SDRMCON
Refresh Control Parameters		
REFRESHR	Number of refresh commands issued during each refresh operation.	EBU_SDRMREF

Table 15-47 SDRAM Access Programmable Parameters (cont'd)

Parameter	Function	Register
ERFSHC & **REFRESHC**	Number of cycles (multiplied by 64) between refresh operations: 0 : no refresh needed 1 - 255 : refresh period defined	EBU_SDRMREF
ARFSH	execute auto refresh on exit from self refresh when set to one	EBU_SDRMREF
CRFSH	Number of refresh commands during initialization	EBU_SDRMCON
SDRAM Timing Constraint Compliance Parameters		
CRC	Number of NOP cycles after a refresh comand before another command can be executed. (device t_{RFC})	EBU_SDRMCON
CRCD	Number of NOP cycles between a row and column address (device t_{RCD})	EBU_SDRMCON
CRP	Number of NOP cycles after a precharge command before another command can be executed. (device t_{RP})	EBU_SDRMCON
CRSC	Number of NOP cycles after a mode register set command before another command can be executed. (device t_{MRD})	EBU_SDRMCON
CRAS	Minimmum number of cycles between a row activate and a precharge command to the same row (device t_{RAS} minimum)	EBU_SDRMCON
RES_DLY	delay after exiting power down before permitting any command other than NOP (device t_{XP})	EBU_SDRMREF
SELFREX_DLY	delay after exiting self refresh before permitting any command other than NOP (device t_{XSR})	EBU_SDRMREF
WRRECOVC	recovery time after write command before starting another command, used to meet device T_{wr} parameter	EBU_BUSWAP
RDDTACS	recovery time after read command before accessing another region.	EBU_BUSRAP
WRDTACS	recovery time after write command before accessing another region.	EBU_BUSWAP

Table 15-47 SDRAM Access Programmable Parameters (cont'd)

Parameter	Function	Register
SDRAM Device Register Contents		
OPMODE	To specify write operation mode: only BURST_WRITE is recognized	EBU_SDRMOD
CASLAT	To specify $\overline{\text{CAS}}$ latency : 2 or 3 clocks	EBU_SDRMOD
BTYP	To specify burst operation mode: SEQUENTIAL only	EBU_SDRMOD
BURSTL	To specify burst length: 1,2,4, 8 or 16	EBU_SDRMOD
XOPM	Value to be written to the extended mode register	EBU_SDRMOD
XBA	Bank Address value to be used for extended mode register write	EBU_SDRMOD
SDRAM Status		
SDRMBUSY	Indicate the busy status of SDRAM	EBU_SDRSTAT
REFERR	Indicate a refresh error	EBU_SDRSTAT
SDERR	Indicates an error has occurred on an SDRAM read	EBU_SDRSTAT
DRIFT_WARN	Indicates an error has occurred on an SDRAM read	EBU_SDRSTAT
SDRAM Controller Mode Control		
PWR_MODE	SDRAM controller power savemode	EBU_SDRMCON
SELFREN	To kick-off a self refresh entry command	EBU_SDRMREF
SELFRENST	Status of self refresh entry command	EBU_SDRMREF
SELFREX	To kick-off a self refresh exit command	EBU_SDRMREF
SELFREXST	Status of self refresh exit command	EBU_SDRMREF
AUTOSELFR	To activate automatic self refresh entry/exit when arbitrating the external bus	EBU_SDRMREF
Clock Control		
EXTCLOCK	ratio between internal clock and external memory clock for SDRAM accesses.	EBU_BUSRAP
SDCMSEL	SDRAM Clocking Mode - continuous clock or power save enabled	EBU_SDRMCON
CLKDIS	Disable the SDRAM clock output	EBU_SDRMCON

15.19 DDRAM/Mobile DDRAM Support

Support for DDRAM is in most ways similar to support for SDRAM. Device command definitions are the same. The major differences are necessary to support the generation and latching of data on both clock edges. This section should therefore be read as an extension of **Chapter 15.18**, **SDRAM Interface**.

Additional waveform diagrams can be found in JESD209, Low Power Double Data Rate (LPDDR) SDRAM Standard.

The following functionality has been provided to support DDR memory:

- A DLL is used to retime the DQS signals for read and write accesses to enable successful data capture. See **"DLL Operation" on Page 15-20** for information on the DLL.
- A read data FIFO is used to enable data to be successfully transferred to the read buffers after being latched by the DDR generated DQS lines.

These functions, and the necessary remapping of interface pins to support the load requirements of the DDR interface, are enabled by configuring the **AGEN** field of any EBU_BUSRCON register to specify a DDR device.

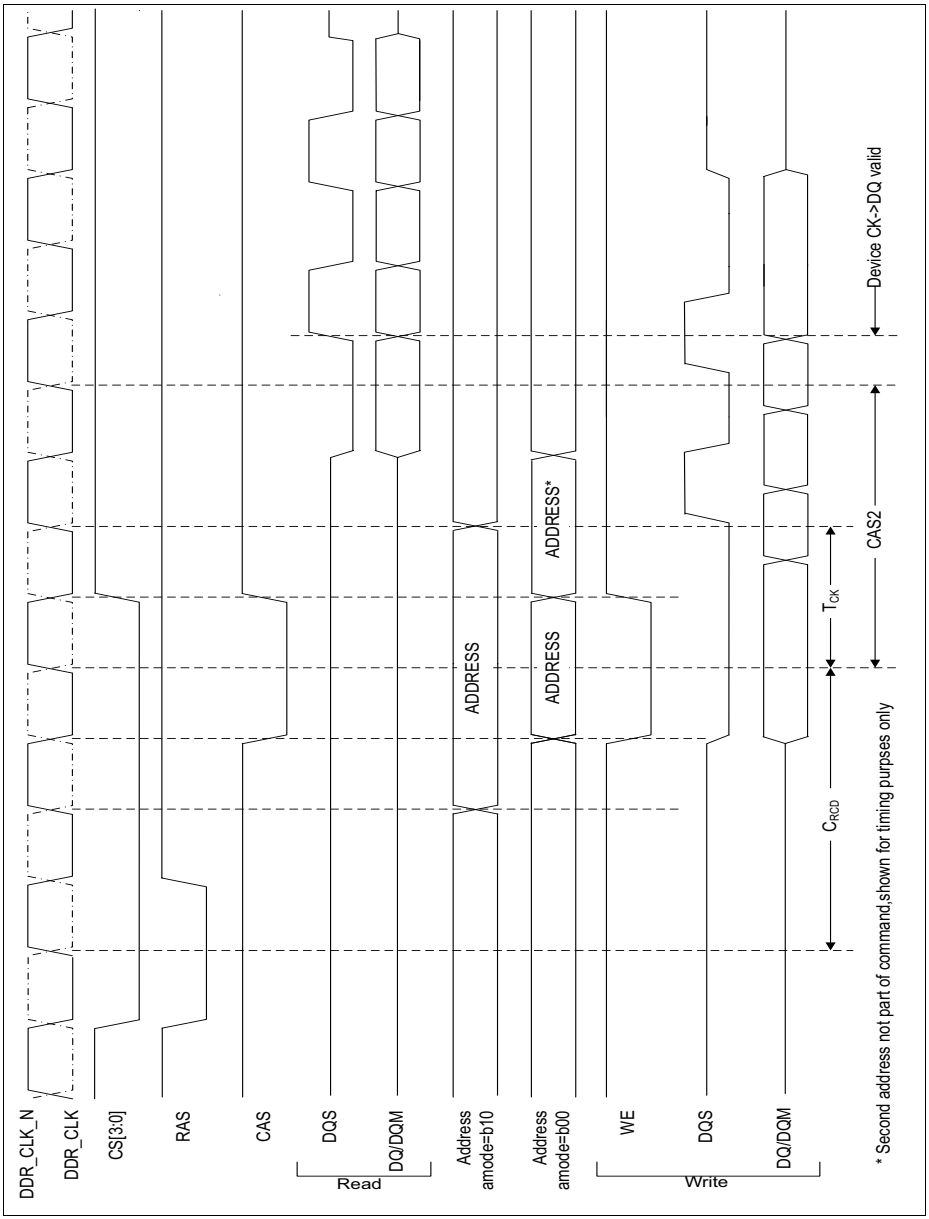


Figure 15-43 Example DDR Waveform

Notes on **Figure 15-43**

1. The DDR clock is a differential signal with the positive clock edge defined as the time when a rising edge of DDR_CLK crosses a falling edge on DDR_CLK_N
2. Two different modes for address generation are available. See **"SDRAM Addressing Scheme" on Page 15-125** for information.
3. CAS is shown for a burst length of 4. Address for amode=b00 and b01 is shown for burst length 2 to clarify differences in addressing modes.
4. The address will only change if necessary. The final address change shown on the waveforms will therefore only occur if a further access has been pipelined. If no access is pending, the last address will remain on the bus.

15.19.1 DDR Mode Address Outputs

There are two options for generating the address outputs to DDR memory.

Option one is for the address for a DDR memory access to be generated in phase with the rising edge of the DDR device clock. This allows a whole clock cycle of setup for the address but means that the address cannot be incremented every clock cycle without timing violations. This prevents burst lengths of two being used for DDRAM but is the simplest mode to configure. Set **EBU_DLLCON.AMODE** to 01_B for this mode.

As a second option, the DDR addresses can be generated with the same timing as the DDR control signals. This will work if the address line loading is closely matched to the clock signal loading. The exact amount of mismatch that can be tolerated will depend on the implementation and required operating frequency. Set **EBU_DLLCON.AMODE** to 00_B for this mode.

15.19.2 DDRAM Initialization sequence

DDRAMs must be initialised in the same way as SDRAMs before being used. Application of power must be followed by 200 µs pause (timed by software) with a stable clock. Then a Precharge All Banks command must be issued. Following this, the device must go through Auto Refresh Cycles (the number of refresh commands is programmable through **Crfsh** in SDRMCON registers and the number of NOP cycles in between is programmable through **Crc**). At the end of it, the Mode Register must be programmed through the address lines. Following that some number of NOP cycles programmable through **Crsc** in EBU_SDRMCON.

Note: This sequence will be referred to as a "cold start",and is necessary when both the memory and the memory controller have just had power applied. Conversely a "warm start" will be required when the memory controller has just been powered up but data has been retained in the external memory by the use of self refresh mode.

The SDRAM controller will, by default, power up with the DDRAM clock disabled and CKE high in compliance with the JEDEC specification JESD209 for mobile DDRAM. This

is not compatible with JESD79E, the specification for standard DDRAM, which requires CKE to be low.

15.19.2.1 Cold Start Initialisation

Care must be taken during software configuration of Memory Controller to ensure the correct DDRAM initialisation sequence is generated for both cold start and warm start.

The recomended sequence for Memory Controller register initialisation after a cold start when using mobile DDRAM devices requires a pull-up resistor to be attached to the CKE pin[1] and is as follows:-

1. If the EBU is in “nobus” arbitration mode, write to the MODCON register to set a valid arbitration mode which allows accesses to external memory.
2. Write to the appropriate BUSRCONx to define which region has DDRAM connected and the required divide ratio for the DDRAM clock output.[2]
3. For DDR mode, initialise the DLL if required[3].
4. Write to EBU_SDRMCON to configure the controller for the attached DDRAM device(s) and to enable the DDRAM clock. (**SDCMSEL**=0_B and **CLKDIS**=0_B.)
5. All other Memory Controller registers except SDRAM specific registers (i.e. other than those listed below).
6. Wait for 200ms (or the appropriate initialisation delay required by the attached device)
7. Write to EBU_SDRMOD with the "**COLDSTART**" bit set to write the mode register values to the DDRAM mode register.
8. Write to EBU_SDRMREF to configure refresh rate.

15.19.2.2 Warm Start Initialisation

The pull-up resistor needed on the CKE pin for correct cold start initialisation means that mobile DDRAM cannot be used with warm start as CKE will taken high by the pull up as soon as the EBU is disabled which will in turn take the attached device out of self-refresh mode.

The recomended sequence for Memory Controller register initialisation after a warm start when using DDRAM devices is as follows:-

1. If the EBU is in “nobus” arbitration mode, write to the MODCON register to set a valid arbitration mode which allows accesses to external memory.

1) The initialisation sequence for standard DDRAM requires a pull-down resistor on the CKE pin but is otherwise the same.

2) The AGEN field in the appropriate BUSWCONx register will be set automatically to the same value.

3) The DLL is required for DDR if either the internal to external clock ratio is 1:1 or the EBU input clock has an asymmetric duty cycle and the internal to external clock ratio is 1:2 or 1:3.

2. Write to BUSRCONx to define which region has DDRAM connected and the required divide ratio for the DDRAM clock.
3. For DDR mode, trigger a lock of the DLL if required.
4. Write to EBU_SDRMCON to configure the controller for the attached DDRAM device(s) and to enable the DDRAM clock. (**SDCMSEL**=0 and **CLKDIS**=0_B.)
5. Initialise all other Memory Controller registers except SDRAM specific registers.
6. Write to EBU_SDRMOD with the "**COLDSTART**" bit cleared to update the mode register values.

15.19.3 DDR External Bus Clock Generation

The frequency of the DDR Clock is controlled in the same way as SDRAM clock generation (See **“SDRAM External Bus Clock Generation” on Page 15-117**) except that the EBU_BUSRCONx.**AGEN** value of 12_D is used as well as 8_D when determining whether a region has a valid device attached. See **“External Bus Clock Generation” on Page 15-26** for more information on clocking DDR devices.

15.20 LPDDR NVM Flash Support (JEDEC 42.4 LPDDR-NVM Protocol)

This section should be read in conjucntion with **Chapter 15.19, “DDRAM/Mobile DDRAM Support” on Page 15-140**

15.20.1 Overview

The memory controller can be confgured to support NOR flash devices utilising an extended version of the interface protocol used for DDR SDRAM memories. The variations on the protocol can be summarised as follows:

- No refresh required
- No precharge required
- No pipelining of "Row Activate" during a running access possible (only one set of sense AMPS)
- Two clock cycles of RAS during "Row Activate" due to the smaller row size creating the need to load more row address bits
- Longer "Row to Column Delay" required because of longer flash read time
- Extra mode register command needed during initialisation. This maps the command registers of the flash into the memory space at an arbitrary address.
- Support for “status register reads” required.

Due to the complexity of the initialisation sequence, it is not be possible to boot directly from the LPDDR-NVM device. The device initialisation must be handled by code running from the internal flash before accesses are attempted.

Support for the LPDDR-NVM protocol is linked to the support for mobile DDRAM memory and will therefore enable the DDR mode of the SDRAM controller when any

AGEN field is set to 10_D. The memory controller can support one DDRAM memory and one LPDDR- NVM memory simultaneously.

A region is configured for accessing LPDDR-NVM flash by setting the BUSCON.agen field to 10_D.

Pin restrictions on the device do not allow DDR and non-DDR memories to be mixed in the same application unless either extreme care is taken to match the DQ/DQS/DQM loading or the maximum operating frequency is reduced to allow for the differential signal skew.

15.20.2 Implementation Requirements

As this LPDDR NVM flash protocol is based on the DDRAM protocol, implementation will be described as deltas to the DDR implementation described in **Section 15.19**.

For a description of options for address generation timing, see **Section 15.10.4 DLL Operation**.

15.20.3 Initialisation

As the NOR flash does not require precharge or refresh, the mandatory device initialisation sequence consists of the following operations under the control of the boot ROM firmware

- Once power has stabilised, drive CKE to logic ‘1’. This will happen as soon as the EBU is enabled by setting EBU_MODCON.ARBMODE to a value other than 00_B.
- Configure the DLL or set up the EBU_CLK to DDR_CLK ratio to allow DDR accesses without the DLL.
- Enable DDR clock. Clock frequency on the external bus should be 50 MHz maximum.
- The external bus must then remain in either the DESELECT or IDLE command states for 200us.
- Write to mode register 11_B to set the DAI bit in the internal control register of the memory device.
- Wait for $\mathbf{t}_{MRD}$.
- Poll the DAI bit (see **“Status Register Reads” on Page 15-148**)
  - Write to mode register 01_B with address 12_H
  - Wait for tSRR
  - Issue read command to mode register 01 with address 12
  - check state of DAI bit in returned data
- If the DAI bit is not cleared, repeat the mode register read
- Read the device characteristics from status register 0
  - Write to mode register 01_B with address 11_H
  - Wait for tSRR
  - Issue read command to mode register 01 with address 11
  - decode device boot characteristics from returned data

- Program initial values to to DDR flash configuration registers.
- Program initial values to the **EBU_DDRNMOD** register based on “Min CL” and “Max BL” values.

Control can now be code read from the external flash device. This code can optionally reconfigure the EBU parameters for optimally match the attached flash device if this has not been done as part of the initialisation.

15.20.4 Additional Supported Commands

The LPDDR-NVM specification requires two new commands to be implemented. These commands are signalled to the device by reusing two of the commands from the SDRAM/DDRAM protocol. Preactivate and Activate are linked commands used to load an RAB (Row Address Buffer) in the memory device. The Activate command will also load the memory page selected by the RAB into one of the RDBs (Row Data Buffers). The RAB and RDB to be used are selected by the Bank Address used for the Preactive and Active commands.

Table 15-48 Supported LPDDR-NVM Commands

Command	Event	CKE (n-1)	CKE (n)	CS	RAS	CAS	RD/ WR	See Section 15.20.5 for Memory Controller pins	
								A(13:0)	BA(1:0)
Preactivate	Load high address bits into RAB	H	-	L	L	H	L	Address MSBs[1)]	Bank Address
Activate	Load RDB	H	-	L	L	H	H	Address LSBs	

1) See **“Normal operating mode” on Page 15-146** for details of address bit mapping.

15.20.5 Normal operating mode

Normal operating mode is enabled when the **EBU_DDRNCON.MODE** field is set to 0_B. This defines the memory as being suitable for “execute in place” (XIP) operation.

During normal operation, the memory controller will issue PREACTIVE and ACTIVE commands to load a page of the attached memory into an internal buffer of the memory device from where it can be read. These commands are separated by sufficient clock cycles not to violate t_{RP} for the memory device. This delay is set by the **EBU_DDRNCON.CRP** field.

There is then a row to column delay (set with **EBU_DDRNCON.CRCD**) before the column address is issued. The number of address bits required for the column address

is set using the **EBU_DDRNCON.PAGESIZE** field. This is used to inform the memory controller of the page size of the attached memory device.

As the LPDDR NVM is only assumed to have one set of sense amplifiers a row activate cannot be queued before the row to column delay of a previous ACTIVE command has expired.

The **EBU_DDRNCON.MAXADD** field is used to set the size of the device. This performs a similar function to the **EBU_SDRMCON.BANKM** when mapping access addresses to pages in the memroy device.

The memory controller will maintain a set of “page tag” registers. This will allow the memory controller to track the addresses of the four, row data buffers (RDB) in the flash memory. Each page tag will be linked to a particular value of the bank address bits used when accessing the device and hence one particular RDB. The **EBU_DDRNCON.MAXADD** bitfield is used to determine the most significant address bit used for page comparisons and **EBU_DDRNCON.PAGESIZE** is used to determine the least significant address bit.

The memory controller will reuse an RDB under the following condition:

- If an access is to the page that has already been loaded into an RDB, the page tag will be reused, the row activate cycles will be skipped and only the column address will be issued.

If the reuse criterion above does not apply, the memory controller will apply a “least active” algorithm to determine which RDB to use for an access. Each page tag register in the memory controller has a counter and an “active flag”[1)] associated with it. This counter will be incremented when an access to the LPDDR-NVM occurs unless the access uses the page tag, in which case the counter will be set to zero and the active flag set. In the event of an access not matching an active page tags full address then

- As a first case, a inactive page tag will be used an its associated RDB opened
- otherwise, the page tag with the highest count will be reused

If, in either case, more than one page tag matches the condition, then the page tag with the lowest value for bank address will be used.

If the page tag to be used already has the correct value for the PREACTIVE address bits then the PREACTIVE command will be skipped

1) the active flag will only be cleared when an RDB invalidation occurs.

Table 15-49 A_{SRI} and CA to SDA bit Mapping(16 bit port width)

	Com-mand	SDA bit[1)]															
		15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
A_{SRI}	PRE-ACTIVE	BA (1:0)		-	-	-	28	27	26	25	24	23	22	21	20	19	18
	ACTIVE			-	17	16	15	14	13	12	11	10	9	8	7	6	5
CA(n)	READ/ WRITE	BA (1:0)		-	13	12	11	10	9	8	7	6	5	4	3	2	1

1) The JEDEC standard allows for memories of up to 16 GBytes. This implementation only supports memories up to 1 Gbyte requiring A(28:0) of the internal address

Table 15-50 A_{SRI} and CA to SDA bit Mapping(32 bit port width)

	Com-mand	SDA bit[1)]															
		15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
A_{SRI}	PRE-ACTIVE	BA (1:0)		-	-	-	-	28	27	26	25	24	23	22	21	20	19
	ACTIVE			-	18	17	16	15	14	13	12	11	10	9	8	7	6
CA(n)	READ/ WRITE	BA (1:0)		-	14	13	12	11	10	9	8	7	6	5	4	3	2

1) The JEDEC standard allows for memories of up to 16 GBytes. This implementation only supports memories up to 1 Gbyte requiring A(28:0) of the internal address

15.20.6 Status Register Reads

Status register reads are a variation on the mode register write commands used for DDRAM. A mode register write is performed to the device and the next read is then performed on an internal status register of the memory device instead of the memory array.

Status register reads are controlled by accessing the **EBU_DDRNMOD2** register. Writing to **EBU_DDRNMOD2** with a bank address value of 01_B (set by the **EBU_DDRNMOD2.XBA** field) and the **ACT** bit set will trigger the expected mode register write. The address of the status register to be read will be obtained from the **XOPM** field of the **EBU_DDRNMOD2** register. This defines A(11:0) of the external address bus. Bits (13:12) are always set to 00_B.

However as a write to mode register 01 is used as a command to prepare the device for a status register read, the write will be followed (after a delay set by the **CSRR** field in the **EBU_DDRNCON** register) by a read operation using the same value on the address bus as the write. The data returned by this read will be placed in the **EBU_DDRNSRR.SRRDATA0** field if a single device is connected or both **EBU_DDRNSRR.SRRDATA0** and **EBU_DDRNSRR.SRRDATA1** if two 16 bit devices are connected in parallel in a 32 bit configuration.

It is not normally permitted for other commands to be pipelined to the LPDDR NVM before the status register read command has completed. This delay is set by the **EBU_DDRNCON.CSRS** field.

While a status register operation is in progress, the **ACT** bit will remain set. Once the operation has completed, the bit will be cleared by hardware.

15.20.7 Discrete Mode Register Writes

when operating an LPDDR_NVM memory it is necessary to perform writes to mode registers which are not connected to device initialisation. These discrete mode register writes are using to configure the device programming interface.

Mode register 11_B is available for these functions and is accessed by writing to the **EBU_DDRNMOD2** register with the **ACT** bit set and the **XBA** field set to 11_B. The data to be written to the register is contained in the **XOPM** field of the **EBU_DDRNMOD2** register. This field contains twelve bits of data and will be output on A[11:0] of the external address bus. The unused bits of the external address bus will be set to 0_B.

15.20.8 Page Preload

This register has two uses. The first applies when **EBU_DDRNCON.MODE** is set to 1_B. In this case, the memory is defined as being unsuitable for “execute in place” XIP operation and therefore needs to be treated in the same way as a NAND flash memory.

If a value is written to the **EBU_DDRNPRLD** register, the contents will be treated as the MEMPORT address of a memory page to be preloaded into the device buffer. The memory controller will issue the PREACTIVE and ACTIVE command sequence as detailed in **“Normal operating mode” on Page 15-146**, but will not expect any data to be returned and so will not issue the final READ command. The page tags in the memory controller will be updated to show that the page is available.

This is intended to enable support for a NAND flash memory with the LPDDR NVM type interface. The proposed method of access would be to issue the page load and then wait for the device t_{RCD} to expire. Accesses to the preloaded page could then be issued. It would be the responsibility of software to ensure that a premature access to the page was not accidentally issued by either polling the device status register or using a dead reckoning timer to measure the page load time of the device.

Accesses to an unopened page will result in an error being returned on the internal bus.

If the CSA function is enabled for the LPDDR-NVM, then bit 28 of the register (corresponding to $A_{MEMPORT}(28)$ will be monitored and used to determine which of the two LPDDR-NVM memories is affected by the preload operation.

It is invalid for two RDBs to have overlapping addresses. The memory controller hardware will detect if the address to be preloaded overlaps another page tag other than that targetted by the page load operation and prevent the page load from taking place. This will not be flagged to the controlling software as the requested page is already available.

For the second use, see **"Overlay Window Control" on Page 15-150**.

15.20.9 Page Tag Control

Page tags are set active when first used. There are some circumstances in which the contents of the RDBs in the memory are no longer guaranteed to be an accurate copy of the device contents and in these cases the RDBs need to be invalidated. This is done by resetting the page tags to inactive. The next accesses to the memory will then force a reload of the RDBs from the memory contents. The following conditions will automatically invalidate the page tags:

- Writing to any of mode registers 00_B, 01_B or 11_B either by triggering an initialisation sequence (write to **EBU_DDRNMOD**) or by a mode register write (write to **EBU_DDRNMOD2**).

The page tags can be invalidated under software control by writing 0_B to the **EBU_DDRNTAGx (x=0-3).ACTIVE** bitfield of the appropriate register. Writing 1_B to this bit field has no effect and will not activate an inactive page tag. This operation does not invalidate the RDB in the memory device

15.20.10 Overlay Window Control

The overlay window is controlled using mode register 11_B in the memory device. Mode register 11_B can be accessed using the **EBU_DDRNMOD2** register to trigger discrete mode register writes (see **"Discrete Mode Register Writes" on Page 15-149**).

Once enabled, the overlay window occupies part of the memory device address space and can be written to. Note that writes to the overlay window are via the RDBs and that the RDB will therefore need to be flushed to transfer the data to the overlay window.

If the memory device supports the optional FLUSH bit in mode register 11, then the data can be flushed to the Overlay Window by using a discrete mode register write to write 1 to the FLUSH bit.

Otherwise, the flush operation can be triggered by sending an ACTIVE command to the appropriate RDB. To do this, use the **EBU_DDRNPRLD** register to trigger the command sequence using the **EBU_DDRNPRLD.BA** field to select the correct RDB. Which RDB (or RDBs) is currently allocated to the Overlay Window address space can be determined by polling the **EBU_DDRNTAGx (x=0-3)** registers.

15.20.11 Clearing The Read FIFO error flag

Writing to the **EBU_DDRNCON** will clear the read FIFO error flag in the SDRAM status register. This is in addition to a write to the **EBU_SDRMCON** register clearing the flag.

15.20.12 LPDDR-NVM Access Programmable Parameters

The following parameters can be used to configure accesses to LPDDR-NVM memories.

Table 15-51 LPDDR-NVM Access Programmable Parameters

Parameter	Function	Register
MAXADD	Highest order address bit used by the NVM memory	**EBU_DDRNCON**
PAGESIZE	Size of a page in the NVM memory	**EBU_DDRNCON**
CRSC	Number of NOP cycles after a mode register set command	**EBU_DDRNCON**
CRP	Number of NOP cycles between a PREACTIVE and ACTIVE command	**EBU_DDRNCON**
CSRS	Number of delay cycles between a status register read and the next command on the bus	**EBU_DDRNCON**
CSRR	Number of delay cycles between a mode register write to MR01 and the associated status register read	**EBU_DDRNCON**
CRCD	Number of NOP cycles between a row activate and a column address	**EBU_DDRNCON**
MODE	Operating mode for attached memory. Either XIP (execute in place) or software controlled page load (NAND mode)	**EBU_DDRNCON**
XBA	Bank address value to be used for an extended mode register access	**EBU_DDRNMOD**
OPMODE	To specify write operation mode: only BURST_WRITE is recognized	**EBU_DDRNMOD**
XOPM	Value to be written to the extended mode register	**EBU_DDRNMOD**
CASLAT	CAS latency setting to be used for device accesses	**EBU_DDRNMOD**
BTYP	To specify burst operation mode: SEQUENTIAL	**EBU_DDRNMOD**
BURSTL	To specify burst length: 4, 8 or 16	**EBU_DDRNMOD**
XBA	Bank address value to be used for an extended mode register access to the second extended mode register.	**EBU_DDRNMOD2**

Table 15-51 LPDDR-NVM Access Programmable Parameters (cont'd)

Parameter	Function	Register
XOPM	Value to be written to the second extended mode register	EBU_DDRNMOD2
BA	Bank address to be used for page preloaded	EBU_DDRNPRLD
PAGE	Internal, byte address of page to be preloaded	EBU_DDRNPRLD

15.21 EBU Registers

[cover refid=Register_map_24] This section describes the registers and programmable parameters of the EBU. All these registers can be read in User Mode, but can only be written in Supervisor Mode.

All registers are reset by the module reset.

Table 15-52 Registers Address Space -Flash Registers

Module	Base Address	End Address	Note
EBU	$F800\ 0000_H$	$F800\ 03FF_H$	-

Table 15-53 Registers Overview EBU Control Registers

Register Short Name	Register Long Name	Offset Address	Access Mode		Description see
			Read	Write	
EBU_CLC	EBU Clock Control Register	0000_H	U, SV, 32, 64	SV, 32, 64, BE	Page 15-156
EBU_MODCON	EBU Configuration Register	0004_H	U, SV, 32, 64	SV, 32, 64	Page 15-158
EBU_MODID	EBU Module ID Register	0008_H	U, SV, 32, 64	SV, 32, 64	Page 15-200
EBU_USERCON	EBU Test/Control Configuration Register	$000C_H$	U, SV, 32, 64	SV, 32, 64	Page 15-199
EBU_EXTBOOT	EBU External Boot Control Register	0010_H	U,SV, 32	SV, 32[1)]	Page 15-161
	reserved	0014_H	BE	BE	
EBU_ADDRSEL0	EBU Address Select Register 0	0018_H	U, SV, 32, 64	SV, 32, 64	Page 15-163
EBU_ADDRSEL1	EBU Address Select Register 1	$001C_H$	U, SV, 32, 64	SV, 32, 64	Page 15-163
EBU_ADDRSEL2	EBU Address Select Register 2	0020_H	U, SV, 32, 64	SV, 32, 64	Page 15-163
EBU_ADDRSEL3	EBU Address Select Register 3	0024_H	U, SV, 32, 64	SV, 32, 64	Page 15-163
EBU_BUSRCON0	EBU Bus Configuration Register 0	0028_H	U, SV, 32, 64	SV, 32, 64	Page 15-165

Table 15-53 Registers Overview EBU Control Registers (cont'd)

Register Short Name	Register Long Name	Offset Address	Access Mode		Description see
			Read	Write	
EBU_BUSRAP0	EBU Bus Access Parameter Register 0	$002C_H$	U, SV, 32, 64	SV, 32, 64	Page 15-172
EBU_BUSWCON0	EBU Bus Configuration Register 0	0030_H	U, SV, 32, 64	SV, 32, 64	Page 15-169
EBU_BUSWAP0	EBU Bus Access Parameter Register 0	0034_H	U, SV, 32, 64	SV, 32, 64	Page 15-175
EBU_BUSRCON1	EBU Bus Configuration Register 1	0038_H	U, SV, 32, 64	SV, 32, 64	Page 15-165
EBU_BUSRAP1	EBU Bus Access Parameter Register 1	$003C_H$	U, SV, 32, 64	SV, 32, 64	Page 15-172
EBU_BUSWCON1	EBU Bus Configuration Register 1	0040_H	U, SV, 32, 64	SV, 32, 64	Page 15-169
EBU_BUSWAP1	EBU Bus Access Parameter Register 1	0044_H	U, SV, 32, 64	SV, 32, 64	Page 15-175
EBU_BUSRCON2	EBU Bus Configuration Register 2	0048_H	U, SV, 32, 64	SV, 32, 64	Page 15-165
EBU_BUSRAP2	EBU Bus Access Parameter Register 2	$004C_H$	U, SV, 32, 64	SV, 32, 64	Page 15-172
EBU_BUSWCON2	EBU Bus Configuration Register 2	0050_H	U, SV, 32, 64	SV, 32, 64	Page 15-169
EBU_BUSWAP2	EBU Bus Access Parameter Register 2	0054_H	U, SV, 32, 64	SV, 32, 64	Page 15-175
EBU_BUSRCON3	EBU Bus Configuration Register 3	0058_H	U, SV, 32, 64	SV, 32, 64	Page 15-165
EBU_BUSRAP3	EBU Bus Access Parameter Register 3	$005C_H$	U, SV, 32, 64	SV, 32, 64	Page 15-172
EBU_BUSWCON3	EBU Bus Configuration Register 3	0060_H	U, SV, 32, 64	SV, 32, 64	Page 15-169
EBU_BUSWAP3	EBU Bus Access Parameter Register 3	0064_H	U, SV, 32, 64	SV, 32, 64	Page 15-175
EBU_SDRMCON	EBU, SDRAM Control Register	0068_H	U, SV, 32, 64	SV, 32, 64	Page 15-178

Table 15-53 Registers Overview EBU Control Registers (cont'd)

Register Short Name	Register Long Name	Offset Address	Access Mode		Description see
			Read	Write	
EBU_SDRMOD	EBU, SDRAM Mode Register	$006C_H$	U, SV, 32, 64	SV, 32, 64	Page 15-180
EBU_SDRMREF	EBU, SDRAM Refresh Control Register	0070_H	U, SV, 32, 64	SV, 32, 64	Page 15-183
EBU_SDRSTAT	EBU, SDRAM Status Register	0074_H	U, SV, 32, 64	SV, 32, 64	Page 15-185
EBU_DLLCON	EBU, DLL Control Register	0078_H	U, SV, 32, 64	SV, 32, 64	Page 15-187
EBU_DDRNCON	EBU, LPDDR NVM Control Register	$007C_H$	U, SV, 32, 64	SV, 32, 64	Page 15-190
EBU_DDRNMOD	EBU, LPDDR NVM Mode Register	0080_H	U, SV, 32, 64	SV, 32, 64	Page 15-192
EBU_DDRNMOD2	EBU, LPDDR NVM Extended Mode Register	0084_H	U, SV, 32, 64	SV, 32, 64	Page 15-194
EBU_DDRNSRR	EBU, LPDDR NVM Page Preload Register	0088_H	U, SV, 32, 64	SV, 32, 64	Page 15-196
EBU_DDRNPRLD	EBU, LPDDR NVM Page Preload Register	$008C_H$	U, SV, 32	SV, 32	Page 15-197
EBU_DDRNTAG0	EBU, LPDDR NVM Page Tag Register	0090_H	U, SV, 32, 64	SV, 32, 64	Page 15-198
EBU_DDRNTAG1	EBU, LPDDR NVM Page Tag Register	0094_H	U, SV, 32, 64	SV, 32, 64	Page 15-198
EBU_DDRNTAG2	EBU, LPDDR NVM Page Tag Register	0098_H	U, SV, 32, 64	SV, 32, 64	Page 15-198
EBU_DDRNTAG3	EBU, LPDDR NVM Page Tag Register	$009C_H$	U, SV, 32, 64	SV, 32, 64	Page 15-198
-	reserved	$00A0_H$ - $03FC_H$	BE	BE	

1) The EXTBOOT register is only writable when the BOOT_ACTIVE flag from the SCU is set.

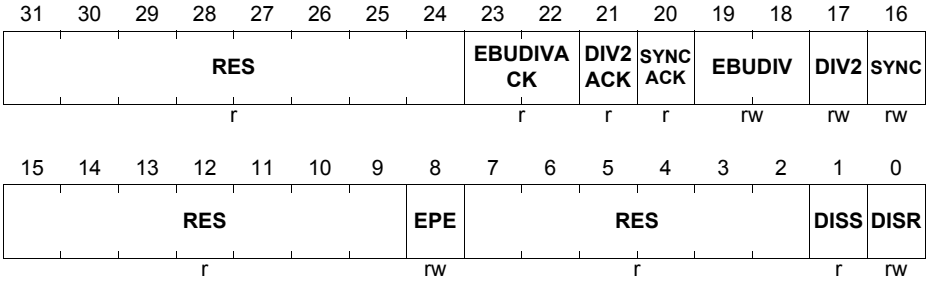
Access Restrictions

Note: The EBU registers are accessible only through word or double-word accesses. Half-word and byte accesses on EBU registers will generate a bus error. Accesses

to a 64bit word only partially populated with accessible registers will cause a bus error. Writes to unused address space, or writes to the endinit protected CLC register will also cause an error .

15.21.1 Clock Control Register, CLC

EBU_CLC
EBU Clock Control Register **(000_H)** **Reset Value: $0055\ 0000_H$**



Field	Bits	Type	Description
DISR	0	rw	**EBU Disable Request Bit**[1)] This bit is used for enable/disable control of the EBU. 0_B EBU disable is not requested 1_B EBU disable is requested
DISS	1	r	**EBU Disable Status Bit** DISS is always read as 0, as accessing the EBU will automatically enable it. 0_B EBU is enabled (default after reset) 1_B EBU is disabled
RES	7:2	r	**Reserved** Read as 0; should be written with 0.
EPE	8	rw	**Endinit Protection Enable**[2)] 0_B Disable Endinit protection of the CLC register (default after reset). 1_B Enable Endinit protection of the CLC register.
RES	15:9	r	**Reserved** Read as 0; should be written with 0.

Field	Bits	Type	Description
SYNC	16	rw	**EBU Clocking Mode** 0_B request EBU to run asynchronously to processor clock and use separate clock source 1_B request EBU to run synchronously to processor (default after reset)
DIV2	17	rw	**DIV2 Clocking Mode** 0_B standard clocking mode. clock input selected by SYNC bitfield (default after reset). 1_B request EBU to run off processor clock divided by 2.
EBUDIV	19:18	rw	**EBU Clock Divide Ratio** 00_B request EBU to run off input clock 01_B request EBU to run off input clock divided by 2 (default after reset) 10_B request EBU to run off input clock divided by 3 11_B request EBU to run off input clock divided by 4
SYNCACK	20	r	**EBU Clocking Mode Status** 0_B the EBU is asynchronous to the SRI bus clock and is using a separate clock source 1_B EBU is synchronous to the SRI bus clock (default after reset)
DIV2ACK	21	r	**DIV2 Clocking Mode Status** 0_B EBU is using standard clocking mode. clock input selected by SYNC bitfield (default after reset). 1_B EBU is running off processor clock divided by 2.
EBUDIVACK	23:22	r	**EBU Clock Divide Ratio Status** 00_B EBU is running off input clock (default after reset) 01_B EBU is running off input clock divided by 2 10_B EBU is running off input clock divided by 3 11_B EBU is running off input clock divided by 4
RES	31:24	r	**Reserved** Read as 0; should be written with 0.

1) *While the DISR bit is implemented in the EBU, it connects to the standby logic which will disable the clock tree. Standby mode will be exited automatically when an attempt is made to access the EBU.*

2) *This register can be Endinit-protected after initialization. Writing to this register in this state will cause the EBU to generate an SRI Error.*

15.21.2 Configuration Register, MODCON

EBU_MODCON
EBU Configuration Register **(004_H)**
Internal Boot Reset Value: $3000\ 0020_H$

EBU_MODCON
EBU Configuration Register **(004_H)**
External Boot Reset Value: $3000\ 0060_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ALE	BUSSTATE	ACCSINHACK	ACCSINH	RES	OCDS_SUSP_DIS	FAST_SRI	FIFO_BYPASS	LOCKTIMEOUT							
rw	rh	r	rw	r	rw	rw	rw	rw							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TIMEOUTC								ARB MODE		ARB SYNC	EXTLOCK	CLK_COMB	SDTRI	LCKABRT	STS
				rw				rw		rw	rw	rw	rwh	rwh	r

Field	Bits	Type	Description
STS	0	r	**Memory Status Bit** Software access to the $\overline{WAIT}$ input pin to the EBU.
LCKABRT	1	rwh	**Lock Abort** This is a status bit which is set when a chip select lock has been cancelled by a program fetch. The flag is cleared by writing 1_B to the field. See **Section 15.9.1** 0_B Lock function is operating normally 1_B Lock function has been aborted by processor instruction read from locked device
SDTRI	2	rw	**SDRAM Tristate** 0_B SDRAM control signals are driven by the EBU when the EBU does not own the external bus. SDRAM cannot be shared. 1_B SDRAM control signals are tri-stated by the EBU when the EBU does not own the external bus. The SDRAM can be shared. *Note: The signals affected by this setting are CKE, SDCLKO, CAS and RAS*

Field	Bits	Type	Description
CLK_COMB	3	rw	**Combined External Bus Clock** Burst flash protocol and SDRAM protocol devices use the same external clock when set. 0_B The SDRAM and synchronous state machines use clocks on separate pins 1_B Both state machines use the clock on BFCLKO when accessing external memories
EXTLOCK	4	rw	**External Bus Lock Control** Allows the external bus arbitration to be locked with the EBU owning the bus. 0_B External bus is not locked after the EBU gains ownership 1_B External bus is locked after the EBU gains ownership
ARBSYNC	5	rw	**Arbitration Signal Synchronization Control** Assumed status of the arbitration control signals, $\overline{BREQ}$ and $\overline{HLDA}$ 0_B Arbitration inputs are synchronous 1_B Arbitration inputs are asynchronous, use two resynchronisation flip-flops.
ARBMODE	7:6	rw	**Arbitration Mode Selection** Operating mode of the external bus arbitration 00_B No Bus arbitration mode selected 01_B Arbiter Mode arbitration mode selected 10_B Participant arbitration mode selected 11_B Sole Master arbitration mode selected
TIMEOUTC	15:8	rw	**Bus Time-out Control** This bit field determines the number of inactive cycles after the EBU gains ownsership of the external bus before an arbitration time-out occurs and re-arbitration can occur. 00_H Time-out is disabled. 01_H Time-out is generated after 1×8 clock cycles. $\cdots_H$ … FF_H Time-out is generated after 255×8 clock cycles.

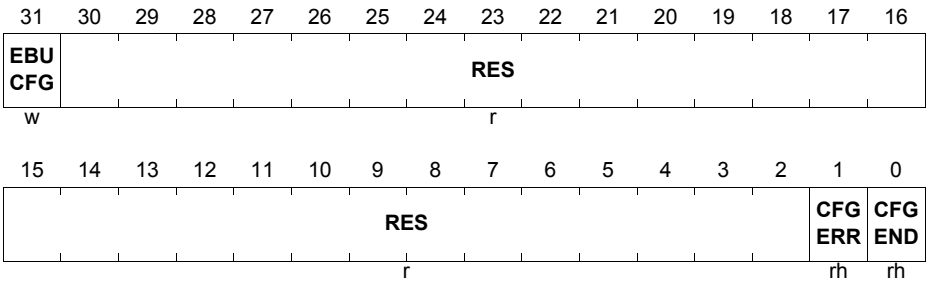
Field	Bits	Type	Description
LOCKTIMEOUT	23:16	rw	**Lock Timeout Counter Preload** Value to be preloaded into the timeout counter for the arbitration lock. *Note: (see **Section 15.9.1**)*
FIFO_BYPASS	24	rw	**Read Mode for SDRAM/DDR Memories** 0_B Use Data FIFO for read data (default) 1_B Bypass the FIFO. See **"FIFO Bypass Mode" on Page 15-25** for detailed description.
FAST_SRI	25	rw	**Clock Cycles used for SRI Address Decode** 0_B Use two clock cycles for address decode (default after reset) 1_B Use one clock cycle for address decode. See **"Address Comparison" on Page 15-48** for a detailed description.
OCDS_SUSP_DIS	26	rw	**OCDS SUSPEND Disable** The EBU external arbitration will normally be disabled with the EBU owning the external bus while OCDS is active. Setting this bit will allow external bus arbitration to continue operation. See **Section 15.11.7**
RES	27	r	**Reserved** write with 0_H
ACCSINH	28	rw	**Access Inhibit request** Prevent any transactions except for processor initiated transfers from accessing the memory regions 0_B Accesses enabled 1_B Accesses inhibited *Note: (see **Section 15.9**)*
ACCSINHACK	29	r	**Access inhibit acknowledge** 0_B Port normal operation possible 1_B Port accesses have been inhibited (except processor) *Note: (see **Section 15.9**)*

Field	Bits	Type	Description
BUSSTATE	30	rh	**External Bus State** Status bit controlled by the arbitration logic (See **"External Bus Arbitration" on Page 15-28**) reflecting the ownership of the external memory bus. 0_B The EBU does not own the external bus and attached memories cannot be accessed. 1_B The EBU owns the external bus.
ALE	31	rw	**ALE Mode** Switch the $\overline{ADV}$ output to be an active high ALE signal instead of active low $\overline{ADV}$. 0_B Output is $\overline{ADV}$ 1_B Output is ALE

15.21.3 External Boot Configuration Control Register, EXTBOOT

EBU_EXTBOOT

EBU External Boot Configuration Register(00010_H) **Reset Value: $0000\ 0001_H$**



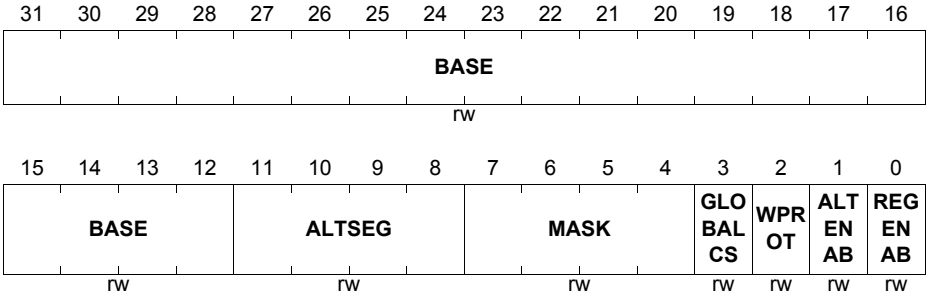
Field	Bits	Type	Description
CFGEND	0	rh	**Configuration End** 0_B Configuration fetch is running 1_B Configuration fetch has completed or not started
CFGERR	1	rh	**Configuration Fetch Error** 0_B No error 1_B The configuration fetch has returned a word with all bits set. This indicates an unprogrammed or missing flash

Field	Bits	Type	Description
EBUCFG	31	w	**Configuration Word Fetch** Write 1_B to trigger automatically set the EBU to arbiter arbitration mode and fetch a configuration word from external memory. Always reads 0_B
RES	30:2	r	**Reserved** Read as 0; must be written with 0.

15.21.4 Address Select Register, ADDRSELx

EBU_ADDRSELx (x = 1-3)
EBU Address Select Register 1-3 (018_H+x*4_H)
ADDRSEL[3:1] - Reset Value: 0000 0000$_H$

EBU_ADDRSEL0
EBU Address Select Register 0 (018_H)
ADDRSEL0 - Reset Value: A000 0001$_H$



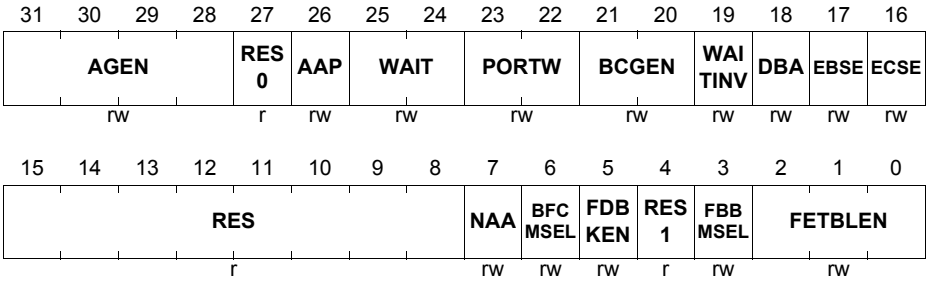
Field	Bits	Type	Description
REGENAB	0	rw	**Memory Region Enable** 0_B Memory region is disabled (default after reset[1)]). 1_B Memory region is enabled.
ALTENAB	1	rw	**Alternate Segment Comparison Enable** 0_B ALTSEG is never compared to SRI address (default after reset). 1_B ALTSEG is always compared to SRI address.
WPROT	2	rw	**Memory Region Write Protect** 0_B Region is enabled for write accesses 1_B Region is write protected.
GLOBALCS	3	rw	**Combined Chip Select Control** Controls whether the $\overline{\text{CSCOMB}}$ output should be asserted for valid accesses to this region. 0_B $\overline{\text{CSCOMB}}$ not asserted 1_B CSCOMB asserted

Field	Bits	Type	Description
MASK	7:4	rw	**Memory Region Address Mask** Specifies the number of right-most bits in the base address starting at bit 26, which should be included in the address comparison. Bits [31:27] will always be part of the comparison.
ALTSEG	11:8	rw	**Memory Region Alternate Segment** Alternate segment to be compared to SRI address bit [31:28].
BASE	31:12	rw	**Memory Region Base Address** Base address to be compared to SRI address in conjunction with the mask control.

1) except for ADDRSEL0, **REGENAB in register ADDRSEL0 is 1_B after reset.**

15.21.5 Bus Configuration Register, BUSRCONx

EBU_BUSRCONx (x = 0-3)
EBU Bus Configuration Register (028_H+x*10_H) **Reset Value: 00D3 0040_H**



Field	Bits	Type	Description
FETBLEN	2:0	rw	**Burst Length for Synchronous Burst** Defines maximum number of burst data cycles which are executed by Memory Controller during a burst access to a Synchronous Burst device. 000_B 1 data access (default after reset). 001_B 2 data accesses. 010_B 4 data accesses. 011_B 8 data accesses. $1xx_B$ reserved.
FBBMSEL	3	rw	**Synchronous burst buffer mode select** 0_B Burst buffer length defined by value in fetblen (default after reset). 1_B Continuous mode. All data required for transaction is transferred in a single burst.
RESERVED	4	r	**Reserved** 0_B Reserved bit always reads ‘0’.
FDBKEN	5	rw	**Burst FLASH Clock Feedback Enable** 0_B BFCLK feedback not used. 1_B Incoming data and control signals (from the Burst FLASH device) are re-synchronised to the BFCLKI input.

Field	Bits	Type	Description
BFCMSEL	6	rw	**Burst Flash Clock Mode Select** 0_B Burst Flash Clock runs continously with values selected by this register 1_B Burst Flash Clock is disabled between accesses
NAA	7	rw	**Enable flash non-array access workaround** set to logic one to enable workaround when region is accessed with address bit 28 set. See **"Flash Non-Array Access Support" on Page 15-101**
RES1	15:8	r	**Reserved** 00_H Reserved Value
ECSE	16	rw	**Early Chip Select for Synchronous Burst** 0_B CS is delayed. 1_B CS is not delayed. *Note: (see **Control of ADV & Other Signal Delays During Asynchronous Accesses** and **Control of ADV & Control Signal Delays During Synchronous Accesses**)*
EBSE	17	rw	**Early Burst Signal Enable for Synchronous Burst** 0_B ADV is delayed. 1_B ADV is not delayed. *Note: (see **Control of ADV & Other Signal Delays During Asynchronous Accesses** and **Control of ADV & Control Signal Delays During Synchronous Accesses**)*

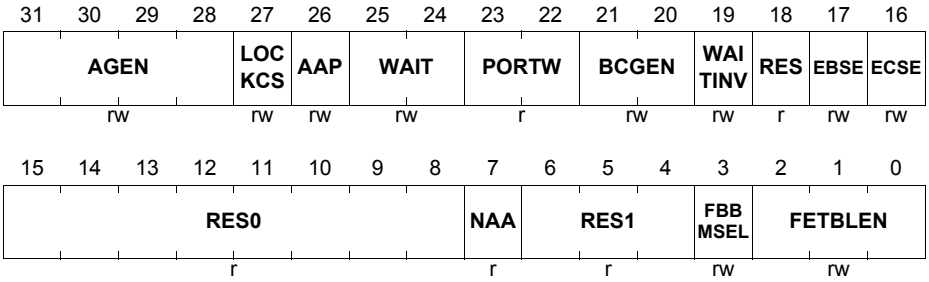
Field	Bits	Type	Description
DBA	18	rw	**Disable Burst Address Wrapping** 0_B Memory Controller automatically re-aligns any non-aligned synchronous burst access so that data can be fetched from the device in a single burst transaction. 1_B Memory Controller always starts any burst access to a synchronous burst device at the address specified by the SRI request. Any required address wrapping must be automatically provided by the Burst FLASH device. *Note: Care must be taken with the use of this feature. The Burst capable device must be programmed to wrap at the appropriate address boundary prior to selection of this mode.* ***"Critical Word First Read Accesses" on Page 15-96***
WAITINV	19	rw	**Reversed polarity at WAIT** 0_B **OFF**, input at WAIT pin is active low (default after reset). 1_B **Polarity reversed**, input at WAIT pin is active high.
BCGEN	21:20	rw	**Byte Control Signal Control** This bit field selects the timing mode of the byte control signals. 00_B Byte control signals follow chip select timing. 01_B Byte control signals follow control signal timing ($\overline{RD}$, RD/$\overline{WR}$) (default after reset). 10_B Byte control signals follow write enable signal timing (RD/$\overline{WR}$ only). 11_B SDRAM access type. Signals used for DQM.
PORTW	23:22	rw	**Device Addressing Mode** See **Table 15-16** and **Table 15-18**

Field	Bits	Type	Description
WAIT	25:24	rw	**External Wait Control** Function of the WAIT input. This is specific to the device type (i.e. the agen field). **For Asynchronous Devices, see "External Extension of the Command Phase by WAIT" on Page 15-76** **For Synchronous Burst Devices, see "External Cycle Control via the WAIT Input" on Page 15-99**
AAP	26	rw	**Asynchronous Address phase:** Enables an access mode for synchronous memories where the clock is not started until after the address hold phase. 0_B Clock is enabled at beginning of access. 1_B Clock is enabled at after address phase.
RES0	27	r	**Reserved, always 0**
AGEN	31:28	rw	**Device Type for Region** See **Section 15.14.1 Programmable Device Types**

*Note: When in external boot mode (see **Page 15-41**) the reset value of BUSCON0 is overwritten automatically (subsequent to the release of reset) as a result of the external Boot Configuration Value fetch.*

15.21.6 Bus Write Configuration Register, BUSWCONx

EBU_BUSWCONx (x = 0-3)
EBU Bus Write Configuration Register(030_H+x*10_H) **Reset Value: 00D3 0000_H**



Field	Bits	Type	Description
FETBLEN	2:0	rw	**Burst Length for Synchronous Burst** Defines maximum number of burst data cycles which are executed by Memory Controller during a burst access to a Synchronous Burst device. 000_B 1 data access (default after reset). 001_B 2 data accesses. 010_B 4 data accesses. 011_B 8 data accesses. $1xx_B$ reserved.
FBBMSEL	3	rw	**Synchronous burst buffer mode select** 0_B Burst buffer length defined by value in FETBLEN (default after reset). 1_B Continuous mode. All data required for transaction transferred in single burst
RES	6:4	r	**Reserved, always reads 0**
NAA	7	r	**Enable flash non-array access workaround** set to logic one to enable workaround when region is accessed with address bit 28 set. See **"Flash Non-Array Access Support" on Page 15-101**. Mirror of equivalent field in BUSRCON register.
RES0	15:8	r	**Reserved** 00_H Reserved Value

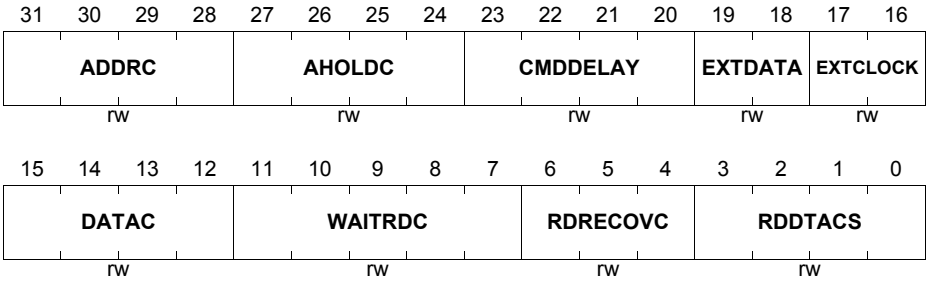
Field	Bits	Type	Description
ECSE	16	rw	**Early Chip Select for Synchronous Burst** 0_B CS is delayed. 1_B CS is not delayed. *Note: (see **Control of ADV & Other Signal Delays During Asynchronous Accesses** and **Control of ADV & Control Signal Delays During Synchronous Accesses**)*
EBSE	17	rw	**Early Burst Signal Enable for Synchronous Burst** 0_B ADV is delayed. 1_B ADV is not delayed. *Note: (see **Control of ADV & Other Signal Delays During Asynchronous Accesses** and **Control of ADV & Control Signal Delays During Synchronous Accesses**)*
RES1	18	r	**Reserved, always reads 0**
WAITINV	19	rw	**Reversed polarity at WAIT** 0_B **OFF**, input at WAIT pin is active low (default after reset). 1_B **Polarity reversed**, input at WAIT pin is active high.
BCGEN	21:20	rw	**Byte Control Signal Control** This bit field selects the timing mode of the byte control signals. 00_B Byte control signals follow chip select timing. 01_B Byte control signals follow control signal timing ($\overline{RD}$, RD/$\overline{WR}$) (default after reset). 10_B Byte control signals follow write enable signal timing (RD/$\overline{WR}$ only). 11_B Reserved.
PORTW	23:22	r	**Device Addressing Mode** See **Table 15-16** and **Table 15-17**

Field	Bits	Type	Description
WAIT	25:24	rw	**External Wait Control** Function of the WAIT input. This is specific to the device type (i.e. the agen field). **For Asynchronous Devices, see "External Extension of the Command Phase by WAIT" on Page 15-76** **For Synchronous Burst Devices, see "External Cycle Control via the WAIT Input" on Page 15-99**
AAP	26	rw	**Asynchronous Address phase:** Enables an access mode for synchronous memories where the clock is not started until after the address hold phase. 0_B Clock is enabled at beginning of access. 1_B Clock is enabled at after address phase.
LOCKCS	27	rw	**Lock Chip Select** Enable Chip Select for Automatic Locking in the event of a write access 0_B Chip Select cannot be locked (default after reset). 1_B Chip Select will be automatically locked when written to from the processor data port.
AGEN	31:28	rw	**Device Type for Region** See **Section 15.14.1 Programmable Device Types**

*Note: When in external boot mode (see **Page 15-41**) the reset value of BUSCON0 is overwritten automatically (subsequent to the release of reset) as a result of the external Boot Configuration Value fetch.*

15.21.7 Bus Read Access Parameter Register, BUSRAPx

EBU_BUSRAPx (x = 0-3)
EBU Bus Read Access Parameter Register
($02C_H$+x*10_H) **Reset Value: FFFF FFFF$_H$**



Field	Bits	Type	Description
RDDTACS	3:0	rw	**Recovery Cycles between Different Regions** This bit field determines the number of clock cycles of the Recovery Phase between consecutive accesses directed to different regions or different types of access. See **"Recovery Phase (RP)" on Page 15-67** and **"SDRAM Recovery Phases" on Page 15-135** 0000_B No Recovery Phase clock cycles available. 0001_B 1 clock cycle selected. …$_B$ … 1110_B 14 clock cycles selected. 1111_B 15 clock cycles selected.
RDRECOVC	6:4	rw	**Recovery Cycles after Read Accesses** This bit field determines the basic number of clock cycles of the Recovery Phase at the end of read accesses. 000_B No Recovery Phase clock cycles available. 001_B 1 clock cycle selected. …$_B$ … 110_B 6 clock cycles selected. 111_B 7 clock cycles selected.

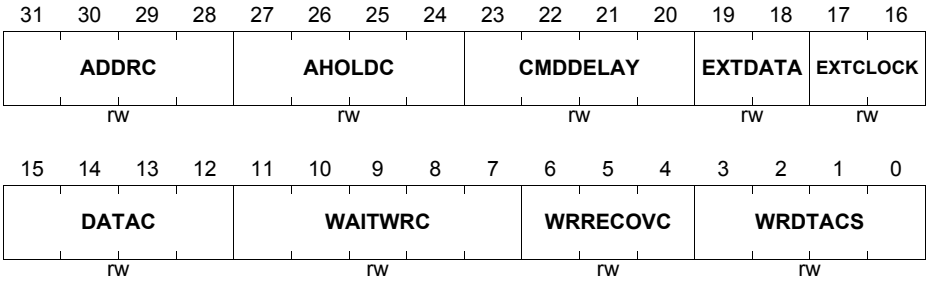
Field	Bits	Type	Description
WAITRDC	11:7	rw	**Programmed Wait States for read accesses** Number of programmed wait states for read accesses. For synchronous accesses, this will always be adjusted so that the phase exits on a rising edge of the external clock. 00000_B1 wait state. 00001_B1 wait states. 00010_B2 wait state. …$_B$ … 11110_B30 wait states. 11111_B31 wait states.
DATAC	15:12	rw	**Data Hold Cycles for Read Accesses** This bit field determines the basic number of Data Hold phase clock cycles during read accesses. This is used for a limited number of read cycle types. See **"Data Hold Phase (DH)" on Page 15-65**. Also controls the length of the Control Hold phase. See **"Control Hold (CH)" on Page 15-66**. 0000_B No Recovery Phase clock cycles available. 0001_B 1 clock cycle selected. …$_B$ … 1110_B 14 clock cycles selected. 1111_B 15 clock cycles selected.
EXTCLOCK	17:16	rw	**Frequency of external clock at pin BFCLKO or SDCLKO** See **"External Bus Clock Generation" on Page 15-26**
EXTDATA	19:18	rw	**Extended data** See **Burst Phase (BP)** 00_B external memory outputs data every BFCLK cycle 01_B external memory outputs data every two BFCLK cycles 10_B external memory outputs data every four BFCLK cycles 11_B external memory outputs data every eight BFCLK cycles

Field	Bits	Type	Description
CMDDELAY	23:20	rw	**Command Delay Cycles** This bit field determines the basic number of Command Delay phase clock cycles. 000_B 0 clock cycle selected. 001_B 1 clock cycle selected. …B … 110_B 6 clock cycles selected. 111_B 7 clock cycles selected.
AHOLDC	27:24	rw	**Address Hold Cycles** This bit field determines the number of clock cycles of the address hold phase.. 0000_B1 clock cycle selected 0001_B1 clock cycle selected …B … 1110_B14 clock cycles selected 1111_B15 clock cycles selected
ADDRC	31:28	rw	**Address Cycles** This bit field determines the number of clock cycles of the address phase. 000_B 1 clock cycle selected 001_B 1 clock cycle selected …B … 110_B 6 clock cycles selected 111_B 7 clock cycles selected

*Note: When in external boot mode (see **Page 15-41**), the reset value of BUSAP0 is overwritten automatically (subsequent to the release of reset) as a result of the external Boot Configuration Value fetch.*

15.21.8 Bus Write Access Parameter Register, BUSWAPx

EBU_BUSWAPx (x = 0-3)
EBU Bus Write Access Parameter Register
(034_H+x*10_H) **Reset Value: FFFF FFFF$_H$**



Field	Bits	Type	Description
WRDTACS	3:0	rw	**Recovery Cycles between Different Regions** This bit field determines the number of clock cycles of the Recovery Phase between consecutive accesses directed to different regions or different types of access. See **"Recovery Phase (RP)" on Page 15-67** and **"SDRAM Recovery Phases" on Page 15-135** 0000_B No Recovery Phase clock cycles available. 0001_B 1 clock cycle selected. …$_B$ … 1110_B 14 clock cycles selected. 1111_B 15 clock cycles selected.
WRRECOVC	6:4	rw	**Recovery Cycles after Write Accesses** This bit field determines the basic number of clock cycles of the Recovery Phase at the end of write accesses. See **"Recovery Phase (RP)" on Page 15-67** and **"SDRAM Recovery Phases" on Page 15-135** 000_B No Recovery Phase clock cycles available. 001_B 1 clock cycle selected. …$_B$ … 110_B 6 clock cycles selected. 111_B 7 clock cycles selected.

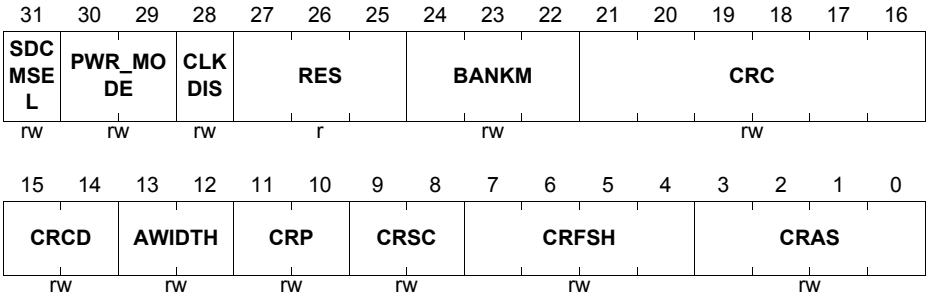
Field	Bits	Type	Description
WAITWRC	11:7	rw	**Programmed Wait States for write accesses** Number of programmed wait states for write accesses. For synchronous accesses, this will always be adjusted so that the phase exits on a rising edge of the external clock. 00000_B 1 wait state. 00001_B 1 wait states. 00010_B 2 wait state. …B … 11110_B 30 wait states. 11111_B 31 wait states.
DATAC	15:12	rw	**Data Hold Cycles for Write Accesses** This bit field determines the basic number of Data Hold phase clock cycles during write accesses. 0000_B No Recovery Phase clock cycles available. 0001_B 1 clock cycle selected. …B … 1110_B 14 clock cycles selected. 1111_B 15 clock cycles selected.
EXTCLOCK	17:16	rw	**Frequency of external clock at pin BFCLKO or SDCLKO** See **"External Bus Clock Generation" on Page 15-26**.
EXTDATA	19:18	rw	**Extended data** See **Burst Phase (BP)** 00_B external memory outputs data every BFCLK cycle 01_B external memory outputs data every two BFCLK cycles 10_B external memory outputs data every four BFCLK cycles 11_B external memory outputs data every eight BFCLK cycles

Field	Bits	Type	Description
CMDDELAY	23:20	rw	**Command Delay Cycles** This bit field determines the basic number of Command Delay phase clock cycles. 000_B 0 clock cycles selected. 001_B 1 clock cycles selected. …B … 110_B 6 clock cycles selected. 111_B 7 clock cycles selected.
AHOLDC	27:24	rw	**Address Hold Cycles** This bit field determines the number of clock cycles of the address hold phase.. 0000_B1 clock cycle selected 0001_B1 clock cycle selected …B … 1110_B14 clock cycles selected 1111_B15 clock cycles selected
ADDRC	31:28	rw	**Address Cycles** This bit field determines the number of clock cycles of the address phase. 0000_B1 clock cycle selected 0001_B1 clock cycle selected …B … 1110_B14 clock cycles selected 1111_B15 clock cycles selected

15.21.9 SDRAM Control Register, SDRMCON

MEMCTRL SDRAM Control Register

EBU_SDRMCON
EBU SDRAM Control Register (068$_H$) Reset Value: 1000 0000$_H$



Field	Bits	Type	Description
SDCMSEL	31	rw	**SDRAM clock mode select** 1_B clock disabled between accesses 0_B clock continuously runs *Note: (see **"Power Down Mode" on Page 15-134**)*
PWR_MODE	30:29	rw	**Power Save Mode used for gated clock mode** 0_H precharge before clock stop (default after reset) 1_H auto-precharge before clock stop 2_H active power down (stop clock without precharge) 3_H clock stop power down *Note: (see **"Power Down Mode" on Page 15-134**)*
CLKDIS	28	rw	**Disable SDRAM clock output** 0_B clock enabled 1_B clock disabled *Note: (see **"Power Down Mode" on Page 15-134**)*
RES	27:25	r	**Reserved**

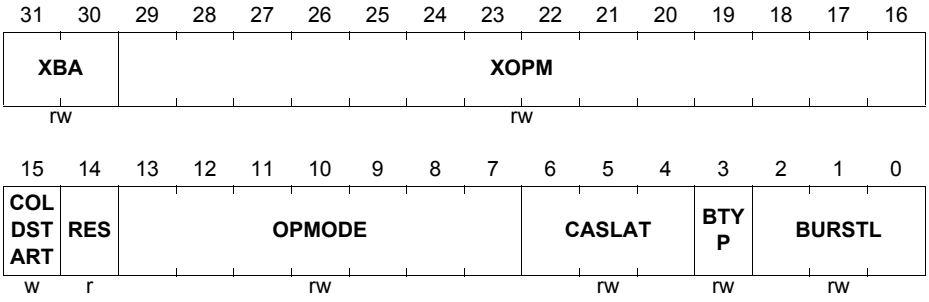
Field	Bits	Type	Description
BANKM	24:22	rw	**Mask for bank tag** SRI address bits to be used for determining bank number. 0_H Reserved; (default after reset) 1_H Address bit 21 to 20 2_H Address bit 22 to 21 3_H Address bit 23 to 22 4_H Address bit 24 to 23 5_H Address bit 25 to 24 6_H Address bit 26 to 25 7_H Address bit 26 *Note: See* ***"Bank Address Multiplexing" on Page 15-126****.*
CRC	21:16	rw	**Refresh cycle time counter** Number of NOP cycles following a refresh command before another command (other than a NOP) can be issued to the SDRAM. Combined with the Crce bit as follows:- 0-$3F_H$: Insert Crc + 1 NOP cycles.
CRCD	15:14	rw	**Row to column delay counter** Number of NOP cycles between a row address and a column address. 0-3_H: Insert Crcd + 1 NOP cycles (default after reset Crcd is 0).
AWIDTH	13:12	rw	**Width of column address** Number of address bits from bit 0 to be used for column address. See also **"SDRAM Addressing Scheme" on Page 15-125**. e.g. for 16 bit DRAMs 0_H **reserved**, do not use 1_H Address(8:0) 2_H Address(9:0) 3_H Address(10:0)
CRP	11:10	rw	**Row precharge time counter** Number of NOP cycles inserted after a precharge command. The actual number performed can be greater due to CAS latency and burst length. 0-3_H: Insert Crsc + 1 NOP cycles (default after reset Crp is 0)

Field	Bits	Type	Description
CRSC	9:8	rw	**Mode register set-up time** Number of NOP cycles after a mode register set command. $0\text{-}3_H$: Insert Crsc + 1 NOP cycles (default after reset Crsc is 0)
CRFSH	7:4	rw	**Initialization refresh commands counter** Number of refresh commands issued during power-up initialization sequence. $0\text{-}15_H$: Perform Crfsh + 1 refresh cycles (default after reset Crfsh is 0)
CRAS	3:0	rw	**Row to precharge delay counter** Number of clock cycles between row activate command and a precharge command. $0\text{-}15_H$: Minimum Cras + 1 clock cycles (default after reset Cras is 0)

15.21.10 SDRAM Mode Register, SDRMOD

SDRAM Mode Register

EBU_SDRMOD
EBU SDRAM Mode Register ($6C_H$) Reset Value: 0000 0020$_H$



Field	Bits	Type	Description
XBA	31:30	rw	**Extended Operation Bank Select** Value to be written to the bank select pins of a “Mobile” SDRAM device during an extended mode register write operation. Control of these bits is provided to allow support of future enhanced “Mobile” SDRAM devices. See **“Mobile SDRAM Support” on Page 15-124** *Note: Care must be taken when programming these bits to ensure that a valid extended mode register access occurs (e.g. it is possible to generate an extra unwanted standard mode register write by incorrect programming of these bits).* *3. Consult the appropriate SDRAM documentation for the function of these bits.*
XOPM	29:16	rw	**Extended Operation Mode** Value to be written to the extended mode register of a “Mobile” SDRAM device. This value is issued to the SDRAM via it’s address inputs during an extended mode register write. This field is wider than current extended mode registers to allow support of future enhanced “Mobile” SDRAM devices. *Note: Consult the appropriate SDRAM documentation for the function of these bits.*
COLDSTART	15	w	**SDRAM coldstart** This bit will always read 0. If a write to the **EBU_SDRMOD** register takes place with this bit set, the SDRAM device mode register will be updated to match the data written to the register. See **“Initialization sequence” on Page 15-121**
RES	14	r	**Reserved** 0_H Fixed Value

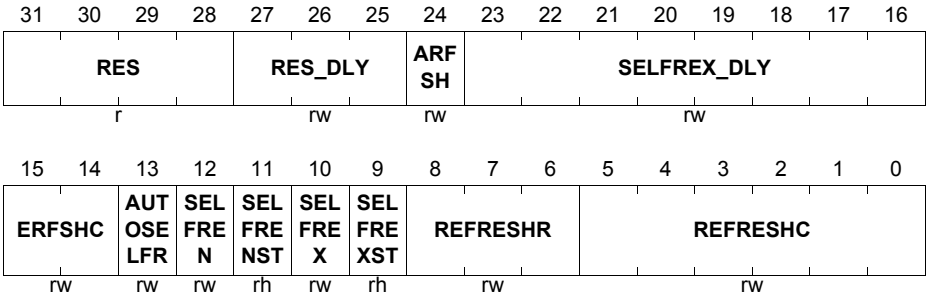
Field	Bits	Type	Description
OPMODE	13:7	rw	**Operation Mode** Memory Controller only supports burst write standard operation. 0_H Only this value should be written (default after reset) *Note: Other values reserved*
CASLAT	6:4	rw	**CAS latency** Number of clocks between a READ command and the availability of data. 2_H Two clocks (default after reset) 3_H Three clocks *Note: Other values reserved*
BTYP	3	rw	**Burst type** Memory Controller only supports sequential burst. 0_B Only this value should be written (default after reset) 1_B Reserved
BURSTL	2:0	rw	**Burst length** Number of locations can be accessed with a single command. 0_H 1 (default after reset) 1_H 2 2_H 4 3_H 8 4_H 16 *Note: Other values reserved*

15.21.11 SDRAM Refresh Control Register, SDRMREF

SDRAM Refresh Control Register

EBU_SDRMREF

EBU SDRAM Refresh Control Register(070_H) **Reset Value: $0000\ 0000_H$**



Field	Bits	Type	Description
RES	31:28	r	**Reserved** 0_H Reserved Value
RES_DLY	27:25	rw	**Delay on Power Down Exit** Number of NOPs after the SDRAM controller exits power down before an active command is permitted. *Note: See **"Power Down Mode" on Page 15-134***
ARFSH	24	rw	**Auto Refresh on Self refresh Exit** If set to one, an auto refresh cycle will be performed on exiting self refresh before the self refresh exit delay. If set to zero, no refresh will be performed. *Note: See **"Self-Refresh Mode" on Page 15-133***
SELFREX_DLY	23:16	rw	**Self Refresh Exit Delay** Number of NOP cycles inserted after a self refresh exit before a command is permitted to the SDRAM/DDRAM. *Note: See **"Self-Refresh Mode" on Page 15-133***
ERFSHC	15:14	rw	**Extended Refresh Counter Period** This field is used to increase the range of the refreshc field from 6 bits to 8 bits with erfshc being used as bits 7 and 6 of the extended field and refreshc as bit 5 to 0.

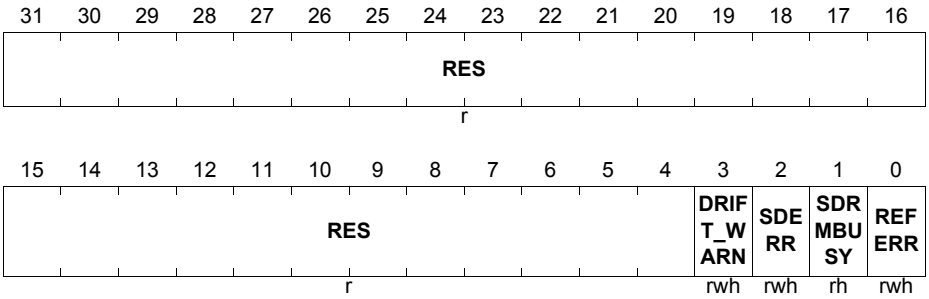
Field	Bits	Type	Description
AUTOSELFR	13	rw	**Automatic Self Refresh** When this bit is set to '1', Memory Controller will automatically issue the Self Refresh Entry command to all SDRAM devices when it gives up control of the external bus, and will automatically issue Self Refresh Exit when it regains control of the bus.
SELFREN	12	rw	**Self Refresh Entry** When this bit is written with '1' the Self Refresh Entry command is issued to all SDRAM devices, regardless whether they are attached to type 0 or type 1.
SELFRENST	11	rh	**Self Refresh Entry Status.** If this bit is set to '1', it means the Self Refresh Entry command has been successfully issued. This bit is reset when bit selfrex is set to '1' or a reset takes place.
SELFREX	10	rw	**Self Refresh Exit (Power Up).** When this bit is written with '1' the Self Refresh Exit command is issued to all SDRAM devices, regardless whether they are attached to type 0 or type 1. This is also used after power is applied to drive CKE high
SELFREXST	9	rh	**Self Refresh Exit Status.** If this bit is set to '1', it means the Self Refresh Exit command has been successfully issued. This bit is reset when bit selfren is set to '1' or a reset takes place.
REFRESHR	8:6	rw	**Number of refresh commands** The number of additional refresh commands issued to SDRAM each time a refresh is due. 00_H 1 refresh command is issued (default after reset). 01_H 1 additional refresh command is issued. $\ldots_H$ … 06_H 6 additional refresh commands are issued. 07_H 7 additional refresh commands are issued.

Field	Bits	Type	Description
REFRESHC	5:0	rw	**Refresh counter period** Number of clock cycles between refresh operations. Uses ((erfshc x 64) +refreshc) as a single counter value where 0_D means that no refresh is needed an the refresh generator is disable. This is the default setting after reset. For all other vales, the refresh period is ((erfshc x 64) + refreshc) x 64 clock cycles

15.21.12 SDRAM Status Register, SDRSTAT

SDRAM Status Register

EBU_SDRSTAT
EBU SDRAM Status Register (074_H) Reset Value: 0000 0000$_H$



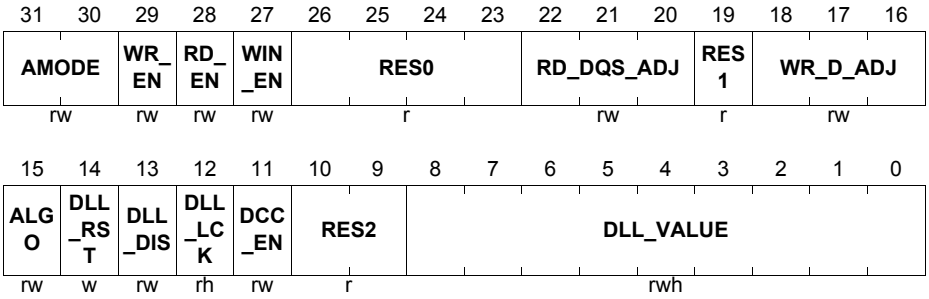
Field	Bits	Type	Description
RES	31:4	r	**Reserved** 0_H Reserved Value
DRIFT_WARN	3	rwh	**DLL Drift Warning** The Drift detector has detected that the DLL operating point drift has exceeded the tracking limit of the DLL. This bit latches at 1_B until cleared by writing a 0_B. See **"DLL Drift Detected (DRIFT_WARN)" on Page 15-137** 0_B DLL tracking successfully 1_B DLL tracking limit has been exceeded

Field	Bits	Type	Description
SDERR	2	rwh	**SDRAM read error** SDRAM controller has detected an error when returning read data. See **"SDRAM Read Error (SDERR)" on Page 15-137** 0_B Reads running successfully 1_B Read error condition has been detected *Note: This bit latches at 1_B and is reset by writing 0_B.*
SDRMBUSY	1	rh	**SDRAM Busy** The status of power-up initialization sequence. See **"SDRAM Controller Busy (SDRMBUSY)" on Page 15-137** 0_B Power-up initialization sequence is not running 1_B Power-up initialization sequence is running
REFERR	0	rwh	**SDRAM Refresh Error** Unsuccessful previous refresh request collides with a new request. See **"Refresh Error (REFERR)" on Page 15-136** This bit latches at 1_B and is reset by writing 0_B. 0_B No refresh error. 1_B Refresh error occurred.

15.21.13 DLL Control Register, EBU_DLLCON

DLL Control Register

EBU_DLLCON
EBU DLL Control Register **(078_H)** **Reset Value: 0000 2000$_H$**



Field	Bits	Type	Description
AMODE	31:30	rw	**Mode for generating address bits on DDR accesses.** 00_B DDR control timing 01_B early address generation) 10_B reserved 11_B reserved. *Note: See* ***"DDR Mode Address Outputs" on Page 15-142***
WR_EN	29	rw	**Write Delay Enable** 0_B The slave delay line used to phase shift the outgoing DQS signals is disabled. 1_B The slave delay line used to phase shift the outgoing DQS signals is enabled.
RD_EN	28	rw	**Read Delay Enable** 0_B The slave delay lines used to phase shift the incoming DQS signals are disabled. 1_B The slave delay lines used to phase shift the incoming DQS signals are enabled.

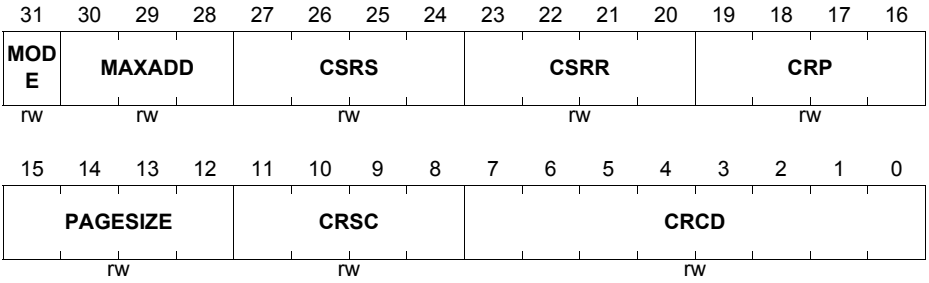
Field	Bits	Type	Description
WIN_EN	27	rw	**Drift Window Enable** See **"DLL Drift detector" on Page 15-23** for information on this field 0_B Warning Window is disabled 1_B Warning Window is Enabled
RES0	26:23	r	**Reserved**
RD_DQS_ADJ	22:20	rw	**Read DQS Adjust** signed binary number (in 64ths of a clock cycle) added to the shift value for the DQS inputs. The value will be sign extended. See **"DLL Operation" on Page 15-20**
RES1	19	r	**Reserved** 0_B Reserved Value
WR_D_ADJ	18:16	rw	**Write Data Adjust** signed binary number (in 64ths of a clock cycle) added to the shift value for the write data outputs. The value will be sign extended. See **"DLL Operation" on Page 15-20**
ALGO	15	rw	**Lock Algorithm Control** 0_B Fast Locking Algorithm 1_B Slow Locking Algorithm
DLL_RST	14	w	**Reset the DLL** Write '1' to reset the DLL control logic. If the DLL is enabled, this will trigger a full relock. Always reads '0'
DLL_DIS	13	rw	**Disable DLL Lock Function** 0_B DLL normal operation 1_B Lock DLL to value in DLL_value field *Note: This should be set to one when the DDR clock frequency is too low for the DLL to lock. It will force the DLL to use the preloaded value.*
DLL_LCK	12	rh	**DLL Lock Status** 0_B DLL is not locked 1_B DLL is locked
DCC_EN	11	r	**Duty Cycle Correction Enable** 0_B Disabled 1_B Enabled

Field	Bits	Type	Description
RES2	10:9	r	**Reserved** 0_B Reserved Value
DLL_VALUE	8:0	rwh	**DLL Lock Value** When read will return the current lock value of the DLL register. (i.e. the number of delay elements required to delay the clock by one clock period) When written will preload the DLL register if the DLL is not enabled. See **“DLL Operation” on Page 15-20**

15.21.14 LPDDR NVM Configuration Register, DDRNCON

EBU_DDRNCON
EBU LPDDR NVM Configuration Register

($07C_H$) **Reset Value: $0000\ 0000_H$**

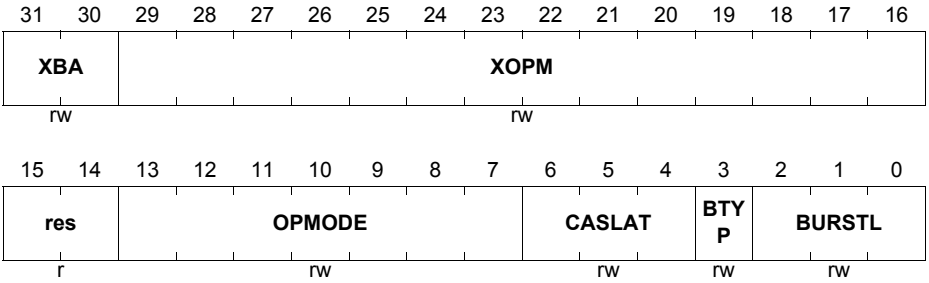


Field	Bits	Type	Description
MODE	31	rw	**Device Operating Mode** 0_B **XIP**, Attached memory is Execute in place technology. 1_B **NAND**, Attached memory is not capable of being used as XIP
MAXADD	30:28	rw	**NVM Device Size** SRI address bits to be used for accessing the attached device. 0_H SRI Address bits 21 to 0 1_H SRI Address bits 22 to 0 2_H SRI Address bits 23 to 0 3_H SRI Address bits 24 to 0 4_H SRI Address bits 25 to 0 5_H SRI Address bits 26 to 0 6_H SRI Address bits 27 to 0 7_H SRI Address bits 28 to 0 *Note: See "Bank Address Multiplexing" on Page 15-126.*
CSRS	27:24	rw	**SRR to next command delay** Number of memory clock cycles delay to insert after the SRR command of a status register read to satisfy the memory device t_{SRS} parameter. Delay inserted will be CSRS+1 NOP cycles.

Field	Bits	Type	Description
CSRR	23:20	rw	**MRS to SRR command delay** Number of memory clock cycles delay to insert between the MRS command and the SRR command during a status register read to satisfy the memory device t_{SRR} parameter.
CRP	19:16	rw	**PREACTIVE to ACTIVE command delay** Number of memory clock cycles delay to insert between PREACTIVE and ACTIVE commands to satisfy the memory device t_{RP} parameter.
PAGESIZE	15:12	rw	**Device Page Size** Page size of the memory device. This defines the number of internal address bits from bit 1 to be used for column address. See also **"Normal operating mode" on Page 15-146**. 3_H **32 bytes** , Address(3:1) 4_H **64 byte**, Address(4:1) 5_H **128 byte**, Address(5:1) 6_H **256 bytes**, Address(6:1) 7_H **512 bytes**, Address(7:1) 8H **1024 bytes**, Address(8:1) 9_H **2048 bytes**, Address(9:1) A_H **4096 bytes**, Address(10:1) B_H **8192 bytes**, Address(11:1) C_H **16384 bytes**, Address(12:1) *Note: All other values reserved and must not be used*
CRSC	11:8	rw	**Mode register set-up time** Number of NOP cycles after a mode register set command. 0-3_H: Insert Crsc + 1 NOP cycles (default after reset Crsc is 0)
CRCD	7:0	rw	**Row to column delay counter** Number of NOP cycles between a row address and a column address. 0-31_D: Insert Crcd + 1 NOP cycles of the device clock (default after reset Crcd is 0).

15.21.15 LPDDR NVM Mode Register, DDRNMOD

EBU_DDRNMOD
EBU DDR NVM Mode Register **(080_H)** **Reset Value: 0000 0024$_H$**



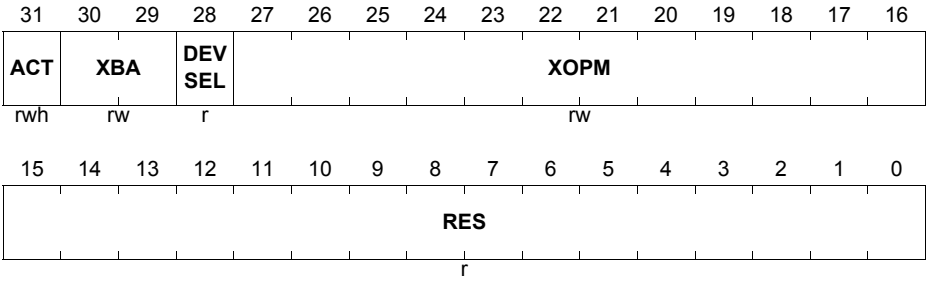
Field	Bits	Type	Description
XBA	31:30	rw	**Extended Operation Bank Select** Value to be written to the bank select pins of a LPDDR NVM device during an extended mode register write operation. Control of these bits is provided to allow support of future devices. *Note: Care must be taken when programming these bits to ensure that a valid extended mode register access occurs (e.g. it is possible to generate an extra unwanted standard mode register write by incorrect programming of these bits).*
XOPM	29:16	rw	**Extended Operation Mode** Value to be written to the extended mode register of a LPDDR NVM device. This value is issued to the device via it's address inputs during an extended mode register write. This field is wider than current extended mode registers to allow support of future devices. *Note: Consult the appropriate device documentation for the function of these bits.*
Res	15:14	r	**Reserved** reads 0_B. Must be written with 0_B.

Field	Bits	Type	Description
OPMODE	13:7	rw	**Operation Mode** Memory Controller only supports burst write standard operation. This field should always be programmed with 00_H. All other values are reserved for possible future device extensions. See the memory device data sheet for any further information.
CASLAT	6:4	rw	**CAS latency** Number of clocks between a READ command and the availability of data. 010_B **CAS2**, Two clocks (default after reset) 011_B **CAS3**, Three clocks *Note: All other values reserved for future expansion and are not supported by the memory controller*
BTYP	3	rw	**Burst type** Memory Controller only supports sequential burst. 0_B **Linear**, Only this value should be written (default after reset) 1_B **Interleave**, reserved. This value is not supported by the memory controller and is reserved in the JEDEC specification
BURSTL	2:0	rw	**Burst length** Number of locations can be accessed with a single command. 010_B **4**, word burst 011_B **8**, word burst 100_B **16**, word burst *Note: All other values reserved and not supported by the memory controller. Not all burst lengths are necessarily supported by all memory devices.*

15.21.16 LPDDR NVM Extended Mode Register, DDRNMOD2

EBU_DDRNMOD2
EBU DDR NVM Extended Mode Register

(084_H) **Reset Value: 0000 0000_H**

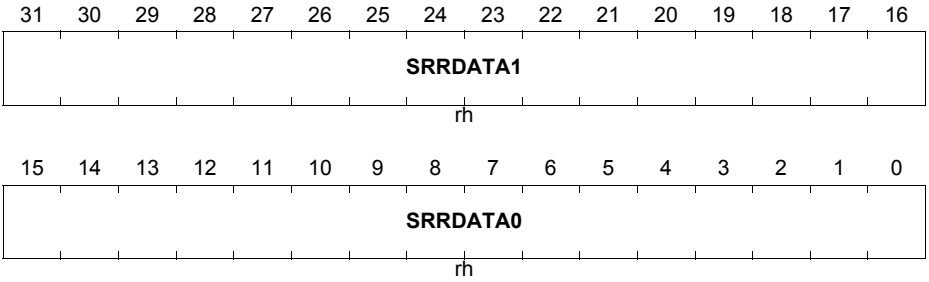


Field	Bits	Type	Description
ACT	31	rwh	**Status Register Operation Active** Write 1_B to this bitfield to trigger a mode/status register operation. When the operation is completed, the bit will be reset to 0_B by hardware. Writing 0_B will have no effect. Writing 1_B while an operation is in progress will not trigger a second status register operation but may overwrite the data to be written by the first.
XBA	30:29	rw	**Extended Operation Bank Select** Value to be written to the bank select pins of an LPDDR-NVM device during an mode register write operation. *Note: Care must be taken when programming these bits to ensure that a valid extended mode register access occurs (e.g. it is possible to generate an extra unwanted standard mode register write by incorrect programming of these bits).*
DEV_SEL	28	r	**Device Select** Must be written with 0_B.

Field	Bits	Type	Description
XOPM	27:16	rw	**Extended Operation Mode** Value to be written to the second extended mode register of a LPDDR-NVM device. This value is issued to the NVM via it's address inputs during an extended mode register write. This field is wider than current extended mode registers to allow support of future devices. *Note: Consult the appropriate device documentation for the function of these bits.* *4. Memory Controller provides a 12-bit wide bit-field for the extended mode register to cater for devices that could theoretically use additional control bits (in comparison to currently available devices).*
RES	15:0	r	**Reserved** Reads as all 0_B.

15.21.17 LPDDR NVM Status Register, DDRNSRR

EBU_DDRNSRR
EBU DDR NVM Status Register (088_H) Reset Value: 0000 0000$_H$

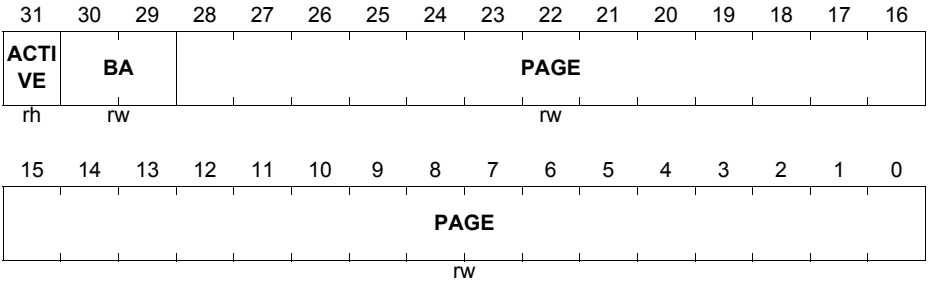


Field	Bits	Type	Description
SRRDATA1	31:16	rh	**Status Register Read Data** Returns the value of the last status register read operation. This field is only used when the LPDDR-NVM region is configured as twin 16 bit. ie. two 16 bit memories are connected.
SRRDATA0	15:0	rh	**Status Register Read Data** Returns the value of the last status register read operation. This field is used when a single 16 bit or 32 bit device is connected

15.21.18 DDR Preload Register, DDRNPRLD

EBU_DDRNPRLD
EBU DDR NVM Page Preload Register

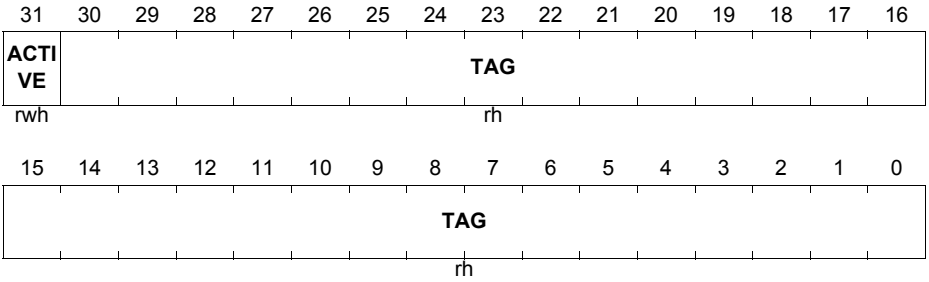
($08C_H$) **Reset Value: $0000\ 0000_H$**



Field	Bits	Type	Description
PAGE	28:0	rw	**Preload Page** Byte Address of page to be preloaded. *Note: See* ***"Page Preload" on Page 15-149***
BA	30:29	rw	**Bank Address** Two bit field identifying the RDB to be used. This value will be used as the bank address bits for the access
ACTIVE	31	rh	**Preload Active** This bit will be set to 1_B while the preload command is in progress

15.21.19 DDR Tag Register, DDRNTAGx

EBU_DDRNTAGx (x=0-3)
EBU DDR Tag Registers **(090_H+x*4_H)** **Reset Value: 0000 0000_H**

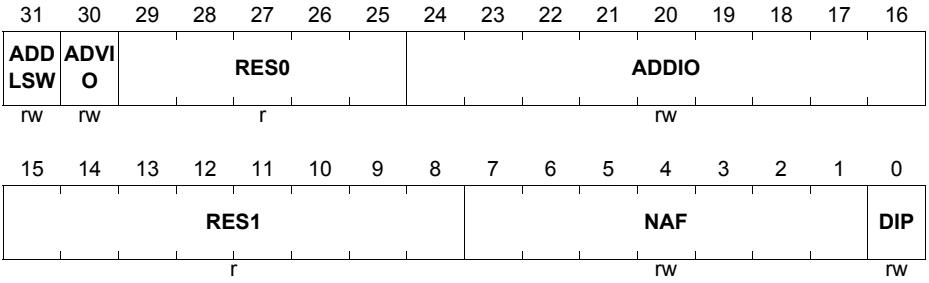


Field	Bits	Type	Description
TAG	30:0	rh	**Current Value for Page Tag** Byte Address (internal, processor address) of page tag. Significant bits will depend on hardware settings
ACTIVE	31	rwh	**Page Tag Active Status** 0_B **Inactive**, Tag Status is Idle. Address is invalid 1_B **active**, Tag Status is Idle. Address is valid

15.21.20 Test/Control Configuration Register, USERCON

EBU_USERCON
EBU Test/Control Configuration Register

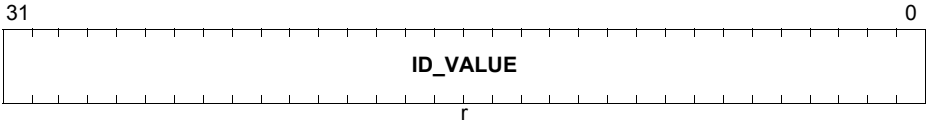
($00C_H$) **Reset Value: $0000\ 0000_H$**



Field	Bits	Type	Description
DIP	0	rw	**Disable Internal Pipelining** Reserved, set to 0_B
NAF	7:1	rw	**No Assigned Function** Reserved for future requirements
RES1	15:8	r	**Reserved** Read as 0; should be written with 0.
ADDIO	24:16	rw	**Address Pins to GPIO Mode** Individual Control Bits for Address Bus Bits 27 downto 19 respectively. 0_B Address Bit is required for addressing memory 1_B Address Bit switched to GPIO function
RES	29:25	r	**Reserved**
ADVIO	30	rw	**ADV Pin to GPIO Mode** Control Bit for the $\overline{ADV}$/ALE output 0_B $\overline{ADV}$ pin is required for controlling memory 1_B $\overline{ADV}$ pin is switched to GPIO function
ADDLSW	31	rw	**Enable Address LSW, A(15:0) for GPIO** Switch the least significant 16 bits of the address bus to GPIO mode. 0_B A(15:0) in use by EBU 1_B A(15:0) used as GPIO.

15.22 Registers for SFR Extraction

EBU_ID
EBU Module Identification Register (08_H) **Reset Value: 0014 C00A$_H$**



Field	Bits	Type	Description
ID_VALUE	[31:0]	r	**Module Identification Value**

16 Interrupt System

The TC1798 interrupt system provides a flexible and time-efficient means of processing interrupts. This chapter describes the interrupt system for the TC1798. Topics covered include the architecture of the interrupt system, interrupt system configuration, and the interrupt operations of the TC1798 peripherals and Central Processing Unit (CPU). General information is also given about the Peripheral Control Processor (PCP).

16.1 Overview

An interrupt request can be serviced either by the CPU or by the PCP. Interrupt requests are called “service requests” rather than “interrupt requests” in this document because they can be serviced by either one of the service providers.

Each peripheral in the TC1798 can generate service requests. Additionally, the Bus Control Units, the Debug Unit, the PCP, and even the CPU itself can generate service requests to either of the two service providers.

As shown in **Figure 16-1**, each TC1798 unit that can generate service requests is connected to one or more Service Request Nodes (SRNs). Each SRN contains a Service Request Control Register mod_SRCx, where “mod” is the identifier of the service requesting unit and “x” an optional index. Two arbitration buses connect the SRNs with two Interrupt Control Units (ICUs), which handle interrupt arbitration among competing interrupt service requests, as follows:

- The Interrupt Control Unit (ICU) arbitrates service requests for the CPU and administers the CPU interrupt arbitration bus.
- The Peripheral Interrupt Control Unit (PICU) arbitrates service requests for the PCP and administers the PCP interrupt arbitration bus.

The PCP can make service requests directly to itself (via the PICU), or it can make service requests to the CPU. The Debug Unit can generate service requests to the PCP or the CPU. The CPU can make service requests directly to itself (via the ICU), or it can make service requests to the PCP. The CPU Service Request Nodes are activated through software.

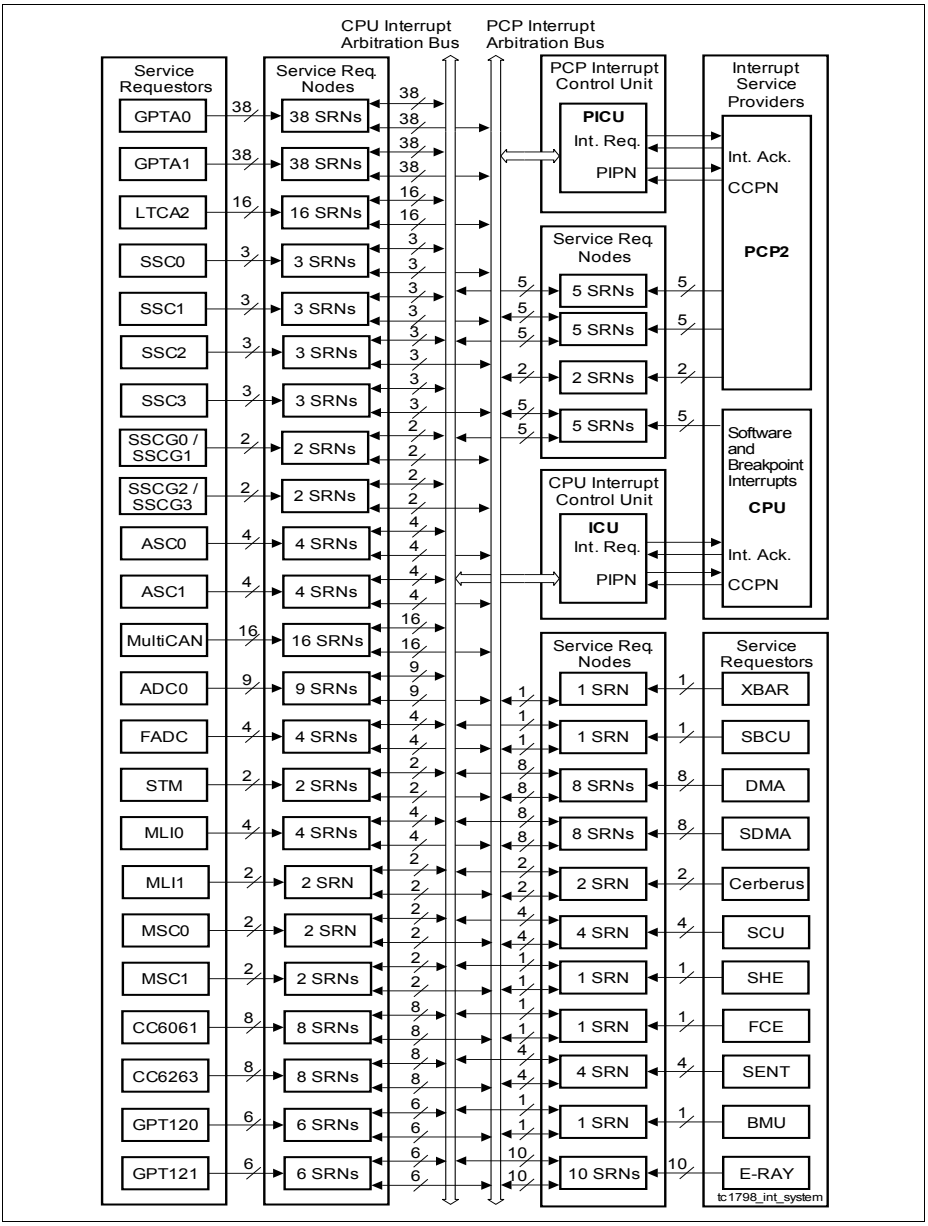


Figure 16-1 Block Diagram of the TC1798 Interrupt System

16.2 Service Request Nodes

Each SRN contains a Service Request Control Register and interface logic that connects it to the triggering unit and to the two interrupt arbitration buses. Some peripheral units of the TC1798 have multiple SRNs.

16.2.1 Service Request Control Registers

All Service Request Control Registers in the TC1798 have the same format. In general, these registers contain:

- Enable/disable information
- Priority information
- Service provider destination
- Service request status bit
- Software-initiated service request set and reset bits

Besides being activated by the associated triggering unit through hardware, each SRN can also be set or reset by software via two software-initiated service request control bits.

The description given in this chapter characterizes all Service Request Control Registers of the TC1798. Information on peripheral module interrupt functions such as enable or request flags is provided in the corresponding sections of the module chapters.

16.2.1.1 General Service Request Control Register Format

The description given in this chapter characterizes all Service Request Control Registers of the TC1798. Information on peripheral module interrupt functions such as enable or request flags is provided in the corresponding sections of the module chapters.

mod_SRC
Service Request Control Register (00_H) Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SETR	CLRR	SRR	SRE	0	TOS	0		SRPN							
w	w	rh	rw	r	rw	r		rw							

Field	Bits	Type	Description
SRPN	[7:0]	rw	**Service Request Priority Number** 00_H Service request is never serviced 01_H Service request is on lowest priority … … FF_H Service request is on highest priority
TOS	10	rw	**Type of Service Control** 0 CPU service is initiated 1 PCP request is initiated
SRE	12	rw	**Service Request Enable** 0 Service request is disabled 1 Service request is enabled
SRR	13	rh	**Service Request Flag** 0 No service request is pending 1 A service request is pending
CLRR	14	w	**Request Clear Bit** CLRR is required to reset SRR. 0 No action 1 Clear SRR; bit value is not stored; read always returns 0; no action if SETR is set also.
SETR	15	w	**Request Set Bit** SETR is required to set SRR. 0 No action 1 Set SRR; bit value is not stored; read always returns 0; no action if CLRR is set also.
0	[9:8], 11, [31:16]	r	**Reserved** Read as 0; should be written with 0.

16.2.1.2 Request Set and Clear Bits (SETR, CLRR)

The SETR and CLRR bits allow software to set or clear the service request bit SRR. Writing a 1 to SETR causes bit SRR to be set to 1. Writing a 1 to CLRR causes bit SRR to be cleared to 0. If hardware attempts to modify SRR during a read-modify-write software operation (such as the bit-set or bit-clear instructions), the software operation will succeed and the hardware operation will have no effect.

The value written to SETR or CLRR is not stored. Writing a 0 to these bits has no effect. These bits always return 0 when read. If both, SETR and CLRR, are set to 1 at the same time, SRR is not changed.

16.2.1.3 Enable Bit (SRE)

The SRE bit enables an interrupt to take part in the arbitration for the selected service provider. It does not enable or disable the setting of the request flag SRR; the request flag can be set by hardware or by software (via SETR) independent of the state of the SRE bit. This allows service requests to be handled automatically by hardware or through software polling.

If SRE = 1, pending service requests are passed on to the designated service provider for interrupt arbitration. The SRR bit is automatically set to 0 by hardware when the service request is acknowledged and serviced. It is recommended that in this case, software should not modify the SRR bit to avoid unexpected behavior due to the hardware controlling this bit.

If SRE = 0, pending service requests are not passed on to service providers. Software can poll the SRR bit to check whether a service request is pending. To acknowledge the service request, the SRR bit must then be reset by software by writing a 1 to CLRR.

Note: In this document, ‘active source’ means an SRN whose Service Request Control Register has its request enable bit SRE set to 1 to allow its service requests to participate in interrupt arbitration.

16.2.1.4 Service Request Flag (SRR)

When set, the SRR flag indicates that a service request is pending. It can be set or reset directly by hardware or indirectly through software using the SETR and CLRR bits. Writing directly to this bit via software has no effect.

The SRR status bit can be directly set or reset by the associated hardware. For instance, in the General Purpose Array Unit, an associated timer event can cause this bit to be set to 1. The details of how hardware events can cause the SRR bit to be set are defined in the individual peripheral/module chapters.

The acknowledgment of the service request by either the Interrupt Control Unit (ICU) or the PCP Interrupt Control Unit (PICU) causes the SRR bit to be cleared.

SRR can be set or cleared either by hardware or by software regardless of the state of the enable bit SRE. However, the request is only forwarded for service if the enable bit is set. If SRE = 1, a pending service request takes part in the interrupt arbitration of the service provider selected by the device's TOS bit. If SRE = 0, a pending service request is excluded from interrupt arbitrations.

SRR is automatically reset by hardware when the service request is acknowledged and serviced. Software can poll SRR to check for a pending service request. SRR must be reset by software in this case by writing a 1 to CLRR.

It is not advisable to clear a pending service request flag SRR (writing CLRR = 1) and enable the corresponding service request node SRN (writing SRE = 1) simultaneously at the same write access to the Service Request Control Register. If this should happen, an unintended interrupt request may be generated. Instead of executing one write access, it is recommended to split the two actions into two consecutive write accesses to the corresponding Service Request Control Register, starting with the clearing of the pending interrupt flag and followed by the enabling of the service request node.

16.2.1.5 Type-Of-Service Control (TOS)

There are two service providers for service requests in the TC1798, the CPU and the PCP. The TOS bit is used to select whether a service request generates an interrupt to the CPU (TOS = 0) or to the PCP (TOS = 1). Bit 11 of the Service Request Control Register is read-only, returning 0 when read. Writing to this bit position has no effect. However, to ensure compatibility with future extensions, bit 11 should always be written with a 0.

Note that several Service Request Control Registers (e.g. in the PCP) have a hardwired TOS bit (0 or 1) that cannot be written. These registers can only generate an interrupt to one dedicated service provider (PCP or CPU).

Note: Before modifying the content of a TOS bit, the corresponding SRN must be disabled (SRE = 0).

16.2.1.6 Service Request Priority Number (SRPN)

The 8-bit Service Request Priority Number (SRPN) indicates the priority of a service request with respect to other sources requesting service from the same service provider, and with respect to the priority of the service provider itself.

Each active source selecting the same service provider must have a unique SRPN value to differentiate its priority. The special SRPN value of 00_H excludes an SRN from taking part in arbitration, regardless of the state of its SRE bit. The SRPN values for active sources selecting different service providers (CPU vs. PCP) may overlap. If a source is not active – meaning its SRE bit is 0 – no restrictions are applied to the service request priority number.

The SRPN is used by service providers to select an Interrupt Service Routine (ISR)) or Channel Program (in case of the PCP) to service the request. ISRs are associated with Service Request Priority Numbers by an Interrupt Vector Table located in each service provider. This means that the TC1798 Interrupt Vector Table is ordered by priority number. This is unlike traditional interrupt architectures in which their interrupt vector tables are ordered by the source of the interrupt. The TC1798 Interrupt Vector Table allows a single peripheral to have multiple priorities for different purposes.

The range of values for SRPNs used in a system depends on the number of possible active service requests and the user-definable organization of the Interrupt Vector Table. The 8-bit SRPNs permit up to 255 sources to be active at one time (remembering that the special SRPN value of 00_H excludes an SRN from taking part in arbitration).

Note: Before modifying the content of an SRPN bit field, the corresponding SRN must be disabled (SRE = 0).

SRPNs in the TC1798

In the TC1798, interrupt sources selecting the same Service Provider are also allowed to have identical SRPN values. In this case, the software (interrupt service routine) must check which of the interrupt sources with identical SRPN has become active.

Note that module-specific interrupt request flags must be available because the SRR flags cannot be used for this check. SRR flags (meaning all SRR flags of interrupts with identical SRPN values) are in general automatically reset by hardware when a service request is acknowledged and serviced.

Note: This practice with identical SRPN values is not recommended as it is not portable to other TriCore devices.

16.3 Interrupt Control Units

The Interrupt Control Units manage the interrupt system, arbitrate incoming service requests, and determine whether and when to interrupt the service provider. The TC1798 contains two interrupt control units, one for the CPU (called ICU), and one for the PCP (called PICU). Each one controls its associated interrupt arbitration bus and manages the communication with its service provider (see).

16.3.1 Interrupt Control Unit (ICU)

This section describes the interrupt control unit (ICU) for the CPU.

16.3.1.1 ICU Interrupt Control Register (ICR)

The ICU Interrupt Control Register ICR holds the current CPU priority number (CCPN), the global interrupt enable/disable bit (IE), the pending interrupt priority number (PIPN), and bit fields which control the interrupt arbitration process.

ICR

ICU Interrupt Control Register (F7E1FE2C$_H$) Reset Value: 0000 0000$_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0					CONECYC	CARBCYC		PIPN							
r					rw	rw		rh							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0							IE	CCPN							
r							rwh	rwh							

Field	Bits	Type	Description
CCPN	[7:0]	rwh	**Current CPU Priority Number** The Current CPU Priority Number (CCPN) bit field indicates the current priority level of the CPU. It is automatically updated by hardware on entry and exit of interrupt service routines, and through the execution of a BISR instruction. CCPN can also be updated through an MTCR instruction.

Field	Bits	Type	Description
IE	8	rwh	**Global Interrupt Enable Bit** The interrupt enable bit globally enables the CPU service request system. Whether or not a service request is delivered to the CPU depends on the individual Service Request Enable Bits (SRE) in the SRNs, and the current state of the CPU. IE is automatically updated by hardware on entry and exit of an Interrupt Service Routine (ISR). IE is cleared to 0 when an interrupt is taken, and is restored to the previous value when the ISR executes an RFE instruction to terminate itself. IE can also be updated through the execution of the ENABLE, DISABLE, MTCR, and BISR instructions. 0 Interrupt system is globally disabled 1 Interrupt system is globally enabled
PIPN	[23:16]	rh	**Pending Interrupt Priority Number** PIPN is a read-only bit field that is updated by the ICU at the end of each interrupt arbitration process. It indicates the priority number of the pending service request. PIPN is set to 0 when no request is pending, and at the beginning of each new arbitration process. 00_H No valid pending request YY_H A request with priority YY_H is pending
CARBCYC	[25:24]	rw	**Number of Arbitration Cycles** CARBCYC controls the number of arbitration cycles used to determine the request with the highest priority. 00_B 4 arbitration cycles (default) 01_B 3 arbitration cycles 10_B 2 arbitration cycles 11_B 1 arbitration cycle
CONECYC	26	rw	**Number of Clocks per Arbitration Cycle Control** The CONECYC bit determines the number of system clocks per arbitration cycle. For the TC1798 this bit can be set to 1 (for SPB frequencies up to the max SPB frequency as defined in the Data Sheet). 0 2 clocks per arbitration cycle (default) 1 1 clock per arbitration cycle
0	[15:9], [31:27]	r	**Reserved** Read as 0; should be written with 0.

16.3.1.2 Operation of the Interrupt Control Unit (ICU)

Service-request arbitration is performed in the ICU in parallel with normal CPU operation. When a triggering event occurs in one or more interrupt sources, the associated SRNs, if enabled, send service requests to the CPU through the ICU. The ICU determines which service request has the highest priority. The ICU will then forward the service request to the CPU. The service request will be acknowledged by the CPU and serviced, depending upon the state of the CPU.

The ICU arbitration process takes place in one or more arbitration cycles over the CPU interrupt arbitration bus. The ICU begins a new arbitration process when a new service request is detected. At the end of the arbitration process, the ICU will have determined the service request with the highest priority number. This number is stored in the ICR.PIPN bit field and becomes the pending service request.

After the arbitration process, the ICU forwards the pending service request to the CPU by attempting to interrupt it. The CPU can be interrupted only if interrupts are enabled globally (that is, ICR.IE = 1) and if the priority of the service request is higher than the current processor priority (ICR.PIPN > ICR.CCPN). Also, the CPU may be temporarily blocked from taking interrupts, for example, if it is executing a multi-cycle instruction such as an atomic read-modify-write operation. The full list of conditions which could block the CPU from immediately responding to an interrupt request generated by the ICU is:

- Current CPU priority, ICR.CCPN, is equal to or higher than the pending interrupt priority, ICR.PIPN
- Interrupt system is globally disabled (ICR.IE = 0)
- CPU is in the process of entering an interrupt- or trap-service routine
- CPU is executing non-interruptible trap services
- CPU is executing a multi-cycle instruction
- CPU is executing an instruction which modifies the conditions of the global interrupt system, such as modifying the ICR
- CPU detects a trap condition (such as context depletion) when trying to enter a service routine

When the CPU is not otherwise prevented from taking an interrupt, the CPU's program counter will be directed to the Interrupt Service Routine entry point associated with the priority of the service request. Next, the CPU saves the value of ICR.PIPN internally, and acknowledges the ICU. The ICU then forwards the acknowledge signal back to the SRN that is requesting service in order to inform it that it will be serviced by the CPU. The SRR bit in this SRN is then reset to 0.

After sending the acknowledgement, the ICU resets ICR.PIPN to 0 and may start a new arbitration process if there is another pending interrupt request. If not, ICR.PIPN remains at 0 and the ICU enters an idle state, waiting for the next interrupt request to awaken it. If there is a new service request waiting, the priority number of the new request will be written to ICR.PIPN at the end of the new arbitration process and the ICU will deliver the pending interrupt to the CPU according to the rules described in this section.

If a new service request is received by the ICU before the CPU has acknowledged the pending interrupt request, the ICU deactivates the pending request and starts a new arbitration process. This reduces the latency of service requests posted before the current request is acknowledged. The ICU deactivates the current pending interrupt request by setting the ICR.PIPN bit field to 0, indicating that the ICU has not yet found a new valid pending request. It then executes its arbitration process again. If the new service request has a higher priority than the previous one, its priority will be written to ICR.PIPN. If the new interrupt has a lower priority, the priority of the previous interrupt request will again be written to ICR.PIPN. In any case, the ICU will deliver a new interrupt request to the CPU according to the rules described in this section.

Once the CPU has acknowledged the current pending interrupt request, any new service request generated by an SRN must wait at least until the end of the next service request arbitration process to be serviced.

Essentially, arbitration in the ICU is performed whenever a new service request is detected, regardless of whether or not the CPU is servicing interrupts. Because of this, the ICR.PIPN bit field always reflects the pending service request with the highest priority. This can, for example, be used by software polling techniques to determine high-priority requests while leaving the interrupt system disabled.

16.3.2 PCP Interrupt Control Unit (PICU)

The PCP Interrupt Control Unit (PICU) is closely coupled with the PCP and its Interrupt Control Register (PCP_PICR). The operation of the PICU is very similar to the ICU of the CPU with respect to the overall scheme.

Note: Details of the PICU and the PCP_ICR register are described in the chapter about the PCP.

16.4 Arbitration Process

The arbitration process implemented in the TC1798 uses a number of arbitration cycles to determine the pending interrupt request with the highest priority number, SRPN. In each of these cycles, two bits of the SRPNs of all pending service requests are compared against each other. The sequence starts with the high-order bits of the SRPNs and works downwards, such that in the last cycle, bits [1:0] of the SRPNs are compared. Thus, to perform an arbitration through all 8 bits of an SRPN, four arbitration cycles are required. There are two factors determining the duration of the arbitration process:

- Number of arbitration cycles, and
- Duration of arbitration cycles.

Both of these can be controlled by the user.

16.4.1 Controlling the Number of Arbitration Cycles

In a real-time system where responsiveness is critical, arbitration must be as fast as possible. However, to maintain flexibility, the TC1798 system is designed to have a large range of service priorities. If not all priorities are needed in a system, arbitration can be accelerated by not examining all the bits used to identify all 255 unique priorities.

For instance, if a 6-bit number is enough to identify all priority numbers used in a system (meaning that bits [7:6] of all SRPNs are always 0), it is not necessary to perform arbitration on these two bits. Three arbitration cycles will be enough to find the highest number in bits [5:0] of the SRPNs of all pending requests. Similarly, the number of arbitration cycles can be reduced to two if only bits [3:0] are used in all SRPNs, and the number of arbitration cycles can be reduced to one cycle if only bits [1:0] are used.

The ICR.CARBCYC bit field controls the number of cycles in the arbitration process. Its default value is 0, which selects four arbitration cycles. **Table 16-1** gives the options for arbitration cycle control.

Table 16-1 Arbitration Cycle Control

Number of Arbitration Cycles	4	3	2	1
ICR.CARBCYC	00_B	01_B	10_B	11_B
Relevant bits of the SRPNs	[7:0]	[5:0]	[3:0]	[1:0]
Range of priority numbers covered	1..255	1..63	1..15	1..3

Note: If less than four arbitration cycles are selected, the corresponding upper bits of the SRPNs are not examined, even if they do not contain zeros.

16.4.2 Controlling the Duration of Arbitration Cycles

During each arbitration cycle, the rate of information flow between the SRNs and the ICU can become limited by propagation delays within the TC1798 when it is executing at high system clock frequencies. At high frequencies, arbitration cycles may require two system clocks to execute properly. In order to optimize the arbitration scheme at lower system frequencies, an additional control bit, ICR.CONECYC, is implemented. The default value of 0 of this bit selects two clock cycles per arbitration cycle. Setting this bit to 1 selects one clock cycle per arbitration cycle. The maximum frequency for the ICR.CONECYC=´1´ setting is defined in the product data sheetSetting this bit for system frequencies above the specified limit leads to unpredictable behavior of the interrupt system. Correct operation is then not guaranteed.

16.5 Entering an Interrupt Service Routine

When an interrupt request from the ICU is pending and all conditions are met such that the CPU can now service the interrupt request, the CPU performs the following actions in preparation for entering the designated Interrupt Service Routine (ISR):

1. Upper context of the current task is saved[1]. The current CPU priority number, ICR.CCPN, and the state of the global interrupt enable bit, ICR.IE, are automatically saved with the PCXI register (bit field PCPN and bit PIE).
2. Interrupt system is globally disabled (ICR.IE is set to 0).
3. Current CPU priority number (ICR.CCPN) is set to the value of ICR.PIPN.
4. PSW is set to a default value:
   a) All permissions are enabled, that is, PSW.IO = 10_B.
   b) Memory protection is switched to PRS0, that is, PSW.PRS = 0.
   c) The stack pointer bit is set to the interrupt stack, that is, PSW.IS = 1.
   d) The call depth counter is cleared, the call depth limit is set to 63, that is, PSW.CDC = 0.
5. Stack pointer, A10, is reloaded with the contents of the Interrupt Stack Pointer, ISP, if the PSW.IS bit of the interrupted routine was set to 0 (using the user stack); otherwise it is left unaltered.
6. CPU program counter is assigned with an effective address consisting of the contents of the BIV register OR-ed with the ICR.PIPN number left-shifted by 5. This indexes the Interrupt Vector Table entry corresponding to the interrupt priority.
7. Contents at the effective address of the program counter in the Interrupt Vector Table are fetched as the first instruction of the Interrupt Service Routine (ISR). Execution continues linearly from there until the ISR branches or exits.

1) Note that, if a context-switch trap occurs while the CPU is in the process of saving the upper context of the current task, the pending ISR will not be entered, the interrupt request will be left pending, and the CPU will enter the appropriate trap handling routine instead.

As explained, receipt of further interrupts is disabled (ICR.IE = 0) when an Interrupt Service Routine is entered. At the same time, the current CPU priority ICR.CCPN is set by hardware to the priority of the interrupting source (ICR.PIPN).

Clearly, before the processor can receive any more interrupts, the ISR must eventually re-enable the interrupt system again by setting ICR.IE = 1. Furthermore, the ISR can also modify the priority number ICR.CCPN to allow effective interrupt priority levels. It is up to the user to enable the interrupt system again and optionally modify the priority number CCPN to implement interrupt priority levels or handle special cases.

To simply enable the interrupt system again, the ENABLE instruction can be used, which sets ICR.IE bit to 1. The BISR instruction offers a convenient way to re-enable the interrupt system, to set ICR.CCPN to a new value, and to save the lower context of the interrupted task. It is also possible to use an MTCR instruction to modify ICR.IE and ICR.CCPN. However, this should be performed together with an ISYNC instruction (which synchronizes the instruction stream) to ensure completion of this operation before the execution of following instructions.

Note: The lower context can also be saved through execution of an SVLCX (Save Lower Context) instruction.

16.6 Exiting an Interrupt Service Routine

When an ISR exits with an RFE (Return From Exception) instruction, the hardware automatically restores the upper context. Register PCXI, which holds the Previous CPU Priority Number (PCPN) and the Previous Global Interrupt Enable Bit (PIE), is a part of this upper context. The value saved in PCPN is written to ICR.CCPN to set the CPU priority number to the value before the interruption, and bit PIE is written to ICR.IE to restore the state of this bit. The interrupted routine then continues.

Note: There is no automatic restoring of the lower context on an exit from an Interrupt Service Routine. If the lower context was saved during the execution of the ISR, either through execution of the BISR instruction or an SVLCX instruction, the ISR must restore the lower context again via the RSLCX (Restore Lower Context) instruction before it exits through RFI execution.

16.7 Interrupt Vector Table

Interrupt Service Routines (ISRs) are associated with interrupts at a particular priority by way of the Interrupt Vector Table. The Interrupt Vector Table is an array of ISR entry points.

When the CPU takes an interrupt, it calculates an address in the Interrupt Vector Table that corresponds with the priority of the interrupt (the ICR.PIPN bit field). This address is loaded in the program counter. The CPU begins executing instructions at this address in the Interrupt Vector Table. The code at this address is the start of the selected ISR. Depending on the code size of the ISR, the Interrupt Vector Table may only store the initial portion of the ISR, such as a jump instruction that vectors the CPU to the rest of the ISR elsewhere in memory.

The Interrupt Vector Table is stored in code memory. The BIV register specifies the base address of the Interrupt Vector Table. Interrupt vectors are ordered in the table by increasing priority.

The Base of Interrupt Vector Table register (BIV) stores the base address of the Interrupt Vector Table. It can be assigned to any available code memory. Its default on power-up is fixed at $0000\ 0000_H$. However, the BIV register can be modified using the MTCR instruction during the initialization phase of the system, before interrupts are enabled. With this arrangement, it is possible to have multiple Interrupt Vector Tables and switch between them by changing the contents of the BIV register.

Note: The BIV register is protected by the ENDINIT bit (see chapter describing the watchdog timer). Modifications should only be done while the interrupt system is globally disabled (ICR.IE = 0). Also, an ISYNC instruction should be issued after modifying BIV to ensure completion of this operation before execution of following instructions.

When interrupted, the CPU calculates the entry point of the appropriate ISR from the PIPN and the contents of the BIV register. The PIPN is left-shifted by five bits and OR-ed with the address in the BIV register to generate a pointer into the Interrupt Vector Table. Execution of the ISR begins at this address. Due to this operation, it is recommended that bits [12:5] of register BIV are set to 0 (see **Figure 16-2**). Note that bit 0 of the BIV register is always 0 and cannot be written to (instructions have to be aligned on even byte boundaries).

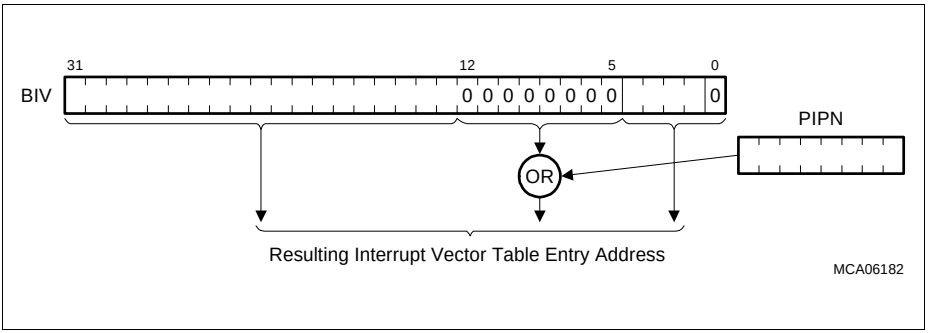


Figure 16-2 Interrupt Vector Table Entry Address Calculation

Left-shifting the PIPN by 5 bits creates entries into the Interrupt Vector Table which are evenly spaced 8 words apart. If an ISR is very short, it may fit entirely within the eight words available in the vector table entry. Otherwise, the code at the entry point must ultimately cause a jump to the rest of the ISR residing elsewhere in memory. Due to the way the vector table is organized according to the interrupt priorities, the TC1798 offers an additional option by allowing spanning several Interrupt Vector Table entries as long as those entries are otherwise unused. **Figure 16-3** illustrates this.

The required size of the Interrupt Vector Table depends only on the range of priority numbers actually used in a system. Of the 256 vector entries, 255 may be used. Vector entry 0 is never used, because if ICR.PIPN is 0, the CPU is not interrupted. Distinct interrupt handlers are supported, but systems requiring fewer entries need not dedicate the full memory area required by the largest configurations.

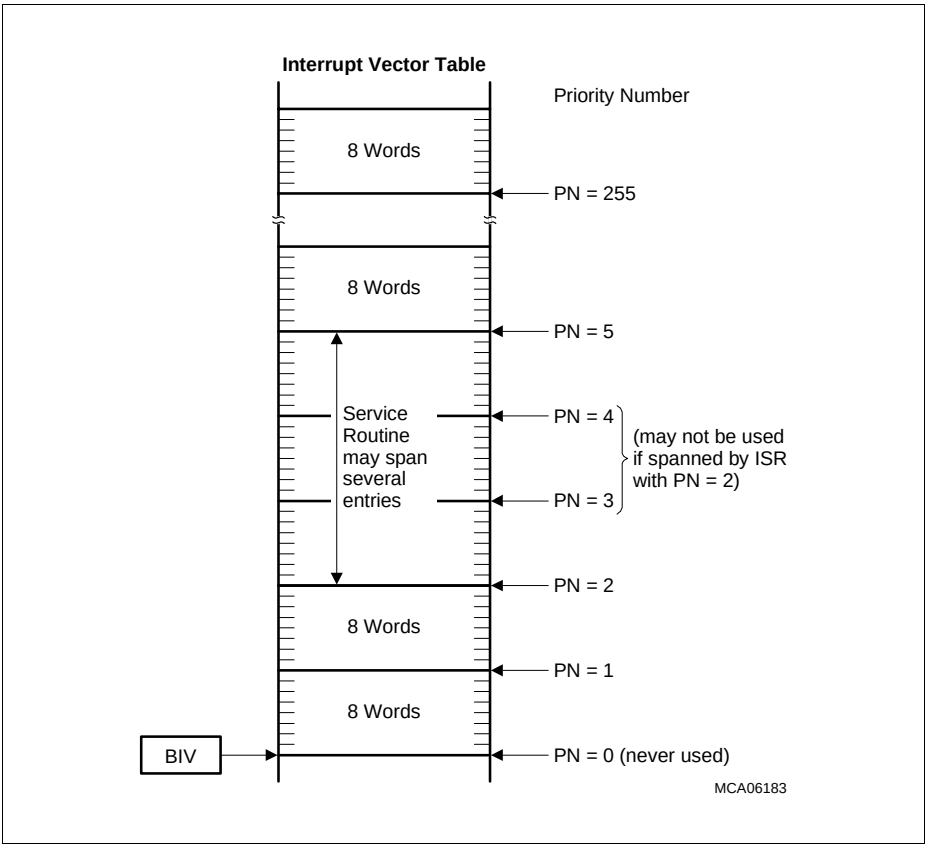


Figure 16-3 Interrupt Vector Table

16.8 Usage of the TC1798 Interrupt System

The following sections provide examples of using the TC1798 interrupt system to solve both typical and special application requirements.

16.8.1 Spanning Interrupt Service Routines Across Vector Entries

Each Interrupt Vector Table entry consists of eight words of memory. If an ISR can be made to fit directly in the Interrupt Vector Table there is no need for a jump instruction to vector to the rest of the interrupt handler elsewhere in memory. However, only the simplest ISRs can fit in the eight words available to a single entry in the table. But it is easy to arrange for ISRs to span across multiple entries, since the Interrupt Vector Table is ordered not by the interrupt source but by interrupt priority. This technique is explained in this section.

In the example of **Figure 16-3**, entry locations 3 and 4 are occupied by the ISR for entry 2. In **Figure 16-3**, the next available entry after entry 2 is entry 5. Of course, if this technique is used, it would be improper to allow any SRN to request service at any of the spanned vector priorities. Thus, priority levels 3 and 4 must not be assigned to SRNs requesting CPU service. They can, however, be used to request PCP service.

There is a performance trade-off that may arise when using this technique because the range of priority numbers used increases. This may have an impact on the number of arbitration cycles required to perform arbitration. Consider the case in which a system uses only three active interrupt sources, that is, where there are only three SRNs enabled to request service. If these three active sources are assigned to priority numbers 1, 2, and 3, it would be sufficient to perform the arbitration in just one cycle. However, if the ISR for interrupt priority 2 is spanned across three Interrupt Vector Table entries as shown in **Figure 16-3**, the priority numbers 1, 2 and 5 would have to be assigned. Thus, two arbitration cycles would have to be used to perform the full arbitration process.

The trade-off between the performance impact of the number of arbitration cycles and the performance gain through spanning service routines can be made by the system designer depending on system needs. Reducing the number of arbitration cycles reduces the service request arbitration latency - spanning service routines reduces the run time of service routines (and therefore also the latency for further interrupts at that priority level or below). For example, if there are multiple fleeting measurements to be made by a system, reducing arbitration latency may be most important. But if keeping total interrupt response time to a minimum is most urgent, spanning Interrupt Vector Table entries may be a solution.

16.8.2 Configuring Ordinary Interrupt Service Routines

When the CPU starts to service an interrupt, the interrupt system is globally disabled and the CPU priority ICR.CCPN is set to the priority of the interrupt now being serviced. This blocks all further interrupts from being serviced until the interrupt system is enabled again.

After an ordinary ISR begins execution, it is usually desirable for the ISR to re-enable global interrupts so that higher-priority interrupts (that is, interrupts that are greater than the current value of ICR.CCPN) can be serviced even during the current ISR's execution. Thus, such an ISR may set ICR.IE = 1 again with, for instance, the ENABLE instruction.

If the ISR enables the interrupt system again by setting ICR.IE = 1 but does not change ICR.CCPN, the effect is that from that point on the hardware can be interrupted by higher-priority interrupts but will be blocked from servicing interrupt requests with the same or lower priority than the current value of bit field ISR.CCPN. Since the current ISR is clearly also at this priority level, the hardware is also blocked from delivering further interrupts to it as well. (This condition is clearly necessary so that the ISR can service the interrupt request automatically.)

When the ISR is finished, it exits with an RFE instruction. Hardware then restores the values of ICR.CCPN and ICR.IE to the values of the interrupted program.

16.8.3 Interrupt Priority Groups

It is sometimes useful to create groups of interrupts at the same or different interrupt priorities that cannot interrupt each other's ISRs. For instance, devices that can generate multiple interrupts may need to have interrupts at different priorities interlocked in this way. The TC1798 interrupt architecture can be used to create such interrupt priority groups. It is effected by managing the current CPU priority level ICR.CCPN in a way described in this section.

For example, in order to make an interrupt priority group out of priority numbers 11 and 12, one would not want an ISR executing at priority 11 to be interrupted by a service request at priority 12, since this would be in the same priority group. Only interrupts above 12 should be allowed to interrupt the ISRs in this interrupt priority group. However, under ordinary ISR usage, the ISR at priority 11 would be interrupted by any request with a higher priority number, including priority 12.

If, however, all ISRs in the interrupt priority group set the value of ICR.CCPN to the highest priority level within their group before they re-enable interrupts, then the desired interlocking will occur.

Figure 16-4 shows an example for interrupt priority grouping. The interrupt requests with the priority numbers 11 and 12 form one group, while the requests with priority numbers 14 through 17 form another group. Each ISR in group 1 sets the value of ICR.CCPN to 12, the highest number in that group, before re-enabling the interrupt system. Each ISR in group 2 sets the value of ICR.CCPN to 17 before re-enabling the interrupt system. If,

for example, interrupt 14 is serviced, it can only be interrupted by requests with a priority number higher than 17; therefore it will not be interrupted by requests from its own priority group or requests with lower priority.

In **Figure 16-4**, the interrupt request with priority number 13 can be said to form an interrupt priority group with just itself as a member.

Setting ICR.CCPN to the maximum value 255 in each service routine has the same effect as not re-enabling the interrupt system; all interrupt requests can then be considered to be in the same group.

Interrupt priority groups demonstrate the power of the TC1798 priority-based interrupt-ordering system. Thus the flexibility of interrupt priority levels ranges from all interrupts in one group to each interrupt request building its own group, and to all possible combinations in between.

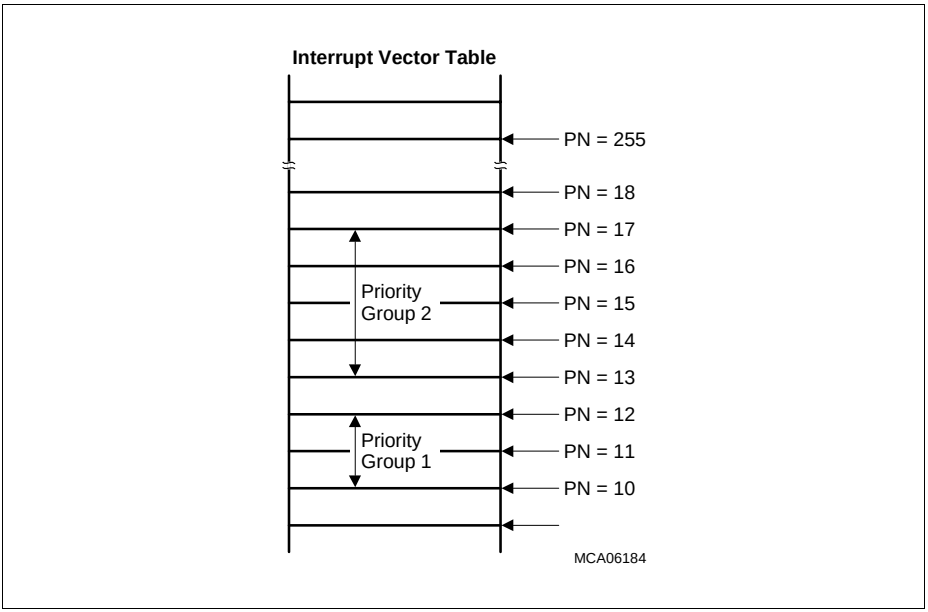


Figure 16-4 Interrupt Priority Groups

16.8.4 Splitting Interrupt Service Across Different Priority Levels

Interrupt service can be divided into multiple ISRs that execute at different priority levels. For example, the beginning stage of interrupt service may be very time-critical, such as reading a data value within a limited time window after the interrupt request activation. However, once the time-critical phase is past, there may still be more to do – for instance,

to process the observation. During this second phase, it may be acceptable for this ISR to be interrupted by lower-level interrupts. This can be performed as follows.

For example, the initial interrupt priority is fixed very high because response time is critical. The necessary actions are carried out immediately by the ISR at that high-priority level. Then the ISR prepares to invoke another ISR at a lower priority level through software to perform the lower-priority actions.

To invoke an ISR through software, the high-priority ISR directly sets an interrupt request bit in an SRN that will invoke the appropriate low-priority ISR. Then the high-priority ISR exits.

When the high-priority ISR exits, the pending low-priority interrupt will eventually be serviced (depending on the priority of other pending interrupts). When the low-priority ISR eventually executes, the low-priority actions of the interrupt will be performed.

The inverse of this method can also be employed, wherein a low-priority ISR raises its own priority level, or leaves interrupts turned off while it executes. For instance, the priority of a service request might be low because the time to respond to the event is not critical, but once it has been granted service, this service should not be interrupted. In this case, the ISR could raise the value of ICR.CCPN to a priority that would exclude some or all other interrupts, or simply leave interrupts disabled.

16.8.5 Using different Priorities for the same Interrupt Source

For some applications, the urgency of a service request may vary, depending on the current state of the system. To handle this, different priority numbers (SRPNs) can be assigned at different times to a service request depending on the application needs.

Of course, Interrupt Service Routines must be placed in the Interrupt Vector Table at all addresses corresponding to the range of priorities used. If service remains the same at different priorities, copies of the ISR can be placed at the possible different entries, or the entries can all vector to a common ISR. If the ISR should execute different code depending on its priority, one need merely put the appropriate ISR in the appropriate entry of the Interrupt Vector Table.

This flexibility is another advantage of the TC1798 interrupt architecture. In traditional interrupt systems where the interrupt vectors are ordered by interrupting source, the ISR would have to check the current priority of the interrupt request and perform a branch to the appropriate code section, causing a delay in the response to the request. In the TC1798, however, the extra check and branch in the ISR are not necessary, hence reduces the interrupt latency.

Because this approach may necessitate an increase in the range of interrupt priorities, the system designer must trade off this advantage against any possible increase in the number of arbitration cycles.

16.8.6 Interrupt Priority 1

Interrupt Priority 1 is the first and lowest-priority entry in the Interrupt Vector Table. It is generally reserved for ISRs which perform task management. ISRs whose actions cause software-managed tasks to be created post a software interrupt request at priority level 1 to signal the event.

The ISR that triggers this event can then execute a normal return from interrupt. There is no need for it to check whether the ISR is returning to the background-task priority level (priority 0) or is returning to a lower-priority ISR that it interrupted. When there is a pending interrupt at a priority higher than the return context for the current interrupt, this interrupt will then be serviced. When a return to the background-task priority level (level 0) is performed, the software-posted interrupt at priority level 1 will be serviced automatically.

16.8.7 Software-Initiated Interrupts

Software can set the service request bit (SRR) in a SRN by writing to its Service Request Control Register. Thus, software can initiate interrupts that are handled by the same mechanism as hardware interrupts.

After the SRR bit is set in an active SRN, there is no way to distinguish between a software-initiated interrupt request and a hardware interrupt request. For this reason, software should only use SRNs and interrupt priority numbers that are not being used for hardware interrupts.

The TC1798 contains four SRNs that support software-initiated interrupts. These SRNs are not connected to peripheral modules and can only cause interrupts when software sets its SRR bit. These SRNs are called the CPU Service Request Nodes (CPU_SRC[3:0]). The PCP can also cause these four SRNs to generate service requests. See also the TriCore chapter for TC1798-specific implementation details of the four CPU Service Request Control Registers.

Additionally, any otherwise unused SRN can be employed to generate software interrupts.

16.8.8 External Interrupts

Four SRNs (SCU_SRC[3:0]) are reserved to handle external interrupts. The setup for external GPIO port input signals (edge/level triggering, gating etc.) that are able to generate an interrupt request is controlled in the External Request Unit (ERU). The ERU functionality is described in detail in the SCU chapter.

16.9 Service Request Node Table

Table 16-2 shows all TC1798 Service Request Nodes.

Table 16-2 Service Request Nodes in the TC1798

Module	No. of Nodes	Description	SRC Register
CPU	4	CPU Service Request Nodes [3:0]	CPU_SRC[3:0]1)
	1	Software Breakpoint Request Node	CPU_SBSRC1)
Cerberus	2	Cerberus/OCDS Request Node[1:0]	CBS_SRC[1:0]
LBCU	1	LBCU Request Node	LBCU_SRC1)
SBCU	1	SBCU Request Node	SBCU_SRC
DMA	8	DMA Service Request Nodes [7:0]	DMA_SRC[7:0]
	4	MLI0 Service Request Nodes [3:0]	DMA_MLI0SRC [3:0]
	2	MLI1 Service Request Nodes [1:0]	DMA_MLI1SRC [1:0]
SDMA	8	Safety DMA Service Request Nodes [7:0]	SDMA_SRC[7:0]
PCP	12	PCP Service Request Nodes [11:0]	PCP_SRC[11:0]1)
STM	2	STM Service Request Nodes [1:0]	STM_SRC[1:0]
SCU	4	SCU Service Request Nodes [3:0]	SCU_SRC[3:0]
ASC0	4	ASC0 Transmit Interrupt Service Request Node	ASC0_TSRC
		ASC0 Receive Interrupt Service Request Node	ASC0_RSRC
		ASC0 Error Interrupt Service Request Node	ASC0_ESRC
		ASC0 Transmit Buffer Interrupt Service Request Node	ASC0_TBSRC
ASC1	4	ASC1 Transmit Interrupt Service Request Node	ASC1_TSRC
		ASC1 Receive Interrupt Service Request Node	ASC1_RSRC
		ASC1 Error Interrupt Service Request Node	ASC1_ESRC
		ASC1 Transmit Buffer Interrupt Service Request Node	ASC1_TBSRC

Table 16-2 Service Request Nodes in the TC1798 (cont'd)

Module	No. of Nodes	Description	SRC Register
SSC0	3	SSC0 Transmit Interrupt Service Request Node	SSC0_TSRC[1)]
		SSC0 Receive Interrupt Service Request Node	SSC0_RSRC[1)]
		SSC0 Error Interrupt Service Request Node	SSC0_ESRC[1)]
SSC1	3	SSC1 Transmit Interrupt Service Request Node	SSC1_TSRC[1)]
		SSC1 Receive Interrupt Service Request Node	SSC1_RSRC[1)]
		SSC1 Error Interrupt Service Request Node	SSC1_ESRC[1)]
SSC2	3	SSC2 Transmit Interrupt Service Request Node	SSC2_TSRC[1)]
		SSC2 Receive Interrupt Service Request Node	SSC2_RSRC[1)]
		SSC2 Error Interrupt Service Request Node	SSC2_ESRC[1)]
SSC3	3	SSC3 Transmit Interrupt Service Request Node	SSC3_TSRC[1)]
		SSC3 Receive Interrupt Service Request Node	SSC3_RSRC[1)]
		SSC3 Error Interrupt Service Request Node	SSC3_ESRC[1)]
SSCG0	1	SSC0 Guardian	SSCG0_GSRC
SSCG1	1	SSC1 Guardian	SSCG1_GSRC
SSCG2	1	SSC2 Guardian	SSCG2_GSRC
SSCG3	1	SSC3 Guardian	SSCG3_GSRC
SENT	4	SENT [3:0]	SENT_SRC[3:0]
SHE	1	Secure Hardware Extension]	SHE_SRC
FCE	1	Flexible CRC Engine	FCE_SRC
BMU	1	Bus Monitor Unit	BMU_SRC
MSC0	2	MSC0 Service Request Nodes [1:0]	MSC0_SRC[1:0]
MSC1	2	MSC1 Service Request Nodes [1:0]	MSC1_SRC[1:0]
CAN	16	CAN Service Request Nodes [15:0]	CAN_SRC[15:0][1)]

Table 16-2 Service Request Nodes in the TC1798 (cont'd)

Module	No. of Nodes	Description	SRC Register
GPTA0	38	GPTA0 Service Request Nodes [37:00]	GPTA0_SRC [37:0]
GPTA1	38	GPTA1 Service Request Nodes [37:00]	GPTA1_SRC [37:0]
LTCA2	8	LTCA Service Request Nodes [07:00]	LTCA2_SRC[07:00]
CC6061	4	CC60 Service Request Nodes [3:0]	CCU60_SRC[3:0]
CC6061	4	CC61 Service Request Nodes [3:0]	CCU61_SRC[3:0]
CC6263	4	CC62 Service Request Nodes [3:0]	CCU62_SRC[3:0]
CC6263	4	CC63 Service Request Nodes [3:0]	CCU63_SRC[3:0]
GPT120	6	GPT12_0 Service Request Nodes [05:00]	GPT120_SRC[05:00]
GPT121	6	GPT12_1 Service Request Nodes [05:00]	GPT121_SRC[05:00]
ADC0	9	ADC0 Service Request Nodes [8:0]	ADC0_SRC[8:0]1)
FADC	4	FADC Service Request Nodes [3:0]	FADC_SRC[3:0]1)
E-Ray	8	Interrupt 0 Service Request Control Register	ERAY_INT0SRC1)
		Interrupt 1 Service Request Control Register	ERAY_INT1SRC1)
		Timer Interrupt 0 Service Request Control Register	ERAY_TINT0SRC1)
		Timer Interrupt 1 Service Request Control Register	ERAY_TINT1SRC1)
		New Data 0 Service Request Control Register	ERAY_NDAT0SRC1)
		New Data 1 Service Request Control Register	ERAY_NDAT1SRC1)
		Message Buffer Status Changed 0 Service Request Control Register	ERAY_MBSC0SRC1)
		Message Buffer Status Changed 1 Service Request Control Register	ERAY_MBSC1SRC1)

1) These service request registers are not bit-addressable because its register address is outside the first 16 Kbyte of a segment.

17 System Timer (STM)

This chapter describes the System Timer (STM). The TC1798's STM is designed for global system timing applications requiring both high precision and long period.

17.1 Overview

The STM has the following features:

- Free-running 56-bit counter
- All 56 bits can be read synchronously
- Different 32-bit portions of the 56-bit counter can be read synchronously
- Flexible service request generation based on compare match with partial STM content
- Counting starts automatically after a reset operation
- STM registers are reset by an application reset if bit ARSTDIS.STMDIS is cleared. If bit ARSTDIS.STMDIS is set, the STM registers are not reset.[1)]
- STM can be halted in debug/suspend mode (via STM_CLC register)

Special STM register semantics provide synchronous views of the entire 56-bit counter, or 32-bit subsets at different levels of resolution.

The maximum timer period is $2^{56} \times f_{STM}$. At f_{STM} = 50 MHz, for example, the STM counts 46.85 years before overflowing. Thus, it is capable of continuously timing the entire expected product life time of a system without overflowing.

17.2 Operation

The STM is an upward counter, running either at the FPI-Bus frequency f_{FPI} or at a fraction of it. The STM clock frequency is $f_{STM} = f_{FPI}$/RMC with RMC = 0-7 (default after reset is $f_{STM} = f_{FPI}/2$, selected by RMC = 010_B). RMC is a bit field in register STM_CLC. In case of an application reset, the STM is reset if bit SCU_ARSTDIS.DIS0 is set. After reset, the STM is enabled and immediately starts counting up. It is not possible to affect the content of the timer during normal operation of the TC1798. The timer registers can only be read but not written to.

The STM can be optionally disabled for power-saving purposes, or suspended for debugging purposes via its clock control register. In suspend mode of the TC1798 (initiated by writing an appropriate value to STM_CLC register), the STM clock is stopped but all registers are still readable.

Due to the 56-bit width of the STM, it is not possible to read its entire content with one instruction. It needs to be read with two load instructions. Since the timer would continue to count between the two load operations, there is a chance that the two values read are not consistent (due to possible overflow from the low part of the timer to the high part

1) "STM registers" means all registers except STM_CLC, STM_SRC0, and STM_SRC1.

between the two read operations). To enable a synchronous and consistent reading of the STM content, a capture register (STM_CAP) is implemented. It latches the content of the high part of the STM each time when one of the registers STM_TIM0 to STM_TIM5 is read. Thus, STM_CAP holds the upper value of the timer at exactly the same time when the lower part is read. The second read operation would then read the content of the STM_CAP to get the complete timer value.

The STM can also be read in sections from seven registers, STM_TIM0 through STM_TIM6, that select increasingly higher-order 32-bit ranges of the STM. These can be viewed as individual 32-bit timers, each with a different resolution and timing range.

The content of the 56-bit System Timer can be compared against the content of two compare values stored in the STM_CMP0 and STM_CMP1 registers. Service requests can be generated on a compare match of the STM with the STM_CMP0 or STM_CMP1 registers.

Figure 17-1 provides an overview on the STM module. It shows the options for reading parts of the STM content.

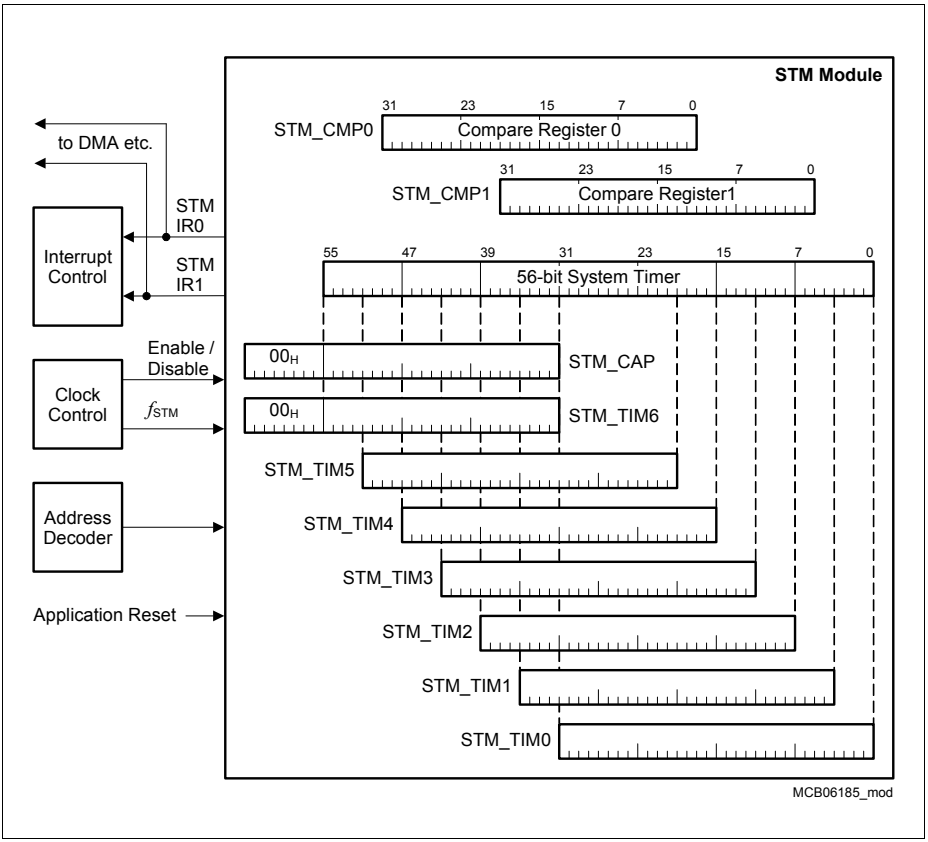


Figure 17-1 General Block Diagram of the STM Module Registers

17.2.1 Resolution and Ranges

Table 17-1 is an overview on the individual timer registers with their resolutions and timing ranges. As an example, the values for 75 MHz STM input clock frequency f_{STM} are given.

Table 17-1 System Timer Resolutions and Ranges

Register	STM Bits	Resolution [s]	Range [s]	Resolution	Range	f_{STM} [MHz]
STM_TIM0	[31:0]	1 / f_{STM}	2^{32} / f_{STM}	13.3 ns	57.3 s	75
STM_TIM1	[35:4]	16 / f_{STM}	2^{36} / f_{STM}	213 ns	916.2 s	
STM_TIM2	[39:8]	256 / f_{STM}	2^{40} / f_{STM}	3.41 µs	244.3 min	
STM_TIM3	[43:12]	4096 / f_{STM}	2^{44} / f_{STM}	54.6 µs	65.1 h	
STM_TIM4	[47:16]	65536 / f_{STM}	2^{48} / f_{STM}	0.874 ms	43.44 days	
STM_TIM5	[51:20]	2^{20} / f_{STM}	2^{52} / f_{STM}	13.98 ms	1.90 yr	
STM_TIM6	[55:32]	2^{32} / f_{STM}	2^{56} / f_{STM}	57.3 s	30.47 yr	
STM_CAP	[55:32]	2^{32} / f_{STM}	2^{56} / f_{STM}	57.3 s	30.47 yr	

17.2.2 Compare Register Operation

The content of the 56-bit STM can be compared against the content of two compare values stored in the STM_CMP0 and STM_CMP1 registers. Service requests can be generated on a compare match of the STM with the STM_CMP0 or STM_CMP1 registers.

Two parameters are programmable for the compare operation:

1. The width of the relevant bits in registers STM_CMP0/STM_CMP1 (compare width MSIZEx) that is taken for the compare operation can be programmed from 1 to 32.
2. The first bit location in the 56-bit STM that is taken for the compare operation can be programmed from 0 to 24.

These programming capabilities make compare functionality very flexible. It even makes it possible to detect bit transitions of a single bit n (n = 0 to 24) within the 56-bit STM by setting MSIZE = 0 and MSTART = n.

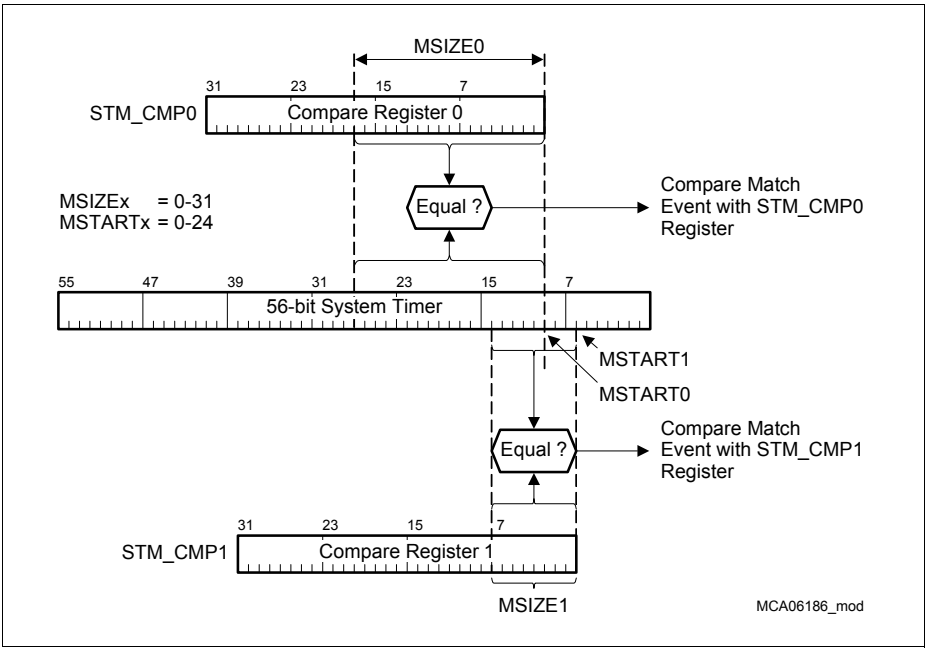


Figure 17-2 Compare Mode Operation

Figure 17-2 shows an example of the compare operation. In this example the following parameters are programmed:

- MSIZE0 = $10001_B = 17_D$; MSTART0 = $01010_B = 9_D$
- MSIZE1 = $00111_B = 7_D$; MSTART1 = $00111_B = 6_D$

A compare operation with MSIZE not equal 0 always implies that the compared value as stored in the CMP register is right-extended with zeros. This means that in the example of **Figure 17-2**, the compare register content STM_CMP0[17:0] plus nine zero bits right-extended is compared with STM[27:0] with STM[8:0] = 000_H. In case of register STM_CMP1, STM[14:0] with STM[5:0] = 00_H are compared with STM_CMP1[8:0] plus six zero bits right-extended.

17.2.3 Compare Match Interrupt Control

The compare match interrupt control logic is shown in **Figure 17-3**. Each STM_CMPx register has its compare match interrupt request flag (STM_ICR.CMPxIR) that is set by hardware on a compare match event. The interrupt request flags can be set (STM_ISSR.CMPxIRS) or cleared (STM_ISSR.CMPxIRR) by software. Note that setting STM_ICR.CMPxIR by writing a 1 into STM_ISSR.CMPxIRS does not generate an interrupt at STMIRx. The compare match interrupts from CMP0 and CMP1 can be further directed by STM_ICR.CMPxOS to either output signal STMIR0 or STMIR1. The STMIR0 and STMIR1 outputs are each connected to interrupt service request control registers, STM_SRC0 and STM_SCR1, respectively.

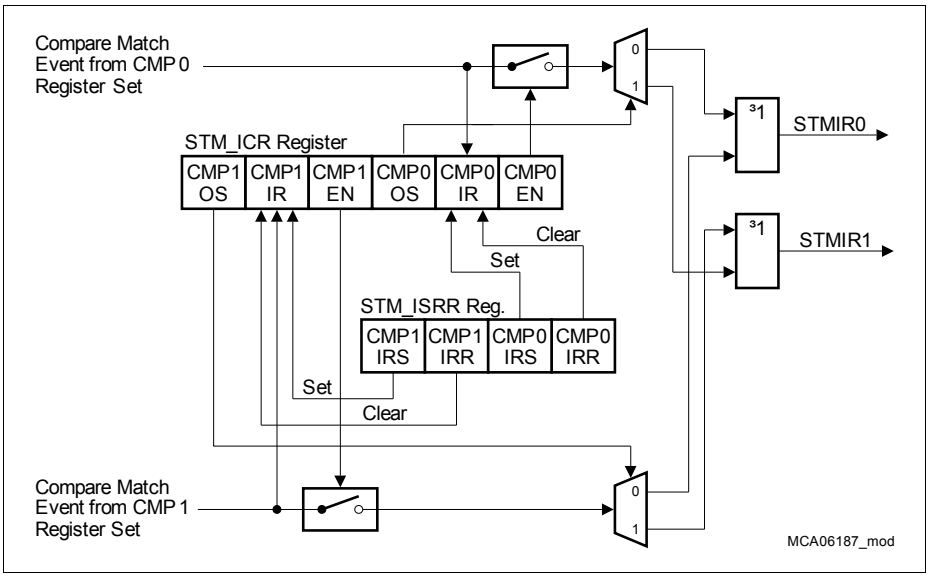


Figure 17-3 STM Interrupt Control

The compare match interrupt flags STM_ICR.CMPxIR are immediately set after an STM reset operation, caused by a compare match event with the reset values of the STM and the compare registers STM_CMPx. This setting of the CMPxIR flags does not directly

generate compare match interrupts because the compare match interrupts are automatically disabled after a STM reset operation (CMPxEN = 0). Therefore, before enabling a compare match interrupt after a STM reset operation, the CMPxIR flags should be cleared by software (writing register STM_ISSR with CMPxIRR set). Otherwise, undesired compare match interrupt events are triggered. Details about DMA connections of STMIR0 and STMIR1 are given in **Table 17-4** on **Page 17-21**.

17.3 STM Registers

This section describes the STM registers of the STM. The STM registers can be divided into four types, as shown in **Figure 17-4**.

STM Registers Overview

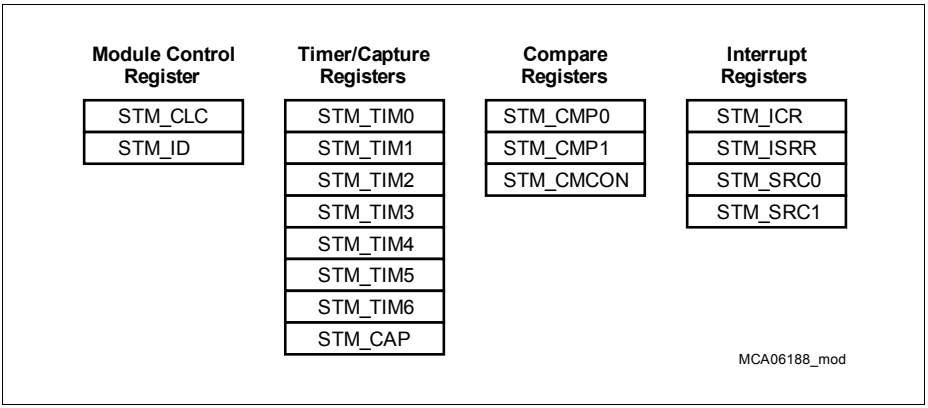


Figure 17-4 STM Registers

In TC1798 all registers are readable is suspend mode. The complete and detailed address map of the STM module with its registers is shown in **Table 17-5** on **Page 17-22**.

Table 17-2 Registers Address Space

Module	Base Address	End Address	Note
STM	$F000\ 0200_H$	$F000\ 02FF_H$	-

Table 17-3 Registers Overview - STM Registers

Register Short Name	Register Long Name	Offset Address	Description see
STM_CLC[1)]	STM Clock Control Register	00_H	Page 17-9
STM_ID	STM Module Identification Register	08_H	Page 17-10
STM_TIM0	STM Timer Register 0	10_H	Page 17-11
STM_TIM1	STM Timer Register 1	14_H	Page 17-11
STM_TIM2	STM Timer Register 2	18_H	Page 17-12
STM_TIM3	STM Timer Register 3	$1C_H$	Page 17-12
STM_TIM4	STM Timer Register 4	20_H	Page 17-12
STM_TIM5	STM Timer Register 5	24_H	Page 17-13
STM_TIM6	STM Timer Register 6	28_H	Page 17-13
STM_CAP	STM Timer Capture Register	$2C_H$	Page 17-14
STM_CMP0	STM Compare Register 0	30_H	Page 17-14
STM_CMP1	STM Compare Register 1	34_H	Page 17-14
STM_CMCON	STM Compare Match Control Register	38_H	Page 17-15
STM_ICR	STM Interrupt Control Register	$3C_H$	Page 17-17
STM_ISRR	STM Interrupt Set/Reset Register	40_H	Page 17-19
STM_SRC1[1)]	STM Service Request Control Register 1	$F8_H$	Page 17-20
STM_SRC0[1)]	STM Service Request Control Register 0	FC_H	Page 17-20

1) These registers are reset by an application reset if bit ARSTDIS.STMDIS is set.

17.3.1 Clock Control Register

The STM clock control register is used to switch the STM on or off and to control its input clock rate. After a power-on reset, the STM is always enabled and starts counting. The STM can be disabled by setting bit DISR to 1.

STM_CLC
STM Clock Control Register **(00_H)** **Reset Value: $0000\ 0200_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

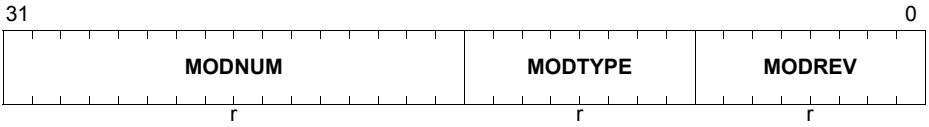
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0					RMC			0		FSOE	SBWE	EDIS	SPEN	DISS	DISR
r					rw			r		rw	w	rw	rw	r	rw

Field	Bits	Type	Description
DISR	0	rw	**Module Disable Request Bit** Used for enable/disable control of the STM module. 0_B No disable requested 1_B Disable requested
DISS	1	r	**Module Disable Status Bit** Bit indicates the current status of the STM module. 0_B STM module is enabled 1_B STM module is disabled
SPEN	2	rw	**Module Suspend Enable for OCDS** Used for enabling the suspend mode.
EDIS	3	rw	**Sleep Mode Enable Control** Used for module sleep mode control.
SBWE	4	w	**Module Suspend Bit Write Enable for OCDS** Determines whether SPEN and FSOE are write-protected.
FSOE	5	rw	**Fast Switch Off Enable** Used for fast clock switch off in OCDS suspend mode.

Field	Bits	Type	Description
RMC	[10:8]	rw	**Clock Divider in Run Mode** 000_B No clock signal f_{STM} generated 001_B Clock signal $f_{STM} = f_{FPI}$ selected 010_B Clock signal f_{STM} / 2 selected (default after reset) 011_B Clock signal f_{STM} / 3 selected ... 111_B Clock signal f_{STM} / 7 selected
0	[7:6], [31:11]	r	**Reserved** Read as 0; should be written with 0.

The STM Module Identification Register ID contains read-only information about the module version.

STM_ID
STM Module Identification Register (08_H) **Reset Value: 0000 C0XX$_H$**

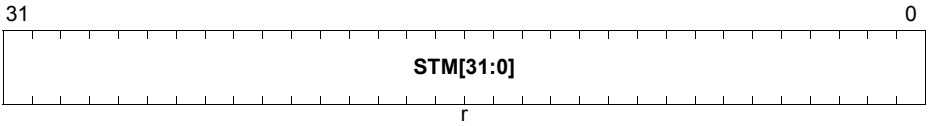


Field	Bits	Type	Description
MODREV	[7:0]	r	**Module Revision Number** MODREV defines the module revision number. The value of a module revision starts with 01_H (first revision).
MODTYPE	[15:8]	r	**Module Type** This bit field defines the module as a 32-bit module: $C0_H$
MODNUM	[31:16]	r	**Module Number Value** This bit field defines the module identification number for the STM: 0000_H

17.3.2 Timer/Capture Registers

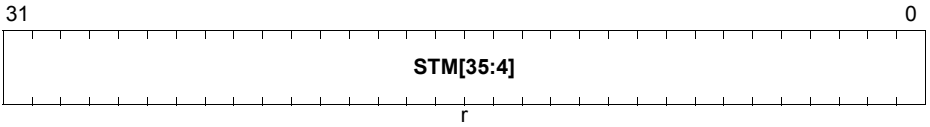
Registers STM_TIM1 to STM_TIM6 provide 32-bit views at varying resolutions of the underlying STM counter.

STM_TIM0
STM Timer Register 0 **(10_H)** **Reset Value: 0000 0000$_H$**



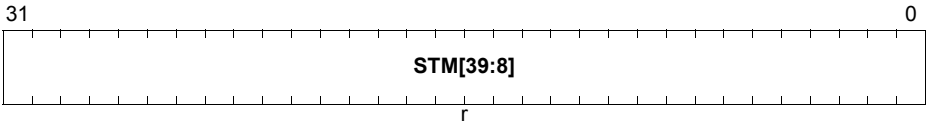
Field	Bits	Type	Description
STM[31:0]	[31:0]	r	**System Timer Bits [31:0]** This bit field contains bits [31:0] of the 56-bit STM.

STM_TIM1
STM Timer Register 1 **(14_H)** **Reset Value: 0000 0000$_H$**



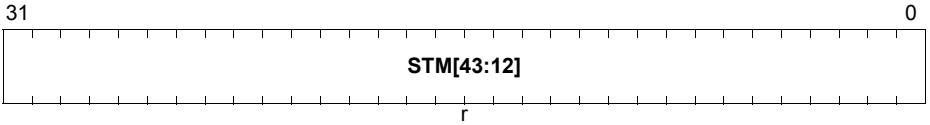
Field	Bits	Type	Description
STM[35:4]	[31:0]	r	**System Timer Bits [35:4]** This bit field contains bits [35:4] of the 56-bit STM.

STM_TIM2
STM Timer Register 2 **(18_H)** **Reset Value: 0000 0000$_H$**



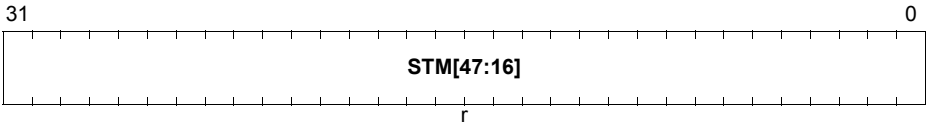
Field	Bits	Type	Description
STM[39:8]	[31:0]	r	**System Timer Bits [39:8]** This bit field contains bits [39:8] of the 56-bit STM.

STM_TIM3
STM Timer Register 3 **($1C_H$)** **Reset Value: 0000 0000$_H$**



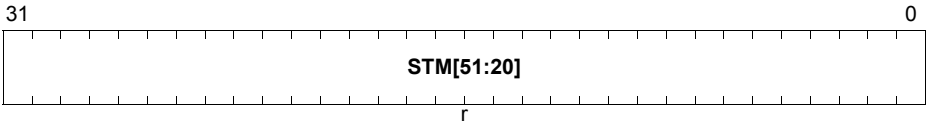
Field	Bits	Type	Description
STM[43:12]	[31:0]	r	**System Timer Bits [43:12]** This bit field contains bits [43:12] of the 56-bit STM.

STM_TIM4
STM Timer Register 4 **(20_H)** **Reset Value: 0000 0000$_H$**



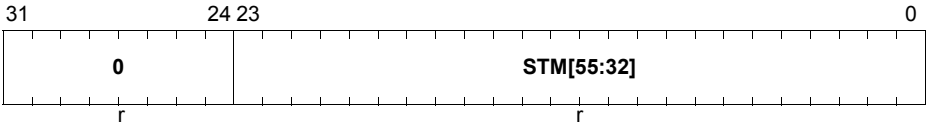
Field	Bits	Type	Description
STM[47:16]	[31:0]	r	**System Timer Bits [47:16]** This bit field contains bits [47:16] of the 56-bit STM.

STM_TIM5
STM Timer Register 5 **(24_H)** **Reset Value: 0000 0000$_H$**



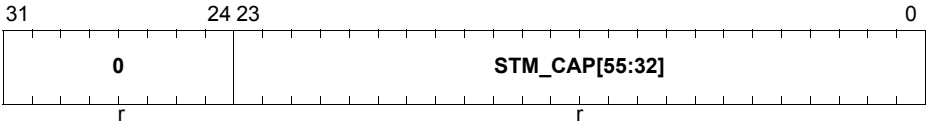
Field	Bits	Type	Description
STM[51:20]	[31:0]	r	**System Timer Bits [51:20]** This bit field contains bits [51:20] of the 56-bit STM.

STM_TIM6
STM Timer Register 6 **(28_H)** **Reset Value: 0000 0000$_H$**



Field	Bits	Type	Description
STM[55:32]	[23:0]	r	**System Timer Bits [55:32]** This bit field contains bits [55:32] of the 56-bit STM.
0	[31:24]	r	**Reserved** Read as 0.

STM_CAP
STM Timer Capture Register **($2C_H$)** **Reset Value: 0000 0000$_H$**



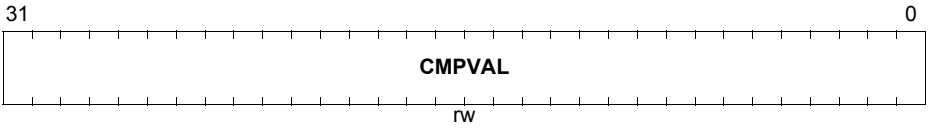
Field	Bits	Type	Description
STM[55:32]	[23:0]	r	**Captured System Timer Bits [55:32]** The capture register STM_CAP always captures the STM bits [55:32] when one of the registers STM_TIM0 to STM_TIM5 is read. This capture operation is performed in order to enable software to operate with a coherent value of all the 56 STM bits at one time stamp.This bit field contains bits [55:32] of the 56-bit STM.
0	[31:24]	r	**Reserved** Read as 0.

Note: The bits in registers STM_CAP to STM_TIM0 are all read-only bits.

17.3.3 Compare Registers

The compare register CMPx holds up to 32-bits; its value is compared to the value of the STM.

STM_CMPx (x = 0-1)
STM Compare Register x **(30_H+x*4_H)** **Reset Value: 0000 0000$_H$**



Field	Bits	Type	Description
CMPVAL	[31:0]	rw	**Compare Value of Compare Register x** This bit field holds up to 32 bits of the compare value (right-adjusted).

The STM Compare Match Control Register controls the parameters of the compare logic.

STM_CMCON
STM Compare Match Control Register

(38_H) **Reset Value: $0000\ 0000_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0			MSTART1					0			MSIZE1				
r			rw					r			rw				

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0			MSTART0					0			MSIZE0				
r			rw					r			rw				

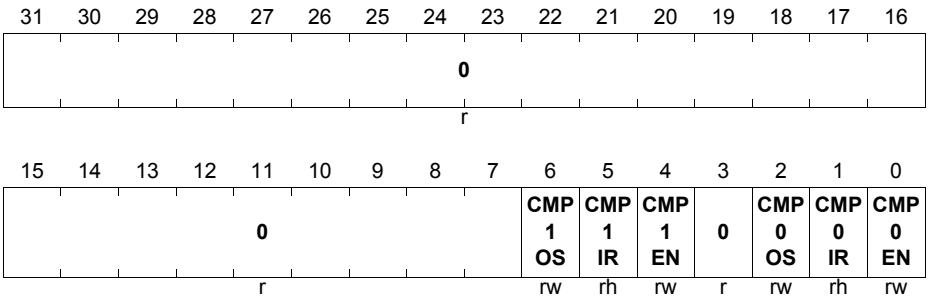
Field	Bits	Type	Description
MSIZE0	[4:0]	rw	**Compare Register Size for CMP0** This bit field determines the number of bits in register CMP0 (starting from bit 0) that are used for the compare operation with the System Timer. 00000_B CMP0[0] used for compare operation 00001_B CMP0[1:0] used for compare operation ... 11110_B CMP0[30:0] used for compare operation 11111_B CMP0[31:0] used for compare operation
MSTART0	[12:8]	rw	**Start Bit Location for CMP0** This bit field determines the lowest bit number of the 56-bit STM that is compared with the content of register CMP0 bit 0. The number of bits to be compared is defined by bit field MSIZE0. 00000_B STM[0] is the lowest bit number 00001_B STM[1] is the lowest bit number ... 10111_B STM[23] is the lowest bit number 11000_B STM[24] is the lowest bit number Bit combinations 11001_B to 11111_B are reserved and must not be used.

Field	Bits	Type	Description
MSIZE1	[20:16]	rw	**Compare Register Size for CMP1** This bit field determines the number of bits in register CMP1 (starting from bit 0) that are used for the compare operation with the System Timer. 00000_B CMP1[0] used for compare operation 00001_B CMP1[1:0] used for compare operation ... 11110_B CMP1[30:0] used for compare operation 11111_B CMP1[31:0] used for compare operation
MSTART1	[28:24]	rw	**Start Bit Location for CMP1** This bit field determines the lowest bit number of the 56-bit STM that is compared with the content of register CMP1 bit 0. The number of bits to be compared is defined by bit field MSIZE1. 00000_B STM[0] is the lowest bit number 00001_B STM[1] is the lowest bit number ... 10111_B STM[23] is the lowest bit number 11000_B STM[24] is the lowest bit number Bit combinations 11001_B to 11111_B are reserved and must not be used.
0	[7:5], [15:13], [23:21], [31:29]	r	**Reserved** Read as 0; should be written with 0.

17.3.4 Interrupt Registers

The two compare match interrupts of the STM are controlled by the STM Interrupt Control Register.

STM_ICR
STM Interrupt Control Register ($3C_H$) Reset Value: 0000 0000$_H$

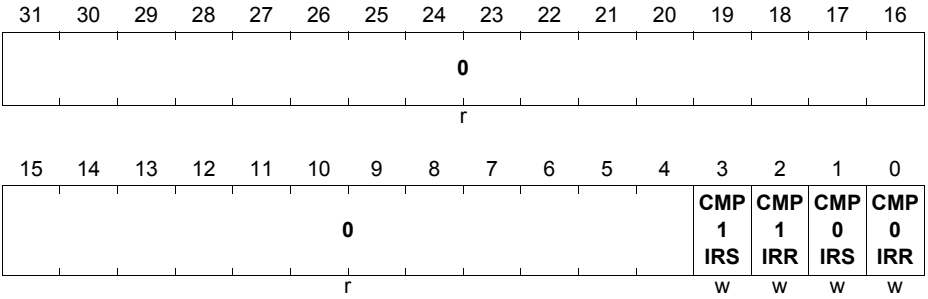


Field	Bits	Type	Description
CMP0EN	0	rw	**Compare Register CMP0 Interrupt Enable Control** This bit enables the compare match interrupt with compare register CMP0. 0_B Interrupt on compare match with CMP0 disabled 1_B Interrupt on compare match with CMP0 enabled
CMP0IR	1	rh	**Compare Register CMP0 Interrupt Request Flag** This bit indicates whether or not a compare match interrupt request of compare register CMP0 is pending. CMP0IR must be cleared by software. 0_B A compare match interrupt has not been detected since the bit has been cleared for the last time. 1_B A compare match interrupt has been detected. CMPIR0 must be cleared by software and can be set by software, too (see CMPISRR register). After a STM reset operation, CMP0IR is immediately set as a result of a compare match event with the reset values of the STM and the compare registers CMP0.

Field	Bits	Type	Description
CMP0OS	2	rw	**Compare Register CMP0 Interrupt Output Selection** This bit determines the interrupt output that is activated on a compare match event of compare register CMP0. 0_B Interrupt output STMIR0 selected 1_B Interrupt output STMIR1 selected
CMP1EN	4	rw	**Compare Register CMP1 Interrupt Enable Control** This bit enables the compare match interrupt with compare register CMP1. 0_B Interrupt on compare match with CMP1 disabled 1_B Interrupt on compare match with CMP1 enabled
CMP1IR	5	rh	**Compare Register CMP1 Interrupt Request Flag** This bit indicates whether or not a compare match interrupt request of compare register CMP1 is pending. CMP1IR must be cleared by software. 0_B A compare match interrupt has not been detected since the bit has been cleared for the last time. 1_B A compare match interrupt has been detected. CMPIR1 must be cleared by software and can be set by software, too (see CMPISRR register). After a STM reset, CMP1IR is immediately set as a result of a compare match event with the reset values of the STM and the compare register CMP1.
CMP1OS	6	rw	**Compare Register CMP1 Interrupt Output Selection** This bit determines the interrupt output that is activated on a compare match event of compare register CMP1. 0_B Interrupt output STMIR0 selected 1_B Interrupt output STMIR1 selected
0	3, [31:7]	r	**Reserved** Read as 0; should be written with 0.

The bits in the STM Interrupt Set/Reset Register make it possible to set or cleared the compare match interrupt request status flags of register ICR.

STM_ISRR
STM Interrupt Set/Reset Register (40_H) Reset Value: 0000 0000_H



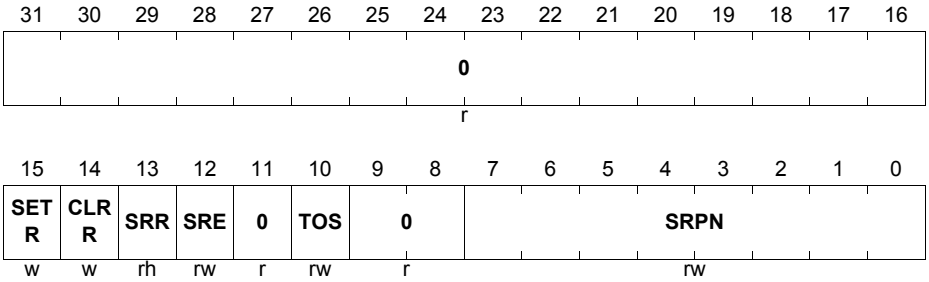
Field	Bits	Type	Description
CMP0IRR	0	w	**Reset Compare Register CMP0 Interrupt Flag** 0_B Bit ICR.CMP0IR is not changed. 1_B Bit ICR.CMP0IR is cleared.
CMP0IRS	1	w	**Set Compare Register CMP0 Interrupt Flag** 0_B Bit ICR.CMP0IR is not changed. 1_B Bit ICR.CMP0IR is set. The state of bit CMP0IRR is “don’t care” in this case.
CMP1IRR	2	w	**Reset Compare Register CMP1 Interrupt Flag** 0_B Bit ICR.CMP1IR is not changed. 1_B Bit ICR.CMP1IR is cleared.
CMP1IRS	3	w	**Set Compare Register CMP1 Interrupt Flag** 0_B Bit ICR.CMP1IR is not changed. 1_B Bit ICR.CMP1IR is set. The state of bit CMP1IRR is “don’t care” in this case.
0	[31:4]	r	**Reserved** Read as 0; should be written with 0.

Note: Reading register CMISRR always returns 0000 0000_H.

In the TC1798, the compare match interrupt output signals of the STM, STMIR0 and STMIR1 are controlled by the STM Service Request Control Registers STM_SRC0 and STM_SRC1.

STM_SRC0
STM Service Request Control Register 0
(FC_H) **Reset Value: 0000 0000$_H$**

STM_SRC1
STM Service Request Control Register 1
($F8_H$) **Reset Value: 0000 0000$_H$**



Field	Bits	Type	Description
SRPN	[7:0]	rw	**Service Request Priority Number**
TOS	10	rw	**Type of Service Control**
SRE	12	rw	**Service Request Enable**
SRR	13	rh	**Service Request Flag**
CLRR	14	w	**Request Clear Bit**
SETR	15	w	**Request Set Bit**
0	[9:8], 11, [31:16]	r	**Reserved** Read as 0; should be written with 0.

17.4 STM Module Implementation

This section defines implementation specific details of the STM in the TC1798.

17.4.1 On-chip Service Request Connections

The two compare match service request outputs STMIR0 and STMIR1 are connected in the TC1798 to on-chip devices as described in **Table 17-4**.

Table 17-4 System Timer On-Chip Interconnections

Service Request Signal	Connected to
STMIR0	DMA Channel 00 Request Input 8 DMA Channel 01 Request Input 8 DMA Channel 02 Request Input 8 DMA Channel 03 Request Input 8 DMA Channel 04 Request Input 8 DMA Channel 05 Request Input 8 DMA Channel 06 Request Input 8 DMA Channel 07 Request Input 8 DMA Channel 10 Request Input 8 DMA Channel 11 Request Input 8 DMA Channel 12 Request Input 8 DMA Channel 13 Request Input 8 DMA Channel 14 Request Input 8 DMA Channel 15 Request Input 8 DMA Channel 16 Request Input 8 DMA Channel 17 Request Input 8
STMIR1	ADC0_REQGT[4:0]_5 ADC1_REQGT[4:0]_5 ADC2_REQGT[4:0]_5

17.4.2 STM Address Map

Table 17-5 defines the complete address range of the STM with absolute addresses and the read/write access rights.

Table 17-5 Address Map of STM

Short Name	Description	Address	Access Mode		Reset Value
			Read	Write	
System Timer (STM)					
STM_CLC	STM Clock Control Register	F000 0200$_H$	U, SV	SV, E	0000 0200$_H$
–	Reserved	F000 0204$_H$	BE	BE	–
STM_ID	STM Module Identification Register	F000 0208$_H$	U, SV	BE	0000 C0XX$_H$
–	Reserved	F000 020C$_H$	BE	BE	–
STM_TIM0	STM Timer Register 0	F000 0210$_H$	U, SV	U, SV	0000 0000$_H$
STM_TIM1	STM Timer Register 1	F000 0214$_H$	U, SV	U, SV	0000 0000$_H$
STM_TIM2	STM Timer Register 2	F000 0218$_H$	U, SV	U, SV	0000 0000$_H$
STM_TIM3	STM Timer Register 3	F000 021C$_H$	U, SV	U, SV	0000 0000$_H$
STM_TIM4	STM Timer Register 4	F000 0220$_H$	U, SV	U, SV	0000 0000$_H$
STM_TIM5	STM Timer Register 5	F000 0224$_H$	U, SV	U, SV	0000 0000$_H$
STM_TIM6	STM Timer Register 6	F000 0228$_H$	U, SV	U, SV	0000 0000$_H$
STM_CAP	STM Timer Capture Reg.	F000 022C$_H$	U, SV	U, SV	0000 0000$_H$
STM_CMP0	STM Compare Register 0	F000 0230$_H$	U, SV	U, SV	0000 0000$_H$
STM_CMP1	STM Compare Register 1	F000 0234$_H$	U, SV	U, SV	0000 0000$_H$
STM_ CMCON	STM Compare Match Control Register	F000 0238$_H$	U, SV	U, SV	0000 0000$_H$
STM_ICR	STM Interrupt Control Register	F000 023C$_H$	U, SV	U, SV	0000 0000$_H$
STM_ISRR	STM Interrupt Set/Reset Register	F000 0240$_H$	U, SV	U, SV	0000 0000$_H$
–	Reserved	F000 0244$_H$ - F000 02F4$_H$	BE	BE	–
STM_ SRC1	STM Service Request Control Register 1	F000 02F8$_H$	U, SV	U, SV	0000 0000$_H$
STM_ SRC0	STM Service Request Control Register 0	F000 02FC$_H$	U, SV	U, SV	0000 0000$_H$

18 Bus Monitor Unit (BMU)

This document describes the functionality of the Bus Monitor Unit (BMU). The BMU is primarily intended to be used in High Integrity Safety Applications. It provides the base hardware mechanisms to simplify the monitoring functions that safety applications need to implement. The core functionality of the BMU consists of logging the peripheral bus write activity. The logged information is stored in a local buffer managed as a cyclic buffer. In non-safety applications the BMU can be used as a PCP data memory extension. The BMU operates as a standard FPI bus slave peripheral and is fully controlled through a set of configuration and control registers. Additionally a dedicated slave interface enables burst accesses to the logged information.

This chapter is structured as follows:

- BMU Features (see **Section 18.2**)
- An operational overview of the BMU Module (see **Section 18.3**)
- Functional description of the BMU Module (see **Section 18.4**)
- Interfaces of the BMU Module (see **Section 18.5**)
- Description of the BMU Module registers (see **Section 18.6**)

18.1 Related documentation

Input documents

- [D1] PRO-SIL Safety Concept for Microcontrollers

Related standards and norms

- [S1] IEC61508 standard. Functional safety of electrical/electronic/programmable electronic safety-related systems Parts 2,7.
- [S2] ISO26262 standard. Road vehicles - Functional safety - Part 5: Product development: hardware level

18.2 BMU Features

The BMU implements the following features:

- Fully synchronous module running at the Peripheral Bus clock frequency
- Implements a standard interrupt service node connecting to the TriCore and PCP interrupt busses.
  - Every internal interrupt source can be identified by a dedicated status flag, cleared by software only. New interrupt events with an active status flag do not lead to a new interrupt.
- Logs write transactions to software selectable peripheral address space
  - Uses the System-on-chip Address decoders select lines to qualify target peripherals (no internal address space decoding)
  - The address phase from master accesses initiated by the Secure Hardware Extension module can optionally be logged. Data phase information is excluded because of secure keys exchange (the address map of the SHE is not visible to the BMU).
- Implements a Bus Transaction Fifo (BTF) that can be accessed via the FPI slave interface using BTR2, BTR4 or BTR8 FPI read bursts. The size of the BTF can be configured on a product basis. It must be a power of two in size.
  - The BTF entries are protected by Error Correction Codes (ECC) with single-bit error correction and double-bit error detection capability (SECDED) covering the data field.
  - The BTF is accessed as a cyclic buffer with automatic wrap around support. The BTF write and read pointers are controlled by Hardware.
- The BTF entries are made of the following FPI information:
  - FPI_A[27:2] address bits of the FPI transaction.
  - FPI_SVM FPI supervisor mode indication
  - FPI_TAG[3:0] FPI TAG, identifies the FPI bus master
  - FPI_STATUS Transaction completion status. This is not an FPI signal
  - FPI_D[31:0] FPI write data
- Fifo Handler that monitors the fullness of the BTF:
  - implements a configurable threshold register to early detect fullness threshold.
  - detects and prevents overruns and underruns (configurable).
- The BTF can be used as a standard memory mapped SRAM in non-safety applications. The SRAM can only be accessed using BTR2, BTR4 or BTR8 FPI bursts.

18.3 Operational overview

18.3.1 Microcontroller Monitoring Framework

The BMU is a component of the PRO-SIL™ Monitoring Framework that enables to simplify the overall software monitoring requirements a safety application must fulfil. Two practical use cases are presented that directly take benefit of the BMU:

- Break-After-Make flow
- Detection of illegal access to safety-related Configuration and Status Registers (CSFR)

Break-After-Make use case

In a single processing channel (a microcontroller without hardware redundancy at the application level) there are two common architectures dealing with the detection of failures at the execution level:

- two processors running in static lockstep or loosely coupled lockstep mode, executing the same safety code and comparing the results in a near cycle accurate fashion. Any discrepancy between the master CPU and the checker CPU caused by any soft or hardware fault is captured by an independent compare unit. The checker CPU does not produce any data to the peripherals nor to the storage elements (SRAMs). The lockstep flow is presented in **Figure 18-1 “Break-After-Make concept” on Page 18-5** (left side).
- a single processor runs sequentially two redundant tasks. The redundant tasks can be implemented with diversity. There is a control task (or control execution thread) that executes and commits its results to the peripherals. The results from the control task need to be saved in order to be checked at a later time. The monitor task (or monitor execution thread) is then scheduled and produces an alternate set of data. The results of both tasks/threads are gathered and compared by an hardware unit independent to the processor. The control flow is presented in **Figure 18-1 “Break-After-Make concept” on Page 18-5** (right side). This is the basic scheme used in the PRO-SIL™ safety concept. The combination of the BMU hardware and the BMU driver running on the PCP provide a generic mechanism that can be used by safety applications to monitor specific data flows to safety-relevant peripherals. The BMU software driver specification is not in the scope of this document.

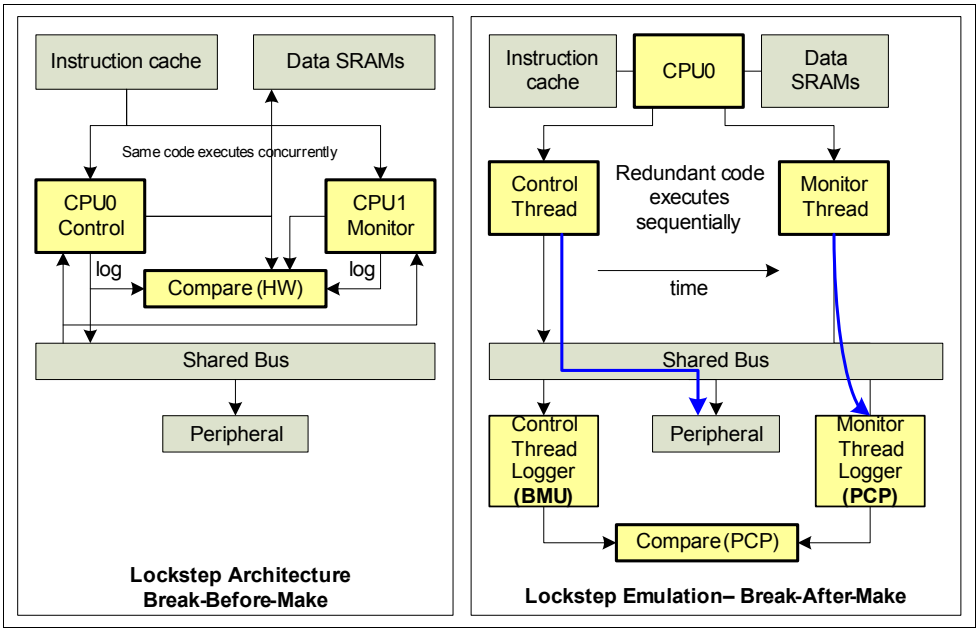


Figure 18-1 Break-After-Make concept

18.3.2 Bus Monitor Unit Overview

The BMU is a standard FPI slave module that implements a FPI slave interface and a Bus Peripheral Interface (BPI) compliant with the FPI bus architecture. The BMU is not FPI master capable. The BMU is fully synchronous with the FPI bus clock and runs with a 1:1 clock ratio. It does not implement a fractional divider

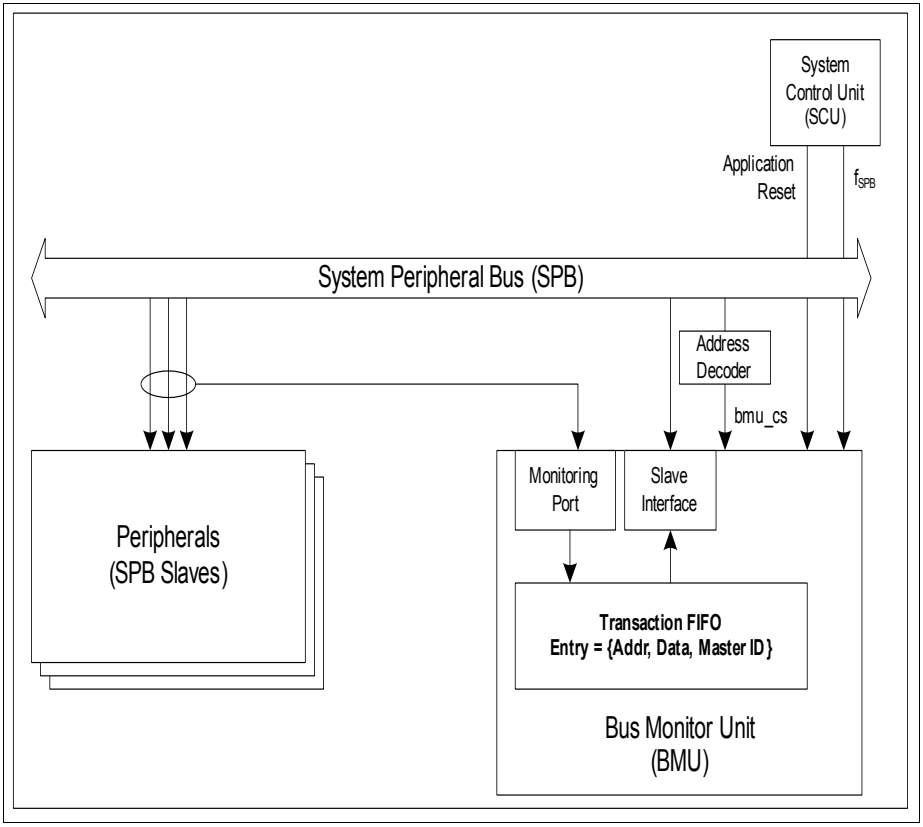


Figure 18-2 BMU overview

In addition to the standard FPI connectivity, the BMU also receives the individual peripheral select signals decoded by the address decoders. **The granularity of each select line is not a peripheral but a FPI region that may include several peripherals**. Each decoded region provides a FPI_ACK[1:0] signal that indicates the completion status of each individual data phase. The FPI_ACK[1:0] of the FPI regions listed in **Table 18-4 “Identification of FPI Regions” on Page 18-22** are required by the BMU to determine if write transactions have been normally terminated or not.

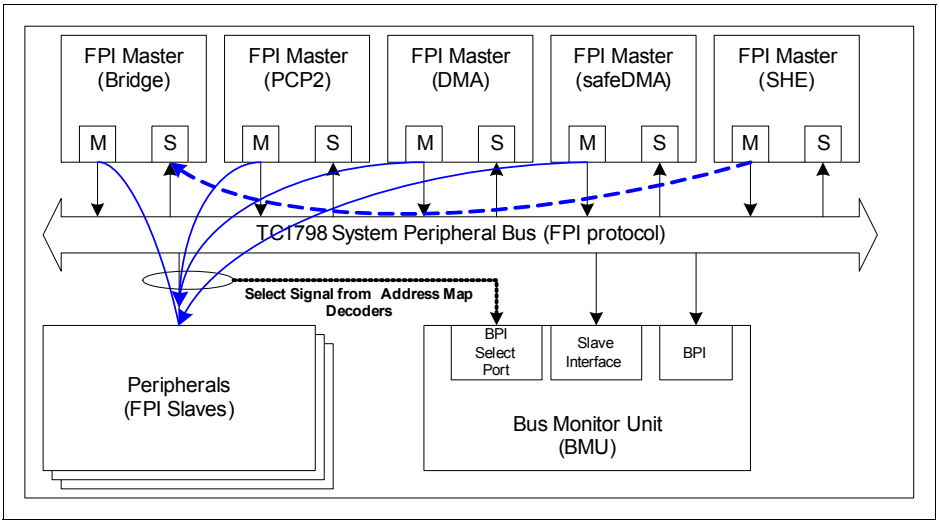


Figure 18-3 BMU operation in TC1798

In a typical microcontroller architecture, the write accesses to the peripherals can be directly controlled by the TriCore CPU or via DMA engines and possibly by the Peripheral Control Processor (PCP). In the TC1798 microcontroller four possible masters (see **Figure 18-3 "BMU operation in TC1798" on Page 18-7**) can control the write data accesses to the peripherals.

Logging SHE write transaction in the TC1798 microcontroller

The Secure Hardware Extension (SHE) module also implements a DMA capability but is not supposed to perform write accesses to peripherals in a Safety Application. Because the SHE module is used in security applications, logging of data written into the SHE is forbidden. For debug purposes it is possible to log the address of write accesses performed by the SHE module, the write data from the FPI bus is ignored and replaced by all zeros. The four upper bits of the address and the two lower bits of the address generated by the SHE module are not logged. The only way to identify that the logging information is related to a SHE write transaction is by using the master identifier information that is logged into the BMU (see **Figure 18-5 "Bus Transaction Information" on Page 18-12**).

18.4 BMU Functional Description

18.4.1 BMU Microarchitecture

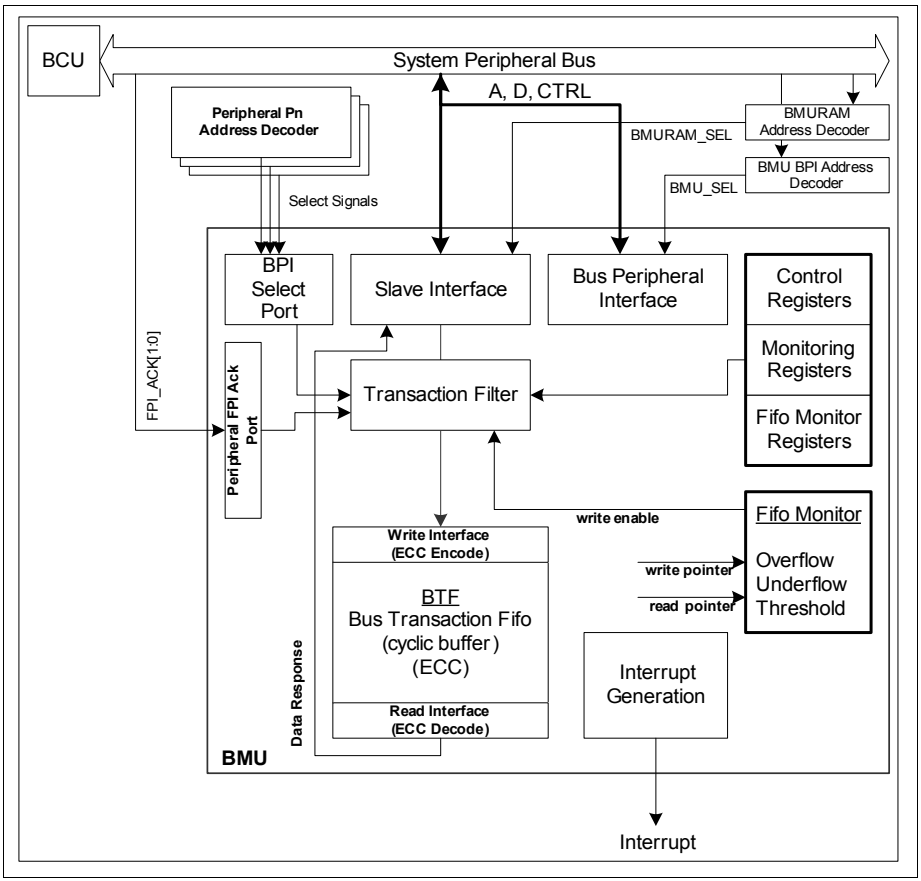


Figure 18-4 BMU Microarchitecture

The BMU is made of the following functions as represented in **Figure 18-4 "BMU Microarchitecture" on Page 18-8**:

- a FPI Bus Peripheral Interface (BPI) that allows software to control the features of the BMU and read status information.
- a cyclic buffer called the Bus Transaction Fifo (BTF) where the selected write transaction are stored.
- a Fifo Monitor that monitors the distance between the BTF write and read pointers. The Fifo Monitor is configured with a threshold register **FMTH** that enables the BMU to raise an interrupt if the threshold is reached.
- a FPI Slave Interface that provides the following functions:
  - filter write transactions taking place in the bus, and if all conditions are fulfilled write the information inside the BTF. The hardware is responsible for the write pointer wrap around conditions.
  - perform memory mapped read and write accesses to the BMU RAM. **This mode is the default one after power-on reset.** Refer to section **"Usage in non safety applications" on Page 18-20** for a description of this mode. The BMU RAM is intended to be use by the PCP processor.
  - perform FIFO-based accesses to the BTF to read the logged information. This mode should be enabled in the **CTL** register. In FIFO mode, the FPI_A[31:0] address information is not used to directly access an entry in the BTF. The internal read and write pointers are updated according to the size of the FPI bus burst transaction.
  - **Table 18-1 "FPI Access Modes to BMU FPI Slave Interface" on Page 18-10** provides the list of FPI transactions supported by the slave interface in the different modes.
- a Service Request Node that centralizes all internal interrupt sources and enables the BMU to directly send interrupt requests to the PCP or the TriCore CPUs.

Table 18-1 FPI Access Modes to BMU FPI Slave Interface

FPI Transaction FPI_OPC[3:0]		Transaction Logging in FIFO Mode	Transaction Support in FIFO Mode	Transaction Support in SRAM Mode
SDTB (8-bit single transfer)	Read	Not Applicable	No (Bus Error)	No (Bus Error)
	Write	**Yes**	No (Bus Error)	No (Bus Error)
SDTH (16-bit single transfer)	Read	Not Applicable	No (Bus Error)	No (Bus Error)
	Write	**Yes**	No (Bus Error)	No (Bus Error)
SDTW (32-bit single transfer)	Read	Not Applicable	No (Bus Error)	No (Bus Error)
	Write	**Yes**	No (Bus Error)	No (Bus Error)
BTR2 (2 transfers of 32-bit)	Read	Not Applicable	**Yes**	**Yes**
	Write	**Yes**	No (Bus Error)	**Yes**
BTR4 (4 transfers of 32-bit)	Read	Not Applicable	**Yes**	**Yes**
	Write	**Yes**	No (Bus Error)	**Yes**
BTR8 (8 transfers of 32-bit)	Read	Not Applicable	**Yes**	**Yes**
	Write	**Yes**	No (Bus Error)	**Yes**

*Note: Single transfer transactions (SDTB, SDTH,SDTW) part of a **Read-Modify-Write** are logged as well.*

Note: During any SDTB, SDTH single transfer transactions the whole 32-bit data bus is written. As the FPI opcode and the lower two bits of the FPI address are not logged, it is not possible to know which bytes were valid during the write. This is a limitation that should be considered by the data monitoring applications using the BMU.

18.4.2 Handling of FPI corner cases

There are specific situations that lead to exceptions with respect to the correct termination of a FPI write transaction, like: master aborts, slave retries, time-out,... The flag FPI_STATUS indicates if the write data phase has been normally completed (FPI_STATUS = 1) or not (FPI_STATUS = 0). In the case of an error there is no additional information that defines the nature of the error.

A Data Phase is completed when the target BPI interface issues a FPI_RDY=1; the signal FPI_ACK[1:0] provides additional information about the status of the completion. The BPI can insert wait states in the FPI bus by delaying the assertion of FPI_RDY. The following situations lead to the detection of an error condition indicating that a write data phase has been either aborted by the master or not accepted by the slave:

- The FPI Master FPI_ABORT_N is asserted during the data phase wait states or coincides with the FPI_RDY assertion by the BPI. If this happens during a burst all subsequent data phases are aborted.
- The BPI issues FPI_RDY=1 together with FPI_ACK=2'b11 (ERR).
- The BPI issues FPI_RDY=1 together with FPI_ACK=2'b10 (RTY).
- In the occurrence of a timeout, FPI_TOUT is issued by the Bus Control Unit during one clock cycle and the selected slave must terminate the data transfer with an error condition (FPI_RDY=1 with FPI_ACK=2'b11) in the following cycle. Therefore the FPI_TOUT does not need to be handled by BMU.

Please refer to the FPI specification version V4.2, 2003-11 chapter 6: FPI Bus Termination conditions for a detailed overview.

18.4.3 Bus Transaction Table

The **Figure 18-5 “Bus Transaction Information” on Page 18-12** defines how each phase of a FPI transaction is written into the BTF. The set of information bits related to a write data is written as a 64-bit value into the BTF. A BTF word or entry is made of:

- the write data itself, referred as the BTF[DataPhase] field and
- the BTF[Control] field

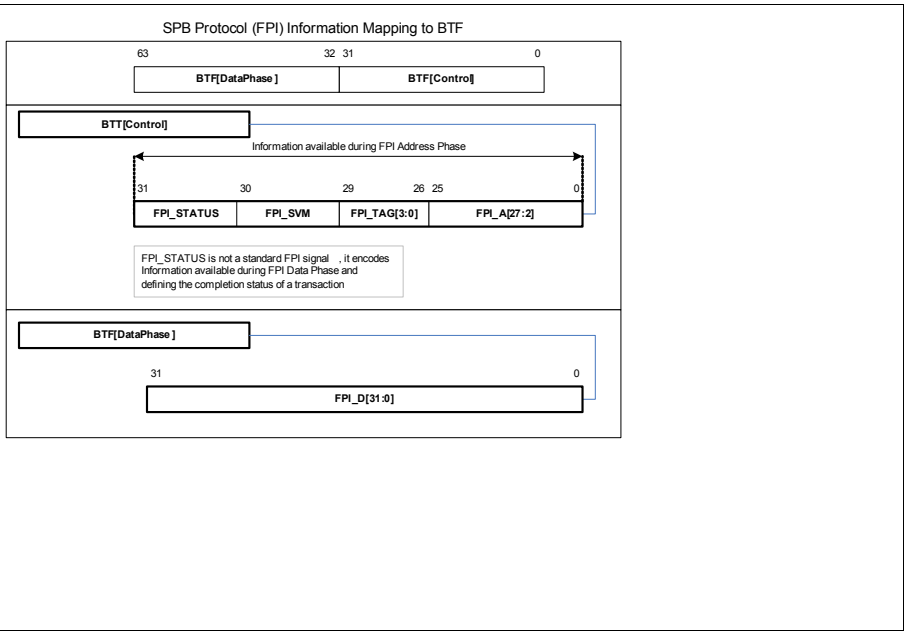


Figure 18-5 Bus Transaction Information

The logging of burst transactions follows the same rules as for single write transactions: the FPI master provides for each data phase the corresponding address information. Examples with single write and burst are given in **Figure 18-6 “Logging information for FPI burst transactions” on Page 18-13**. The address information shown is directly the information present in the FPI bus.

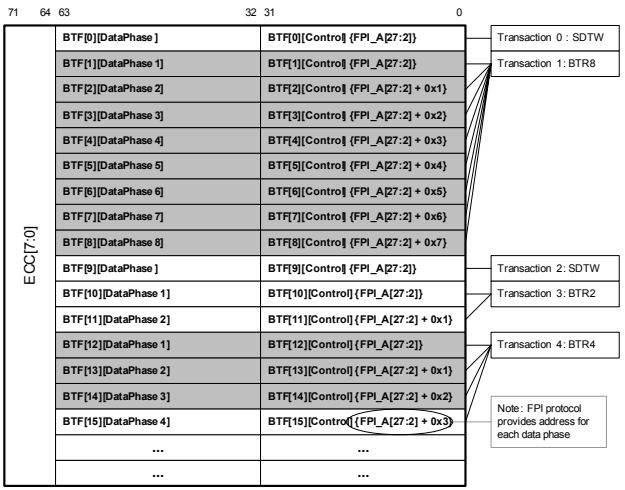


Figure 18-6 Logging information for FPI burst transactions

18.4.4 Write Operation and Fifo Structure

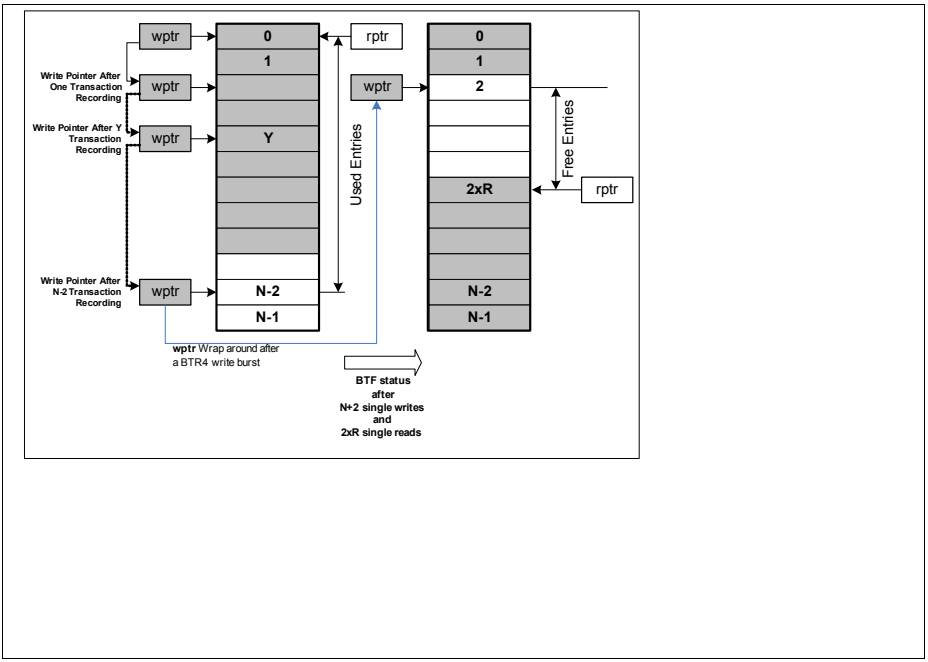


Figure 18-7 BTF Cyclic Buffer Write Pointer Management

The write pointer is controlled by the BMU internal logic. If N is the number of words in the BTF (corresponding a maximum of N single write FPI transactions), when the write pointer reaches the word at position N-1 and a new single write FPI transaction is logged, the new position of the write pointer is 0. If in the meantime no read pointer update took place, the BTF is declared full.

18.4.5 Read Operation and Fifo Structure

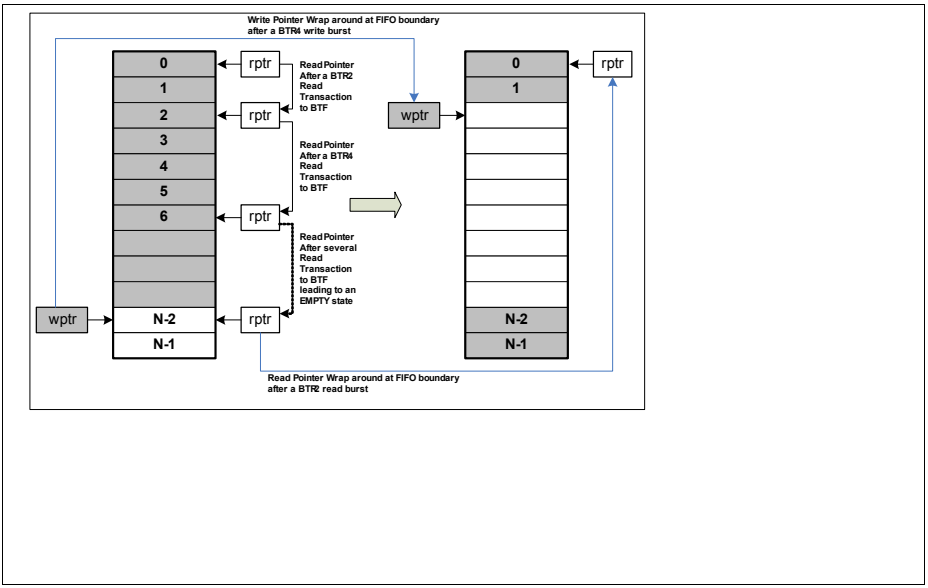


Figure 18-8 BTF Cyclic Buffer Read Pointer Management

The read pointer (**rptr** in Figure 18-7) is also only controlled by hardware. **Depending on the FPI transaction size given by the FPI_OPC[3:0] opcode the read pointer is incremented accordingly**. A BTR2 read burst will increment the read pointer by 2 and so on. The FPI_A[31:0] address information is not used to directly access an entry in the BTF. The FPI_A[31:0] shall point to the base address of the BTF SRAM, otherwise a Bus Error will be returned with the first read data terminating the FPI burst.

Having the read pointer controlled by hardware enables to free the fifo space in a faster way, increasing the logging performance.

18.4.6 Fullness Monitoring

The **Figure 18-9 "BTF Fullness Monitoring" on Page 18-16** shows how the fullness is calculated in order to check if the fullness threshold defined by the register **FMTH** is reached or not. The BufferSize is a constant value defining the number of 64-bit words of the internal SRAM building the Bus Transaction Fifo.

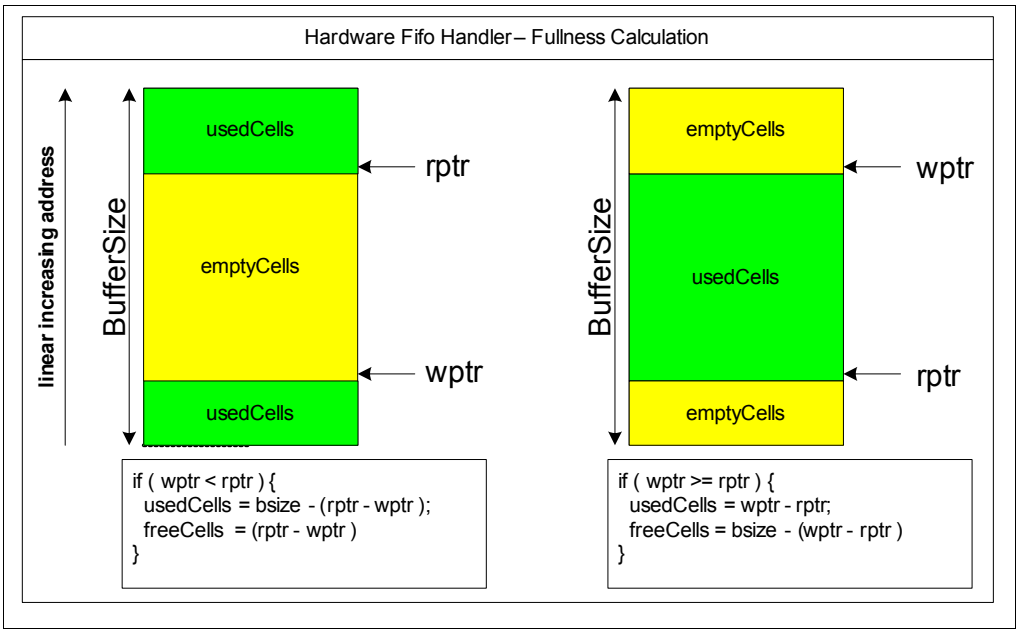


Figure 18-9 BTF Fullness Monitoring

The fullness information is computed dynamically based on the contents of the read and write pointers and the corresponding events (write pulse/read pulse indicators). For convenience the fullness information (see **Figure 18-9 "BTF Fullness Monitoring" on Page 18-16**) is made visible to software via the **FULLNESS** registers. If a write event takes place and the next position of the write pointer is identical to the read pointer and if no read event takes place the BTF is declared **FULL**. If a read event only takes place and the value of the read pointer equals the value of the write pointer the BTF is declared **EMPTY**.

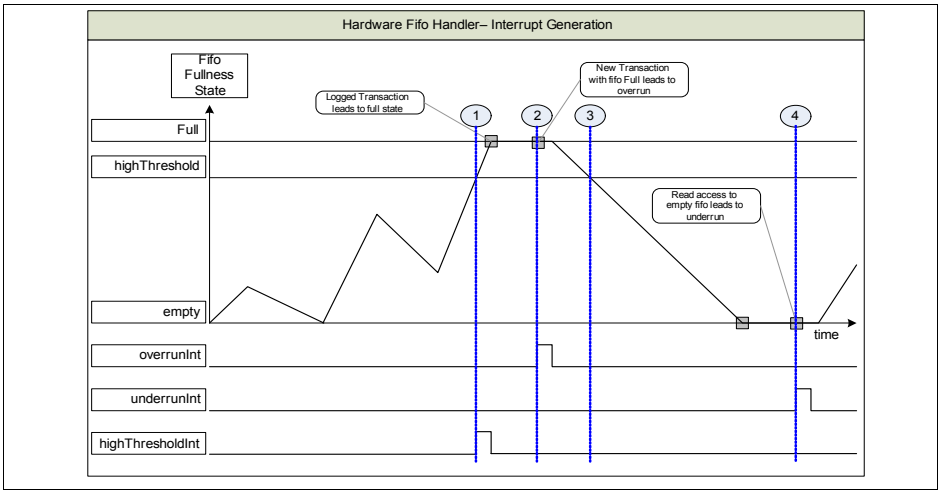


Figure 18-10 BTF Fullness Monitoring - Threshold Interrupts

Figure 18-10 "BTF Fullness Monitoring - Threshold Interrupts" on Page 18-17 shows the fullness conditions that can be reported by the Fifo Monitor:

- [1] The fullness reaches or crosses the High Threshold level as configured in the register **FMTH**. If the corresponding bit is set in the **FMCTL** register an interrupt is triggered to the Interrupt Service Request Node and the corresponding flag is set in the **FMSTS** register. The flag is set regardless of the interrupt generation mode.
- [2] The BTF is full. A new write access is detected leading to an overrun condition. The interrupt reporting is similar to the one described for the case [1]. The write pointer is not incremented and the FPI transaction information is not logged. If the overrun situation occurs during a burst transaction, only the data phases that can do not lead to the overrun condition are logged.
- [3] Reaching again the High Threshold value while the fullness is decreasing does not trigger an interrupt.
- [4] The fifo (BTF) is empty, a read takes place leading to an underrun condition. The interrupt reporting is similar to the one described for the case [1]. The read pointer is not incremented. If the underrun condition occurs during a read burst, a data phase error acknowledge will be issued by the BMU. The software handling the BMU should take care to avoid such conditions. However errors taking place in the system caused by soft errors (single event upsets for instance), may lead to such condition.

18.4.7 Error Correction Code (ECC)

The BMU SRAM is protected by information redundancy based on Error Correction Codes with a Hamming Distance of 4. The ECC information redundancy applies to the data bits of each BMU SRAM word. **CTL**

Limitations with ECC accesses

When the ECC mapping is enabled the memory access limitations described in **"Usage in non safety applications" on Page 18-20** apply as well. Therefore the ECC information can only be accessed using FPI BTR2 bursts as described in **Figure 18-11 "ECC information mapping into FPI BTR2 transactions" on Page 18-18**. The burst base address is 8-byte aligned (FPI_A[2:0] = 3'b000).

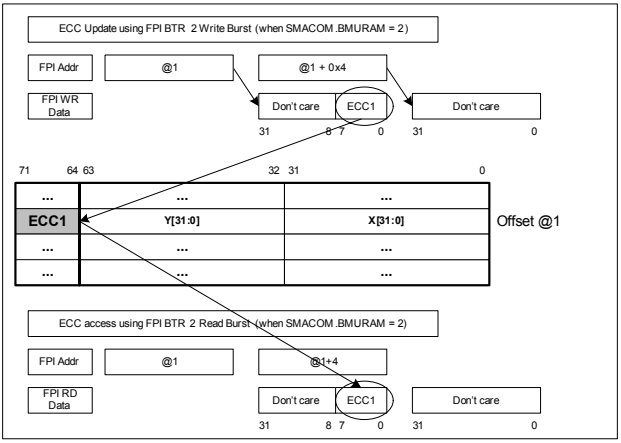


Figure 18-11 ECC information mapping into FPI BTR2 transactions

Memory Integrity Error Control

A pair of architecturally visible registers (MIECON, MIECON2) are included to allow software to control the memory integrity error detection / correction mechanisms. The existence of the MIECON and MIECON2 registers is architecturally defined. However, the fields within these registers are implementation specific. The behavior of MIECON2

is configured according to the “secwen_i” input to the BMU. “secwen_i” is connected to a Product Configuration bit from the SCU, and is locked after execution of Startup Software (SSW). With “secwen_i” not asserted, and the MIECON2 bits previously set by SSW, single-bit correction of memory integrity errors is transparent to software and may not be disabled or detected.

When “secwen_i” is asserted, MIECON2 may only be written in supervisor mode and is ENDINIT protected. MIECON2 reads return the register contents. When “secwen_i” is not asserted accesses to MIECON2 will generate an FPI error acknowledge.

The DED_EN and SEC_EN bits (located **MIECON** and **MIECON2** respectively) and the appropriate SMACON field settings interact to perform the following general function:

Table 18-2 Memory integrity error modes

SEC_EN	DED_EN	SMACON	Description
X	X	01_B or 10_B	**Array Mapping** All single and double-bit memory integrity errors ignored.
0	0	00_B or 11_B	**No Memory Integrity Handling** All single and double-bit memory integrity errors ignored.
0	1	00_B or 11_B	**Error Detection Mode** Single and double-bit errors treated as un-correctable errors. In this mode the BMU_ECC_ERROR_O is asserted every time a single or double bit error is detected.
1	0	00_B or 11_B	**SEC Only Mode** Single-bit errors corrected by ECC, double-bit errors ignored. BMU_ECC_ERROR_O is never asserted in this mode
1	1	00_B or 11_B	**SECDED Mode** Single-bit errors corrected by ECC, double-bit errors treated as un-correctable errors. BMU_ECC_ERROR_O is asserted every time a double bit error is detected.

18.4.8 Usage in non safety applications

When the BMU is not used in a safety application the BTF fifo can be accessed as a standard linear memory through the BMU slave interface using BTR2, BTR4 or BTR8 FPI transactions. This mode of operation is controlled by the **CTL**.MODE field. Single word or sub word (8/16-bit) accesses are not allowed; such requests will result in a Bus Error. **The start address of the FPI burst transactions is aligned with the size of the burst.**

Table 18-3 SRAM address map

Module	Base address	End address	Note
Bus Monitoring Unit	$F032\ 4000_H$	$F032\ 5FFF_H$	BMURAM

Figure 18-12 "Mapping between FPI Burst transaction and SRAM contents" on Page 18-20 shows how the FPI bus 32-bit data phases are mapped into the 64-bit word of the BMU SRAM. An example with read and write bursts is given.

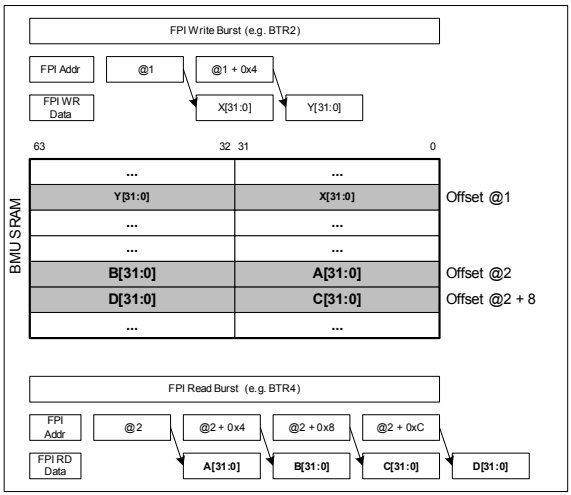


Figure 18-12 Mapping between FPI Burst transaction and SRAM contents

18.4.9 BMU interrupts

Interrupt generation rules

- Each interrupt source has a dedicated status bit that indicates if an interrupt has been issued or not.
- A status flag shall be cleared by software by writing a 1 to the corresponding bit position.
- If a status flag is set and a new hardware condition leading to an interrupt occurs, no new interrupt is generated. **If a software access to clear the interrupt status bit takes place and in the same cycle the hardware wants to set the bit, the hardware condition wins the arbitration**.

18.4.10 Peripheral Monitoring Selection

The **Table 18-4** shows the list of peripherals present in the TC1798 device together with an identifier. The FPI bus infrastructure provides address decoders that are configured to generate chip select signals. The chip select signals are connected to the standard BPI modules or to the FPI Slave Interfaces or directly to custom FPI interfaces (some FPI peripherals have neither a BPI nor a FPI slave interface). Each select line identifies a FPI region that corresponds to the FPI regions defined in the **PSET0** and **PSET1** registers. Behind a decoded FPI region there may be multiple peripherals. This situation is reflected in **Table 18-4**. Peripherals that belong to the DMA subsystem (FPI extension) will all use the DMA identifier. Only the FPI write transactions enabled by **PSET0** and **PSET1** will be stored in the BMU.

Table 18-4 Identification of FPI Regions

Unit	FPI Region Identifier
System Peripheral Bus Control Unit (SBCU)	0
System Timer (STM)	1
System Control Unit (SCU) and Watchdog Timer (WDT)	2
MicroSecond Bus Controller 0 (MSC0)	3
MicroSecond Bus Controller 1 (MSC1)	4
Async./Sync. Serial Interface 0 (ASC0)	5
Async./Sync. Serial Interface 1 (ASC1)	5
Port Group 0	6
Port Group 1	7
Port Group 2	8
Port Group 3	9
General Purpose Timer Array (GPTA0)	10
General Purpose Timer Array (GPTA1)	10
Local Timer Cell Array (LTCA2)	10
Capture/Compare Unit 6 0 (CCU60)	11
Capture/Compare Unit 6 1 (CCU61)	11
Capture/Compare Unit 6 2 (CCU62)	12
Capture/Compare Unit 6 3 (CCU63)	12
General Purpose Timer 12 0 (GPT120)	13
General Purpose Timer 12 1 (GPT121)	14

Table 18-4 Identification of FPI Regions

Unit		FPI Region Identifier
Safety Direct Memory Access Controller (SDMA)		15
Direct Memory Access Controller (DMA)		16
On-Chip Debug Support (Cerberus)		17 Belongs to DMA region 2
Micro Link Interface 0 (MLI0)		17 Belongs to DMA region 2
Micro Link Interface 1 (MLI1)		17 Belongs to DMA region 2
Memory Checker (MCHK)		17 Belongs to DMA region 2
MLI0 Small Transfer Windows		17 Belongs to DMA region 2
MLI1 Small Transfer Windows		17 Belongs to DMA region 2
MLI0 Large Transfer Windows		17 Belongs to DMA region 2
MLI1 Large Transfer Windows		17 Belongs to DMA region 2
MultiCAN Controller (CAN)		18
FlexRay™ Protocol Controller (E-Ray)		19
PCP	PCP Registers	20
	PCP Data Memory (PRAM)	20
	PCP Code Memory (PCODE)	20
Fast Analog-to-Digital Converter (FADC)		21
Analog-to-Digital Converter 0 (ADC0)		22
Analog-to-Digital Converter 1 (ADC1)		22
Analog-to-Digital Converter 2 (ADC2)		22
Analog-to-Digital Converter 3 (ADC3)		22
Synchronous Serial Interface 0 (SSC0)		23
Synchronous Serial Interface 1 (SSC1)		24
Synchronous Serial Interface 2 (SSC2)		25

Table 18-4 Identification of FPI Regions

Unit	FPI Region Identifier
Synchronous Serial Interface 3 (SSC3)	26
Guardian for SSC0 (SSCG0)	27
Guardian for SSC1 (SSCG1)	28
Guardian for SSC2 (SSCG2)	29
Guardian for SSC3 (SSCG3)	30
Flexible CRC Engine (FCE)	31
Secure Hardware Extension (SHE)	**Not Logged**
SENT Module (SENT)	32
Peripheral Bus Monitor Registers (BMU)	33
Peripheral Bus Monitor Memory (BMURAM)	**Not Logged**

18.5 Interfaces of the BMU Module

This section only describes the signals that do not belong to the system-on-chip standard interfaces (Interrupt Bus, FPI Bus).

Table 18-5 Generic BMU Digital Connections[1)]

Signal	from/to Module	I/O to BMU	Reset Value
EINIT	SCU (System Control Unit)	I	
FPI_CLK_EN	SCU (System Control Unit)	I	
OCDS_P_SUSPEND	On Chip Debug	I	
SLEEP_N	SCU (System Control Unit)	I	
SECWEN	SCU (System Control Unit) Connects to SCU PRDCFG2.SENAV Single Error Correction Availability Control	I	
BMU_ECC_ERROR	SCU (System Control Unit) un-correctable ECC error detected output	O	0
BMU_SPB_SEL[63:0]	System Peripheral Bus (SPB) Address Decoders	I	
BMU_SPB_ACK[1:0]	Global FPI_ACK[1:0] generated by the FPI bus	I	

1) The postfix indicating the direction of the signal is not part of the signal name specification as it depends on the naming conventions used by the development flow. The I/O column indicated the direction of the signal. When the signal is specific to the BMU module it gets “BMU_” as prefix.

Notes

- FPI_CLK_EN is the FPI clock signal.
- OCDS_P_SUSPEND: the suspend feature is not supported by BMU. The OCDS_P_SUSPEND signal is not used.
- SLEEP_N is used to control the sleep mode. The sleep mode function is not supported by BMU, the SLEEP_N signal is not used.
- The FPI_ACK[1:0] signals from the FPI bus are ored together and sent to all masters (only the granted master interprets the FPI_ACK[1:0] contents). The BMU will see the global FPI_ACK[1:0] signal and not directly the individual FPI_ACK corresponding to a FPI region.
- The width of the BMU_SPB_SEL signal is set to 64 bits to make it independent from the peripheral configuration. The non-used upper bits of BMU_SPB_SEL must be set to the logic value LOW. The order of the select lines is given by **Table 18-4 “Identification of FPI Regions” on Page 18-22**.

- The BMU_ECC_ERROR is an active HIGH signal that delivers a pulse of one FPI clock cycle duration. See **Table 18-2 “Memory integrity error modes” on Page 18-19** for the un-correctable modes.
- In TC1798 microcontroller there are 47 BMU_SPB_SEL signals connected to the BMU.

18.6 BMU Module Registers

Figure 18-13 shows the BMU module register map.

Table 18-6 shows the BMU Address Space

Table 18-7 lists all registers implemented in the BMU.

BMU Address Map Overview

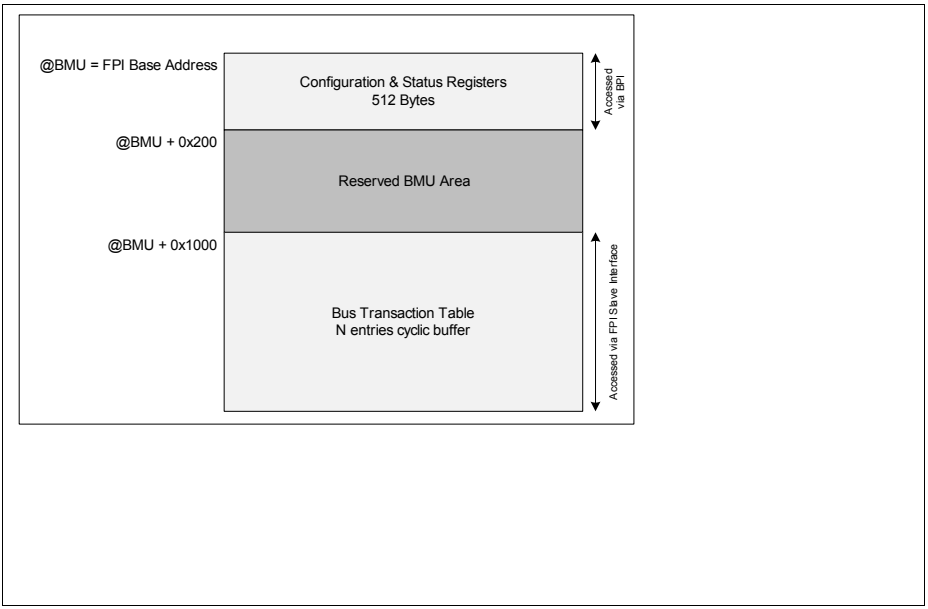


Figure 18-13 BMU Register Map

In TC1798 device the Bus Transaction Table is made of 1024 entries, where each entry is made of 64-bits. **Table 18-6** shows the base address of the addressable SRAM space when the access mode defined by the **CTL**.MODE configuration register is set to 0.

Table 18-6 Registers Address Space for TC1798

Module	Base Address	End Address	Note
BMU	$F032\ 3000_H$	$F032\ 31FF_H$	Registers

Table 18-7 Registers Overview

Short Name	Description	Offset Addr	Access Mode		Reset Class	Description See
			Read	Write		
System Registers						
CLC	Clock Control Register	00_H	U, SV	SV, **E**	3	**Page 18-30**
ID	Module Identifier	08_H	U, SV	BE	3	**Page 18-32**
Global Control over Read access to Bus Transaction Table						
CTL	Transaction Filtering Control Register	20_H	U, SV	SV, **E**	3	**Page 18-33**
PTR	BTF running pointers	24_H	U, SV	BE	3	**Page 18-34**
FULLNESS	Fifo Fullness	28_H	U, SV	BE	3	**Page 18-35**
Bus Logging Configuration Registers						
PSET0	Peripheral Set 0	30_H	U, SV	SV, **E**	3	**Page 18-36**
PSET1	Peripheral Set 1	34_H	U, SV	SV, **E**	3	**Page 18-39**
TID	Transaction ID Set 0	38_H	U, SV	SV, **E**	3	**Page 18-42**
Fifo Monitoring Configuration and Status Registers						
FMCTL	Control Register	40_H	U, SV	SV, **E**	3	**Page 18-43**
FMSTS	Status Register	44_H	U, SV	U,SV	3	**Page 18-43**
FMTH	High Threshold Value	48_H	U, SV	SV, **E**	3	**Page 18-44**
Control of ECC operation						
SMACON	Control of SIST Mode	50_H	U, SV	SV,**E**	3	**Page 18-46**
MIECON	ECC modes control	54_H	U, SV	SV,**E**	3	**Page 18-47**
MIECON2	ECC modes control	58_H	U, SV	SV,**E**	3	**Page 18-47**
Interrupt System Registers						
SRC	Service Request Control	FC_H	U, SV	SV	3	**Page 18-49**

Access Mode Rules

The **Table 18-7 “Registers Overview” on Page 18-28** uses the standard access mode conventions.

- **E** indicates that an access is only possible if the **end of initialization** signal from the System Control Unit is active. In this case Supervisor Mode (SV) is also mandatory.
- When U, SV are both listed it means that a read or write access can be done either in user mode (U) or supervisor mode (V).

- BE stands for Bus Error, NSC stands for No Special Condition

*Note: Configuration registers that determine the behavior of the BMU are protected by the end of init protection mechanism. They are intended to be only configured once during the initial system startup phase. In safety-related applications the configuration is controlled by the Safety Driver. Registers that need to be updated by the application (run-time interaction) are only protected by supervisor mode: applies to **FMSTS**.*

Register access constraints

The registers that control the operation of the BMU are assumed to be static, they are configured by the safety driver according to the requirements of the safety application(s) during the initial microcontroller configuration. Exceptions will be documented in each register sub-chapter. As indication the list of registers that are assumed to be static are:

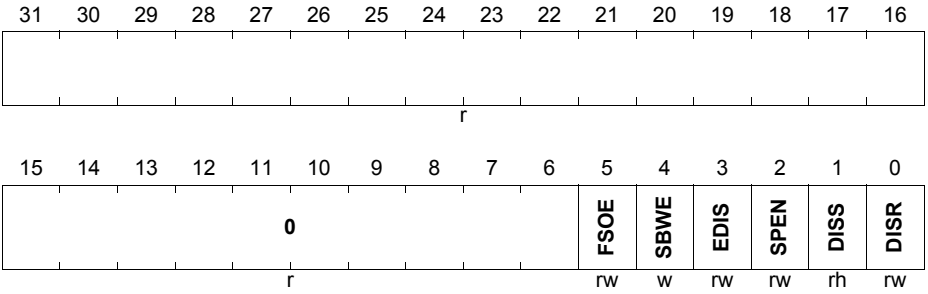
- **PSET0**, **PSET1**, **TID**[1)], **FMCTL**, **FMTH**
- **CTL** is only allowed to be change if SIST mode is used during run-time for ECC checks. The necessity to do ECC checks during run-time will depend on the safety monitoring concept.

1) Currently **TID** is a read-only register, this may change in future enhancements of the BMU.

18.6.1 System Registers description

BMU Module Clock Control Register.

CLC
Control Clock Register **(00_H)** **Reset Value: $0000\ 0000_H$**



Field	Bits	Type	Description
DISR	0	rw	**Module Disable Bit Request** Used for enable/disable control of the module 0_B Module disable is not requested 1_B Module disable is requested
DISS	1	rh	**Module Disable Bit Status** Bit indicates the current status of the module 0_B Module is enabled 1_B Module is disabled
0	[31:2]	r	**Reserved** Read as 0; write has no effect.

Note: The BMU does not implement a fractional divider.

Note: Sleep and Suspend modes are not supported by BMU, therefore the bit fields controlling those features are not present in the CLC register.

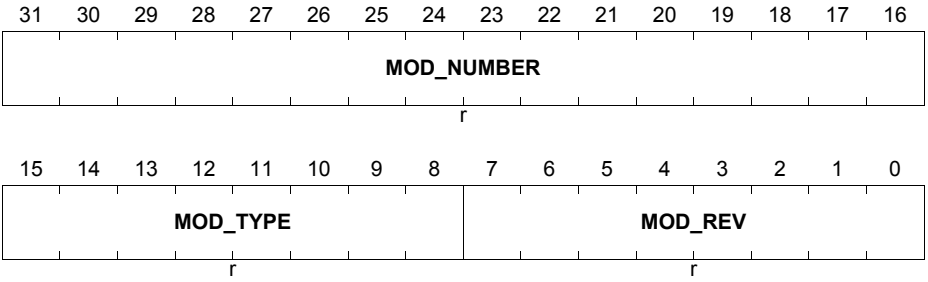
Note: The BMU can be disabled. When the disable state is requested all pending transactions running on the FPI slave interface must be completed before the disabled state is entered. The CLC Register Module Disable Bit Status BMU_CLC.DISS indicates whether the module is currently disabled (DISS == 1). Any attempt to write any of the BPI writable registers with the exception of the CLC Register will generate a bus error. A read operation of BPI registers is allowed and does not generate a bus error. As long as the BMU is disabled no logging is possible (including the write access to the BMU_CLC register to enable again the

BMU). Logging is possible after software writes 0 to DISR and the DISS field value indicates the enabled state.

BMU Module Identification Register.

ID

Module Identification Register **(08_H)** **Reset Value: $0089\ C001_H$**

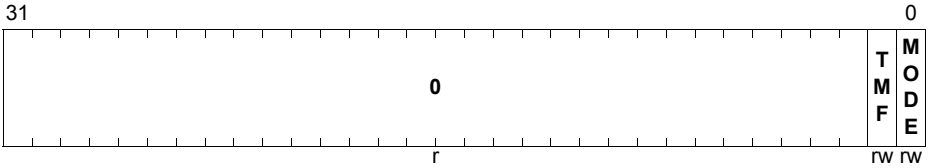


Field	Bits	Type	Description
MOD_REV	[7:0]	r	**Module Revision Number** This bit field defines the module revision number. The value of a module revision starts with 01_H (first revision).
MOD_TYPE	[15:8]	r	**Module Type** The bit field is set to $C0_H$ which defines the module as a 32-bit module.
MOD_NUMBER	[31:16]	r	**Module Number Value** This bit field defines a module identification number. The value for the BMU module is 0089_H.

18.6.2 BMU Control/Status Registers

CTL
Transaction Filtering Control

(20_H) **Reset Value: $0000\ 0000_H$**



Field	Bits	Type	Description
MODE	0	rw	**Access Mode** 0_B The BTF is accessed in linear mode as a standard memory mapped SRAM 1_B The BTF is used in FIFO Mode enabling to log the write transaction to the regions selected in **PSET0** and **PSET1** registers.
TMF	1	rw	**Transaction Master Filtering** In FIFO mode, this field enables an additional logging mechanism controlled by the master identifier of a FPI write transaction. 0_B Logging controlled by the transaction master identifier disabled. 1_B Logging controlled by the transaction master identifier Enabled.
0	[31:2]	r	reserved bit fields. A write has no effect. Returns 0s on read.

CTL defines the access mode to the internal SRAM and enables to control additional logging mechanisms based on the initiator of the transaction. The operation mode is statically defined for the whole run-time, changes of operating mode are to be avoided.

In the event the BMU is configured in FIFO mode (CTL.MODE = 1) then the CTL register should be polled to confirm the FIFO mode is set before any write transaction on the FPI bus is logged.

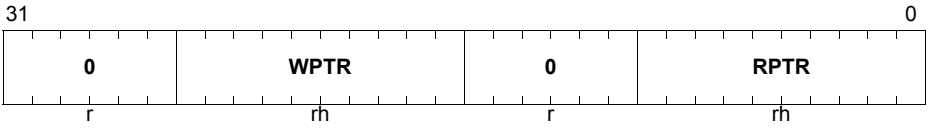
However when the BMU is configured in FIFO mode, it may be necessary to switch to SRAM mode if run time diagnostics of the ECC logic is required. It must be ensured at system level that during the time the diagnostics will be performed, the safety application

will not be able to use the logging capability of the BMU. If the BMU is intended to be used in SRAM mode only, it is not allowed to switch during run-time to FIFO mode.

In the FPI bus protocol the initiator (also called the master) is uniquely identified by the FPI Transaction Identifier made of 4-bits. When the MODE field and TMF field are both set to 1, the BMU monitors the master identifier of every FPI write transaction. When the master identifier matches with the value(s) present in the **TID** register, the address information of every address phase of the transaction is logged into the BMU FIFO. The logging based on the master identifier monitoring has precedence over the logging based on the FPI region monitoring.

PTR
Pointer Information for Bus Transaction Fifo

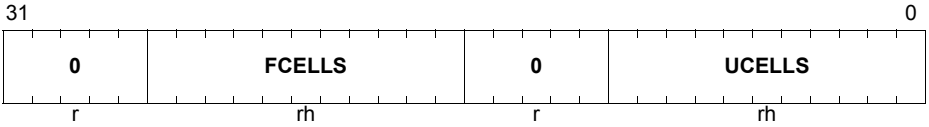
(24_H) **Reset Value: 0000 0000_H**



Field	Bits	Type	Description
RPTR	[9:0]	rh	**Read Pointer for a 1024 entry SRAM** Indicates the current position of the read pointer. A write to this field has no hardware effect. For debug purposes only.
WPTR	[25:16]	rh	**Write Pointer for a 1024 entry SRAM** Indicates the current position of the write pointer. A write to this field has no hardware effect. For debug purposes only.
0	[15:10], [31:26]	r	**reserved bit fields. A write has no effect. Returns 0s on read.**

PTR is to be used for debug or verification purposes.

FULLNESS
Fullness Information for Bus Transaction Fifo (28_H) **Reset Value: $0400\ 0000_H$**



Field	Bits	Type	Description
UCELLS	[10:0]	rh	**Number of valid (used) entries in the BTF** Fullness of the BTF as a number of words. UCELLS value ranges from 0 to N, where N is the number of fifo entries. UCELLS = N represents a full fifo. For TC1798 microcontroller, N = 1024. Writing to this field has no effect.
FCELLS	[26:16]	rh	**Number of free entries in the BTF** Writing to this field has no effect. FCELLS value ranges from 0 to N, where N is the number of fifo entries. FCELLS = N represents an empty fifo. For TC1798 microcontroller, N = 1024. Writing to this field has no effect.
0	[31:27], [15:11]	r	reserved bit fields. A write has no effect. Returns 0s on read.

The **UCELLS** and **FCELLS** information can be used to schedule the number of consecutive burst reads that can be made to read the available information from the BTF.

18.6.3 BMU: Bus Logging Configuration Registers

PSET0
Peripheral Set 0 Configuration

(30_H) **Reset Value: $0000\ 0000_H$**

31																													0
FPI_SEL31	FPI_SEL30	FPI_SEL29	FPI_SEL28	FPI_SEL27	FPI_SEL26	FPI_SEL25	FPI_SEL24	FPI_SEL23	FPI_SEL22	FPI_SEL21	FPI_SEL20	FPI_SEL19	FPI_SEL18	FPI_SEL17	FPI_SEL16	FPI_SEL15	FPI_SEL14	FPI_SEL13	FPI_SEL12	FPI_SEL11	FPI_SEL10	FPI_SEL9	FPI_SEL8	FPI_SEL7	FPI_SEL6	FPI_SEL5	FPI_SEL4	FPI_SEL3	FPI_SEL2	FPI_SEL1	FPI_SEL0
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
FPI_SEL0	0	rw	**Select Bit for FPI Region 0** 0_B Region Disabled 1_B Region Enabled
FPI_SEL1	1	rw	**Select Bit for FPI Region 1** 0_B Region Disabled 1_B Region Enabled
FPI_SEL2	2	rw	**Select Bit for FPI Region 2** 0_B Region Disabled 1_B Region Enabled
FPI_SEL3	3	rw	**Select Bit for FPI Region 3** 0_B Region Disabled 1_B Region Enabled
FPI_SEL4	4	rw	**Select Bit for FPI Region 4** 0_B Region Disabled 1_B Region Enabled
FPI_SEL5	5	rw	**Select Bit for FPI Region 5** 0_B Region Disabled 1_B Region Enabled
FPI_SEL6	6	rw	**Select Bit for FPI Region 6** 0_B Region Disabled 1_B Region Enabled
FPI_SEL7	7	rw	**Select Bit for FPI Region 7** 0_B Region Disabled 1_B Region Enabled

Field	Bits	Type	Description
FPI_SEL8	8	rw	**Select Bit for FPI Region 8** 0_B Region Disabled 1_B Region Enabled
FPI_SEL9	9	rw	**Select Bit for FPI Region 9** 0_B Region Disabled 1_B Region Enabled
FPI_SEL10	10	rw	**Select Bit for FPI Region 10** 0_B Region Disabled 1_B Region Enabled
FPI_SEL11	11	rw	**Select Bit for FPI Region 11** 0_B Region Disabled 1_B Region Enabled
FPI_SEL12	12	rw	**Select Bit for FPI Region 12** 0_B Region Disabled 1_B Region Enabled
FPI_SEL13	13	rw	**Select Bit for FPI Region 13** 0_B Region Disabled 1_B Region Enabled
FPI_SEL14	14	rw	**Select Bit for FPI Region 14** 0_B Region Disabled 1_B Region Enabled
FPI_SEL15	15	rw	**Select Bit for FPI Region 15** 0_B Region Disabled 1_B Region Enabled
FPI_SEL16	16	rw	**Select Bit for FPI Region 16** 0_B Region Disabled 1_B Region Enabled
FPI_SEL17	17	rw	**Select Bit for FPI Region 17** 0_B Region Disabled 1_B Region Enabled
FPI_SEL18	18	rw	**Select Bit for FPI Region 18** 0_B Region Disabled 1_B Region Enabled
FPI_SEL19	19	rw	**Select Bit for FPI Region 19** 0_B Region Disabled 1_B Region Enabled

Field	Bits	Type	Description
FPI_SEL20	20	rw	**Select Bit for FPI Region 20** 0_B Region Disabled 1_B Region Enabled
FPI_SEL21	21	rw	**Select Bit for FPI Region 21** 0_B Region Disabled 1_B Region Enabled
FPI_SEL22	22	rw	**Select Bit for FPI Region 22** 0_B Region Disabled 1_B Region Enabled
FPI_SEL23	23	rw	**Select Bit for FPI Region 23** 0_B Region Disabled 1_B Region Enabled
FPI_SEL24	24	rw	**Select Bit for FPI Region 24** 0_B Region Disabled 1_B Region Enabled
FPI_SEL25	25	rw	**Select Bit for FPI Region 25** 0_B Region Disabled 1_B Region Enabled
FPI_SEL26	26	rw	**Select Bit for FPI Region 26** 0_B Region Disabled 1_B Region Enabled
FPI_SEL27	27	rw	**Select Bit for FPI Region 27** 0_B Region Disabled 1_B Region Enabled
FPI_SEL28	28	rw	**Select Bit for FPI Region 28** 0_B Region Disabled 1_B Region Enabled
FPI_SEL29	29	rw	**Select Bit for FPI Region 29** 0_B Region Disabled 1_B Region Enabled
FPI_SEL30	30	rw	**Select Bit for FPI Region 30** 0_B Region Disabled 1_B Region Enabled
FPI_SEL31	31	rw	**Select Bit for FPI Region 31** 0_B Region Disabled 1_B Region Enabled

PSET1
Peripheral Set 1 Configuration

(34_H) **Reset Value: $0000\ 0000_H$**

31																															0
FPI_SEL63	FPI_SEL62	FPI_SEL61	FPI_SEL60	FPI_SEL59	FPI_SEL58	FPI_SEL57	FPI_SEL56	FPI_SEL55	FPI_SEL54	FPI_SEL53	FPI_SEL52	FPI_SEL51	FPI_SEL50	FPI_SEL49	FPI_SEL48	FPI_SEL47	FPI_SEL46	FPI_SEL45	FPI_SEL44	FPI_SEL43	FPI_SEL42	FPI_SEL41	FPI_SEL40	FPI_SEL39	FPI_SEL38	FPI_SEL37	FPI_SEL36	FPI_SEL35	FPI_SEL34	FPI_SEL33	FPI_SEL32
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
FPI_SEL32	0	rw	**Select Bit for FPI Region 32** 0_B Region Disabled 1_B Region Enabled
FPI_SEL33	1	rw	**Select Bit for FPI Region 33** 0_B Region Disabled 1_B Region Enabled
FPI_SEL34	2	rw	**Select Bit for FPI Region 34** 0_B Region Disabled 1_B Region Enabled
FPI_SEL35	3	rw	**Select Bit for FPI Region 35** 0_B Region Disabled 1_B Region Enabled
FPI_SEL36	4	rw	**Select Bit for FPI Region 36** 0_B Region Disabled 1_B Region Enabled
FPI_SEL37	5	rw	**Select Bit for FPI Region 37** 0_B Region Disabled 1_B Region Enabled
FPI_SEL38	6	rw	**Select Bit for FPI Region 38** 0_B Region Disabled 1_B Region Enabled
FPI_SEL39	7	rw	**Select Bit for FPI Region 39** 0_B Region Disabled 1_B Region Enabled

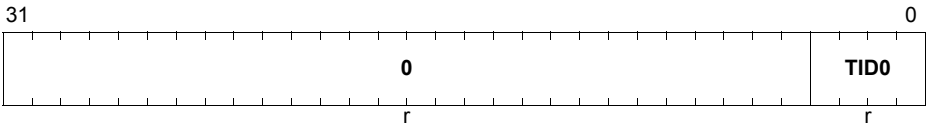
Field	Bits	Type	Description
FPI_SEL40	8	rw	**Select Bit for FPI Region 40** 0_B Region Disabled 1_B Region Enabled
FPI_SEL41	9	rw	**Select Bit for FPI Region 41** 0_B Region Disabled 1_B Region Enabled
FPI_SEL42	10	rw	**Select Bit for FPI Region 42** 0_B Region Disabled 1_B Region Enabled
FPI_SEL43	11	rw	**Select Bit for FPI Region 43** 0_B Region Disabled 1_B Region Enabled
FPI_SEL44	12	rw	**Select Bit for FPI Region 44** 0_B Region Disabled 1_B Region Enabled
FPI_SEL45	13	rw	**Select Bit for FPI Region 45** 0_B Region Disabled 1_B Region Enabled
FPI_SEL46	14	rw	**Select Bit for FPI Region 46** 0_B Region Disabled 1_B Region Enabled
FPI_SEL47	15	rw	**Select Bit for FPI Region 47** 0_B Region Disabled 1_B Region Enabled
FPI_SEL48	16	rw	**Select Bit for FPI Region 48** 0_B Region Disabled 1_B Region Enabled
FPI_SEL49	17	rw	**Select Bit for FPI Region 49** 0_B Region Disabled 1_B Region Enabled
FPI_SEL50	18	rw	**Select Bit for FPI Region 50** 0_B Region Disabled 1_B Region Enabled
FPI_SEL51	19	rw	**Select Bit for FPI Region 51** 0_B Region Disabled 1_B Region Enabled

Field	Bits	Type	Description
FPI_SEL52	20	rw	**Select Bit for FPI Region 52** 0_B Region Disabled 1_B Region Enabled
FPI_SEL53	21	rw	**Select Bit for FPI Region 53** 0_B Region Disabled 1_B Region Enabled
FPI_SEL54	22	rw	**Select Bit for FPI Region 54** 0_B Region Disabled 1_B Region Enabled
FPI_SEL55	23	rw	**Select Bit for FPI Region 55** 0_B Region Disabled 1_B Region Enabled
FPI_SEL56	24	rw	**Select Bit for FPI Region 56** 0_B Region Disabled 1_B Region Enabled
FPI_SEL57	25	rw	**Select Bit for FPI Region 57** 0_B Region Disabled 1_B Region Enabled
FPI_SEL58	26	rw	**Select Bit for FPI Region 58** 0_B Region Disabled 1_B Region Enabled
FPI_SEL59	27	rw	**Select Bit for FPI Region 59** 0_B Region Disabled 1_B Region Enabled
FPI_SEL60	28	rw	**Select Bit for FPI Region 60** 0_B Region Disabled 1_B Region Enabled
FPI_SEL61	29	rw	**Select Bit for FPI Region 61** 0_B Region Disabled 1_B Region Enabled
FPI_SEL62	30	rw	**Select Bit for FPI Region 62** 0_B Region Disabled 1_B Region Enabled
FPI_SEL63	31	rw	**Select Bit for FPI Region 63** 0_B Region Disabled 1_B Region Enabled

PSET0 and **PSET1** are used to control which FPI region is to be monitored by the BMU.

TID
FPI Transaction ID Set 0 Configuration

(38_H) **Reset Value: 0000 000D$_H$**



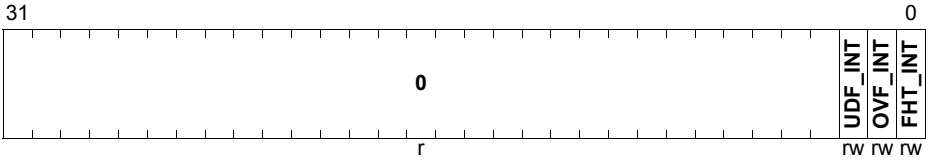
Field	Bits	Type	Description
TID0	[3:0]	r	**Transaction Identifier 0** This field is statically encoded with the 4'b1101 value that corresponds to the SHE FPI master identifier in the TC1798 device.
0	[31:4]	r	reserved bit fields. A write has no effect. Returns 0s on read.

The Transaction Identifier **TID** enables to perform monitoring actions based on the master identifier provided by the FPI master. This mode can be further extended (in future versions of the BMU) to do broader checks based on the TID: for instance in a multi-processor system, the TID can uniquely identity the CPU core that initiated the transaction. The current implementation only allows to do a static detection of write accesses initiated by the SHE module when present in the product.

18.6.4 BMU: Fifo Monitoring Registers

FMCTL
Fifo Monitor control register

(40_H) **Reset Value: 0000 0000$_H$**

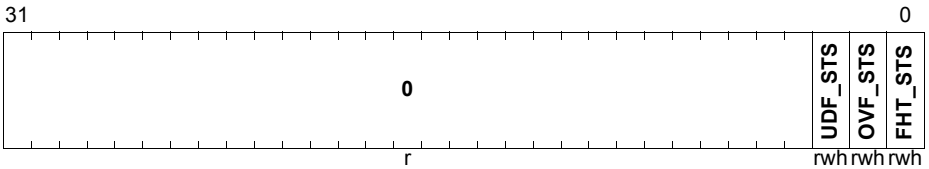


Field	Bits	Type	Description
FHT_INT	0	rw	**Interrupt Enable for Fifo High Threshold** 0_B interrupt generation disabled 1_B interrupt generation enabled
OVF_INT	1	rw	**Interrupt Enable for Overflow Detection** 0_B interrupt generation disabled 1_B interrupt generation enabled
UDF_INT	2	rw	**Interrupt Enable for Underflow Detection** 0_B interrupt generation disabled 1_B interrupt generation enabled
0	[31:3]	r	reserved bit fields. A write has no effect. Returns 0s on read.

FMCTL controls the interrupt generation related to the Fifo Fullness Monitoring.

FMSTS
Fifo Monitor Status Register

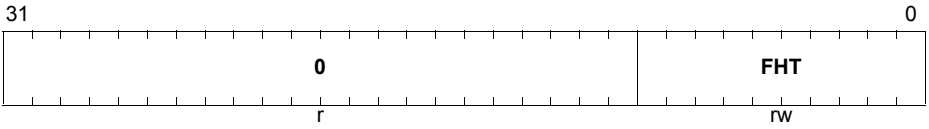
(44_H) **Reset Value: 0000 0000$_H$**



Field	Bits	Type	Description
FHT_STS	0	rwh	**Status Flag for Fifo High Threshold interrupt** 0_B No interrupt pending 1_B Event related to High Threshold monitoring has been detected. The event leads to an interrupt if FMCTL.FHT_INT = 1.
OVF_STS	1	rwh	**Status Flag for Overrun interrupt** 0_B No interrupt pending 1_B Event related to overflow monitoring has been detected. The event leads to an interrupt if FMCTL.OVF_INT = 1.
UDF_STS	2	rwh	**Status Flag for Underflow interrupt** 0_B No interrupt pending 1_B Event related to underflow monitoring has been detected. The event leads to an interrupt if FMCTL.UDF_INT = 1.
0	[31:3]	r	reserved bit fields. A write has no effect. Returns 0s on read.

FMSTS is used to log the status of the interrupt source(s). The bits are set to 1 by hardware. To clear a status bit the software must write a 0 at the bit position corresponding to be bit to be cleared (writing a 1 per software has no effect on the status bits). If software writes a 0 to a status bit that is already cleared and in the same cycle the hardware wants to set the bit, the hardware has priority over the software.

FMTH
Fifo Monitor: Fullness Threshold Register
(48_H) **Reset Value: 0000 0000_H**



Field	Bits	Type	Description
FHT	[9:0]	rw	**Fifo High Threshold** This field defines a number of used entries defining a threshold. When set to 0 the threshold monitoring is disabled.
0	[31:10]	r	reserved bit fields. A write has no effect. Returns 0s on read.

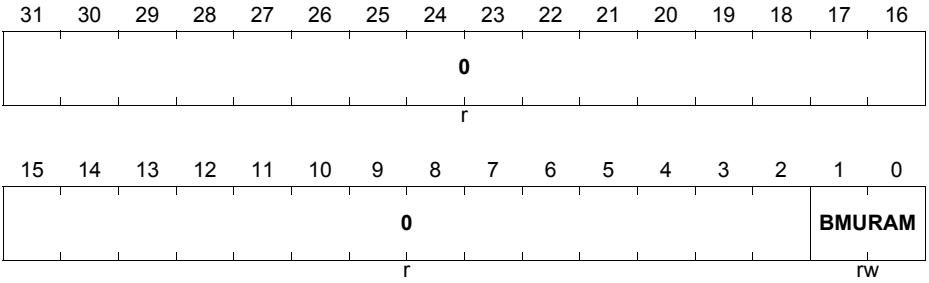
FMTH defines a boundary for the number of used words in the Bus Transaction Fifo that will be monitored during run-time. When the number of words configured in the **FHT** field is reached (or crossed) and if the **FMCTL**.**FHT_INT** field is set, an interrupt is triggered. This FHT field must be initialized by SW to the expected threshold before enabling the interrupt generation.

18.6.5 BMU: SIST Mode Access Control Register

*Note: Please see **"Error Correction Code (ECC)" on Page 18-18** for more information regarding the use of this register.*

This register is ENDINIT protected.

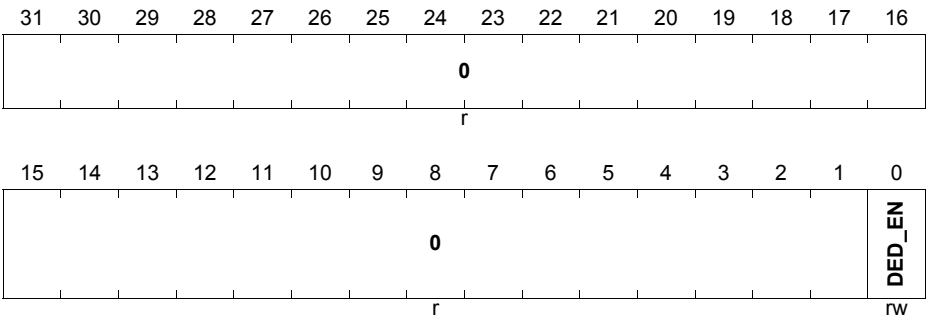
SMACON
SIST Mode Access Control Register (50$_H$) **Reset Value: 0000 0000$_H$**



Field	Bits	Type	Description
BMURAM	[1:0]	rw	**SIST mode access control** 00_B Normal Operation, No Mapping 01_B Data Array Mapping, no error detection/correction 10_B Check Array Mapping, no error detection/correction 11_B Data Array Mapping, error detection/correction enabled
0	[31:2]	r	**reserved** returns '0' if read; should be written with '0'.

MIECON

Memory Integrity Error Control Register(54_H) **Reset Value: 0000 0000$_H$**

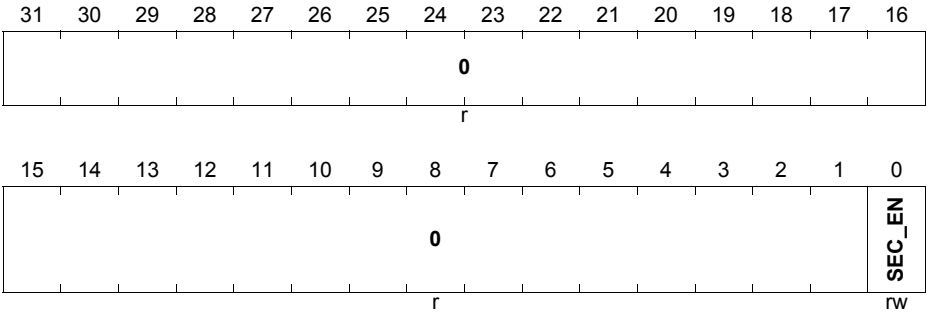


Field	Bits	Type	Description
DED_EN	0	rw	**Double error detection enable** 0_B Double bit error detection for BMURAM disabled 1_B Double bit error detection for BMURAM enabled
0	[31:1]	r	**reserved** returns ‘0’ if read; should be written with ‘0’.

Please see **“Error Correction Code (ECC)” on Page 18-18** for more information regarding the use of this register.

MIECON2

Memory Integrity Error Control 2 Register(58_H) **Reset Value: 0000 0000$_H$**



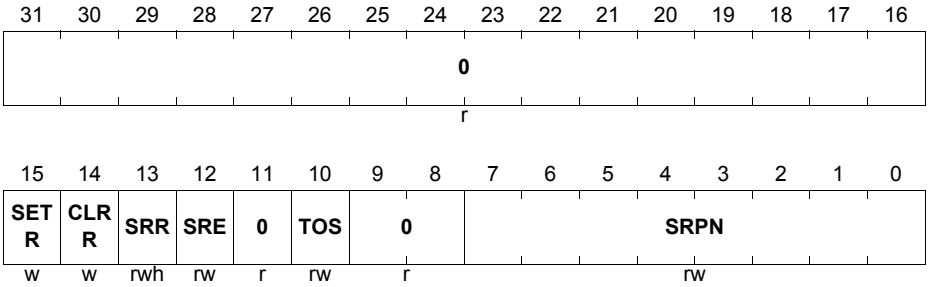
Field	Bits	Type	Description
SEC_EN	0	rw	**Single error correction enable** 0_B Single bit error correction for BMURAM disabled 1_B Single bit error correction for BMURAM enabled
0	[31:1]	r	**reserved** returns ‘0’ if read; should be written with ‘0’.

Please see **“Error Correction Code (ECC)” on Page 18-18** for more information regarding the use of this register.

*Note: This register is ENDINIT protected, in addition the register cannot be accessed unless the “secwen_i” input is asserted. When “secwen_i” is not asserted accesses to **MIECON2** will generate an FPI error acknowledge.*

18.6.6 Interrupt System Registers

SRC
Service Request Control Register (FC_H) Reset Value: 0000 0000$_H$



Field	Bits	Type	Description
SRPN	[7:0]	rw	**Service Request Priority Number** 00_H Service request is never serviced 01_H Service request is on lowest priority ... FF_H Service request is on highest priority
TOS	10	rw	**Type of Service Control** 0_B CPU service is initiated 1_B PCP service is initiated
SRE	12	rw	**Service Request Enable** 0_B Service request is disabled 1_B Service request is enabled
SRR	13	rwh	**Service Request Flag** 0_B No service request is pending 1_B A service request is pending[1)]
CLRR	14	w	**Request Clear Bit** CLRR is required to clear SRR. 0_B No action 1_B Clear SRR; bit value is not stored; read always returns 0; no action if SETR is set also.

Field	Bits	Type	Description
SETR	15	w	**Request Set Bit** SETR is required to set SRR. 0_B No action 1_B Set SRR; bit value is not stored; read always returns 0; no action if CLRR is set also.
0	[9:8], 11, [31:16]	r	**Reserved** Read as 0; should be written with 0.

1) The bit field SRR is automatically cleared by hardware at the end of an interrupt arbitration round if the node was the winner, therefore this information is not suitable for interrupt plausibility checks.

19 On-Chip Debug Support (OCDS)

This chapter gives an overview about the debug features of the TC1798 device. This chapter does not describe the TC1798 debug functionality and capabilities in detail. For detailed information about the On-Chip Debug Support (OCDS) functionality as required by tool suppliers please contact local Infineon representatives.

19.1 Overview

TC1798 supports OCDS Level 1 and 3.

OCDS Level 1

The OCDS Level 1 is mainly assigned for system software debugging purposes which have a demand for low-cost standard debugger hardware.

The OCDS Level 1 is based on a Debug Interface that is used by the external debug hardware to communicate with the system. The on-chip Cerberus module controls the interactions between the Debug Interface and the on-chip modules and allows in particular to access the whole address space of the device. The memory mapped on-chip debug resources make it possible to trigger on instruction and data addresses as well as to control user program execution (run/stop, breakpoint, single-step).

OCDS Level 3

The OCDS Level 3 is based on a Multi Core Debug Solution (MCDS) using an Emulation Device. This device has the following features required for high-end emulation purposes:

- Emulation Device is available in the same package variants as TC1798
- Higher current consumption due to trace and overlay RAM is the only difference
- TriCore program trace
- TriCore data trace (no register file trace)
- PCP ownership trace
- PCP program trace
- PCP data write to PRAM trace (no register file trace)
- Full visibility of internal peripheral bus (SPB)
- Full visibility of up to two arbitrary SRI bus slaves
- Time aligned parallel trace of all sources
- Breakpoints and watchpoints based on common event generation logic
- Magnitude comparators working on instruction pointers and memory addresses: A <= IP <= B
- Masked magnitude comparators working on the data busses: DATA = “xxxx55xx”
- Sequential event logic: Counters driven by events and equipped with limit comparators are used as event sources again for breakpoint or trace qualification
- Optimized compression of buffered trace data
- Code and data fetch from Emulation Memory

- Highly sophisticated complex qualification- and trigger mechanism
- Pre- and post event trace buffering (“digital oscilloscope”)
- Performance counters
- Continuous trace logging and trace data acquisition up to the bandwidth of the used host interface
- Central time stamp unit to correlate traces from different cores or other sources
- Central mechanism to start and stop all cores simultaneously or selectively
- Halt the system when trace memory is full

The Emulation Device includes the product chip part extended with additional emulation hardware. For detailed information about the Emulation Device functionality (e.g. as required by tool suppliers), please contact local Infineon representatives.

Figure 19-1 shows a block diagram of the TC1798 OCDS system.

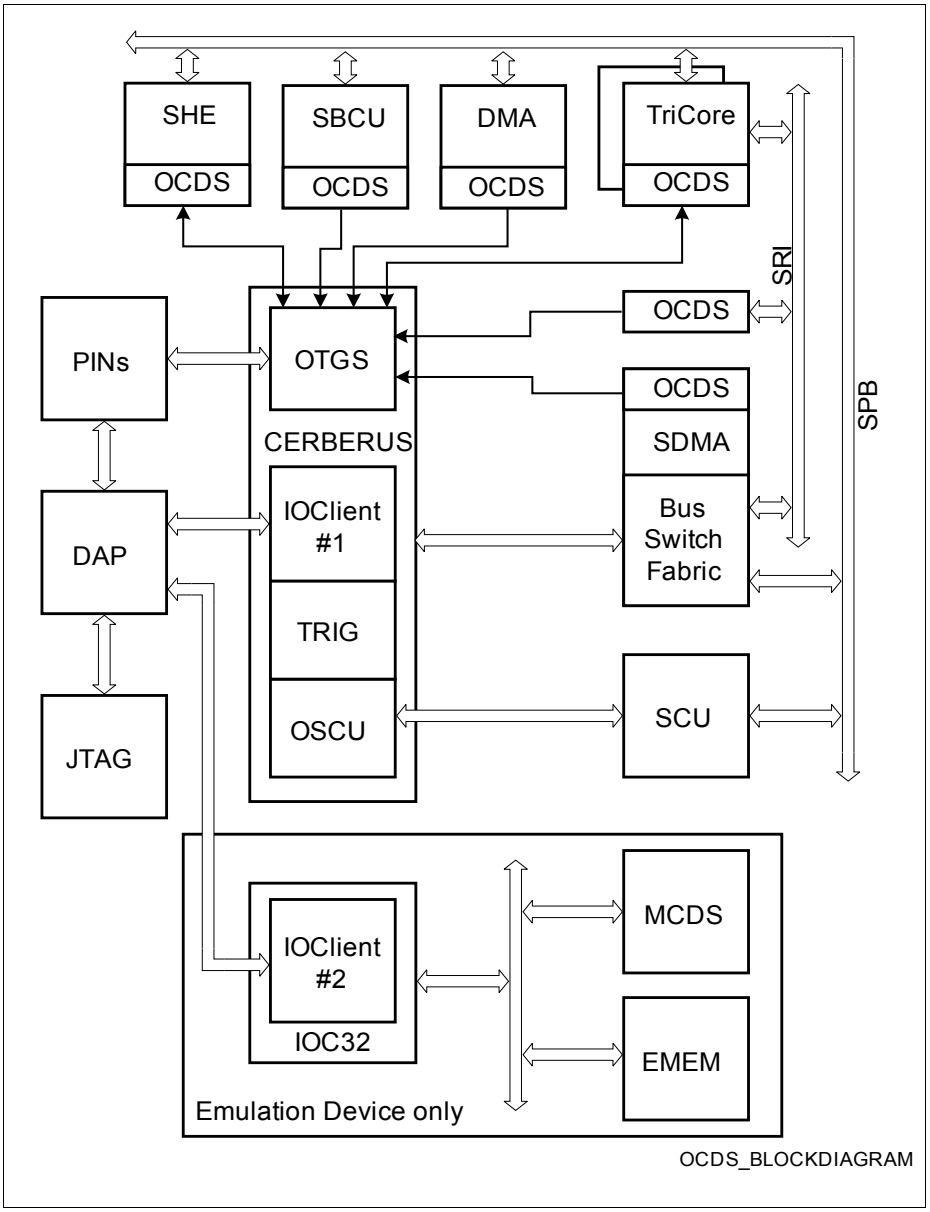


Figure 19-1 OCDS System Block Diagram

Components

The OCDS of the TC1798 consists of the following building blocks:

- OCDS System Control Unit (OSCU)
- TriCore OCDS
- PCP OCDS
- DMA OCDS
- SBCU OCDS
- SRI OCDS
- Multi Core Break Switch (MCBS)
- Break Pin Control
- IOClient
- Device Access Port (DAP)
- JTAG Interface
- Overlay Control

Summary of OCDS Features

- OCDS System Control Unit (OSCU)
  - Controls OCDS enabling
  - Automatic Power Saving
  - Reset control of debug resources
  - Halt After Reset
  - Hot attach of a debugger to a running system
  - Key mechanism allows control the device access in a secure way.
  - State-aware watchdog timer suspension during debugging
  - Control of SoC specific OCDS features
  - Interrupt service request node for debug purposes
- TriCore OCDS features
  - Hardware event generation
  - Break by DEBUG instruction or Break signal from break switch
  - Suspend by Suspend bus or Break signal from break switch
  - Full hardware supported single step
  - Concurrent access to memory and SFRs via Cerberus
- PCP OCDS features
  - Break by DEBUG instruction or Break signal from break switch
  - Concurrent access to memory and SFRs via Cerberus
- DMA/SDMA OCDS features
  - Soft-suspend Mode of DMA channels
  - Break signal generation
  - Trace signal generation
- SBCU OCDS features
  - Event generation on specified transactions

- SRI OCDS features
  - Error recording and service request on bus error
- Multi-Core Break Switch (Cerberus MCBS)
  - TriCore, PCP, DMA/SDMA, break pins and SBCU available as break sources
  - TriCore and PCP available as break targets; other parts can be suspended in addition
  - Synchronous stop and restart of the system
  - Break to Suspend converter

19.2 OCDS Level 1

The basic principle of the TriCore OCDS Level 1 is that all relevant user and debug resources are memory mapped. These resources include on-chip memories, CPU core registers and registers of the peripheral units.

A typical OCDS Level 1 debugging configuration is shown in **Figure 19-2**. It comprises two parts:

- The tool software
- The tool access hardware interface adapter

This configuration makes it possible to realize a cost effective debugging environment that permits comprehensive real-time debugging tasks to be performed.

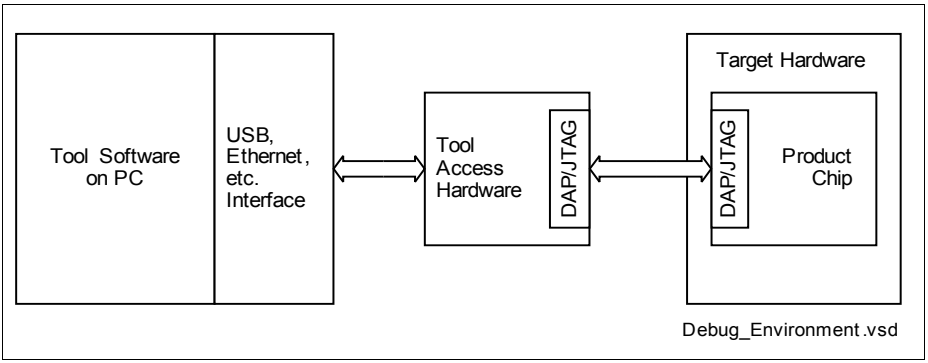


Figure 19-2 Typical OCDS Level 1 Hardware Connections

19.2.1 TriCore CPU OCDS Level 1

This section describes the basic features of the TriCore OCDS Level 1 hardware. For more details please refer to the “TriCore Core Architecture V1.6” manual.

Features

- Single-step support by hardware
- Up to 8 programmable hardware breakpoints. Each one can be defined as a combination of program counter and data address:
  - Breaks on program counter (PC) value
    Two precise PC values or one PC range
    Break before make (BBM) possible
  - Breaks on data address
    Two precise data addresses or one data address range
    No break before make possible (due to pipelined architecture)
  - Combinations of the above break conditions
- Suspend features
  - Core Suspend-Out to suspend bus
  - Configurable Core Suspend-In
- Real-time features
  - Read and write of memory/registers independent of CPU, with minimum intrusion (stealing bus cycles by Cerberus)
  - High-priority requests can still be serviced when the core is in emulation mode - by interrupting the monitor program

19.2.1.1 Basic Concept

The TriCore CPU in the TC1798 provides OCDS with the following two basic parts:

- Debug Event Trigger Generation
- Debug Event Trigger Processing

The first part controls the generation of debug events and the second part controls what actions are taken when a debug event is generated.

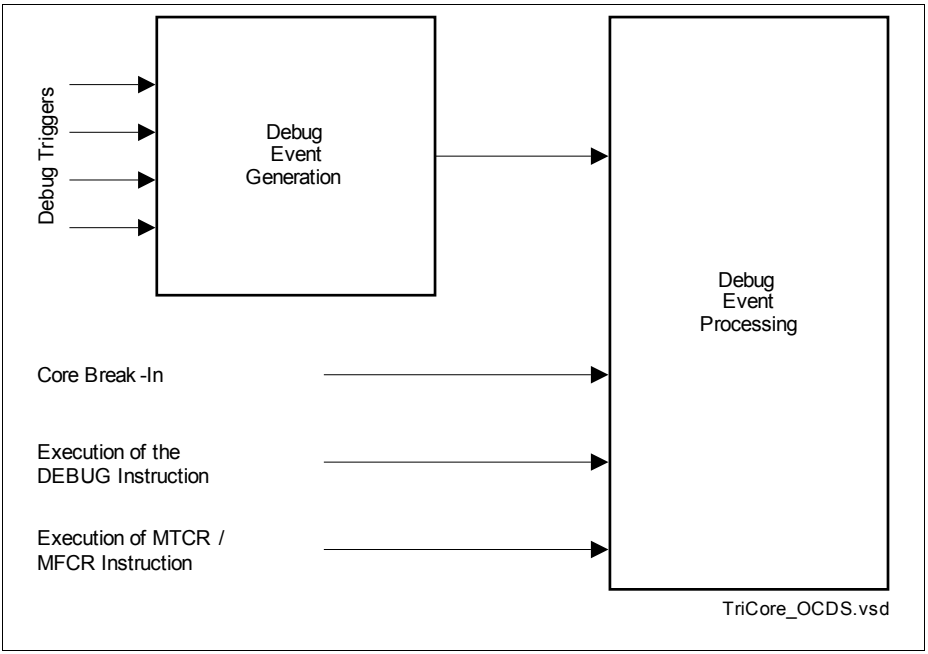


Figure 19-3 Basic TriCore Debug Concept

19.2.1.2 Debug Event Generation

If debug mode is enabled, debug events can be generated by:

- Debug event generation from debug triggers
- Activation of the external Core Break-In signal to the core
- Execution of a DEBUG instruction
- Execution of an MTCR/MFCR instruction

Debug Event Generation from Debug Triggers

The debug event generation unit is responsible for generating debug events when a programmable set of debug triggers is active. TC1.6 has 8 address comparator registers dedicated for debug. Pairs can be used for range triggers.

These debug triggers provide the inputs to a programmable block of combinational logic that outputs debug events. The aim is to be able to specify the breakpoints that use fairly simple criteria purely in the on-chip debug event generation unit, and to rely on help from the external debug system or debug monitor to implement more complex breakpoints.

Activation of the External Core Break-in signal

When activating the TC1798 device pin $\overline{\text{BRKIN}}$ = 0 and if MCBS and port control is configured to forward this event to the Core Break-In signal, a break event is induced as specified in an External Break Input Event Specifier Register EXEVT (**Figure 19-4**).

Execution of a DEBUG Instruction

The TriCore architecture supports a mechanism through which software can explicitly generate a debug event. This can be used, for instance, by a debugger to patch code held in RAM in order to implement breakpoints. A special DEBUG instruction is defined which is a user mode instruction, and its operation depends on whether the debug mode is enabled. 16-bit and 32-bit forms of the DEBUG instruction are provided.

If debug mode is enabled, the DEBUG instruction causes a debug event to be raised and the action defined in the Software Break Event Specifier Register SWEVT is taken. If the debug mode is not enabled, then the DEBUG instruction is treated as a NOP instruction.

Execution of an MTCR/MFCR Instruction

In order to protect the emulator resource, a debug event is raised whenever an MTCR or MFCR instruction is used to read or modify a user core SFR, but an event is not raised when the user reads or modifies one of the dedicated core debug registers: DBSR, CREVT, SWEVT, EXEVT, TR0EVT, TR1EVT, DMS, DCX or DBGTCR.

The action that is performed when an MTCR or MFCR instruction is executed on user core SFRs defined by the content of the Emulator Resource Protection Event Specifier Register CREVT.

19.2.1.3 Debug Actions

Four types of debug actions are available:

- Assert Core Break-out signal and $\overline{\text{BRKOUT}}$ (**Figure 19-4**) via MCBS unit and port control
- Halt the CPU core
- Cause a breakpoint trap
- Generate an interrupt request

These debug actions are selected by programming the corresponding Event Specifier registers. Their contents determine which action shall be taken when the corresponding debug event occurs. In parallel the Core Suspend-Out signal can be activated.

19.2.1.4 TriCore OCDS Registers

Please refer to “TriCore Core Architecture V1.6” manual.

19.2.2 PCP OCDS Level 1

PCP has no hardware means of generating trigger events.

To set breakpoints, the debugger is expected to patch the code in the PCP code memory (CMEM) with DEBUG instructions. If a DEBUG instruction is executed, the running channel program is terminated, either with Debug Exit or with Error Exit.

The PCP has a suspend input, a break input and a break output. The Break Switch can send an external break request to the PCP, with the same consequence as above (Debug Exit or Error Exit).

19.2.3 SBCU OCDS Level 1

The BCU of the SPB bus in the TC1798 offers very powerful means for trigger generation. The BCU contains comparators for

- the arbitration phase (look for specific bus master)
- the address phase (look for specific address or range)
- the data phase (look for read, write, supervisor mode, etc.)

The results can be combined to generate a break request signal, which is sent to the Break Switch.

The OCDS registers of SBCU are described in chapter “On-Chip System Buses and Bus Bridges” starting from section “System Bus Control Unit Registers”.

19.2.4 DMA/SDMA OCDS Level 1

The DMA/SDMA controller in the TC1798 provides the following debugging capabilities:

- Hard suspend mode of the DMA/SDMA controller (for test purposes only)
- Soft suspend mode of DMA/SDMA channels
- Break signal generation

In suspend modes, the operations of DMA/SDMA channels or the complete module are stopped. Under certain conditions, a break signal is also generated for the on-chip debug support logic.

More details on the OCDS Level 1 debug capabilities of the DMA/SDMA controller are provided in section “On-Chip Debug Capabilities” of the DMA/SDMA chapter.

19.3 Debug Interface (Cerberus)

The Cerberus module is the on-chip unit that controls all OCDS main debug functions. Generally, the Cerberus may not be used by any application software, since this could disturb the emulation tool behavior.

The Cerberus module is built up by three parts (see also **Figure 19-1**):

- OCDS System Control Unit - OSCU
- IOClient
- Multi Core Break Switch - MCBS

A tool can be connected to the device in two ways:

- A two line DAP interface via the DAP module receives the debugger commands, converts them and outputs them to the IOClient interface.
- Standard JTAG interface is connected via the JTAG controller with the IOClient interface

Two additional pins are available to handle an external break condition. The external debug hardware can access the Cerberus registers and arbitrary memory locations across the System Peripheral Bus.

Features

- OCDS Level 1 control via
  - 5-pin standard JTAG interface
  - 2-pin DAP interface
- Generation of external break condition via $\overline{\text{BRKIN}}$/$\overline{\text{BRKOUT}}$ pins possible
- Full access to the complete SPB Bus address space via DAP/JTAG
- No user resources (hardware/software) are required
- No or minimum run-time impact (Cerberus bus priority can be controlled)
- Generic memory read/write functionality
- Write word, half-word and byte
- Block read and write
- Full support for communication between an on-chip monitor program and the external debugger
- Pending reads/writes can be optionally triggered by the OCDS module (memory tracing)
- Download of programs and data via DAP/JTAG
- Control of the OCDS blocks
- Data acquisition

19.3.1 RW Mode

As the name implies, the RW mode is used by a DAP/JTAG host to read or write arbitrary memory locations via the DAP/JTAG interface. The RW mode needs the SPB Bus master interface of the Cerberus to actively request data reads or data writes.

Data Types Supported

- WORD (32-bit): The default data type; used for single word transfers and block transfers.
- HWORD (16-bit): For reading 16-bit registers without getting a bus error, a dedicated IOClient instruction is provided.
- BYTE (8-bit): If the DAP/JTAG host wants to read a byte, it has to read the associated word or half-word. Then the host has to extract the part needed itself.

19.3.2 Communication Mode

In Communication Mode, the Cerberus has no access to the internal buses and communication is established between the external DAP/JTAG host and a software monitor (embedded into the application program) via the Cerberus registers. The communication mode is the default mode after reset.

In Communication Mode, the external DAP/JTAG host is master of all transactions. The host requests the monitor to write or read a value to/from the Cerberus register COMDATA. The difference to RW Mode is that the read or write request is not actively executed by Cerberus. The request just sets bits in the CPU accessible IOSR register to signal the monitor that the debugger wants to send or receive a value. The software monitor has to poll the IOSR register for that.

19.3.3 Triggered Transfers

Triggered transfers can be used to read from or write to a certain memory location when an OCDS trigger becomes active.

The main application for Triggered Transfers is to trace a certain memory location. This can be done, when the OCDS of the CPU activates its break out signal, if this memory location is written by the user program. This event is used as a transfer trigger through the configuration of the MCBS. Cerberus is configured to read the location on this trigger.

19.3.4 Multi Core Break Switch

In TC1798, there are several sources and targets for break signals. For instance the OCDS run control of one processor can break the other processor unit. The Multi Core Break Switch (MCBS) is a part of the Cerberus and allows to propagate break requests from sources to targets in a generic and flexible way. **Figure 19-4** shows the break signal interfaces of the MCBS.

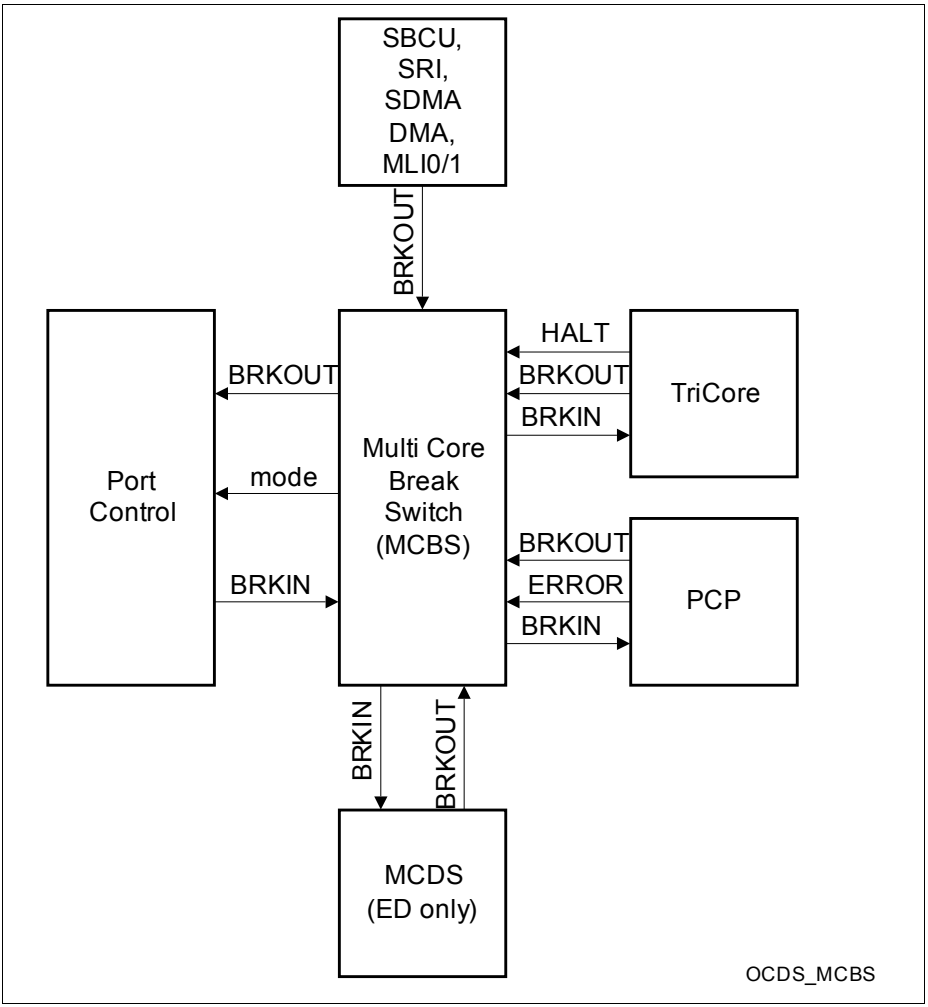


Figure 19-4 Break Switch Interfaces

The MCBS unit supports the following features:

- Break-in sources: TriCore, PCP, DMA, SBCU, MLI0, MLI1
- Up to two device pins configurable as BRKIN/BRKOUT pins
- Two independent break buses
- Suspend generation supports delayed suspend
- Break-to-suspend converter

- Create interrupt request with a break coming from a source
- Synchronous restart of the system

19.4 JTAG Interface

The JTAG interface is a standardized unit that is typically used for boundary scan and internal device tests. Because both of these applications are not active during normal device operation in a system, the JTAG port can be used during normal device operation as an ideal interface for debugging tasks.

19.5 Device Access Port (DAP)

The cost inferred by each non-functional pin is a strong argument to reduce the tool access port to as few pins as possible. The standardized Device Access Port (DAP) of Infineon's latest micro controllers offers a convenient method to get the required functionality at the least possible cost. With DAP only two pins (DAP0 for the clock, DAP1 for the bidirectional data) are needed to communicate with the tool.

DAP uses a straightforward half-duplex protocol, i.e. the DAP1 pin is used for data transfer from tool to device and from device to tool at different periods of time while the clock is provided by the tool to the DAP0 input.

19.5.1 DAP Telegram Format

All information transport between tool and device is done in telegrams. Mandatory 6 bit CRC check sums assure secure transport even in noisy environments. Splitting command and reply into separate units transported sequentially allows half-duplex transmission over a single bidirectional line. The physical interface medium can be chosen independently as long as the serial bit stream can be transported.

19.5.2 DAP Telegram Catalog

This chapter lists the telegrams implemented by the TC1798. Other telegrams are silently ignored, resulting in a time-out condition on the tool side.

Three groups of telegrams can be distinguished:

Control Telegrams

These four telegrams are needed to establish and maintain the connection from tool to device as such. No data is transported.

- sync - request synchronization pattern
- turn_off - shut down DAP
- poll - get the current service request
- set_maxwait - adjust the parameter for time out

JTAG Telegrams

The telegrams of this group are simple wrappers around the standard JTAG commands, adding the relaxed timing and increased transmission speed and quality of DAP.

- jtag_mode - switch DAP to BYPASS mode
- jtag_reset - reset the TAP controller
- jtag_setIR - write the TAP's INSTRUCTION register
- jtag_swapIR - write and read the TAP's INSTRUCTION register
- jtag_setDR - write the current JTAG data register
- jtag_swapDR - write and read the current JTAG data register
- jtag_moreDR - write and read part of a long JTAG data register

Client Telegrams

The last group allows direct access to IOClients like Cerberus of the device, completely hiding the asynchronous timing between tool clock and system clock of the device.

The following five telegrams belong to this group:

- client_set - define the current IOClient
- client_get - ask for the index of the current IOClient
- client_reset - reset the current IOClient
- client_write - write to the current IOClient
- client_read - read from the current IOClient

19.6 Cerberus and JTAG Registers

This section summarizes all Cerberus and JTAG registers for reference purposes. Details on these registers are contained in OCDS documents that are available for tool suppliers on request (please contact local Infineon representatives). All CERBERUS registers are prefixed “CBS_” in the register map of a device.

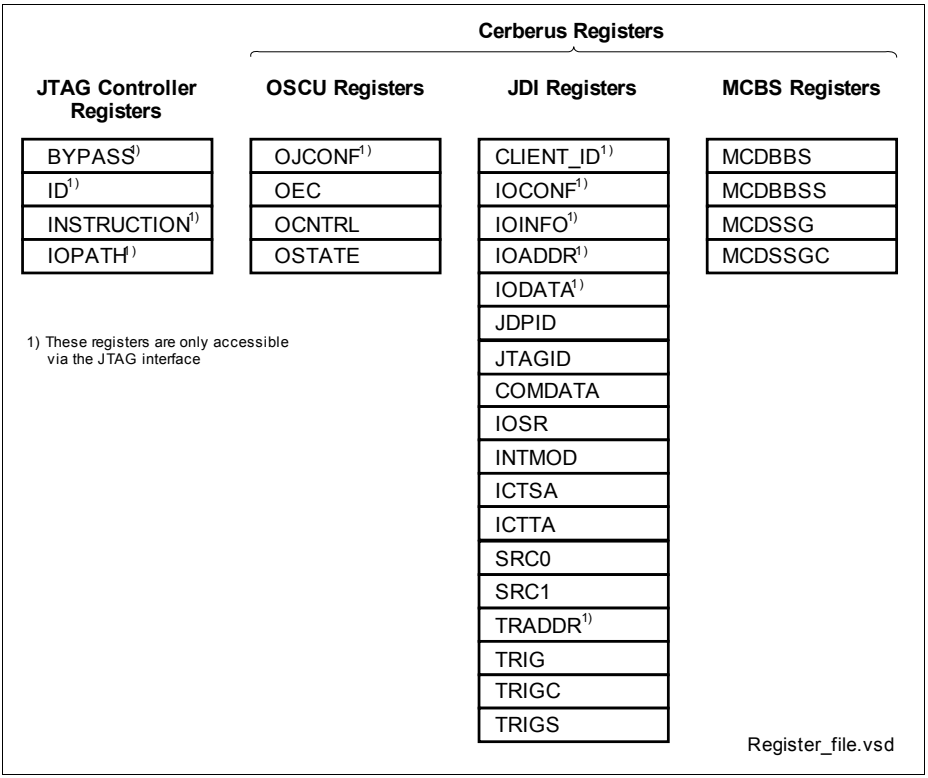


Figure 19-5 JTAG/Cerberus Register Overview

Table 19-1 JTAG/Cerberus Register Overview

Register Short Name	Register Long Name	Address
JTAG Controller Registers		
BYPASS	JTAG Bypass Register (1-bit)	1)
ID	JTAG Device Identification Register (32-bit)	1)
INSTRUCTION	JTAG Instruction Register (8-bit)	1)
IOPATH	IO Client Selection Register (2-bit)	1)
Cerberus Registers		
OJCONF	OSCU Configuration by JTAG Register	1)

Table 19-1 JTAG/Cerberus Register Overview (cont'd)

Register Short Name	Register Long Name	Address
OEC	OCDS Enable Control Register	F000 0478$_H$
OCNTRL	OSCU Configuration and Control Register	F000 047C$_H$
OSTATE	OSCU Status Register	F000 0480$_H$
CLIENT_ID	JTAG Client Identification Register (32-bit)	1)
IOCONF	Configuration Register (12-bit)	1)
IOINFO	State Information for Error Analysis Register (16-bit)	1)
IOADDR	Address for Data Access Register (32-bit)	1)
IODATA	RW Mode Data Register (32-bit)	1)
JDPID	Cerberus Module Identification Register	F000 0408$_H$
JTAGID	JTAG Device Identification Register	F000 0464$_H$
COMDATA	Communication Mode Data Register	F000 0468$_H$
IOSR	Status Register	F000 046C$_H$
INTMOD	Internal Mode Status and Control Register	F000 0484$_H$
ICTSA	Internal Controlled Trace Source Address Register	F000 0488$_H$
ICTTA	Internal Controlled Trace Target Address Register	F000 048C$_H$
MCDBBS	Break Bus Switch Configuration Register	F000 0470$_H$
MCDBBSS	Break Bus Switch Status Register	F000 0490$_H$
MCDSSG	Suspend Signal Generation Status and Control Register	F000 0474$_H$
MCDSSGC	Suspend Signal Generation Configuration Register	F000 0494$_H$
SRC0	Service Request Control Register 0	F000 04FC$_H$
SRC1	Service Request Control Register 1	F000 04F8$_H$
TRADDR	Triggered Transfer Destination Address	1)
TRIG	Trigger to Host	F000 04A8$_H$
TRIGC	Clear Trigger to Host	F000 04A4$_H$
TRIGS	Set Trigger to Host	F000 04A0$_H$

1) These registers are only accessible via the JTAG interface.

20 Asynchronous/Synchronous Serial Interface (ASC)

This chapter describes the two ASC Asynchronous/Synchronous Serial Interfaces, ASC0 and ASC1, of the TC1798. It contains the following sections:

- Functional description of the ASC kernel, valid for ASC0 and ASC1 (see **Page 20-1**)
- ASC kernel register description, describes all ASC kernel specific registers (see **Page 20-19**)
- TC1798 implementation-specific details and registers of the ASC0/ASC1 modules (see **Page 20-30**).

*Note: The ASC kernel register names described in **Section 20.2** are referenced in the TC1798 User´s Manual by the module name prefix "ASC0_" for the ASC0 interface and by "ASC1_" for the ASC1 interface.*

20.1 ASC Kernel Description

Figure 20-1 shows a global view of the ASC interface.

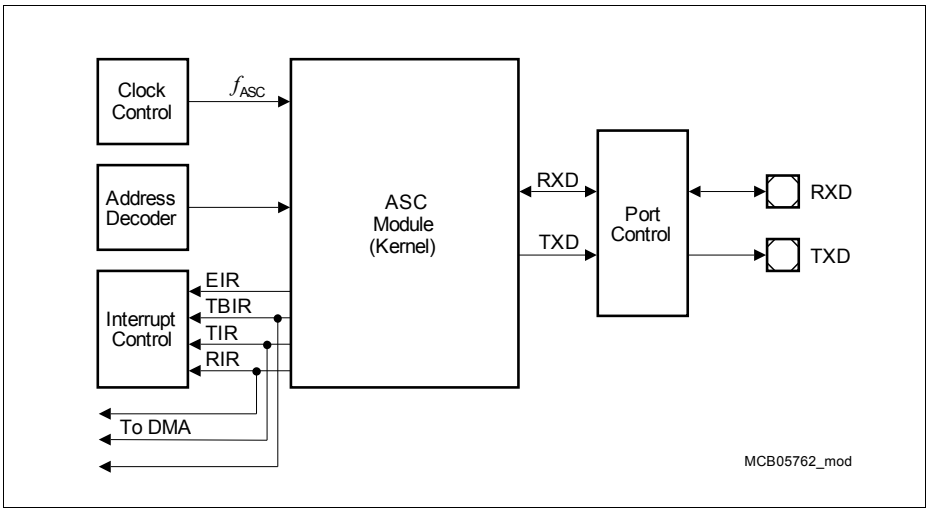


Figure 20-1 General Block Diagram of the ASC Interface

The ASC module communicates with the external world via two I/O lines. The RXD line is the receive data input signal (and also output signal in Synchronous Mode), and TXD is the transmit output signal.

Clock control, address decoding, and interrupt service request control are managed outside the ASC module kernel.

20.1.1 Overview

The ASC provides serial communication between the TC1798 and other microcontrollers, microprocessors, or external peripherals.

The ASC supports full-duplex asynchronous communication and half-duplex synchronous communication. In Synchronous Mode, data is transmitted or received synchronous to a shift clock that is generated by the ASC internally. In Asynchronous Mode, 8-bit or 9-bit data transfer, parity generation, and the number of stop bits can be selected. Parity, framing, and overrun error detection are provided to increase the reliability of data transfers. Transmission and reception of data is double-buffered. For multiprocessor communication, a mechanism is included to distinguish address bytes from data bytes. Testing is supported by a loop-back option. A 13-bit baud rate generator provides the ASC with a separate serial clock signal, which can be accurately adjusted by a prescaler implemented as fractional divider.

Features

- Full-duplex asynchronous operating modes
  - 8-bit or 9-bit data frames, LSB first
  - Parity-bit generation/checking
  - One or two stop bits
  - Baud rate from 6.875 Mbit/s to 1.64 bit/s (@ 110 MHz module clock)
  - Multiprocessor mode for automatic address/data byte detection
  - Loop-back capability
- Half-duplex 8-bit synchronous operating mode
  - Baud rate from 13.75 Mbit/s to 1119 bit/s (@ 110 MHz module clock)
- Double-buffered transmitter/receiver
- Interrupt generation
  - On a transmit buffer empty condition
  - On a transmit last bit of a frame condition
  - On a receive buffer full condition
  - On an error condition (frame, parity, overrun error)
- Implementation features
  - Connections to DMA Controller
  - Connections of receiver input to GPTA (LTC) for baud rate detection and LIN break signal measuring

20.1.2 General Operation

The ASC supports full-duplex asynchronous communication up to Mbit/s and half-duplex synchronous communication up to Mbit/s (@ MHz module clock). In Synchronous Mode, data is transmitted or received synchronous to a shift clock generated by the microcontroller. In Asynchronous Mode, 8-bit or 9-bit data transfer, parity generation, and the number of stop bits can be selected. Parity, framing, and overrun error detection are provided to increase the reliability of data transfers. Transmission and reception of data are double-buffered. For multiprocessor communication, a mechanism is included to distinguish address bytes from data bytes. Testing is supported by a loop-back option. A 13-bit baud rate generator provides the ASC with a separate serial clock signal, which can be accurately adjusted by a prescaler implemented as fractional divider.

A transmission is started by writing to the Transmit Buffer Register, TBUF. Only the number of data bits determined by the selected operating mode will actually be transmitted; that is, bits written to positions 9 through 15 of register TBUF are always insignificant. Data transmission is double-buffered, so a new character may be written to TBUF before the transmission of the previous character is complete. This allows a back-to-back transmission of characters to take place without gaps.

Data reception is enabled by the receiver enable bit CON.REN. After a reception has been completed, the received data and, if provided by the selected operating mode, the received parity bit can be read from the (read-only) receive buffer register RBUF. Unused bits in the upper half of RBUF that are not required in the selected operating mode will be read as zeros.

Data reception is double-buffered, so that reception of a second character may already begin before the previously received character has been read out of the receive buffer register. In all modes, receive buffer overrun error detection can be selected through bit CON.OEN. When enabled, the overrun error status flag CON.OE and the error interrupt request line EIR will be activated when the receive buffer register has not been read by the time reception of a second character is complete. In this case, the previously received character in the receive buffer is overwritten.

The loop-back option (selected by bit CON.LB) allows the data currently being transmitted to be received simultaneously in the receive buffer. This may be used to test serial communication routines at an early stage without having to provide an external network. In loop-back mode, the alternate input/output function of port pins is not required.

20.1.3 Asynchronous Operation

Asynchronous Mode supports full-duplex communication, in which both transmitter and receiver use the same data frame format and have the same baud rate. Data is transmitted on pin TXD and received on pin RXD. **Figure 20-2** shows the block diagram of the ASC when operating in Asynchronous Mode.

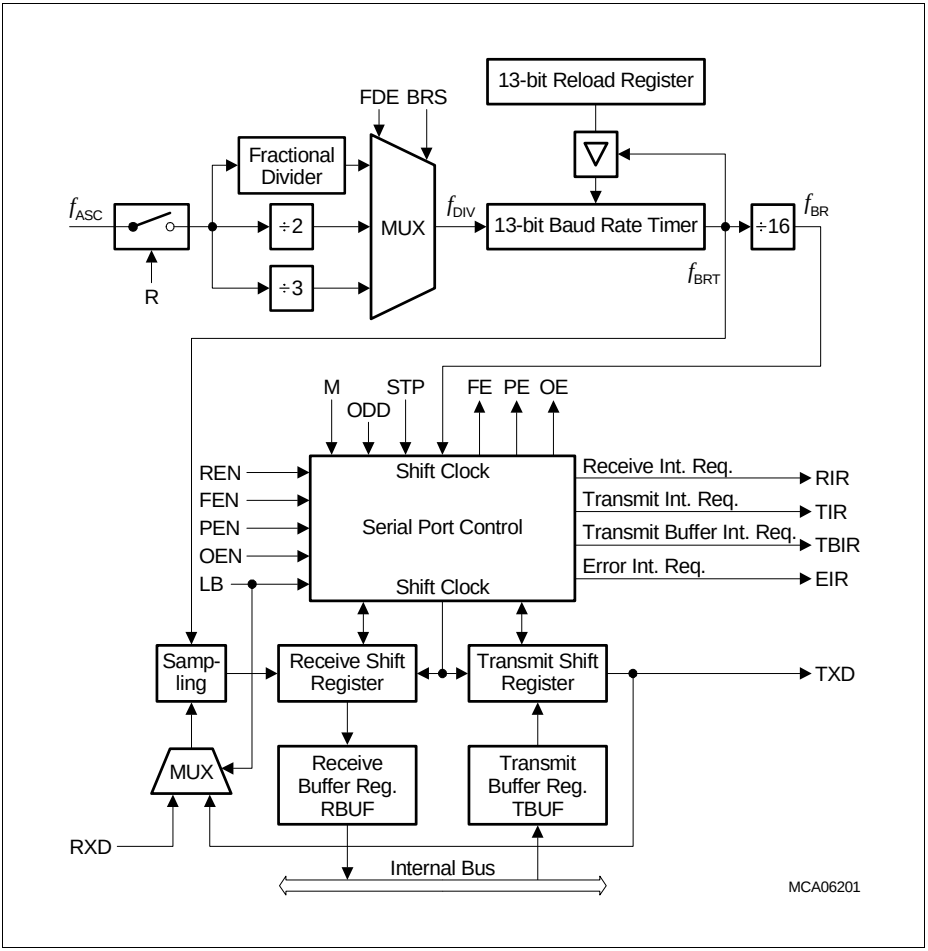


Figure 20-2 Asynchronous Mode of the ASC

20.1.3.1 Asynchronous Data Frames

Asynchronous data frames can consist of 8-bit or 9-bit data frames.

8-bit Data Frames

The 8-bit data frames consist of either eight data bits D7 … D0 (CON.M = 001_B), or of seven data bits D6 … D0 plus an automatically generated parity bit (CON.M = 011_B). Parity may be odd or even, depending on bit CON.ODD. An even parity bit will be set if the modulo-2 sum of the seven data bits is 1. An odd parity bit will be cleared in this case. Parity checking is enabled via bit CON.PEN (always OFF in 8-bit data mode). The parity error flag CON.PE will be set, along with the error interrupt request flag, if a wrong parity bit is received. The received parity bit itself will be stored in RBUF too.

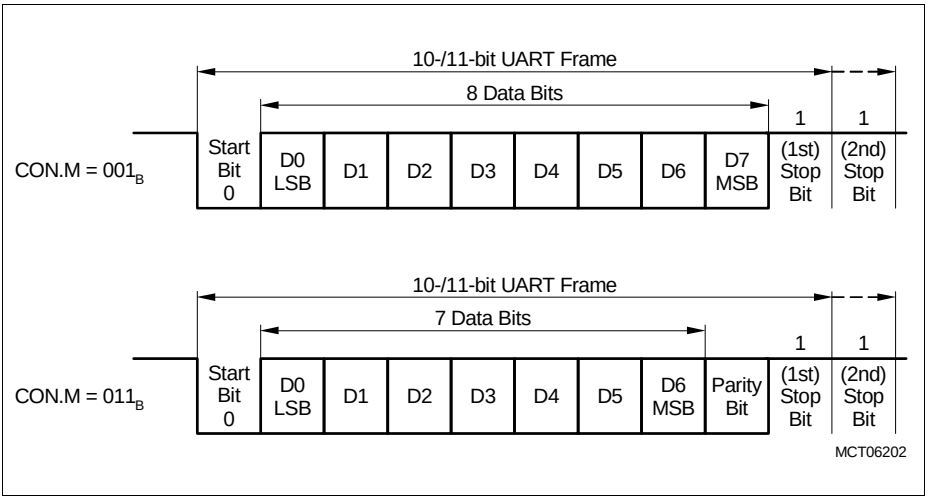


Figure 20-3 Asynchronous 8-bit Frames

9-bit Data Frames

The 9-bit data frames consist of nine data bits D8 … D0 (CON.M = 100_B), or of eight data bits D7 … D0 plus an automatically generated parity bit (CON.M = 111_B) or of eight data bits D7 … D0 plus wake-up bit (CON.M = 101_B). Parity may be odd or even, depending on bit CON.ODD. An even parity bit will be set if the modulo-2-sum of the eight data bits is 1. An odd parity bit will be cleared in this case. Parity checking is enabled via bit CON.PEN (always OFF in 9-bit data and wake-up mode). The parity error flag CON.PE will be set along with the error interrupt request flag if a wrong parity bit is received. The received parity bit itself will be stored in RBUF too.

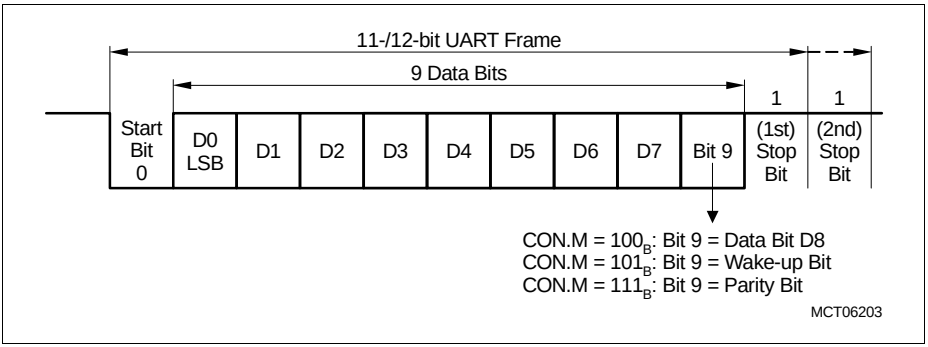


Figure 20-4 Asynchronous 9-bit Frames

In Wake-up Mode (CON.M = 101_B), received frames are transferred to the receive buffer register only if the 9th bit (the wake-up bit) of the frame is 1. If this bit is 0, no receive interrupt request will be activated and no data will be transferred.

This feature can be used to control communication in multi-processor systems, for example:
When the master processor aims to transmit a block of data to one of several slaves, it first sends out an address ‘byte’ (in this case, a ‘byte’ consists of nine bits) that identifies the target slave. An address ‘byte’ differs from a data ‘byte’ in that the additional 9th bit is a 1 for an address ‘byte’ but is a 0 for a data ‘byte’, so, no slave will be interrupted by a data ‘byte’. An address ‘byte’ will interrupt all slaves (operating in 8-bit data + wake-up bit mode), so each slave can examine the eight LSBs of the received character (the address). The addressed slave will switch to 9-bit data mode (for example, by clearing bit CON.M[0]), which enables it to also receive the data bytes that will be coming (having the wake-up bit cleared). The slaves that were not being addressed remain in 8-bit data + wake-up bit mode, ignoring the following data ‘bytes’.

20.1.3.2 Asynchronous Transmission

Asynchronous transmission begins when the next overflow of the divide-by-16 baud rate timer (transition of the baud rate clock f_{BR}) occurs, if bit CON.R is set and data has been loaded into TBUF. The transmitted data frame consists of three elements:

1. The start bit
2. The data field (8 or 9 bits, LSB first, including a parity bit, if selected)
3. The delimiter (1 or 2 stop bits)

Data transmission is double-buffered. When the transmitter is idle, the transmit data loaded into TBUF is immediately moved to the transmit shift register; thus, freeing TBUF for the next transmit data to be loaded. This is indicated by the transmit buffer interrupt request line TBIR being activated. TBUF may then be loaded with the next transmit data while transmission of the previous one continues.

The Transmit Interrupt Request line TIR will be activated before the last bit of a frame is transmitted, that is, before the first or the second stop bit is shifted out of the transmit shift register.

Note: A dedicated GPIO device pin which is connected to the module output pin TXD must be configured by software as alternate data output for asynchronous transmission.

20.1.3.3 Asynchronous Reception

Asynchronous reception is initiated by a falling edge (1-to-0 transition) on pin RXD, on the condition that bits CON.R and CON.REN are set. The receive data input pin RXD is sampled at sixteen times the rate of the selected baud rate. A majority decision of the 7^{th}, 8^{th} and 9^{th} sample determines the effective sampled bit value. This avoids erroneous results that may be caused by noise.

If the detected value is not a 0 when the start bit is sampled, the receive circuit is reset and waits for the next 1-to-0 transition at pin RXD. If the start bit proves valid, the receive circuit continues sampling and shifts the incoming data frame into the receive shift register.

When the last stop bit has been received, the contents of the receive shift register are transferred to the Receive Data Buffer Register RBUF. Simultaneously, the receive interrupt request line RIR is activated after the 9^{th} sample in the last stop bit time-slot (as programmed), regardless whether valid stop bits have been received or not. The receive circuit then waits for the next start bit (1-to-0 transition) at the receive data input line.

Note: A dedicated GPIO pin that is connected to the module input pin RXD must be configured by software as input for asynchronous reception.

Asynchronous reception is stopped by clearing bit CON.REN. A currently received frame is completed including generation of the receive interrupt request and an error interrupt request, if appropriate. Start bits that follow this frame will not be recognized.

Note: In wake-up mode, received frames are transferred to the receive buffer register only if the 9th bit (the wake-up bit) is 1. If this bit is 0, no receive interrupt request will be activated and no data will be transferred.

20.1.3.4 RXD/TXD Data Path Selection in Asynchronous Modes

The data paths for the serial input and output data in Asynchronous Modes are affected by control bit CON.LB (loop-back) as shown in **Figure 20-5**.

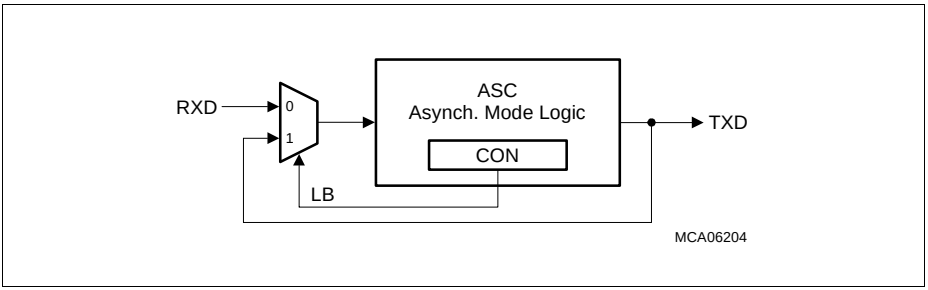


Figure 20-5 RXD/TXD Data Path Selection in Asynchronous Modes

20.1.4 Synchronous Operation

Synchronous Mode supports half-duplex communication, usable for simple I/O expansion via shift registers. Data is transmitted and received via pin RXD while pin TXD outputs the shift clock. These signals are typically connected as alternate functions with GPIO port pins. Synchronous Mode is selected with CON.M = 000_B.

Eight data bits are transmitted or received synchronous to a shift clock generated by the internal baud rate generator. The shift clock is active only as long as data bits are transmitted or received.

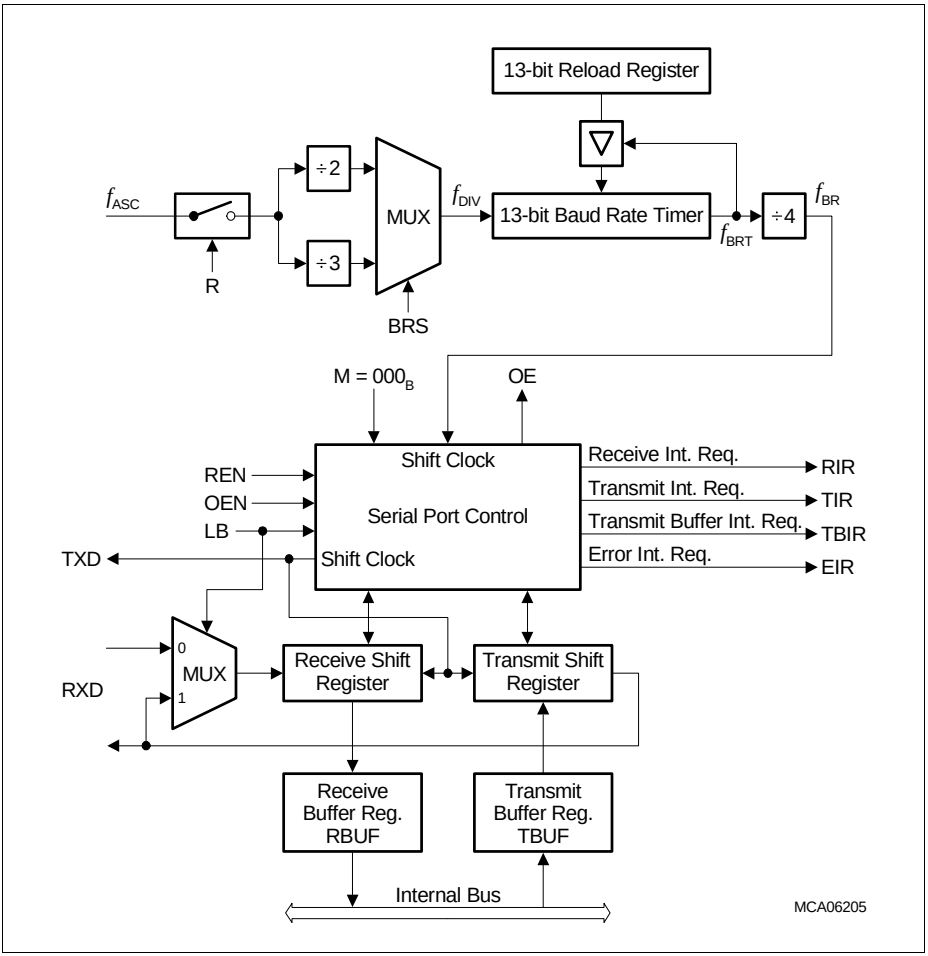


Figure 20-6 Synchronous Mode of Serial Channel ASC

20.1.4.1 Synchronous Transmission

Synchronous transmission begins within four state times after data has been loaded into TBUF, provided that CON.R is set and CON.REN = 0 (half-duplex, no reception), with one exception: in Loop-back Mode (bit CON.LB set), CON.REN must be set for reception of the transmitted byte. Data transmission is double-buffered. When the transmitter is idle, the transmit data loaded into TBUF is immediately moved to the transmit shift register, thus freeing TBUF for the next data to be sent. This is indicated by the transmit buffer interrupt request line TBIR being activated. TBUF may now be loaded with the next data, while transmission of the previous one continues. The data bits are transmitted synchronously with the shift clock. After the bit time for the 8th data bit, both TXD and RXD will be set to high level, the transmit interrupt request line TIR is activated, and serial data transmission stops.

Note: The dedicated GPIO device pins that are connected to TXD and RXD must be configured by software as alternate data outputs in order to provide the shift clock and the output data during synchronous transmission.

20.1.4.2 Synchronous Reception

Synchronous reception is initiated by setting bit CON.REN = 1. If bit CON.R = 1, the data applied at RXD is clocked into the receive shift register synchronously to the clock which is output at TXD. After the 8th bit has been shifted in, the contents of the receive shift register are transferred to the receive data buffer RBUF, the receive interrupt request line RIR is activated, the receiver enable bit CON.REN is reset, and serial data reception stops.

Synchronous reception is stopped by clearing bit CON.REN. Any byte that is currently being received is completed, including the generation of the receive interrupt request and an error interrupt request, if appropriate. Writing to the transmit buffer register while a reception is in progress has no effect on reception and will not start a transmission.

If a previously received byte has not been read out of the receive buffer register by the time the reception of the next byte is complete, both the error interrupt request line EIR and the overrun error status flag CON.OE will be activated/set, provided that the overrun check has been enabled by bit CON.OEN.

Note: The dedicated GPIO device pin that is connected to TXD must be configured by software as alternate data output in order to provide the shift clock. The dedicated GPIO device pin that is connected to RXD must be configured by software as input during synchronous reception.

20.1.4.3 Synchronous Timing

Figure 20-7 shows timing diagrams of the ASC Synchronous Mode data reception and data transmission. In idle state, the shift clock is at high level. With the beginning of a synchronous transmission of a data byte, the data is shifted out at RXD with the falling edge of the shift clock. If a data byte is received through RXD, data is latched with the rising edge of the shift clock.

One shift clock cycle (f_{BR}) delay is inserted between two consecutive receive or transmit data bytes.

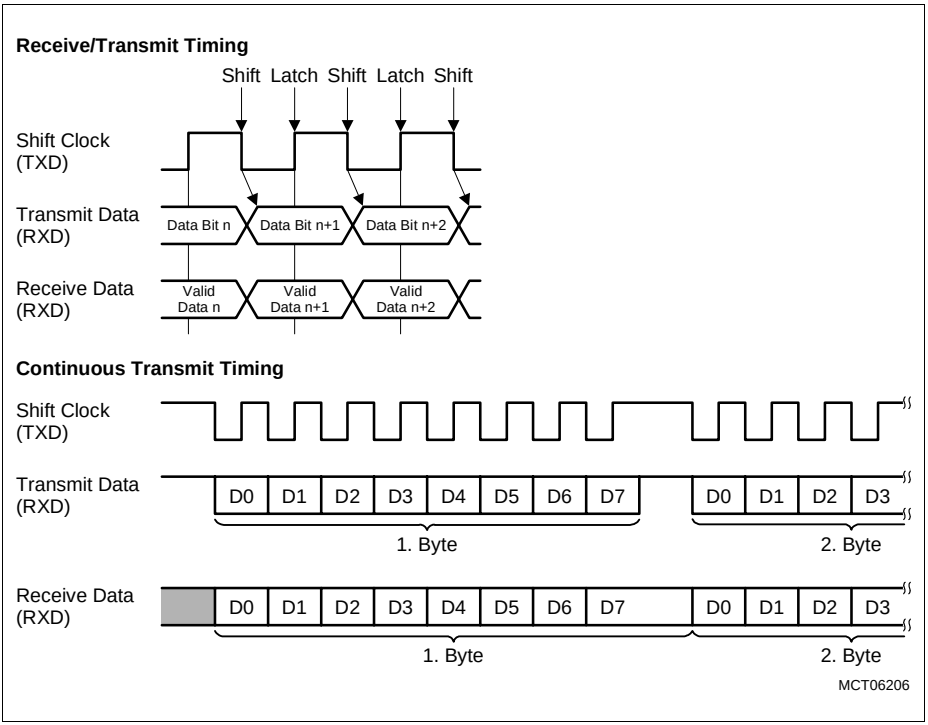


Figure 20-7 ASC Synchronous Mode Waveforms

20.1.5 Baud Rate Generation

The ASC has its own dedicated 13-bit baud rate generator with 13-bit reload capability, allowing baud rate generation independent of other timers.

The baud rate generator is clocked with a clock (f_{DIV}) which is derived via a prescaler from the ASC module clock f_{ASC}. The baud rate timer is counting downwards and can be started or stopped through the baud rate generator run bit CON.R. Each underflow of the timer generates one clock pulse to the serial channel. The timer is reloaded with the value stored in its 13-bit reload register at each underflow. The resulting clock f_{BRT} is again divided by a factor for the baud rate clock (÷ 16 in asynchronous operating modes and ÷ 4 in synchronous operating mode). The prescaler is selected by the bits CON.BRS and CON.FDE. In the asynchronous operating modes, a fractional divider prescaler unit is available (in addition to the two fixed dividers) that allows selection of prescaler divider ratios of n/512 with n = 0-511. Therefore, the baud rate of ASC is determined by the module clock, the content of register FDV, the reload value in register BG, and the operating mode (asynchronous or synchronous).

Register BG is the dual-function baud rate generator/reload register. Reading BG returns the contents of the timer in bit field BR_VALUE (bits 31:13 return zero), while writing to BG always updates the reload register (bits 31:13 are insignificant).

An auto-reload of the timer with the contents of the reload register is performed each time BG is written to. However, if CON.R = 0 at the time the write operation to BG is performed, the timer will not be reloaded until the first instruction cycle after CON.R = 1. For a clean baud rate initialization, BG should only be written if CON.R = 0. If BG is written with CON.R = 1, an unpredictable behavior of the ASC may occur during running transmit or receive operations.

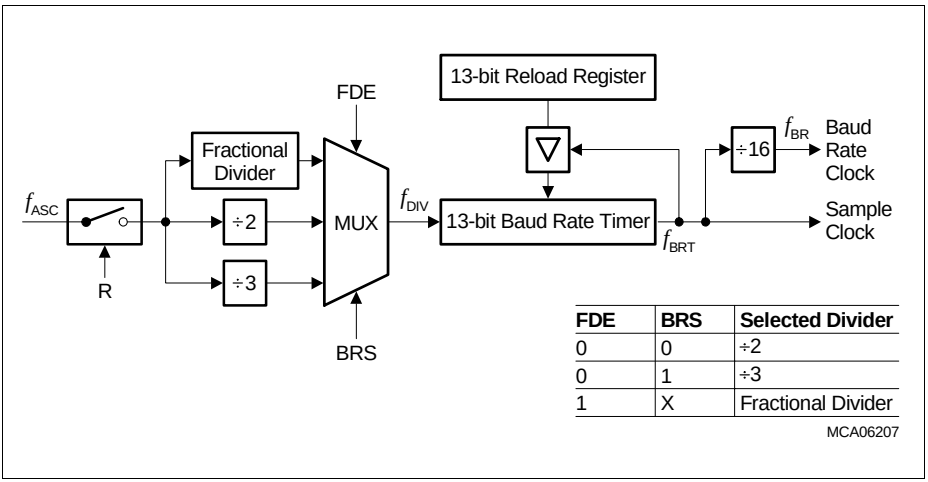
20.1.5.1 Baud Rates in Asynchronous Mode

For asynchronous operation, the baud rate generator provides a clock f_{BRT} with sixteen times the rate of the established baud rate. Every received bit is sampled on the 7th, 8th and 9th cycle of this clock. The clock divider circuitry, which generates the input clock f_{DIV} for the 13-bit baud rate timer, is extended by a fractional divider circuitry that allows the adjustment of more accurate baud rates and the extension of the baud rate range.

The baud rate of the baud rate generator depends on the settings of the following bits and register values:

- Input clock f_{ASC}
- Selection of the baud rate timer input clock f_{DIV} by bits CON.FDE and CON.BRS
- If bit CON.FDE = 1 (fractional divider): value of register FDV
- Value of the 13-bit reload register BG

The output clock of the baud rate timer with the reload register is the sample clock in the asynchronous operating modes of the ASC. For baud rate calculations, this baud rate clock f_{BR} is derived from the sample clock f_{BRT} by a division of sixteen.



FDE	BRS	Selected Divider
0	0	÷2
0	1	÷3
1	X	Fractional Divider

Figure 20-8 ASC Baud Rate Generator Circuitry in Asynchronous Modes

Using the Fixed Input Clock Divider

The baud rate for asynchronous operation of the serial channel ASC when using the fixed input clock divider ratios (CON.FDE = 0) and the required BG reload value for a given baud rate can be determined by the following formulas:

Table 20-1 Asynchronous Baud Rate Formulas using the Fixed Input Clock Dividers

FDE	BRS	BG	Formula
0	0	0 … 8191	$\text{Baud rate} = \frac{f_{ASC}}{32 \times (BG + 1)}$ $BG = \frac{f_{ASC}}{32 \times \text{Baud rate}} - 1$
	1		$\text{Baud rate} = \frac{f_{ASC}}{48 \times (BG + 1)}$ $BG = \frac{f_{ASC}}{48 \times \text{Baud rate}} - 1$

BG represents the content of the reload register bit field BG.BR_VALUE, taken as an unsigned 13-bit integer.

The maximum baud rate that can be achieved for the asynchronous operating modes when using the two fixed clock dividers and a module clock of 110 MHz is 3.4375 Mbit/s. **Table 20-2** lists various commonly used baud rates together with the required reload values and the deviation errors compared to the intended baud rate.

Table 20-2 Typical Asynchronous Baud Rates using Fixed Input Clock Dividers

Baud Rate	CON.BRS = 0, f_{ASC} = 110 MHz		CON.BRS = 1, f_{ASC} = 110 MHz	
	Deviation Error	Reload Value	Deviation Error	Reload Value
3.4375 Mbit/s	–	0000_H	–	–
19.2 kbit/s	+0.02% / -0.6%	$00B2_H$ / $00B3_H$	+0.3% / -0.6%	0076_H / 0077_H
9600 bit/s	+0.02% / -0.3%	0165_H / 0166_H	+0.3% / -0.1%	$00ED_H$ / $00EE_H$
4800 bit/s	+0.02% / -0.1%	$02CB_H$ / $02CC_H$	+0.1% / -0.1%	$01DC_H$ / $01DD_H$

Note: CON.FDE must be 0 to achieve the baud rates in the table above. The deviation errors given in the table are rounded. Using a baud rate crystal will provide correct baud rates without deviation errors.

Using the Fractional Divider

When the fractional divider is selected, the input clock f_{DIV} for the baud rate timer is derived from the module clock f_{ASC} by a programmable fractional divider. If CON.FDE = 1, the fractional divider is activated. It divides f_{ASC} by a fraction of n/512 for any value of n from 0 to 511. If n = 0, the divider ratio is 1, which means that $f_{DIV} = f_{ASC}$. In general, the fractional divider allows the baud rate to be programmed with much better accuracy than with the two fixed prescaler divider stages.

Note: In fractional divider mode, the clock f_{DIV} can have a maximum period jitter of one f_{ASC} clock period.

Table 20-3 Asynchronous Baud Rate Formulas using the Fractional Input Clock Divider

FDE	BRS	BG	FDV	Formula
1	–	0 … 8191	1 … 511	$\text{Baud rate} = \frac{FDV}{512} \times \frac{f_{ASC}}{16 \times (BG + 1)}$
			0	$\text{Baud rate} = \frac{f_{ASC}}{16 \times (BG + 1)}$

BG represents the content of the reload register bit field BG.BR_VALUE, taken as an unsigned 13-bit integer. FDV represents the contents of the fractional divider register bit field FDV.FD_VALUE, taken as an unsigned 9-bit integer.

Table 20-4 Typical Asynchronous Baud Rates using the Fractional Input Clock Divider

f_{ASC}	Desired Baud Rate	BG	FDV	Resulting Baud Rate	Deviation
110 MHz	115.2 kbit/s	$003A_H$	$1FA_H$	115.160 kbit/s	-0.04%
	57.6 kbit/s	0075_H	$1FA_H$	57.579 kbit/s	-0.04%

20.1.5.2 Baud Rates in Synchronous Mode

For synchronous operation, the baud rate generator provides a clock f_{BRT} that runs with four times the established baud rate (see **Figure 20-9**).

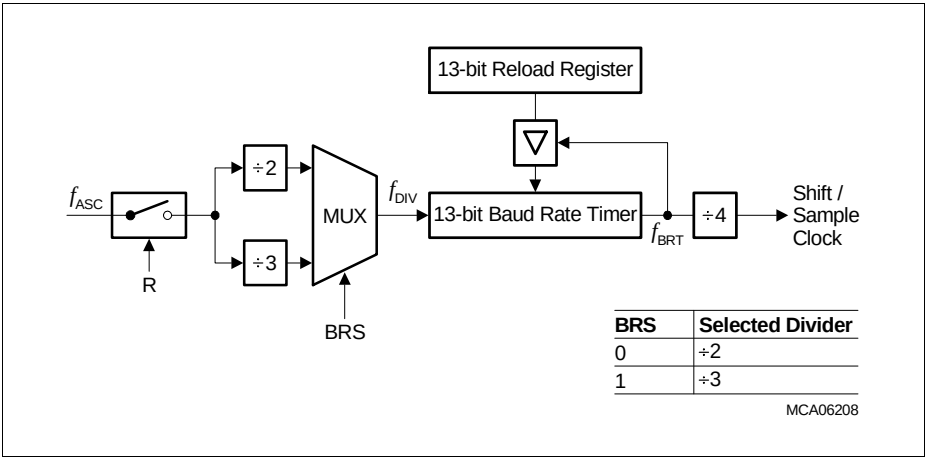


Figure 20-9 ASC Baud Rate Generator Circuitry in Synchronous Mode

The baud rate for synchronous operation of the serial channel ASC can be determined by the formulas as shown in **Table 20-5**.

Table 20-5 Synchronous Baud Rate Formulas

BRS	BG	Formula
0	0 … 8191	$\text{Baud rate} = \frac{f_{ASC}}{8 \times (BG + 1)}$ $\quad BG = \frac{f_{ASC}}{8 \times \text{Baud rate}} - 1$
1		$\text{Baud rate} = \frac{f_{ASC}}{12 \times (BG + 1)}$ $\quad BG = \frac{f_{ASC}}{12 \times \text{Baud rate}} - 1$

BG represents the content of the reload register bit field BG.BR_VALUE, taken as an unsigned 13-bit integer.

The maximum baud rate that can be achieved in Synchronous Mode when using a module clock of MHz is Mbit/s.

20.1.6 Hardware Error Detection Capabilities

To improve the reliability of serial data exchange, the serial channel ASC provides an error interrupt request flag that indicates the presence of an error and three (selectable) error status flags in register CON that indicate which error has been detected during reception. Upon completion of a reception, the error interrupt request line EIR will be activated simultaneously with the receive interrupt request line RIR, if one or more of the following conditions are met:

- If the framing error detection enable bit CON.FEN is set and any of the expected stop bits is not high, the framing error flag CON.FE is set, indicating that the error interrupt request is due to a framing error (asynchronous operating modes only).
- If the parity error detection enable bit CON.PEN is set in the modes where a parity bit is received and the parity check on the received data bits proves false, the parity error flag CON.PE is set, indicating that the error interrupt request is due to a parity error (asynchronous operating modes only).
- If the overrun error detection enable bit CON.OEN is set and the last character received was not read out of the receive buffer by software or DMA transfer at the time the reception of a new frame is complete, the overrun error flag CON.OE is set indicating that the error interrupt request is due to an overrun error (Asynchronous and Synchronous Modes).

20.1.7 Interrupts

Four interrupt sources are provided for serial channel ASC. Line TIR indicates a transmit interrupt, TBIR indicates a transmit buffer interrupt, RIR indicates a receive interrupt, and EIR indicates an error interrupt of the serial channel. The interrupt output lines TBIR, TIR, RIR, and EIR are activated (active state) for two periods of the module clock f_{ASC}.

The cause of an error interrupt request EIR (framing, parity, overrun error) can be identified by the error status flags CON.FE, CON.PE, and CON.OE.

Note: By contrast to the error interrupt request line EIR, the error status flags CON.FE/CON.PE/CON.OE are not reset automatically but must be cleared by software.

For normal operation (that is, other than error interrupt), the ASC provides three interrupt requests to control data exchange via this serial channel:

- TBIR is activated when data is moved from TBUF to the transmit shift register.
- TIR is activated before the last bit of an asynchronous frame is transmitted, or after the last bit of a synchronous frame has been transmitted.
- RIR is activated when the received frame is moved to RBUF.

While the task of the receive interrupt handler is quite clear, the transmitter is serviced by two interrupt handlers. This provides advantages for the servicing software.

For single transfers, it is sufficient to use the transmitter interrupt (TIR), which indicates that the previously loaded data has been transmitted, except for the last bit of an asynchronous frame.

For multiple back-to-back transfers, it is necessary to load the following piece of data at least before the last bit of the previous frame has been transmitted. In Asynchronous Mode, this leaves just one bit-time for the handler to respond to the transmitter interrupt request; in Synchronous Mode, it is entirely impossible.

Using the Transmit Buffer Interrupt (TBIR) to reload transmit data provides the time necessary to transmit a complete frame for the service routine, as TBUF may be reloaded while the previous data is still being transmitted.

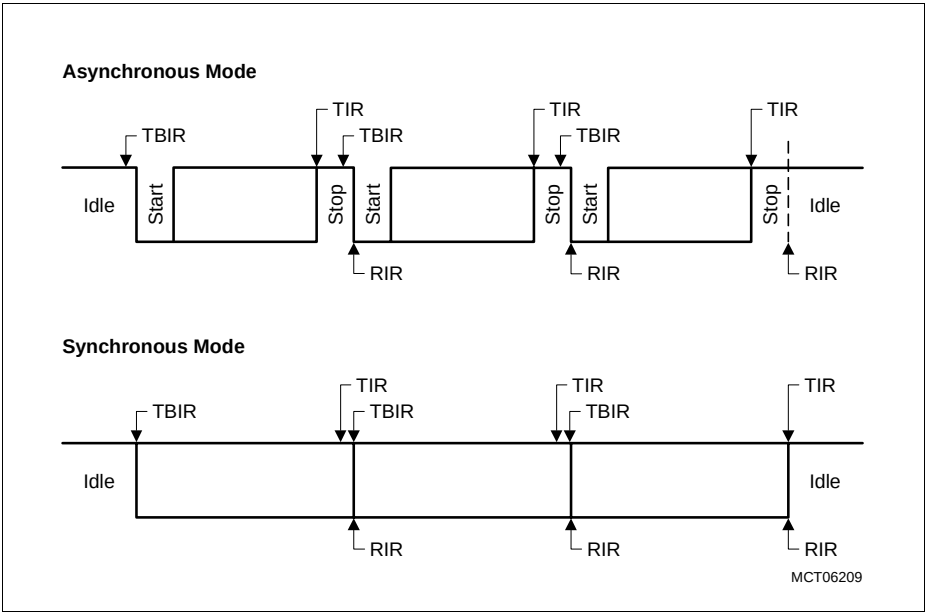


Figure 20-10 ASC Interrupt Generation

As shown in **Figure 20-10**, TBIR is an early trigger for the reload routine, while TIR indicates the completed transmission. Software using handshake should, therefore, rely on TIR at the end of a data block to ensure that all data has been transmitted.

20.2 ASC Kernel Registers

This section describes the kernel registers of the ASC module. All ASC kernel register names described in this section will be referenced in other parts of the TC1798 User´s Manual by the module name prefix “ASC0_” for the ASC0 interface and “ASC1_” for the ASC1 interface.

All registers in the ASC address spaces are reset with the application reset.

ASC Kernel Register Overview

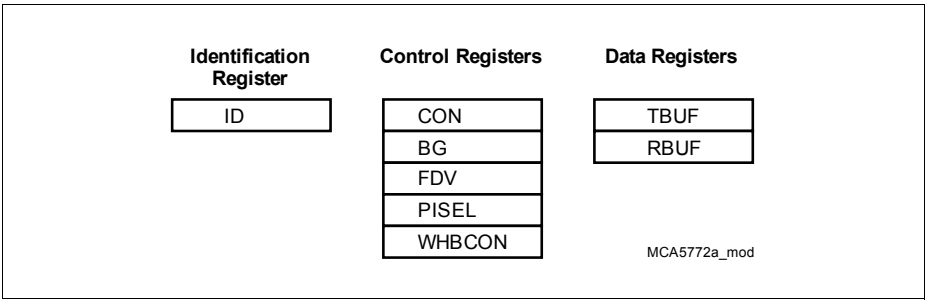


Figure 20-11 ASC Kernel Registers

The complete and detailed address map of the of the ASC module and its registers is described in **Table 20-10** on **Page 20-42**.

Table 20-6 Registers Address Space

Module	Base Address	End Address	Note
ASC0	F000 0A00$_H$	F000 0AFF$_H$	–
ASC1	F000 0B00$_H$	F000 0BFF$_H$	–

Table 20-7 Registers Overview - ASC Kernel Registers

Register Short Name	Register Long Name	Offset Address[1)]	Description see
PISEL	Peripheral Input Select Register	0004$_H$	**Page 20-20**
ID	Module Identification Register	0008$_H$	**Page 20-21**
CON	Control Register	0010$_H$	**Page 20-22**
BG	Baud Rate Timer Reload Register	0014$_H$	**Page 20-27**
FDV	Fractional Divider Register	0018$_H$	**Page 20-27**
TBUF	Transmit Buffer Register	0020$_H$	**Page 20-28**

Table 20-7 Registers Overview - ASC Kernel Registers (cont'd)

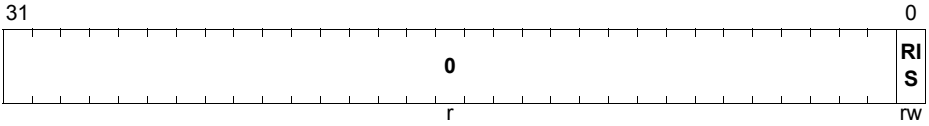
Register Short Name	Register Long Name	Offset Address[1)]	Description see
RBUF	Receive Buffer Register	0024_H	Page 20-29
WHBCON	Write Hardware Bits Control Register	0050_H	Page 20-25

1) The absolute register address is calculated as follows:
Module Base Address ((Table 20-6 on Page 20-19) + Offset Address (shown in this column)

20.2.1 Control Registers

The ASC module kernel provides two receive input lines, RXD_I0 and RXD_I1. Bit RIS in the Peripheral Input Select Register PISEL determines which of theses two input lines is taken for RXD receive input purposes.

PISEL
Peripheral Input Select Register (04_H) Reset Value: 0000 0000$_H$

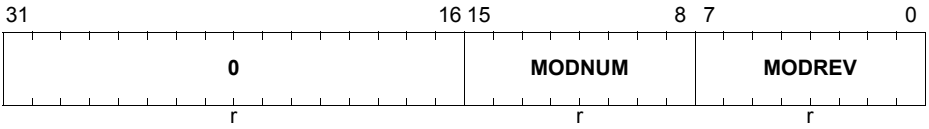


Field	Bits	Type	Description
RIS	0	rw	**Receive Input Select** 0_B ASC receiver input RXD_I0 selected 1_B ASC receiver input RXD_I1 selected
0	[31:1]	r	**Reserved** Read as 0; should be written with 0.

Note: Implementation specific details (RIS functionality) see "Peripheral Input Select Register" on Page 20-35.

The ASC Module Identification Register ID contains read-only information about the module version.

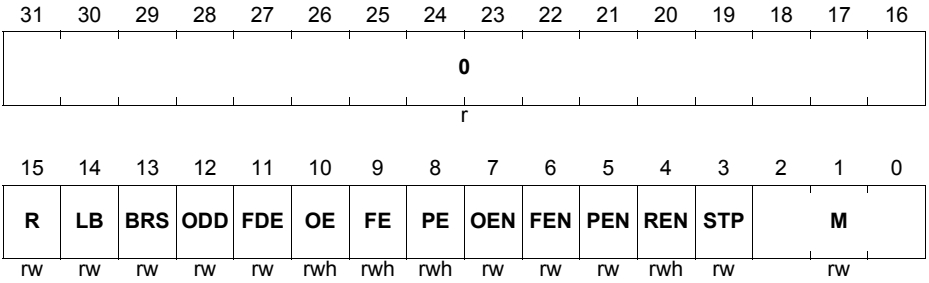
ID
Module Identification Register **(08_H)** **Reset Value: 0000 44XX$_H$**



Field	Bits	Type	Description
MODREV	[7:0]	r	**Module Revision Number** This bit field defines the module revision number. The value of a module revision starts with 01_H (first revision).
MODNUM	[15:8]	r	**Module Number Value** This bit field defines the module identification number for the ASC: 44_H
0	[31:16]	r	**Reserved** Read as 0.

The serial operating modes of the ASC module are controlled by its Control Register CON. This register contains control bits for mode and error check selection, and status flags for error identification.

CON
Control Register **(10_H)** **Reset Value: $0000\ 0000_H$**



Field	Bits	Type	Description
M	[2:0]	rw	**Mode Selection** 000_B 8-bit data Synchronous Mode 001_B 8-bit data Asynchronous Mode 010_B Reserved. Do not use this combination. 011_B 7-bit data + parity Asynchronous Mode 100_B 9-bit data Asynchronous Mode 101_B 8-bit data + wake up bit Asynchronous Mode 110_B Reserved. Do not use this combination. 111_B 8-bit data + parity Asynchronous Mode
STP	3	rw	**Number of Stop Bit Selection** 0_B One stop bit 1_B Two stop bits
REN	4	rwh	**Receiver Enable Control** 0_B Receiver disabled 1_B Receiver enabled Bit is reset by hardware after reception of a byte in Synchronous Mode.
PEN	5	rw	**Parity Check Enable (asynchronous mode only)** 0_B Ignore parity 1_B Check parity

Field	Bits	Type	Description
FEN	6	rw	**Framing Check Enable (asynchronous mode only)** 0_B Ignore framing errors 1_B Check framing errors
OEN	7	rw	**Overrun Check Enable** 0_B Ignore overrun errors 1_B Check overrun errors
PE	8	rwh	**Parity Error Flag** Set by hardware on a parity error (PEN = 1). Must be reset by software.
FE	9	rwh	**Framing Error Flag** Set by hardware on a framing error (FEN = 1). Must be reset by software.
OE	10	rwh	**Overrun Error Flag** Set by hardware on an overrun error (OEN = 1). Must be reset by software.
FDE	11	rw	**Fractional Divider Enable** 0_B Fractional divider disabled 1_B Fractional divider is enabled and used as prescaler for baud rate timer (bit BRS is don't care)
ODD	12	rw	**Parity Selection** 0_B Even parity selected (parity bit = 1 on odd number of 1s in data, parity bit = 0 on even number of 1s in data) 1_B Odd parity selected (parity bit = 1 on even number of 1s in data, parity bit = 0 on odd number of 1s in data)
BRS	13	rw	**Baud Rate Selection** 0_B Baud rate timer prescaler divide-by-2 selected 1_B Baud rate timer prescaler divide-by-3 selected BRS is don't care if FDE = 1 (fractional divider enabled)
LB	14	rw	**Loop-back Mode Enable** 0_B Loop-Back mode disabled 1_B Loop-Back mode enabled

Field	Bits	Type	Description
R	15	rw	**Baud Rate Generator Run Control** 0_B Baud rate generator disabled (ASC inactive) 1_B Baud rate generator enabled Register BG should only be written if R = 0.
0	[31:16]	r	**Reserved** Read as 0; should be written with 0.

Serial data transmission or reception is possible only when the run bit CON.R is set to 1. Otherwise, the serial interface is idle. To avoid unpredictable behavior of the serial interface, do not program the mode control field CON.M to one of the reserved combinations.

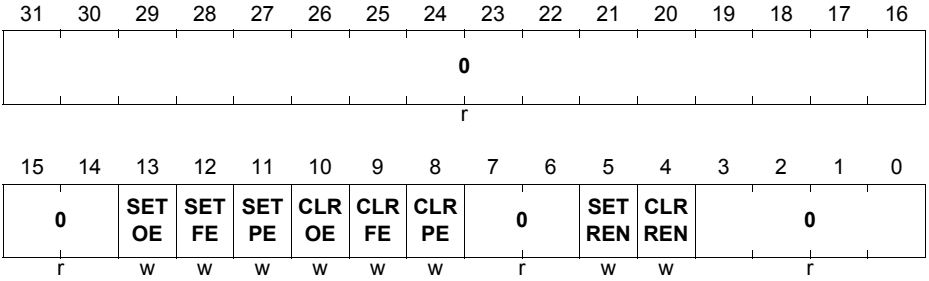
Critical “rwh” Bits

Register CON contains three error flags: PE, FE, and OE. If the software modifies only one of these error flags, it uses typically a Read-Modify-Write (RMW) instruction. When one of the other error flags that is not intended to be modified by the RMW instruction is changed by hardware after the read access but before the write back access of the RMW instruction, it is overwritten with the old bit value, and the hardware change of the bit gets lost. This problem does not affect the bits that are intended to be modified by the RMW instruction. It only affects bits that were not intended to be changed with the RMW instruction.

The three error flags in register CON and the REN bit can be additionally set or reset by software via register WHBCON. This capability avoids the problem with the CON register RMW instruction access to the error flags. WHBCON is a write-only register. Reading WHBCON always returns 0000 0000_H.

WHBCON

Write Hardware Bits Control Register (50_H) **Reset Value: $0000\ 0000_H$**



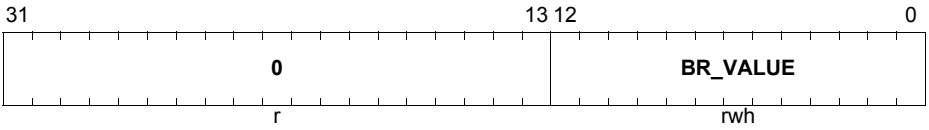
Field	Bits	Type	Description
CLRREN	4	w	**Clear Receiver Enable Bit** 0_B No effect 1_B Bit CON.REN is cleared. Bit is always read as 0.
SETREN	5	w	**Set Receiver Enable Bit** 0_B No effect 1_B Bit CON.REN is set. Bit is always read as 0.
CLRPE	8	w	**Clear Parity Error Flag** 0_B No effect 1_B Bit CON.PE is cleared. Bit is always read as 0.
CLRFE	9	w	**Clear Framing Error Flag** 0_B No effect 1_B Bit CON.FE is cleared. Bit is always read as 0.
CLROE	10	w	**Clear Overrun Error Flag** 0_B No effect 1_B Bit CON.OE is cleared. Bit is always read as 0.
SETPE	11	w	**Set Parity Error Flag** 0_B No effect 1_B Bit CON.PE is set. Bit is always read as 0.

Field	Bits	Type	Description
SETFE	12	w	**Set Framing Error Flag** 0_B No effect 1_B Bit CON.FE is set. Bit is always read as 0.
SETOE	13	w	**Set Overrun Error Flag** 0_B No effect 1_B Bit CON.OE is set. Bit is always read as 0.
0	[3:0], [7:6], [31:14]	r	**Reserved** Read as 0; should be written with 0.

Note: When the set and clear bits for an error flag are set at the same time during a WHBCON write operation (e.g SETPE = CLRPE = 1), the error flag in CON is not affected.

The Baud Rate Timer Reload Register BG of the ASC module contains the 13-bit reload value for the baud rate timer in Asynchronous and Synchronous Modes.

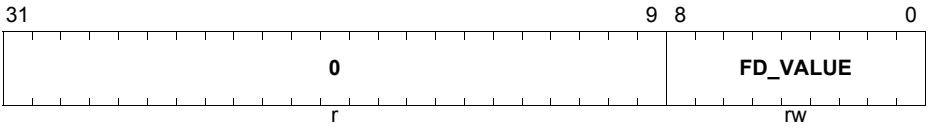
BG
Baud Rate Timer/Reload Register (14_H) Reset Value: 0000 0000$_H$



Field	Bits	Type	Description
BR_VALUE	[12:0]	rwh	**Baud Rate Timer/Reload Register Value** Reading BR_VALUE returns the 13-bit content of the baud rate timer. Writing BR_VALUE loads the baud rate timer reload register. BG should only be written if CON.R = 0.
0	[31:13]	r	**Reserved** Read as 0; should be written with 0.

The Fractional Divider Register FDV of the ASC module contains the 9-bit divider value for the fractional divider (asynchronous mode only).

FDV
Fractional Divider Register (18_H) Reset Value: 0000 0000$_H$

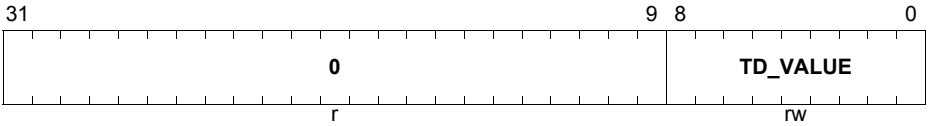


Field	Bits	Type	Description
FD_VALUE	[8:0]	rw	**Fractional Divider Register Value** FD_VALUE contains the 9-bit value n of the fractional divider which determines the fractional divider ratio n/512 (n = 0-511). With n = 0, the fractional divider is switched off (divider ratio = 1).
0	[31:9]	r	**Reserved** Read as 0; should be written with 0.

20.2.2 Data Registers

The Transmit Buffer Register TBUF of the ASC module contains the transmit data value in Asynchronous And Synchronous Modes.

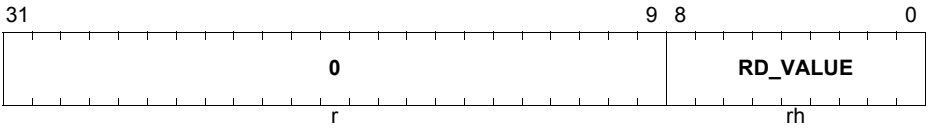
TBUF
Transmit Buffer Register **(20_H)** **Reset Value: 0000 0000_H**



Field	Bits	Type	Description
TD_VALUE	[8:0]	rw	**Transmit Data Register Value** TBUF contains the data to be transmitted in the asynchronous and synchronous operating modes of the ASC. Data transmission is double-buffered; therefore, a new value can be written to TBUF before the transmission of the previous value is complete.
0	[31:9]	r	**Reserved** Read as 0; should be written with 0.

The receive buffer register RBUF of the ASC module contains the receive data value in Asynchronous and Synchronous Modes.

RBUF
Receive Buffer Register **(24_H)** **Reset Value: 0000 0000$_H$**



Field	Bits	Type	Description
RD_VALUE	[8:0]	rh	**Receive Data Register Value** RBUF contains the received data bits and, depending on the selected mode, the parity bit in the asynchronous and synchronous operating modes of the ASC. In Asynchronous Mode, with CON.M = 011_B (7-bit data + parity), the received parity bit is written into RBUF.7. In Asynchronous Mode, with CON.M = 111_B (8-bit data + parity), the received parity bit is written into RBUF.8.
0	[31:9]	r	**Reserved** Read as 0.

20.3 ASC0/ASC1 Module Implementation

This section describes ASC0/ASC1 module interfaces with the clock control, port connections, interrupt control, and address decoding.

20.3.1 Interfaces of the ASC Modules

The serial I/O lines of both modules are connected either to Port 5 or Port 6. Each of the ASC modules is further supplied with interrupt control, address decoding, and port control logic. Two DMA requests can be generated by each ASC module. Both ASC modules are supplied by one common clock control unit.

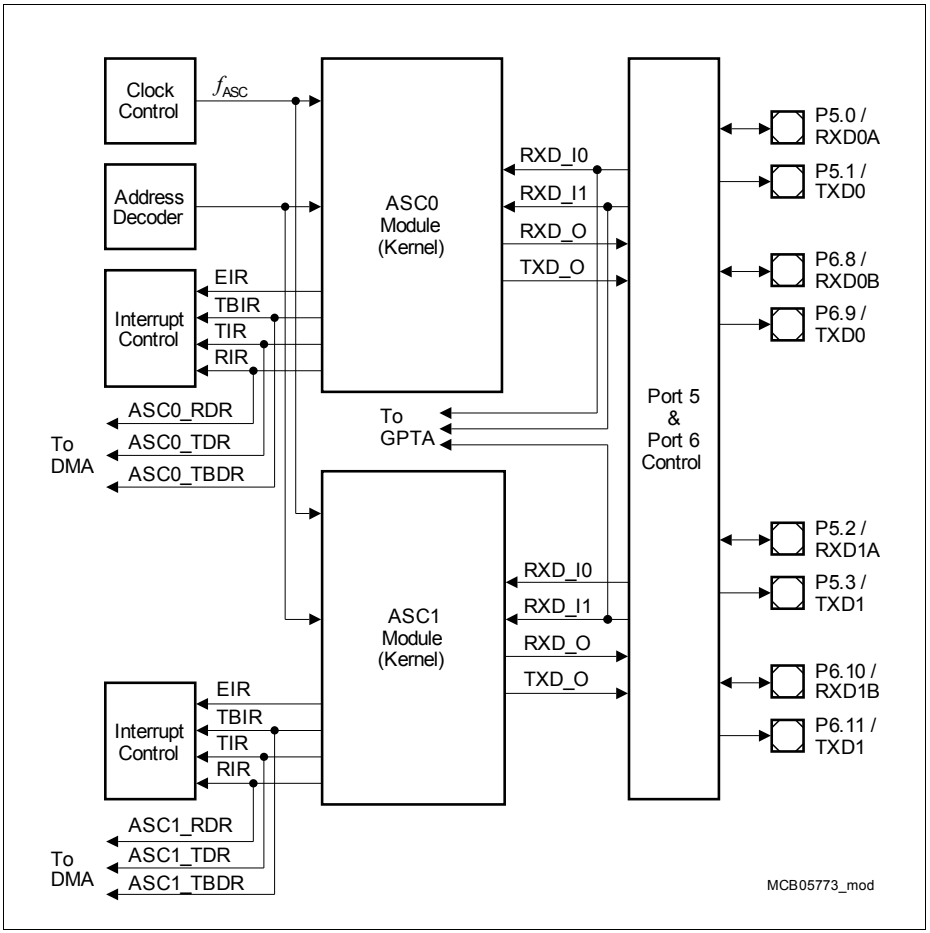


Figure 20-12 ASC0/ASC1 Module Implementation and Interconnections

Some of the receive inputs of the ASC0 and ASC1 are connected via a multiplexer to an LTC input of the GPTA module. Details are described in the SCU and the GPTA chapters.

20.3.2 ASC0/ASC1 Module Related External Registers

Figure 20-13 summarizes the module-related external registers which are required for ASC0/ASC1 programming (see also **Figure 20-11** for the module kernel-specific registers).

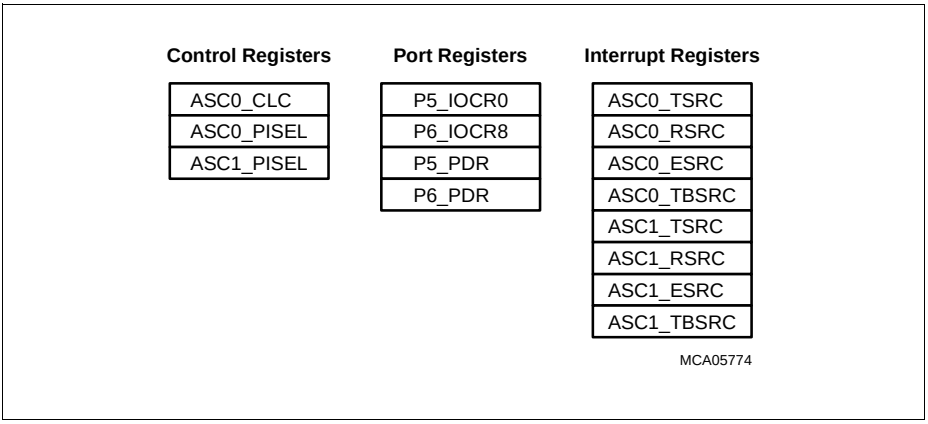


Figure 20-13 ASC0/ASC1 Implementation-specific Special Function Registers

20.3.2.1 Clock Control Register

The Clock Control Register ASC0_CLC allows the programmer to adapt the functionality and power consumption of the ASC modules to the requirements of the application. The description below shows the clock control register functionality which is implemented for the ASC modules. Because ASC0 and ASC1 share one common clock control interface, ASC0_CLC controls the f_{ASC} module clock signal, sleep mode, suspend mode and fast shut-off mode for both modules.

ASC0_CLC
ASC0 Clock Control Register **(00_H)** **Reset Value: 0000 0003$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RMC								0		FSOE	SBWE	EDIS	SPEN	DISS	DISR
rw								r		rw	w	rw	rw	r	rw

Field	Bits	Type	Description
DISR	0	rw	**Module Disable Request Bit** Used for enable/disable control of the module.
DISS	1	r	**Module Disable Status Bit** Bit indicates the current status of the module.
SPEN	2	rw	**Module Suspend Enable for OCDS** Used to enable the suspend mode.
EDIS	3	rw	**Sleep Mode Enable Control** Used to control module's sleep mode.
SBWE	4	w	**Module Suspend Bit Write Enable for OCDS** Determines whether SPEN and FSOE are write-protected.
FSOE	5	rw	**Fast Switch Off Enable** Used to switch off fast clock in Suspend Mode.
RMC	[15:8]	rw	**8-bit Clock Divider Value in RUN Mode**
0	[7:6], [31:16]	r	**Reserved** Read as 0; should be written with 0.

Note: After a hardware reset operation, the two ASC modules are disabled.

Note: The number of module clock cycles (wait states) which are required for a "destructive read" access (means: flags/bits are set/reset by one read access) to ASC module register depends on the selected CLC clock frequency, which is selected via bit field RMC in the CLC register. Therefore, increasing ASC0_CLC.RMC may result in a longer FPI Bus read cycle access time.

20.3.2.2 Peripheral Input Select Register

The ASC0/ASC1 modules include a peripheral input select registers that are used to switch the RXD input lines of the ASC0/ASC1 module kernels between different pairs of pins of Port 5 and Port 6 as shown in **Figure 20-14**. Register ASC0_PISEL controls the RXD input selection for ASC0, and ASC1_PISEL controls the RXD input selection for ASC1.

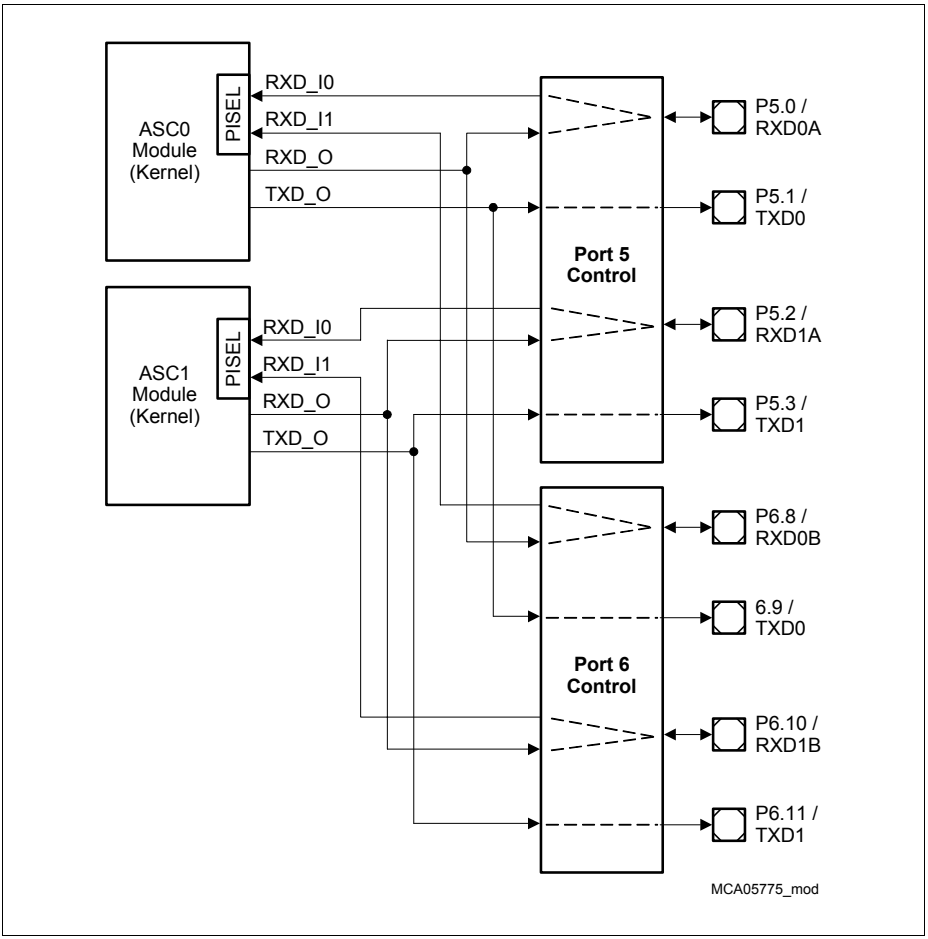
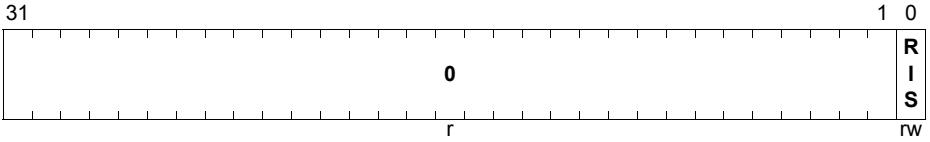


Figure 20-14 RXD Input Line Selection of the ASC Modules

ASC0_PISEL
ASC0 Peripheral Input Select Register

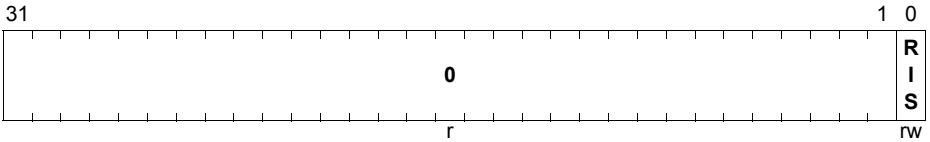
(04_H) **Reset Value: 0000 0000$_H$**



Field	Bits	Type	Description
RIS	0	rw	**Receive Input Select** 0_B ASC0 receiver input RXD0A (P5.0) selected 1_B ASC0 receiver input RXD0B (P6.8) selected
0	[31:1]	0	**Reserved** Read as 0; should be written with 0.

ASC1_PISEL
ASC1 Peripheral Input Select Register

(04_H) **Reset Value: 0000 0000$_H$**



Field	Bits	Type	Description
RIS	0	rw	**Receive Input Select** 0_B ASC1 receiver input RXD1A (P5.2) selected 1_B ASC1 receiver input RXD1B (P6.10) selected
0	[31:1]	0	**Reserved** Read as 0; should be written with 0.

20.3.2.3 Port Control Registers

As shown in **Figure 20-14**, the I/O lines of the ASC modules are connected to Class A2 port pins of Port 3. Additionally to the PISEL register programming, the required ASC port lines must be programmed by software for the desired ASC input/output functionality. Two selections must be executed:

- Input/output function selection
  (controlled by the port input/output control registers IOCR)
- Pad driver characteristics selection for the outputs
  (controlled by the port pad driver mode register PDR)

Input/Output Function Selection

The port input/output control registers contain the 4-bit wide bit fields that select the digital output and input driver characteristics such as pull-up/down devices, port direction (input/output), open-drain, and alternate output selections individually for each pin. The I/O lines for the ASC modules are controlled by the port input/output control registers P5_IOCR0 and P6_IOCR8.

Table 20-8 shows how bits and bit fields must be programmed for the required I/O functionality of the ASC I/O lines. This table also shows the values of the peripheral input select registers.

Table 20-8 ASC0/ASC1 I/O Control Selection and Setup

Module	Related ASC Interrupt	DMA Request Line	Description	I/O
ASC0	P5.0/RXD0A	ASC0_PISEL.RIS = 0	P5_IOCR0.PC0 = $0XXX_B$	Input
		–	P5_IOCR0.PC0 = $1X01_B$	Output[1)]
	P6.8/RXD0B	ASC0_PISEL.RIS = 1	P6_IOCR8.PC8 = $0XXX_B$	Input
		–	P6_IOCR8.PC8 = $1X10_B$	Output[1)]
	P5.1/TXD0	–	P5_IOCR0.PC1 = $1X01_B$	Output
	P6.9/TXD0		P6_IOCR8.PC9 = $1X10_B$	Output
ASC1	P5.2/RXD1A	ASC1_PISEL.RIS = 0	P5_IOCR0.PC2 = $0XXX_B$	Input
		–	P5_IOCR0.PC2 = $1X01_B$	Output[1)]
	P6.10/RXD1B	ASC1_PISEL.RIS = 1	P6_IOCR8.PC10 = $0XXX_B$	Input
		–	P6_IOCR8.PC10 = $1X10_B$	Output[1)]
	P5.3/TXD1	–	P5_IOCR0.PC3 = $1X01_B$	Output
	P6.11/TXD1		P6_IOCR8.PC11 = $1X10_B$	Output

1) Applicable in Synchronous Mode only.

*Note: In synchronous operating mode of the ASC, the type of the selected RXD port pin (input or output) is **not** automatically controlled by the ASC but must be defined by a user program by writing the appropriate bit field in the IOCR registers.*

20.3.2.4 Interrupt Control Registers

The eight interrupts of the ASC0 and ASC1 modules are controlled by the following service request control registers:

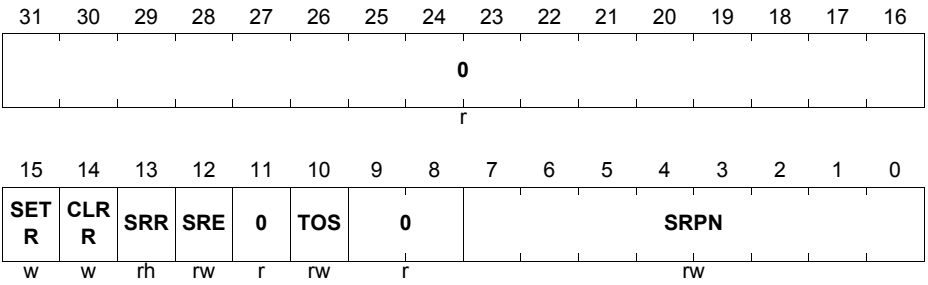
- ASC0_TSRC, ASC1_TSRC: control the transmit interrupts
- ASC0_RSRC, ASC1_RSRC: control the receive interrupts
- ASC0_ESRC, ASC1_ESRC: control the error interrupts
- ASC0_TBSRC, ASC1_TBSRC: control the transmit buffer empty interrupts

TSRC
Transmit Interrupt Service Request Control Register
($F0_H$) **Reset Value: 0000 0000$_H$**

RSRC
Receive Interrupt Service Request Control Register
($F4_H$) **Reset Value: 0000 0000$_H$**

ESRC
Error Interrupt Service Request Control Register
($F8_H$) **Reset Value: 0000 0000$_H$**

TBSRC
Transmit Buffer Interrupt Service Request Control Register
(FC_H) **Reset Value: 0000 0000$_H$**



Field	Bits	Type	Description
SRPN	[7:0]	rw	**Service Request Priority Number**
TOS	10	rw	**Type of Service Control**
SRE	12	rw	**Service Request Enable**
SRR	13	rh	**Service Request Flag**
CLRR	14	w	**Request Clear Bit**
SETR	15	w	**Request Set Bit**

Field	Bits	Type	Description
0	[9:8], 11, [31:16]	r	**Reserved** Read as 0; should be written with 0.

20.3.3 DMA Requests

The DMA request output lines of the ASC0/ASC1 modules become active whenever the related ASC interrupt line becomes activated. The DMA request lines are connected to the DMA controller as shown in **Table 20-9**.

Table 20-9 DMA Request Lines of ASC0/ASC1

Module	Related ASC Interrupt	DMA Request Line	Description
ASC0	RIR	ASC0_RDR	DMA Channel 00 Request Input 5
			DMA Channel 10 Request Input 5
			DMA Channel 06 Request Input 5
			DMA Channel 16 Request Input 5
	TIR	ASC0_TDR	DMA Channel 02 Request Input 5
			DMA Channel 12 Request Input 5
			DMA Channel 04 Request Input 5
			DMA Channel 14 Request Input 5
	TBIR	ASC0_TBDR	DMA Channel 02 Request Input 12
			DMA Channel 12 Request Input 12
			DMA Channel 04 Request Input 12
			DMA Channel 14 Request Input 12

Table 20-9 DMA Request Lines of ASC0/ASC1 (cont'd)

Module	Related ASC Interrupt	DMA Request Line	Description
ASC1	RIR	ASC1_RDR	DMA Channel 01 Request Input 5
			DMA Channel 11 Request Input 5
			DMA Channel 07 Request Input 5
			DMA Channel 17 Request Input 5
	TIR	ASC1_TDR	DMA Channel 03 Request Input 5
			DMA Channel 13 Request Input 5
			DMA Channel 05 Request Input 5
			DMA Channel 15 Request Input 5
	TBIR	ASC1_TBDR	DMA Channel 03 Request Input 12
			DMA Channel 13 Request Input 12
			DMA Channel 05 Request Input 12
			DMA Channel 15 Request Input 12

Note: Further details on DMA handling and processing are described in the chapter "DMA Controller" of the TC1798 System Units User´s Manual.

20.3.4 Address Map

An absolute register address is given by the offset address of the register (given in Table 20-7) plus the module base address (given in Table 20-6).

Table 20-10 Address Map of ASC0/ASC1

Short Name	Description	Address	Access Mode		Reset Value
			Read	Write	
Async./Sync. Serial Interface 0 (ASC0)					
ASC0_ CLC	ASC0 Clock Control Register	F000 0A00$_H$	U, SV	SV, E	0000 0003$_H$
ASC0_ PISEL	ASC0 Peripheral Input Select Register	F000 0A04$_H$	U, SV	U, SV	0000 0000$_H$
ASC0_ ID	ASC0 Module Identification Register	F000 0A08$_H$	U, SV	BE	0000 44XX$_H$
–	Reserved	F000 0A0C$_H$	BE	BE	–
ASC0_ CON	ASC0 Control Register	F000 0A10$_H$	U, SV	U, SV	0000 0000$_H$
ASC0_ BG	ASC0 Baud Rate/Timer Reload Register	F000 0A14$_H$	U, SV	U, SV	0000 0000$_H$
ASC0_ FDV	ASC0 Fractional Divider Register	F000 0A18$_H$	U, SV	U, SV	0000 0000$_H$
–	Reserved	F000 0A1C$_H$	BE	BE	–
ASC0_ TBUF	ASC0 Transmit Buffer Register	F000 0A20$_H$	U, SV	U, SV	0000 0000$_H$
ASC0_ RBUF	ASC0 Receive Buffer Register	F000 0A24$_H$	U, SV	U, SV	0000 0000$_H$
–	Reserved	F000 0A28$_H$ - F000 0A4C$_H$	BE	BE	–
ASC0_ WHBCON	ASC0 Write Hardware Bits Control Register	F000 0A50$_H$	U, SV	U, SV	0000 0000$_H$
–	Reserved	F000 0A54$_H$ - F000 0AEC$_H$	BE	BE	–
ASC0_ TSRC	ASC0 Transmit Interrupt Service Req. Control Reg.	F000 0AF0$_H$	U, SV	U, SV	0000 0000$_H$
ASC0_ RSRC	ASC0 Receive Interrupt Service Req. Control Reg.	F000 0AF4$_H$	U, SV	U, SV	0000 0000$_H$

Table 20-10 Address Map of ASC0/ASC1 (cont'd)

Short Name	Description	Address	Access Mode		Reset Value
			Read	Write	
ASC0_ ESRC	ASC0 Error Interrupt Service Req. Control Reg.	F000 0AF8$_H$	U, SV	U, SV	0000 0000$_H$
ASC0_ TBSRC	ASC0 Transmit Buffer Interrupt Service Req. Control Reg.	F000 0AFC$_H$	U, SV	U, SV	0000 0000$_H$
Async./Sync. Serial Interface 1 (ASC1)					
–	Reserved	F000 0B00$_H$	BE	BE	–
ASC1_ PISEL	ASC1 Peripheral Input Select Register	F000 0B04$_H$	U, SV	U, SV	0000 0000$_H$
ASC1_ ID	ASC1 Module Identification Register	F000 0B08$_H$	U, SV	BE	0000 44XX$_H$
–	Reserved	F000 0B0C$_H$	BE	BE	–
ASC1_ CON	ASC1 Control Register	F000 0B10$_H$	U, SV	U, SV	0000 0000$_H$
ASC1_ BG	ASC1 Baud Rate/Timer Reload Register	F000 0B14$_H$	U, SV	U, SV	0000 0000$_H$
ASC1_ FDV	ASC1 Fractional Divider Register	F000 0B18$_H$	U, SV	U, SV	0000 0000$_H$
–	Reserved	F000 0B1C$_H$	BE	BE	–
ASC1_ TBUF	ASC1 Transmit Buffer Register	F000 0B20$_H$	U, SV	U, SV	0000 0000$_H$
ASC1_ RBUF	ASC1 Receive Buffer Register	F000 0B24$_H$	U, SV	U, SV	0000 0000$_H$
–	Reserved	F000 0B28$_H$ - F000 0B4C$_H$	BE	BE	–
ASC1_ WHBCON	ASC1 Write Hardware Bits Control Register	F000 0B50$_H$	U, SV	U, SV	0000 0000$_H$
–	Reserved	F000 0B54$_H$ - F000 0BEC$_H$	BE	BE	–
ASC1_ TSRC	ASC1 Transmit Interrupt Service Req. Control Reg.	F000 0BF0$_H$	U, SV	U, SV	0000 0000$_H$
ASC1_ RSRC	ASC1 Receive Interrupt Service Req. Control Reg.	F000 0BF4$_H$	U, SV	U, SV	0000 0000$_H$

Table 20-10 Address Map of ASC0/ASC1 (cont'd)

Short Name	Description	Address	Access Mode		Reset Value
			Read	Write	
ASC1_ ESRC	ASC1 Error Interrupt Service Req. Control Reg.	F000 0BF8$_H$	U, SV	U, SV	0000 0000$_H$
ASC1_ TBSRC	ASC1 Transmit Buffer Interrupt Service Req. Control Reg.	F000 0BFC$_H$	U, SV	U, SV	0000 0000$_H$

20.3.5 Application Hint Regarding the ATM Feature

If the ASC0 is operated under certain conditions, the communication can be affected by the ATM functionality overlaid to the RXD0B pin.

The conditions are:

- ASC communication is using the pin where CAN RXDCAN0 is mapped to as well
- ASC protocol uses only one stop bit
- Start bit follows immediately after stop bit of previous data byte
- Block transfer with more than 100 bytes
- Data is 0xAA for all bytes
- ASC baud rate is higher than XTAL1 frequency / 14
  (for example, 1.42 Mbaud for a 20 MHz crystal)

There are two options to prevent the effect:

- Add a wait cycle between start and stop bit after 100 or less transferred bytes.
- Disable (temporarily) the ATM feature from within the SCU module
- Use 0x55, 0xAA55 or 0x55AA instead of 0xAA as fill or test data pattern

21 Synchronous Serial Interface (SSC)

This chapter describes the four SSC Synchronous Serial Interfaces SSC0, SSC1, SSC2 and SSC3 of the TC1798. It contains the following sections:

- Functional description of the SSC kernel, valid for SSC0, SSC1, SSC2 and SSC3 (see **Page 21-1**).
- SSC kernel register description, describes all SSC kernel specific registers (see **Page 21-27**).
- TC1798 implementation-specific details and registers of the SSC0/SSC1/SSC2 modules (port connections and control, interrupt control, address decoding, clock control, see **Page 21-43**).

*Note: The SSC kernel register names described in **Section 21.2** are referenced in the TC1798 User´s Manual by the module name prefix "SSC0_" for the SSC0 interface, by "SSC1_" for the SSC1 interface, and by "SSC2_" for the SSC2 interface.*

21.1 SSC Kernel Description

Figure 21-1 shows a global view of the SSC interface.

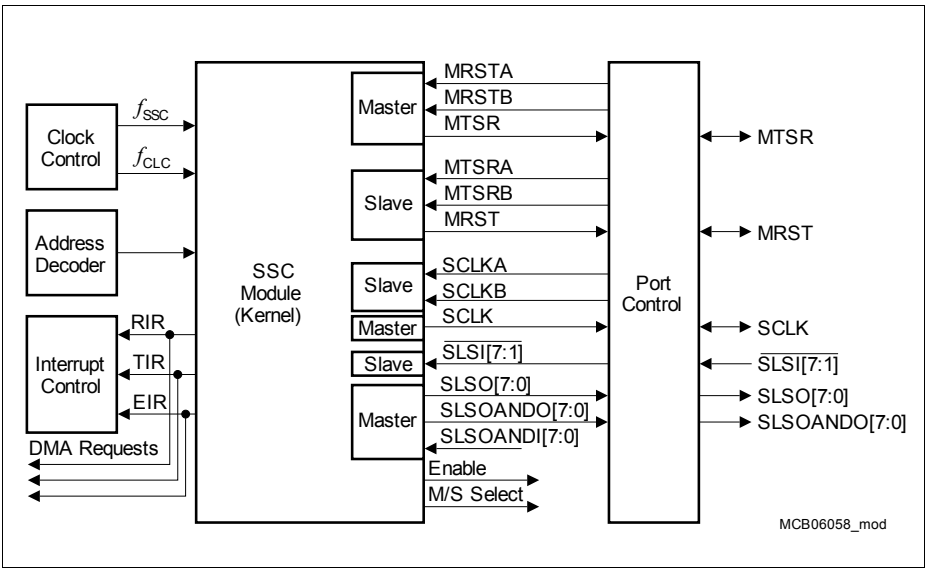


Figure 21-1 General Block Diagram of the SSC Interface

21.1.1 Overview

The SSC supports full-duplex and half-duplex serial synchronous communication up to 55.0 Mbit/s (@ 110.0 MHz module clock, Master Mode). The serial clock signal can be generated by the SSC itself (Master Mode) or can be received from an external master (Slave Mode). Data width, shift direction, clock polarity and phase are programmable. This allows communication with SPI-compatible devices. Transmission and reception of data is double-buffered. A shift clock generator provides the SSC with a separate serial clock signal. Seven slave select inputs are available for Slave Mode operation. Eight programmable slave select outputs (chip selects) are supported in Master Mode.

Features:

- Master and Slave Mode operation
  - Full-duplex or half-duplex operation
  - Automatic pad control possible
- Flexible data format
  - Programmable number of data bits: 2 to 16 data bits (with parity: 1 to 15 data bits)
  - Programmable shift direction: LSB or MSB shift first
  - Programmable clock polarity: Idle low or idle high state for the shift clock
  - Programmable clock/data phase: Data shift with leading or trailing edge of the shift clock
- Baud rate generation
  - Master Mode: 33.25 Mbit/s to 507.4 bit/s (@ 66.5 MHz module clock)
  - Master Mode: 55.0 Mbit/s to 839.3 bit/s (@ 110 MHz module clock)
  - Slave Mode: 16.625 Mbit/s to 507.4 bit/s (@ 66.5 MHz module clock)
  - Slave Mode: 27.5 Mbit/s to 839.3 bit/s (@ 110 MHz module clock)
- Interrupt generation
  - On a transmitter empty condition
  - On a receiver full condition
  - On an error condition (receive, phase, baud rate, transmit error, parity error)
- Queued SSC Mode supports control and data handling by the DMA controller
- Flexible SSC pin configuration
- Hardware supported parity mode
  - Individually selectable for transmit and receive frames
  - Even/odd parity selection
- Seven slave select inputs $\overline{\text{SLSI}}$[7:1] in Slave Mode
- Eight programmable slave select outputs SLSO[7:0] in Master Mode
  - Automatic SLSO generation with programmable timing
  - Programmable active level and enable control
  - Combinable with SLSO output signals from other SSC modules

21.1.2 General Operation

The SSC supports full-duplex and half-duplex synchronous communication up to 55.0 Mbit/s (@ 110.0 MHz module clock). The serial clock signal can be generated by the SSC itself (Master Mode) or be received from an external master (Slave Mode). Data width, shift direction, clock polarity and phase are programmable. This allows communication with SPI-compatible devices. Transmission and reception of data are double-buffered. A shift clock generator provides the SSC with a separate serial clock signal.

Configuration of the high-speed synchronous serial interface is very flexible, so it can work with other synchronous serial interfaces, can serve master/slave or multi-master interconnections, or can operate compatibly with the popular SPI interface. It can be used to communicate with shift registers (I/O expansion), peripherals (e.g. EEPROMs etc.), or other controllers (networking). The SSC supports half-duplex and full-duplex communication. Data is transmitted or received on pins MTSR (Master Transmit/Slave Receive) and MRST (Master Receive/Slave Transmit). The clock signal is output or input via pin SCLK (Serial Clock). These three pins are typically used for alternate output functions of port pins. If they are implemented as dedicated bi-directional pins, they can be directly controlled by the SSC. In Slave Mode, the SSC can be selected from a master via dedicated slave select input lines (SLSI). In Master Mode, automatic generation of slave select output lines (SLSO) is supported. In Master Mode, control and data handling of transfers can be also be controlled independently by the DMA controller (Queued SSC Mode).

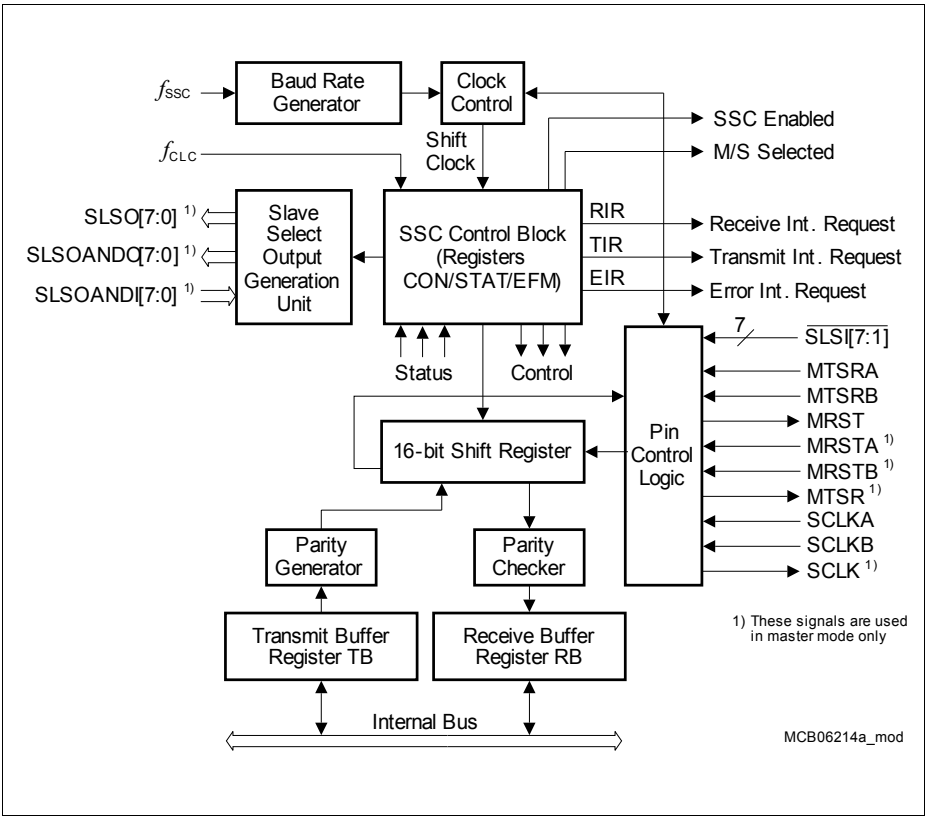


Figure 21-2 Synchronous Serial Channel SSC Block Diagram

21.1.2.1 Operating Mode Selection

The operating mode of the serial channel SSC is controlled by its Control Register, CON. Status information is contained in its Status Register, STAT.

The shift register of the SSC is connected to both the transmit pin and the receive pin via the pin control logic (see block diagram in **Figure 21-2**). Transmission and reception of serial data are synchronized and take place at the same time, that is, the same number of transmitted bits is also received. Transmit data is written into the Transmit Buffer TB. It is moved to the shift register as soon as this is empty, including the generated parity bit for the transmit data if transmit parity mode is enabled (CON.PARTEN = 1). An SSC master (CON.MS = 1) immediately begins transmitting, while an SSC slave (CON.MS = 0) will wait for an active shift clock. When the transfer starts, the busy flag STAT.BSY is set, and the transmit interrupt request line (TIR) will be activated to indicate that the Transmit Buffer Register (TB) may be reloaded. When the number of bits as programmed in CON.BM have been received, the data bits of the shift register are moved to the Receive Buffer Register (RB) right-aligned, the receive parity bit (if enabled by CON.PARREN = 1) is loaded into STAT.PARRVAL, and the receive interrupt request line (RIR) will be activated. If no further transfer is to take place (TB is empty), STAT.BSY will be cleared at the same time. Software should not modify STAT.BSY, as this flag is hardware-controlled.

Note: Only one SSC can be master at a given time.

The following features of the serial data bit transfer can be programmed:

- The data width can be selected from 2 to 16 data bits (with parity: 1 to 15 data bits)
- A transfer may start with the LSB or the MSB of the data bits
- The shift clock may be idle low or idle high
- The data bits may be shifted with the leading or trailing edge of the clock signal
- The baud rate (shift clock) can be set from 839.3 bit/s up to 55.0Mbit/s (@ 110 MHz module clock)
- The shift clock can be generated (master) or received (slave)

These features allow the SSC to be adapted to a wide range of applications that require serial data transfer.

The Data Width Selection supports the transfer of frames of any data length from 2-bit “characters” up to 16-bit “characters”. If parity is enabled, the maximum number of data bits of a frame is 15-bit.

Starting the serial data bit transfer with the LSB (CON.HB = 0) allows communication with devices such as an SSC device in Synchronous Mode, or 8051-like serial interfaces. If parity mode is enabled, the parity bit preceeds the serial data bit transfer (see **Page 21-12**).

Starting with the MSB (CON.HB = 1) allows operation compatible with the SPI interface. If parity mode is enabled, the parity bit follows the serial data bit transfer (see **Page 21-12**).

Regardless of the selected data width and whether the MSB or the LSB is transmitted first, the transfer data is always right-aligned in registers TB and RB, with the LSB of the transfer data in bit 0 of these registers. The data bits are rearranged for transfer by the internal shift register logic. The unselected bits of TB are ignored, and the unselected bits of RB will not be valid and should be ignored by the receiver service routine.

The Clock Control allows the adaptation of transmit and receive behavior of the SSC to a variety of serial interfaces. A specific clock edge (rising or falling) is used to shift out transmit data, while the other clock edge is used to latch in receive data. Bit CON.PH selects the leading edge or the trailing edge for each function. Bit CON.PO selects the level of the clock line in the idle state. For an idle-high clock, the leading edge is a falling one, a 1-to-0 transition (see **Figure 21-3**).

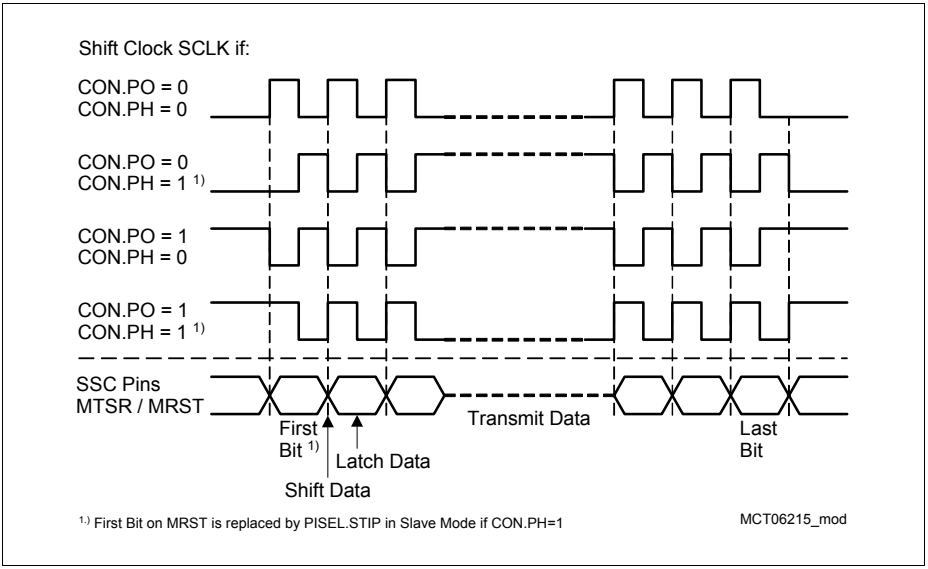


Figure 21-3 Serial Clock SCLK Phase and Polarity Options

21.1.2.2 Full-Duplex Operation

The description in this section assumes that the SSC is used with software controlled bi-directional GPIO port lines that have open-drain capability (see also **Section 21.1.2.6**).

The various devices are connected through three lines. The definition of these lines is always determined by the master. The line connected to the master's data output pin MTSR is the transmit line, the receive line is connected to its data input line MRST, and the clock line is connected to pin SCLK. Only the device selected for master operation generates and outputs the serial clock on pin SCLK. All slaves receive this clock, so their

pin SCLK must be switched to input mode. The output of the master's shift register is connected to the external transmit line, which in turn is connected to the slaves' shift register input. The output of the slaves' shift register is connected to the external receive line in order to enable the master to receive the data shifted out of the slave. The external connections are hard-wired, with the function and direction of these pins determined by the master or slave operation of the individual device.

*Note: The shift direction shown in **Figure 21-4** applies to both MSB-first and LSB-first operation.*

When initializing the devices in this configuration, one device must be selected for master operation while all other devices must be programmed for slave operation. Initialization includes the operating mode of the device's SSC and also the function of the respective port lines.

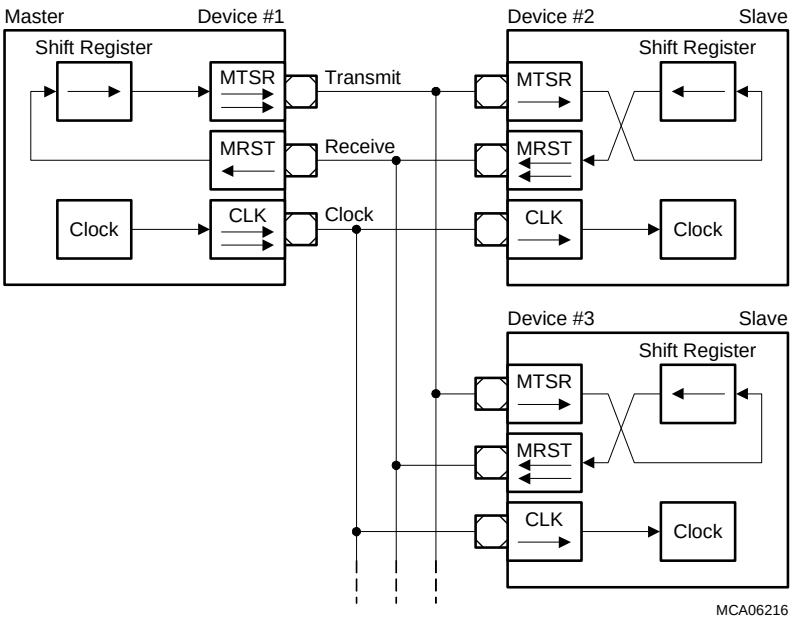


Figure 21-4 SSC Full-Duplex Configuration

The data output pins MRST of all slave devices are connected onto one receive line in this configuration. During a transfer, each slave shifts out data from its shift register. There are two ways to avoid collisions on the receive line due to different slave data:

- **Only one slave drives the line** and enables the driver of its MRST pin. All the other slaves must program their MRST pins to input. Therefore, only one slave can put its data onto the master's receive line. Only reception of data from the master is possible. The master selects the slave device from which it expects data either by separate select lines, or by sending a special command to this slave. The selected slave then switches its MRST line to output until it gets a de-selection signal or command.
- **The slaves use open drain output on MRST.** This forms a wired-AND connection. The receive line needs an external pull-up in this case. Corruption of the data on the receive line sent by the selected slave is avoided when all slaves not selected for transmission to the master send only 1s. Since this high level is not actively driven onto the line, but is only held through the pull-up device, the selected slave can pull this line actively to a low level when transmitting a zero bit. The master selects the slave device from which it expects data either by separate select lines, or by sending a special command to this slave.

After performing all necessary initializations of the SSC, the serial interfaces can be enabled. For a master device, the alternate clock line will now go to its programmed polarity. The alternate data line will go to either 0 or 1, until the first transfer starts. After a transfer, the alternate data line will always remain at the logic level of the last transmitted data bit.

When the serial interfaces are enabled, the master device can initiate the first data transfer by writing the transmit data into register TB. This value is copied into the shift register (assumed to be empty at this time), and the selected first bit of the transmit data will be placed onto the MTSR line on the next clock from the shift clock generator (transmission only starts, if CON.EN = 1). Depending on the selected clock phase, a clock pulse is generated on the SCLK line. With the opposite clock edge, the master simultaneously latches and shifts in the data detected at its input line MRST. This "exchanges" the transmit data with the receive data. Because the clock line is connected to all slaves, their shift registers will be shifted synchronously with the master's shift register, shifting out the data contained in the registers, and shifting in the data detected at the input line. After the pre-programmed number of clock pulses (via the data width selection), the data transmitted by the master is contained in all slaves' shift registers, while the master's shift register holds the data of the selected slave. In the master and all slaves, the content of the shift register is copied into the Receive Buffer (RB) and the receive interrupt line (RIR) is activated.

A slave device will immediately output the selected first bit (MSB or LSB of the transfer data) at pin MRST when the contents of the transmit buffer are copied into the slave's shift register. Bit STAT.BSY is not set until the first clock edge at SCLK appears. The slave device will not wait for the next clock from the shift clock generator – as the master does – because the first clock edge generated by the master may be already used to clock in the first data bit, depending on the selected clock phase. So the slave's first data bit must already be valid at this time.

*Note: On the SSC, a transmission **and** a reception always take place at the same time, regardless whether valid data has been transmitted or received.*

21.1.2.3 Half-Duplex Operation

The description in this section assumes that the SSC is used with software controlled bi-directional GPIO port lines that provide open-drain capability (see also **Section 21.1.2.6**).

In a half-duplex configuration, only one data line is necessary for both receiving **and** transmitting data. The data exchange line is connected to both pins MTSR and MRST of each device, and the clock line is connected to the SCLK pin.

The master device controls the data transfer by generating the shift clock, while the slave devices receive it. Due to the fact that all transmit and receive pins are connected to the one data exchange line, serial data may be moved between arbitrary stations.

As in full-duplex mode, there are two ways to avoid collisions on the data exchange line:

- Only the transmitting device may enable its transmit pin driver
- The non-transmitting devices use open-drain output and send only 1s

Because the data inputs and outputs are connected together, a transmitting device will clock in its own data at the input pin (MRST for a master device, MTSR for a slave). In this way, any corruption is detected on the common data exchange line when the received data is not equal to the transmitted data.

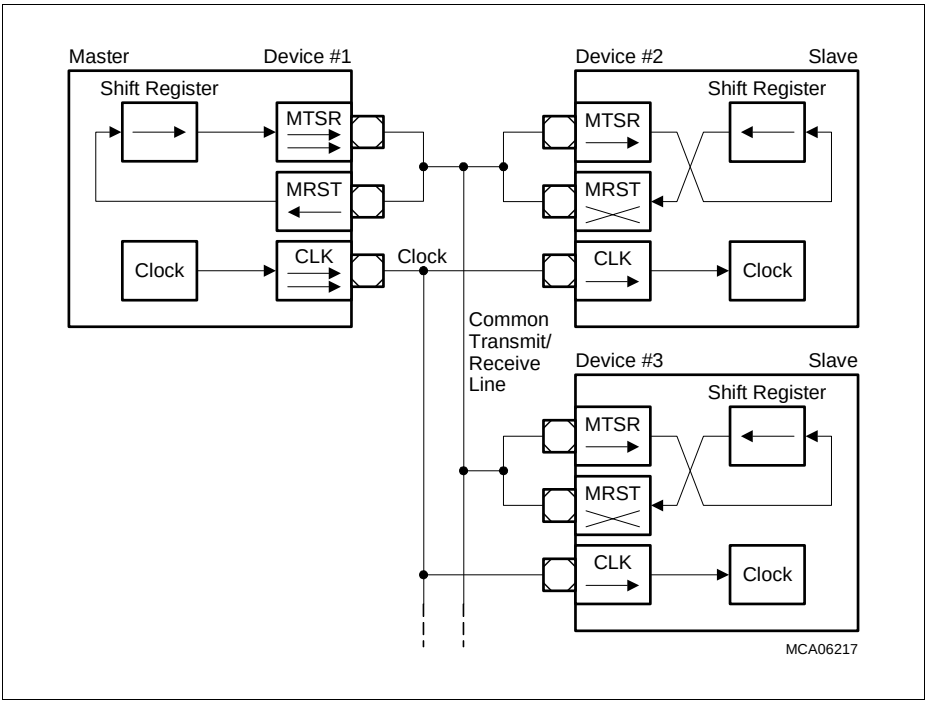


Figure 21-5 SSC Half-Duplex Configuration

21.1.2.4 Continuous Transfers

When the transmit interrupt request flag is set, it indicates that the Transmit Buffer (TB) is empty and is ready to be loaded with the next transmit data. If the TB has been reloaded by the time the current transmission is finished, the data is immediately transferred to the shift register and the next transmission can start without any additional delay (according to the selected SLSO timings). On the data line, there is no gap between the two successive frames if no delays are selected. For example, two byte transfers would look the same as one word transfer. This feature can be used to interface with devices that can operate with (or require more than) 16 data bits per transfer. It is just a matter for software how long a total data frame length can be. This option can also be used, e.g., to interface to byte-wide and word-wide devices on the same serial bus.

Note: This option can only happen in multiples of the selected basic data width, because it would require disabling/enabling of the SSC to reprogram the basic data width on-the-fly.

Note: In Master Mode, the Transmit Buffer register TB is loaded with new data for the following transmission just at the end of the current transmission and a leading delay > 0 is selected (SSOTC.LEAD not equal 00_B), a slightly enlarged leading delay (< one SCLK shift clock period) is generated for the following transmission.

21.1.2.5 Parity Mode

The SSC allows to add a parity bit to a serial frame. The parity mode can be enabled individually for frame transmission (CON.PARTEN) and frame reception (CON.PARREN). The type of parity (even/odd parity) can be selected, valid for transmit and receive parity.

If transmit parity is enabled (CON.PARTEN = 1), the shift register is loaded for a frame transmission by the content of the Transmit Buffer TB, the parity bit becomes calculated and stored in STAT.PARTVAL. Depending on bit CON.HB, the parity bit preceeds or follows the transmitted data bits.

If receive parity is enabled (CON.PARREN = 1) and the last bit of a frame has been received, the received data of the frame is stored in RB and the received parity bit is stored in STAT.PARRVAL. The received and calculated parity bits are now compared. If this comparison fails, a parity error is detected and the error status flag STAT.PARE is set. If enabled by bit CON.PAREEN, a parity error activates the error interrupt request line EIR.

Figure 21-6 shows how a parity bit is added to the transmitted data bits of a frame. The number of the transmitted bits of a complete frame remains constant without or with parity, assuming that COM.BM is not changed. Therefore, the number of transmitted data bits is reduced by one bit when parity mode is enabled.

If the heading control bit CON.HB = 0 (LSB first), the parity bit preceeds the data bits in parity mode and is transmitted as the first bit of a frame. If the heading control bit CON.HB = 1 (MSB first), the parity bit follows the data bits in parity mode and is transmitted as the last bit of a frame.

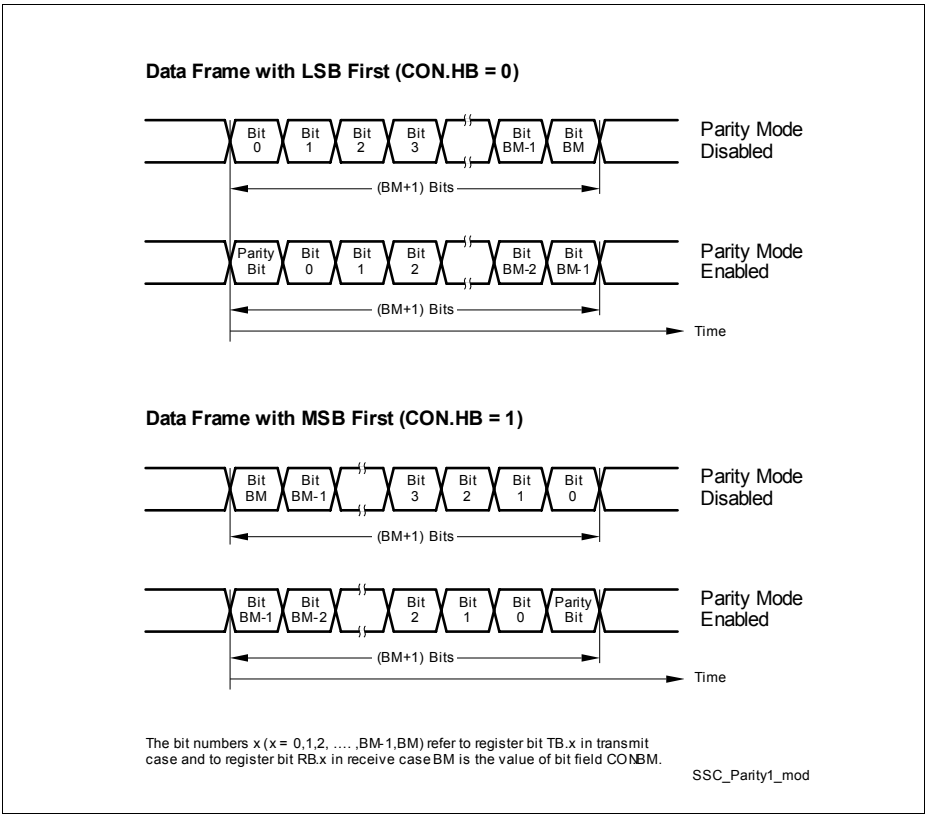


Figure 21-6 Data Frames without/with Parity

21.1.2.6 Port Control

The SSC uses three lines to communicate with the external world. Pin SCLK serves as the clock line, while pins MRST (Master Receive/Slave Transmit) and MTSR (Master Transmit/Slave Receive) serve as the serial data input/output lines. As shown in **Figure 21-1** these three lines (SCLK as input, Master Receive, Slave Receive) have two inputs each at the SSC Module kernel. Three bits in register PISEL determine which of the two kernel inputs (A or B) are connected. This feature allows for each of the three SSC communication lines to be connected to two inputs coming from different port pins.

Operation of the SSC I/O lines depends on the selected operating mode (master or slave). The direction of the port lines depends on the operating mode. The SSC will automatically use the correct kernel output or kernel input line of the ports when

switching modes. Port pins assigned as SSC I/O lines can be controlled either by hardware or by software.

When the SSC I/O lines are connected to dedicated pins, hardware I/O control should typically be used. In this case, two output signals reflect the state of the CON.EN and CON.MS bits directly (the M/S select line is inverted to the CON.MS bit definition).

When the SSC I/O lines are connected with bi-directional lines of general purpose I/O ports, software I/O control should be typically used. In this case port registers must be programmed for alternate output and input selection. When switching between master and slave mode port registers must be reprogrammed.

Using the open-drain output feature of port lines helps to avoid bus contention problems and reduces the need for hard-wired hand-shaking or slave select lines. In open-drain output mode, it is not always necessary to switch the direction of a port pin. Note that in hardware-controlled I/O mode, the availability of open-drain outputs depends on the type of the dedicated output pins that are used. The SSC module itself does not provide any control capability for open-drain control.

Note: For details of SSC port connections and configuration, see ***Page 21-53****.*

21.1.2.7 Baud Rate Generation

The serial channel SSC has its own dedicated 16-bit baud rate generator with 16-bit reload capability, allowing baud rate generation independent of timers. In addition to **Figure 21-2**, **Figure 21-7** shows the baud rate generator of the SSC in more detail.

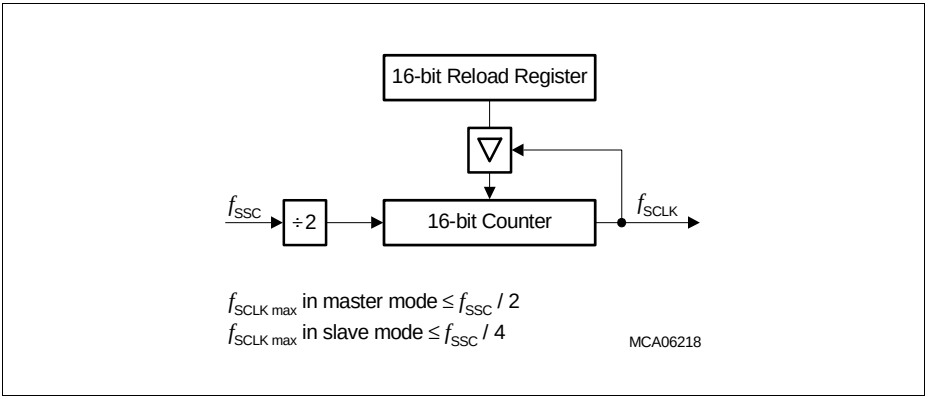


Figure 21-7 SSC Baud Rate Generator

The baud rate generator is clocked with f_{SSC}. The timer counts downwards. Register BR is the dual-function Baud Rate Generator/Reload register. Reading BR while the SSC is enabled returns the contents of the timer. Reading BR while the SSC is disabled returns the programmed reload value. In this mode, the desired reload value can be written to BR.

Note: Never write to BR while the SSC is enabled.

The formulas below calculate either the resulting baud rate for a given reload value, or the required reload value for a given baud rate:

$$\text{Baud rate}_{SSC} = \frac{f_{SSC}}{2 \times (\text{BR\_VALUE} + 1)} \qquad \text{BR\_VALUE} = \frac{f_{SSC}}{2 \times \text{Baud rate}_{SSC}} - 1 \qquad (21.1)$$

BR_VALUE represents the content of the reload register, taken as an unsigned 16-bit integer, while Baud rate_{SSC} is equal to f_{SCLK} as shown in **Figure 21-7**.

The maximum baud rate that can be achieved with f_{SSC} = 110 MHz is 55.0 Mbit/s in Master Mode (with BR_VALUE = 0000_H) and 275.0 Mbit/s in Slave Mode (with BR_VALUE = 0001_H).

Table 21-1 lists some possible baud rates together with the required reload values and the resulting bit times, assuming a module clock f_{SSC} of 110 MHz.

Table 21-1 Typical Asynchronous Baud Rates using Fixed Input Clock Dividers

Reload Value	Baud Rate (= f_{SCLK})	Deviation
0000_H	55 Mbit/s (only in Master Mode)	0.0%
0001_H	27.5 Mbit/s	0.0%
0003_H	13.75 Mbit/s	0.0%
0036_H	1 Mbit/s	0.0%
$006D_H$	500 kbit/s	0.0%
0225_H	100 kbit/s	0.0%
$157B_H$	10 kbit/s	0.0%
$D6D7_H$	1 kbit/s	0.0%
$FFFF_H$	839.3 bit/s	0.0%

In the TC1798, the module clock f_{SSC} is generated outside the SSC module kernel. Therefore, for baud rate calculations the dependencies of f_{SSC} from f_{FPI} must be taken into account. on describes these dependencies in detail.

21.1.2.8 Slave Select Input Operation

For systems with multiple slaves, the SSC module provides seven $\overline{SLSI}$ slave select input lines, that permit enabling or disabling of the SCLK, MTSR, and MRST signals in Slave Mode. Slave Mode is selected by CON.MS = 0. The $\overline{SLSI}$ input logic shown in **Figure 21-8** is controlled by register PISEL and CON.

Note: In the following description, only one of the seven $\overline{SLSI}$ input lines is mentioned. The remaining six $\overline{SLSI}$ input lines are connected to the other six inputs of the input multiplexer, which is controlled by PISEL.SLSIS.

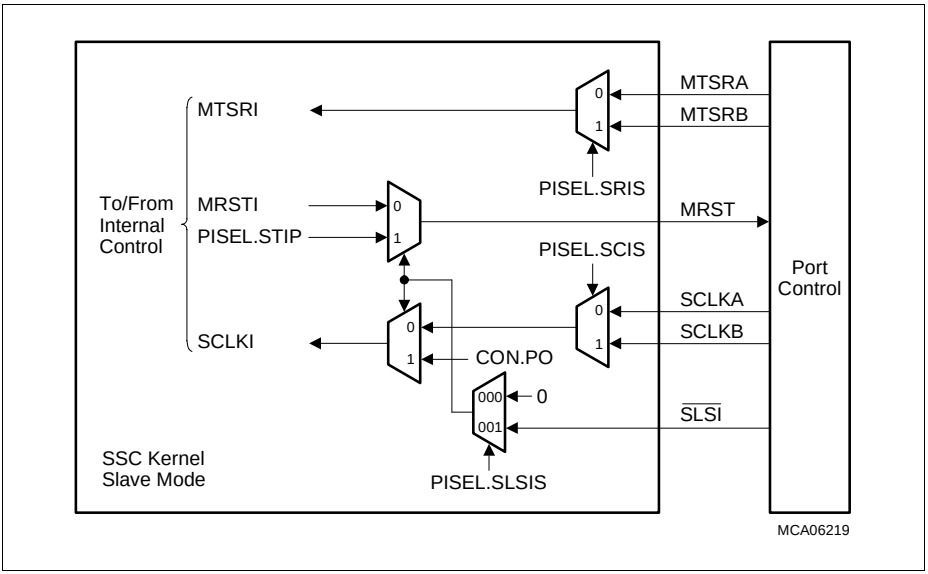


Figure 21-8 Slave Select Input Logic

With PISEL.SLSIS = 000_B and Slave Mode selected, the $\overline{SLSI}$ input line does not control the SSC I/O lines. The slave receive input signal MTSRA or MTSRB (selected by PISEL.SRIS) and the slave clock input signal SCLKA or SCLKB (selected by PISEL.SCIS) are passed further as MTRSI and SCLKI to the internal SSC control logic. The slave transmit signal MRSTI from the internal SSC control logic MRSTI is passed directly to MRST.

With PISEL.SLSIS = 001_B, input signal $\overline{SLSI}$ controls the operation of the SSC I/O lines as a slave select signal as follows:

- $\overline{SLSI}$ = 1: SSC slave is not selected.
  - The slave receive input signals, MTSRA or MTSRB are connected to MTSRI, depending on PISEL.SRIS (Slave Mode receive input select).

  - MRST is driven with the logic level of bit PISEL.STIP (slave transmit idle state).
  - SCLKI is driven with the logic level of CON.PO (clock polarity control).
- $\overline{SLSI}$ = 0: SSC is selected as slave.
  - The slave receive input signals MTSRA or MTSRB are connected to MTSRI, depending on PISEL.SRIS (Slave Mode receive input select).
  - MRST is directly driven with the slave transmit output signal MRSTI.
  - The slave clock input signals SCLKA or SCLKB are connected to SCLKI, depending on PISEL.SCIS (Slave Mode clock input select).

21.1.2.9 Slave Select Output Generation Unit

In Master Mode, the slave select output generation unit of the SSC automatically generates up to eight slave select output lines SLSO[7:0] for serial transmit operations. The slave select output generation unit further makes it possible to adjust the chip select timing parameters. The active/inactive state of a slave select output as well as the enable/disable state can be controlled individually for each slave select output (see **Figure 21-10**). The basic slave select output timing is shown in **Figure 21-9**, assuming a low active level of the SLSOn lines.

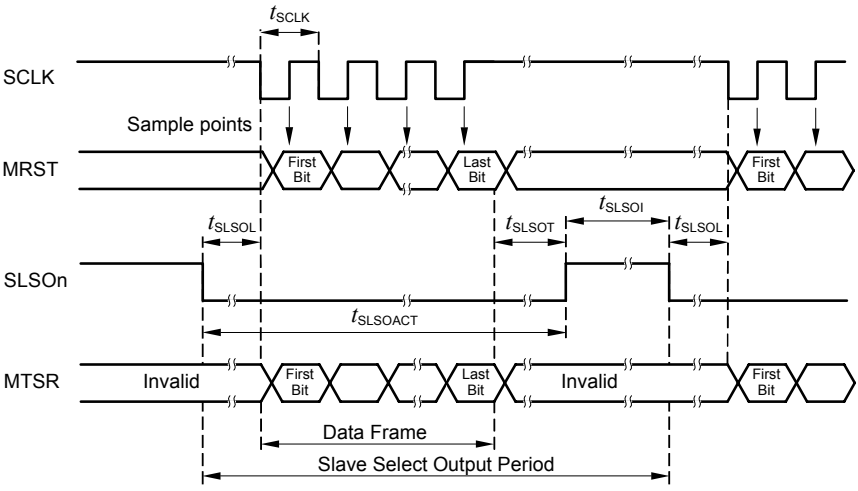


Figure 21-9 SSC Slave Select Output Timing

A slave select output period always starts after a write operation to register TB. With a TB write operation, all timing parameters stored in register SSOTC (LEAD, TRAIL,

INACT, and SLSO7MOD) and register SSOC (AOLn and OENn) are latched and remain valid for the consecutive transmission. Following that, SLSOn becomes active (low) for a number of SCLK cycles (leading delay cycles) before the first bit of the serial data stream occurs at MTSR. After the transmission of the data frame, SLSOn remains active (low) for a number of SCLK cycles (trailing delay cycles) before it becomes inactive again. This inactive state of SLSOn is valid at least for a number of SCLK cycles (inactive delay cycles) before a new chip select period can be started.

Note: When operating in Master Mode with CON.PH = 1 and sampling data from a slave device that becomes enabled by an SLSOn output, a leading delay of at least one leading delay clock cycle should be selected. The reason is that with CON.PH = 1, the first SCLK edge already latches the first data bit at MRST.

The three parameters of a chip select period are controlled by bit fields in the Slave Select Output Timing Control Register SSOTC. Each of these bit fields can contain a value from 0 to 3 defining delay cycles of 0 to 3 multiples of the t_{SCLK} shift clock period. The three parameters are:

1. Number of leading delay cycles (t_{SLSOL} = SSOTC.LEAD × t_{SCLK})
2. Number of trailing delay cycles (t_{SLSOT} = SSOTC.TRAIL × t_{SCLK})
3. Number of inactive delay cycles (t_{SLSOI} = SSOTC.INACT × t_{SCLK})

If SSOTC.INACT = 00_B and register TB has already been loaded with the data for the next data frame, the next chip select period is started with its leading delay phase without SLSOn going inactive. If, in this case, TB has not been loaded in time with the data for the next data frame, SLSOn becomes inactive again.

Slave Select Output Control

Each slave select output SLSOn can be enabled individually. When SSOC.OENn = 1, SLSOn is enabled. Furthermore, active and inactive levels of the SLSOn outputs are programmable. Bit SSOC.AOLn determines the state of the active level of SLSOn.

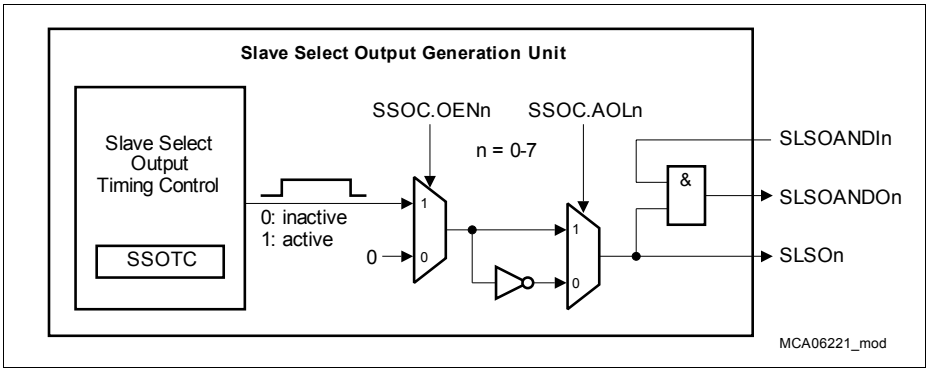


Figure 21-10 Slave Select Output Control Logic

As a special feature, each SLSOn output signal can be combined (ANDed) by an external signal SLSOANDIn coming from another SSC to an output signal SLSANDOn. This AND gate can be used for example to combine two slave select output signals from two SSCs to one common SLSOn output signal. Note that this functionality only works for low active SLSOn signals (SSOC.AOLn = 0).

Slave Select Output 7 Delayed Mode

In the SLSO7 delayed mode (SSOTC.SLSO7MOD = 1), the timing of the slave select output SLSO7 as programmed by the three parameters in SSOTC (number of trailing, leading, and inactive delay clock cycles) is delayed by one shift clock period for the inactive-to-active edge. The active-to-inactive edge is not delayed. The timing of SLSO7 in the delayed mode is shown in **Figure 21-11**. The bold lines show the timing of SLSO7 in normal operating mode, and the dotted lines show the timing of SLSO7 in delayed mode.

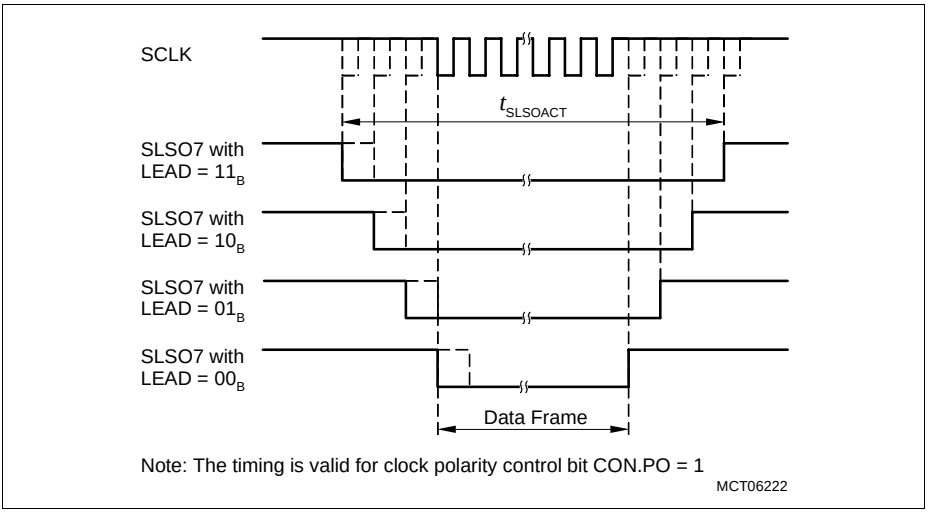


Figure 21-11 SLSO7 Delayed Mode

Slave Select Register Update

At the start of an internal transmit sequence (with the TB register write operation), the parameters in registers SSOC and SSOTC are latched. This means that they remain stable while a serial transmission is in progress. Therefore, it is always guaranteed that the data of one serial transmission is always transmitted with a constant slave select configuration setup. A configuration change by reprogramming SSOC or SSOTC during a serial transmission will first become valid with the start of the subsequent serial transmission.

21.1.2.10 Error Detection Mechanisms

The SSC is able to detect four different error conditions. Receive Error and Phase Error are detected in all modes, while Transmit Error and Baud Rate Error apply to Slave Mode only. In case of a Transmit Error or Receive Error, the respective error flags are always set and the error interrupt requests will be generated by activating the EIR line only if the corresponding error enable bits have been set (see **Figure 21-12**). The error interrupt handler may then check the error flags to determine the cause of the error interrupt. The error flags are not cleared automatically, but must be cleared via register EFM after servicing. This allows servicing of some error conditions via interrupt, while others may be polled by software. The error status flags can be set and cleared by software via the error flag modification register EFM.

Note: The error interrupt handler must clear the associated (enabled) error flag(s) to prevent repeated interrupt requests. The setting of an error flag by software does not generate an interrupt request.

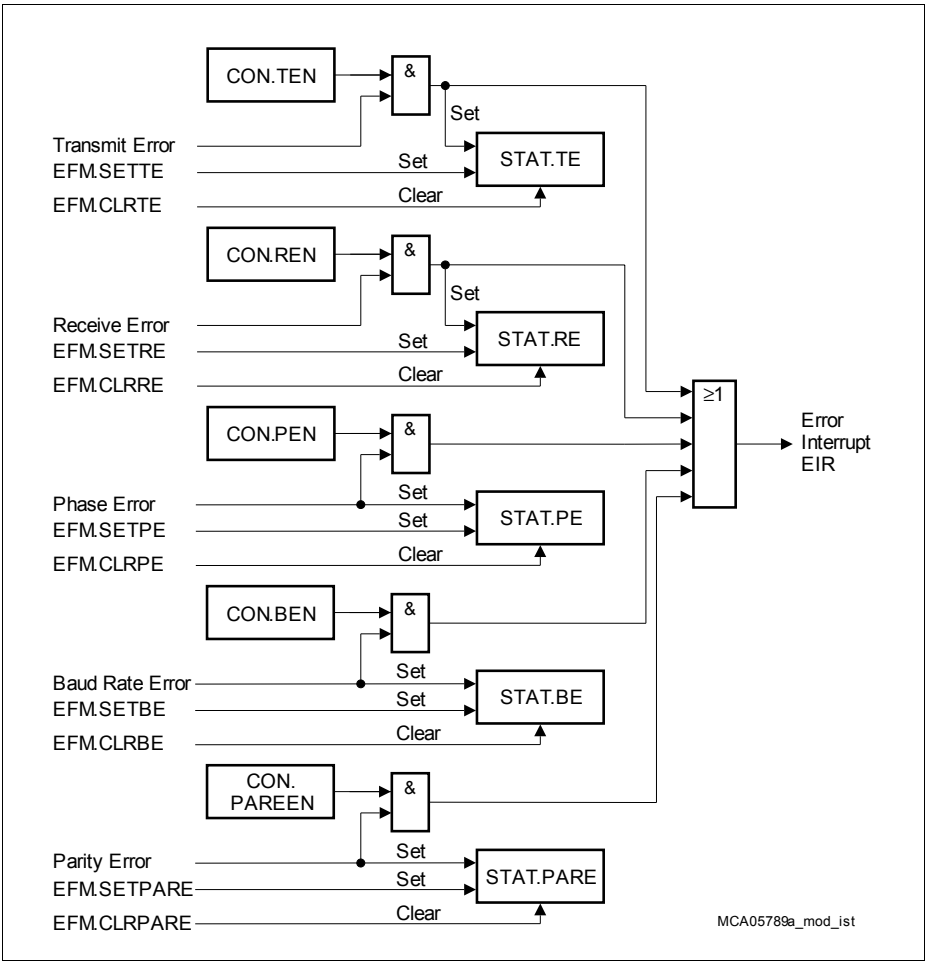


Figure 21-12 SSC Error Interrupt Control

A **Receive Error** (Master or Slave mode) is detected when a new data frame is completely received, but the previous data was not read out of the receive buffer register RB. If enabled via CON.REN, this condition sets the error flag STAT.RE and activates the error interrupt request line EIR. This condition sets the error flag STAT.RE and, if enabled via CON.REN, sets the error interrupt request line EIR. The old data in the receive buffer RB will be overwritten with the new value and is irretrievably lost.

A **Phase Error** (Master or Slave Mode) is detected when the incoming data at pin MRST (Master Mode) or MTSR (Slave Mode), sampled with the same frequency as the module

clock, changes between one cycle before and two cycles after the latching edge of the shift clock signal SCLK. This condition sets the error status flag STAT.PE and, if enabled via CON.PEN, the error interrupt request line EIR.

Note: When CON.PH = 1, the data output signal may be disturbed shortly when the slave select input signal is changed after a serial transmission, resulting in a phase error.

A **Baud Rate Error** (Slave Mode) is detected when the incoming clock signal deviates from the programmed baud rate (shift clock) by more than 100%, meaning it is either more than double or less than half the expected baud rate. This condition sets the error status flag STAT.BE and, if enabled via CON.BEN, the EIR line. Using this error detection capability requires that the slave's shift clock generator is programmed to the same baud rate as the master device. This feature detects false additional pulses or missing pulses on the clock line (within a certain frame).

Note: If this error condition occurs and bit CON.AREN = 1, an automatic reset of the SSC will be performed. This is done to re-initialize the SSC, if too few or too many clock pulses have been detected.

Note: The baud rate error can occur in slave mode after any transfer if the communication is stopped by the master. This is the case due to the fact that SSC module supports back-to-back transfers for multiple transfers. In order to handle this the baud rate detection logic expects after a finished transfer immediately a next clock cycle for a new transfer.

If baud rate error is enabled and the transmit buffer of the slave SSC is loaded with a new value for the next data frame while the current data frame is not yet finished (while STAT.BSY = 1), the slave SSC expects continuation of the clock pulses for the next data frame transmission immediately after finishing the current data frame. Any write to TBUF of the slave SSC while STAT.BSY = 1 initiates or sustains a continuous transmission in the slave. Therefore, the master (shift) clock must be continued after the current frame transmission. Otherwise, the slave SSC will detect a baud rate error. Note that the master SSC does not necessarily send out a continuous shift clock in the case that its transmit buffer is not yet filled with new data or transmission delays occur. Further details on continuous transfers are described in **Section 21.1.2.4** on **Page 21-10**.

A **Transmit Error** (Slave Mode) is detected when a transfer was initiated by the master (shift clock gets active), but the transmit buffer (TB) of the slave was not updated since the last transfer. If enabled via CON.TEN, this condition sets the error status flag STAT.TE and activates the EIR line. This condition sets the error status flag STAT.TE and, if enabled via CON.TEN, the EIR line. If a transfer starts while the transmit buffer is not updated, the slave will shift out the 'old' contents of the shift register, which is normally the data received during the last transfer. This may lead to the corruption of the data on the transmit/receive line in half-duplex mode (open drain configuration) if this slave is not selected for transmission. This mode requires that slaves not selected for

transmission only shift out ones; thus, their transmit buffers must be loaded with $FFFF_H$ prior to any transfer.

A **Parity Error** (Master or Slave Mode) is detected when the data frame is completely received and the generated parity bit for the received data is not equal to the calculated parity bit. This condition sets the error status flag STAT.PARE and, if enabled via CON.PAREEN, the error interrupt request line EIR.

Note: A slave with push/pull output drivers not selected for transmission will normally have its output drivers switched off. However, to avoid possible conflicts or misinterpretations, it is recommended to always load the slave's transmit buffer prior to any transfer.

The cause of an error interrupt request (receive, phase, baud rate, transmit error) can be identified by the error status flags in control register CON.

Note: In contrast to the EIR line, the error status flags STAT.TE, STAT.RE, STAT.PE, and STAT.BE, are not automatically cleared upon entry into the error interrupt service routine, but must be cleared by software.

21.1.2.11 Queued SSC Mode

In queued SSC mode, the enable/disable control of the SSC is possible by two bit locations, one control bit in register CON and one additional control bit in register SSOTC. This double-enable control capability allows control and data operations of the SSC to be completely handled by a DMA controller.

The bits for queued SSC mode are:

- Bit SSCTC.QSMEN: Queued SSC Mode Enable
- Bit SSCTC.EN: Enable SSC (functionality identical with bit CON.EN)

Table 21-2 Queued SSC Mode Control

Write SSOTC Register		SSC Module Enable/Disable Control	
Bit QSMEN	**Bit EN**		
0	X	Enable/disable control of SSC is only possible via bit CON.EN (queued SSC mode disabled).	
1	0	Enable/disable control of SSC is possible via bits SSOTC.EN and CON.EN (queued SSC mode enabled).	SSC is disabled
	1		SSC is enabled

Note: Both register bits, CON.EN and SSOTC.EN, control one common flip-flop for enable/disable control.

Figure 21-13 shows how the Queued SSC Mode control logic. Reading SSOTC returns the state of CON.EN for SSOTC.EN. Writing to SSOTC with QSMEN = 1, sets CON.EN if SSOTC.EN is written with 1 and clears CON.EN if SSOTC.EN is written with 0.

Compared to the timing parameters stored in register SSOTC (LEAD, TRAIL, INACT, and SLSO7MOD), the Queued SSC Mode control bits QSMEN and EN are a not latched and directly control the receive/transmit functionality. But note that CON.EN should only be cleared by software (either by a CON or SSOTC write operation) while no transfer is in progress (STAT.BSY = 0).

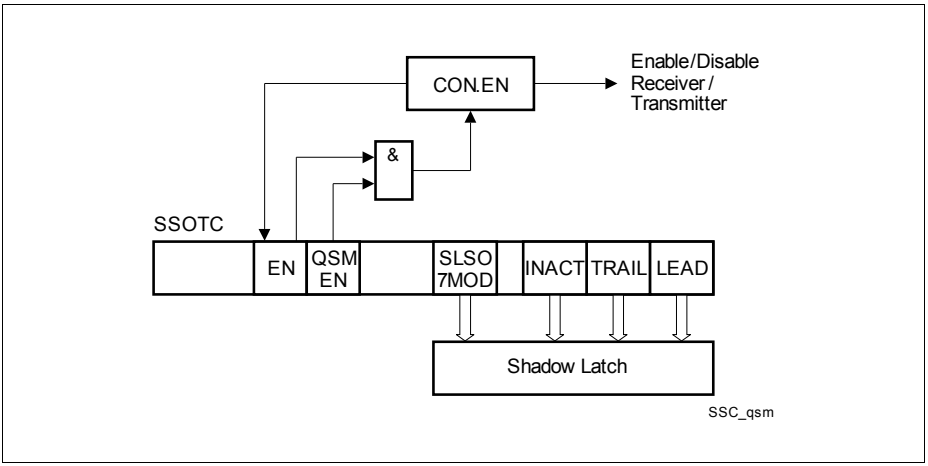


Figure 21-13 Queued SSC Mode Control

Application for Queued SSC Mode

Example: the SSC operates in master mode and controls multiple SSC slave devices with different frame settings and baud rates.

For controlling such an application task, that can be time critical when CPU is used for SSC control, the queued SSC mode is applicable. In this case, the control and data handling for an SSC slave is handled by three DMA channels.

- **DMA Channel 1**
  One DMA transaction consists of four consecutive DMA write transfers, programming registers CON, BR, SSOC, and SSOTC. All these registers are on consecutive addresses with an offset of 4.
  With the CON write operation, CON.EN is set to 0 (SSC disabled). The BR, SSOC, and SSOTC write operations program the SSC slave parameters such as baud rate, frame layout, and slave select output timing. The fourth write operation to SSOTC enables again the SSC by writing SSOTC.QSMEN = 1 and SSOTC.EN = 1. After DMA channel 1 has finished this 4-byte control setup transaction it can be programmed to start automatically data transactions via DMA channel 2 or 3 (depending on the application).
- **DMA Channel 2**
  This DMA channel is setup to write the transmit buffer register TB.
- **DMA Channel 3**
  This DMA channel is setup to read the receive buffer register RB.

Depending on the details of the application, the write or read DMA channel may be unnecessary.

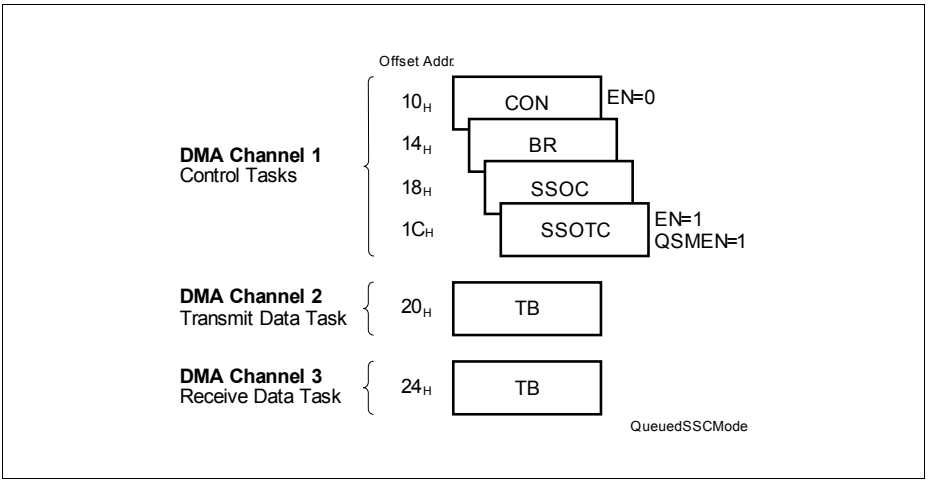


Figure 21-14 SSC Error Interrupt Control

21.2 SSC Kernel Registers

This section describes the kernel registers of the SSC module. All SSC kernel register names described in this section will be referenced in other parts of the TC1798 User´s Manual by the module name prefix “SSC0_” for the SSC0 interface and “SSC1_” for the SSC1 interface.

All registers in the SSC address spaces are reset with the application reset (definition see SCU section “Reset Operation”).

SSC Kernel Register Overview

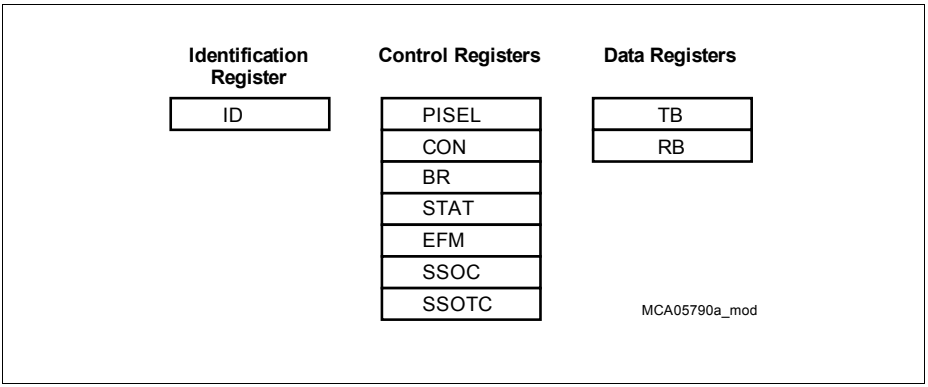


Figure 21-15 SSC Kernel Registers

The complete and detailed address map of the SSC modules is described at the end of this chapter.

Table 21-3 Registers Address Space - SSC Kernel Registers

Module	Base Address	End Address	Note
SSC0	$F031\ 0000_H$	$F031\ 00FF_H$	–
SSC1	$F031\ 0100_H$	$F031\ 01FF_H$	–
SSC2	$F031\ 0200_H$	$F031\ 02FF_H$	–
SSC3	$F031\ 0300_H$	$F031\ 03FF_H$	–

Table 21-4 Registers Overview - SSC Kernel Registers

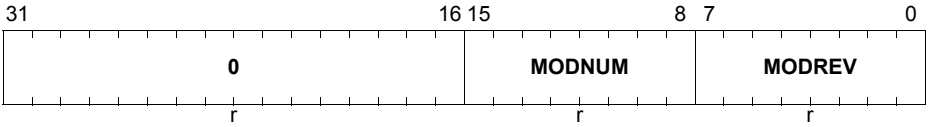
Register Short Name	Register Long Name	Offset Address[1)]	Description see
PISEL	Port Input Select Register	04_H	Page 21-29
ID	Module Identification Register	08_H	Page 21-28
CON	Control Register	10_H	Page 21-31
BR	Baud Rate Timer Reload Register	14_H	Page 21-41
STAT	Status Register	28_H	Page 21-34
EFM	Error Flag Modification Register	$2C_H$	Page 21-36
SSOC	Slave Select Output Control Register	18_H	Page 21-38
SSOTC	Slave Select Output Timing Control Register	$1C_H$	Page 21-39
TB	Transmit Buffer Register	20_H	Page 21-42
RB	Receive Buffer Register	24_H	Page 21-42

1) The absolute register address is calculated as follows:
Module Base Address (Table 21-3) + Offset Address (shown in this column)

21.2.1 Module Identification Register

The SSC Module Identification Register ID contains read-only information about the module version.

ID
Module Identification Register **(08_H)** **Reset Value: 0000 45XX$_H$**



Field	Bits	Type	Description
MODREV	[7:0]	r	**Module Revision Number** MODREV defines the module revision number. The value of a module revision starts with 01_H (first revision).
MODNUM	[15:8]	r	**Module Number Value** This bit field defines the module identification number for the SSC: 45_H

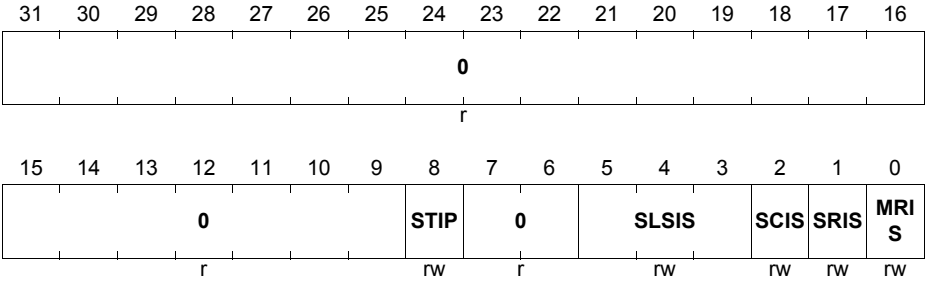
Field	Bits	Type	Description
0	[31:16]	r	**Reserved** Read as 0.

Note: Implementation specific details (e.g. reset value) see ***"Module Identification Registers" on Page 21-43****.*

21.2.2 Control Registers

The PISEL register controls the input signal selection of the SSC module. Each input of the module kernel receive, transmit and clock signals has associated two input lines (marked by suffix A and B).

PISEL
Port Input Select Register **(04_H)** **Reset Value: 0000 0000_H**



Field	Bits	Type	Description
MRIS	0	rw	**Master Mode Receive Input Select** MRIS selects the receive input line in Master Mode. 0_B Receive input line MRSTA is selected 1_B Receive input line MRSTB is selected
SRIS	1	rw	**Slave Mode Receive Input Select** SRIS selects receive input line in Slave Mode. 0_B Receive input line MTSRA is selected 1_B Receive input line MTSRB is selected
SCIS	2	rw	**Slave Mode Clock Input Select** SCIS selects the module kernel SCLK input line that is used as clock input line in slave mode. 0_B Slave Mode clock input line SCLKA is selected 1_B Slave Mode clock input line SCLKB is selected

Field	Bits	Type	Description
SLSIS	[5:3]	rw	**Slave Mode Slave Select Input Selection** 000_B Slave select input lines are deselected; SSC is operating without slave select input functionality. 001_B $\overline{SLSI}$ input line 1 is selected for operation. 010_B $\overline{SLSI}$ input line 2 is selected for operation. 011_B $\overline{SLSI}$ input line 3 is selected for operation. 100_B $\overline{SLSI}$ input line 4 is selected for operation. 101_B $\overline{SLSI}$ input line 5 is selected for operation. 110_B $\overline{SLSI}$ input line 6 is selected for operation. 111_B $\overline{SLSI}$ input line 7 is selected for operation. In the TC1798, other combinations of SLSIS except 000_B and 001_B are reserved and must not be used.
STIP	8	rw	**Slave Transmit Idle State Polarity** This bit determines the logic level of the Slave Mode transmit signal MRST when the SSC slave select input signals are inactive (PISEL.SLSIS $\neq 000_B$). 0_B MRST = 0 when SSC is deselected in Slave Mode. 1_B MRST = 1 when SSC is deselected in Slave Mode.
0	[7:6], [31:9]	r	**Reserved** Read as 0; should be written with 0.

The operating modes of the SSC are controlled by the Control Register CON. This register contains control bits for mode and error check selection.

Note: Whenever operating mode parameters in the CON register are changed by software, no transfer should be in progress (STAT.BSY = 0) and the SSC should be disabled (CON.EN = 0) and afterwards enabled again (CON.EN = 1).

CON
Control Register **(10_H)** **Reset Value: $0000\ 0000_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0												PAREEN	PARTYP	PARREN	PARTEN
r												rw	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EN	MS	0	AREN	BEN	PEN	REN	TEN	LB	PO	PH	HB	BM			
rw	rw	r	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw			

Field	Bits	Type	Description
BM	[3:0]	rw	**Frame Width Selection** BM determines the number of bits of the serial frame. PAREN = 0, parity mode disabled: 0000_B Reserved; do not use this combination. 0001_B Frame width is 2 bits (2 data bits). 0010_B Frame width is 3 bits (3 data bits). $\cdots_B$ ... 1110_B Frame width is 15 bits (15 data bits). 1111_B Frame width is 16 bits (16 data bits). PAREN = 1, parity mode enabled: 0000_B Reserved; do not use this combination. 0001_B Frame width is 2 bits (1 data bit + parity bit. 0010_B Frame width is 3 bits (2 data bits + parity bit). $\cdots_B$ ... 1110_B Frame width is 15 bits (14 data bits + parity bit). 1111_B Frame width is 16 bits (15 data bits + parity bit).

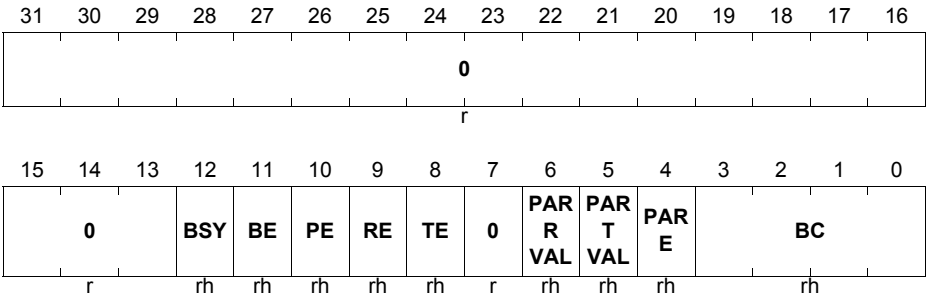
Field	Bits	Type	Description
HB	4	rw	**Heading Bit Control** 0_B Transmit/Receive LSB First 1_B Transmit/Receive MSB First
PH	5	rw	**Clock Phase Control** 0_B Shift transmit data on the leading clock edge, latch on trailing edge 1_B Latch receive data on leading clock edge, shift on trailing edge
PO	6	rw	**Clock Polarity Control** 0_B Idle clock line is low, the leading clock edge is low-to-high transition 1_B Idle clock line is high, the leading clock edge is high-to-low transition
LB	7	rw	**Loop-Back Control** 0_B Normal output 1_B Receive input is connected to transmit output (Half-duplex Mode)
TEN	8	rw	**Transmit Error Enable** 0_B Ignore transmit errors 1_B Check transmit errors
REN	9	rw	**Receive Error Enable** 0_B Ignore receive errors 1_B Check receive errors
PEN	10	rw	**Phase Error Enable** 0_B Ignore phase errors 1_B Check phase errors
BEN	11	rw	**Baud Rate Error Enable** 0_B Ignore baud rate errors 1_B Check baud rate errors
AREN	12	rw	**Automatic Reset Enable** 0_B No additional action upon a baud rate error 1_B SSC is automatically reset on a baud rate error

Field	Bits	Type	Description
MS	14	rw	**Master Select** 0_B Slave Mode. Operate on shift clock received via SCLK 1_B Master Mode. Generate shift clock and output it via SCLK The inverted state of this bit is available on module output line “M/S selected” (see **Figure 21-2**).
EN	15	rw	**Enable Bit** 0_B Transmission and reception are disabled. 1_B Transmission and reception are enabled. This bit is available as module output line “SSC enabled” (see **Figure 21-2**). Note that EN should only be cleared by software while no transfer is in progress (STAT.BSY = 0). Note that the transmission/reception enable can also be controlled in queued SSC mode by bit SSOTC.EN (see **Page 21-24**).
PARTEN	16	rw	**Parity Transmit Enable Bit** This bit enables the parity mode for the transmission of frames. 0_B Parity mode for transmission is disabled. 1_B Parity mode for transmission is enabled.
PARREN	17	rw	**Parity Receive Enable Bit** This bit enables the parity mode for the reception of frames. 0_B Parity mode for reception is disabled. 1_B Parity mode for reception is enabled.
PARTYP	18	rw	**Parity Type Bit** If PAREN = 1, this bit defines the type of parity to be generated or checked. 0_B Even parity is selected (parity bit = 1 on odd number of 1s in data, parity bit = 0 on even number of 1s in data). 1_B Odd parity selected (parity bit = 1 on even number of 1s in data, parity bit = 0 on odd number of 1s in data)
PAREEN	19	rw	**Parity Error Enable** 0_B Ignore receive parity errors 1_B Check receive parity errors

Field	Bits	Type	Description
0	13, [31:20]	r	**Reserved** Read as 0; should be written with 0.

The Status Register STAT contains status flags for error identification, the busy flag, and a bit field that indicates the current shift counter status.

STAT
Status Register **(28_H)** **Reset Value: 0000 0000$_H$**



Field	Bits	Type	Description
BC	[3:0]	rh	**Bit Count Status** BC indicates the current status of the shift counter. The shift counter is updated with every shifted bit.
PARE	4	rh	**Parity Error Flag** 0_B No error 1_B Received parity bit is wrong.
PARTVAL	5	rh	**Parity Transmit Value** If parity mode is enabled, this bit indicates the calculated parity bit for the transmission of the actual serial frame. PARTVAL is written with the transmit parity value when the shift register is loaded from TB. PARTVAL is reset when CON.PAREN is reset.
PARRVAL	6	rh	**Parity Receive Value** if parity mode is enabled, this bit PARRVAL is loaded when the received data is written into RB. PARRVAL is reset when CON.PAREN is reset.

Field	Bits	Type	Description
TE	8	rh	**Transmit Error Flag** 0_B No error 1_B Transfer starts with the slave's transmit buffer not being updated
RE	9	rh	**Receive Error Flag** 0_B No error 1_B Reception completed before the receive buffer was read
PE	10	rh	**Phase Error Flag** 0_B No error 1_B Received data changes during the sampling clock edge
BE	11	rh	**Baud Rate Error Flag** 0_B No error 1_B There is more than factor 2 or less than factor 0.5 between the slave's actual and the expected baud rate.
BSY	12	rh	**Busy Flag** BSY is set while a transfer is in progress.
0	7, [31:13]	r	**Reserved** Read as 0; should be written with 0.

The Error Flag Modification Register EFM is required for clearing or setting the four error flags which are located in register STAT.

EFM
Error Flag Modification Register (2C$_H$) Reset Value: 0000 0000$_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SETBE	SETPE	SETRE	SETTE	CLRBE	CLRPE	CLRRE	CLRTE	0			SETPARE	0			CLRPARE
w	w	w	w	w	w	w	w	r			w	r			w

Field	Bits	Type	Description
CLRPARE	0	w	**Clear Parity Error Flag** 0_B No effect 1_B Bit STAT.PARE is cleared. Bit is always read as 0.
SETPARE	4	w	**Set Parity Error Flag** 0_B No effect 1_B Bit STAT.PARE is set. Bit is always read as 0.
CLRTE	8	w	**Clear Transmit Error Flag** 0_B No effect 1_B Bit STAT.TE is cleared. Bit is always read as 0.
CLRRE	9	w	**Clear Receive Error Flag** 0_B No effect 1_B Bit STAT.RE is cleared. Bit is always read as 0.
CLRPE	10	w	**Clear Phase Error Flag** 0_B No effect 1_B Bit STAT.PE is cleared. Bit is always read as 0.

Field	Bits	Type	Description
CLRBE	11	w	**Clear Baud Rate Error Flag** 0_B No effect 1_B Bit STAT.BE is cleared. Bit is always read as 0.
SETTE	12	w	**Set Transmit Error Flag** 0_B No effect 1_B Bit STAT.TE is set. Bit is always read as 0.
SETRE	13	w	**Set Receive Error Flag** 0_B No effect 1_B Bit STAT.RE is set. Bit is always read as 0.
SETPE	14	w	**Set Phase Error Flag** 0_B No effect 1_B Bit STAT.PE is set. Bit is always read as 0.
SETBE	15	w	**Set Baud Rate Error Flag** 0_B No effect 1_B Bit STAT.BE is set. Bit is always read as 0.
0	[3:1], [7:5], [31:16]	r	**Reserved** Read as 0; should be written with 0.

Note: When the set and clear bits for an error flag are set at the same time during an EFM write operation (e.g SETPE = CLRPE = 1), the error flag in STAT is not affected.

The Slave Select Output Control Register controls the operation of the Chip Select Output Generation Unit.

SSOC

Slave Select Output Control Register (18_H) **Reset Value: $0000\ 0000_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

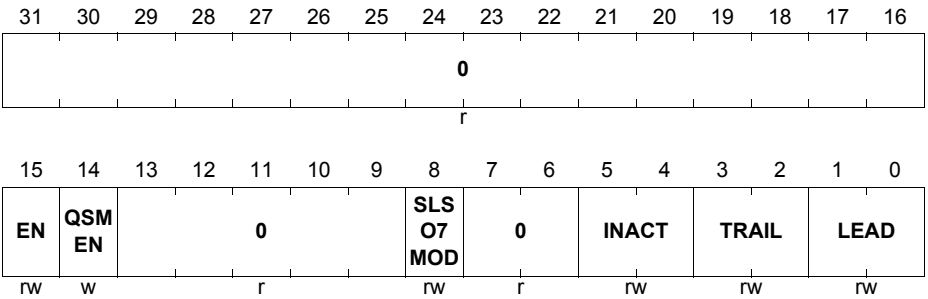
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OEN 7	OEN 6	OEN 5	OEN 4	OEN 3	OEN 2	OEN 1	OEN 0	AOL 7	AOL 6	AOL 5	AOL 4	AOL 3	AOL 2	AOL 1	AOL 0
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
AOLn (n = 0-7)	n	rw	**Active Output Level** 0_B SLSOn is at low level during the chip select active time $t_{SLSOACT}$. The high level is the inactive level of SLSOn. 1_B SLSO line n is at high level during the chip select active time $t_{SLSOACT}$. The low level is the inactive level of SLSOn.
OENn (n = 0-7)	8 + n	rw	**Output n Enable Control** 0_B SLSOn output is disabled; SLSOn is always at inactive level as defined by AOLn. 1_B SLSOn output is enabled.
0	[31:16]	r	**Reserved** Read as 0; should be written with 0.

Note: The SSOC register content is latched by each TB register write operation and remains latched during the consecutive serial transmission.

The Slave Select Output Timing Control Register controls the operation of the Slave Select Output Generation Unit.

SSOTC
Slave Select Output Timing Control Register
($1C_H$) **Reset Value: $0000\ 0000_H$**



Field	Bits	Type	Description
LEAD	[1:0]	rw	**Slave Output Select Leading Delay** This bit field determines the number of leading delay clock cycles. A leading delay clock cycle is always a multiple of an SCLK shift clock period. 00_B Zero leading delay clock cycle selected[1)] 01_B One leading delay clock cycle selected 10_B Two leading delay clock cycles selected 11_B Three leading delay clock cycles selected
TRAIL	[3:2]	rw	**Slave Output Select Trailing Delay** This bit field determines the number of trailing delay clock cycles. A trailing delay clock cycle is always a multiple of an SCLK shift clock period. 00_B Zero trailing delay clock cycle selected[1)] 01_B One trailing delay clock cycle selected 10_B Two trailing delay clock cycles selected 11_B Three trailing delay clock cycles selected

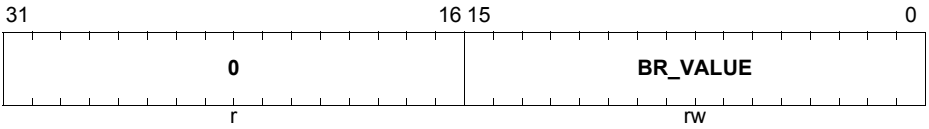
Field	Bits	Type	Description
INACT	[5:4]	rw	**Slave Output Select Inactive Delay** This bit field determines the number of inactive delay clock cycles. An inactive delay clock cycle is always a multiple of an SCLK shift clock period. 00_B Zero inactive delay clock cycle selected[1)] 01_B One inactive delay clock cycle selected 10_B Two inactive delay clock cycles selected 11_B Three inactive delay clock cycles selected
SLSO7MOD	8	rw	**SLSO7 Delayed Mode Selection** This bit selects the delayed mode for the SLSO7 slave select output. 0_B Normal mode selected for SLSO7 1_B Delayed mode selected for SLSO7
QSMEN	14	w	**Queued SSC Mode Enabled** 0_B When QSMEN is written with 0, the state of bit SSOTC.EN is don't care. In this case, the enable/disable of the SSC is controlled by bit CON.EN only. Note that EN should only be cleared by software while no transfer is in progress (STAT.BSY = 0). 1_B When QSMEN is written with 1, queued SSC mode is enabled, and the state of bit SSOTC.EN is copied to CON.EN. QSMEN is always read as 0.
EN	15	rw	**Enable Bit** 0_B Transmission and reception are disabled. 1_B Transmission and reception are enabled. Note that the transmission/reception enable can also be controlled in queued SSC mode by bit CON.EN.
0	[7:6], [13:9], [31:16]	r	**Reserved** Read as 0; should be written with 0.

1) For getting a best case timing with no timing delays (see **Figure 21-9**), this bit field value should be set when the SLSOn outputs are disabled (SSOC.OENn bits set to 0).

Note: The SSOTC register timing parameters LEAD, TRAIL, INACT, and SLSO7MOD are latched by each TB register write operation and remain latched during a consecutive serial transmission. Bits QSMEN and EN of register SSOTC are not latched.

The Baud Rate Timer Reload Register BR contains the 16-bit reload value for the baud rate timer.

BR
Baud Rate Timer Reload Register (14_H) Reset Value: 0000 0000_H

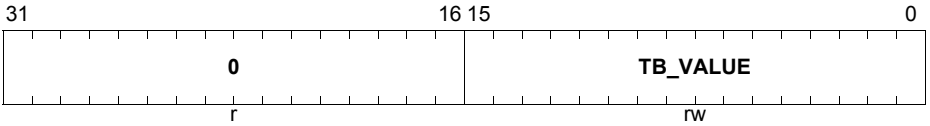


Field	Bits	Type	Description
BR_VALUE	[15:0]	rw	**Baud Rate Timer/Reload Register Value** Reading BR returns the 16-bit content of the baud rate timer. Writing BR loads the baud rate timer reload register with BR_VALUE.
0	[31:16]	r	**Reserved** Read as 0; should be written with 0.

21.2.3 Data Registers

The Transmit Buffer Register TB contains the transmit data value. A TB write operation latches all timing parameters stored in register SSOTC.

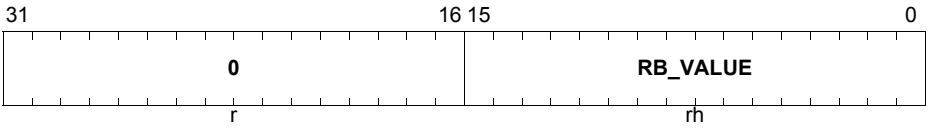
TB
Transmit Buffer Register **(20_H)** **Reset Value: 0000 0000_H**



Field	Bits	Type	Description
TB_VALUE	[15:0]	rw	**Transmit Data Register Value** Register TB stores the data value to be transmitted TB_VALUE. Unused bits of TB_VALUE (as defined by CON.BM) are ignored during transmission.
0	[31:16]	r	**Reserved** Read as 0; should be written with 0.

The Receive Buffer Register RB contains the receive data value.

RB
Receive Buffer Register **(24_H)** **Reset Value: 0000 0000_H**



Field	Bits	Type	Description
RB_VALUE	[15:0]	rh	**Receive Data Register Value** Register RB contains the received data value RB_VALUE (without the parity bit in parity mode) right aligned. Unused bits of RB_VALUE (as defined by CON.BM) will not be valid and should be ignored.
0	[31:16]	r	**Reserved** Read as 0; should be written with 0.

21.3 SSC0/SSC1/SSC2/SSC3 Module Implementation

This section describes SSC0/SSC1/SSC2/SSC3 module interfaces with the clock control, port connections, interrupt control, and address decoding.

21.3.1 Module Identification Registers

The reset values of the SSCx_ID module identification registers are 0000 4512_H.

21.3.2 Interfaces of the SSC Modules

Figure 21-16 and **Figure 21-17** show the TC1798-specific implementation details and interconnections of the SSC0/SSC1/SSC2/SSC3 modules.

Each of the SSC modules is supplied with a separate clock control, interrupt control, and address decoding logic. Two interrupt outputs can be used to generate DMA requests. The SSC0/SSC1/SSC2/SSC3 I/O lines are connected to Port 1, Port 2, Port 4, Port 6, Port 7, Port 10 and Port 18.

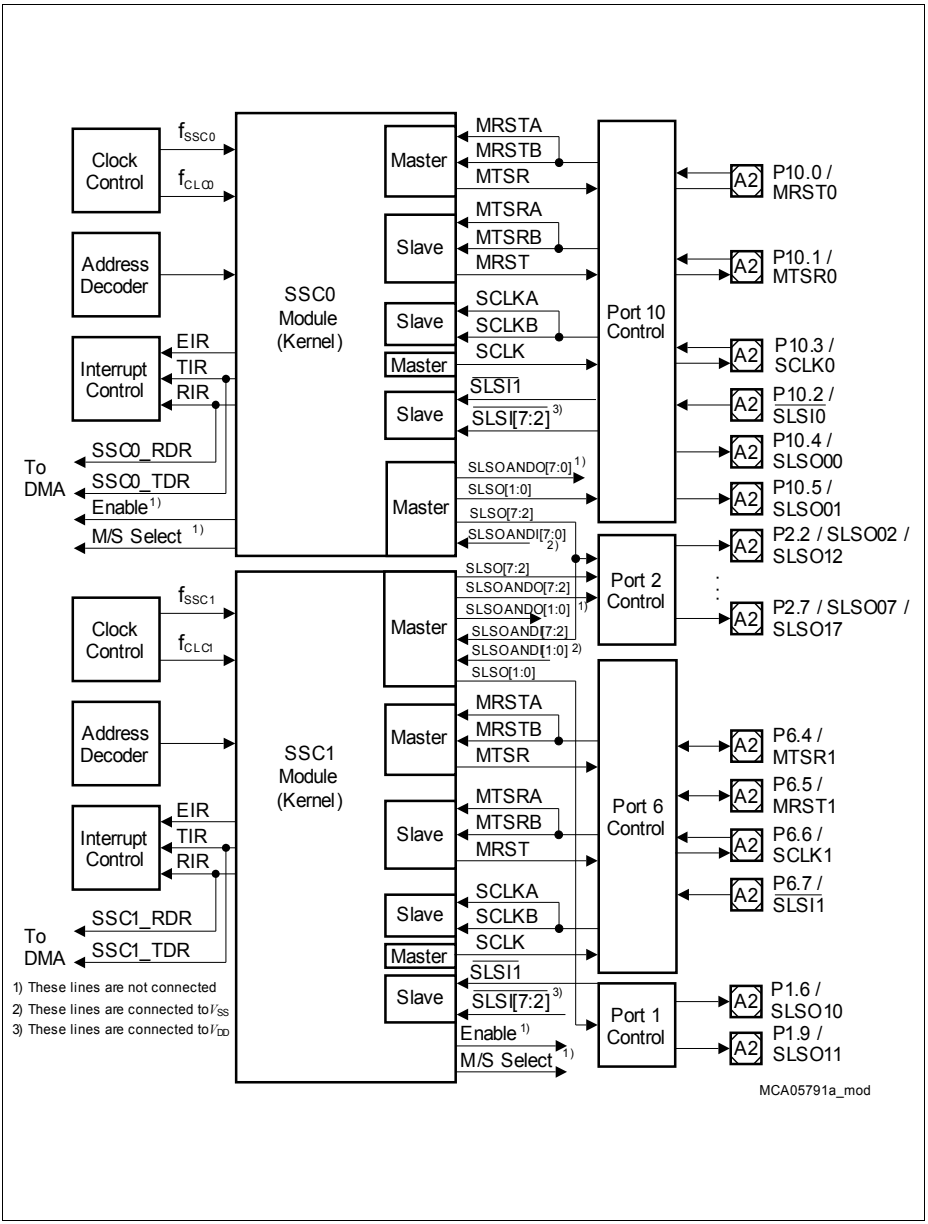


Figure 21-16 SSC0/SSC1 Module Implementation and Interconnections

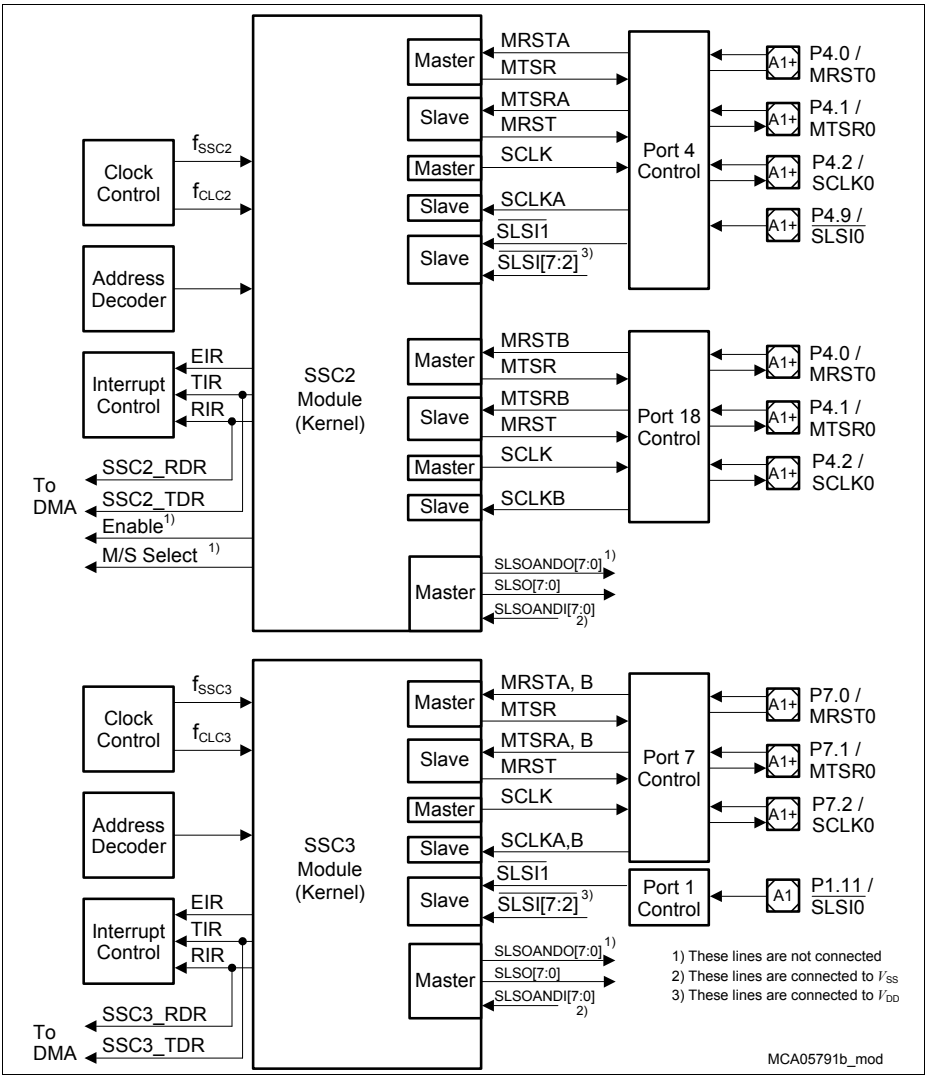


Figure 21-17 SSC2/SSC3 Module Implementation and Interconnections

21.3.3 On-Chip Connections

This section describes the on-chip connections of the SSC0/SSC1/SSC2 modules.

DMA Requests

The DMA request lines of the SSC0/SSC1/SSC2 modules become active whenever the related interrupt line is activated. The DMA request lines are connected to the DMA controller as shown in **Table 21-5**.

Table 21-5 DMA Request Lines of SSC0/SSC1/SSC2/SSC3

Module	SSC Interrupt Request Line	DMA Request Line	Description
SSC0	RIR	SSC0_RDR	DMA Channel 00 Request Input 4
			DMA Channel 06 Request Input 4
	TIR	SSC0_TDR	DMA Channel 02 Request Input 4
			DMA Channel 04 Request Input 4
SSC1	RIR	SSC1_RDR	DMA Channel 01 Request Input 4
			DMA Channel 07 Request Input 4
	TIR	SSC1_TDR	DMA Channel 03 Request Input 4
			DMA Channel 05 Request Input 4
SSC2	RIR	SSC2_RDR	DMA Channel 00 Request Input 13
	TIR	SSC2_TDR	DMA Channel 02 Request Input 13
SSC3	RIR	SSC2_RDR	DMA Channel 07 Request Input 12
	TIR	SSC2_TDR	DMA Channel 06 Request Input 12

21.3.4 SSC0/SSC1/SSC2/SSC3 Module Related External Registers

Figure 21-18 summarizes the module-related external registers which are required for SSC0/SSC1/SSC2/SSC3 programming (see also **Figure 21-15** for the module kernel specific registers).

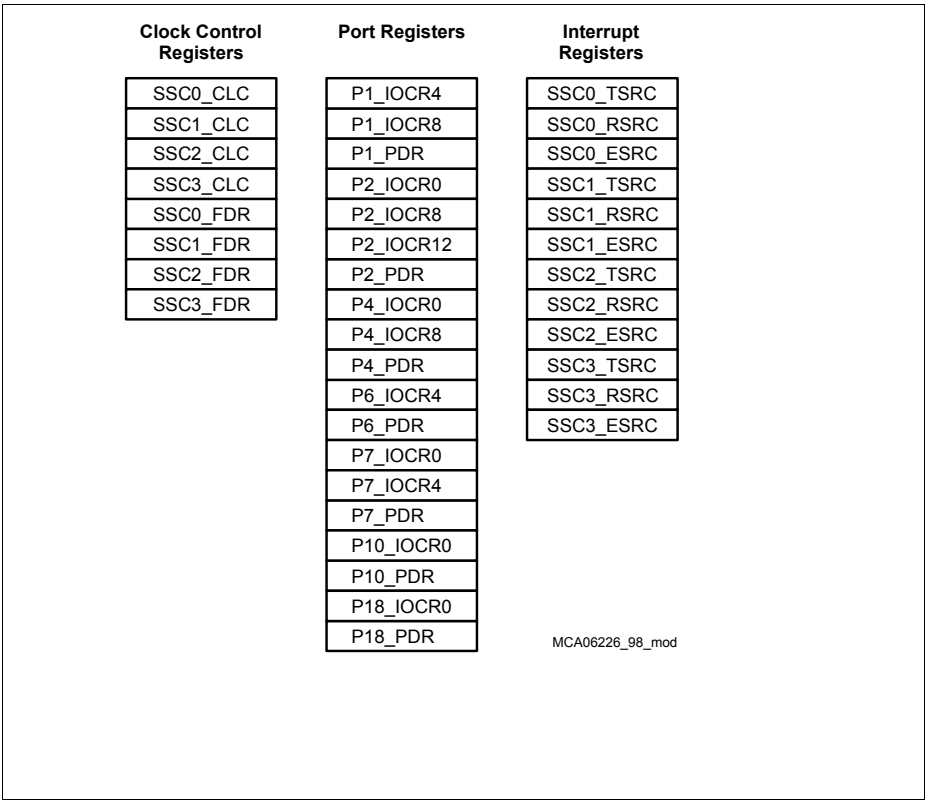


Figure 21-18 SSC0/SSC1/SSC2/SSC3 Implementation-specific Special Function Registers

21.3.4.1 Clock Control

Each SSC module has two clock signals (x = 0-3):

- f_{CLCx}
  This is the module clock that is used inside the SSC kernel for control purposes such as clocking of control logic and register operations. The frequency of f_{CLCx} is always identical to the system clock frequency f_{FPI}. The clock control registers SSCx_CLC make it possible to enable/disable f_{CLCx} under certain conditions.
- f_{SSCx}
  This clock is the module clock that is used in the SSCx as input clock of the baud rate generator, which finally determines the baud rate of the serial data. The fractional divider registers SSCx_FDR control the frequency of f_{SSCx} and make it possible to enable/disable it independently of f_{CLCx}.
  The Baud Rate Timer Reload Register SSCx_BR define serial data baud rate dependent from the frequency of f_{SSCx}.

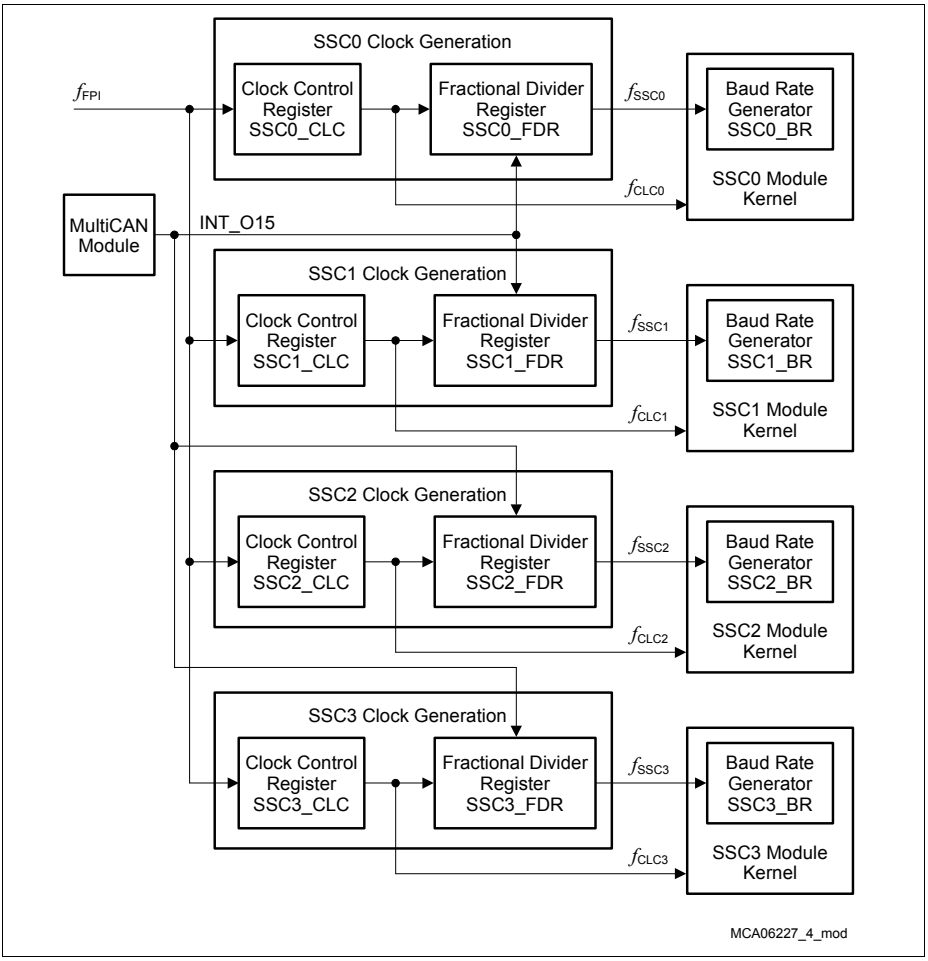


Figure 21-19 SSC Clock Generation

Output signal CAN_INT_O15 of the MultiCAN module can be used for external clock enable control of the fractional divider.

The following formulas define the frequency of f_{SSCx}.

$$f_{SSCx} = f_{FPI} \times \frac{1}{n} \text{ with n = 1024 - FDR.STEP} \quad (21.2)$$

$$f_{SSCx} = f_{FPI} \times \frac{n}{1024} \text{ with n = 0-1023} \quad (21.3)$$

Note: In SSC Master Mode, the maximum shift clock frequency is $f_{SSCx}/2$. In SSC Slave Mode, the maximum shift clock frequency is $f_{SSCx}/4$.

Combined with the formulas of the baud rate generator (see **Page 21-14**) and the fractional divider, the resulting serial data baud rate is defined by:

$$\text{Baud rate}_{SSC} = \frac{f_{FPI}}{2 \times (\text{BR.BR\_VALUE} + 1) \times (1024 - \text{FDR.STEP})} \quad (21.4)$$

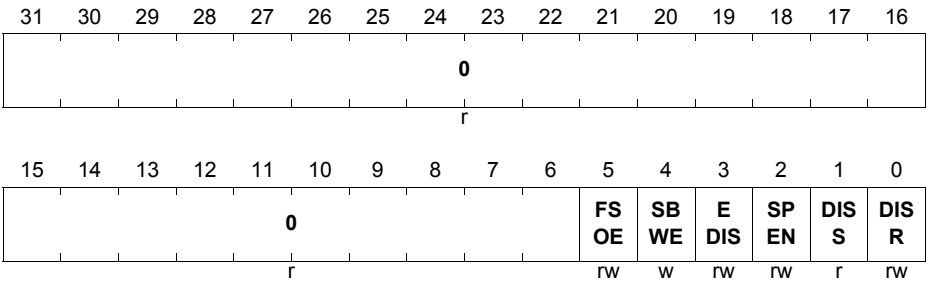
$$\text{Baud rate}_{SSC} = \frac{f_{FPI} \times \text{FDR.STEP}}{2 \times (\text{BR.BR\_VALUE} + 1) \times 1024} \text{ with FDR.STEP = 0-1023} \quad (21.5)$$

*Note: **Equation (21.2)** and **Equation (21.4)** apply to normal divider mode of the fractional divider (FDR.DM = 01_B). **Equation (21.3)** and **Equation (21.5)** apply to fractional divider mode (FDR.DM = 10_B).*

Clock Control Register

Each SSC has its own clock control register. The Clock Control Registers SSCx_CLC make it possible to control (enable/disable) the clock signals f_{CLCx} under certain conditions.

SSC0_CLC
SSC0_Clock Control Register **(00_H)** **Reset Value: 0000 0003$_H$**
SSC1_CLC
SSC1 Clock Control Register **(00_H)** **Reset Value: 0000 0003$_H$**
SSC2_CLC
SSC2 Clock Control Register **(00_H)** **Reset Value: 0000 0003$_H$**
SSC3_CLC
SSC3 Clock Control Register **(00_H)** **Reset Value: 0000 0003$_H$**



Field	Bits	Type	Description
DISR	0	rw	**Module Disable Request Bit** Used for enable/disable control of the module.
DISS	1	r	**Module Disable Status Bit** Bit indicates the current status of the module.
SPEN	2	rw	**Module Suspend Enable for OCDS** Used to enable the suspend mode.
EDIS	3	rw	**Sleep Mode Enable Control** Used to control module's sleep mode.
SBWE	4	w	**Module Suspend Bit Write Enable for OCDS** Determines whether SPEN and FSOE are write-protected.
FSOE	5	rw	**Fast Switch Off Enable** Used to switch off fast clock in Suspend Mode.

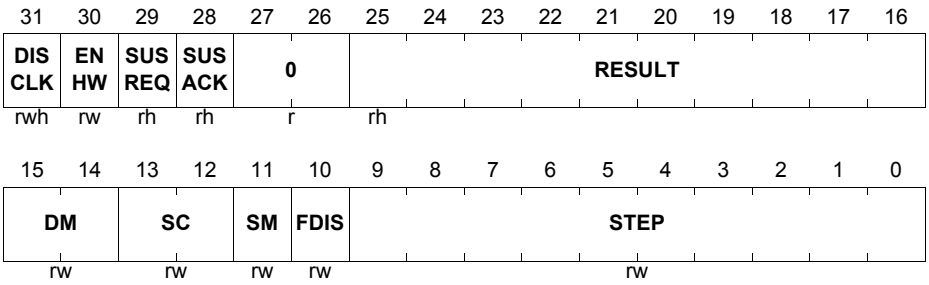
Field	Bits	Type	Description
0	[31:6]	r	**Reserved** Read as 0; should be written with 0.

Note: After a hardware reset operation, the f_{CLCx} clocks are disabled, and therefore also the SSC modules are disabled (DISS set).

Fractional Divider Register

Each SSC has its own fractional divider register. The Fractional Divider Registers SSCx_FDR control the clock rate of the shift clocks f_{SSCx}.

SSC0_FDR
SSC0 Fractional Divider Register (0C$_H$) Reset Value: 1000 0000$_H$
SSC1_FDR
SSC1 Fractional Divider Register (0C$_H$) Reset Value: 1000 0000$_H$
SSC2_FDR
SSC2 Fractional Divider Register (0C$_H$) Reset Value: 1000 0000$_H$
SSC3_FDR
SSC3 Fractional Divider Register (0C$_H$) Reset Value: 1000 0000$_H$



Field	Bits	Type	Description
STEP	[9:0]	rw	**Step Value** Reload or addition value for RESULT.
FDIS	10	rw	**Freeze Disable** This bit controls the freeze function for this module. 0_B Module operates on corrected clock, with reduced modulation jitter. 1_B Module operates on uncorrected clock, with full modulation jitter.

Field	Bits	Type	Description
SM	11	rw	**Suspend Mode** SM selects between granted or immediate suspend mode.
SC	[13:12]	rw	**Suspend Control** This bit field determines the behavior of the fractional divider in suspend mode.
DM	[15:14]	rw	**Divider Mode** This bit field selects normal divider mode, fractional divider mode, and off-state.
RESULT	[25:16]	rh	**Result Value** Bit field for the addition result.
SUSACK	28	rh	**Suspend Mode Acknowledge** Indicates state of SPNDACK signal.
SUSREQ	29	rh	**Suspend Mode Request** Indicates state of SPND signal.
ENHW	30	rw	**Enable Hardware Clock Control** Controls operation of ECEN input and DISCLK bit.
DISCLK	31	rwh	**Disable Clock** Hardware-controlled disable for f_{OUT} signal.
0	[27:26]	r	**Reserved** Read as 0; should be written with 0.

21.3.4.2 Port Control

Note: The SSCs in the TC1798 do not directly control the I/O functionality of pins. Therefore, control bits CON.EN and CON.MS have no functionality.

The interconnections between the SSC modules and the I/O lines/pins are controlled by software in the port logics. The SSC0/SSC1/SSC2 I/O functionality must be selected by the following port control operations (additionally to the PISEL programming):

- Input/output function selection (IOCR registers)
- Pad driver characteristics selection for the outputs (PDR registers)

The SSC0/SSC1/SSC2 port input/output control registers contain the bit fields that select the digital output and input driver characteristics such as pull-up/down devices, port direction (input/output), open-drain, and alternate output selections.

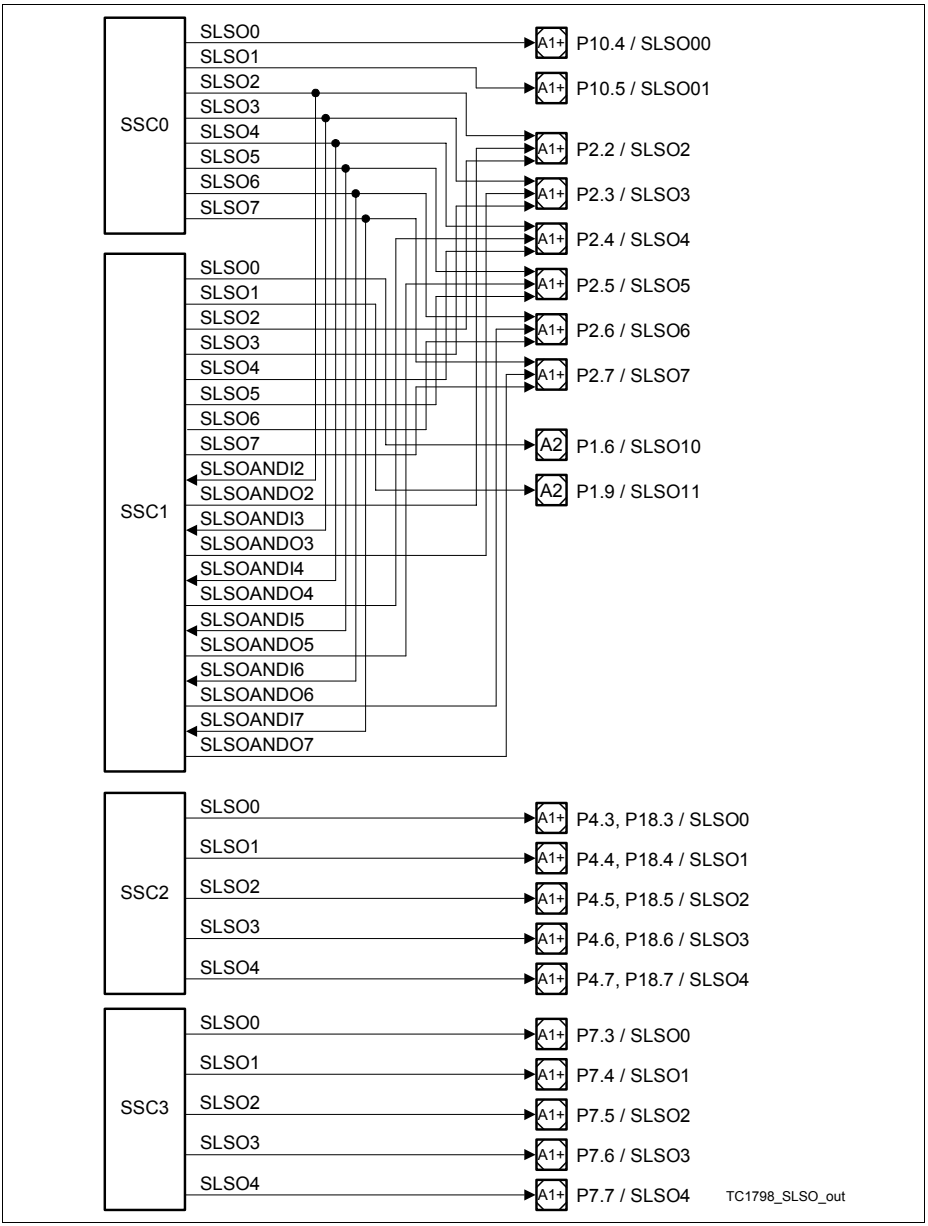


Figure 21-20 SLSI and SLSO Input/Output Connections

Table 21-6 shows how bits and bit fields must be programmed for the required I/O functionality of the SSC I/O lines.

Table 21-6 SSC I/O Line Selection and Setup

Module	Port Lines	Input/Output Control Register Bits	I/O
SSC0	P10.1 / MTSR0	P10_IOCR0.PC1 = $0XXX_B$	Input
		P10_IOCR0.PC1 = $1X01_B$	Output
	P10.0 / MRST0	P10_IOCR0.PC0 = $0XXX_B$	Input
		P10_IOCR0.PC0 = $1X01_B$	Output
	P10.3 / SCLK0	P10_IOCR0.PC3 = $0XXX_B$	Input
		P10_IOCR0.PC3 = $1X01_B$	Output
	P10.2 / SLSI0	P10_IOCR0.PC4 = $0XXX_B$	Input
SSC1	P6.4 / MTSR1	P6_IOCR4.PC4 = $0XXX_B$	Input
		P6_IOCR4.PC4 = $1X01_B$	Output
	P6.5 / MRST1	P6_IOCR4.PC5 = $0XXX_B$	Input
		P6_IOCR4.PC5 = $1X01_B$	Output
	P6.6 / SCLK1	P6_IOCR4.PC6 = $0XXX_B$	Input
		P6_IOCR4.PC6 = $1X01_B$	Output
	P6.7 / $\overline{\text{SLSI1}}$	P6_IOCR4.PC7 = $0XXX_B$	Input
SSC2	P4.1 / MTSR2	P4_IOCR0.PC1 = $0XXX_B$	Input
		P4_IOCR0.PC1 = $1X10_B$	Output
	P4.0 / MRST2	P4_IOCR0.PC0 = $0XXX_B$	Input
		P4_IOCR0.PC0 = $1X10_B$	Output
	P4.2 / SCLK2	P4_IOCR0.PC2 = $0XXX_B$	Input
		P4_IOCR0.PC2 = $1X10_B$	Output
	P4.9 / $\overline{\text{SLSI2}}$	P4_IOCR8.PC9 = $0XXX_B$	Input
SSC2B	P18.1 / MTSR2B	P18_IOCR0.PC1 = $0XXX_B$	Input
		P18_IOCR0.PC1 = $1X01_B$	Output
	P18.0 / MRST2B	P18_IOCR0.PC0 = $0XXX_B$	Input
		P18_IOCR0.PC0 = $1X01_B$	Output
	P18.2 / SCLK2B	P4_IOCR0.PC2 = $0XXX_B$	Input
		P4_IOCR0.PC2 = $1X01_B$	Output

Table 21-6 SSC I/O Line Selection and Setup (cont'd)

Module	Port Lines	Input/Output Control Register Bits	I/O
SSC3	P7.1 / MTSR3	P7_IOCR0.PC1 = $0XXX_B$	Input
		P7_IOCR0.PC1 = $1X10_B$	Output
	P7.0 / MRST3	P7_IOCR0.PC0 = $0XXX_B$	Input
		P7_IOCR0.PC0 = $1X10_B$	Output
	P7.2 / SCLK3	P7_IOCR0.PC2 = $0XXX_B$	Input
		P7_IOCR0.PC2 = $1X10_B$	Output
	P1.11 / $\overline{\text{SLSI3}}$	P1_IOCR8.PC11 = $0XXX_B$	Input
Slave Select Outputs			
SSC0	P10.4 / SLSO00	P10_IOCR4.PC4 = $1X01_B$	Output
	P10.5 / SLSO01	P10_IOCR4.PC5 = $1X01_B$	Output
SSC0	P2.2 / SLSO2	P2_IOCR0.PC2 = $1X01_B$	Output
SSC1		P2_IOCR0.PC2 = $1X10_B$	
SSC0 & SSC1		P2_IOCR0.PC2 = $1X11_B$	
SSC0	P2.3 / SLSO3	P2_IOCR0.PC3 = $1X01_B$	Output
SSC1		P2_IOCR0.PC3 = $1X10_B$	
SSC0 & SSC1		P2_IOCR0.PC3 = $1X11_B$	
SSC0	P2.4 / SLSO4	P2_IOCR4.PC4 = $1X01_B$	Output
SSC1		P2_IOCR4.PC4 = $1X10_B$	
SSC0 & SSC1		P2_IOCR4.PC4 = $1X11_B$	
SSC0	P2.5 / SLSO5	P2_IOCR4.PC5 = $1X01_B$	Output
SSC1		P2_IOCR4.PC5 = $1X10_B$	
SSC0 & SSC1		P2_IOCR4.PC5 = $1X11_B$	
SSC0	P2.6 / SLSO6	P2_IOCR4.PC6 = $1X01_B$	Output
SSC1		P2_IOCR4.PC6 = $1X10_B$	
SSC0 & SSC1		P2_IOCR4.PC6 = $1X11_B$	
SSC0	P2.7 / SLSO7	P2_IOCR4.PC7 = $1X01_B$	Output
SSC1		P2_IOCR4.PC7 = $1X10_B$	
SSC0 & SSC1		P2_IOCR4.PC7 = $1X11_B$	
SSC1	P1.6 / SLSO10	P1_IOCR4.PC6 = $1X10_B$	Output
	P1.9 / SLSO11	P1_IOCR8.PC9 = $1X10_B$	Output

Table 21-6 SSC I/O Line Selection and Setup (cont'd)

Module	Port Lines	Input/Output Control Register Bits	I/O
SSC2	P4.3 / SLSO20	P4_IOCR0.PC3 = $1X10_B$	Output
	P4.4 / SLSO21	P4_IOCR4.PC4 = $1X10_B$	
	P4.5 / SLSO22	P4_IOCR4.PC5 = $1X10_B$	
	P4.6 / SLSO23	P4_IOCR4.PC6 = $1X10_B$	
	P4.7 / SLSO24	P4_IOCR4.PC7 = $1X10_B$	
	P18.3 / SLSO20	P18_IOCR4.PC6 = $1X01_B$	
	P18.4 / SLSO20	P18_IOCR4.PC6 = $1X01_B$	
	P18.5 / SLSO20	P18_IOCR4.PC6 = $1X01_B$	
	P18.6 / SLSO20	P18_IOCR4.PC6 = $1X01_B$	
	P18.7 / SLSO20	P18_IOCR4.PC6 = $1X01_B$	
SSC3	P7.3 / SLSO30	P7_IOCR0.PC3 = $1X10_B$	Output
	P7.4 / SLSO31	P7_IOCR4.PC4 = $1X10_B$	
	P7.5 / SLSO32	P7_IOCR4.PC5 = $1X10_B$	
	P7.6 / SLSO33	P7_IOCR4.PC6 = $1X10_B$	
	P7.7 / SLSO34	P7_IOCR4.PC7 = $1X10_B$	

21.3.4.3 Interrupt Control Registers

The 3 × 3 interrupts of the SSC0/SSC1/SSC2 modules are controlled by the following service request control registers:

- SSCx_TSRC (x = 0-3) controls the transmit interrupts of the SSCx module
- SSCx_RSRC (x = 0-3) controls the receive interrupts of the SSCx module
- SSCx_ESRC (x = 0-3) controls the error interrupts of the SSCx module

TSRC
Transmit Interrupt Service Request Control Register
($F4_H$) **Reset Value: 0000 0000_H**

RSRC
Receive Interrupt Service Request Control Register
($F8_H$) **Reset Value: 0000 0000_H**

ESRC
Error Interrupt Service Request Control Register
(FC_H) **Reset Value: 0000 0000_H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SETR	CLRR	SRR	SRE	0	TOS	0		SRPN							
w	w	rh	rw	r	rw	r		rw							

Field	Bits	Type	Description
SRPN	[7:0]	rw	**Service Request Priority Number**
TOS	10	rw	**Type of Service Control**
SRE	12	rw	**Service Request Enable**
SRR	13	rh	**Service Request Flag**
CLRR	14	w	**Request Clear Bit**
SETR	15	w	**Request Set Bit**
0	[9:8], 11, [31:16]	r	**Reserved** Read as 0; should be written with 0.

21.3.5 Address Map of the SSC Modules

An absolute register address is given by the offset address of the register (given in Table 21-4) plus the module base address (given in Table 21-3).

Table 21-7 Address Map of SSC0/SSC1/SSC2/SSC3

Short Name	Description	Address	Access Mode		Reset Value
			Read	Write	
Synchronous Serial Interface 0 (SSC0)					
SSC0_ CLC	SSC0 Clock Control Register	$F031\ 0000_H$	U, SV	SV, E	$0000\ 0003_H$
SSC0_ PISEL	SSC0 Port Input Select Register	$F031\ 0004_H$	U, SV	U, SV	$0000\ 0000_H$
SSC0_ ID	SSC0 Module Identification Register	$F031\ 0008_H$	U, SV	BE	$0000\ 45XX_H$
SSC0_ FDR	SSC0 Fractional Divider Register	$F031\ 000C_H$	U, SV	SV, E	$1000\ 0000_H$
SSC0_CON	SSC0 Control Register	$F031\ 0010_H$	U, SV	U, SV	$0000\ 0000_H$
SSC0_ BR	SSC0 Baud Rate Timer Reload Register	$F031\ 0014_H$	U, SV	U, SV	$0000\ 0000_H$
SSC0_ SSOC	SSC0 Slave Select Output Control Register	$F031\ 0018_H$	U, SV	U, SV	$0000\ 0000_H$
SSC0_ SSOTC	SSC0 Slave Select Output Timing Control Register	$F031\ 001C_H$	U, SV	U, SV	$0000\ 0000_H$
SSC0_ TB	SSC0 Transmit Buffer Register	$F031\ 0020_H$	U, SV	U, SV	$0000\ 0000_H$
SSC0_ RB	SSC0 Receive Buffer Register	$F031\ 0024_H$	U, SV	U, SV	$0000\ 0000_H$
SSC0_ STAT	SSC0 Status Register	$F031\ 0028_H$	U, SV	U, SV	$0000\ 0000_H$
SSC0_ EFM	SSC0 Error Flag Modification Register	$F031\ 002C_H$	U, SV	U, SV	$0000\ 0000_H$
–	Reserved	$F031\ 0030_H$ - $F031\ 00F0_H$	BE	BE	–
SSC0_ TSRC	SSC0 Transmit Interrupt Service Req. Control Reg.	$F031\ 00F4_H$	U, SV	SV	$0000\ 0000_H$

Table 21-7 Address Map of SSC0/SSC1/SSC2/SSC3 (cont'd)

Short Name	Description	Address	Access Mode		Reset Value
			Read	Write	
SSC0_ RSRC	SSC0 Receive Interrupt Service Req. Control Reg.	F031 00F8$_H$	U, SV	SV	0000 0000$_H$
SSC0_ ESRC	SSC0 Error Interrupt Service Req. Control Reg.	F031 00FC$_H$	U, SV	SV	0000 0000$_H$
Synchronous Serial Interface 1 (SSC1)					
SSC1_CLC	SSC1 Clock Control Register	F031 0100$_H$	U, SV	SV, E	0000 0003$_H$
SSC1_ PISEL	SSC1 Port Input Select Register	F031 0104$_H$	U, SV	U, SV	0000 0000$_H$
SSC1_ ID	SSC1 Module Identification Register	F031 0108$_H$	U, SV	BE	0000 45XX$_H$
SSC1_ FDR	SSC1 Fractional Divider Register	F031 010C$_H$	U, SV	SV, E	1000 0000$_H$
SSC1_CON	SSC1 Control Register	F031 0110$_H$	U, SV	U, SV	0000 0000$_H$
SSC1_ BR	SSC1 Baud Rate Timer Reload Register	F031 0114$_H$	U, SV	U, SV	0000 0000$_H$
SSC1_ SSOC	SSC1 Slave Select Output Control Register	F031 0118$_H$	U, SV	U, SV	0000 0000$_H$
SSC1_ SSOTC	SSC1 Slave Select Output Timing Control Register	F031 011C$_H$	U, SV	U, SV	0000 0000$_H$
SSC1_ TB	SSC1 Transmit Buffer Register	F031 0120$_H$	U, SV	U, SV	0000 0000$_H$
SSC1_ RB	SSC1 Receive Buffer Register	F031 0124$_H$	U, SV	U, SV	0000 0000$_H$
SSC1_STAT	SSC1 Status Register	F031 0128$_H$	U, SV	U, SV	0000 0000$_H$
SSC1_ EFM	SSC1 Error Flag Modification Register	F031 012C$_H$	U, SV	U, SV	0000 0000$_H$
–	Reserved	F031 0130$_H$ - F031 01F0$_H$	BE	BE	–
SSC1_ TSRC	SSC1 Transmit Interrupt Service Req. Control Reg.	F031 01F4$_H$	U, SV	SV	0000 0000$_H$
SSC1_ RSRC	SSC1 Receive Interrupt Service Req. Control Reg.	F031 01F8$_H$	U, SV	SV	0000 0000$_H$

Table 21-7 Address Map of SSC0/SSC1/SSC2/SSC3 (cont'd)

Short Name	Description	Address	Access Mode		Reset Value
			Read	Write	
SSC1_ ESRC	SSC1 Error Interrupt Service Req. Control Reg.	F031 01FC$_H$	U, SV	SV	0000 0000$_H$
Synchronous Serial Interface 2 (SSC2)					
SSC2_CLC	SSC2 Clock Control Register	F031 0300$_H$	U, SV	SV, E	0000 0003$_H$
SSC2_ PISEL	SSC2 Port Input Select Register	F031 0304$_H$	U, SV	U, SV	0000 0000$_H$
SSC2_ ID	SSC2 Module Identification Register	F031 0308$_H$	U, SV	BE	0000 45XX$_H$
SSC2_ FDR	SSC2 Fractional Divider Register	F031 030C$_H$	U, SV	SV, E	1000 0000$_H$
SSC2_CON	SSC2 Control Register	F031 0310$_H$	U, SV	U, SV	0000 0000$_H$
SSC2_ BR	SSC2 Baud Rate Timer Reload Register	F031 0314$_H$	U, SV	U, SV	0000 0000$_H$
SSC2_ SSOC	SSC2 Slave Select Output Control Register	F031 0318$_H$	U, SV	U, SV	0000 0000$_H$
SSC2_ SSOTC	SSC2 Slave Select Output Timing Control Register	F031 031C$_H$	U, SV	U, SV	0000 0000$_H$
SSC2_ TB	SSC2 Transmit Buffer Register	F031 0320$_H$	U, SV	U, SV	0000 0000$_H$
SSC2_ RB	SSC2 Receive Buffer Register	F031 0324$_H$	U, SV	U, SV	0000 0000$_H$
SSC2_STAT	SSC2 Status Register	F031 0328$_H$	U, SV	U, SV	0000 0000$_H$
SSC2_ EFM	SSC2 Error Flag Modification Register	F031 032C$_H$	U, SV	U, SV	0000 0000$_H$
–	Reserved	F031 0330$_H$ - F031 03F0$_H$	BE	BE	–
SSC2_ TSRC	SSC2 Transmit Interrupt Service Req. Control Reg.	F031 03F4$_H$	U, SV	SV	0000 0000$_H$
SSC2_ RSRC	SSC2 Receive Interrupt Service Req. Control Reg.	F031 03F8$_H$	U, SV	SV	0000 0000$_H$
SSC2_ ESRC	SSC2 Error Interrupt Service Req. Control Reg.	F031 03FC$_H$	U, SV	SV	0000 0000$_H$

Table 21-7 Address Map of SSC0/SSC1/SSC2/SSC3 (cont'd)

Short Name	Description	Address	Access Mode		Reset Value
			Read	Write	
Synchronous Serial Interface 3 (SSC3)					
SSC3_CLC	SSC3 Clock Control Register	$F031\ 0400_H$	U, SV	SV, E	$0000\ 0003_H$
SSC3_ PISEL	SSC3 Port Input Select Register	$F031\ 0404_H$	U, SV	U, SV	$0000\ 0000_H$
SSC3_ ID	SSC3 Module Identification Register	$F031\ 0408_H$	U, SV	BE	$0000\ 45XX_H$
SSC3_ FDR	SSC3 Fractional Divider Register	$F031\ 040C_H$	U, SV	SV, E	$1000\ 0000_H$
SSC3_CON	SSC3 Control Register	$F031\ 0410_H$	U, SV	U, SV	$0000\ 0000_H$
SSC3_ BR	SSC3 Baud Rate Timer Reload Register	$F031\ 0414_H$	U, SV	U, SV	$0000\ 0000_H$
SSC3_ SSOC	SSC3 Slave Select Output Control Register	$F031\ 0418_H$	U, SV	U, SV	$0000\ 0000_H$
SSC3_ SSOTC	SSC3 Slave Select Output Timing Control Register	$F031\ 041C_H$	U, SV	U, SV	$0000\ 0000_H$
SSC3_ TB	SSC3 Transmit Buffer Register	$F031\ 0420_H$	U, SV	U, SV	$0000\ 0000_H$
SSC3_ RB	SSC3 Receive Buffer Register	$F031\ 0424_H$	U, SV	U, SV	$0000\ 0000_H$
SSC3_STAT	SSC3 Status Register	$F031\ 0428_H$	U, SV	U, SV	$0000\ 0000_H$
SSC3_ EFM	SSC3 Error Flag Modification Register	$F031\ 042C_H$	U, SV	U, SV	$0000\ 0000_H$
–	Reserved	$F031\ 0430_H$ - $F031\ 04F0_H$	BE	BE	–
SSC3_ TSRC	SSC3 Transmit Interrupt Service Req. Control Reg.	$F031\ 04F4_H$	U, SV	SV	$0000\ 0000_H$
SSC3_ RSRC	SSC3 Receive Interrupt Service Req. Control Reg.	$F031\ 04F8_H$	U, SV	SV	$0000\ 0000_H$
SSC3_ ESRC	SSC3 Error Interrupt Service Req. Control Reg.	$F031\ 04FC_H$	U, SV	SV	$0000\ 0000_H$

22 Synchronous Serial Interface Guardian (SSCG)

This chapter describes one SSCG module in top-down fashion. The chapter consists of the following sections:

- Overview - providing a description of the subsystem consisting of one SSC module and the corresponding SSCG module.
- Kernel description, describing how the SSCG module works and how it is to be used.
- Registers description, providing detailed information on each SSCG specific register.
- TC1798 implementation description.

22.1 Overview

Figure 22-1 shows a sub-system consisting of
- one SSC module SSC0
- one SSCG module SSCG0

This sub-system can be analyzed independently of the rest of the chip. One chip can contain one or more such subsystems.

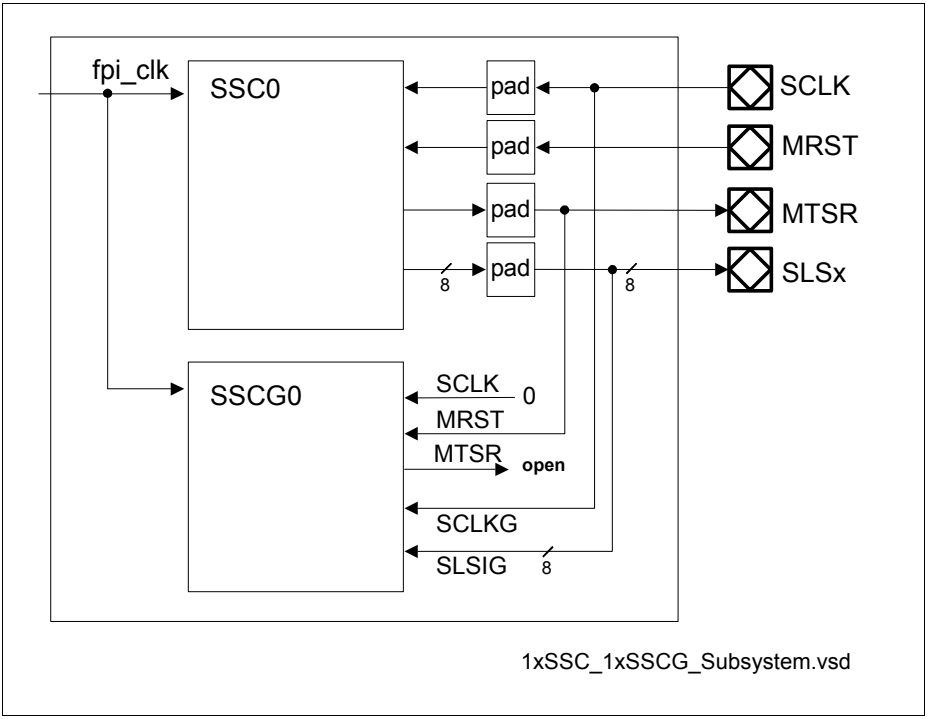


Figure 22-1 General Block Diagram of an SSC / SSCG Sub-System

22.1.1 General Operation

One SSCG monitors one SSC module. The SSCG itself can be considered as an SSC module, extended with some additional logic and registers. It is always configured in master mode, that is, the same as the monitored SSC. On the serial communication side, it receives all messages transmitted by the SSC module. On the FPI bus side, its registers inherited from the SSC module are always written in parallel to the registers of the SSC and contain identical values. The SSCG has an additional compare logic with additional registers which compares a copy of the ideal transmit message with the message that really appears on the pin. If a mismatch occurs, an interrupt is raised.

A user software can access the SSCG by reading / writing in two address ranges: one address range common to SSC and SSCG, and one dedicated to SSCG only. The extended SSCG registers can be accessed only through the dedicated address range.

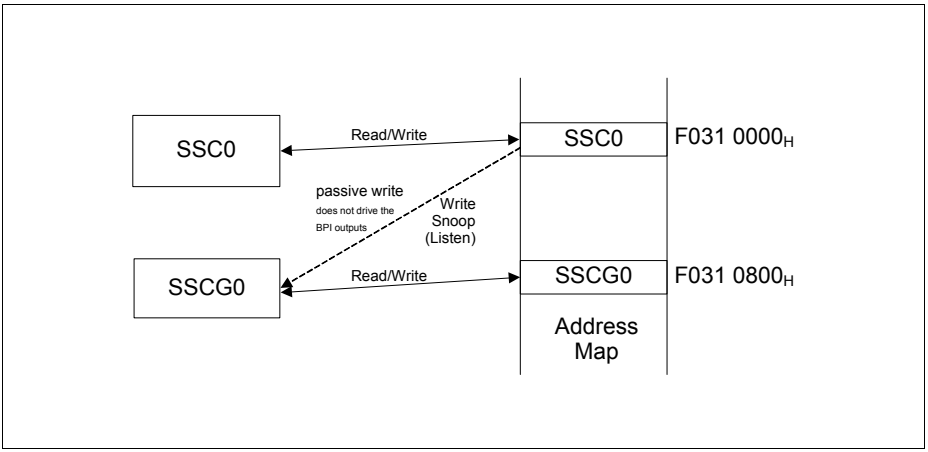


Figure 22-2 An Address Map of an SSC / SSCG Sub-System

22.2 SSCG Kernel Description

This chapter describees the additional functionality provided by the guardian.

22.2.1 Details on the Operation Principles and the Architecture

The SSCG module generates its own clock the same way the SSC does, by using identical but independent hardware. SSCG is initialized in parallel to the SSC using the same write accesses for initializing the SSC. The parallel register accesses insure cycle accurate parallel operation of the both modules.

Once all the common registers are initialized and the SSC starts to operate, the guardian immediately and transparently to the user starts with comparing the outgoing messages on the pin to the ideally programmed messages written in the transmit buffers of the SSC and the SSCG.

The SSC and the guardian both transmit the same message in parallel with their state machines operating cycle-synchronously, but whereas the SSC receives messages from the outside world, the SSCG receives the message being sent by its SSC.

A write to the transmit buffer of the SSCG copies in parallel the message to two locations: to the shift register and to the TB1 register. The message shifted out of the guardian ends nowhere, but the SSC transmitted message, which should be the identical one, is shifted into the guardian. The received message is copied from the shift register to the receive buffer and with this copy event a comparison between the sent and the received message is triggered.

If a difference is detected, an interrupt is raised, the contents of the TB1 and RB are copied to the snapshot registers TB1SNAP and RBSNAP, and at the same time the sticky error flag SNAPF is set. The hardware can only set the bit SNAPF, and the software can reset (or set) this flag. Reading this flag by software does not reset this flag automatically. It is reset by a second memory access, a write to the GEFM register.

Message Length

The message length can vary according to the settings from 2 to 16 bits. The padding bits not belonging to the message filling the maximum length of 16 are undefined, and shall be masked out when performing the comparison.

Parity Bit

If the parity bit is set, than the effective message length is one bit shorter, and the total length includes the concatenated parity bit. Parity error shall be raised by the guardian using the normal parity check mechanisms. The guardian comparison shall be done on effective message length, taking the parity out.

Snapshots

The SSCG keeps a snapshot of the information of the last error message in the registers TB1SNAP and RBSNAP. The SNAPF bit flags that error occurred. The snapshot is sticky, that is it is not destroyed by the consequent correct messages. Only a new error message overwrites the snapshot of an old error message. A lost snapshot is not flagged.

Interrupts

The three SSC interrupts, the Rx and Tx and Error interrupts, are not used.

There is a dedicated SSCG interrupt node, signaling a comparison error and parity error.

Both errors cause taking a sticky snapshot on TB1 and RB. Compare error sets the sticky flag GSTAT.CE. Parity error sets the sticky flag STAT.PARE.

Additionally the SSCG interupt node signals a phase error and clock and slave select compare errors.

Phase error sets the sticky flag STAT.PE. Clock and slave select errors set the sticky flags in the GSTAT register.

Data comparison error and the parity error trigger the interrupt after the data comparison has been done. The SLS and CLK comparison errors and the phase error trigger an interrupt immediately.

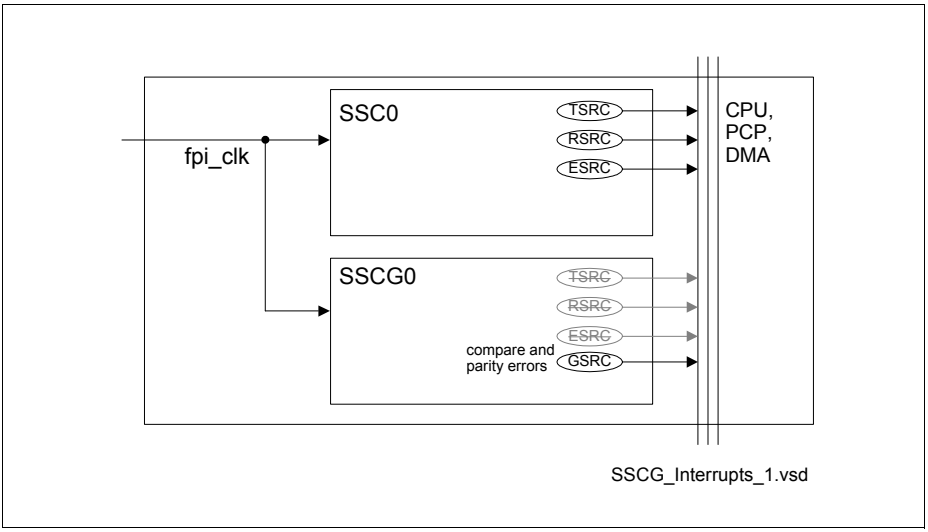


Figure 22-3 SSCG Interrupts

22.2.1.1 Monitoring the Slave Select and Serial Clock Signals

The slave select signals SLSx are monitored continuously with the same serial clock edge as the data signals. In contrast to the data signal which is sampled only during the data shift phase, all SLS signals are sampled and compared all the time: during the idle, leading delay, data shift, inter word delay, and trailing delay phases. The goal is to monitor if the SSC module operates properly and to detect stuck-at and other failiures in the hardware of the module.

The clock signal SCLK is monitored continuously in the middle of each half-period. This is achieved by using a double frequency, which is generated by a dedicated clock divider, similar to the main baud-rate generator. The purpose of the monitoring is to assure the corect operation of the SSC baud-rate generator and quickly detect hardware failiures.

This concept covers the hardware operation with focus on the digital functionality. Checking the timing constraints is not a subject of the monitoring, due to the wide variation of the timings and their dependency on process, voltage, temperature and the capacitive load at the lines. Therefore the baud rates are limited to single digit Mbaud rates, which is necessary in order to have robust monitoring without timing violations and with stable signals arround the sample points. Communication disturbances due to signal glitches and EMI effects can not be covered sufficiently using monitoring with digital sampling, and therefore they are not covered. They are covered with the parity bit and taken care of by the customer during the design of the printed circuit board.

Each of the eight SLS signals and the one SCLK is associated to a sticky flag signaling an occurence of a mismatch between an SSC signal and the corresponding SSCG signal. It is set by hardware and can be reset only by software. For test purposes these flags can be set by software, using the GEFM register.

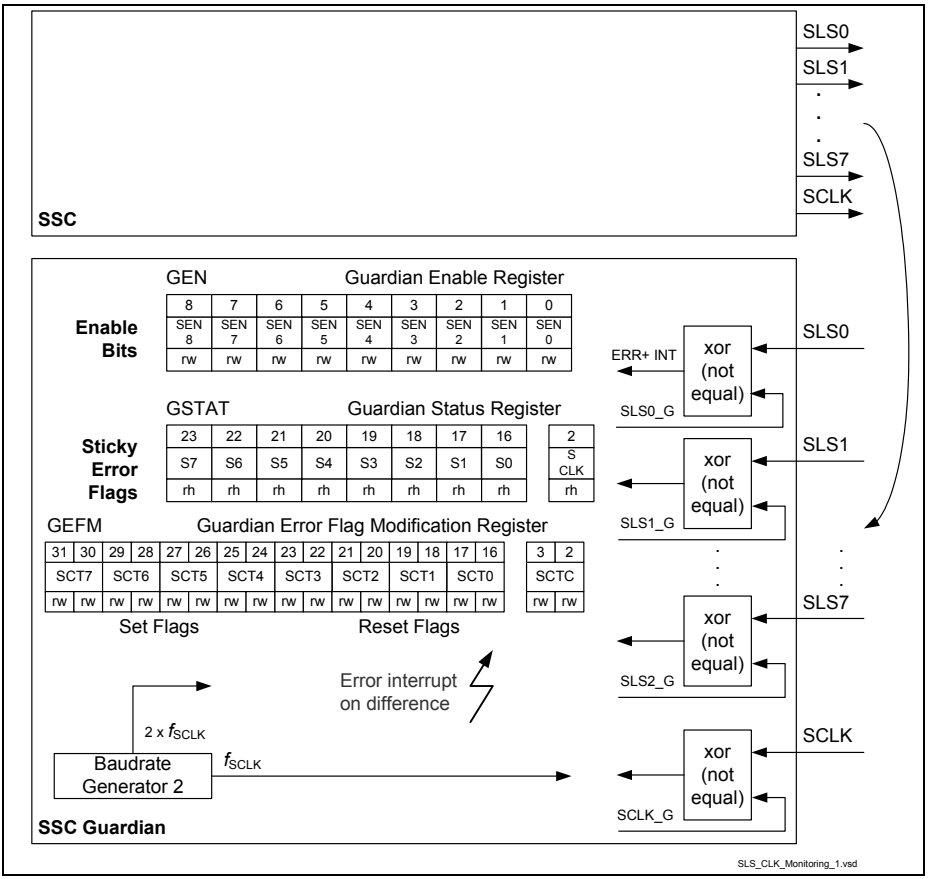


Figure 22-4 Implementation of the SLSx and SCLK monitoring registers

22.3 SSCG Kernel Registers, inherited from SSC

This section describes the kernel registers of the SSC module. All SSC kernel register names described in this section will be referenced in other parts of the TC1798 User´s Manual by the module name prefix “SSCG0_” for the SSCG0 interface, “SSCG1, 2, 3_” for the SSCG1, 2, 3 interfaces.

All registers in the SSCG address spaces are reset with the application reset (definition see SCU section “Reset Operation”).

SSC Kernel Register Overview

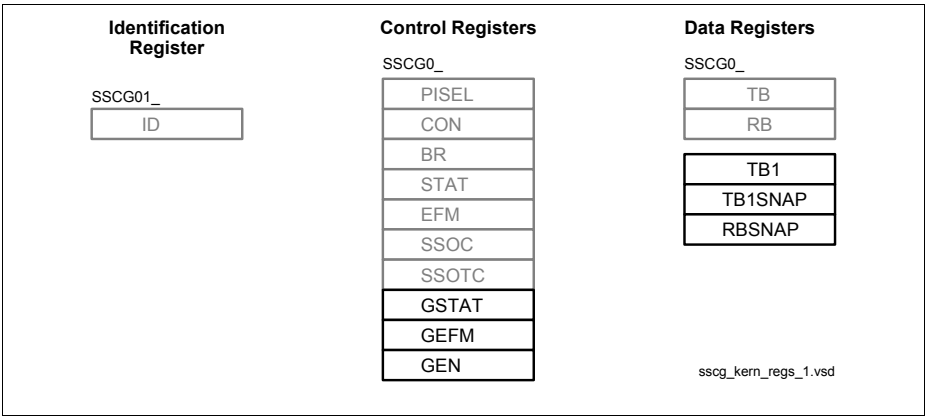


Figure 22-5 SSCG Kernel Registers

The complete address map of the SSC modules is described in **Table 22-5** on **Page 22-41**.

Table 22-1 Registers Address Space - SSC Kernel Registers

Module	Base Address	End Address	Note
SSCG0	F031 0800$_H$	F031 09FF$_H$	–
SSCG1	F031 0A00$_H$	F031 0BFF$_H$	–
SSCG2	F031 0C00$_H$	F031 0DFF$_H$	–
SSCG3	F031 0E00$_H$	F031 0FFF$_H$	–

Table 22-2 Registers Overview - SSC Kernel Registers

Register Short Name	Register Long Name	Offset Address[1)]	Description see
SSC - inherited registers			
PISEL	Port Input Select Register	004_H	Page 22-11
ID	Module Identification Register	008_H	Page 22-10
CON	Control Register	010_H	Page 22-13
BR	Baud Rate Timer Reload Register	014_H	Page 22-23
STAT	Status Register	028_H	Page 22-16
EFM	Error Flag Modification Register	$02C_H$	Page 22-18
SSOC	Slave Select Output Control Register	018_H	Page 22-20
SSOTC	Slave Select Output Timing Control Reg.	$01C_H$	Page 22-21
TB	Transmit Buffer Register	020_H	Page 22-24
RB	Receive Buffer Register	024_H	Page 22-24
SSCG - specific registers			
TB1	Transmit Buffer Compare Register	100_H	Page 22-25
TB1SNAP	Transmit Buffer Snapshot Register	104_H	Page 22-25
RBSNAP	Receive Buffer Snapshot Register	108_H	Page 22-26
GSTAT	Guardian Status Register	$10C_H$	Page 22-27
GEFM	Guardian Error Flag Modification Register	110_H	Page 22-28
GEN	Guardian Enable Register	114_H	Page 22-29
GSRC	Guardian Service Request Control Reg.	$1FC_H$	Page 22-39

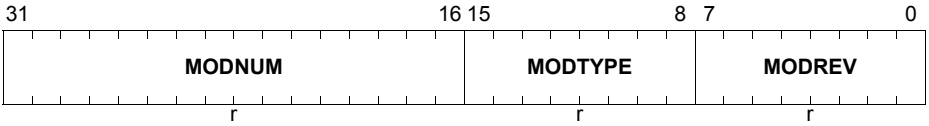
1) The absolute register address is calculated as follows:
Module Base Address (Table 22-1) + Offset Address (shown in this column)

22.3.1 Module Identification Register

The SSC Module Identification Register ID contains read-only information about the module version.

ID

Module Identification Register **(08_H)** **Reset Value: 0085 C0XX$_H$**



Field	Bits	Type	Description
MODREV	[7:0]	r	**Module Revision Number** This bit field defines the module revision number..
MODTYPE	[15:8]	r	**Module Type** This bit field defines the module as a 32-bit module: $C0_H$
MODNUM	[31:16]	r	**Module Number Value** This bit field defines the module identification number for the SSCG: 0085_H

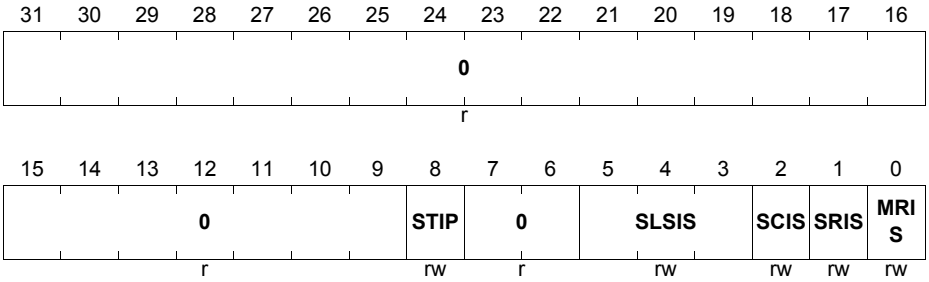
22.3.2 Control Registers

The PISEL register controls the input signal selection of the SSGC module. Each input of the module kernel receive, transmit and clock signals has associated two input lines (marked by suffix A and B).

Note: They may need to be programmed / initialized differently for SSC / SSCG module, depending on the top level connections to the ports and pins. In general, such situation should be avoided, if possible.

PISEL

Port Input Select Register **(04_H)** **Reset Value: 0000 0000$_H$**



Field	Bits	Type	Description
MRIS	0	rw	**Master Mode Receive Input Select** MRIS selects the receive input line in Master Mode. 0_B Receive input line MRSTA is selected 1_B Receive input line MRSTB is selected
SRIS	1	rw	**Slave Mode Receive Input Select** SRIS selects receive input line in Slave Mode. 0_B Receive input line MTSRA is selected 1_B Receive input line MTSRB is selected
SCIS	2	rw	**Slave Mode Clock Input Select** SCIS selects the module kernel SCLK input line that is used as clock input line in slave mode. 0_B Slave Mode clock input line SCLKA is selected 1_B Slave Mode clock input line SCLKB is selected

Field	Bits	Type	Description
SLSIS	[5:3]	rw	**Slave Mode Slave Select Input Selection** 000_B Slave select input lines are deselected; SSC is operating without slave select input functionality. 001_B $\overline{SLSI}$ input line 1 is selected for operation. 010_B $\overline{SLSI}$ input line 2 is selected for operation. 011_B $\overline{SLSI}$ input line 3 is selected for operation. 100_B $\overline{SLSI}$ input line 4 is selected for operation. 101_B $\overline{SLSI}$ input line 5 is selected for operation. 110_B $\overline{SLSI}$ input line 6 is selected for operation. 111_B $\overline{SLSI}$ input line 7 is selected for operation. In the TC1798, other combinations of SLSIS except 000_B and 001_B are reserved and must not be used.
STIP	8	rw	**Slave Transmit Idle State Polarity** This bit determines the logic level of the Slave Mode transmit signal MRST when the SSC slave select input signals are inactive (PISEL.SLSIS $\neq 000_B$). 0_B MRST = 0 when SSC is deselected in Slave Mode. 1_B MRST = 1 when SSC is deselected in Slave Mode.
0	[7:6], [31:9]	r	**Reserved** Read as 0; should be written with 0.

The operating modes of the SSC are controlled by the Control Register CON. This register contains control bits for mode and error check selection.

Note: Whenever operating mode parameters in the CON register are changed by software, no transfer should be in progress (STAT.BSY = 0) and the SSC should be disabled (CON.EN = 0) and afterwards enabled again (CON.EN = 1).

CON
Control Register **(10_H)** **Reset Value: $0000\ 0000_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0												PAREEN	PARTYP	PARREN	PARTEN
r												rw	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EN	MS	0	AREN	BEN	PEN	REN	TEN	LB	PO	PH	HB	BM			
rw	rw	r	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw			

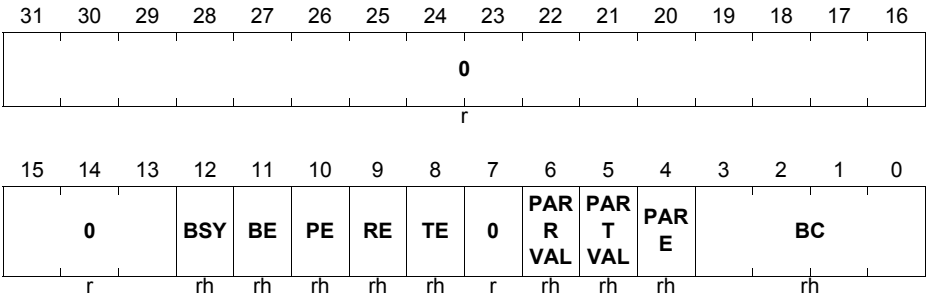
Field	Bits	Type	Description
BM	[3:0]	rw	**Frame Width Selection** BM determines the number of bits of the serial frame. Frame width without parity: 0000_B Reserved; do not use this combination. 0001_B Frame width is 2 bits (2 data bits). 0010_B Frame width is 3 bits (3 data bits). $\cdots_B$ ... 1110_B Frame width is 15 bits (15 data bits). 1111_B Frame width is 16 bits (16 data bits). Frame width with parity: 0000_B Reserved; do not use this combination. 0001_B Frame width is 2 bits (1 data bit + parity bit. 0010_B Frame width is 3 bits (2 data bits + parity bit). $\cdots_B$ ... 1110_B Frame width is 15 bits (14 data bits + parity bit). 1111_B Frame width is 16 bits (15 data bits + parity bit).
HB	4	rw	**Heading Bit Control** 0_B Transmit/Receive LSB First 1_B Transmit/Receive MSB First

Field	Bits	Type	Description
PH	5	rw	**Clock Phase Control** 0_B Shift transmit data on the leading clock edge, latch on trailing edge 1_B Latch receive data on leading clock edge, shift on trailing edge
PO	6	rw	**Clock Polarity Control** 0_B Idle clock line is low, the leading clock edge is low-to-high transition 1_B Idle clock line is high, the leading clock edge is high-to-low transition
LB	7	rw	**Loop-Back Control** 0_B Normal output 1_B Receive input is connected to transmit output (Half-duplex Mode)
TEN	8	rw	**Transmit Error Enable** 0_B Ignore transmit errors 1_B Check transmit errors
REN	9	rw	**Receive Error Enable** 0_B Ignore receive errors 1_B Check receive errors
PEN	10	rw	**Phase Error Enable** 0_B Check phase errors 1_B Check phase errors In the SSC Guardian module, the phase error is always checked, independent of the setting of the enable bit.
BEN	11	rw	**Baud Rate Error Enable** 0_B Ignore baud rate errors 1_B Check baud rate errors
AREN	12	rw	**Automatic Reset Enable** 0_B No additional action upon a baud rate error 1_B SSC is automatically reset on a baud rate error
MS	14	rw	**Master Select** 0_B Slave Mode. Operate on shift clock received via SCLK 1_B Master Mode. Generate shift clock and output it via SCLK The inverted state of this bit is available on module output line “M/S selected”.

Field	Bits	Type	Description
EN	15	rw	**Enable Bit** 0_B Transmission and reception are disabled. 1_B Transmission and reception are enabled. This bit is available as module output line “SSC enabled”. Note that EN should only be cleared by software while no transfer is in progress (STAT.BSY = 0). Note that the transmission/reception enable can also be controlled in queued SSC mode by bit SSOTC.EN.
PARTEN	16	rw	**Parity Transmit Enable Bit** This bit enables the parity mode for transmit frames. 0_B Parity mode for transmit frames is disabled. 1_B Parity mode for transmit frames is enabled.
PARREN	17	rw	**Parity Receive Enable Bit** This bit enables the parity mode for receive frames. 0_B Parity mode for receive frames is disabled. 1_B Parity mode for receive frames is enabled.
PARTYP	18	rw	**Parity Type Bit** If PAREN = 1, this bit defines the type of parity to be generated or checked. 0_B Even parity is selected (parity bit = 1 on odd number of 1s in data, parity bit = 0 on even number of 1s in data). 1_B Odd parity selected (parity bit = 1 on even number of 1s in data, parity bit = 0 on odd number of 1s in data)
PAREEN	19	rw	**Parity Error Enable** 0_B Ignore receive parity errors 1_B Check receive parity errors
0	13, [31:20]	r	**Reserved** Read as 0; should be written with 0.

The Status Register STAT contains status flags for error identification, the busy flag, and a bit field that indicates the current shift counter status.

STAT
Status Register **(28_H)** **Reset Value: 0000 0000$_H$**



Field	Bits	Type	Description
BC	[3:0]	rh	**Bit Count Status** BC indicates the current status of the shift counter. The shift counter is updated with every shifted bit.
PARE	4	rh	**Parity Error Flag** 0_B No error 1_B Received parity bit is wrong.
PARTVAL	5	rh	**Parity Transmit Value** If parity mode is enabled, this bit indicates the calculated parity bit for the transmission of the actual serial frame. PARTVAL is written with the transmit parity value when the shift register is loaded from TB. PARTVAL is reset when CON.PAREN is reset.
PARRVAL	6	rh	**Parity Receive Value** if parity mode is enabled, this bit PARRVAL is loaded when the received data is written into RB. PARRVAL is reset when CON.PAREN is reset.
TE	8	rh	**Transmit Error Flag** 0_B No error 1_B Transfer starts with the slave's transmit buffer not being updated
RE	9	rh	**Receive Error Flag** 0_B No error 1_B Reception completed before the receive buffer was read

Field	Bits	Type	Description
PE	10	rh	**Phase Error Flag** 0_B No error 1_B Received data changes during the sampling clock edge
BE	11	rh	**Baud Rate Error Flag** 0_B No error 1_B There is more than factor 2 or less than factor 0.5 between the slave's actual and the expected baud rate.
BSY	12	rh	**Busy Flag** BSY is set while a transfer is in progress.
0	7, [31:13]	r	**Reserved** Read as 0; should be written with 0.

The Error Flag Modification Register EFM is required for clearing or setting the four error flags which are located in register STAT.

EFM
Error Flag Modification Register (2C$_H$) Reset Value: 0000 0000$_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SETBE	SETPE	SETRE	SETTE	CLRBE	CLRPE	CLRRE	CLRTE	0			SETPARE	0			CLRPARE
w	w	w	w	w	w	w	w	r			w	r			w

Field	Bits	Type	Description
CLRPARE	0	w	**Clear Parity Error Flag** 0_B No effect 1_B Bit STAT.PARE is cleared. Bit is always read as 0.
SETPARE	4	w	**Set Parity Error Flag** 0_B No effect 1_B Bit STAT.PARE is set. Bit is always read as 0.
CLRTE	8	w	**Clear Transmit Error Flag** 0_B No effect 1_B Bit STAT.TE is cleared. Bit is always read as 0.
CLRRE	9	w	**Clear Receive Error Flag** 0_B No effect 1_B Bit STAT.RE is cleared. Bit is always read as 0.
CLRPE	10	w	**Clear Phase Error Flag** 0_B No effect 1_B Bit STAT.PE is cleared. Bit is always read as 0.

Field	Bits	Type	Description
CLRBE	11	w	**Clear Baud Rate Error Flag** 0_B No effect 1_B Bit STAT.BE is cleared. Bit is always read as 0.
SETTE	12	w	**Set Transmit Error Flag** 0_B No effect 1_B Bit STAT.TE is set. Bit is always read as 0.
SETRE	13	w	**Set Receive Error Flag** 0_B No effect 1_B Bit STAT.RE is set. Bit is always read as 0.
SETPE	14	w	**Set Phase Error Flag** 0_B No effect 1_B Bit STAT.PE is set. Bit is always read as 0.
SETBE	15	w	**Set Baud Rate Error Flag** 0_B No effect 1_B Bit STAT.BE is set. Bit is always read as 0.
0	[3:1], [7:5], [31:16]	r	**Reserved** Read as 0; should be written with 0.

Note: When the set and clear bits for an error flag are set at the same time during an EFM write operation (e.g SETPE = CLRPE = 1), the error flag in STAT is not affected.

The Slave Select Output Control Register controls the operation of the Chip Select Output Generation Unit.

SSOC

Slave Select Output Control Register (18_H) **Reset Value: $0000\ 0000_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OEN 7	OEN 6	OEN 5	OEN 4	OEN 3	OEN 2	OEN 1	OEN 0	AOL 7	AOL 6	AOL 5	AOL 4	AOL 3	AOL 2	AOL 1	AOL 0
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
AOLn (n = 0-7)	n	rw	**Active Output Level** 0_B SLSOn is at low level during the chip select active time $t_{SLSOACT}$. The high level is the inactive level of SLSOn. 1_B SLSO line n is at high level during the chip select active time $t_{SLSOACT}$. The low level is the inactive level of SLSOn.
OENn (n = 0-7)	8 + n	rw	**Output n Enable Control** 0_B SLSOn output is disabled; SLSOn is always at inactive level as defined by AOLn. 1_B SLSOn output is enabled.
0	[31:16]	r	**Reserved** Read as 0; should be written with 0.

Note: The SSOC register content is latched by each TB register write operation and remains latched during the consecutive serial transmission.

The Slave Select Output Timing Control Register controls the operation of the Slave Select Output Generation Unit.

SSOTC
Slave Select Output Timing Control Register
($1C_H$) **Reset Value: $0000\ 0000_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EN	QSM EN	0					SLS O7 MOD	0		INACT		TRAIL		LEAD	
rw	w	r					rw	r		rw		rw		rw	

Field	Bits	Type	Description
LEAD	[1:0]	rw	**Slave Output Select Leading Delay** This bit field determines the number of leading delay clock cycles. A leading delay clock cycle is always a multiple of an SCLK shift clock period. 00_B Zero leading delay clock cycle selected[1)] 01_B One leading delay clock cycle selected 10_B Two leading delay clock cycles selected 11_B Three leading delay clock cycles selected
TRAIL	[3:2]	rw	**Slave Output Select Trailing Delay** This bit field determines the number of trailing delay clock cycles. A trailing delay clock cycle is always a multiple of an SCLK shift clock period. 00_B Zero trailing delay clock cycle selected[1)] 01_B One trailing delay clock cycle selected 10_B Two trailing delay clock cycles selected 11_B Three trailing delay clock cycles selected

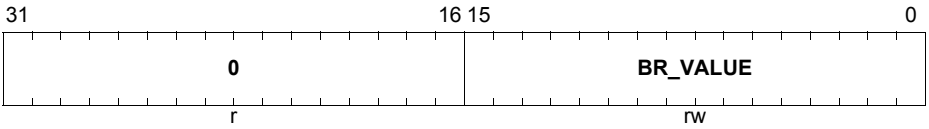
Field	Bits	Type	Description
INACT	[5:4]	rw	**Slave Output Select Inactive Delay** This bit field determines the number of inactive delay clock cycles. An inactive delay clock cycle is always a multiple of an SCLK shift clock period. 00_B Zero inactive delay clock cycle selected[1)] 01_B One inactive delay clock cycle selected 10_B Two inactive delay clock cycles selected 11_B Three inactive delay clock cycles selected
SLSO7MOD	8	rw	**SLSO7 Delayed Mode Selection** This bit selects the delayed mode for the SLSO7 slave select output. 0_B Normal mode selected for SLSO7 1_B Delayed mode selected for SLSO7
QSMEN	14	w	**Queued SSC Mode Enabled** 0_B When QSMEN is written with 0, the state of bit SSOTC.EN is don't care. In this case, the enable/disable of the SSC is controlled by bit CON.EN only. Note that EN should only be cleared by software while no transfer is in progress (STAT.BSY = 0). 1_B When QSMEN is written with 1, queued SSC mode is enabled, and the state of bit SSOTC.EN is copied to CON.EN. QSMEN is always read as 0.
EN	15	rw	**Enable Bit** 0_B Transmission and reception are disabled. 1_B Transmission and reception are enabled. Note that the transmission/reception enable can also be controlled in queued SSC mode by bit CON.EN.
0	[7:6], [13:9], [31:16]	r	**Reserved** Read as 0; should be written with 0.

1) For getting a best case timing with no timing delays, this bit field value should be set when the SLSOn outputs are disabled (SSOC.OENn bits set to 0).

Note: The SSOTC register timing parameters LEAD, TRAIL, INACT, and SLSO7MOD are latched by each TB register write operation and remain latched during a consecutive serial transmission. Bits QSMEN and EN of register SSOTC are not latched.

The Baud Rate Timer Reload Register BR contains the 16-bit reload value for the baud rate timer.

BR
Baud Rate Timer Reload Register (14_H) Reset Value: 0000 0000_H

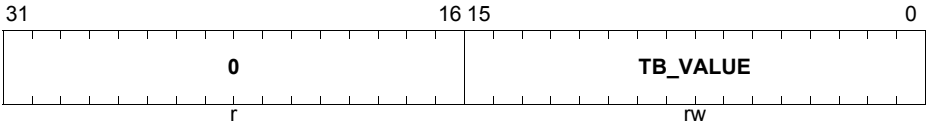


Field	Bits	Type	Description
BR_VALUE	[15:0]	rw	**Baud Rate Timer/Reload Register Value** Reading BR returns the 16-bit content of the baud rate timer. Writing BR loads the baud rate timer reload register with BR_VALUE.
0	[31:16]	r	**Reserved** Read as 0; should be written with 0.

22.3.3 Data Registers

The Transmit Buffer Register TB contains the transmit data value. A TB write operation latches all timing parameters stored in register SSOTC.

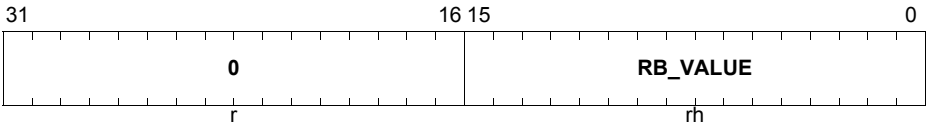
TB
Transmit Buffer Register **(20_H)** **Reset Value: 0000 0000_H**



Field	Bits	Type	Description
TB_VALUE	[15:0]	rw	**Transmit Data Register Value** Register TB stores the data value to be transmitted TB_VALUE. Unused bits of TB_VALUE (as defined by CON.BM) are ignored during transmission.
0	[31:16]	r	**Reserved** Read as 0; should be written with 0.

The Receive Buffer Register RB contains the receive data value.

RB
Receive Buffer Register **(24_H)** **Reset Value: 0000 0000_H**



Field	Bits	Type	Description
RB_VALUE	[15:0]	rh	**Receive Data Register Value** Register RB contains the received data value RB_VALUE (without the parity bit in parity mode) right aligned. Unused bits of RB_VALUE (as defined by CON.BM) will not be valid and should be ignored.
0	[31:16]	r	**Reserved** Read as 0; should be written with 0.

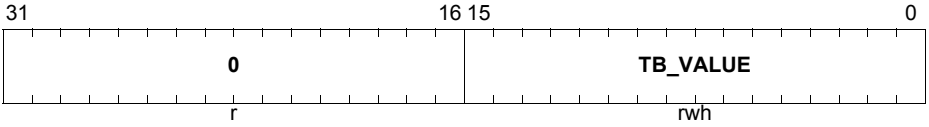
22.3.4 SSCG Specific Registers

The Transmit Buffer Compare Register TB1 contains a copy of the currently transmitted data value.

This register can be written by software. A software write triggers automatically a compare with the receive buffer. This is used for error injection for test purposes, and should not be performed during a real application.

This register is writen also by hardware. When transferring the TB value to the shift register, at the same time in parallel, the same data is written to the TB1 register.

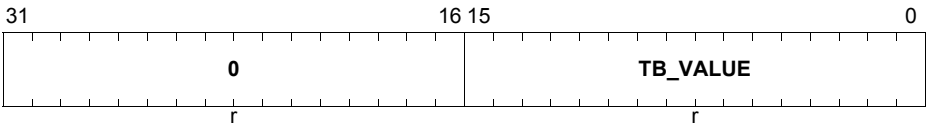
TB1
Transmit Buffer Compare Register (100_H) **Reset Value: 0000 0000$_H$**



Field	Bits	Type	Description
TB_VALUE	[15:0]	rwh	**Transmit Data Register Value** Register TB stores the data value to be transmitted TB_VALUE. Unused bits of TB_VALUE (as defined by CON.BM) are ignored during transmission.
0	[31:16]	r	**Reserved** Read as 0; should be written with 0.

The Transmit Buffer Snapshot Register TB1SNAP contains the last erroneous transmitted data value. This is a read only register

TB1SNAP
Transmit Buffer Snapshot Register (104_H) **Reset Value: 0000 0000$_H$**

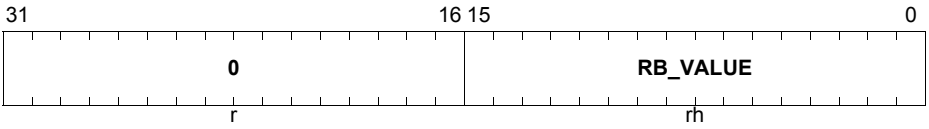


Field	Bits	Type	Description
TB_VALUE	[15:0]	rw	**Transmit Data Snapshot Value** Register TB1SNAP stores the last erroneous transmitted data TB_VALUE. Unused bits of TB_VALUE (as defined by CON.BM) are ignored during transmission.
0	[31:16]	r	**Reserved** Read as 0; should be written with 0.

The Receive Buffer Snapshot Register RBSNAP contains the last erroneous received data value. This is a read only register.

RBSNAP

Receive Buffer Snapshot Register (108_H) Reset Value: 0000 0000_H



Field	Bits	Type	Description
RB_VALUE	[15:0]	rh	**Receive Snapshot Register Value** Register RB contains the last received erroneous data value RB_VALUE right aligned. Unused bits of RB_VALUE (as defined by CON.BM) will not be valid and should be ignored.
0	[31:16]	r	**Reserved** Read as 0; should be written with 0.

The Status Register GSTAT contains sticky status flags for error identification. They are set by hardware in case of an error, and can be cleared only by software, using the GEFM register. They can be set and cleared by software, but can not be cleared by hardware.

Phase error and parity error are flaged in the STAT register and generate an interrupt.

GSTAT
Guardian Status Register **($10C_H$)** **Reset Value: $0000\ 0000_H$**

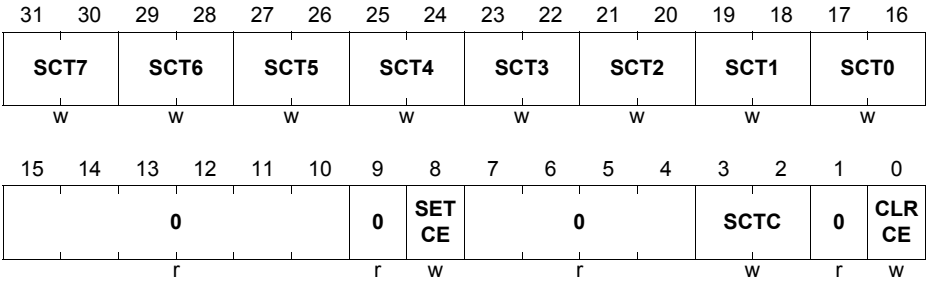
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
								S7	**S6**	**S5**	**S4**	**S3**	**S2**	**S1**	**S0**
r								rh	rh	rh	rh	rh	rh	rh	rh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0													**SCLK**	**0**	**CE**
r													rh	r	rh

Field	Bits	Type	Description
CE	0	rh	**Compare Error Flag** 0_B No compare error 1_B Compare error has occurred
SCLK	2	rh	**SCLK Error Flag** 0_B No error 1_B Error on the SCLK signal
S0, **S1,** **S2,** **S3,** **S4,** **S5,** **S6,** **S7**	16, 17, 18, 19, 20, 21, 22, 23	rh	**SLSx Error Flag** 0_B No error 1_B Error on the corresponding SLS signal
0	1, [15:3], [31:24]	r	**Reserved** Read as 0; should be written with 0.

The Guardian Error Flag Modification Register GEFM contains bits for modifying the error flags and injecting errors per software.

GEFM
Guardian Error Flag Modification Register(110_H) **Reset Value: $0000\ 0000_H$**



Field	Bits	Type	Description
CLRCE	0	w	**Clear Compare Error Flag** 0_B No effect 1_B Clear the compare error flag GSTAT.CE
SETCE	8	w	**Set Compare Error Flag** 0_B No effect 1_B Set the compare error flag GSTAT.CE
SCT0, **SCT1,** **SCT2,** **SCT3,** **SCT4,** **SCT5,** **SCT6,** **SCT7**	[17:16], [19:18], [21:20], [23:22], [25:24], [27:26], [29:28], [31:30]	w	**Set Clear Toggle the SLSx Error Flag** 00_B No action 01_B Set the SLSx error flag GSTAT.Sx. 10_B Clear the SLSx error flag GSTAT.Sx. 11_B Toggle the SLSx error flag GSTAT.Sx. Reading this bit field deliveres 0.
SCTC	[3:2]	w	**Set Clear Toggle the SCLK Error Flag** 00_B No action 01_B Set the error flag GSTAT.SCLK. 10_B Clear the error flag GSTAT.SCLK. 11_B Toggle the error flag GSTAT.SCLK. Reading this bit field deliveres 0.
0	1, 9, [7:4], [15:10]	r	**Reserved** Read as 0; should be written with 0.

The Guardian Enable Register GEN contains bits for enabling and disabling the monitoring of the slave select and clock signals.

GEN
Guardian Enable Register **(114_H)** **Reset Value: 0000 0100_H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0							CEN	SEN 7	SEN 6	SEN 5	SEN 4	SEN 3	SEN 2	SEN 1	SEN 0
r							rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
SEN0, **SEN1,** **SEN2,** **SEN3,** **SEN4,** **SEN5,** **SEN6,** **SEN7**	0, 1, 2, 3, 4, 5, 6, 7	rw	**Slave Select x Monitoring Enable** 0_B Disabled (default value) 1_B Enabled
CEN	8	w	**Clock Monitoring Enable** 0_B Disabled 1_B Enabled (default value)
0	[31:9]	r	**Reserved** Read as 0; should be written with 0.

22.4 SSCG0 Module Implementation

This section describes SSC / SSCG modules interfaces with the clock control, port connections, interrupt control, and address decoding.

22.4.1 Module Identification Registers

The reset values of the SSCGx_ID module identification register is 0085 C0XX$_H$.

22.4.2 Interfaces of the SSCG Modules

Figure 22-6 shows the interconnections of the SSC / SSCG subsystem.

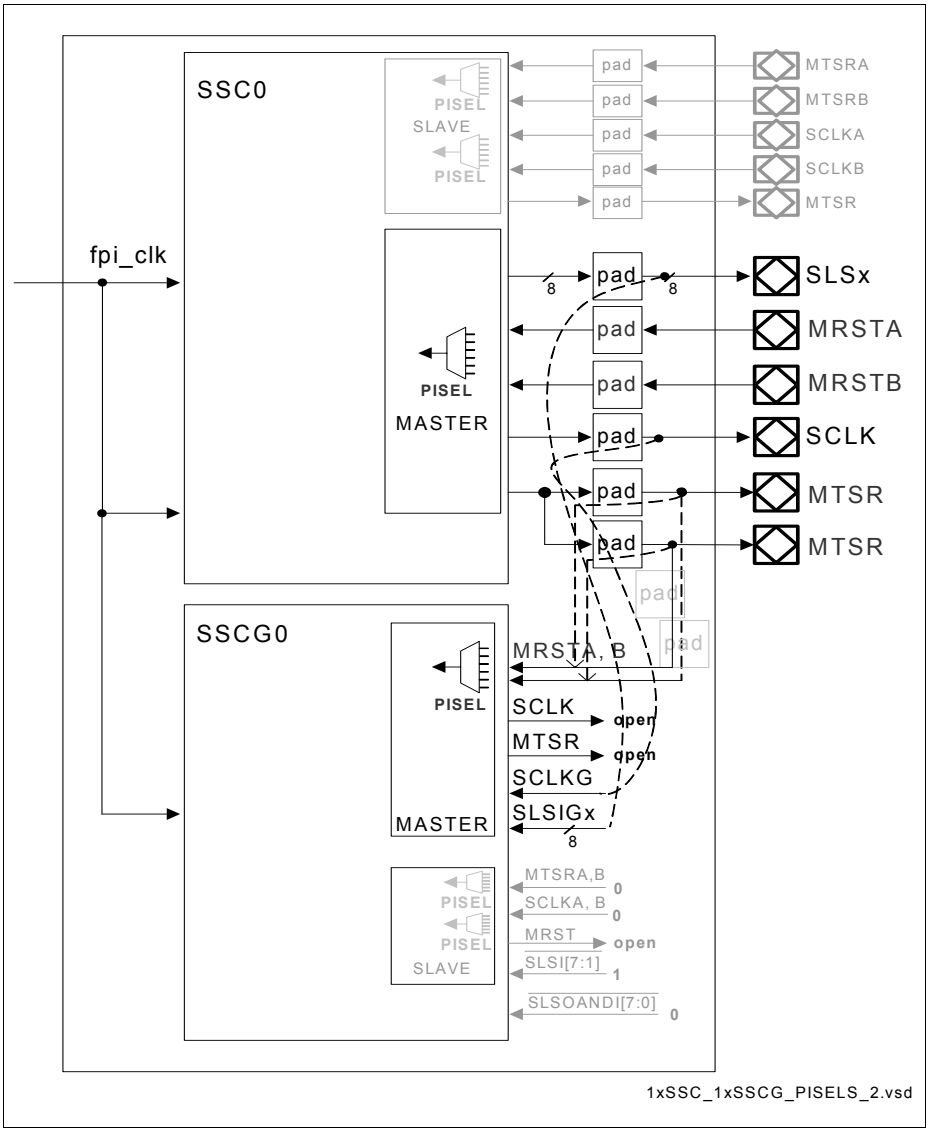


Figure 22-6 SSC0/SSC1/SSCG01 Subsystem Interconnections

The PISEL register of the SSCG0 select the particular output used by the SSC in an application which is to be monitored. On the other hand, the PISEL registers of the SSC0 selects the inputs of the SSC module which are used in the application.

22.4.3 On-Chip Connections

This section describes the on-chip connections of the SSC0/SSCG0 modules.

DMA Requests

The SSCG does not have its own DMA requests. It is always served in parallel by the SSC requests.

22.4.3.1 Receive Input Selection

The MRSTG inputs (master receive) of the SSC Guardian module are mapped to some pins where the MTSR (master transmit) outputs of the corresponding SSC are connected. The alternative inputs A/B of each MRSTG are selected via the corresponding PISEL register of the SSC Guardian.

The PISEL register of the SSCG is normally programmed in parallel with the PISEL register of the SSC, but it can be reprogammed afterwards, if needed.

Table 22-3 Receive Input Selection

Receive Input	Connected to	Selected by
SSCG0_MRSTG0 (A/B)	P10.1	SSCG0_PISEL.MRIS = X_B
SSCG1_MRSTG1 (A/B)	P6.4	SSCG1_PISEL.MRIS = X_B
SSCG2_MRSTG2A SSCG2_MRSTG2B	P4.1 P18.1	SSCG2_PISEL.MRIS = 0_B SSCG2_PISEL.MRIS = 1_B
SSCG3_MRSTG3A SSCG3_MRSTG3B	0 P7.1	SSCG3_PISEL.MRIS = 0_B SSCG3_PISEL.MRIS = 1_B

22.4.4 SSC0/SSC1 Module Related External Registers

Figure 22-7 summarizes the module-related external registers which are required for SSC0/SSC1 programming (see also **Figure 22-5** for the module kernel specific registers).

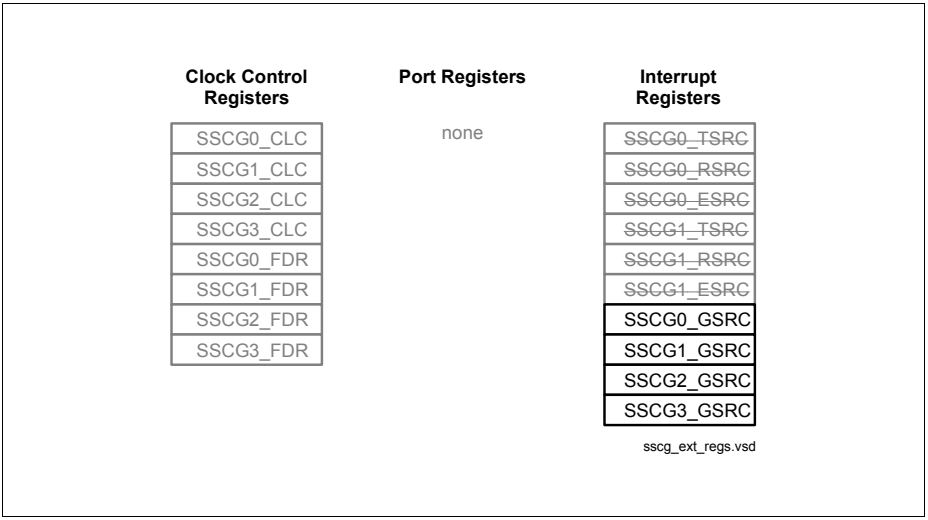


Figure 22-7 SSC0/SSC1 Implementation-specific Special Function Registers

22.4.4.1 Clock Control

Each SSCG module has two clock signals:

- f_{CLC0}
  This is the module clock that is used inside the SSC kernel for control purposes such as clocking of control logic and register operations. The frequency of f_{CLC0} and f_{CLC1} is always identical to the system clock frequency f_{FPI} The clock control registers SSC0_CLC and SSC1_CLC make it possible to enable/disable f_{CLC0} and f_{CLC1} under certain conditions.
- f_{SSCG0}
  This clock is the module clock that is used in the SSCG as input clock of the baud rate generator, which finally determines the baud rate of the serial data. The fractional divider registers SSCG0_FDR and SSCG1_FDR control the frequency of f_{SSCG0} and f_{SSC1} and make it possible to enable/disable it independently of f_{CLC0} and f_{CLC1}.
  The Baud Rate Timer Reload Register SSCG0_BR and SSCG1_BR define serial data baud rate dependent from the frequency of f_{SSCG0} and f_{SSCG1}.

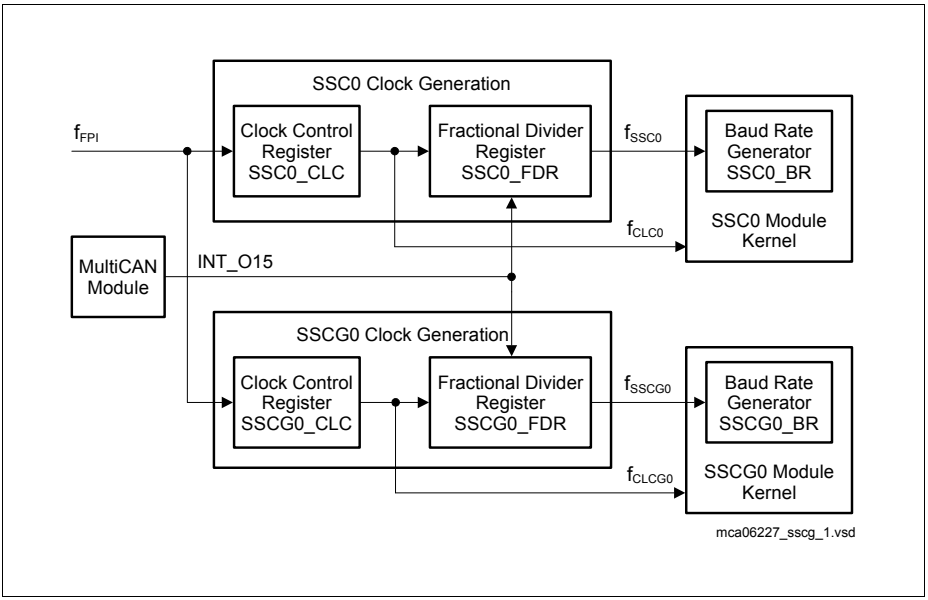


Figure 22-8 SSC Clock Generation

Output signal CAN_INT_O15 of the MultiCAN module can be used for external clock enable control of the fractional divider.

The following formulas define the frequency of f_{SSC0} or f_{SSC1}

$$f_{SSCx} = f_{FPI} \times \frac{1}{n} \text{ with n = 1024 - FDR.STEP} \quad (22.1)$$

$$f_{SSCx} = f_{FPI} \times \frac{n}{1024} \text{ with n = 0-1023} \quad (22.2)$$

Note: In SSC Master Mode, the maximum shift clock frequency is $f_{SSCx}/2$. In SSC Slave Mode, the maximum shift clock frequency is $f_{SSCx}/4$.

Combined with the formulas of the baud rate generator and the fractional divider, the resulting serial data baud rate is defined by:

$$\text{Baud rate}_{SSC} = \frac{f_{FPI}}{2 \times (\text{BR.BR\_VALUE} + 1) \times (1024 - \text{FDR.STEP})} \quad (22.3)$$

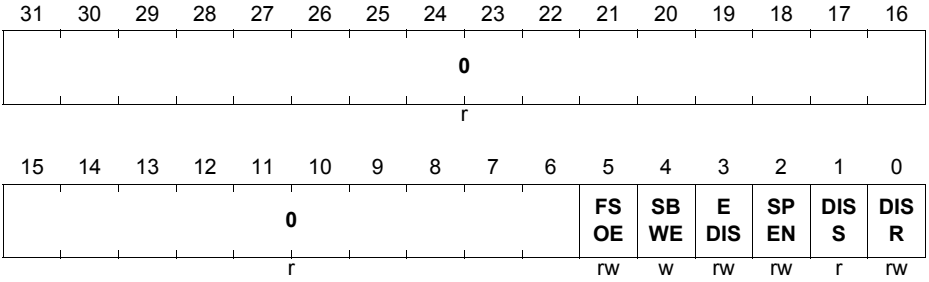
$$\text{Baud rate}_{SSC} = \frac{f_{FPI} \times \text{FDR.STEP}}{2 \times (\text{BR.BR\_VALUE} + 1) \times 1024} \text{ with FDR.STEP = 0-1023} \quad (22.4)$$

*Note: **Equation (22.1)** and **Equation (22.3)** apply to normal divider mode of the fractional divider (FDR.DM = 01_B). **Equation (22.2)** and **Equation (22.4)** apply to fractional divider mode (FDR.DM = 10_B).*

Clock Control Register

The Clock Control Register SSCG0_CLC makes it possible to control (enable/disable) the clock signal f_{CLC0} under certain conditions. Each SSC has its own clock control register.

CLC
Clock Control Register **(00_H)** **Reset Value: 0000 0003$_H$**



Field	Bits	Type	Description
DISR	0	rw	**Module Disable Request Bit** Used for enable/disable control of the module.
DISS	1	r	**Module Disable Status Bit** Bit indicates the current status of the module.
SPEN	2	rw	**Module Suspend Enable for OCDS** Used to enable the suspend mode.
EDIS	3	rw	**Sleep Mode Enable Control** Used to control module's sleep mode.
SBWE	4	w	**Module Suspend Bit Write Enable for OCDS** Determines whether SPEN and FSOE are write-protected.
FSOE	5	rw	**Fast Switch Off Enable** Used to switch off fast clock in Suspend Mode.
0	[31:6]	r	**Reserved** Read as 0; should be written with 0.

Note: After a hardware reset operation, the f_{CLCx} clocks are disabled, and therefore the SSC modules are disabled (DISS set) also.

Fractional Divider Register

The Fractional Divider Registers SSCG0_FDR and SSCG1_FDR control the clock rate of the shift clock f_{SSCG0} and f_{SSCG1}. Each SSCG has its own fractional divider register.

FDR
Fractional Divider Register **($0C_H$)** **Reset Value: $1000\ 0000_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DISCLK	ENHW	SUSREQ	SUSACK	0		RESULT									
rwh	rw	rh	rh	r		rh									

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DM		SC		SM	FDIS	STEP									
rw		rw		rw	rw	rw									

Field	Bits	Type	Description
STEP	[9:0]	rw	**Step Value** Reload or addition value for RESULT.
FDIS	10	rw	**Freeze Disable** This bit controls the freeze function for this module. 0_B Module operates on corrected clock, with reduced modulation jitter. 1_B Module operates on uncorrected clock, with full modulation jitter.
SM	11	rw	**Suspend Mode** SM selects between granted or immediate suspend mode.
SC	[13:12]	rw	**Suspend Control** This bit field determines the behavior of the fractional divider in suspend mode.
DM	[15:14]	rw	**Divider Mode** This bit field selects normal divider mode, fractional divider mode, and off-state.
RESULT	[25:16]	rh	**Result Value** Bit field for the addition result.
SUSACK	28	rh	**Suspend Mode Acknowledge** Indicates state of $\overline{\text{SPNDACK}}$ signal.

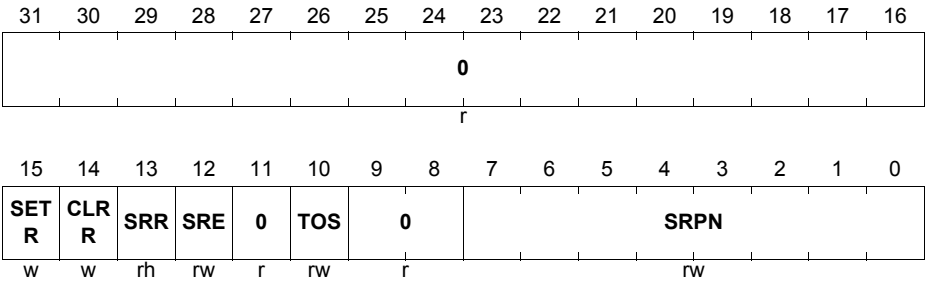
Field	Bits	Type	Description
SUSREQ	29	rh	**Suspend Mode Request** Indicates state of SPND signal.
ENHW	30	rw	**Enable Hardware Clock Control** Controls operation of ECEN input and DISCLK bit.
DISCLK	31	rwh	**Disable Clock** Hardware-controlled disable for f_{OUT} signal.
0	[27:26]	r	**Reserved** Read as 0; should be written with 0.

22.4.4.2 Interrupt Control Registers

The SSC service request control registers are removed from the guardian module. Their read value is constant FFFF FFFF$_H$.´

There is a dedicated guardian service request register GSRC.

GSRC
Guardian Interrupt Service Request Control Register
(1FC$_H$) **Reset Value: 0000 0000$_H$**



Field	Bits	Type	Description
SRPN	[7:0]	rw	**Service Request Priority Number**
TOS	10	rw	**Type of Service Control**
SRE	12	rw	**Service Request Enable**
SRR	13	rh	**Service Request Flag**
CLRR	14	w	**Request Clear Bit**
SETR	15	w	**Request Set Bit**
0	[9:8], 11, [31:16]	r	**Reserved** Read as 0; should be written with 0.

22.4.5 SSCG Address Map

An absolute register address is given by the offset address of the register (given in Table 22-2) plus the module base address (given in Table 22-1).

SSCG has two chip-selects, one common with the SSC module, and one common and dedicated at the same time, OR-ed inside the module to select the address decoder. Additionally, the read signal is combined with the common chip select to suppres a read access parallel to the SSC read access. The common interrupt registers can be read as FFFF FFFF$_H$, but they are not functionally available. Write access has no effect and does not cause a bus error.

Table 22-4 SSCG Address Overview

Module	Base Address	End Address	Note
SSCG0	F031 0000$_H$	F031 00FF$_H$	shared with SSC0
SSCG1	F031 0100$_H$	F031 01FF$_H$	shared with SSC1
SSCG2	F031 0200$_H$	F031 02FF$_H$	shared with SSC2
SSCG3	F031 0300$_H$	F031 03FF$_H$	shared with SSC3
SSCG0	F031 0800$_H$	F031 09FF$_H$	dedicated
SSCG1	F031 0A00$_H$	F031 0BFF$_H$	dedicated
SSCG2	F031 0C00	F031 0DFF	dedicated
SSCG3	F031 0E00	F031 0FFF	dedicated

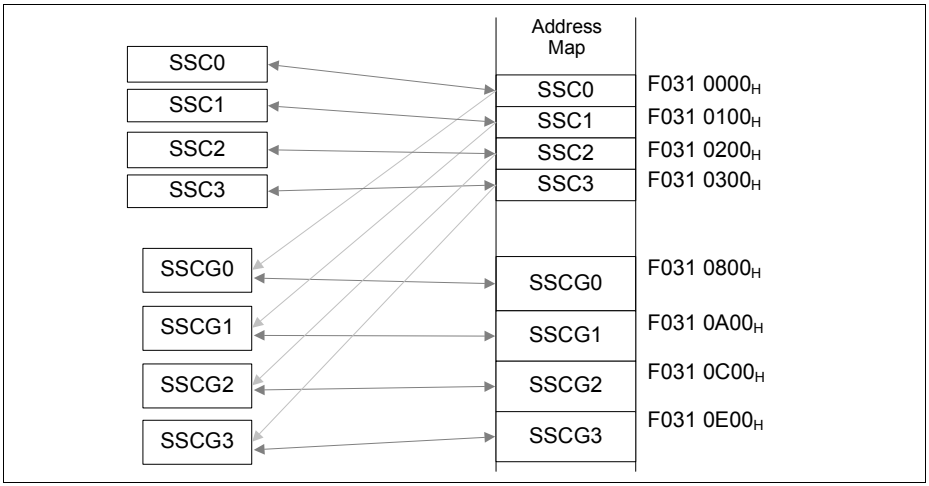


Figure 22-9 SSC and SSCG Address Map

Table 22-5 Address Maps of SSCGx, x = 0 to 3

Short Name	Description	Address offset	Access Mode		Reset Value
			Read	Write	
Address location shared with SSC0, writable in user and supervisor mode					
SSCGx_CLC	SSCGx Clock Control Register	000_H	U, SV	SV, E	0000 0003$_H$
SSCGx_PISEL	SSCGx Port Input Select Register	004_H	U, SV	U, SV	0000 0000$_H$
SSCGx_ID	SSCGx Module Identification Register	008_H	U, SV	BE	0085 C0XX$_H$
SSCGx_FDR	SSCGx Fractional Divider Register	$00C_H$	U, SV	SV, E	1000 0000$_H$
SSCGx_CON	SSCGx Control Register	010_H	U, SV	U, SV	0000 0000$_H$
SSCGx_BR	SSCGx Baud Rate Timer Reload Reg.	014_H	U, SV	U, SV	0000 0000$_H$
SSCGx_SSOC	SSCGx Slave Select Output Control Reg	018_H	U, SV	U, SV	0000 0000$_H$
SSCGx_SSOTC	Slave Select Output Timing Control Reg.	$01C_H$	U, SV	U, SV	0000 0000$_H$
SSCGx_TB	SSCGx Transmit Buffer Register	020_H	U, SV	U, SV	0000 0000$_H$
SSCGx_RB	SSCGx Receive Buffer Register	024_H	U, SV	U, SV	0000 0000$_H$
SSCGx_STAT	SSCGx Status Register	028_H	U, SV	U, SV	0000 0000$_H$
SSCGx_EFM	SSCGx Error Flag Modification Register	$02C_H$	U, SV	U, SV	0000 0000$_H$
–	Reserved	030_H - $0F0_H$	BE	BE	–
~~SSCGx_TSRC~~	~~Transmit Int. Service Req. Control Reg.~~	~~$0F4_H$~~	U, SV	nBE	FFFF FFFF$_H$
~~SSCGx_RSRC~~	~~Receive Int. Service Req. Control Reg.~~	~~$0F8_H$~~	U, SV	nBE	FFFF FFFF$_H$
~~SSCGx_ESRC~~	~~Error Int. Service Req. Control Reg.~~	~~$0FC_H$~~	U, SV	nBE	FFFF FFFF$_H$
Address location dedicated to SSCGx, writable only in supervisor mode					
SSCGx_TB1	SSCGx Transmit Buffer 1	100_H	U, SV	SV	0000 0000$_H$
SSCGx_TB1SNAP	SSCGx Transmit Buffer 1 Snapshot	104_H	U, SV	SV	0000 0000$_H$
SSCGx_RBSNAP	SSCGx Receive Buffer Snapshot	108_H	U, SV	SV	0000 0000$_H$
SSCGx_GSTAT	SSCGx Guardian Status Register	$10C_H$	U, SV	SV	0000 0000$_H$
SSCGx_GEFM	SSCGx Guardian Error Flag Modification	110_H	U, SV	SV	0000 0000$_H$
SSCGx_GEN	SSCGx Enable Register	114_H	U, SV	SV	0000 0100$_H$
–	Reserved	118_H - $1EC_H$	BE	BE	–
SSCGx_GSRC	Guardian Int. Service Req. Control Reg.	$1FC_H$	SV	SV	0000 0000$_H$

23 Micro Second Channel (MSC)

This chapter describes the Micro Second Channel Interface s, MSC0 and MSC1, of the TC1798. It contains the following sections:

- Functional description of the MSC kernel (see **Page 23-3**)
- MSC kernel register descriptions (see **Page 23-36**)
- TC1798 implementation-specific details and registers of the MSC module (port connections and control, interrupt control, address decoding, and clock control, see **Page 23-62**)

*Note: The MSC kernel register names described in **Section 23.2** are also referenced in the TC1798 User´s Manual by the module name prefix “MSC0_” for the MSC0 module and by “MSC1_” for the MSC1 module.*

MSC Applications

The MSC is a serial interface that is especially designed to connect external power devices to the TC1798. The serial data transmission capability minimizes the number of pins required to connect such external power devices. Parallel data information (coming from the timer units) or command information is sent out to the power device via a high-speed synchronous serial data stream (downstream channel). The MSC receives data and status back from the power device via a low-speed asynchronous serial data stream (upstream channel).

Figure 23-1 shows a typical TC1798 application in which an MSC interface controls two power devices. Output data is provided by the GPTA module.

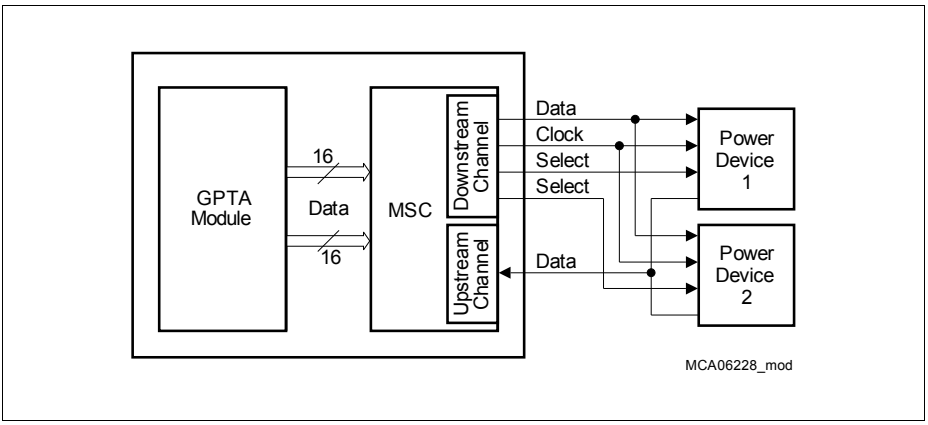


Figure 23-1 MSC to External Power Device Connection

Some applications are:

- Control of the external power switching unit via the downstream channel
- Receiving information back from power switching unit
- Serial connections of the TC1798 to other peripheral devices

23.1 MSC Kernel Description

This section describes the functionality of the MSC kernel.

23.1.1 Overview

The MSC interface provides a serial communication link typically used to connect power switches or other peripheral devices. The serial communication link includes a fast synchronous downstream channel and a slow asynchronous upstream channel. **Figure 23-2** shows a global view of the MSC interface signals.

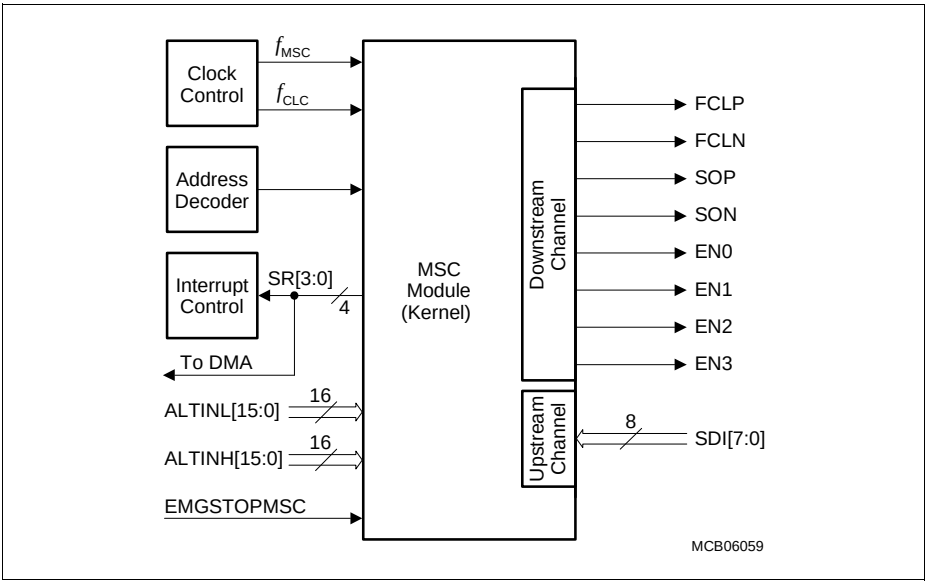


Figure 23-2 General Block Diagram of the MSC Interface

The downstream and upstream channels of the MSC module communicate with the external world via nine I/O lines. Eight output lines are required for the serial communication of the downstream channel (clock, data, and enable signals). One out of eight input lines SDI[7:0] is used as serial data input signal for the upstream channel. The source of the serial data to be transmitted by the downstream channel can be MSC register contents or data that is provided at the ALTINL/ALTINH input lines. These input lines are typically connected to other on-chip peripheral units (for example with a timer unit like the GPTA). An emergency stop input signal makes it possible to set bits of the serial data stream to dedicated values in emergency case.

Clock control, address decoding, and interrupt service request control are managed outside the MSC module kernel. Service request outputs are able to trigger an interrupt or a DMA request.

Features

- Fast synchronous serial interface to connect power switches in particular, or other peripheral devices via serial buses
- High-speed synchronous serial transmission on downstream channel
  - Serial output clock frequency: $f_{FCL} = f_{MSC}/2$ (f_{MSCmax} = 110 MHz)
  - Fractional clock divider for precise frequency control of serial clock f_{MSC}
  - Command, data, and passive frame types
  - Start of serial frame: Software-controlled, timer-controlled, or free-running
  - Transmission with or without SEL bit
  - Flexible chip select generation indicates status during serial frame transmission
  - Emergency stop without CPU intervention
- Low-speed asynchronous serial reception on upstream channel
  - Baud rate: f_{MSC} divided by 4, 8, 16, 32, 64, 128, or 256 (f_{MSCmax} = 110 MHz)
  - Standard asynchronous serial frames
  - Programmable upstream data frame length (16 or 12 bits)
  - Parity error checker
  - 8-to-1 input multiplexer for SDI lines
  - Built-in spike filter on SDI lines
- Selectable pin types of downstream channel interface:
  four LVDS differential output drivers or four digital GPIO pins

23.1.2 Downstream Channel

The downstream channel performs a high-speed synchronous serial transmission of data to external devices. Its 32-bit shift register is divided into two 16-bit parts, SRL and SRH. Each bit of SRL and SRH can be selected to be delivered by the downstream data register DD, by the Downstream Command Register DC, or by two 16-bit wide input signal buses ALTINL and ALTINH.

Figure 23-3 is a diagram of the MSC downstream channel.

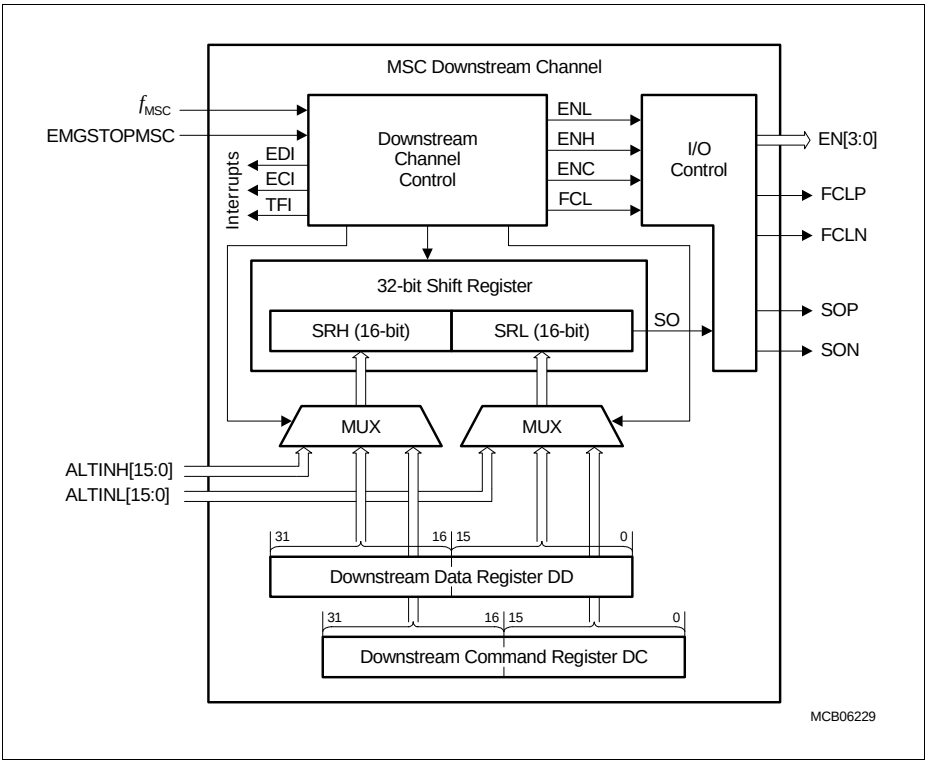


Figure 23-3 Downstream Channel Block Diagram

The enable signals ENL, ENH, and ENC indicate certain phases of the serial transmission in relation to the serial clock FCL. In the I/O control logic, these signals can be combined to four enable/select outputs EN[3:0]. For supporting differential output drivers, the serial clock output FCL and the serial data output SO are available in both polarities, indicated by the signal name suffix “P” and “N”.

The emergency stop input line EMGSTOPMSC is used to indicate an emergency stop condition of a power device. In emergency case, shift register bits can be loaded bit-wise from the downstream data register instead from the ALTINL and ALTINH buses.

23.1.2.1 Frame Formats and Definitions

This section describes the frame formats and definitions of the MSC.

Basic Definitions

Figure 23-4 shows the layout and definitions of a downstream frame. A downstream frame is composed of an active phase and a passive phase. During the active phase, data transmission takes place and during the passive phase no data is transmitted at SO. The active phase is split into two parts: The SRL active phase in which the content of the shift register low part SRL is transmitted, and the SRH active phase in which the content of the shift register high part SRH is transmitted. At the beginning of the SRL and SRH active phase, a selection bit (SELL) can be optionally inserted into the serial data stream. In the frame shown in **Figure 23-4**, SELL is generated at the beginning of the SRL active phase (not for the SRH active phase). The least significant bits of SRL and SRH are sent out first.

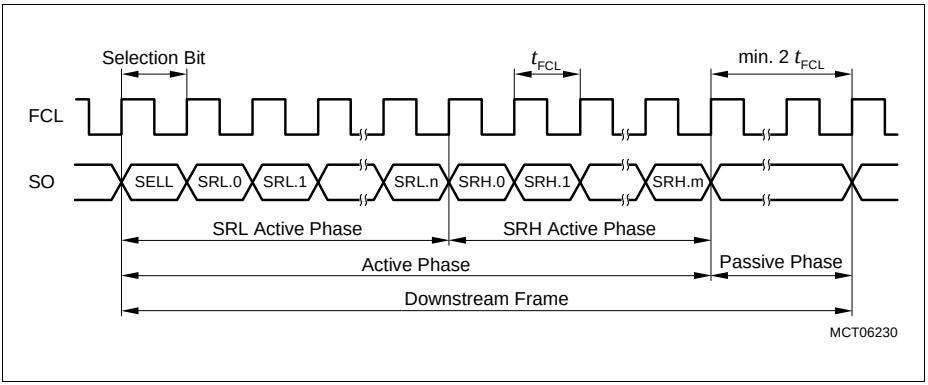


Figure 23-4 Downstream Channel Frame

The MSC downstream channel uses three types of frame formats for operation:

- Command frames, indicated by SELL = 1
- Data frames, indicated by SELL = 0 or SELL bit insertion disabled
- Passive time frame, indicated by ENL = ENH = 0

Command Frames

A command frame has two active phase parts, SRL active phase and SRH active phase. The command frame always starts with a high-level selection bit, independently whether the selection bit insertion (as defined by bit DSC.ENSELL) is enabled or not. The number of the bits transmitted during SRL and SRH active phases (except the selection bit) is defined by bit field DSC.NBC. SRL and SRH are combined to a 32-bit value whose length can be selected from 0 up to 32 bits. In other words, whenever bits of SRH are transmitted, they are always preceded by the transmission of the complete SRL content.

During the active phase of a command frame, the enable output signal ENC becomes active. The enable output signals ENL and ENH remain inactive.

The passive phase of a command frame always has a fixed length of $2 \times t_{FCL}$. The diagram shown in **Figure 23-5** assumes that the FCL clock is only generated during the active phase of the command frame (OCR.CLKCTRL = 0).

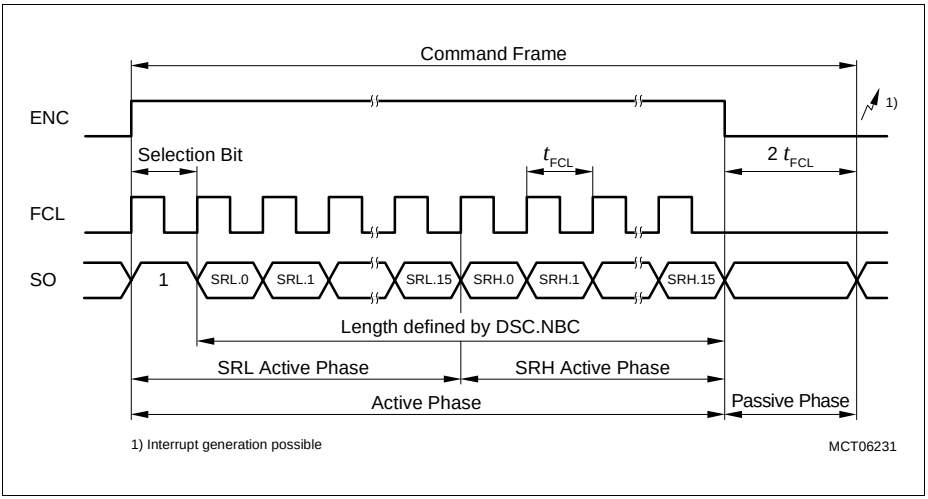


Figure 23-5 Command Frame Layout

Table 23-1 shows the programming of the bits to be transmitted and the resulting length of the complete command frame.

Table 23-1 Command Frame Length

DSC.NBC	SRL/SRH Bits that are Transmitted in Active Phase	Command Frame Length in t_{FCL} Periods
000000_B	No bit shifted out	1 + 0 + 2 = 3
000001_B	SRL[0] shifted out	1 + 1 + 2 = 4
000010_B	SRL[1:0] shifted out	1 + 2 + 2 = 5
000011_B	SRL[2:0] shifted out	1 + 3 + 2 = 6
…	…	…
001111_B	SRL[14:0] shifted out	1 + 15 + 2 = 18
010000_B	SRL[15:0] shifted out	1 + 16 + 2 = 19
010001_B	SRL[15:0] and SRH[0] shifted out	1 + 17 + 2 = 20
010010_B	SRL[15:0] and SRH[1:0] shifted out	1 + 18 + 2 = 21
010011_B	SRL[15:0] and SRH[2:0] shifted out	1 + 19 + 2 = 22
…	…	…
011111_B	SRL[15:0] and SRH[14:0] shifted out	1 + 31 + 2 = 34
100000_B	SRL[15:0] and SRH[15:0] shifted out	1 + 32 + 2 = 35
Other NBC combinations	Reserved; do not use these bit combinations.	

Data Frames

A data frame has two active phase parts, SRL active phase and SRH active phase. The number of bits that are transmitted can be programmed separately for each of these two phases. Bit field DSC.NDBL determines the number of SRL bits that are transmitted during the SRL active phase and DSC.NDBH determines the number of SRH bits that are transmitted during the SRH active phase.

SRL and SRH active phases can start with a low-level selection bit when enabled by bits DSC.ENSELL or DSC.ENSELH.

During the SRL active phase of a data frame, the enable output signal ENL becomes active and during the SRH active phase of a data frame, the enable output signal ENH becomes active. The enable output signal ENC remains inactive.

The length of the data frame's passive phase is variable and is defined by bit field DSC.PPD. It can be within a range of $2 \times t_{FCL}$ up to $31 \times t_{FCL}$. The diagram shown in **Figure 23-6** assumes that the FCL clock is only generated during the active phase of the data frame (OCR.CLKCTRL = 0).

Table 23-2, **Table 23-3**, and **Table 23-4** show the definitions of the five data frame parameters that determine the layout of the data frame.

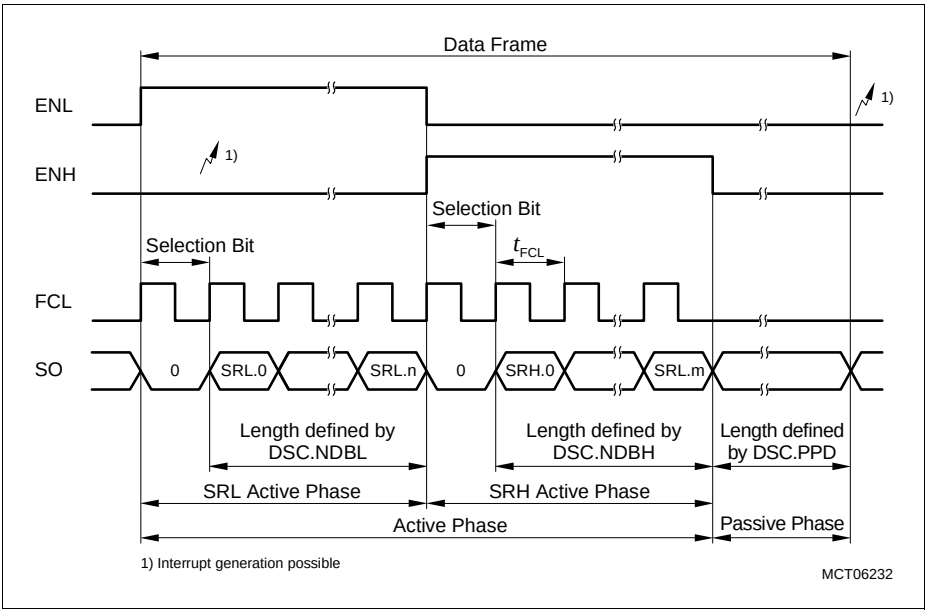


Figure 23-6 Data Frame Layout

Table 23-2 Data Frame Selection Bit Parameters

DSC.ENSELL	Selection Bit	DSC.ENSELH	Selection Bit
0	No selection bit inserted at the beginning of the SRL active phase	0	No selection bit inserted at the beginning of the SRH active phase
1	A low level selection bit is inserted at the beginning of the SRL active phase	1	A low level selection bit is inserted at the beginning of the SRH active phase

Table 23-3 Data Frame SRL/SRH Length Parameters

DSC.NDBL	SRL Bits Transmitted in SRL Active Phase	DSC.NDBH	SRH Bits Transmitted in SRH Active Phase
00000_B	No SRL bit transmitted	00000_B	No SRH bit transmitted
00001_B	SRL[0]	00001_B	SRHL[0]
00010_B	SRL[1:0]	00010_B	SRH[1:0]
00011_B	SRL[2:0]	00011_B	SRH[2:0]
…	…	…	…
01111_B	SRL[14:0]	01111_B	SRH[14:0]
10000_B	SRL[15:0]	10000_B	SRH[15:0]
Other bit combinations	Reserved; do not use these bit combinations.	Other bit combinations	Reserved; do not use these bit combinations.

Table 23-4 Data Frame Passive Phase Length

DSC.PPD	Passive Phase Length
00000_B	$2 \times t_{FCL}$
00001_B	$2 \times t_{FCL}$
00010_B	$2 \times t_{FCL}$
00011_B	$3 \times t_{FCL}$
…	…
01110_B	$30 \times t_{FCL}$
01111_B	$31 \times t_{FCL}$

The following formula determines the number of t_{FCL} cycles of a data frame: All parameters (bits and bit fields) are located in register DSC.

$$\text{Number of cycles} = \text{ENSELL} + \text{NDBL} + \text{ENSELH} + \text{NDBH} + \text{PPD} \quad (23.1)$$

Note that in the formula above, PPD must be set to 2 when DSC.PPD $\leq 00010_B$.

Passive Time Frames

A passive time frame has the length defined by the five data frame parameters according **Equation (23.1)**. They are generated only in Data Repetition Mode. Under special conditions (command frame insertion), passive time frames can be shortened (see **Figure 23-9**).

During passive time frames, the data output SO have to be considered as invalid at the receiving device and the clock output FCL may toggle or not (as selected by bit OCR.CLKCTRL). The ENL and ENH enable signals remain at low level during a passive time frame.

23.1.2.2 Shift Register Operation

This section describes the SRL and SRH shift register loading.

SRL Shift Register Loading

During the SRL/SRH shift register load operation at the beginning of each downstream frame transmission, several parameters determine which information is loaded into the bits of the shift register. **Figure 23-7** shows the logic that is implemented for the SRL shift register loading operation. The logic for the SRH shift register loading operation is equivalent to the one for the SRL register. Its differences in data sources and register controls are described later in this section.

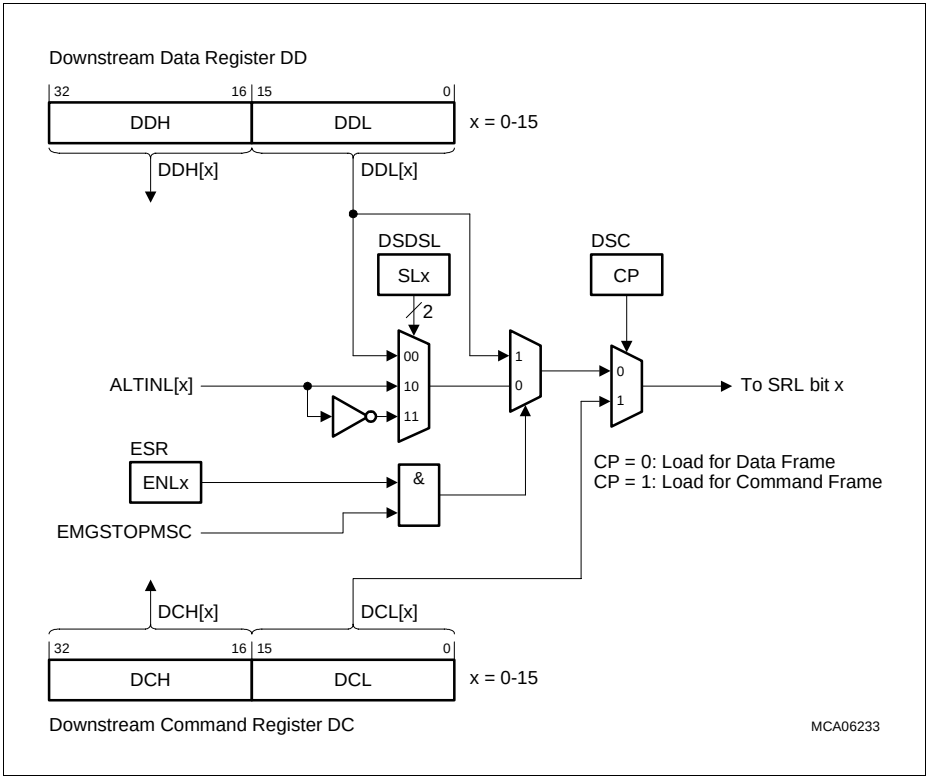


Figure 23-7 SRL Shift Register Data Loading Control

Four data sources can be selected for each SRL bit by using several control bits and one control signal:

- ALTINL input line (non-inverted)
- ALTINL input line (inverted)
- Bit of DD.DDL (downstream data register)
- Bit of DC.DCL (downstream control register)

When SRL is loaded for data frame transmission (DSC.CP = 0), bit fields DSDSL.SLx determine bit-wise which data is loaded into SRL bit x. The data source selection as controlled by DSDSL.SLx will only be effective when EMGSTOPMSC is inactive (at low level). When EMGSTOPMSC = 1 (active) during the load operation, all SRL[x] bits that are enabled for the emergency stop feature (bit ESR.ENLx = 1) are loaded directly with the corresponding bit DDL[x] of the downstream data register DD.

When SRL is loaded for command frame transmission (DSC.CP = 1), always the lower 16-bit part DCL of the downstream control register is loaded completely into SRL.

Table 23-5 summarizes all SRL data source selection capabilities (x = 0-15).

Table 23-5 SRL Data Source Selection Capabilities

DSC.CP	DSDSL.SLx	ESR.ENLx	EMGSTOPMSC	Selection
0	00_B	0	–	Bit DD.DDL[x] is loaded into SRL[x].
	01_B			Reserved.
	10_B			State of ALTINL[x] input is loaded into SRL[x].
	11_B			Inverted state of ALTINL[x] input is loaded into SRL[x].
	XX_B	1	1	Bit DD.DDL[x] is loaded into SRL[x].
1	XX_B	X	X	Bit fields DCL and DCH are completely loaded into SRL and SRH, respectively.

SRH Shift Register Loading

The SRH shift register load operation is equivalent to the SRL shift register load operation. The following differences must be taken into account for SRH shift register loading:

- Input lines ALTINH are connected instead of ALTINL input lines.
- DSDSH register bits control data source selection instead of DSDSL register.
- Emergency stop is enabled by ESR.ENHx bits instead of ESR.ENLx bits.
- Bits of the downstream data register high part DDH are selected instead of DDL.
- Downstream control register high part DCH is selected instead of DCL.

23.1.2.3 Transmission Modes

The downstream channel of the MSC makes it possible to select between two transmission modes:

- Triggered Mode, selected by DSC.TM = 0, or
- Data Repetition Mode, selected by DSC.TM = 1

Triggered Mode

In Triggered Mode, command frames or data frames are sent out as a result of a software event. When a frame transmission has been finished and no further frame transmission has been requested, the downstream channel returns to idle state and waits for the next frame transmission to be triggered by software.

When the Downstream Command Register DC is written, the command pending bit DSC.CP becomes set and a command frame will be immediately started and sent out if the downstream channel is idle. If a data or command frame is currently processed and output, the command frame transmission is delayed, and started when the active downstream frame has been finished. The command pending bit DSC.CP becomes cleared by hardware when the first bit of the command frame is sent out.

If the downstream channel is idle and the data pending bit DSC.DP is set by writing bit ISC.SDP with 1, a data frame will be immediately started and sent out if the downstream channel is idle. If a data frame or a command frame is currently processed and output, the data frame transmission is delayed and started when the active downstream frame has been finished. The data pending bit DSC.DP becomes cleared by hardware when the first bit of the data frame is sent out.

A command frame always has priority over the data frame. This means that if both frame pending bits are set (DSC.DP = DSC.CP = 1), the command frame will always be sent first. Therefore, a pending data frame transmission will be delayed as long as no further command frame transmission is running or requested.

Figure 23-8 is a flow diagram of the Triggered Mode. This diagram especially shows the behavior of the data and command pending bits DSC.DP and DSC.CP. If both frame pending bits are set (DSC.DP = DSC.CP = 1), the command frame will always be sent first, followed by the data frame (assuming no further command frame has been requested).

The type of the active frame that is currently processed and output is indicated by two status flags: DSS.DFA is set during a data frame transmission and DSS.CFA is set during a command frame transmission. Further, the downstream counter DSS.DC indicates the number of shift clock periods that have been elapsed since the start of the current frame.

In Triggered Mode, the shift register loading event as described in **Section 23.1.2.2** occurs just before a command or data frame transmission is started.

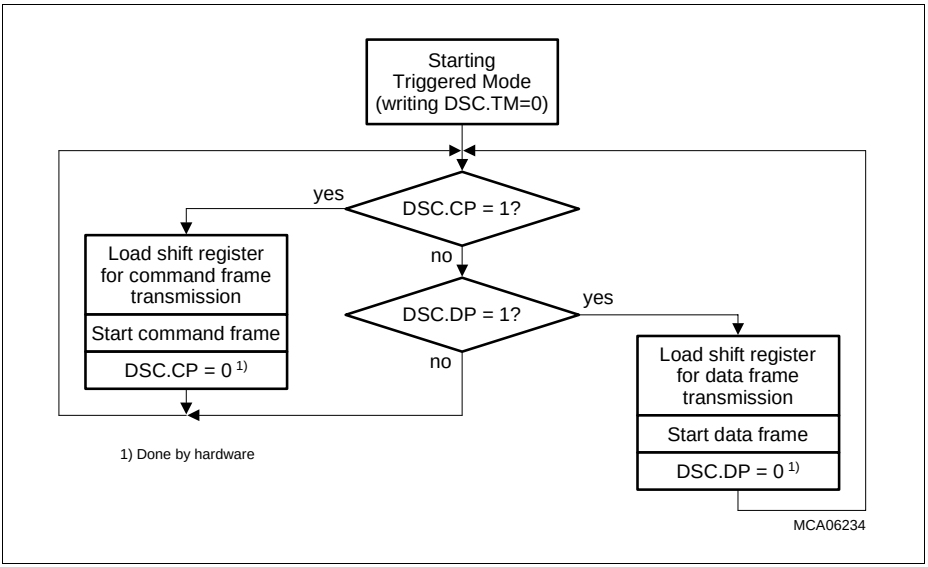


Figure 23-8 Triggered Mode Flow Diagram

Data Repetition Mode

In Data Repetition Mode, data frames are sent out continuously without any software interaction. In the time gap between two consecutive data frames, passive time frames can be inserted. The number of passive time frames to be inserted (0 to 15) is defined by bit field DSS.NPTF. The duration of data frame (t_{DF}) and passive time frames (t_{PTF}) is determined by the five data frame parameters (see **Equation (23.1)**). These parameters determine time reference points (TRP) at which a data or passive time frames is started (see diagram A in **Figure 23-9**).

The automatic data frame generation is controlled by the data pending bit DSC.DP. This bit is set near the end of the last transmitted passive time frame. At the next TRP, a data frame is started (if no command frame has been requested) and DSC.DP is cleared again by hardware after the data frame has been started. Data Frames are always aligned to time reference points. This means they always start at a TRP. Passive time frames can be shortened. This is especially the case when command frames are inserted.

Continuous data frame transmission can be interrupted by insertion of command frames. Command frames are initiated by software. When the downstream control register DSC is written, the command pending bit DSC.CP is set by hardware. CP = 1 indicates that the MSC starts a command frame at the next TRP, independently of whether a data

frame (indicated by DSC.DP = 1) or passive time frame should be started with the next TRP. This means also that command frames are always aligned to time reference points.

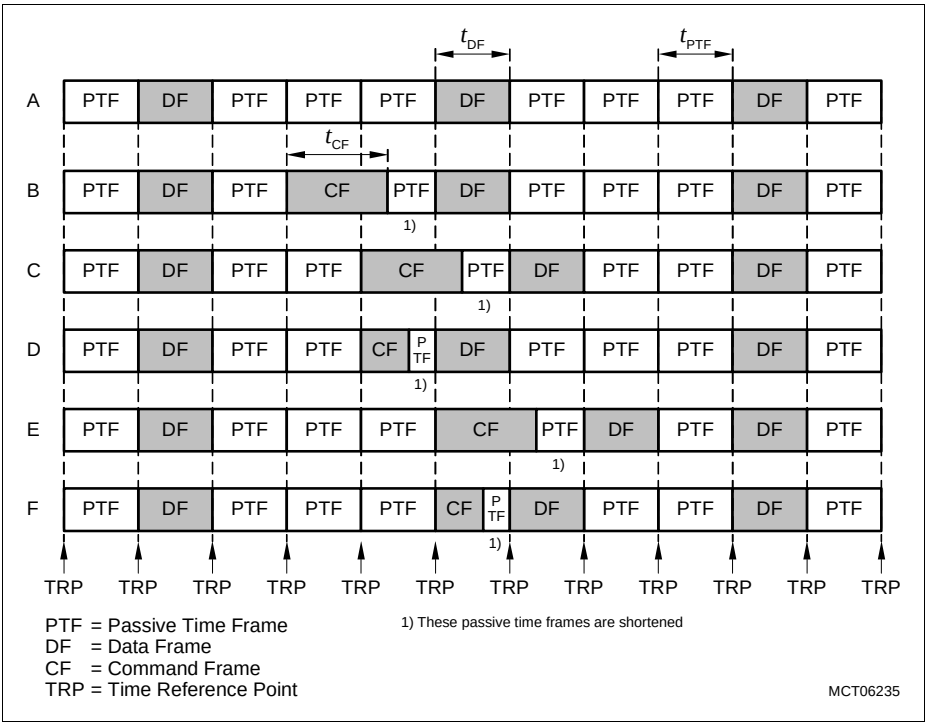


Figure 23-9 Data Repetition Mode Frame Examples with DSS.NPTF = 0011_B

Diagrams B to F in **Figure 23-9** show the command frame insertion in Data Repetition Mode.

In diagram B, a command frame has been requested during the first passive time frame after the data frame, and is inserted at the next TRP. In diagrams C and D, a command frame has been requested during the second passive time frame, and is inserted at the time reference point of the last nominal passive time frame.

When the command frame and data frame is not of the same length (this is the case in diagram B to F), a shortened passive time frame is inserted until the next TRP is reached. This ensures that the next data or normal passive time frame is again aligned to a TRP.

Figure 23-10 is a flow diagram of the Data Repetition Mode. This diagram especially shows the behavior of the data and command pending bits DSC.DP and DSC.CP. If both frame pending bits are set (DSC.DP = DSC.CP = 1), the command frame will always be

sent first, followed by the data frame when the next TRP is reached (assuming no further command frame has been requested).

When the last passive frame is transmitted, DSC.DP becomes set by hardware. This triggers the start of a data frame when the next TRP is reached.

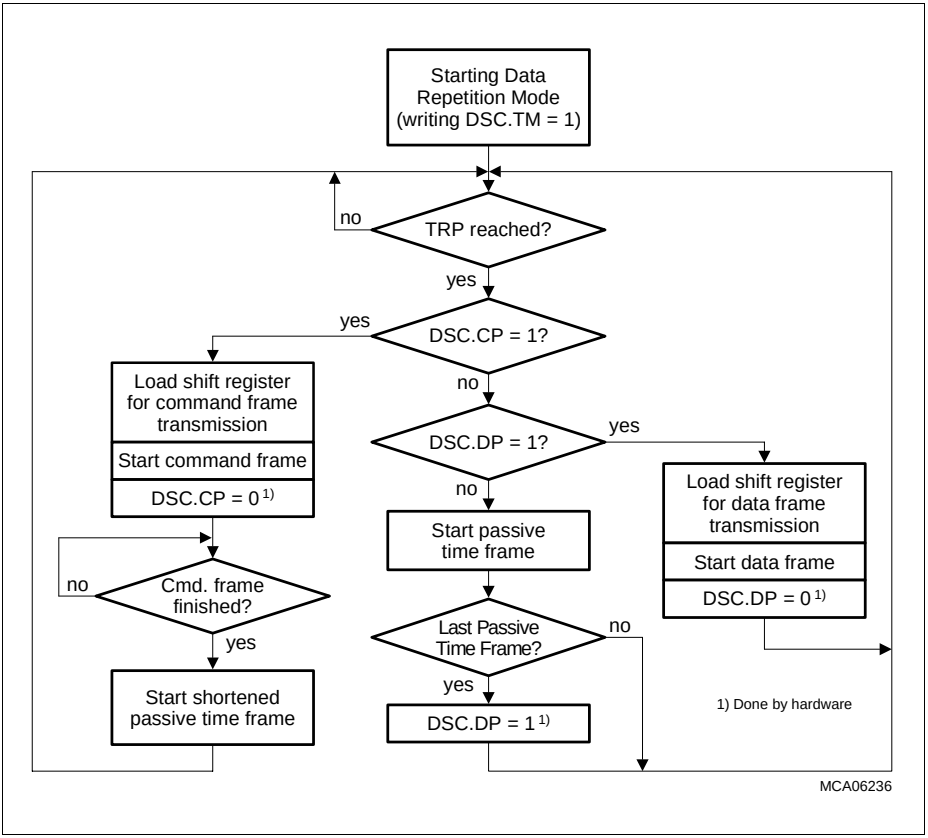


Figure 23-10 Data Repetition Mode Flow Diagram

The type of the active frame (data or command frame) that is currently processed and output is indicated by two status flags: DSS.DFA is set during a data frame transmission and DSS.CFA is set during a command frame transmission. Further, the downstream counter DSS.DC indicates the number of shift clock periods that have been elapsed since the start of the current data, command, or passive time frame.

As in Triggered Mode, the shift register loading event as described in **Section 23.1.2.2** occurs in Data Repetition Mode just before a TRP, this means shortly before a command or data frame transmission is started.

Passive Frame Counter in Data Repetition Mode

In Data Repetition Mode, a passive time frame counter DSS.PFC indicates how many time frames have been already transmitted after the last regular data frame occurrence. The passive time frame counter counts up from 0000_B to the value which has been written into bit field DSS.NPTF (number of passive time frames). DSS.PFC = 0000_B indicates that a data frame is requested for transmission.

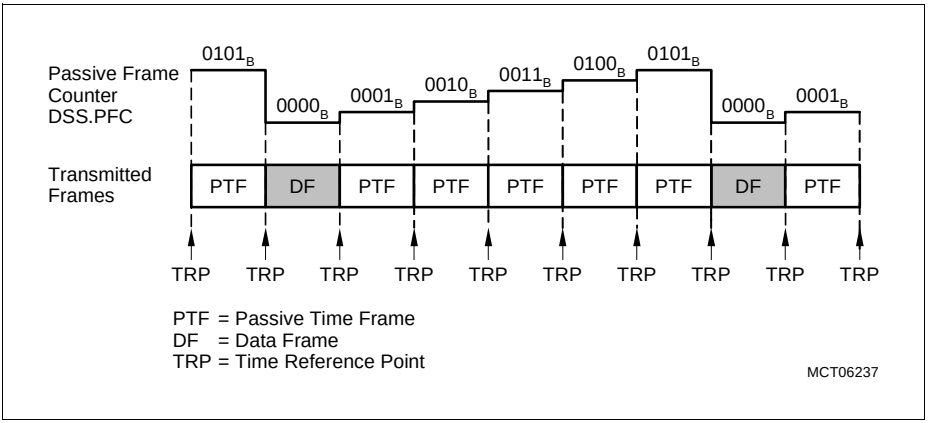


Figure 23-11 Passive Frame Counter Operation (with DSS.NPTF = 0101_B)

23.1.2.4 Downstream Counter and Enable Signals

During downstream channel operation, a 7-bit downstream counter DSS.DC is counting FCL shift clock periods. With the loading of the shift register, the downstream counter is reset to 00_H and started for counting up to the end of the downstream frame (end of passive phase).

In Triggered Mode, the downstream counter stops counting at the end of the passive phase and waits until a new downstream frame is started.

In Repetition Mode, the downstream counter does not stop at the end of the passive phase but is reset and starts counting up again with the next frame, independently whether a data frame, command frame, or passive time frame is started as next frame.

Figure 23-12 shows an example of downstream channel data frame transmission. In this example, the selection bit for the SRL active frame is enabled (ENSELL = 1), and the selection bit for the SRH active frame is disabled (ENSELH = 0). With loading of the shift register SRL/SRH, the downstream counter is reset and then starts counting up with each FCL clock until the end of the passive phase. ENL is set to high level at the beginning of the SRL active frame selection bit.

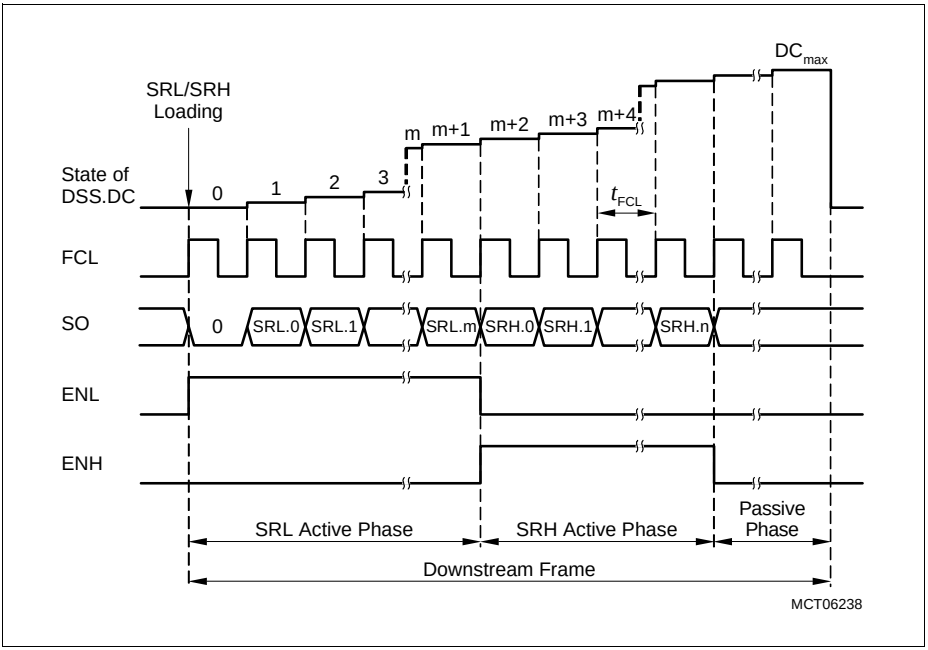


Figure 23-12 Shift Clock Counting: Data Frame with ENSELL = 1 and ENSELH = 0

When the selection bit for the SRL active frame is disabled (ENSELL = 0, see **Figure 23-13**), the loading of the shift register SRL/SRH (and reset of the downstream counter) occurs one FCL clock cycle before the first data bit SRL.0 is output. ENL is set to high level with the beginning of the first data bit SRL.0.

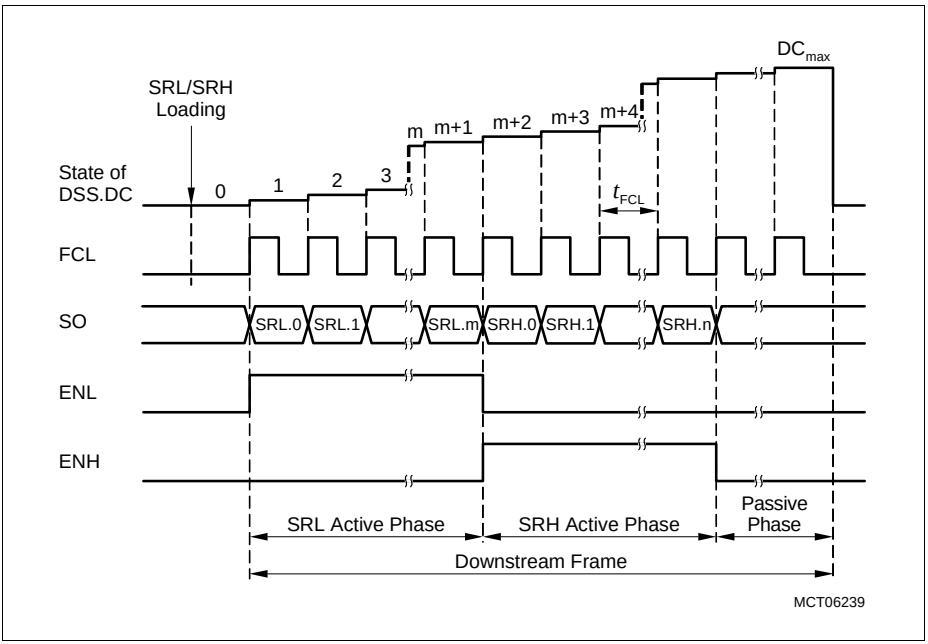


Figure 23-13 Shift Clock Counting: Data Frame with ENSELL = 0 and ENSELH = 0

23.1.2.5 Baud Rate

The baud rate of the downstream channel's serial transmission is defined by the frequency of the serial clock FCL, and is always $f_{MSC}/2$. The f_{MSC} generation is device specific and depends on the implementation of the MSC module. The TC1798 specific clock generation is described on **Page 23-65**.

23.1.2.6 Abort of Frames

Only a reset condition of the device can abort a current transmission. The MSC module does not start a new frame transmission when the downstream channel becomes disabled, the suspend mode is requested, or the sleep mode is entered. If one of these three conditions becomes active during a running frame transmission, the frame transmission is completely finished before the requested abort state is entered. Note that in this case no time frame finished interrupt is generated any more.

23.1.3 Upstream Channel

The MSC upstream channel is an asynchronous serial receiver based on the standard asynchronous data transfer protocol. It is dedicated to receive a serial data stream from a peripheral device via its serial data input SDI, using two specific data frame formats.

Figure 23-14 is a block diagram of the MSC upstream channel.

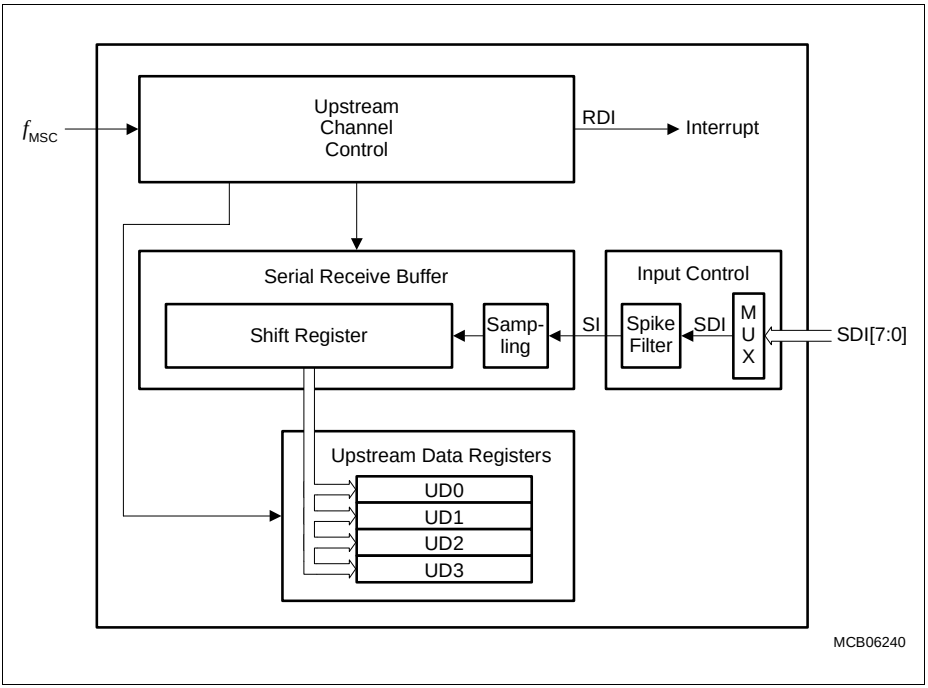


Figure 23-14 Upstream Channel Block Diagram

The incoming data at SI is sampled after it has been filtered for spikes. The detected logic states of the serial input are clocked into a shift register. After the complete reception of the serial data frame, the content of the shift register is transferred into one of the four data registers, and an interrupt can be generated optionally.

The reception baud rate is directly coupled to the module clock f_{MSC}, and can be within a range of $f_{MSC}/4$ up to $f_{MSC}/256$.

23.1.3.1 Data Frames

The asynchronous data frames used by the upstream channel include four basic parts:

1. One start bit, always at low level
2. An 8-bit data field D[7:0] with LSB first
3. An optional 4-bit address field A[3:0] with LSB first
4. One parity bit and two stop bits, that are always at high level

As shown in **Figure 23-15**, the 16-bit upstream data frame includes an additional 4-bit address field. The upstream frame type is selected by bit USR.UFT.

- USR.UFT = 0: 12-bit upstream data frame selected
- USR.UFT = 1: 16-bit upstream data frame with 4-bit address field selected

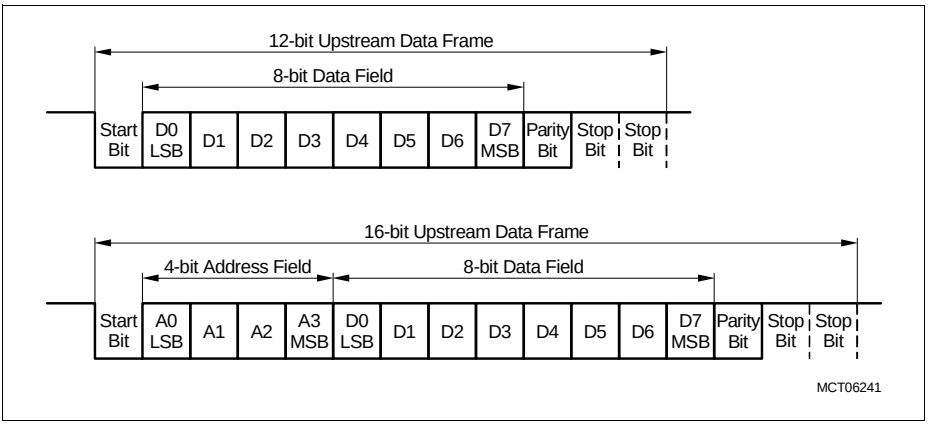


Figure 23-15 Upstream Channel Frame Types

23.1.3.2 Parity Checking

The incoming parity bit of the data frames can be checked by the upstream channel. When a parity error is detected, the parity error flag PERR in the related Upstream Data Register UDx is set. Note that a setting of the parity error flag PERR does not generate an interrupt. The PERR bits must be checked by software. The UDx registers also store the parity bit of the incoming data frame (UDx.P) and the parity bit that is generated internally (UDx.IPF).

Bit USR.PCTR determines the parity mode, even or odd, that is selected for parity checking. With USR.PCTR = 0, even parity mode is selected. Even parity means that the parity bit is set on an odd number of 1s in the data field (12-bit upstream data frame) or in the address plus data field (16-bit upstream data frame). With USR.PCTR = 1, odd parity mode is selected. In odd parity mode, the parity bit is set on an even number of 1s of the related data.

The parity checking logic in the upstream channel also controls whether start bit and the two stop bits of the upstream data frame are at correct logic level. If the start bit is not at low level and the two stop bits are not at high level at the end of the frame reception, the parity error flag UDx.PERR is set, too.

23.1.3.3 Data Reception

The reception of the upstream frame is started with a falling edge (1-to-0 transition) on the SI line. When the start bit is detected, serial reception is enabled and the receive circuit begins to sample the incoming serial data and to buffer it in the receive buffer. After the second stop bit has been detected, the content of the receive buffer is transferred to one of four upstream data registers UDx. The receive circuit then waits for the next start bit (1-to-0 transition) at the SI line. When the content of the receive buffer has been transferred to UDx, the valid bit UDx.V is set by hardware, and a receive interrupt can be generated.

*Note: The SI input line is the filtered non-inverted (OCR.ILP = 0) or inverted (OCR.ILP = 1) SDI input signal. The SI input signal selection is described on **Page 23-30**).*

Frame Reception with Address Field

Frame reception for a 16-bit data frame (see **Figure 23-16**) is selected by USR.UFT = 1. When the content of the receive buffer has been received completely, it is transferred to one of the four UDx registers. The two most significant address bits A[3:2] of the received 4-bit address field select the number x of register UDx in which the received frame content is stored. Register UDx is loaded with the two least significant address bits A0 and A1 (UDx.LABF), the 8-bit data (UDx.DATA), the received parity bit (UDx.P), the calculated parity bit (UDx.IPF), and the parity checking result (UDx.PERR). Finally, the valid bit UDx.V is set to indicate that the UDx register contains valid data.

The current state of the frame reception is indicated by the content of an upstream counter that is readable via bit field USR.UC. The upstream counter is a 5-bit counter that counts the upstream frame bits during reception. As shown in **Figure 23-16**, the upstream counter is loaded with 10000_B at the detection of a start bit. It counts down and is again at 00000_B when the second stop bit has been detected and the frame reception is finished.

The state of the serial input data line SI is sampled in the middle of a bit cell and shifted into the receive buffer at the end of the bit cell. The frequency of the shift clock f_{SHIFT} depends the selected baud rate (see **Page 23-25**).

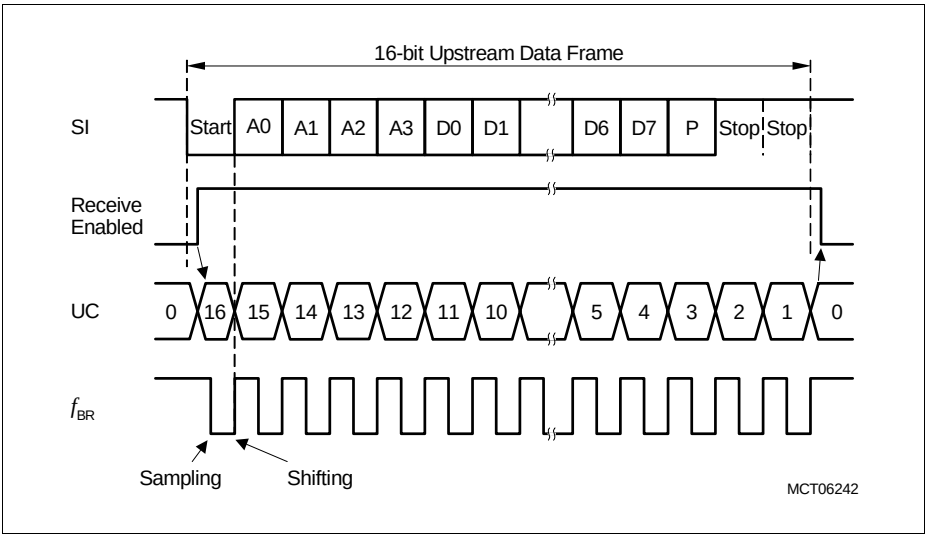


Figure 23-16 16-bit Upstream Reception

Data Reception without Address Field

Frame reception for a 12-bit data frame is selected by USR.UFT = 0. The reception scheme is comparable with that of the 16-bit data frame reception but there are a few differences:

- The upstream counter is initially loaded with 01100_B.
- The received frame content is always stored in register UD0.
- Bit field UD0.LABF is always loaded with 00_B when the frame is stored.

23.1.3.4 Baud Rate

The baud rate of the upstream channel is derived from the MSC module clock f_{MSC}. Figure 23-17 shows the configuration of the upstream channel clock circuitry.

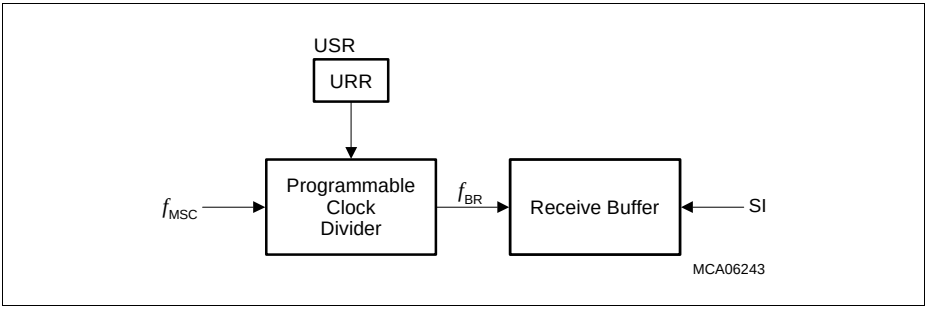


Figure 23-17 Upstream Channel Clock Circuitry

The serial data input SI is evaluated with the baud rate clock f_{BR} in the middle of each bit cell, and latched in case of a data bit. The baud rate clock f_{BR} is derived from f_{MSC} by a programmable clock divider. The frequency of f_{BR} determines the width of a received bit cell and therefore the baud rate for the received data. The content of bit field USR.URR selects the baud rate according Table 23-6. The resulting baud rate formula is:

$$\text{Baud rate}_{\text{MSC Upstream Channel}} = \frac{f_{MSC}}{DF} \quad (23.2)$$

Table 23-6 Upstream Channel Divide Factor DF Selection & Baud Rate

USR.URR	Divide Factor DF	Baud Rate
000_B	reception disabled	–
001_B	4	$f_{MSC}/4$
010_B	8	$f_{MSC}/8$
011_B	16	$f_{MSC}/16$
100_B	32	$f_{MSC}/32$
101_B	64	$f_{MSC}/64$
110_B	128	$f_{MSC}/128$
111_B	256	$f_{MSC}/256$

Note: With the USR.URR = 000_B the upstream channel is disabled and data reception is not possible.

The content of bit field USR.URR determines the operation of an internal sampling reload counter that is clocked with f_{MSC}. **Figure 23-18** shows the operation of the sampling counter at the beginning of an upstream frame with a divide factor DF of 8 (USR.URR = 010_B is equal to DF = 8) which means eight sampling clocks per each frame bit cell.

When the upstream channel is in idle state, it waits for a falling edge (1-to-0 transition) at SI. Therefore, the sample counter starts counting up and is reset when the selected divide factor DF as shown in **Table 23-6** is reached. In the middle of the sampling counter's count range, the logic state at SI is evaluated and, in case of a data bit, latched in the receive buffer's shift register. With the reload of the sampling counter, the shift register is shifted by one bit position.

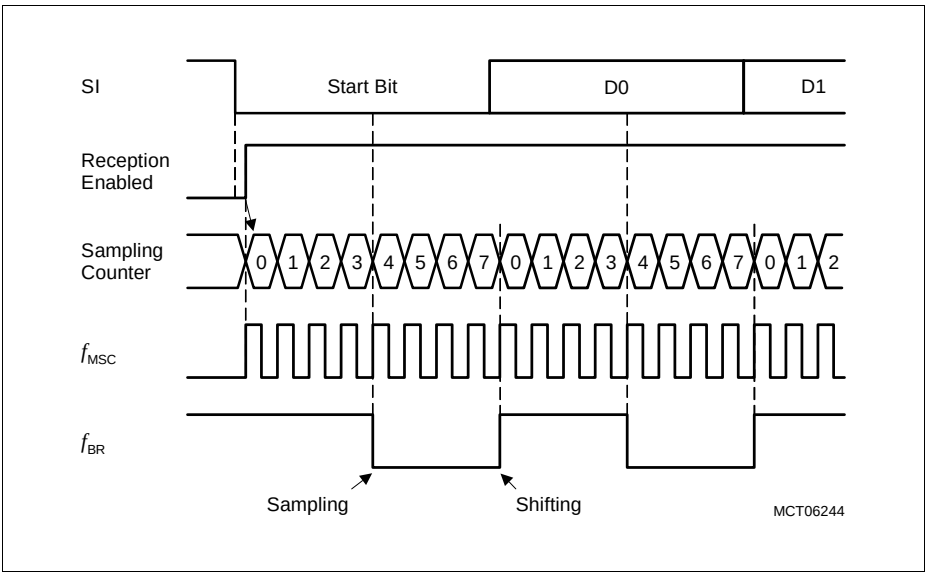


Figure 23-18 Upstream Channel Sampling with URR = 010_B

23.1.3.5 Spike Filter

The upstream channel input line SDI is sampled using a built-in spike filter with synchronization stage, both clocked with f_{MSC}. The spike filter is a chain of flip-flops with a majority decision logic (2 out of 3). A sampled value that is found at least twice in three samples is taken as data input value for SI.

23.1.4 I/O Control

The types of I/O control logic for the MSC module I/O lines are shown in **Figure 23-19**. The downstream channel generates five output signals that control eight MSC module outputs, split into four chip select outputs, two clock outputs, and two serial data outputs. The upstream channel has one input signal.

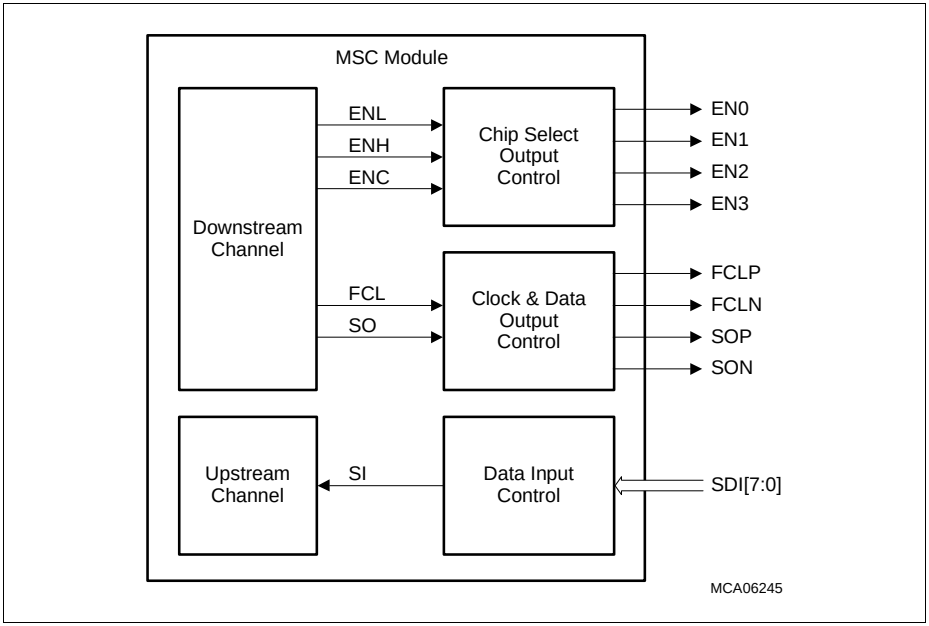


Figure 23-19 I/O Control

The MSC module I/O signals is controlled by bit fields that are located in the Output Control Register OCR.

23.1.4.1 Downstream Channel Output Control

As shown in **Figure 23-5** and **Figure 23-6**, the active phases during downstream channel operation are indicated by three enable signals:

- ENL indicates the SRL active phase of a data frame
- ENH indicates the SRH active phase of a data frame
- ENC indicates the active phase of a command frame

The chip select output control logic of the MSC uses a signal compressing scheme (similar to the interrupt request compressing scheme in **Figure 23-27**) that allows each of the three enable signals to be directed via a 2-bit selector to one of the four chip enable

outputs EN[3:0]. This also makes it possible to connect more than one internal enable signal (ENL, ENH, ENC) to one chip enable output ENx. Three bit fields in register OCR (CSL, CSH, and CSC) determine which chip enable output becomes active on a valid internal enable signal.

In the MSC, enable signals are high-level active signals. If required in a specific application, all chip enable outputs ENx can be assigned for low-level active polarity by setting bit OCR.CSLP.

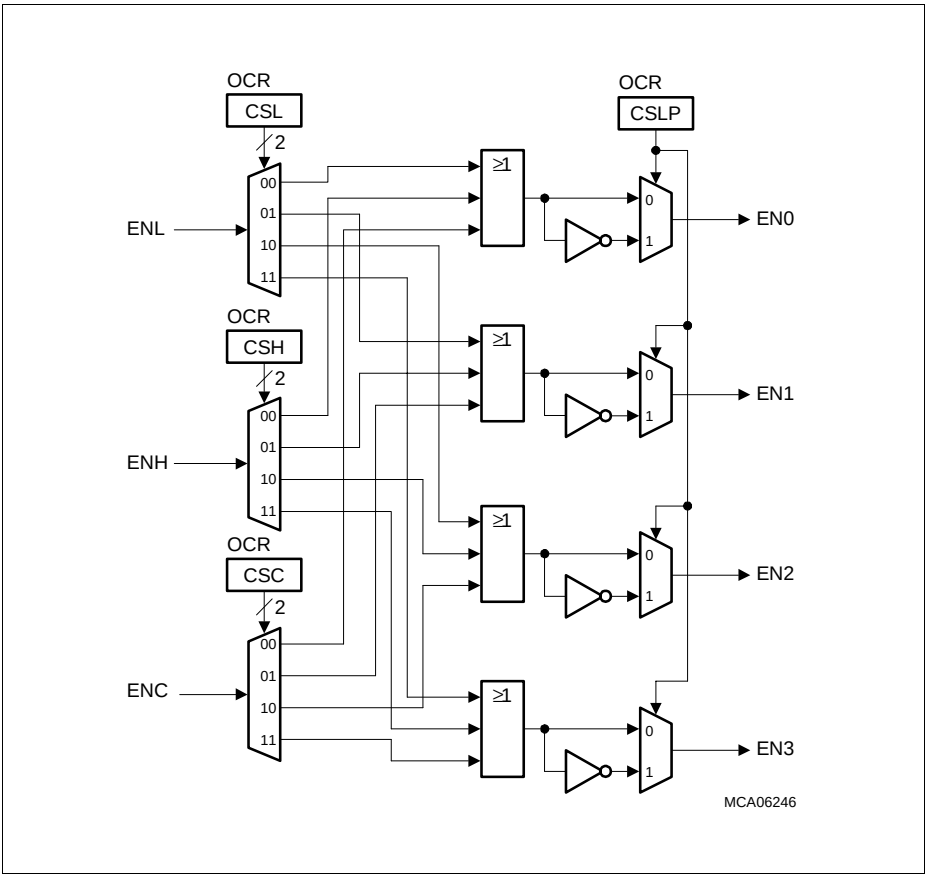


Figure 23-20 Downstream Channel: Chip Enable Output Control

At the MSC downstream channel, the internal serial clock output FCL and data output line SO are available outside the MSC module as two signal pairs with inverted signal polarity, FCLP/FCLN and SOP/SON. Both, clock and data outputs, are generated from the module internal signals FCL and SO according to **Figure 23-21**.

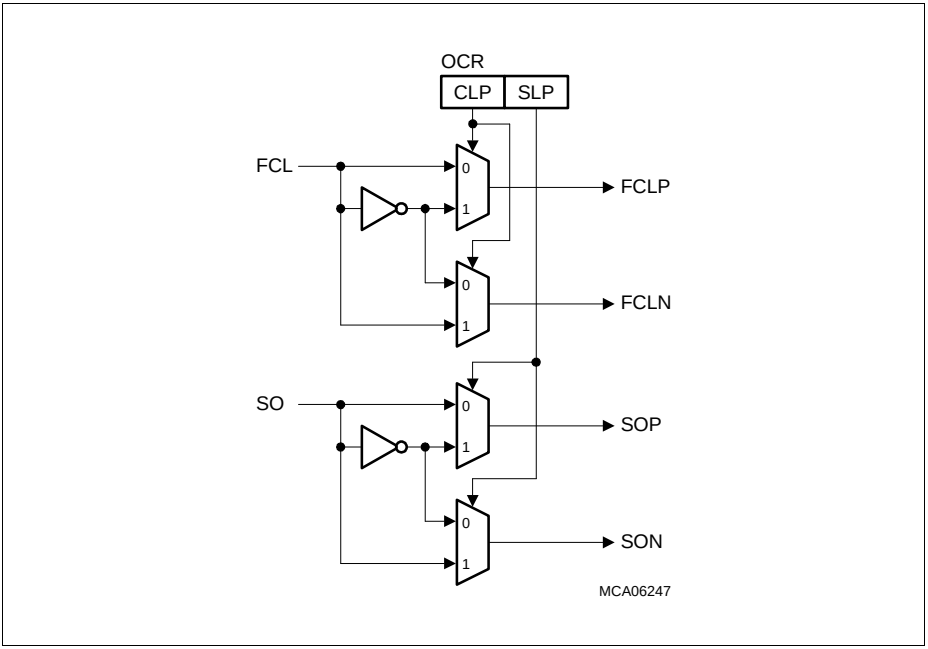


Figure 23-21 Downstream Channel: Clock and Data Output Control

With OCR.CLP = 0, FCLP has identical and FCLN has inverted polarity compared to FCL. Setting OCR.CLP, exchanges the signal polarities of FCLP and FCLN. An equivalent control capability is available for the SOP and SON data outputs (controlled by OCR.SLP).

One additional control capability not shown in **Figure 23-21** is available for the FCL signal. With OCR.CLKCTRL = 1, the FCL clock signal will always be generated, independently whether a downstream frame is currently transmitted or not. If OCR.CLKCTRL = 0, FCL becomes only active during the active phases of data or command frames (not during passive time frames).

23.1.4.2 Upstream Channel

As shown in **Figure 23-22**, the MSC upstream channel can be connected to up to eight SDI[7:0] serial inputs. Bit field OCR.SDISEL selects one out of these input lines (input signal SDI). If OCR.ILP = 0, SDI is directly connected to the serial receive buffer input SI. If OCR.ILP = 1, SDI is connected to input SI via an inverter.

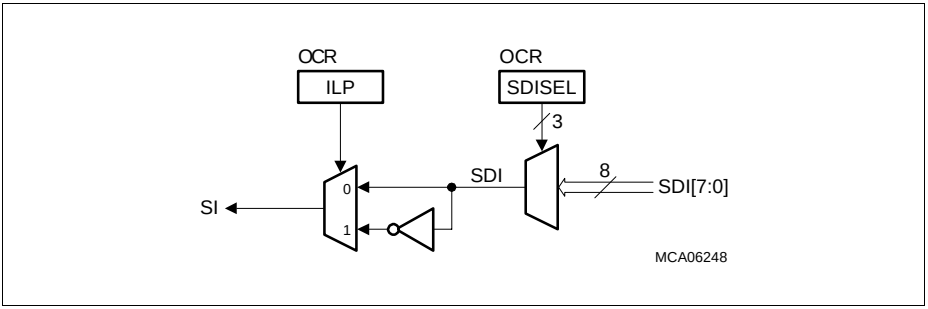


Figure 23-22 Upstream Channel Serial Data Input Control

23.1.5 MSC Interrupts

The MSC module has four interrupt sources and four service request outputs. A service request output is able to generate interrupts (controlled by a service request control register) or DMA requests. The service request output assignment, interrupt or DMA request, is specific for each microcontroller that is using the MSC. In this section, the term “interrupt request” has the meaning of “service request” that is able to handle interrupt or DMA requests.

Each interrupt source is provided with a status flag, enable bit(s) with software set/clear capability, and an interrupt node pointer. An interrupt event, internally generated as a request pulse, is always stored in an interrupt status flag that is located in the Interrupt Status Register ISR. All interrupt status flag can be set or cleared individually by software via the interrupt Set Clear Register ISC. Software-controlled interrupt generation can be initiated by setting the interrupt status flag of the corresponding interrupt. Each interrupt source can be enabled or disabled individually. When an interrupt event is enabled, a 2-bit interrupt node pointer determines which of the service request outputs will be activated.

Table 23-7 shows the four MSC interrupt sources.

Table 23-7 MSC Interrupts

Interrupt Type	Generated by
Data frame interrupt	Downstream Channel
Command frame interrupt	
Time frame finished interrupt	
Receive data interrupt	Upstream Channel

23.1.5.1 Data Frame Interrupt

A data frame interrupt can be generated when either the first or the last data bit of the downstream channel is shifted out and becomes available at the SO output line (see also **Figure 23-6**). Bit ICR.EDIEI selects which case is selected.

Note: If ICR.EDIE = 10_B, an interrupt at the first data bit is only generated if DSC.NDBL is not equal 00000_B. This means, at least one SRL bit must be shifted out for the first data bit shifted interrupt to become active.

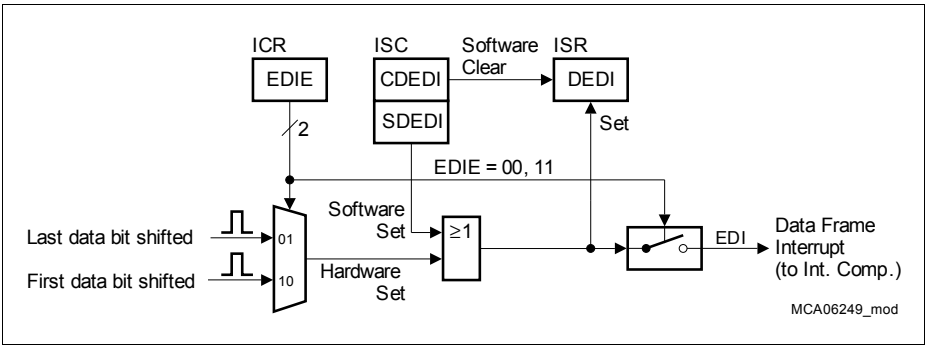


Figure 23-23 Data Frame Interrupt Control

23.1.5.2 Command Frame Interrupt

A command frame interrupt can be generated at the end of a downstream channel command frame (see also **Figure 23-5**).

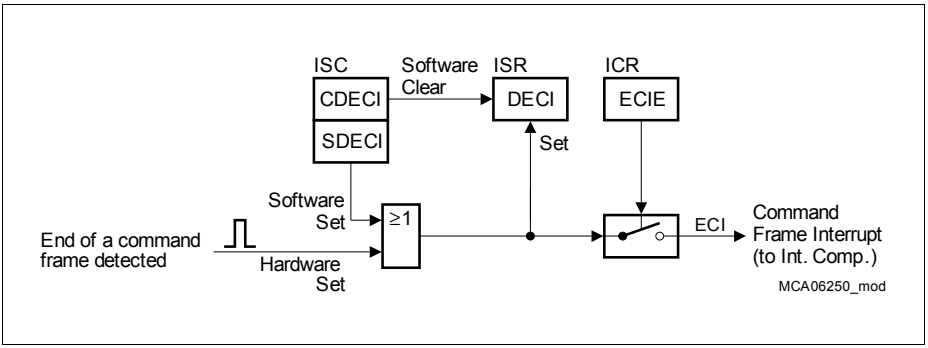


Figure 23-24 Command Frame Interrupt Control

23.1.5.3 Time Frame Finished Interrupt

A time frame finished interrupt can be generated at the end of a downstream channel passive time phase.

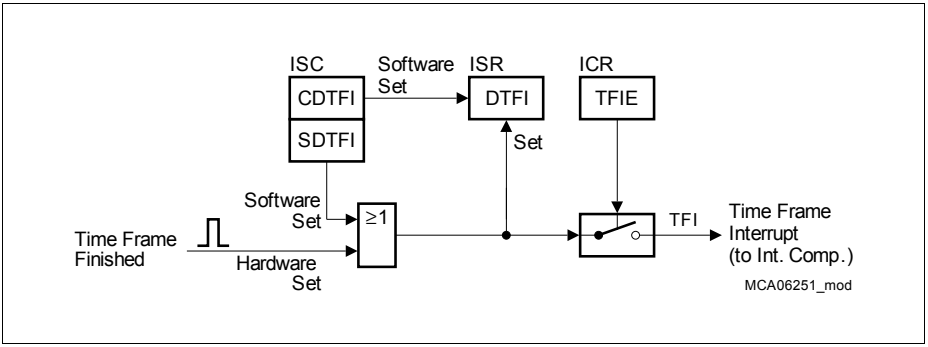


Figure 23-25 Time Frame Interrupt Control

23.1.5.4 Receive Data Interrupt

Whenever the upstream channel receives data in registers UDx (x = 0-3), the MSC is able to generate an interrupt. Three interrupt generation conditions can be selected for the receive data interrupt:

- Each update of UDx (x = 0-3) generates a receive data interrupt.
- Each update of UDx (x = 0-3) generates a receive data interrupt when the updated value is not equal 00_H.
- Only an update of register UD3 generates a receive data interrupt.

The selection of the interrupt generation condition is controlled by bit field ICR.RDIE. Setting ICR.RDIE = 0 disables the receive data interrupt in general. ISR.URDI is the interrupt status flag that can be set or clear when writing bits ISC.SURDI or ISC.CURDI with a 1.

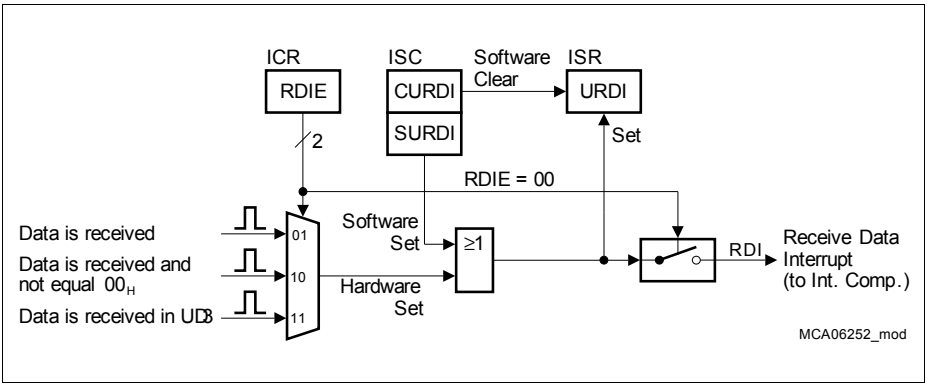


Figure 23-26 Receive Data Interrupt Control

23.1.5.5 Interrupt Request Compressor

The interrupt control logic of the MSC uses an interrupt compressing scheme that allows high flexibility in interrupt processing. Each of the four interrupt sources can be directed via a 2-bit interrupt node pointer to one of the four service request outputs SR[3:0]. This also makes it possible to connect more than one interrupt source to one interrupt output SRx.

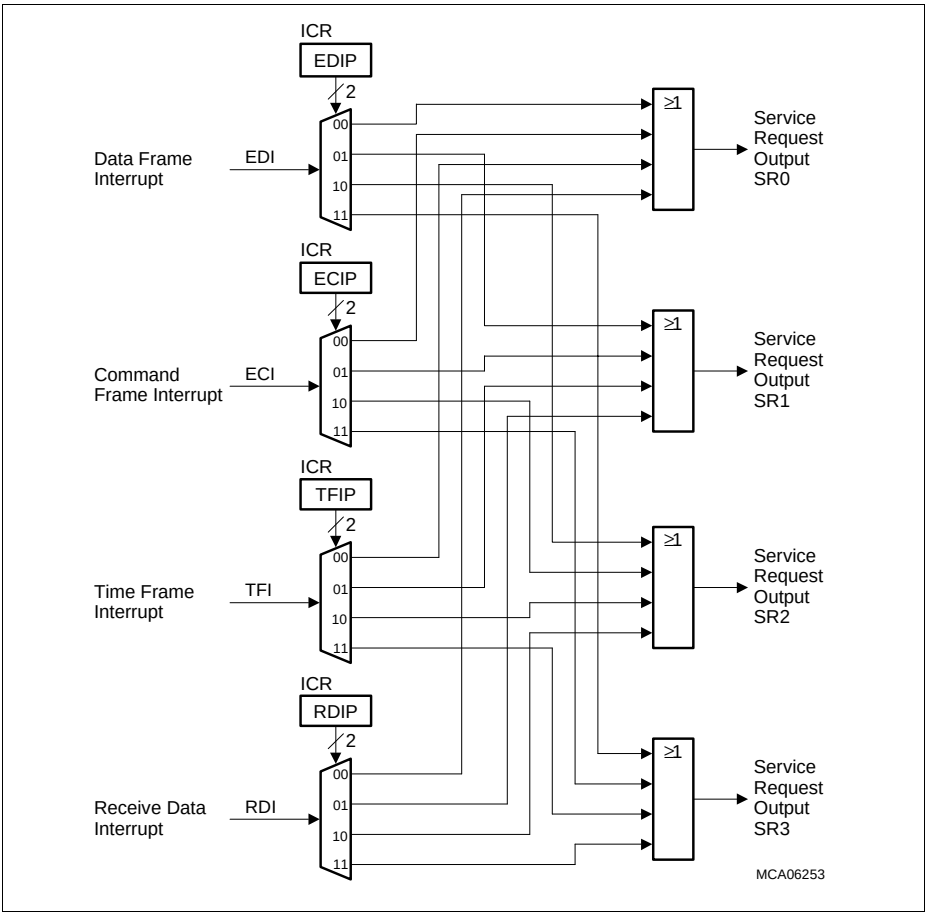


Figure 23-27 MSC Interrupt Request Compressor

*Note: The number of available MSC interrupt outputs depends on the implementation of the MSC module(s) in the specific product (see **Page 23-74** for TC1798 details).*

23.2 MSC Kernel Registers

This section describes the kernel registers of the MSC module. All MSC kernel register names described in this section will be referenced in other parts of the TC1798 User´s Manual by the module name prefix “MSC0_” for the MSC0 interface and “MSC1_” for the MSC1 interface.

All registers in the MSC address spaces are reset with the application reset (definition see SCU section “Reset Operation”).

MSC Kernel Register Overview

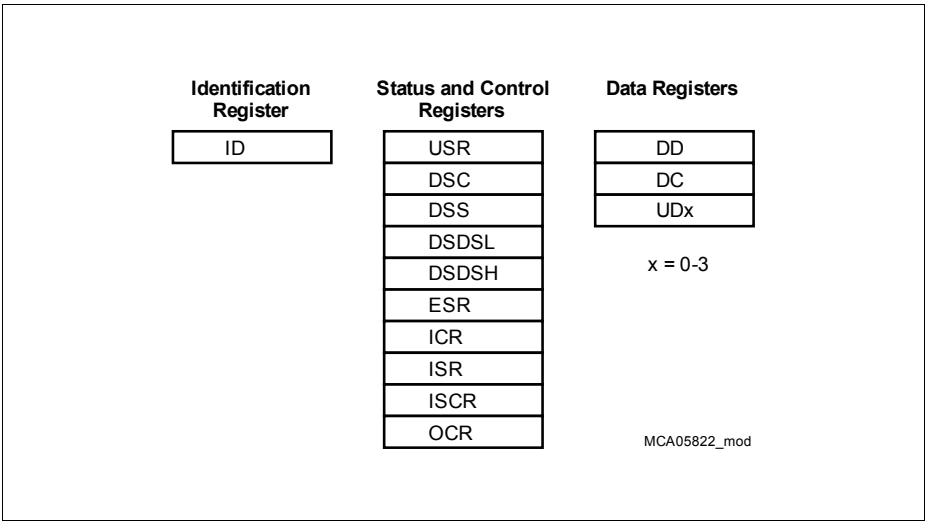


Figure 23-28 MSC Kernel Registers

The complete and detailed address map of the MSC0 module is described in Table 23-12 on Page 23-75.

Table 23-8 Registers Address Space - MSC0 Kernel Registers

Module	Base Address	End Address	Note
MSC0	$F000\ 0800_H$	$F000\ 08FF_H$	–
MSC1	$F000\ 0900_H$	$F000\ 09FF_H$	–

Table 23-9 Registers Overview - MSC Kernel Registers

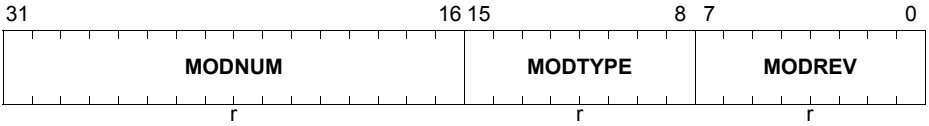
Register Short Name	Register Long Name	Offset Address[1)]	Description see
ID	Module Identification Register	08_H	Page 23-38
USR	Upstream Status Register	10_H	Page 23-39
DSC	Downstream Control Register	14_H	Page 23-41
DSS	Downstream Status Register	18_H	Page 23-44
DD	Downstream Data Register	$1C_H$	Page 23-59
DC	Downstream Command Register	20_H	Page 23-59
DSDSL	Downstream Select Data Source Low Register	24_H	Page 23-46
DSDSH	Downstream Select Data Source High Register	28_H	Page 23-47
ESR	Emergency Stop Register	$2C_H$	Page 23-48
UD0	Upstream Data Register 0	30_H	Page 23-60
UD1	Upstream Data Register 1	34_H	
UD2	Upstream Data Register 2	38_H	
UD3	Upstream Data Register 3	$3C_H$	
ICR	Interrupt Control Register	40_H	Page 23-49
ISR	Interrupt Status Register	44_H	Page 23-52
ISC	Interrupt Set Clear Register	48_H	Page 23-54
OCR	Output Control Register	$4C_H$	Page 23-56

1) The absolute register address is calculated as follows:
Module Base Address (Table 23-8) + Offset Address (shown in this column)

23.2.1 Module Identification Register

The MSC Module Identification Register ID contains read-only information about the module version.

ID
Module Identification Register **(08_H)** **Reset Value: $0028\ C0XX_H$**

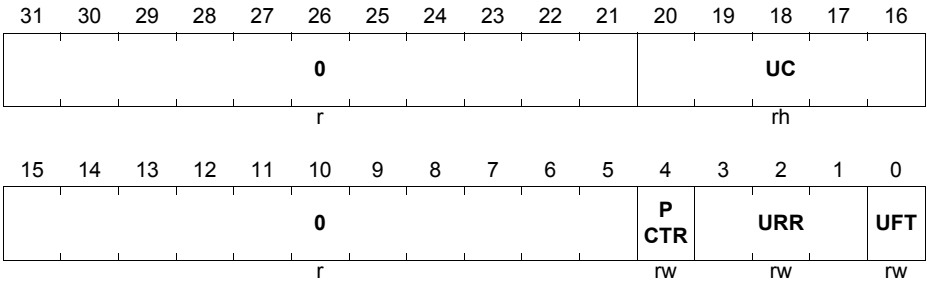


Field	Bits	Type	Description
MODREV	[7:0]	r	**Module Revision Number** This bit field defines the module revision number. The value of a module revision starts with 01_H (first revision).
MODTYPE	[15:8]	r	**Module Type** This bit field defines the module as a 32-bit module: $C0_H$
MODNUM	[31:16]	r	**Module Number Value** This bit field defines the module identification number for the MSC: 0028_H

23.2.2 Status and Control Registers

The Upstream Status Register is used to configure the upstream channel data format, baud rate, and parity type. It also provides the status information of the upstream counter (UC).

USR
Upstream Status Register **(10_H)** **Reset Value: $0000\ 0000_H$**



Field	Bits	Type	Description
UFT	0	rw	**Upstream Channel Frame Type** This bit determines the frame type used by the upstream channel for data reception. 0_B 12-bit upstream frame selected 1_B 16-bit upstream frame selected (with 4-bit address field)
URR	[3:1]	rw	**Upstream Channel Receiving Rate** This bit field determines the baud rate for the upstream channel. 000_B Upstream channel disabled; no reception is possible 001_B Baud rate = $f_{MSC}/4$ 010_B Baud rate = $f_{MSC}/8$ 011_B Baud rate = $f_{MSC}/16$ 100_B Baud rate = $f_{MSC}/32$ 101_B Baud rate = $f_{MSC}/64$ 110_B Baud rate = $f_{MSC}/128$ 111_B Baud rate = $f_{MSC}/256$

Field	Bits	Type	Description
PCTR	4	rw	**Parity Control** This bit determines the parity mode used by the upstream channel for data reception. 0_B Even parity mode is selected. A parity bit is set on an odd number of 1s in the serial address/data stream. 1_B Odd parity mode is selected. A parity bit is set on an even number of 1s in the serial address/data stream.
UC	[20:16]	rh	**Upstream Counter** This bit field indicates the content of the upstream counter that counts the bits during upstream channel reception.
0	[15:5], [31:21]	r	**Reserved** Read as 0; should be written with 0.

The Downstream Control Register is used to control the operation mode and frame layout of the downstream channel transmission. It also contains the two pending status bits.

DSC
Downstream Control Register (14_H) Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0			PPD					0		NBC					
r			rw					r		rw					

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DS DIS	EN SEL H	EN SEL L	NDBH					NDBL					DP	CP	TM
rh	rw	rw	rw					rw					rh	rh	rw

Field	Bits	Type	Description
TM	0	rw	**Transmission Mode** This bit selects the transmission mode of the downstream channel. 0_B Triggered Mode selected 1_B Data Repetition Mode selected
CP	1	rh	**Command Pending** This bit is set when the downstream command register DC is written. CP is cleared when the first bit of the related command frame is sent out.
DP	2	rh	**Data Pending** In Triggered Mode, this bit is set when the set data pending bit ISC.SDP is set by software. In Data Repetition Mode, this bit is set by hardware at the last passive time frame. At the start of the data frame, DP is cleared by hardware.

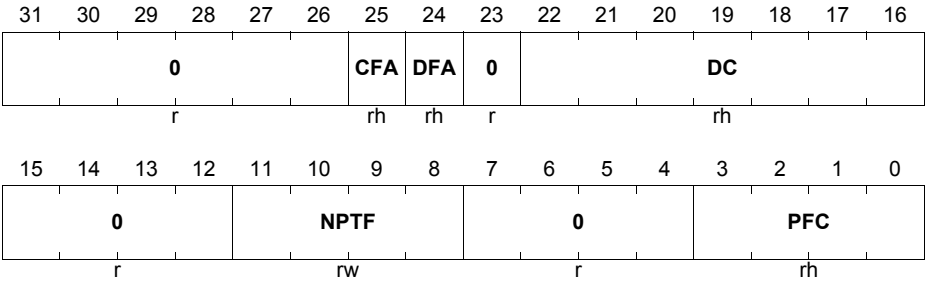
Field	Bits	Type	Description
NDBL	[7:3]	rw	**Number of SRL Bits Shifted at Data Frames** NDBL determines the number of shift register low part (SRL) bits that are shifted out on SO during a data frame. 00000_B No SRL bit shifted 00001_B SRL[0] shifted 00010_B SRL[1:0] shifted $...B$ ... 01111_B SRL[14:0] shifted 10000_B SRL[15:0] shifted Other bit combinations are reserved; do not use these bit combinations.
NDBH	[12:8]	rw	**Number of SRH Bits Shifted at Data Frames** NDBH determines the number of shift register high part (SRH) bits that are shifted out on SO during a data frame. 00000_B No SRH bit shifted; no selection bit is generated, the SRH active phase is completely skipped. 00001_B SRH[0] shifted 00010_B SRH[1:0] shifted $...B$ ... 01111_B SRH[14:0] shifted 10000_B SRH[15:0] shifted Other bit combinations are reserved; do not use these bit combinations.
ENSELL	13	rw	**Enable SRL Active Phase Selection Bit** This bit determines whether a low level selection bit is inserted at the beginning of a data frame's SRL active phase. 0_B No selection bit inserted. 1_B Low level selection bit inserted.
ENSELH	14	rw	**Enable SRH Active Phase Selection Bit** This bit determines whether a low level selection bit is inserted at the beginning of a data frame's SRH active phase. 0_B No selection bit inserted. 1_B Low level selection bit inserted.

Field	Bits	Type	Description
DSDIS	15	rh	**Downstream Disable** This bit indicates the state of the downstream channel operation. 0_B The downstream channel is enabled. A frame transmission can take place (Triggered Mode) or takes place (Data Repetition Mode). 1_B Downstream Counter becomes disabled. No new frame transmission is started. A running frame transmission is always completed.
NBC	[21:16]	rw	**Number of Bits Shifted at Command Frames** This bit field determines how many bits of the SRL/SRH shift registers are shifted out during transmission of a command frame. 000000_B No bit shifted 000001_B SRL[0] shifted 000010_B SRL[1:0] shifted 000011_B SRL[2:0] shifted $\cdots_B$ ... 010000_B SRL[15:0] shifted 010001_B SRL[15:0] and SRH[0] shifted 010010_B SRL[15:0] and SRH[1:0] shifted $\cdots_B$ ... 011111_B SRL[15:0] and SRH[14:0] shifted 100000_B SRL[15:0] and SRH[15:0] shifted Other bit combinations are reserved; do not use these bit combinations
PPD	[28:24]	rw	**Passive Phase Length at Data Frames** This bit field determines the length of the passive phase of a data frame. 00000_B Passive phase length is $2 \times t_{FCL}$ 00001_B Passive phase length is $2 \times t_{FCL}$ 00010_B Passive phase length is $2 \times t_{FCL}$ 00011_B Passive phase length is $3 \times t_{FCL}$ $\cdots_B$ ... 11111_B Passive phase length is $31 \times t_{FCL}$
0	[23:22], [31:29]	r	**Reserved** Read as 0; should be written with 0.

Note: The "rw" bits in the DSC register are buffered in a shadow buffer at the start of a corresponding frame transmission.

The Downstream Status Register DSS contains counter bit fields, status bits, and indicates the number of passive time frames.

DSS
Downstream Status Register (18_H) Reset Value: $0000\ 0000_H$

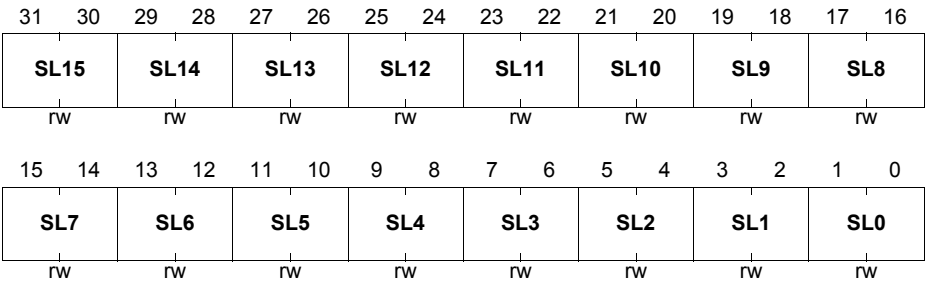


Field	Bits	Type	Description
PFC	[3:0]	rh	**Passive Time Frame Counter** In Data Repetition Mode, this bit field indicates the count of passive time frames that are currently transmitted. In Triggered Mode PFC remains at 0000_B. 0000_B Data frame is transmitted. 0001_B First passive time frame is transmitted. 0010_B Second passive time frame is transmitted. $\ldots_B$ ... 1111_B Fifteenth passive time frame is transmitted.
NPTF	[11:8]	rw	**Number Of Passive Time Frames** This bit field indicates the number of passive time frames that are inserted in Data Repetition Mode between two data frames. 0000_B No passive time frame inserted. 0001_B One passive time frame inserted. 0010_B Two passive time frames inserted. $\ldots_B$ ... 1111_B Fifteen passive time frames inserted. *Note: NPTF is buffered in a shadow buffer at the start of each data frame.*

Field	Bits	Type	Description
DC	[22:16]	rh	**Downstream Counter** This bit field indicates the number of downstream shift clock periods that have been elapsed since the start of the current frame. 00_H No shift clock elapsed (after counter reset). 01_H 1 shift clock elapsed. …$_H$ … $7F_H$ 127 shift clocks elapsed. DC is reset at the end of a downstream frame.
DFA	24	rh	**Data Frame Active** This bit indicates if a data frame is currently sent out. 0_B No data frame is currently sent out. 1_B A data frame is currently sent out.
CFA	25	rh	**Command Frame Active** This bit indicates if a command frame is currently sent out. 0_B No command frame is currently sent out. 1_B A command frame is currently sent out.
0	[7:4], [15:12], 23, [31:26]	r	**Reserved** Read as 0; should be written with 0.

The bit fields of the Downstream Select Data Low Register DSDSL determine the data source for each bit in shift register SRL.

DSDSL
Downstream Select Data Source Low Register
(24_H) **Reset Value: $0000\ 0000_H$**



Field	Bits	Type	Description
SLx **(x = 0-15)**	[2*x+1: 2*x]	rw	**Select Source for SRL** SLx determines which data source is used for the shift register bit SRL[x] during data frame transmission. 00_B SRL[x] is taken from data register DD.DDL[x]. 01_B Reserved. 10_B SRL[x] is taken from the ALTINL input line x. 11_B SRL[x] is taken from the ALTINL input line x in inverted state.

The bit fields of the Downstream Select Data Source High Register DSDSH determine the data source for each bit in shift register SRH.

DSDSH
Downstream Select Data Source High Register
(28_H) **Reset Value: $0000\ 0000_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SH15		SH14		SH13		SH12		SH11		SH10		SH9		SH8	
rw		rw		rw		rw		rw		rw		rw		rw	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SH7		SH6		SH5		SH4		SH3		SH2		SH1		SH0	
rw		rw		rw		rw		rw		rw		rw		rw	

Field	Bits	Type	Description
SHx (x = 0-15)	[2*x+1: 2*x]	rw	**Select Source for SRH** SHx determines which data source is used for the shift register bit SRH[x] during data frame transmission. 00_B SRH[x] is taken from data register DD.DDH[x]. 01_B Reserved. 10_B SRH[x] is taken from the ALTINH input line x. 11_B SRH[x] is taken from the ALTINH input line x in inverted state.

The Emergency Stop Register ESR determines which bits of SRL and SRH are enabled for emergency operation.

ESR
Emergency Stop Register **($2C_H$)** **Reset Value: $0000\ 0000_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ENH 15	**ENH 14**	**ENH 13**	**ENH 12**	**ENH 11**	**ENH 10**	**ENH 9**	**ENH 8**	**ENH 7**	**ENH 6**	**ENH 5**	**ENH 4**	**ENH 3**	**ENH 2**	**ENH 1**	**ENH 0**
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ENL 15	**ENL 14**	**ENL 13**	**ENL 12**	**ENL 11**	**ENL 10**	**ENL 9**	**ENL 8**	**ENL 7**	**ENL 6**	**ENL 5**	**ENL 4**	**ENL 3**	**ENL 2**	**ENL 1**	**ENL 0**
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
ENLx (x = 0-15)	x	rw	**Emergency Stop Enable for Bit x in SRL** This bit enables the emergency stop feature selectively for each SRL bit. If the emergency stop condition is met and enabled (ENLx = 1), the SRL[x] bit is of the data register DD.DDL[x] is used for the shift register load operation. 0_B Emergency stop feature for bit SRL[x] is disabled. 1_B The emergency stop feature for bit SRL[x] is enabled.
ENHx (x = 0-15)	x+16	rw	**Emergency Stop Enable for Bit x in SRH** This bit enables the emergency stop feature selectively for each SRH bit. If the emergency stop condition is met and enabled (ENHx = 1), the SRH[x] bit of the data register DD.DDH[x] is used for the shift register load operation. 0_B Emergency stop feature for bit SRH[x] is disabled. 1_B The emergency stop feature for bit SRH[x] is enabled.

The Interrupt Control Register ICR holds the interrupt enable bits and interrupt pointers of all four MSC interrupts.

ICR
Interrupt Control Register **(40_H)** **Reset Value: $0000\ 0000_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RDIE		RDIP		TFIE	0	TFIP		ECIE	0	ECIP		EDIE		EDIP	
rw		rw		rw	r	rw		rw	r	rw		rw		rw	

Field	Bits	Type	Description
EDIP	[1:0]	rw	**Data Frame Interrupt Node Pointer** EDIP selects the service request output line SRn (n = 0-3) for the data frame interrupt. 00_B Service request output SR0 selected 01_B Service request output SR1 selected 10_B Service request output SR2 selected 11_B Service request output SR3 selected
EDIE	[3:2]	rw	**Data Frame Interrupt Enable** This bit field determines the enable conditions for the data frame interrupt. 00_B Interrupt generation disabled 01_B An interrupt is generated when the last data bit has been shifted out. 10_B An interrupt is generated when the first data bit has been shifted out, but only if DSC.NDBL is not equal 00000_B. This means, at least one SRL bit must be shifted out for the first data bit shifted interrupt to become active. 11_B Interrupt generation disabled

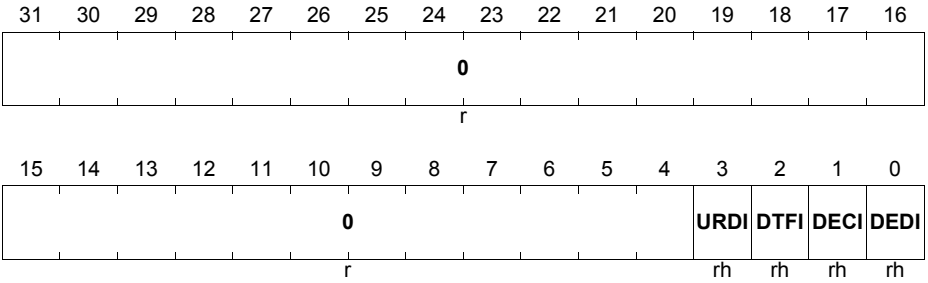
Field	Bits	Type	Description
ECIP	[5:4]	rw	**Command Frame Interrupt Node Pointer** ECIP selects the service request output line SRn (n = 0-3) for the command frame interrupt. 00_B Service request output SR0 selected 01_B Service request output SR1 selected 10_B Service request output SR2 selected 11_B Service request output SR3 selected
ECIE	7	rw	**Command Frame Interrupt Enable** This bit enables the command frame interrupt. 0_B Interrupt generation disabled. 1_B Interrupt generation enabled.
TFIP	[9:8]	rw	**Time Frame Interrupt Pointer** TFIP selects the service request output line SRn (n = 3-0) for the time frame interrupt. 00_B Service request output SR0 selected 01_B Service request output SR1 selected 10_B Service request output SR2 selected 11_B Service request output SR3 selected
TFIE	11	rw	**Time Frame Interrupt Enable** This bit enables the time frame interrupt. 0_B Interrupt generation disabled. 1_B Interrupt generation enabled.
RDIP	[13:12]	rw	**Receive Data Interrupt Pointer** RDIP selects the service request output line SRn (n = 3-0) for the receive data interrupt. 00_B Service request output SR0 selected 01_B Service request output SR1 selected 10_B Service request output SR2 selected 11_B Service request output SR3 selected

Field	Bits	Type	Description
RDIE	[15:14]	rw	**Receive Data Interrupt Enable** This bit field determines the enable conditions for the receive data interrupt. 00_B Interrupt generation disabled. 01_B An interrupt is generated when data is received and written into the upstream data registers UDx (x = 0-3). 10_B An interrupt is generated as with RDIE = 01_B but only if the received data is not equal to 00_H. 11_B An interrupt is generated when data is received and written into register UD3.
0	6, 10, [31:16]	r	**Reserved** Read as 0; should be written with 0.

The Interrupt Status Register ISR holds the interrupt status flags that indicate an interrupt occurrence in downstream and upstream channels.

ISR

Interrupt Status Register **(44_H)** **Reset Value: 0000 0000_H**



Field	Bits	Type	Description
DEDI	0	rh	**Data Frame Interrupt Flag** This flag is always set by hardware when a downstream channel data frame interrupt is generated. DEDI can be set or cleared by software when writing to register ISC with the appropriate bits ISC.SDEDI or ISC.CDEDI set.
DECI	1	rh	**Command Frame Interrupt Flag** This flag is always set by hardware when a downstream channel command frame interrupt is generated, whether or not it is enabled. DECI can be set or cleared by software when writing to register ISC with the appropriate bits SDECI or CDECI set.
DTFI	2	rh	**Time Frame Interrupt Flag** This flag is always set by hardware when a downstream channel time frame interrupt is generated, whether or not it is enabled. DTFI can be set or cleared by software when writing to register ISC with the appropriate bits SDTFI or CDTFI set.

Field	Bits	Type	Description
URDI	3	rh	**Receive Data Interrupt Flag** This flag is always set by hardware when an upstream channel receive data interrupt is generated, whether or not it is enabled. URDI can be set or cleared by software when writing to register ISC with the appropriate bits SURDI or CURDI set.
0	[31:4]	r	**Reserved** Read as 0; should be written with 0.

The Interrupt Set Clear Register ISC is used to set or clear the MSC interrupt flags located in the Interrupt Status Register ISR. Reading ISC always returns 0000 0000$_H$.

ISC
Interrupt Set Clear Register **(48$_H$)** **Reset Value: 0000 0000$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0									SDDIS	SCP	SDP	SURDI	SDTFI	SDECI	SDEDI
r									w	w	w	w	w	w	w

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0									CDDIS	CCP	CDP	CURDI	CDTFI	CDECI	CDEDI
r									w	w	w	w	w	w	w

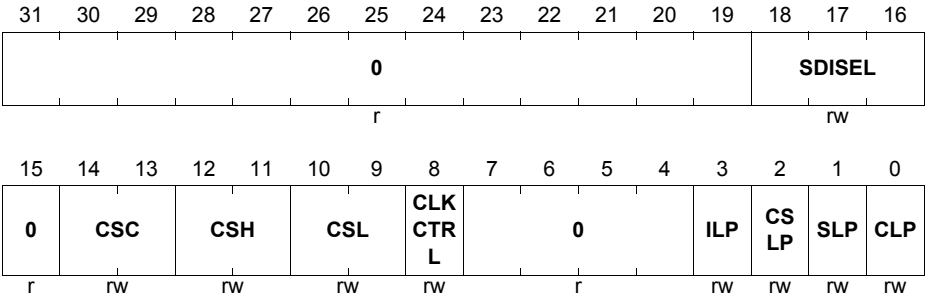
Field	Bits	Type	Description
CDEDI	0	w	**Clear DEDI Flag** 0_B No operation 1_B Bit ISR.DEDI is cleared.
CDECI	1	w	**Clear DECI Flag** 0_B No operation 1_B Bit ISR.DECI is cleared.
CDTFI	2	w	**Clear DTFI Flag** 0_B No operation 1_B Bit ISR.DTFI is cleared.
CURDI	3	w	**Clear URDI Flag** 0_B No operation 1_B Bit ISR.URDI is cleared.
CDP	4	w	**Clear DP Flag** 0_B No operation 1_B Bit DSC.DP is cleared.
CCP	5	w	**Clear CP Flag** 0_B No operation 1_B Bit DSC.CP is cleared.
CDDIS	6	w	**Clear DSDIS Flag** 0_B No operation 1_B Bit DSC.DSDIS is cleared.

Field	Bits	Type	Description
SDEDI	16	w	**Set DEDI Flag** 0_B No operation 1_B Bit ISR.DEDI is set.
SDECI	17	w	**Set DECI Flag** 0_B No operation 1_B Bit ISR.DECI is set.
SDTFI	18	w	**Set DTFI Flag** 0_B No operation 1_B Bit ISR.DTFI is set.
SURDI	19	w	**Set URDI Flag** 0_B No operation 1_B Bit ISR.URDI is set.
SDP	20	w	**Set DP Bit** 0_B No effect 1_B Bit DSC.DP is set.
SCP	21	w	**Set CP Flag** 0_B No operation 1_B Bit DSC.CP is set.
SDDIS	22	w	**Set DSDIS Flag** 0_B No operation 1_B Bit DSC.DSDIS is set.
0	[15:7], [31:23]	r	**Reserved** Read as 0; should be written with 0.

Note: When the ISC register is written with both bits (set and reset bit) for a specific interrupt flag, the clear operation takes place and the set operation is ignored.

The Output Control Register OCR determines the MSC input/output signal polarities, the chip select output signal assignment, and the serial output clock generation.

OCR
Output Control Register **($4C_H$)** **Reset Value: $0000\ 0000_H$**



Field	Bits	Type	Description
CLP	0	rw	**FCLP Line Polarity** 0_B FCLP and FCL signal polarity is identical. FCLN signal has inverted FCL signal polarity. 1_B FCLP signal has inverted FCL signal polarity. FCLN and FCL signal polarities are identical.
SLP	1	rw	**SOP Line Polarity** 0_B SOP and SO signal polarity is identical. SON signal has inverted SO signal polarity. 1_B SOP signal has inverted SO signal polarity. SON and SO signal polarities are identical.
CSLP	2	rw	**Chip Selection Lines Polarity** 0_B EN[3:0] and ENL, ENH, ENC signal polarities are identical (high active). 1_B EN[3:0] signal polarities are inverted (low active) to the ENL, ENH, ENC signal polarities. Bit CSLP is buffered during a frame transmission. This means that any change of CSLP becomes valid first with the start of the next frame transmission.
ILP	3	rw	**SDI Line Polarity** 0_B SDI and SI signal polarities are identical. 1_B SDI and SI signal polarities are inverted.

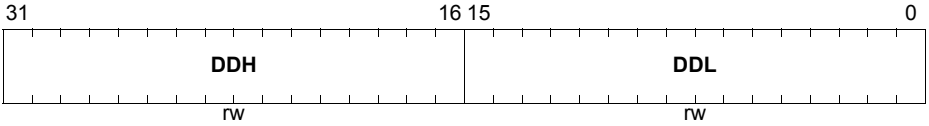
Field	Bits	Type	Description
CLKCTRL	8	rw	**Clock Control** This bit determines the activation of clock output FCL. 0_B FCL is activated only during the active phases of data or command frames (not during passive time frames). 1_B FCL is always active whether or not a downstream frame is currently transmitted.
CSL	[10:9]	rw	**Chip Enable Selection for ENL** This bit field selects the chip enable output ENx that becomes active during the SRL active phase (ENL = 1) of a data frame. The active level of ENx is defined by bit CSLP. 00_B EN0 line is selected for ENL. 01_B EN1 line is selected for ENL. 10_B EN2 line is selected for ENL. 11_B EN3 line is selected for ENL.
CSH	[12:11]	rw	**Chip Enable Selection for ENH** This bit field selects the chip enable output ENx that becomes active during the SRH active phase (ENH = 1) of a data frame. The active level of ENx is defined by bit CSLP. 00_B EN0 line is selected for ENH. 01_B EN1 line is selected for ENH. 10_B EN2 line is selected for ENH. 11_B EN3 line is selected for ENH.
CSC	[14:13]	rw	**Chip Enable Selection for ENC** This bit field selects the chip enable output ENx that becomes active during the active phase (ENC = 1) of a command frame. The active level of ENx is defined by bit CSLP. 00_B EN0 line is selected for ENC. 01_B EN1 line is selected for ENC. 10_B EN2 line is selected for ENC. 11_B EN3 line is selected for ENC.

Field	Bits	Type	Description
SDISEL	[18:16]	rw	**Serial Data Input Selection** This bit field selects the source for the serial data input SDI of the upstream channel. 000_B SDI0 input is selected for SDI. 001_B SDI1 input is selected for SDI. 010_B SDI2 input is selected for SDI. 011_B SDI3 input is selected for SDI. 100_B SDI4 input is selected for SDI. 101_B SDI5 input is selected for SDI. 110_B SDI6 input is selected for SDI. 111_B SDI7 input is selected for SDI.
0	[7:4], 15, [31:19]	r	**Reserved** Read as 0; should be written with 0.

23.2.3 Data Registers

The Downstream Data Register DD contains data to be transmitted during data frames.

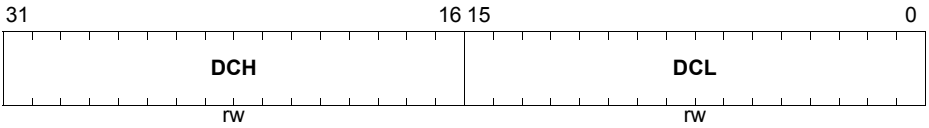
DD
Downstream Data Register **($1C_H$)** **Reset Value: 0000 0000$_H$**



Field	Bits	Type	Description
DDL	[15:0]	rw	**Downstream Data for SRL Shift Register** Contains the data bits to be transmitted during the SRL active phase of a data frame.
DDH	[31:16]	rw	**Downstream Data for SRH Shift Register** Contains the data bits to be transmitted during the SRH active phase of a data frame.

The Downstream Command Register DC contains command information to be transmitted during command frames.

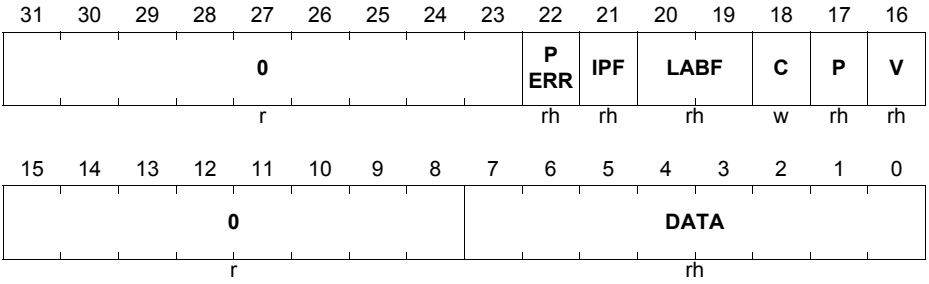
DC
Downstream Command Register **(20_H)** **Reset Value: 0000 0000$_H$**



Field	Bits	Type	Description
DCL	[15:0]	rw	**Downstream Command for SRL Shift Register** Contains the data bits to be transmitted during the SRL active phase of a command frame.
DCH	[31:16]	rw	**Downstream Command for SRH Shift Register** Contains the data bits to be transmitted during the SRH active phase of a command frame.

The four Upstream Data Registers UDx store the content (data, addresses, received and calculated parity bit, parity error bit) of a received upstream channel data frame.

UDx (x = 0-3)
Upstream Data Register x **(30_H+x*4_H)** **Reset Value: 0000 0000_H**



Field	Bits	Type	Description
DATA	[7:0]	rh	**Received Data** This bit field contains the 8-bit receive data.
V	16	rh	**Valid Bit** This bit is set by hardware when the received data is written to UDx. Writing bit C = 1 clears V. If hardware setting and software clearing of the valid bit occur simultaneously, bit V will be cleared.
P	17	rh	**Parity Bit** This flag contains the parity bit that has been received with the data frame.
C	18	w	**Clear Bit** 0_B No operation. 1_B Bit V is cleared. C is always read as 0.
LABF	[20:19]	rh	**Lower Address Bit Field** This bit field contains the two address bits A[1:0] of the 4-bit address field (16-bit data frame). If 12-bit data frame is selected, LABF is always set to 00_B.
IPF	21	rh	**Internal Parity Flag** This bit contains the parity bit that has been calculated in the MSC during data frame reception.

Field	Bits	Type	Description
PERR	22	rh	**Parity Error** This bit indicates if a start bit error, parity error, or stop bit error occurred during frame reception. 0_B No error detected. 1_B Error detected.
0	[15:8], [31:23]	r	**Reserved** Read as 0; should be written with 0.

23.3 MSC Module Implementation

This section describes the MSC module interface as implemented in the TC1798. It especially covers clock control, port and on-chip connections, interrupt control, and address decoding.

23.3.1 Interface Connections of the MSC Modules

Figure 23-29 shows the TC798-specific implementation details and interconnections of the MSC0 and MSC1 modules.

Each MSC module is supplied with a separate clock control, address decoding, and interrupt control logic. Two of the four modules' service request outputs are connected with interrupt nodes, and two with the DMA controller. Outputs of the GPTA module are connected to the alternate input buses ALTINL/ALTINH. The emergency stop output from the SCU controls the corresponding inputs of both MSC modules.

The serial data and clock outputs of the downstream channels of each MSC module are connected to combined GPIO/LVDS differential output drivers. Details about these eight Port 5 pins are defined in the ports chapter (see also **Table 23-10**).

Additionally, the positive serial clock (FCLP) and positive data output (SOP) are available at GPIO lines of Port 9. The device select outputs (ENxy) are wired to GPIO lines of Port 5 and Port 9. One Port 5 input line is connected to the upstream channel serial data input.

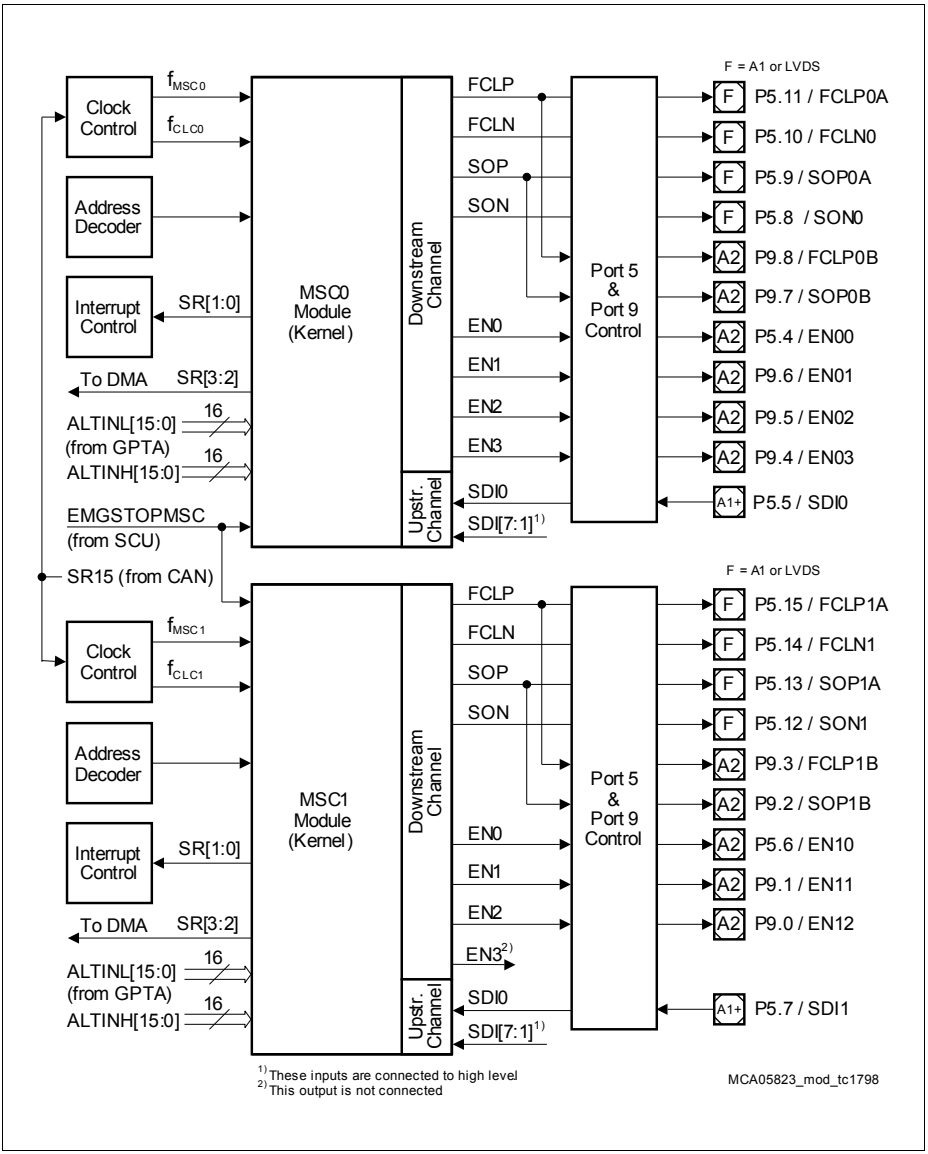


Figure 23-29 MSC0 and MSC1 Module Implementations and Interconnections

23.3.2 MSC0/MSC1 Module-Related External Registers

Figure 23-30 summarizes the module-related external registers which are required for MSC programming (see also **Figure 23-28** for the module kernel specific registers). These registers are described in the following sections.

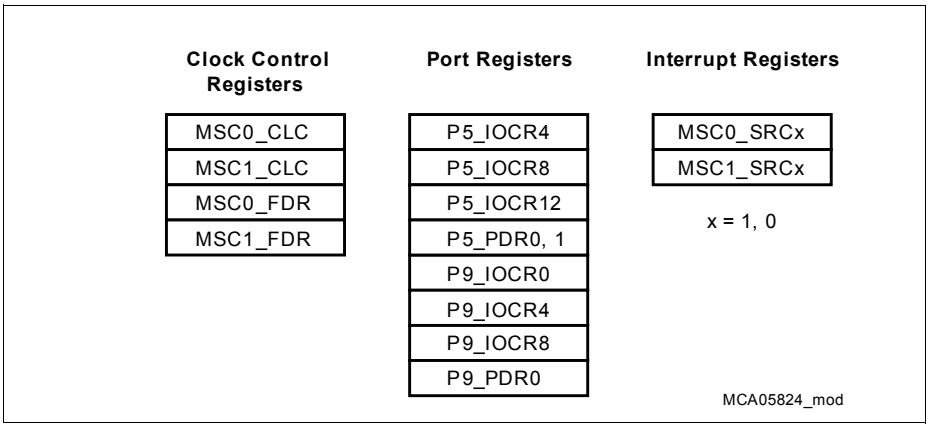


Figure 23-30 MSC Implementation-specific Special Function Registers

23.3.3 Clock Control

The MSC modules are provided with two independent clock signals (**Figure 23-31**):

- f_{CLC0} and f_{CLC1}
  These are the module clocks that are used inside the MSC kernel for control purposes such as clocking of control logic and register operations. The frequency of f_{CLC0} and f_{CLC1} is always identical to the system clock frequency f_{FPI}. The clock control registers MSC0_CLC and MSC1_CLC make it possible to enable/disable f_{CLC0} and f_{CLC1} under certain conditions.
- f_{MSC0} and f_{MSC1}
  These clocks are the module clocks that are used inside the MSC for baud rate generation of the serial upstream and downstream channel. The fractional divider registers MSC0_FDR and MSC1_FDR control the frequency of f_{MSC0} and f_{MSC1} and make it possible to enable/disable it independently of f_{CLC0} and f_{CLC1}.

For module test purposes only, the service request output SR15 of the MultiCAN controller makes it possible to synchronize the fractional divider clock generation of both MSC modules to external events. This feature should not be used for normal MSC operation.

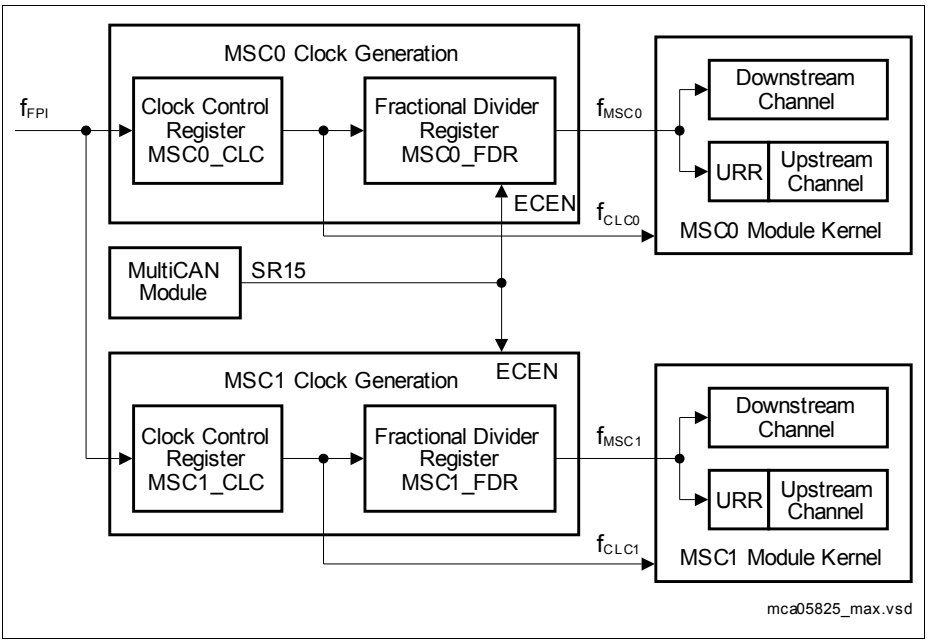


Figure 23-31 MSC Module Clock Generation

The following two formulas define the frequency of f_{MSC0}:

$$f_{MSC0} = f_{FPI} \times \frac{1}{n} \text{ with n = 1024 - MSC0.FDR.STEP} \quad (23.3)$$

$$f_{MSC0} = f_{FPI} \times \frac{n}{1024} \text{ with n = 0-1023} \quad (23.4)$$

Downstream Channel Baud Rate

As the clock signal FCL of the synchronous downstream channel is always half the frequency of f_{MSC0}, the resulting downstream channel baud rate is defined by:

$$\text{Baud rate}_{MSC0} = f_{FPI} \times \frac{1}{2 \times (1024 - \text{MSC0.FDR.STEP})} \quad (23.5)$$

$$\text{Baud rate}_{MSC0} = f_{FPI} \times \frac{\text{MSC0.FDR.STEP}}{2 \times 1024} \quad (23.6)$$

Upstream Channel Baud Rate

The baud rate of the asynchronous upstream channel is derived from the module clock f_{MSC0} by a programmable clock divider selected by bit field MSC0_USR.URR (see also **Equation (23.2)** on **Page 23-25**). The divide factor DF can be at minimum 4 and at maximum 256.

$$\text{Baud rate}_{MSC0} = f_{FPI} \times \frac{1}{DF \times (1024 - \text{MSC0.FDR.STEP})} \quad (23.7)$$

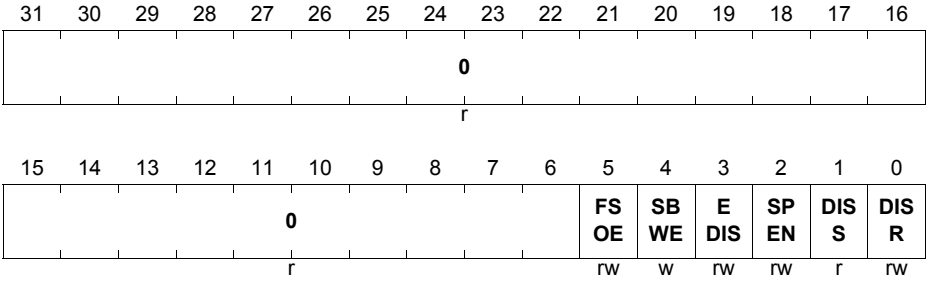
$$\text{Baud rate}_{MSC0} = f_{FPI} \times \frac{\text{MSC0.FDR.STEP}}{DF \times 1024} \quad (23.8)$$

Equation (23.3), **Equation (23.5)**, and **Equation (23.7)** are valid for normal divider mode (MSC0.FDR.DM = 01_B). **Equation (23.4)**, **Equation (23.6)**, and **Equation (23.8)** are valid for fractional divider mode (MSC0.FDR.DM = 10_B).

23.3.3.1 Clock Control Register

The Clock Control Register allows the programmer to control (enable/disable) the clock signals to the MSC0 module under certain conditions. The diagram below shows the clock control register functionality as is implemented for the MSC0 and MSC1 modules.

MSC0_CLC
MSC0 Clock Control Register **(00_H)** **Reset Value: $0000\ 0003_H$**
MSC1_CLC
MSC1 Clock Control Register **(00_H)** **Reset Value: $0000\ 0003_H$**



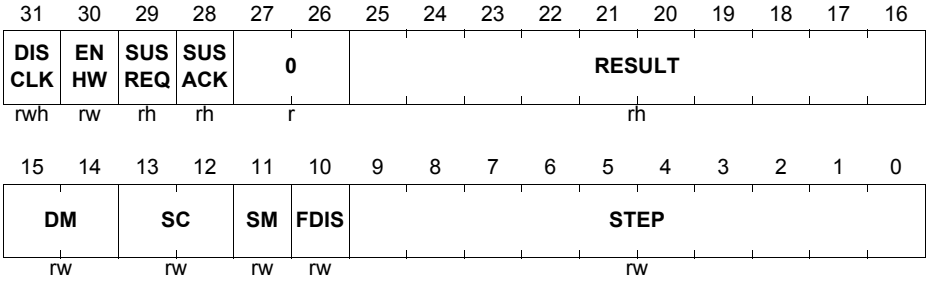
Field	Bits	Type	Description
DISR	0	rw	**Module Disable Request Bit** Used for enable/disable control of the module.
DISS	1	r	**Module Disable Status Bit** Bit indicates the current status of the module.
SPEN	2	rw	**Module Suspend Enable for OCDS** Used to enable the suspend mode
EDIS	3	rw	**Sleep Mode Enable Control** Used to control module's sleep mode.
SBWE	4	w	**Module Suspend Bit Write Enable for OCDS** Determines whether SPEN and FSOE are write-protected.
FSOE	5	rw	**Fast Switch Off Enable** Used to switch off fast clock in Suspend Mode.
0	[31:6]	r	**Reserved** Read as 0; should be written with 0.

Note: After a hardware reset operation, the f_{CLC0} and f_{MSC0} clocks are switched off and the MSC modules are disabled (DISS set).

23.3.3.2 Fractional Divider Register

The Fractional Divider Registers control the clock rate of the shift clock f_{MSC0} and f_{MSC1}. Each MSC module has its own fractional divider register.

MSC0_FDR
MSC0 Fractional Divider Register ($0C_H$) Reset Value: 0000 0000$_H$
MSC1_FDR
MSC1 Fractional Divider Register ($0C_H$) Reset Value: 0000 0000$_H$



Field	Bits	Type	Description
STEP	[9:0]	rw	**Step Value** Reload or addition value for RESULT.
FDIS	10	rw	**Freeze Disable** This bit controls the freeze function for this module. 0_B Module operates on corrected clock, with reduced modulation jitter. 1_B Module operates on uncorrected clock, with full modulation jitter.
SM	11	rw	**Suspend Mode** SM selects between granted or immediate suspend mode.
SC	[13:12]	rw	**Suspend Control** This bit field determines the behavior of the fractional divider in suspend mode.
DM	[15:14]	rw	**Divider Mode** DM selects normal or fractional divider mode.
RESULT	[25:16]	rh	**Result Value** Bit field for the addition result.

Field	Bits	Type	Description
SUSACK	28	rh	**Suspend Mode Acknowledge** Indicates state of $\overline{\text{SPNDACK}}$ signal.
SUSREQ	29	rh	**Suspend Mode Request** Indicates state of SPND signal.
ENHW	30	rw	**Enable Hardware Clock Control** Controls operation of ECEN input and DISCLK bit.
DISCLK	31	rwh	**Disable Clock** Hardware controlled disable for f_{OUT} signal.
0	[27:26]	r	**Reserved** Read as 0; should be written with 0.

23.3.4 Port Control

MSC0 and MSC1 clock and data output lines are connected to dedicated differential output drivers. Some of the MSC module I/O lines are connected to I/O ports and therefore controlled in the port logic (see also **Figure 23-29**). The following port control operations selections must be executed for these I/O lines:

- Input/output function selection (IOCR registers)
- Pad driver characteristics selection for the outputs (PDR registers)

23.3.4.1 Input/Output Function Selection

The port input/output control registers contain the bit fields that select the digital output and input driver characteristics such as port direction (input/output) with alternate output selection, pull-up/down devices, and open-drain selections. The I/O lines for the MSC modules are controlled by the Port 5 and Port 9 input/output control registers.

Table 23-10 shows in an overview how bits and bit fields must be programmed for the required I/O functionality of the MSC I/O lines.

Table 23-10 MSC0 and MSC1 I/O Line Selection and Setup

Module	Port Lines	Input/Output Control Register Bits	I/O
MSC0	P5.8 / SON0	P5_IOCR8.PC8 = $1X01_B$ P5_PDR1.PD8 = $0XX_B$	CMOS Output[1)]
		P5_IOCR8.PC8 = $1XXX_B$ P5_PDR1.PD8 = $1XX_B$	LVDS Output
	P5.9 / SOP0A	P5_IOCR8.PC9 = $1X01_B$ P5_PDR1.PD8 = $0XX_B$	CMOS Output[1)]
		P5_IOCR8.PC9 = $1XXX1_B$ P5_PDR1.PD8 = $1XX_B$	LVDS Output
	P5.10 / FCLN0	P5_IOCR8.PC10 = $1X01_B$ P5_PDR1.PD10 = $0XX_B$	CMOS Output[1)]
		P5_IOCR8.PC10 = $1XXX_B$ P5_PDR1.PD10 = $1XX_B$	LVDS Output
	P5.11 / FCLP0A	P5_IOCR8.PC11 = $1X01_B$ P5_PDR1.PD10 = $0XX_B$	CMOS Output[1)]
		P5_IOCR8.PC11 = $1XXX_B$ P5_PDR1.PD10 = $1XX_B$	LVDS Output
	P5.4 / EN00	P5_IOCR4.PC12 = $1X01_B$	Output
	P5.5 / SDI0[2)]	P5_IOCR4.PC5 = $0XXX_B$	Input
	P9.4 / EN03	P9_IOCR4.PC4 = $1X11_B$	Output
	P9.5 / EN02	P9_IOCR4.PC5 = $1X11_B$	Output
	P9.6 / EN01	P9_IOCR4.PC6 = $1X11_B$	Output
	P9.7 / SOP0B	P9_IOCR4.PC7 = $1X11_B$	Output
	P9.8 / FCLP0B	P9_IOCR8.PC8 = $1X01_B$	Output
		P9_IOCR8.PC8 = $1X10_B$	
		P9_IOCR8.PC8 = $1X11_B$	

Table 23-10 MSC0 and MSC1 I/O Line Selection and Setup (cont'd)

Module	Port Lines	Input/Output Control Register Bits	I/O
MSC1[3]	P5.12 / SON1	P5_IOCR12.PC12 = $1X01_B$ P5_PDR1.PD12 = $0XX_B$	CMOS Output[1]
		P5_IOCR12.PC12 = $1XXX_B$ P5_PDR1.PD12 = $1XX_B$	LVDS Output
	P5.13 / SOP1A	P5_IOCR12.PC13 = $1X01_B$ P5_PDR1.PD12 = $0XX_B$	CMOS Output[1]
		P5_IOCR12.PC13 = $1XXX_B$ P5_PDR1.PD12 = $1XX_B$	LVDS Output
	P5.14 / FCLN1	P5_IOCR12.PC14 = $1X01_B$ P5_PDR1.PD14 = $0XX_B$	CMOS Output[1]
		P5_IOCR12.PC14 = $1XXX1_B$ P5_PDR1.PD14 = $1XX_B$	LVDS Output
	P5.15 / FCLP1A	P5_IOCR12.PC15 = $1X01_B$ P5_PDR1.PD14 = $0XX_B$	CMOS Output[1]
		P5_IOCR12.PC15 = $1XXX_B$ P5_PDR1.PD14 = $1XX_B$	LVDS Output
	P5.6 / EN10	P5_IOCR4.PC6 = $1X01_B$	Output
	P5.7 / SDI1[2]	P5_IOCR4.PC7 = $0XXX_B$	Input
	P9.0 / EN12	P9_IOCR0.PC0 = $1X11_B$	Output
	P9.1 / EN11	P9_IOCR0.PC1 = $1X11_B$	Output
	P9.2 / SOP1B	P9_IOCR0.PC2 = $1X10_B$	Output
	P9.3 / FCLP1B	P9_IOCR0.PC3 = $1X10_B$	Output

1) Default after reset.

2) For the upstream channel serial data inputs, additionally bit fields MSC0_OCR.SDISEL (for SDI0) and MSC1_OCR.SDISEL (for MSC1) must be set to 000_B.

3) Chip enable output 3 (EN3) of the MSC1 module is not connected in the TC1798.

23.3.5 On-Chip Connections

This section describes the on-chip connections of the MSC0/MSC1 modules.

23.3.5.1 EMGSTOPMSC Signal (from SCU)

The emergency stop input signals EMGSTOPMSC of both MSC modules are connected to the output signal of the emergency stop input control logic. This logic is located in the SCU. Its functionality is controlled by the SCU emergency stop register.

23.3.5.2 ALTINH and ALTINL Connections

In the TC1798, output lines of GPTA0, GPTA1, and LTCA2 are connected to ALTINH and ALTINL inputs of the MSC0/MSC1 downstream channels as shown in **Figure 23-32**. The setting of the GPTA-to-MSC multiplexer determines which output of the three GPTA sub-modules is connected to a specific ALTINL/ALTINH line.

Please note that the upper eight MSC1 input lines ALTINH[15:8] are connected to logic 0 level.

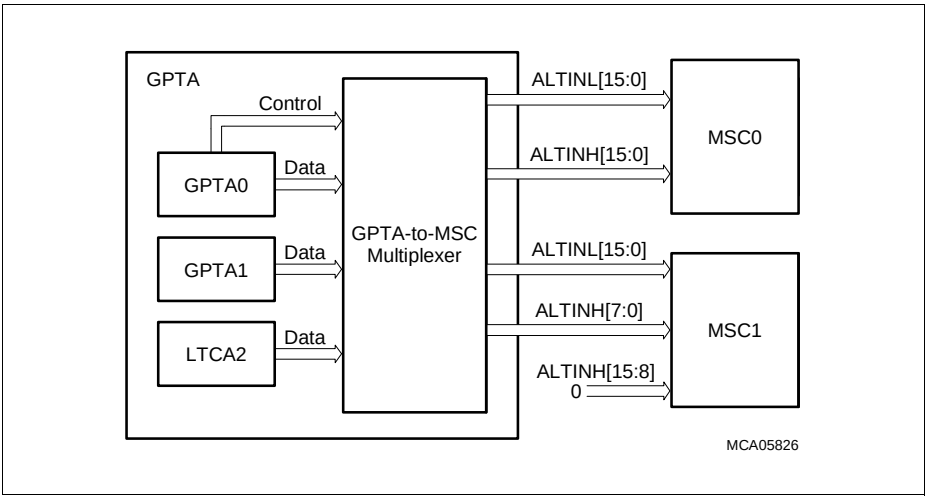


Figure 23-32 ALTINL/ALTINH Connections of the MSC0/MSC1

23.3.5.3 DMA Controller Service Requests

Two service request outputs (SR[3:2]) of each MSC module are connected as DMA request input to the DMA controller. The DMA request lines are connected to the DMA controller as shown in **Table 23-11**.

Table 23-11 Service Request Lines of MSC0/MSC1

Module	Service Request Line	Connected to	Description
MSC0	SR0	MSC0_SRC0	MSC0 Service Request Node 0
	SR1	MSC0_SRC1	MSC0 Service Request Node 1
	SR2	CH02_REQI6	DMA Channel 02 Request Input 6
		CH04_REQI6	DMA Channel 04 Request Input 6
	SR3	CH03_REQI6	DMA Channel 03 Request Input 6
		CH05_REQI6	DMA Channel 05 Request Input 6
MSC1	SR0	MSC1_SRC0	MSC1 Service Request Node 0
	SR1	MSC1_SRC1	MSC1 Service Request Node 1
	SR2	CH12_REQI14	DMA Channel 12 Request Input 14
		CH14_REQI14	DMA Channel 14 Request Input 14
	SR3	CH13_REQI14	DMA Channel 13 Request Input 14
		CH15_REQI14	DMA Channel 15 Request Input 14

23.3.6 Interrupt Control Registers

In the TC1798, the two service request outputs SR[1:0] of each MSC module are connected to one interrupt node. The upper two service request outputs SR[3:2] of each MSC module are not connected to interrupt nodes, but can be used as DMA requests (see **Table 23-11**).

SRC1
Service Request Control Register 1 ($F8_H$) Reset Value: 0000 0000$_H$
SRC0
Service Request Control Register 0 (FC_H) Reset Value: 0000 0000$_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SETR	CLRR	SRR	SRE	0	TOS	0		SRPN							
w	w	rh	rw	r	rw	r		rw							

Field	Bits	Type	Description
SRPN	[7:0]	rw	**Service Request Priority Number**
TOS	10	rw	**Type of Service Control**
SRE	12	rw	**Service Request Enable**
SRR	13	rh	**Service Request Flag**
CLRR	14	w	**Request Clear Bit**
SETR	15	w	**Request Set Bit**
0	[9:8], 11, [31:16]	r	**Reserved** Read as 0; should be written with 0.

23.3.7 MSC0/MSC1 Address Map

An absolute register address is given by the offset address of the register (given in Table 23-9) plus the module base address (given in Table 23-8).

Table 23-12 Address Map of MSC0/MSC1

Short Name	Description	Address	Access Mode		Reset Value
			Read	Write	
MicroSecond Bus Controller 0 (MSC0)					
MSC0_ CLC	MSC0 Clock Control Register	F000 0800$_H$	U, SV	SV, E	0000 0003$_H$
–	Reserved	F000 0804$_H$	BE	BE	–
MSC0_ ID	MSC0 Module Identification Register	F000 0808$_H$	U, SV	BE	0028 C0XX$_H$
MSC0_ FDR	MSC0 Fractional Divider Register	F000 080C$_H$	U, SV	SV, E	0000 0000$_H$
MSC0_ USR	MSC0 Upstream Status Register	F000 0810$_H$	U, SV	U, SV	0000 0000$_H$
MSC0_ DSC	MSC0 Downstream Control Register	F000 0814$_H$	U, SV	U, SV	0000 0000$_H$
MSC0_ DSS	MSC0 Downstream Status Register	F000 0818$_H$	U, SV	U, SV	0000 0000$_H$
MSC0_ DD	MSC0 Downstream Data Register	F000 081C$_H$	U, SV	U, SV	0000 0000$_H$
MSC0_ DC	MSC0 Downstream Command Register	F000 0820$_H$	U, SV	U, SV	0000 0000$_H$
MSC0_ DSDSL	MSC0 Downstream Select Data Source Low Register	F000 0824$_H$	U, SV	U, SV	0000 0000$_H$
MSC0_ DSDSH	MSC0 Downstream Select Data Source High Register	F000 0828$_H$	U, SV	U, SV	0000 0000$_H$
MSC0_ ESR	MSC0 Emergency Stop Register	F000 082C$_H$	U, SV	U, SV	0000 0000$_H$
MSC0_ UD0	MSC0 Upstream Data Register 0	F000 0830$_H$	U, SV	U, SV	0000 0000$_H$
MSC0_ UD1	MSC0 Upstream Data Register 1	F000 0834$_H$	U, SV	U, SV	0000 0000$_H$

Table 23-12 Address Map of MSC0/MSC1 (cont'd)

Short Name	Description	Address	Access Mode		Reset Value
			Read	Write	
MSC0_ UD2	MSC0 Upstream Data Register 2	F000 0838$_H$	U, SV	U, SV	0000 0000$_H$
MSC0_ UD3	MSC0 Upstream Data Register 3	F000 083C$_H$	U, SV	U, SV	0000 0000$_H$
MSC0_ ICR	MSC0 Interrupt Control Register	F000 0840$_H$	U, SV	U, SV	0000 0000$_H$
MSC0_ ISR	MSC0 Interrupt Status Register	F000 0844$_H$	U, SV	U, SV	0000 0000$_H$
MSC0_ ISC	MSC0 Interrupt Set Clear Register	F000 0848$_H$	U, SV	U, SV	0000 0000$_H$
MSC0_ OCR	MSC0 Output Control Register	F000 084C$_H$	U, SV	U, SV	0000 0000$_H$
–	Reserved	F000 0850$_H$ - F000 0854$_H$	nBE	nBE	–
		F000 0858$_H$ - F000 08F4$_H$	BE	BE	–
MSC0_ SRC1	MSC0 Service Request Control Register 1	F000 08F8$_H$	U, SV	U, SV	0000 0000$_H$
MSC0_ SRC0	MSC0 Service Request Control Register 0	F000 08FC$_H$	U, SV	U, SV	0000 0000$_H$
Micro Second Channel 1 (MSC1)					
MSC1_ CLC	MSC1 Clock Control Register	F000 0900$_H$	U, SV	SV, E	0000 0003$_H$
–	Reserved	F000 0904$_H$	BE	BE	–
MSC1_ ID	MSC1 Module Identification Register	F000 0908$_H$	U, SV	BE	0000 44XX$_H$
MSC1_ FDR	MSC1 Fractional Divider Register	F000 090C$_H$	U, SV	SV, E	0000 0000$_H$
MSC1_ USR	MSC1 Upstream Status Register	F000 0910$_H$	U, SV	U, SV	0000 0000$_H$
MSC1_ DSC	MSC1 Downstream Control Register	F000 0914$_H$	U, SV	U, SV	0000 0000$_H$

Table 23-12 Address Map of MSC0/MSC1 (cont'd)

Short Name	Description	Address	Access Mode		Reset Value
			Read	Write	
MSC1_ DSS	MSC1 Downstream Status Register	F000 0918$_H$	U, SV	U, SV	0000 0000$_H$
MSC1_ DD	MSC1 Downstream Data Register	F000 091C$_H$	U, SV	U, SV	0000 0000$_H$
MSC1_ DC	MSC1 Downstream Command Register	F000 0920$_H$	U, SV	U, SV	0000 0000$_H$
MSC1_ DSDSL	MSC1 Downstream Select Data Source Low Register	F000 0924$_H$	U, SV	U, SV	0000 0000$_H$
MSC1_ DSDSH	MSC1 Downstream Select Data Source High Register	F000 0928$_H$	U, SV	U, SV	0000 0000$_H$
MSC1_ ESR	MSC1 Emergency Stop Register	F000 092C$_H$	U, SV	U, SV	0000 0000$_H$
MSC1_ UD0	MSC1 Upstream Data Register 0	F000 0930$_H$	U, SV	U, SV	0000 0000$_H$
MSC1_ UD1	MSC1 Upstream Data Register 1	F000 0934$_H$	U, SV	U, SV	0000 0000$_H$
MSC1_ UD2	MSC1 Upstream Data Register 2	F000 0938$_H$	U, SV	U, SV	0000 0000$_H$
MSC1_ UD3	MSC1 Upstream Data Register 3	F000 093C$_H$	U, SV	U, SV	0000 0000$_H$
MSC1_ ICR	MSC1 Interrupt Control Register	F000 0940$_H$	U, SV	U, SV	0000 0000$_H$
MSC1_ ISR	MSC1 Interrupt Status Register	F000 0944$_H$	U, SV	U, SV	0000 0000$_H$
MSC1_ ISC	MSC1 Interrupt Set Clear Register	F000 0948$_H$	U, SV	U, SV	0000 0000$_H$
MSC1_ OCR	MSC1 Output Control Register	F000 094C$_H$	U, SV	U, SV	0000 0000$_H$
–	Reserved	F000 0950$_H$ - F000 0954$_H$	nBE	nBE	–

Table 23-12 Address Map of MSC0/MSC1 (cont'd)

Short Name	Description	Address	Access Mode		Reset Value
			Read	Write	
MSC1_ SRC1	MSC1 Service Request Control Register 1	F000 09F8$_H$	U, SV	U, SV	0000 0000$_H$
MSC1_ SRC0	MSC1 Service Request Control Register 0	F000 09FC$_H$	U, SV	U, SV	0000 0000$_H$

24 Controller Area Network Controller (MultiCAN)

This chapter describes the MultiCAN controller of the TC1798. It contains the following sections:

- CAN basics (see **Page 24-2**)
- Overview of the CAN Module in the TC1798 (see **Page 24-14**)
- Functional description of the MultiCAN Kernel (see **Page 24-18**)
- MultiCAN Kernel register description (see **Page 24-60**)
- Functional description of the TTCAN extension (see **Page 24-117**)
- TTCAN extension register description (see **Page 24-157**)
- TC1798 implementation-specific details (port connections and control, interrupt control, address decoding, clock control, see **Page 24-202**).

Note: The MultiCAN register names described in this chapter are referenced in the TC1798 User´s Manual by the module name prefix “CAN_”.

Table 24-1 Fixed Module Constants

Constant	Description
n_objects	**Number of Message Objects available.**
n_interrupts	**Number of Interrupt Output Lines available.**
n_pendings **n_pendingregs**	**Number of Message Pending Bits available.** There are n_pendings/32 message pending registers.
n_lists	**Number of Lists available for allocation of Message Objects.**
n_nodes	**Number of CAN Nodes available** As each CAN node has it’s own list in addition to the list of un-allocated elements, the relation n_nodes < n_lists is true.

24.1 CAN Basics

CAN is an asynchronous serial bus system with one logical bus line. It has an open, linear bus structure with equal bus participants called nodes. A CAN bus consists of two or more nodes.

The bus logic corresponds to a “wired-AND” mechanism. Recessive bits (equivalent to the logic 1 level) are overwritten by dominant bits (logic 0 level). As long as no bus node is sending a dominant bit, the bus is in the recessive state. In this state, a dominant bit from any bus node generates a dominant bus state. The maximum CAN bus speed is, by definition, 1 Mbit/s. This speed limits the CAN bus to a length of up to 40 m. For bus lengths longer than 40 m, the bus speed must be reduced.

The binary data of a CAN frame is coded in NRZ code (Non-Return-to-Zero). To ensure re-synchronization of all bus nodes, bit stuffing is used. This means that during the transmission of a message, a maximum of five consecutive bits can have the same polarity. Whenever five consecutive bits of the same polarity have been transmitted, the transmitter will insert one additional bit (stuff bit) of the opposite polarity into the bit stream before transmitting further bits. The receiver also checks the number of bits with the same polarity and removes the stuff bits from the bit stream (= destuffing).

24.1.1 Addressing and Bus Arbitration

In the CAN protocol, address information is defined in the identifier field of a message. The identifier indicates the contents of the message and its priority. The lower the binary value of the identifier, the higher is the priority of the message.

For bus arbitration, CSMA/CD with NDA (Carrier Sense Multiple Access/Collision Detection with Non-Destructive Arbitration) is used. If bus node A attempts to transmit a message across the network, it first checks that the bus is in the idle state (“Carrier Sense”) i.e. no node is currently transmitting. If this is the case (and no other node wishes to start a transmission at the same moment), node A becomes the bus master and sends its message. All other nodes switch to receive mode during the first transmitted bit (Start-Of-Frame bit). After correct reception of the message (acknowledged by each node), each bus node checks the message identifier and stores the message, if required. Otherwise, the message is discarded.

If two or more bus nodes start their transmission at the same time (“Multiple Access”), bus collision of the messages is avoided by bit-wise arbitration (“Collision Detection / Non-Destructive Arbitration” together with the “Wired-AND” mechanism, dominant bits override recessive bits). Each node that sends also reads back the bus level. When a recessive bit is sent but a dominant one is read back, bus arbitration is lost and the transmitting node switches to receive mode. This condition occurs for example when the message identifier of a competing node has a lower binary value and therefore sends a message with a higher priority. In this way, the bus node with the highest priority message wins arbitration without losing time by having to repeat the message. Other nodes that lost arbitration will automatically try to repeat their transmission once the bus

returns to idle state. Therefore, the same identifier can be sent in a Data Frame only by one node in the system. There must not be more than one node programmed to send Data Frames with the same identifier.

Standard message identifier has a length of 11 bits. CAN specification 2.0B extends the message identifier lengths to 29 bits, i.e. the extended identifier.

24.1.2 CAN Frame Formats

There are three types of CAN frames:

- Data Frames
- Remote Frames
- Error Frames

A Data Frame contains a Data Field of 0 to 8 bytes in length. A Remote Frame contains no Data Field and is typically generated as a request for data (e.g. from a sensor). Data and Remote Frames can use an 11-bit “Standard” identifier or a 29-bit “Extended” identifier. An Error Frame can be generated by any node that detects a CAN bus error.

24.1.2.1 Data Frames

There are two types of Data Frames defined (see **Figure 24-1**):

- Standard Data Frame
- Extended Data Frame

Standard Data Frame

A Data Frame begins with the Start-Of-Frame bit (SOF = dominant level) for hard synchronization of all nodes. The SOF is followed by the Arbitration Field consisting of 12 bits, the 11-bit identifier (reflecting the contents and priority of the message), and the RTR (Remote Transmission Request) bit. With RTR at dominant level, the frame is marked as Data Frame. With RTR at recessive level, the frame is defined as a Remote Frame.

The next field is the Control Field consisting of 6 bits. The first bit of this field is the IDE (Identifier Extension) bit and is at dominant level for the Standard Data Frame. The following bit is reserved and defined as a dominant bit. The remaining 4 bits of the Control Field are the Data Length Code (DLC) that specifies the number of bytes in the Data Field. The Data Field can be 0 to 8 bytes wide. The Cyclic Redundancy (CRC) Field that follows the data bytes is used to detect possible transmission errors. It consists of a 15-bit CRC sequence, completed by a recessive CRC delimiter bit.

The final field is the Acknowledge Field. During the ACK Slot, the transmitting node sends out a recessive bit. Any node that has received an error free frame acknowledges the correct reception of the frame by sending back a dominant bit, regardless of whether or not the node is configured to accept that specific message. This behavior assigns the

CAN protocol to the “in-bit-response” group of protocols. The recessive ACK delimiter bit, which must not be overwritten by a dominant bit, completes the Acknowledge Field.

Seven recessive End-of-Frame (EOF) bits finish the Data Frame. Between any two consecutive frames, the bus must remain in the recessive state for at least 3 bit times (called Inter Frame Space). If after the Inter Frame Space, no other nodes attempt to transmit the bus remains in idle state with a recessive level.

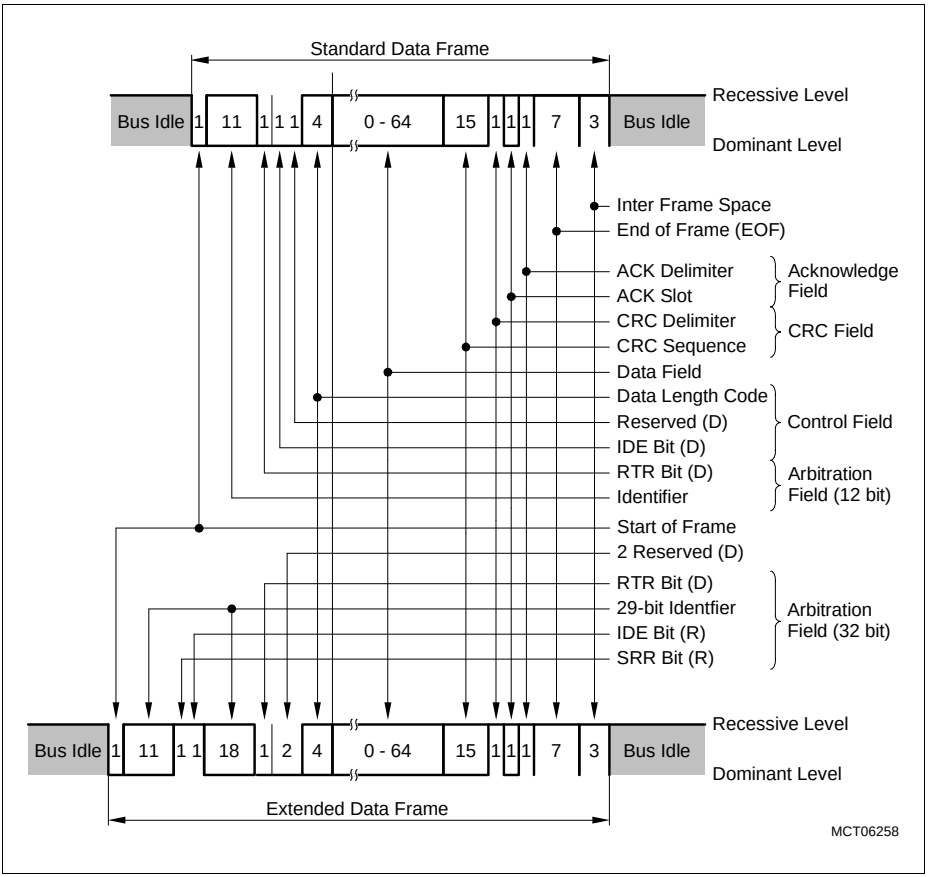


Figure 24-1 CAN Data Frame

Extended Data Frame

In the Extended CAN Data Frame, the message identifier of the standard frame has been extended to 29-bit. A split of the extended identifier into two parts, an 11-bit least

significant section (as in standard CAN frame) and an 18-bit most significant section, ensures that the Identifier Extension bit (IDE) can remain at the same bit position in both standard and extended frames.

In the Extended CAN Data Frame, the SOF bit is followed by the 32-bit Arbitration Field. The first 11 bits are the least significant bits of the 29-bit Identifier (“Base-ID”). These 11 bits are followed by the recessive Substitute Remote Request (SRR) bit. The SRR is further followed by the recessive IDE bit, which indicates the frame to be an Extended CAN frame. If arbitration remains unresolved after transmission of the first 11 bits of the identifier, and if one of the nodes involved in arbitration is sending a Standard CAN frame, then the Standard CAN frame will win arbitration due to the assertion of its dominant IDE bit. Therefore, the SRR bit in an Extended CAN frame is recessive to allow the assertion of a dominant RTR bit by a node that is sending a Standard CAN Remote Frame. The SRR and IDE bits are followed by the remaining 18 bits of the extended identifier and the RTR bit.

Control field and frame termination is identical to the Standard Data Frame.

24.1.2.2 Remote Frames

Normally, data transmission is performed on an autonomous basis with the data source node (e.g. a sensor) sending out a Data Frame. It is also possible, however, for a destination node (or nodes) to request the data from the source. For this purpose, the destination node sends a Remote Frame with an identifier that matches the identifier of the required Data Frame. The appropriate data source node will then send a Data Frame as a response to this remote request.

There are 2 differences between a Remote Frame and a Data Frame.

- The RTR bit is in the recessive state in a Remote Frame.
- There is no Data Field in a Remote Frame.

If a Data Frame and a Remote Frame with the same identifier are transmitted at the same time, the Data Frame wins arbitration due to the dominant RTR bit following the identifier. In this way, the node that transmitted the Remote Frame receives the requested data immediately. The format of a Standard and Extended Remote Frames is shown in **Figure 24-2**.

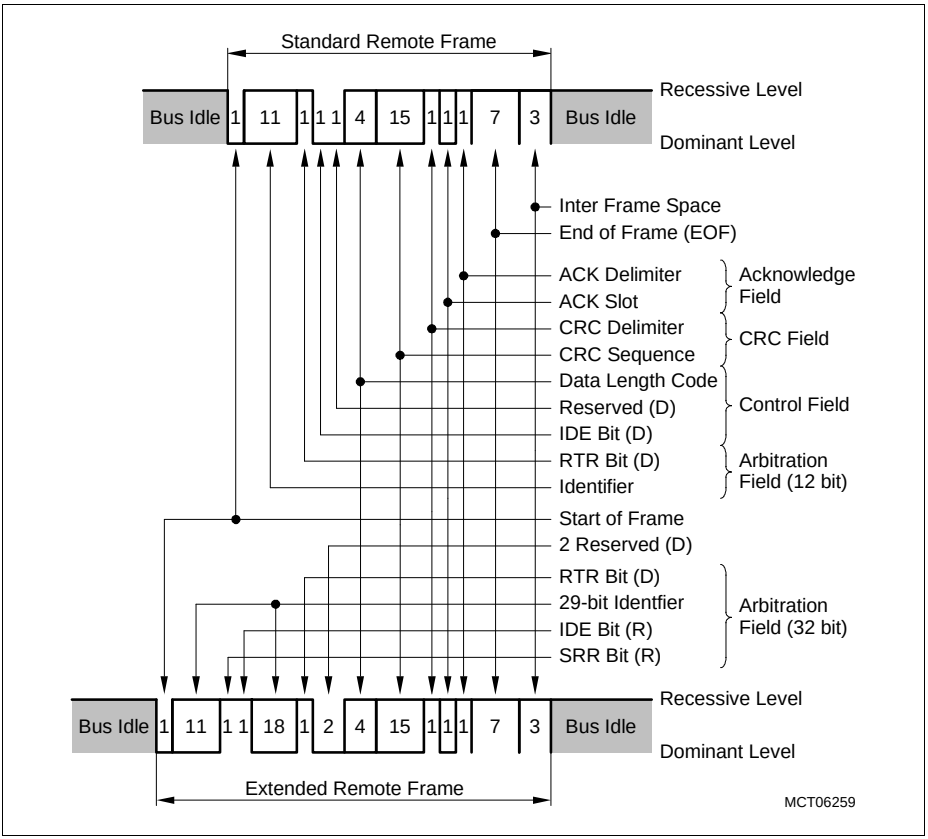


Figure 24-2 CAN Remote Frame

24.1.2.3 Error Frames

An Error Frame is generated by any node that detects a bus error. An Error Frame consists of two fields, an Error Flag field followed by an Error Delimiter field. The Error Delimiter Field consists of 8 recessive bits and allows the bus nodes to restart bus communications after an error. There are, however, two forms of Error Flag fields. The form of the Error Flag field depends on the error status of the node that detects the error.

When an error-active node detects a bus error, the node generates an Error Frame with an active-error flag. The error-active flag is composed of six consecutive dominant bits that actively violate the bit-stuffing rule. All other stations recognize a bit-stuffing error and generate Error Frames themselves. The resulting Error Flag field on the CAN bus therefore consists of six to twelve consecutive dominant bits (generated by one or more nodes). The Error Delimiter field completes the Error Frame. After completion of the Error Frame, bus activity returns to normal and the interrupted node attempts to re-send the aborted message.

If an error-passive node detects a bus error, the node transmits an error-passive flag followed, again, by the Error Delimiter field. The error-passive flag consists of six consecutive recessive bits, and therefore the Error Frame (for an error-passive node) consists of 14 recessive bits (i.e. no dominant bits). Therefore, the transmission of an Error Frame by an error-passive node will not affect any other node on the network, unless the bus error is detected by the node that is actually transmitting (i.e. the bus master). If the bus master node generates an error-passive flag, this may cause other nodes to generate Error Frames due to the resulting bit-stuffing violation. After transmission of an Error Frame an error-passive node must wait for 6 consecutive recessive bits on the bus before attempting to rejoin bus communications.

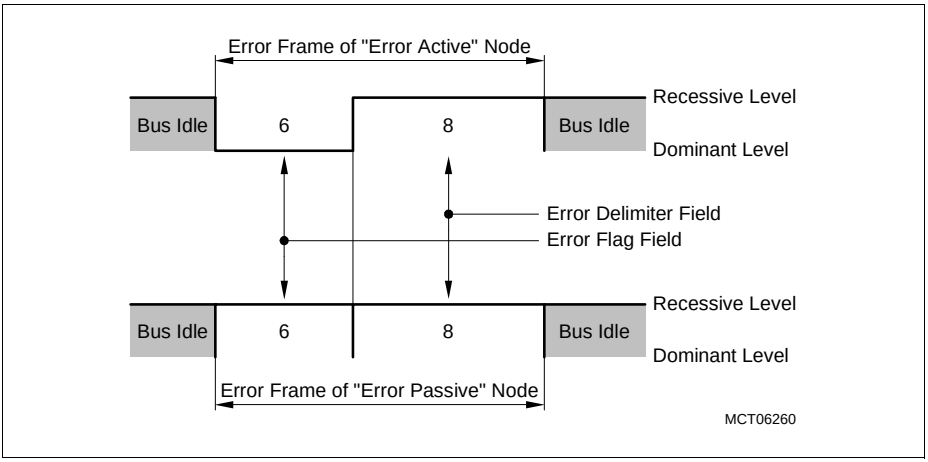


Figure 24-3 CAN Error Frames

24.1.3 The Nominal Bit Time

One bit cell (this means one high or low pulse of the NRZ code) is composed by four segments. Each segment is an integer multiple of Time Quanta t_Q. The Time Quanta is the smallest discrete timing resolution used by a CAN node. The nominal bit time definition with its segments is shown in **Figure 24-4**.

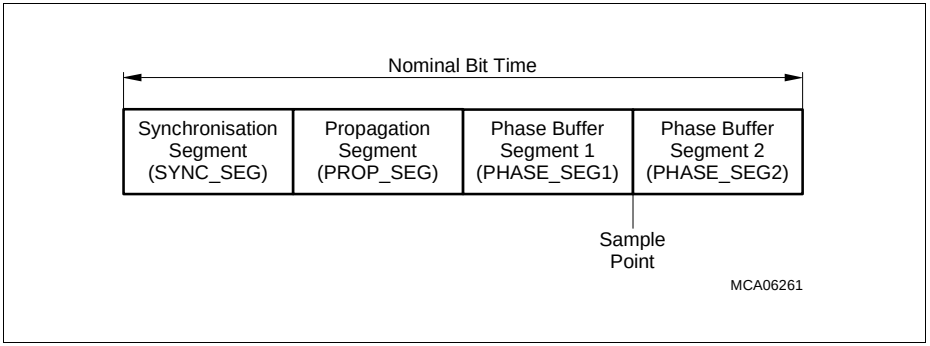


Figure 24-4 Partition of Nominal Bit Time

The Synchronization Segment (SYNC_SEG) is used to synchronize the various bus nodes. If there is a bit state change between the previous bit and the current bit, then the bus state change is expected to occur within this segment. The length of this segment is always 1 t_Q.

The Propagation Segment (PROP_SEG) is used to compensate for signal delays across the network. These delays are caused by signal propagation delay on the bus line and through the electronic interface circuits of the bus nodes.

The Phase Segments 1 and 2 (PHASE_SEG1, PHASE_SEG2) are used to compensate for edge phase errors. These segments can be lengthened or shortened by re-synchronization. PHASE_SEG2 is reserved for calculation of the subsequent bit level, and is $\geq 2\ t_Q$. At the sample point, the bus level is read and interpreted as the value of the bit cell. It occurs at the end of PHASE_SEG1.

The total number of t_Q in a bit time is between 8 and 25.

As a result of re-synchronization, PHASE_SEG1 can be lengthened or PHASE_SEG2 can be shortened. The amount of lengthening or shortening the phase buffer segments has an upper limit given by the re-synchronization jump width. The re-synchronization jump width may be between 1 and 4 t_Q, but it may not be longer than PHASE_SEG1.

24.1.4 Error Detection and Error Handling

The CAN protocol has sophisticated error detection mechanisms. The following errors can be detected:

- **Cyclic Redundancy Check (CRC) Error**
  With the Cyclic Redundancy Check, the transmitter calculates special check bits for the bit sequence from the start of a frame until the end of the Data Field. This CRC sequence is transmitted in the CRC Field. The receiving node also calculates the CRC sequence using the same formula, and performs a comparison to the received sequence. If a mismatch is detected, a CRC error has occurred and an Error Frame is generated. The message is repeated.
- **Acknowledge Error**
  In the Acknowledge Field of a message, the transmitter checks whether a dominant bit is read during the Acknowledge Slot (that is sent out as a recessive bit). If not, no other node has received the frame correctly, an Acknowledge Error has occurred, and the message must be repeated. No Error Frame is generated.
- **Form Error**
  If a transmitter detects a dominant bit in one of the four segments End of Frame, Interframe Space, Acknowledge Delimiter, or CRC Delimiter, a Form Error has occurred, and an Error Frame is generated. The message is repeated.
- **Bit Error**
  A Bit Error occurs if a) a transmitter sends a dominant bit and detects a recessive bit or b) if the transmitter sends a recessive bit and detects a dominant bit when monitoring the actual bus level and comparing it to the just transmitted bit. In case b), no error occurs during the Arbitration Field (ID, RTR, IDE) and the Acknowledge Slot.
- **Stuff Error**
  If between Start of Frame and CRC Delimiter, six consecutive bits with the same polarity are detected, the bit-stuffing rule has been violated. A stuff error occurs and an Error Frame is generated. The message is repeated.

Detected errors are made public to all other nodes via Error Frames (except Acknowledge Errors). The transmission of the erroneous message is aborted and the frame is repeated as soon as possible. Furthermore, each CAN node is in one of the three error states (error-active, error-passive or bus-off) according to the value of the internal error counters. The error-active state is the usual state where the bus node can transmit messages and active-error frames (made of dominant bits) without any restrictions. In the error-passive state, messages and passive-error frames (made of recessive bits) may be transmitted. The bus-off state makes it temporarily impossible for the node to participate in the bus communication. During this state, messages can be neither received nor transmitted.

Basic CAN, Full CAN

There is one more CAN characteristic that is related to the interface of a CAN module (controller) and the host CPU: Basic-CAN and Full-CAN functionality.

In Basic-CAN devices, only basic functions of the protocol are implemented in hardware, such as the generation and the check of the bit stream. The decision, whether a received message has to be stored or not (acceptance filtering), and the complete message management must be done by software. Normally, the CAN device also provides only one transmit buffer and one or two receive buffers. Therefore, the host CPU load is quite high when using Basic-CAN modules. The main advantage of Basic-CAN is a reduced chip size leading to low costs of these devices.

Full-CAN devices (this is the case for the MultiCAN controller as implemented in TC1798) manage the whole bus protocol in hardware, including the acceptance filtering and message management. Full-CAN devices contain message objects that handle autonomously the identifier, the data, the direction (receive or transmit) and the information of Standard CAN/Extended CAN operation. During the initialization of the device, the host CPU determines which messages are to be sent and which are to be received. The host CPU is informed by interrupt if the identifier of a received message matches with one of the programmed (receive-) message objects. The CPU load of Full-CAN devices is greatly reduced. When using Full-CAN devices, high baud rates and high bus loads with many messages can be handled.

24.2 TTCAN Basics

In general, a CAN network is event-oriented due to the error handling and bus arbitration. The exact time for a message to be transferred is difficult to determine. In order to allow deterministic message transfers, the event-driven mechanism has been changed into a time-driven mechanism by a TTCAN extension, with “TT” standing for Time-Triggered.

TTCAN is a higher-layer protocol above the standard CAN protocol that synchronizes the communication schedules of all CAN nodes in a CAN network, and that provides a global system time. When CAN nodes are synchronized, messages can be transmitted at a specific time slot, without competing with other messages for the bus. Thus, the loss of arbitration is avoided, and the latency time becomes predictable. Apart from the synchronized communication schedule, TTCAN-compliant nodes operate according to the standard CAN protocol as defined by ISO 11898-4.

24.2.1 Time Reference

In TTCAN networks, a global time reference makes it possible to synchronize the activities of all CAN nodes. Each CAN node has its own local time represented by a counter that is incremented with each network time unit (NTU). The NTU is derived from the node’s local clock and local Time Unit Ratio (TUR).

In TTCAN, synchronization is achieved by a periodic transmission of a reference message. This reference message (transmitted by a time master) restarts the cycle time in each node. The reference message can be easily recognized by its identifier. Within TTCAN level 1, the reference message holds control information in one byte of the message Data Field. In TTCAN level 2, the reference message provides additional control information in four bytes of the message Data Field (e.g. the global time information of the current TTCAN time master) with downwards compatibility.

24.2.2 Basic Cycle

A reference message starts a new basic cycle and resets the cycle time. The cycle time counts the time since the start of the basic cycle. A basic cycle consists of several non-overlapping time windows of different sizes. The sequence of the time windows is described by time marks that determine when a time window begins. Time marks are compared to the cycle time, and particular actions are triggered when the cycle time matches the time mark.

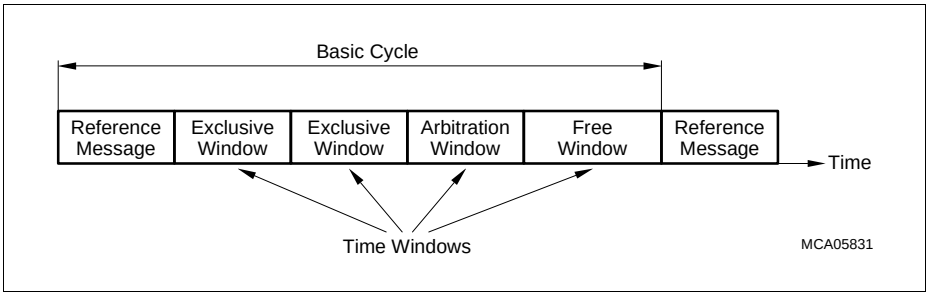


Figure 24-5 TTCAN Basic Cycle

The structure of the basic cycle is defined once for the whole TTCAN network. Several different basic cycles are combined to build a matrix cycle or the system matrix. The sequence of basic cycles in the matrix cycle is controlled by the reference messages.

All possible messages in the TTCAN system are assigned to time windows of the system matrix. A time window can be:

- An exclusive time window, in which only one particular message can be transmitted.
- An arbitrating time window, in which messages can arbitrate for bus access.
- A free time window, reserved for future extensions.

In exclusive time windows automatic retransmission of messages is disabled. This guarantees that messages are not delayed by other bus traffic.

24.2.3 Global System Time

Level 2 of TTCAN supports a global system time. The time master establishes its own local time as global time by transmitting reference message. The other CAN nodes in the network operate as time slaves that calculate their local time offset to the global time by comparing their local time with the received global time. To compensate for slightly different clock drifts in the CAN nodes and to provide a consistent view of the global time, the nodes can perform a drift compensation operation. They compare the length of the basic cycle in local time to the length of the basic cycle in global time. The difference (quotient) of the two values gives the adapted TUR.

24.2.4 The System Matrix

Typical CAN applications include many control loops and tasks with different periods. All of them need individual sending patterns for their information. One TTCAN basic cycle would not offer enough flexibility to satisfy this needs. Therefore, the TTCAN specification also makes it possible to use more than one basic cycle to build the communication matrix or system matrix. Several different basic cycles are connected together to build the matrix cycle. Most combinations of basic cycles are possible, such

as sending every basic cycle, sending every second basic cycle, or sending only once within the matrix cycle.

24.2.5 Generation of the Network Time Unit (NTU)

The granularity of any timing information within TTCAN is the NTU. The cycle time is measured in NTU that is based on the nominal CAN bit time (TTCAN level 1), or on the Time Quantum t_Q (TTCAN level 2), or on the CAN input frequency. In level 2, the node's local relation between the physical oscillator of a TTCAN controller and the system wide NTU must be established. A clock signal in the node provides the system clock to a frequency divider. This frequency divider generates the system-wide NTU while a node local TUR takes care for the correct relationship between the system clock and NTU. NTU now can be used to calculate a local time and to build the global time.

24.2.6 Global Time Generation and Drift Correction

The node sending the reference message is the time master in the TTCAN network. The reference message includes the time master's (by definition correct) global time value for frame synchronization. All nodes take a snap-shot of their time values at the SOF bit sample point of the received reference message. After reference message reception, each node can calculate its local offset that indicates the difference between the master global time value and the own local time value. In the current basic cycle, the node can compute the global time for the next basic cycle by:

global time = local time + local offset

This equation ensures that all nodes have a consistent global time. Due to slightly different clock drifts of the different nodes in a CAN network, a mechanism is established that guarantees that local and global time run in parallel. This mechanism is the continuous update of the TUR. The initial value of TUR is locally known in the node by the node clock signal specification. During node operation, the node locally measures the length between two successive reference messages in number of oscillator periods and in local time. The quotient of these two values gives the actual TUR. The achievable precision determines a reasonable choice of the NTU value in physical seconds.

24.3 Overview

This section describes the serial communication module called MultiCAN (CAN = Controller Area Network) of the TC1798. A MultiCAN module can contain between two and eight independent CAN nodes, depending on the device, each representing one serial communication interface.

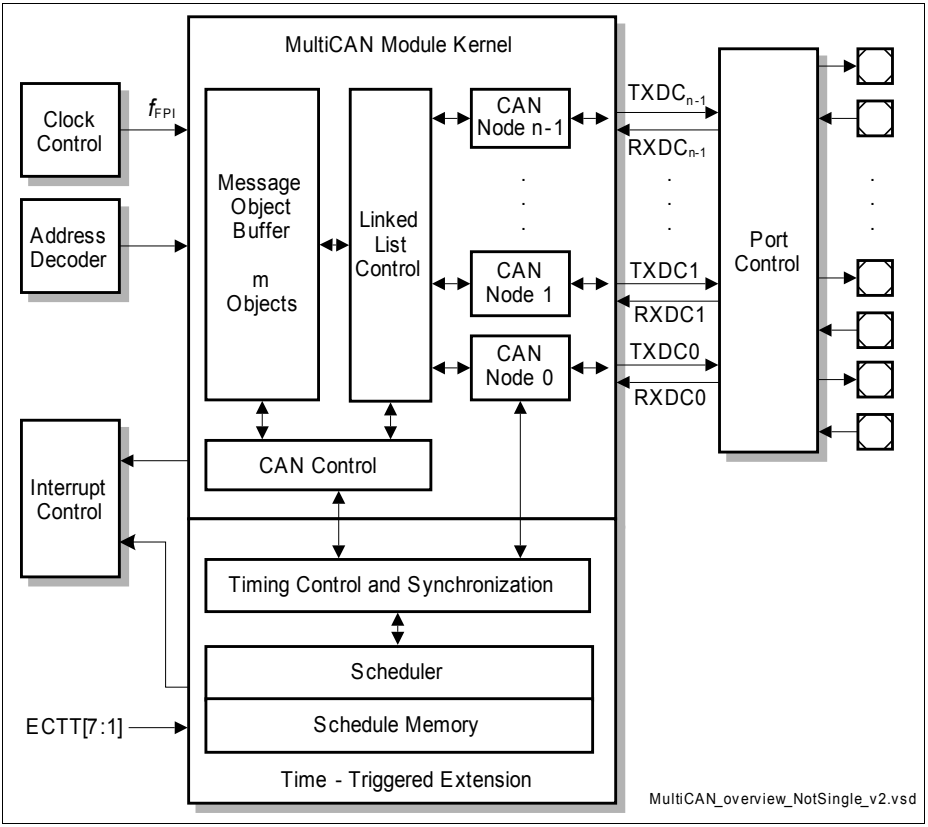


Figure 24-6 Overview of the MultiCAN Module with TTCAN extension

24.3.1 MultiCAN Module

The MultiCAN module contains independently operating CAN nodes with Full-CAN functionality that are able to exchange Data and Remote Frames via a gateway function. Transmission and reception of CAN frames is handled in accordance with CAN specification V2.0 B (active). Each CAN node can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers.

Both CAN nodes share a common set of message objects. Each message object can be individually allocated to one of the CAN nodes. Besides serving as a storage container for incoming and outgoing frames, message objects can be combined to build gateways between the CAN nodes or to setup a FIFO buffer.

The message objects are organized in double-chained linked lists, where each CAN node has its own list of message objects. A CAN node stores frames only into message objects that are allocated to the message object list of the CAN node, and it transmits only messages belonging to this message object list. A powerful, command-driven list controller performs all message object list operations.

The bit timings for the CAN nodes are derived from the module timer clock (f_{CAN}), and are programmable up to a data rate of 1 Mbit/s. External bus transceivers are connected to a CAN node via a pair of receive and transmit pins.

Features

- Compliant with ISO 11898
- CAN functionality according to CAN specification V2.0 B active
- Dedicated control registers for each CAN node
- Data transfer rates up to 1 Mbit/s
- Flexible and powerful message transfer control and error handling capabilities
- Advanced CAN bus bit timing analysis and baud rate detection for each CAN node via a frame counter
- Full-CAN functionality: A set of message objects can be individually
  - Allocated (assigned) to any CAN node
  - Configured as transmit or receive object
  - Set up to handle frames with 11-bit or 29-bit identifier
  - Identified by a timestamp via a frame counter
  - Configured to remote monitoring mode
- Advanced acceptance filtering
  - Each message object provides an individual acceptance mask to filter incoming frames
  - A message object can be configured to accept standard or extended frames or to accept both standard and extended frames
  - Message objects can be grouped into four priority classes for transmission and reception

  - The selection of the message to be transmitted first can be based on frame identifier, IDE bit and RTR bit according to CAN arbitration rules, or according to its order in the list
- Advanced message object functionality
  - Message objects can be combined to build FIFO message buffers of arbitrary size, limited only by the total number of message objects
  - Message objects can be linked to form a gateway that automatically transfers frames between two different CAN buses. A single gateway can link any two CAN nodes. An arbitrary number of gateways can be defined.
- Advanced data management
  - The message objects are organized in double-chained lists
  - List reorganizations can be performed at any time, even during full operation of the CAN nodes
  - A powerful, command-driven list controller manages the organization of the list structure and ensures consistency of the list
  - Message FIFOs are based on the list structure and can easily be scaled in size during CAN operation
  - Static allocation commands offer compatibility with TwinCAN applications that are not list-based
- Advanced interrupt handling
  - Up to 16 interrupt output lines are available. Interrupt requests can be routed individually to one of the 16 interrupt output lines
  - Message post-processing notifications can be mapped flexibly using dedicated registers consisting of notification bits

24.4 Time-Triggered Extension (TTCAN)

In addition to the event-driven CAN functionality, a deterministic behavior can be achieved for CAN node 0 by an extension module that supports TTCAN functionality. The TTCAN protocol is compliant with the confirmed standardization proposal for ISO 11898-4 and fully conforms to the existing CAN protocol.

The time-triggered functionality is added as higher-layer extension (session layer) to the CAN protocol in order to be able to operate in safety-critical applications. The new features allow for deterministic behavior of a CAN network and the synchronization of networks. Global time information is available. The time-triggered extension is based on a scheduler mechanism with a timing control unit and a dedicated timing data part.

TTCAN Features

- Full support of basic cycle and system matrix functionality
- Support of reference messages level 1 and level 2
- Usable as time master
- Arbitration windows supported in time-triggered mode
- Global time information available
- CAN node 0 can be configured either for event-driven or time-triggered mode
- Built-in scheduler mechanism and a timing synchronization unit
- Write protection for scheduler timing data memory
- Timing-related interrupt functionality
- Parity protection for scheduler memory

24.5 MultiCAN Kernel Functional Description

This section describes the functionality of the MultiCAN module.

24.5.1 Module Structure

Figure 24-7 shows the general structure of the MultiCAN module.

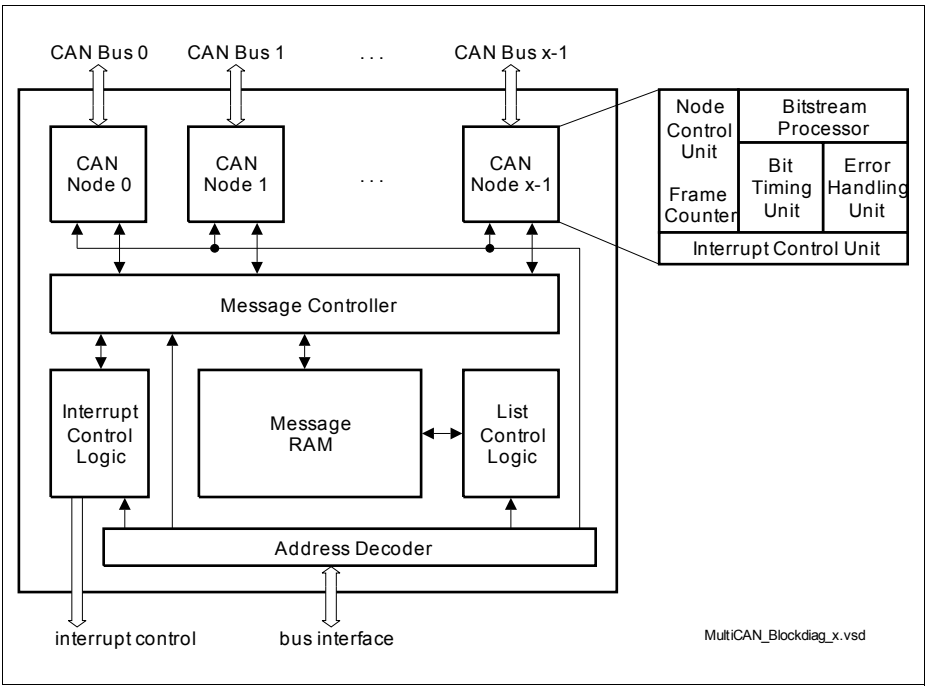


Figure 24-7 MultiCAN Block Diagram

CAN Nodes

Each CAN node consists of several sub-units.

- **Bitstream Processor**
  The Bitstream Processor performs data, remote, error and overload frame processing according to the ISO 11898 standard. This includes conversion between the serial data stream and the input/output registers.
- **Bit Timing Unit**
  The Bit Timing Unit determines the length of a bit time and the location of the sample point according to the user settings, taking into account propagation delays and phase shift errors. The Bit Timing Unit also performs resynchronization.

- **Error Handling Unit**
  The Error Handling Unit manages the receive and transmit error counter. Depending on the contents of both counters, the CAN node is set into an error-active, error passive or bus-off state.
- **Node Control Unit**
  The Node Control Unit coordinates the operation of the CAN node:
  – Enable/disable CAN transfer of the node
  – Enable/disable and generate node-specific events that lead to an interrupt request (CAN bus errors, successful frame transfers etc.)
  – Administration of the Frame Counter
- **Interrupt Control Unit**
  The Interrupt Control Unit in the CAN node controls the interrupt generation for the different conditions that can occur in the CAN node.

Message Controller

The Message Controller handles the exchange of CAN frames between the CAN nodes and the message objects that are stored in the Message RAM. The Message Controller performs several functions:

- Receive acceptance filtering to determine the correct message object for storing of a received CAN frame
- Transmit acceptance filtering to determine the message object to be transmitted first, individually for each CAN node
- Transfer contents between message objects and the CAN nodes, taking into account the status/control bits of the message objects
- Handling of the FIFO buffering and gateway functionality
- Aggregation of message-pending notification bits

List Controller

The List Controller performs all operations that lead to a modification of the double-chained message object lists. Only the list controller is allowed to modify the list structure. The allocation/deallocation or reallocation of a message object can be requested via a user command interface (command panel). The list controller state machine then performs the requested command autonomously.

Interrupt Control

The general interrupt structure is shown in **Figure 24-9**. The interrupt event can trigger the interrupt generation. The interrupt pulse is generated independently of the interrupt flag in the interrupt status register. The interrupt flag can be reset by software by writing a 0 to it.

If enabled by the related interrupt enable bit in the interrupt enable register, an interrupt pulse can be generated at one of the 16 interrupt output lines INT_Om of the MultiCAN

module. If more than one interrupt source is connected to the same interrupt node pointer (in the interrupt node pointer register), the requests are combined to one common line.

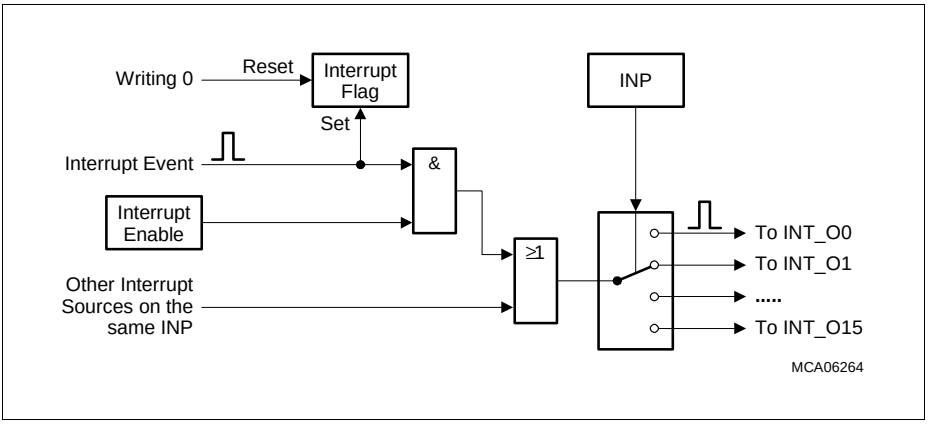


Figure 24-8 General Interrupt Structure

24.5.2 Clock Control

The CAN module timer clock f_{CAN} of the functional blocks of the MultiCAN module is derived from the module control clock f_{CLC}. The Fractional Divider is used to generate f_{CAN} used for bit timing calculation, the generation of the NTU, and the local time of the TTCAN part. The frequency of f_{CAN} is identical for all CAN nodes. The register file and the TTCAN scheduler operate with the module control clock f_{CLC}. See also **"Module Clock Generation" on Page 24-204**.

The output clock f_{CAN} of the Fractional Divider is based on the system clock f_{CLC}, but only every n-th clock pulse is taken. The suspend signal (coming as acknowledge from the MultiCAN module in response to a OCDS suspend request) freezes or resets the Fractional Divider.

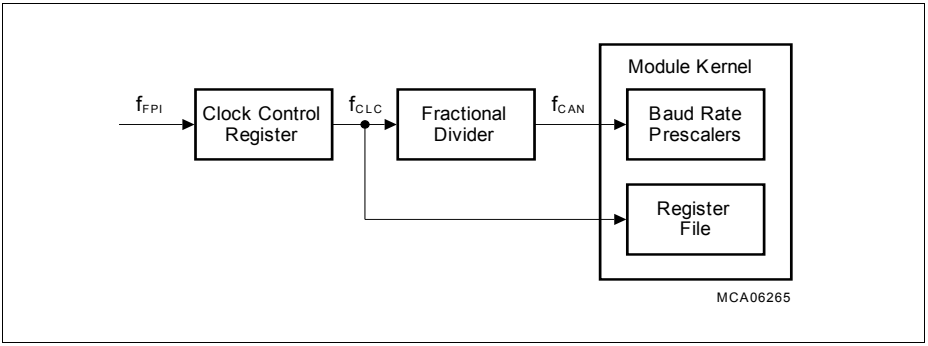


Figure 24-9 MultiCAN Clock Generation

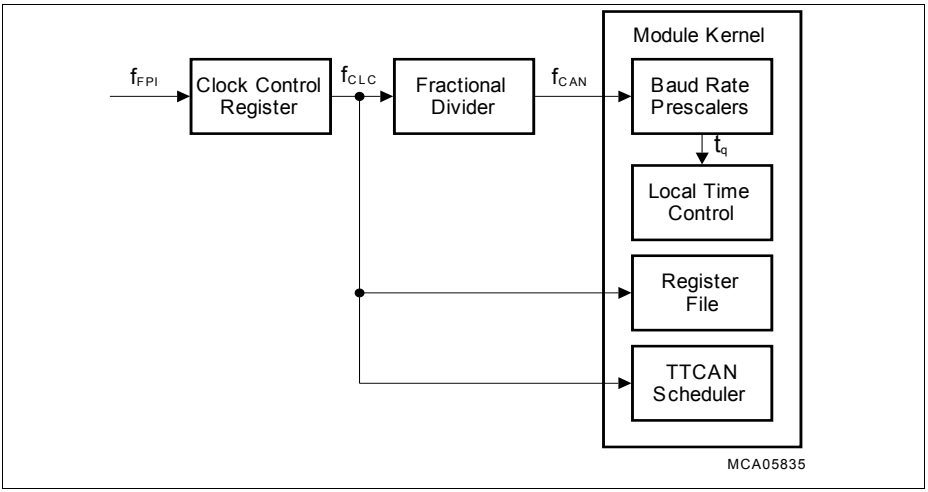


Figure 24-10 MultiCAN with TTCAN Clock Generation

Table 24-2 indicates the minimum operating frequencies in MHz for f_{CLC} that are required for a baud rate of 1 Mbit/s for the active CAN nodes. If a lower baud rate is desired, the values can be scaled linearly (e.g. for a maximum of 500 kbit/s, 50% of the indicated value are required).

The values imply that the CPU (or DMA) executes maximum accesses to the MultiCAN module. The values may contain rounding effects.

Table 24-2 Minimum Operating Frequencies [MHz]

Number of allocated message objects MO[1], with or without TTCAN functionality	1 CAN node active	2 CAN nodes active	3 CAN nodes active	4 CAN nodes active
16 MO, without TTCAN	12	19	26	33
16 MO, with 1 TTCAN	14	21	28	35
32 MO, without TTCAN	15	23	30	37
32 MO, with 1 TTCAN	17	25	32	39
64 MO, without TTCAN	21	28	37	46
64 MO, with 1 TTCAN	23	30	39	48
128 MO, without TTCAN	40	45	50	55
128 MO, with 1 TTCAN	42	47	52	57

1) Only those message objects have to be taken into account that are allocated to a CAN node. The unallocated message objects have no influence on the minimum operating frequency.

The baud rate generation of the MultiCAN being based on f_{FPI}, this frequency has to be chosen carefully to allow correct CAN bit timing. The required value of f_{FPI} is given by an integer multiple (n) of the CAN baud rate multiplied by the number of time quanta per CAN bit time. For example, to reach 1 Mbit/s with 20 tq per bit time, possible values of f_{FPI} are given by formula [n × 20] MHz, with n being an integer value, starting at 1.
In order to minimize jitter, it is not recommended to use the fractional divider mode for high baud rates.

24.5.3 Port Input Control

It is possible to select the input lines for the RXDCANx inputs for the CAN nodes. The selected input is connected to the CAN node and is also available to wake-up the system. More details are defined in **Section 24.11.4.2** on **Page 24-208**.

24.5.4 Suspend Mode

The Suspend Mode can be triggered by the OCDS in order to freeze the state of the module and to permit access to the registers (at least for read actions). The MultiCAN module provides two types of Suspend Modes:

- All actions are immediately stopped (Hard Suspend Mode):
  The module clocks f_{CLC} and f_{CAN} are switched off as soon as the suspend request becomes active. Read and write operations to the module are no longer possible. This means that the CAN registers cannot be accessed anymore. In this mode, there is a very high probability that the communication with other CAN devices is made

impossible, and that the CAN bus is blocked (e.g. if the suspended CAN module just sends a dominant level). A reset operation must be executed to leave Hard Suspend Mode.

- The current action is finished (Soft Suspend Mode):
  The module clock f_{CLC} keeps running. Module functions are stopped automatically after internal actions have been finished (for example, after a CAN frame has been sent out). The end of the internal actions is indicated to the fractional divider by a suspend mode acknowledged signal. Due to this behavior, the communication network is not blocked. Furthermore, all registers are accessible for read and write actions. As a result, the debugger can stop the module actions and modify registers. These modifications are taken into account after the Suspend Mode is left.

The Hard Suspend Mode can be enabled/disabled only for the complete MultiCAN module. The Soft Suspend Mode can be individually enabled for each CAN node.

The fractional divider disables module clock f_{CAN} only if all CAN nodes signal that they can be suspended. A CAN node that is not active can always be suspended.

The user has to be aware that the Soft Suspend Mode can corrupt the TTCAN timing values, because the counter clock can be disabled. In order to guarantee correct TTCAN behavior, a TTCAN node should not enter any Suspend Mode if the consistency of the timing data must be ensured.

24.5.5 CAN Node Control

Each CAN node may be configured and run independently of the other CAN node. Each CAN node is equipped with its own node control logic to configure the global behavior and to provide status information.

Note: In the following descriptions, index “x” stands for the node number and index “n” represents the message object number.

Configuration Mode is activated when bit NCRx.CCE is set to 1. This mode allows CAN bit timing parameters and the error counter registers to be modified.

CAN Analyze Mode is activated when bit NCRx.CALM is set to 1. In this operation mode, Data And Remote Frames are monitored without active participation in any CAN transfer (CAN transmit pin is held on recessive level). Incoming Remote Frames are stored in a corresponding transmit message object, while arriving data frames are saved in a matching receive message object.

In CAN Analyze Mode, the entire configuration information of the received frame is stored in the corresponding message object, and can be evaluated by the CPU to determine their identifier, XTD bit information and data length code (ID and DLC optionally if the Remote Monitoring Mode is active, bit MOFCRn.RMM = 1). Incoming frames are not acknowledged, and no Error Frames are generated. If CAN Analyze Mode is enabled, Remote Frames are not responded to by the corresponding Data Frame, and Data Frames cannot be transmitted by setting the transmit request bit MOSTATn.TXRQ. Receive interrupts are generated in CAN Analyze Mode (if enabled) for all error free received frames.

The node-specific interrupt configuration is also defined by the Node Control Logic via the NCRx register bits TRIE, ALIE and LECIE:

- If control bit TRIE is set to 1, a transfer interrupt is generated when the NSRx register has been updated (after each successfully completed message transfer).
- If control bit ALIE is set to 1, an error interrupt is generated when a “bus-off” condition has been recognized or the Error Warning Level has been exceeded or under-run. Additionally, list or object errors lead to this type of interrupt.
- If control bit LECIE is set to 1, a last error code interrupt is generated when an error code > 0 is written into bit field NSRx.LEC by hardware.

The Node x Status Register NSRx provides an overview about the current state of the respective CAN node x, comprising information about CAN transfers, CAN node status, and error conditions.

The CAN frame counter can be used to check the transfer sequence of message objects or to obtain information about the instant a frame has been transmitted or received from the associated CAN bus. CAN frame counting is performed by a 16-bit counter, controlled by register NFCRx. Bit fields NFCRx.CFMOD and NFCRx.CFSEL determine the operation mode and the trigger event incrementing the frame counter.

24.5.5.1 Bit Timing Unit

According to the ISO 11898 standard, a CAN bit time is subdivided into different segments (**Figure 24-11**). Each segment consists of multiples of a time quantum t_q. The magnitude of t_q is adjusted by Node x Bit Timing Register bit fields NBTRx.BRP and NBTRx.DIV8, both controlling the baud rate prescaler (register NBTRx is described on **Page 24-87**). The baud rate prescaler is driven by the module timer clock f_{CAN} (generation and control of f_{CAN} is described on **Page 24-204**).

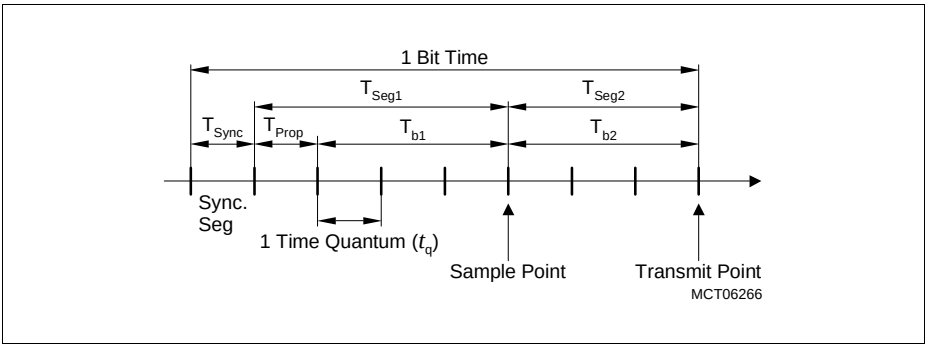


Figure 24-11 CAN Bus Bit Timing Standard

The Synchronization Segment (T_{Sync}) allows a phase synchronization between transmitter and receiver time base. The Synchronization Segment length is always one t_q. The Propagation Time Segment (T_{Prop}) takes into account the physical propagation delay in the transmitter output driver on the CAN bus line and in the transceiver circuit. For a working collision detection mechanism, T_{Prop} must be two times the sum of all propagation delay quantities rounded up to a multiple of t_q. The phase buffer segments 1 and 2 (T_{b1}, T_{b2}) before and after the signal sample point are used to compensate for a mismatch between transmitter and receiver clock phases detected in the synchronization segment.

The maximum number of time quanta allowed for re-synchronization is defined by bit field NBTRx.SJW. The Propagation Time Segment and the Phase Buffer Segment 1 are combined to parameter T_{Seg1}, which is defined by the value NBTRx.TSEG1. A minimum of 3 time quanta is demanded by the ISO standard. Parameter T_{Seg2}, which is defined by the value of NBTRx.TSEG2, covers the Phase Buffer Segment 2. A minimum of 2 time quanta is demanded by the ISO standard. According to ISO standard, a CAN bit time, calculated as the sum of T_{Sync}, T_{Seg1} and T_{Seg2}, must not fall below 8 time quanta.

Calculation of the bit time:

t_q	= (BRP + 1) / f_{CAN}	if DIV8 = 0
	= 8 × (BRP + 1) / f_{CAN}	if DIV8 = 1
T_{Sync}	= 1 × t_q	
T_{Seg1}	= (TSEG1 + 1) × t_q	(min. 3 t_q)
T_{Seg2}	= (TSEG2 + 1) × t_q	(min. 2 t_q)
bit time	= T_{Sync} + T_{Seg1} + T_{Seg2}	(min. 8 t_q)

To compensate phase shifts between clocks of different CAN controllers, the CAN controller must synchronize on any edge from the recessive to the dominant bus level. If the hard synchronization is enabled (at the start of frame), the bit time is restarted at the synchronization segment. Otherwise, the re-synchronization jump width T_{SJW} defines the maximum number of time quanta, a bit time may be shortened or lengthened by one re-synchronization. The value of SJW is defined by bit field NBTRx.SJW.

T_{SJW}	= (SJW + 1) × t_q
T_{Seg1}	≥ T_{SJW} + T_{prop}
T_{Seg2}	≥ T_{SJW}

The maximum relative tolerance for f_{CAN} depends on the Phase Buffer Segments and the re-synchronization jump width.

df_{CAN}	≤ min (T_{b1}, T_{b2}) / 2 × (13 × bit time - T_{b2})	AND
df_{CAN}	≤ T_{SJW} / 20 × bit time	

A valid CAN bit timing must be written to the CAN Node Bit Timing Register NBTR before resetting the INIT bit in the Node Control Register, i.e. before enabling the operation of the CAN node.

The Node Bit Timing Register may be written only if bit CCE (Configuration Change Enable) is set in the corresponding Node Control Register.

24.5.5.2 Bitstream Processor

Based on the message objects in the message buffer, the Bitstream Processor generates the remote and Data Frames to be transmitted via the CAN bus. It controls the CRC generator and adds the checksum information to the new remote or Data Frame. After including the SOF bit and the EOF field, the Bitstream Processor starts the CAN

bus arbitration procedure and continues with the frame transmission when the bus was found in idle state. While the data transmission is running, the Bitstream Processor continuously monitors the I/O line. If (outside the CAN bus arbitration phase or the acknowledge slot) a mismatch is detected between the voltage level on the I/O line and the logic state of the bit currently sent out by the transmit shift register, a CAN error interrupt request is generated, and the error code is indicated by the Node x Status Register bit field NSRx.LEC.

The data consistency of an incoming frame is verified by checking the associated CRC field. When an error has been detected, a CAN error interrupt request is generated and the associated error code is presented in the Node x Status Register NSRx. Furthermore, an Error Frame is generated and transmitted on the CAN bus. After decomposing a faultless frame into identifier and data portion, the received information is transferred to the message buffer executing remote and Data Frame handling, interrupt generation and status processing.

24.5.5.3 Error Handling Unit

The Error Handling Unit of a CAN node x is responsible for the fault confinement of the CAN device. Its two counters, the Receive Error Counter REC and the Transmit Error Counter TEC (bit fields of the Node x Error Counter Register NECNTx, see **Page 24-89**) are incremented and decremented by commands from the Bitstream Processor. If the Bitstream Processor itself detects an error while a transmit operation is running, the Transmit Error Counter is incremented by 8. An increment of 1 is used when the error condition was reported by an external CAN node via an Error Frame generation. For error analysis, the transfer direction of the disturbed message and the node that recognizes the transfer error are indicated for the respective CAN node x in register NECNTx. Depending on the values of the error counters, the CAN node is set into error-active, error-passive, or bus-off state.

The CAN node is in error-active state if both error counters are below the error-passive limit of 128. The CAN node is in error-passive state, if at least one of the error counters is equal to or greater than 128.

The bus-off state is activated if the Transmit Error Counter is equal to or greater than the bus-off limit of 256. This state is reported for CAN node x by the Node x Status Register flag NSRx.BOFF. The device remains in this state, until the “bus-off” recovery sequence is finished. Additionally, Node x Status Register flag NSRx.EWRN is set when at least one of the error counters is equal to or greater than the error warning limit defined by the Node x Error Count Register bit field NECNTx.EWRNLVL. Bit NSRx.EWRN is reset if both error counters fall below the error warning limit again (see **Page 24-77**).

24.5.5.4 CAN Frame Counter

Each CAN node is equipped with a frame counter that counts transmitted/received CAN frames or obtains information about the time when a frame has been started to transmit or be received by the CAN node. CAN frame counting/bit time counting is performed by a 16-bit counter that is controlled by Node x Frame Counter Register NFCRx (see Page 24-90). Bit field NFCRx.CFSEL determines the operation mode of the frame counter:

- **Frame Count Mode:**
  After the successful transmission and/or reception of a CAN frame, the frame counter is copied into the CFCVAL bit field of the MOIPRn register of the message object involved in the transfer. Afterwards, the frame counter is incremented.
- **Time Stamp Mode:**
  The frame counter is incremented with the beginning of a new bit time. When the transmission/reception of a frame starts, the value of the frame counter is captured and stored to the CFC bit field of the NFCRx register. After the successful transfer of the frame the captured value is copied to the CFCVAL bit field of the MOIPRn register of the message object involved in the transfer.
- **Bit Timing Mode:**
  Used for baud rate detection and analysis of the bit timing (Chapter 24.5.7.3).

24.5.5.5 CAN Node Interrupts

Each CAN node has four hardware triggered interrupt request types that are able to generate an interrupt request upon:

- The successful transmission or reception of a frame
- A CAN protocol error with a last error code
- An alert condition: Transmit/receive error counters reach the warning limit, bus-off state changes, a List Length Error occurs, or a List Object Error occurs
- An overflow of the frame counter

Besides the hardware generated interrupts, software initiated interrupts can be generated using the Module Interrupt Trigger Register MITR. Writing a 1 to bit n of bit field MITR.IT generates an interrupt request signal on the corresponding interrupt output line INT_On. When writing MITR.IT more than one bit can be set resulting in activation of multiple INT_On interrupt output lines at the same time. See also **“Interrupt Control” on Page 24-211** for further processing of the CAN node interrupts.

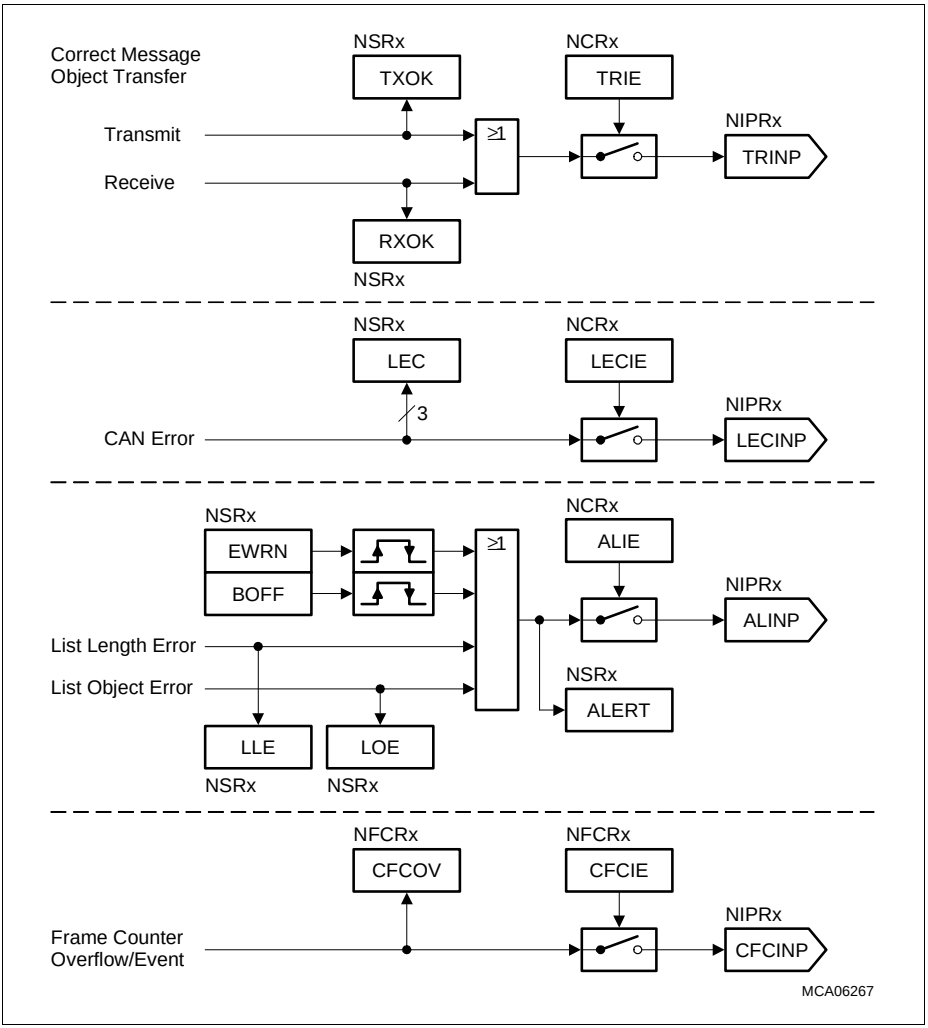


Figure 24-12 CAN Node Interrupts

24.5.6 Message Object List Structure

This section describes the structure of the message object lists in the MultiCAN module.

24.5.6.1 Basics

The message objects of the MultiCAN module are organized in double-chained lists, where each message object has a pointer to the previous message object in the list as well as a pointer to the next message object in the list. The MultiCAN module provides eight lists. Each message object is allocated to one of these lists. In the example in **Figure 24-13**, the three message objects (3, 5, and 16) are allocated to the list with index 2 (List Register LIST2).

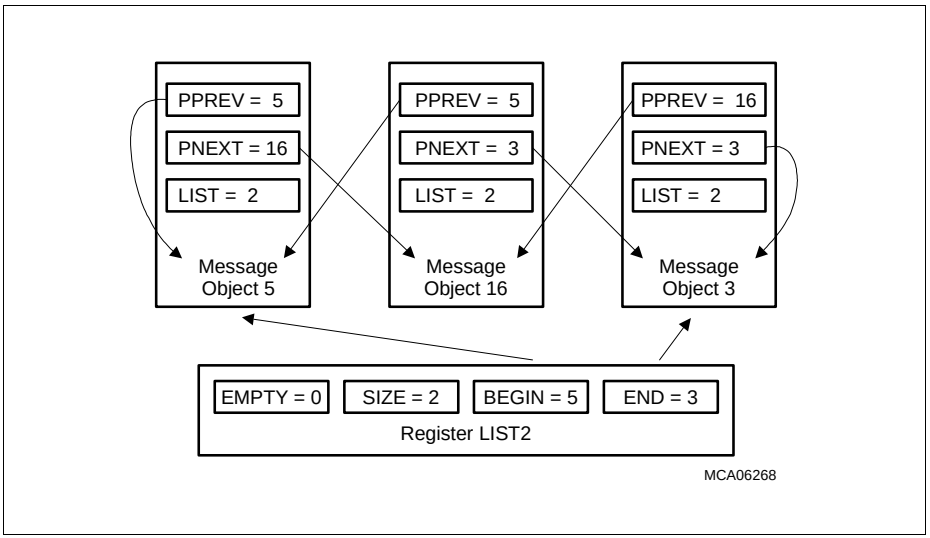


Figure 24-13 Example Allocation of Message Objects to a List

Bit field BEGIN in the List Register (for definition, see **Page 24-71**) points to the first element in the list (object 5 in the example), and bit field END points to the last element in the list (object 3 in the example). The number of elements in the list is indicated by bit field SIZE of the List Register (SIZE = number of list elements - 1, thus SIZE = 2 for the 3 elements in the example). The EMPTY bit of the List Register indicates whether or not a list is empty (EMPTY = 0 in the example, because list 2 is not empty).

Each message object n has a pointer PNEXT in its Message Object n Control Register MOCTRn (see **Page 24-94**) that points to the next message object in the list, and a pointer PPREV that points to the previous message object in the list. PPREV of the first message object points to the message object itself because the first message object has no predecessor (in the example message object 5 is the first message object in the list,

indicated by PPREV = 5). PNEXT of the last message object also points to the message object itself because the last message object has no successor (in the example, object 3 is the last message object in the list, indicated by PNEXT = 3).

Bit field MOCTRn.LIST indicates the list index number to which the message object is currently allocated. The message object of the example are allocated to list 2. Therefore, all LIST bit fields for the message objects assigned to list 2 are set to LIST = 2.

24.5.6.2 List of Unallocated Elements

The list with list index 0 has a special meaning: it is the list of all unallocated elements. An element is called unallocated if it belongs to list 0 (MOCTRn.LIST = 0). It is called allocated if it belongs to a list with an index not equal to 0 (MOCTRn.LIST > 0).

After reset, all message objects are unallocated. This means that they are assigned to the list of unallocated elements with MOCTRn.LIST = 0. After this initial allocation of the message objects caused by reset, the list of all unallocated message objects is ordered by message number (predecessor of message object n is object n-1, successor of object n is object n+1).

24.5.6.3 Connection to the CAN Nodes

Each CAN node is linked to one unique list of message objects. A CAN node performs message transfer only with the message objects that are allocated to the list of the CAN node. This is illustrated in **Figure 24-14**. Frames that are received on a CAN node may only be stored in one of the message objects that belongs to the CAN node; frames to be transmitted on a CAN node are selected only from the message objects that are allocated to that node, as indicated by the vertical arrows.

There are more lists (eight) than CAN nodes (two). This means that some lists are not linked to one of the CAN nodes. A message object that is allocated to one of these unlinked lists cannot receive messages directly from a CAN node and it may not transmit messages.

FIFO and gateway mechanisms refer to message numbers and not directly to a specific list. The user must take care that the message objects targeted by FIFO/gateway belong to the desired list. The mechanisms make it possible to work with lists that do not belong to the CAN node.

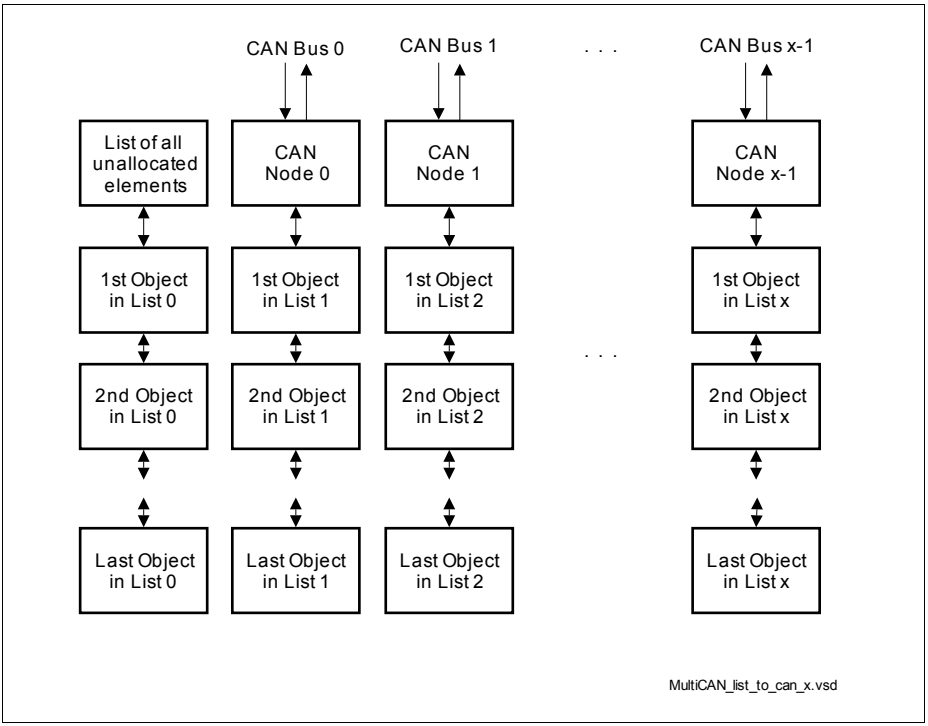


Figure 24-14 Message Objects Linked to CAN Nodes

24.5.6.4 List Command Panel

The list structure cannot be modified directly by write accesses to the LIST registers and the PPREV, PNEXT and LIST bit fields in the Message Object Control Registers, as they are read only. The list structure is managed by and limited to the list controller inside the MultiCAN module. The list controller is controlled via a command panel allowing the user to issue list allocation commands to the list controller. The list controller has two main purposes:

1. Ensure that all operations that modify the list structure result in a consistent list structure.
2. Present maximum ease of use and flexibility to the user.

The list controller and the associated command panel allows the programmer to concentrate on the final properties of the list, which are characterized by the allocation of message objects to a CAN node, and the ordering relation between objects that are allocated to the same list. The process of list (re-)building is done in the list controller.

Table 24-3 gives an overview on the available panel commands while Table 24-7 on Page 24-66 describes the panel commands in more detail.

Table 24-3 Panel Commands Overview

Command Name	Description
No Operation	No new command is started.
Initialize Lists	Run the initialization sequence to reset the CTRL and LIST field of all message objects.
Static Allocate	Allocate message object to a list.
Dynamic Allocate	Allocate the first message object of the list of unallocated objects to the selected list.
Static Insert Before	Remove a message object (source object) from the list that it currently belongs to, and insert it before a given destination object into the list structure of the destination object.
Dynamic Insert Before	Insert a new message object before a given destination object.
Static Insert Behind	Remove a message object (source object) from the list that it currently belongs to, and insert it behind a given destination object into the list structure of the destination object.
Dynamic Insert Behind	Insert a new message object behind a given destination object.

A panel command is started by writing the respective command code into the Panel Control Register bit field PANCTR.PANCMD (see Page 24-65). The corresponding command arguments must be written into bit fields PANCTR.PANAR1 and PANCTR.PANAR2 before writing the command code, or latest along with the command code in a single 32-bit write access to the Panel Control Register.

With the write operation of a valid command code, the PANCTR.BUSY flag is set and further write accesses to the Panel Control Register are ignored. The BUSY flag remains active and the control panel remains locked until the execution of the requested command has been completed. After a reset, the list controller builds up list 0. During this operation, BUSY is set and other accesses to the CAN RAM are forbidden. The CAN RAM can be accessed again when BUSY becomes inactive.

Note: The CAN RAM is automatically initialized after reset by the list controller in order to ensure correct list pointers in each message object. The end of this CAN RAM initialization is indicated by bit PANCTR.BUSY becoming inactive.

In case of a dynamic allocation command that takes an element from the list of unallocated objects, the PANCTR.RBUSY bit is also set along with the BUSY bit

(RBUSY = BUSY = 1). This indicates that bit fields PANAR1 and PANAR2 are going to be updated by the list controller in the following way:

1. The message number of the message object taken from the list of unallocated elements is written to PANAR1.
2. If ERR (bit 7 of PANAR2) is set to 1, the list of unallocated elements was empty and the command is aborted. If ERR is 0, the list was not empty and the command will be performed successfully.

The results of a dynamic allocation command are written before the list controller starts the actual allocation process. As soon as the results are available, RBUSY becomes inactive (RBUSY = 0) again, while BUSY still remains active until completion of the command. This allows the user to set up the new message object while it is still in the process of list allocation. The access to message objects is not limited during ongoing list operations. However, any access to a register resource located inside the RAM delays the ongoing allocation process by one access cycle.

As soon as the command is finished, the BUSY flag becomes inactive (BUSY = 0) and write accesses to the Panel Control Register are enabled again. Also, the “No Operation” command code is automatically written to the PANCTR.PANCMD field. A new command may be started any time when BUSY = 0.

All fields of the Panel Control Register PANCTR except BUSY and RBUSY may be written by the user. This makes it possible to save and restore the Panel Control Register if the Command Panel is used within independent (mutually interruptible) interrupt service routines. If this is the case, any task that uses the Command Panel and that may interrupt another task that also uses the Command Panel should poll the BUSY flag until it becomes inactive and save the whole PANCTR register to a memory location before issuing a command. At the end of the interrupt service routine, the task should restore PANCTR from the memory location.

Before a message object that is allocated to the list of an active CAN node shall be moved to another list or to another position within the same list, bit MOCTRn.MSGVAL (“Message Valid”) of message object n must be cleared.

24.5.7 CAN Node Analysis Features

The chapter describes the CAN node analysis capabilities of the MultiCAN module.

24.5.7.1 Analyze Mode

The CAN Analyze Mode makes it possible to monitor the CAN traffic for each CAN node individually without affecting the logical state of the CAN bus. The CAN Analyze Mode for CAN node x is selected by setting Node x Control Register bit NCRx.CALM.

In CAN Analyze Mode, the transmit pin of a CAN node is held at a recessive level permanently. The CAN node may receive frames (Data, Remote, and Error Frames) but is not allowed to transmit. Received Data/Remote Frames are not acknowledged (i.e. acknowledge slot is sent recessive) but will be received and stored in matching message objects as long as there is any other node that acknowledges the frame. The complete message object functionality is available, but no transmit request will be executed.

24.5.7.2 Loop-Back Mode

The MultiCAN module provides a Loop-Back Mode to enable an in-system test of the MultiCAN module as well as the development of CAN driver software without access to an external CAN bus.

The loop-back feature consists of an internal CAN bus (inside the MultiCAN module) and a bus select switch for each CAN node (see **Figure 24-15**). With the switch, each CAN node can be connected either to the internal CAN bus (Loop-Back Mode activated) or the external CAN bus, respectively to transmit and receive pins (normal operation). The CAN bus that is not currently selected is driven recessive; this means the transmit pin is held at 1, and the receive pin is ignored by the CAN nodes that are in Loop-Back Mode.

The Loop-Back Mode is selected for CAN node x by setting the Node x Port Control Register bit NPCRx.LBM. All CAN nodes that are in Loop-Back Mode may communicate together via the internal CAN bus without affecting the normal operation of the other CAN nodes that are not in Loop-Back Mode.

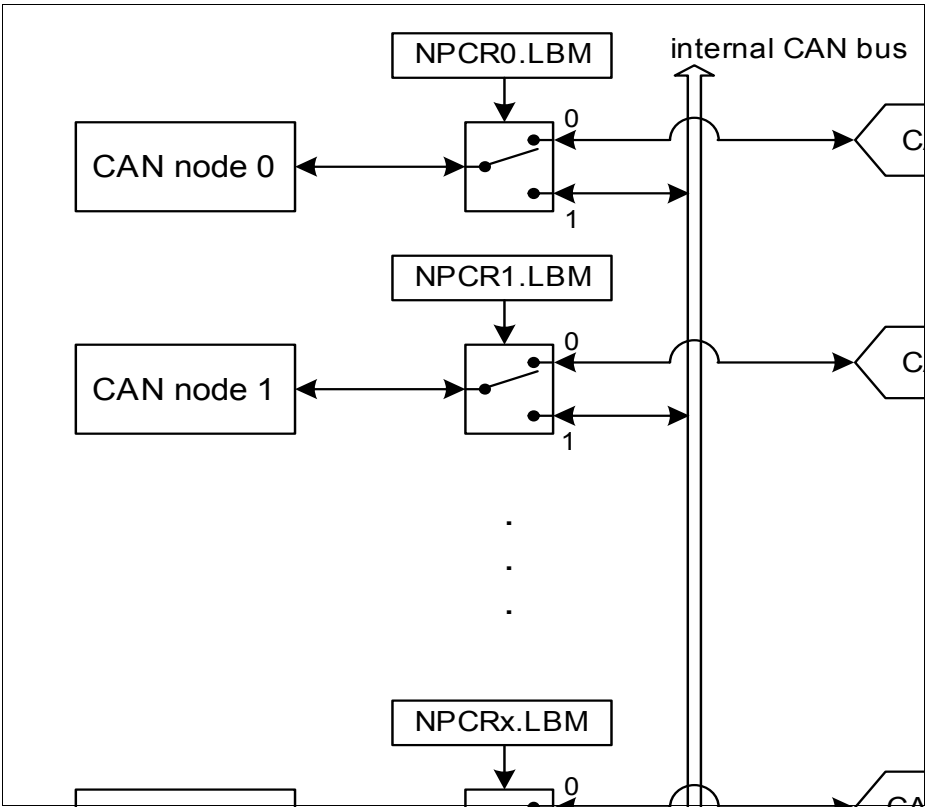


Figure 24-15 Loop-Back Mode

24.5.7.3 Bit Timing Analysis

Detailed analysis of the bit timing can be performed for each CAN node using the analysis modes of the CAN frame counter. The bit timing analysis functionality of the frame counter may be used for automatic detection of the CAN baud rate, as well as to analyze the timing of the CAN network.

Bit timing analysis for CAN node x is selected when bit field NFCRx.CFMOD = 10_B. Bit timing analysis does not affect the operation of the CAN node.

The bit timing measurement results are written into the NFCRx.CFC bit field. Whenever NFCRx.CFC is updated in bit timing analysis mode, bit NFCRx.CFCOV is also set to indicate the CFC update event. If NFCRx.CFCIE is set, an interrupt request can be generated (see **Figure 24-12**).

Automatic Baud Rate Detection

For automatic baud rate detection, the time between the observation of subsequent dominant edges on the CAN bus must be measured. This measurement is automatically performed if bit field NFCRx.CFSEL = 000_B. With each dominant edge monitored on the CAN receive input line, the time (measured in f_{CAN} clock cycles) between this edge and the most recent dominant edge is stored in the NFCRx.CFC bit field.

Synchronization Analysis

The bit time synchronization is monitored if NFCRx.CFSEL = 010_B. The time between the first dominant edge and the sample point is measured and stored in the NFCRx.CFC bit field. The bit timing synchronization offset may be derived from this time as the first edge after the sample point triggers synchronization and there is only one synchronization between consecutive sample points.

Synchronization analysis can be used, for example, for fine tuning of the baud rate during reception of the first CAN frame with the measured baud rate.

Driver Delay Measurement

The delay between a transmitted edge and the corresponding received edge is measured when NFCRx.CFSEL = 011_B (dominant to dominant) and NFCRx.CFSEL = 100_B (recessive to recessive). These delays indicate the time needed to represent a new bit value on the physical implementation of the CAN bus.

24.5.8 Message Acceptance Filtering

The chapter describes the Message Acceptance Filtering capabilities of the MultiCAN module.

24.5.8.1 Receive Acceptance Filtering

When a CAN frame is received by a CAN node, a unique message object is determined in which the received frame is stored after successful frame reception. A message object is qualified for reception of a frame if the following six conditions are met.

- The message object is allocated to the message object list of the CAN node by which the frame is received.
- Bit MOSTATn.MSGVAL in the Message Status Register (see **Page 24-97**) is set.
- Bit MOSTATn.RXEN is set.
- Bit MOSTATn.DIR is equal to bit RTR of the received frame.
  If bit MOSTATn.DIR = 1 (transmit object), the message object accepts only Remote Frames. If bit MOSTATn.DIR = 0 (receive object), the message object accepts only Data Frames.
- If bit MOAMRn.MIDE = 1, the IDE bit of the received frame becomes evaluated in the following way: If MOARn.IDE = 1, the IDE bit of the received frame must be set (indicates extended identifier). If MOARn.IDE = 0, the IDE bit of the received frame must be cleared (indicates standard identifier).
  If bit MOAMRn.MIDE = 0, the IDE bit of the received frame is “don’t care”. In this case, message objects with standard and extended frames are accepted.
- The identifier of the received frame matches the identifier stored in the Arbitration Register of the message object as qualified by the acceptance mask in the MOAMRn register. This means that each bit of the received message object identifier is equal to the bit field MOARn.ID, except those bits for which the corresponding acceptance mask bits in bit field MOAMRn.AM are cleared. These identifier bits are “don’t care” for reception. **Figure 24-16** illustrates this receive message identifier check.

Among all messages that fulfill all six qualifying criteria the message object with the highest receive priority wins receive acceptance filtering and becomes selected to store the received frame. All other message objects lose receive acceptance filtering.

The following priority scheme is defined for the message objects:

A message object a (MOa) has higher receive priority than a message object b (MOb) if the following two conditions are fulfilled (see **Page 24-113**):

1. MOa has a higher priority class than MOb. This means, the 2-bit priority bit field MOARa.PRI must be equal or less than bit field MOARb.PRI.
2. If both message objects have the same priority class (MOARa.PRI = MOARb.PRI), MOb is a list successor of MOa. This means that MOb can be reached by means of successively stepping forward in the list, starting from a.

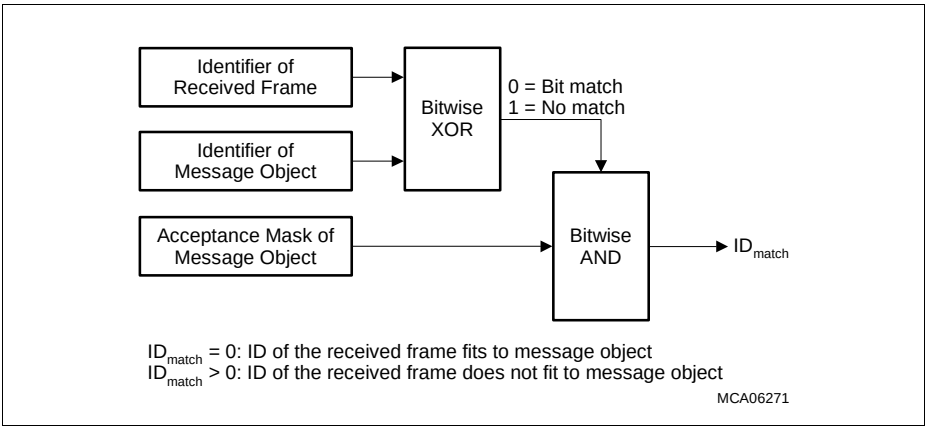


Figure 24-16 Received Message Identifier Acceptance Check

24.5.8.2 Transmit Acceptance Filtering

A message is requested for transmission by setting a transmit request in the message object that holds the message. If more than one message object have a valid transmit request for the same CAN node, one of these message objects is chosen for transmission, because only a single message object can be transmitted at one time on a CAN bus.

A message object is qualified for transmission on a CAN node if the following four conditions are met (see also **Figure 24-17**).

1. The message object is allocated to the message object list of the CAN node.
2. Bit MOSTATn.MSGVAL is set.
3. Bit MOSTATn.TXRQ is set.
4. Bit MOSTATn.TXEN0 and MOSTATn.TXEN1 are set.

A priority scheme determines which one of all qualifying message objects is transmitted first. It is assumed that message object a (MOa) and message object b (MOb) are two message objects qualified for transmission. MOb is a list successor of MOa. For both message objects, CAN messages CANa and CANb are defined (identifier, IDE, and RTR are taken from the message-specific bit fields and bits MOARn.ID, MOARn.IDE and MOCTRn.DIR).

If both message objects belong to the same priority class (identical PRI bit field in register MOARn), MOa has a higher transmit priority than MOb if one of the following conditions is fulfilled.

- PRI = 10_B and CAN message MOa has higher or equal priority than CAN message MOb with respect to CAN arbitration rules (see **Table 24-13** on **Page 24-114**).
- PRI = 01_B or PRI = 11_B (priority by list order).

- PRI = 00_B and the actual matrix position in a TTCAN network matches the matrix position(s) given in MOAMRn of MOa, i.e.
  CYCLE & MCYCLE = CYCTMR.BCC & MCYCLE and
  COLUMN & MCOLUMN = CYCTMR.CSM & MCOLUMN
  A message object with PRI = 00_B can be transmitted only by an active TTCAN node.

The message object that is qualified for transmission and has highest transmit priority wins the transmit acceptance filtering, and will be transmitted first. All other message objects lose the current transmit acceptance filtering round. They get a new chance in subsequent acceptance filtering rounds.

The three priority rules listed before are valid for normal CAN operation (without TTCAN functionality) as well as for arbitration windows within a TTCAN system matrix.

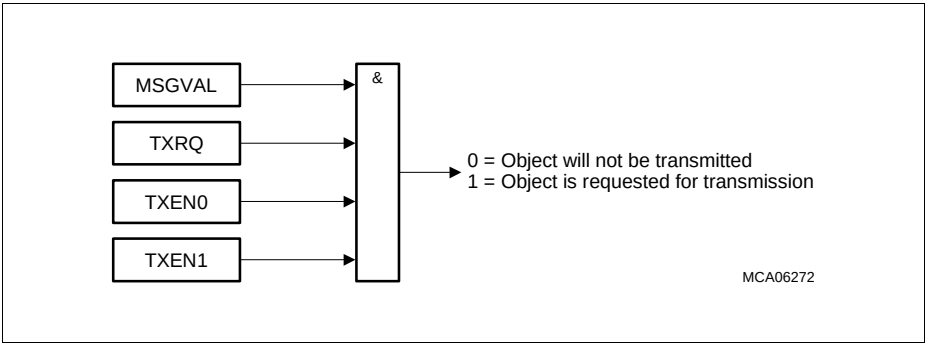


Figure 24-17 Effective Transmit Request of Message Object

Transmission Acceptance Filtering in TTCAN Exclusive Windows

In exclusive windows of a TTCAN, transmit acceptance filtering is performed as described in the previous section but with the exception that only message objects with MOARn.PRI = 00_B can be transmitted. Message objects with other PRI values are not taken into account. Hence the transmit acceptance filtering process selects the first message object in the list that meets the following conditions:

1. MOARn.PRI = 00_B
   a) MSGVAL & TXRQ & TXEN0 & TXEN1 = 1 (i.e. the message object qualifies for transmission)
   b) The actual matrix position in a TTCAN network matches the matrix position(s) given in MOAMR of MOa, i.e.
   CYCLE & MCYCLE = CYCTMR.BCC & MCYCLE and
   COLUMN & MCOLUMN = CYCTMR.CSM & MCOLUMN

24.5.9 Message Postprocessing

After a message object has successfully received or transmitted a frame, the CPU can be notified to perform a postprocessing on the message object. The postprocessing of the MultiCAN module consists of two elements:

1. Message interrupts to trigger postprocessing.
2. Message pending registers to collect pending message interrupts into a common structure for postprocessing.

24.5.9.1 Message Object Interrupts

When the storage of a received frame into a message object or the successful transmission of a frame is completed, a message interrupt can be issued. For each message object, a transmit and a receive interrupt can be generated and routed to one of the sixteen CAN interrupt output lines (see **Figure 24-18**). A receive interrupt occurs also after a frame storage event that has been induced by a FIFO or a gateway action. The status bits TXPND and RXPND in the Message Object n Status Register are always set after a successful transmission/reception, whether or not the respective message interrupt is enabled.

A third FIFO full interrupt condition of a message object is provided. If bit field MOFCRn.OVIE (Overflow Interrupt Enable) is set, the FIFO full interrupt will be activated depending on the actual message object type.

In case of a Receive FIFO Base Object (MOFCRn.MMC = 0001_B), the FIFO full interrupt is routed to the interrupt output line INT_Om as defined by the transmit interrupt node pointer MOIPRn.TXINP.

In case of a Transmit FIFO Base Object (MOFCRn.MMC = 0010_B), the FIFO full interrupt becomes routed to the interrupt output line INT_Om as defined by the receive interrupt node pointer MOIPRn.RXINP.

See also **“Interrupt Control” on Page 24-211** for further processing of the message object interrupts.

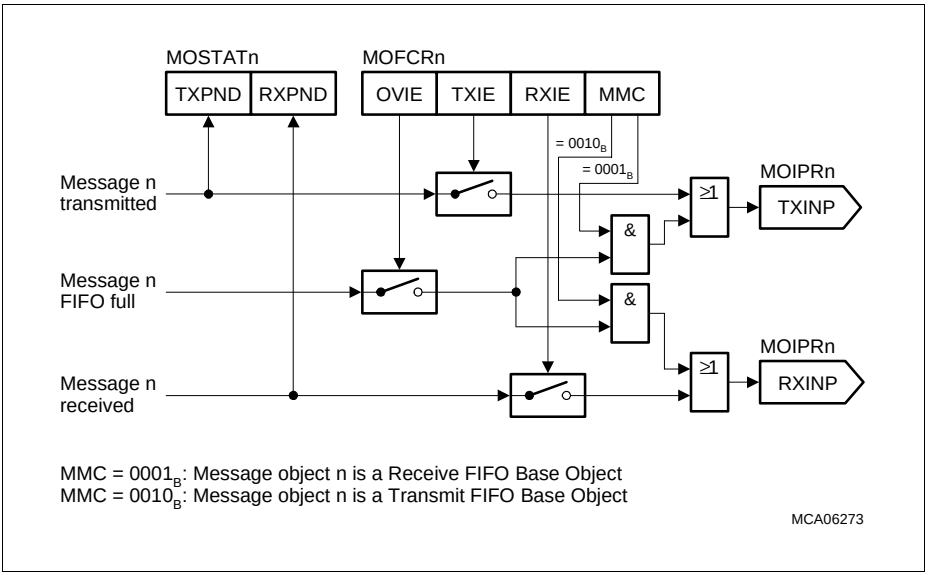


Figure 24-18 Message Interrupt Request Routing

24.5.9.2 Pending Messages

When a message interrupt request is generated, a message pending bit is set in one of the Message Pending Registers. There are 8 Message Pending Registers, MSPNDk (k = 0-7) with 32 pending bits available each. The general **Figure 24-19** shows the allocation of the message pending bits in case that the maximum possible number of eight Message Pending Registers are implemented and available on the chip.

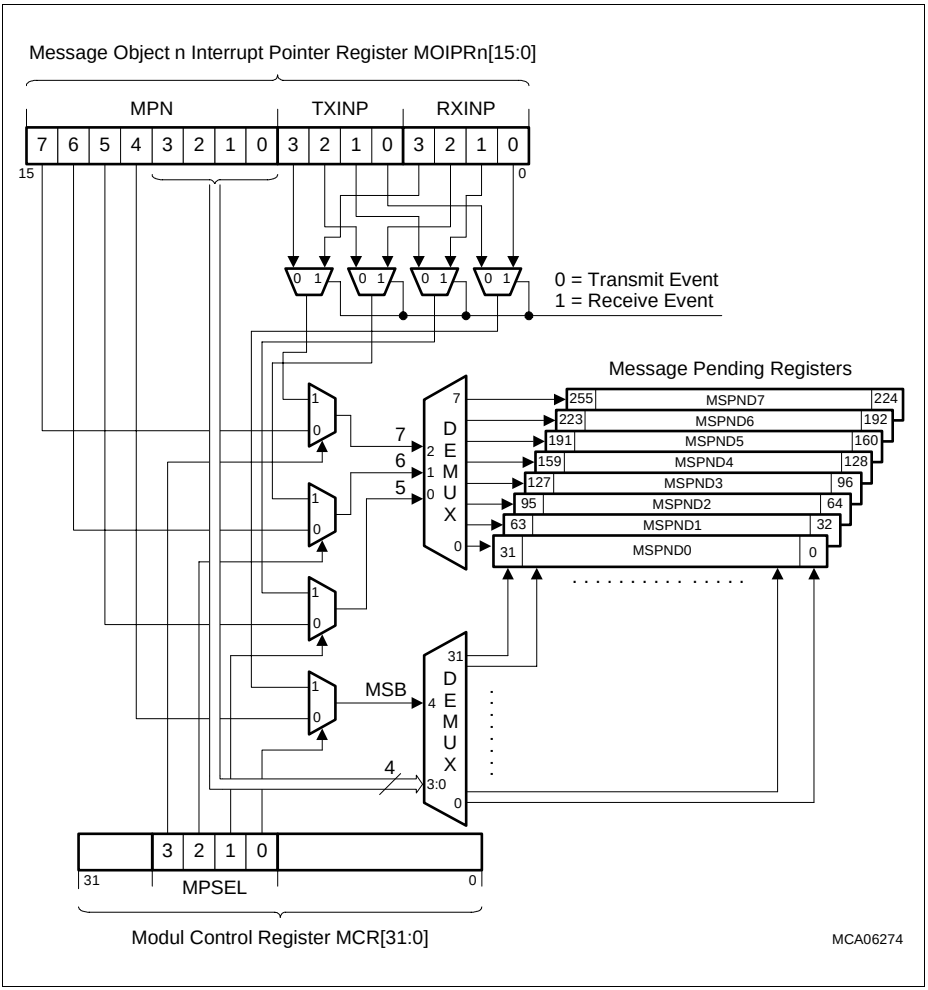


Figure 24-19 Message Pending Bit Allocation

The location of a pending bit is defined by two demultiplexers selecting the number k of the MSPNDk registers (3-bit demux), and the bit location within the corresponding MSPNDk register (5-bit demux).

Allocation Case 1

In this allocation case, bit field MCR.MPSEL = 0000_B (see **Page 24-69**). The location selection consists of 2 parts:

- The upper three bits of MOIPRn.MPN (MPN[7:5]) select the number k of a Message Pending Register MSPNDk in which the pending bit will be set.
- The lower five bits of MOIPRn.MPN (MPN[4:0]) select the bit position (0-31) in MSPNDk for the pending bit to be set.

Allocation Case 2

In this allocation case, bit field MCR.MPSEL is taken into account for pending bit allocation. Bit field MCR.MPSEL makes it possible to include the interrupt request node pointer for reception (MOIPRn.RXINP) or transmission (MOIPRn.TXINP) for pending bit allocation in such a way that different target locations for the pending bits are used in receive and transmit case. If MPSEL = 1111_B, the location selection operates in the following way:

- At a transmit event, the upper 3 bits of TXINP determine the number k of a Message Pending Register MSPNDk in which the pending bit will be set. At a receive event, the upper 3 bits of RXINP determine the number k.
- The bit position (0-31) in MSPNDk for the pending bit to be set is selected by the lowest bit of TXINP or RXINP (selects between low and high half-word of MSPNDk) and the four least significant bits of MPN.

General Hints

The Message Pending Registers MSPNDk can be written by software. Bits that are written with 1 are left unchanged, and bits which are written with 0 are cleared. This makes it possible to clear individual MSPNDk bits with a single register write access. Therefore, access conflicts are avoided when the MultiCAN module (hardware) sets another pending bit at the same time when software writes to the register.

Each Message Pending Register MSPNDk is associated with a Message Index Register MSIDk (see **Page 24-74**) which indicates the lowest bit position of all set (1) bits in Message Pending Register k. The MSIDk register is a read-only register that is updated immediately when a value in the corresponding Message Pending Register k is changed by software or hardware.

24.5.10 Message Object Data Handling

This chapter describes the handling capabilities for the Message Object Data of the MultiCAN module.

24.5.10.1 Frame Reception

After the reception of a message, it is stored in a message object according to the scheme shown in **Figure 24-20**. The MultiCAN module not only copies the received data into the message object, and it provides advanced features to enable consistent data exchange between MultiCAN and CPU.

MSGVAL

Bit MSGVAL (Message Valid) in the Message Object n Status Register MOSTATn is the main switch of the message object. During the frame reception, information is stored in the message object only when MSGVAL = 1. If bit MSGVAL is reset by the CPU, the MultiCAN module stops all ongoing write accesses to the message object. Now the message object can be re-configured by the CPU with subsequent write accesses to it without being disturbed by the MultiCAN.

RTSEL

When the CPU re-configures a message object during CAN operation (for example, clears MSGVAL, modifies the message object and sets MSGVAL again), the following scenario can occur:

1. The message object wins receive acceptance filtering.
2. The CPU clears MSGVAL to re-configure the message object.
3. The CPU sets MSGVAL again after re-configuration.
4. The end of the received frame is reached. As MSGVAL is set, the received data is stored in the message object, a message interrupt request is generated, gateway and FIFO actions are processed, etc.

After the re-configuration of the message object (after step 3 above) the storage of further received data may be undesirable. This can be achieved through bit MOCTRn.RTSEL (Receive/Transmit Selected) that makes it possible to disconnect a message object from an ongoing frame reception.

When a message object wins the receive acceptance filtering, its RTSEL bit is set by the MultiCAN module to indicate an upcoming frame delivery. The MultiCAN module checks RTSEL whether it is set on successful frame reception to verify that the object is still ready for receiving the frame. The received frame is then stored in the message object (along with all subsequent actions such as message interrupts, FIFO & gateway actions, flag updates) only if RTSEL = 1.

When a message object is invalidated during CAN operation (resetting bit MSGVAL), RTSEL should be cleared before setting MSGVAL again (latest with the same write

access that sets MSGVAL) to prevent the storage of a frame that belongs to the old context of the message object. Therefore, a message object re-configuration should consist of the following steps:

1. Clear MSGVAL bit
2. Re-configure the message object while MSGVAL = 0
3. Clear RTSEL bit and set MSGVAL again

RXEN

Bit MOSTATn.RXEN enables a message object for frame reception. A message object can receive CAN messages from the CAN bus only if RXEN = 1. The MultiCAN module evaluates RXEN only during receive acceptance filtering. After receive acceptance filtering, RXEN is ignored and has no further influence on the actual storage of a received message in a message object.

Bit RXEN enables the “soft phase out” of a message object: after clearing RXEN, a currently received CAN message for which the message object has won acceptance filtering is still stored in the message object but for subsequent messages the message object no longer wins receive acceptance filtering.

RXUPD, NEWDAT and MSGLST

An ongoing frame storage process is indicated by the RXUPD (Receive Updating) flag in the MOSTATn register. RXUPD is set with the start and cleared with the end of a message object update, which consists of frame storage as well as flag updates.

After storing the received frame (identifier, IDE bit, DLC; including the Data Field for Data Frames), the NEWDAT (New Data) bit of the message object is set. If NEWDAT was already set before it becomes set again, bit MSGLST (Message Lost) is set to indicate a data loss condition.

The RXUPD and NEWDAT flags can help to read consistent frame data from the message object during an ongoing CAN operation. The following steps are recommended to be executed:

1. Clear NEWDAT bit.
2. Read message content (identifier, data etc.) from the message object.
3. Check that both, NEWDAT and RXUPD, are cleared. If this is not the case, go back to step 1.
4. When step 3 was successful, the message object contents are consistent and has not been updated by the MultiCAN module while reading.

Bits RXUPD, NEWDAT and MSGLST have the same behavior for the reception of Data as well as Remote Frames.

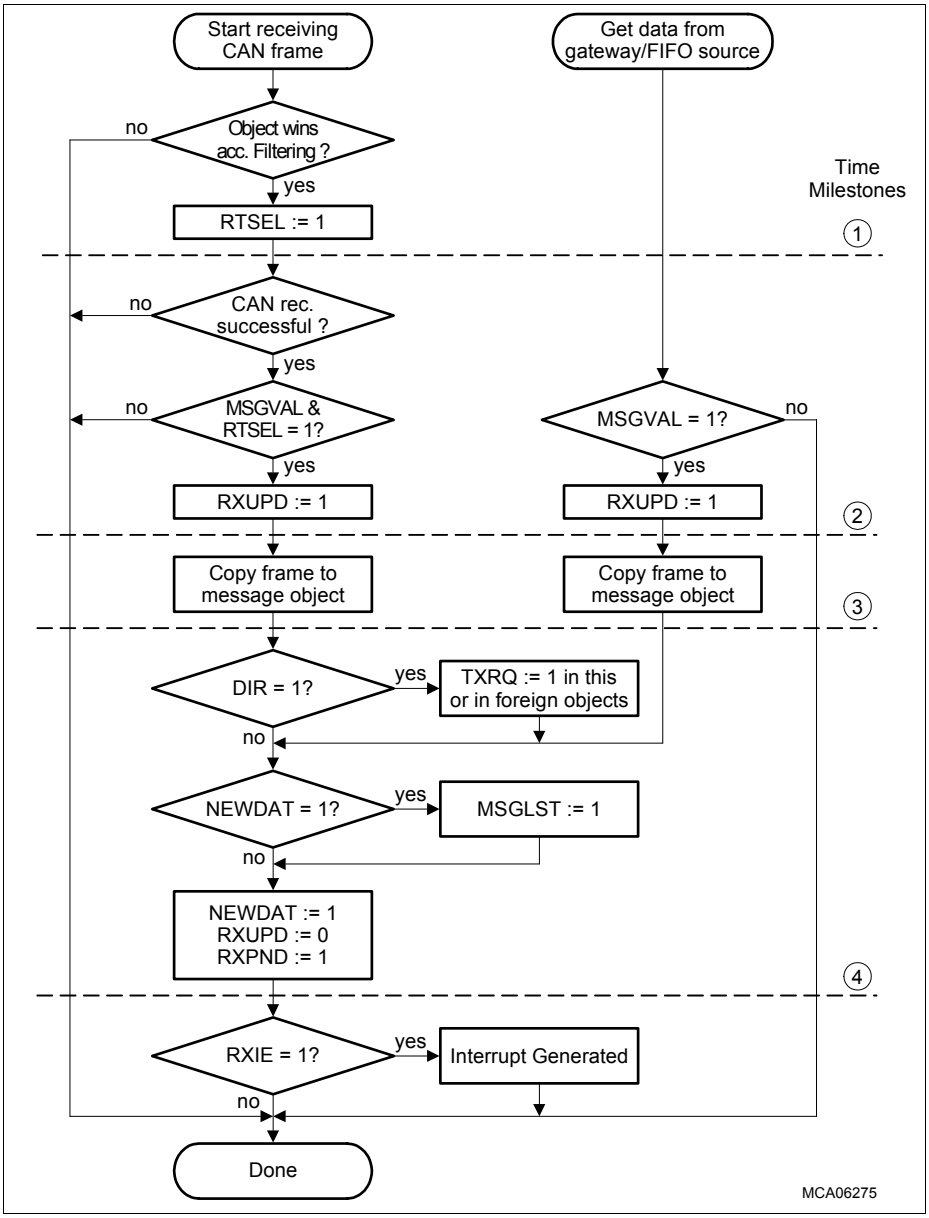


Figure 24-20 Reception of a Message Object

24.5.10.2 Frame Transmission

The process of a message object transmission is shown in **Figure 24-21**. Along with the copy of the message object content to be transmitted (identifier, IDE bit, RTR = DIR bit, DLC, including the Data Field for Data Frames) into the internal transmit buffer of the assigned CAN node, several status flags are also served and monitored to control consistent data handling.

The transmission process of a message object starting after the transmit acceptance filtering is identical for Remote and Data Frames.

MSGVAL, TXRQ, TXEN0, TXEN1

A message can only be transmitted if all four bits in registers MOSTATn, MSGVAL (Message Valid), TXRQ (Transmit Request), TXEN0 (Transmit Enable 0), TXEN1 (Transmit Enable 1) are set as shown in **Figure 24-17**. Although these bits are equivalent with respect to the transmission process, they have different semantics:

Table 24-4 Message Transmission Bit Definitions

Bit	Description
MSGVAL	**Message Valid** This is the main switch bit of the message object.
TXRQ	**Transmit Request** This is the standard transmit request bit. This bit must be set whenever a message object should be transmitted. TXRQ is cleared by hardware at the end of a successful transmission, except when there is new data (indicated by NEWDAT = 1) to be transmitted. When bit MOFCRn.STT (“Single Transmit Trial”) is set, TXRQ becomes already cleared when the contents of the message object are copied into the transmit frame buffer of the CAN node. A received remote request (after a Remote Frame reception) sets bit TXRQ to request the transmission of the requested data frame.
TXEN0	**Transmit Enable 0** This bit can be temporarily cleared by software to suppress the transmission of this message object when it writes new content to the Data Field. This avoids transmission of inconsistent frames that consist of a mixture of old and new data. Remote requests are still accepted when TXEN0 = 0, but transmission of the Data Frame is suspended until transmission is re-enabled by software (setting TXEN0).

Table 24-4 Message Transmission Bit Definitions (cont'd)

Bit	Description
TXEN1	**Transmit Enable 1** This bit is used in transmit FIFOs to select the message object that is transmit active within the FIFO structure. For message objects that are not transmit FIFO elements, TXEN1 can either be set permanently to 1 or can be used as a second independent transmission enable bit.

RTSEL

When a message object has been identified to be transmitted next after transmission acceptance filtering, bit MOCTRn.RTSEL (Receive/Transmit Selected) is set.

When the message object is copied into the internal transmit buffer, bit RTSEL is checked, and the message is transmitted only if RTSEL = 1. After the successful transmission of the message, bit RTSEL is checked again and the message postprocessing is only executed if RTSEL = 1.

For a complete re-configuration of a valid message object, the following steps should be executed:

1. Clear MSGVAL bit
2. Re-configure the message object while MSGVAL = 0
3. Clear RTSEL and set MSGVAL

Clearing of RTSEL ensures that the message object is disconnected from an ongoing/scheduled transmission and no message object processing (copying message to transmit buffer including clearing NEWDAT, clearing TXRQ, time stamp update, message interrupt, etc.) within the old context of the object can occur after the message object becomes valid again, but within a new context.

NEWDAT

When the contents of a message object have been transferred to the internal transmit buffer of the CAN node, bit MOSTATn.NEWDAT (New Data) is cleared by hardware to indicate that the transmit message object data is no longer new.

When the transmission of the frame is successful and NEWDAT is still cleared (if no new data has been copied into the message object meanwhile), TXRQ (Transmit Request) is cleared automatically by hardware.

If, however, the NEWDAT bit has been set again by the software (because a new frame should be transmitted), TXRQ is not cleared to enable the transmission of the new data.

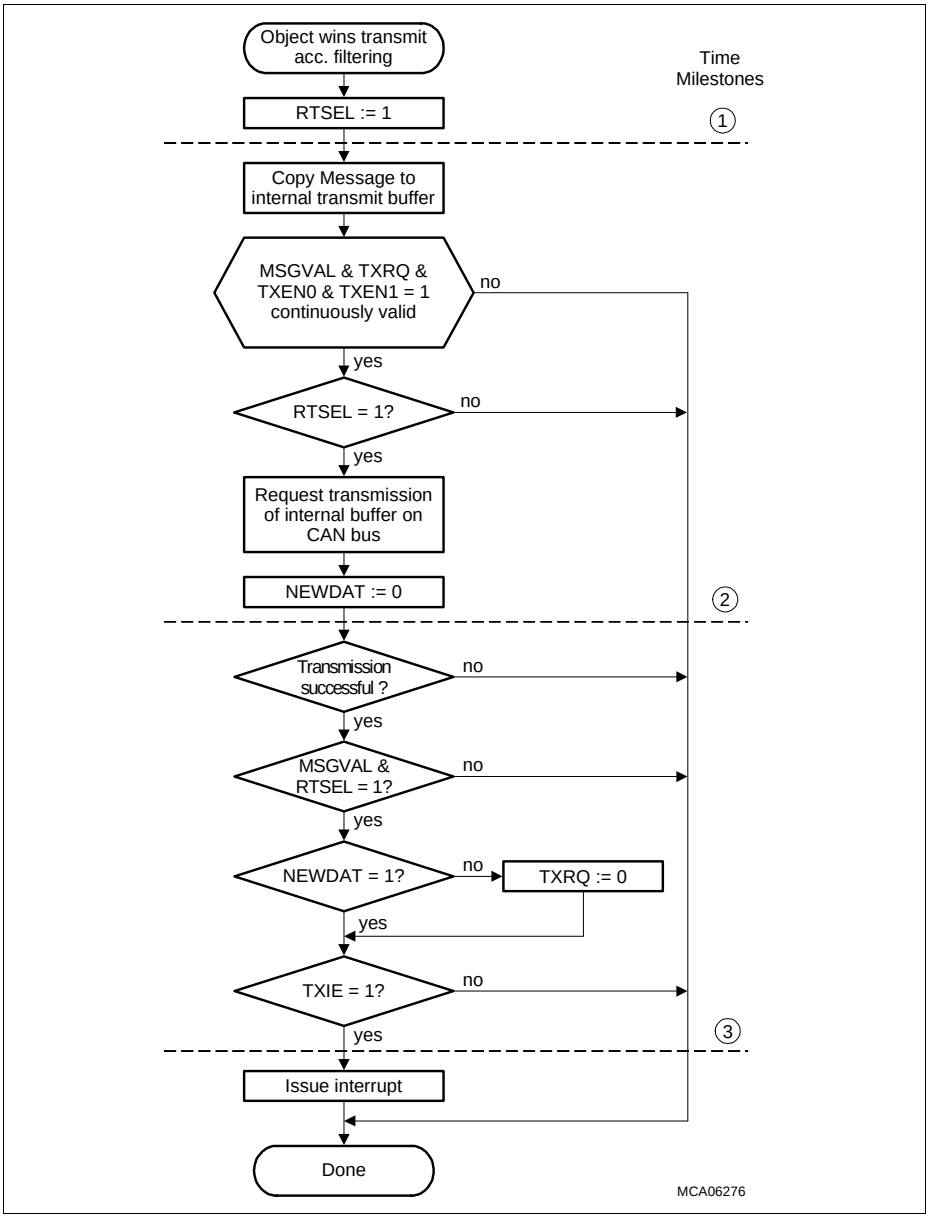


Figure 24-21 Transmission of a Message Object

24.5.11 Message Object Functionality

This chapter describes the functionality of the Message Objects in the MultiCAN module.

24.5.11.1 Standard Message Object

A message object is selected as standard message object when bit field MOFCRn.MMC = 0000_B (see **Page 24-90**). The standard message object can transmit and receive CAN frames according to the basic rules described in the previous sections. Additional services such as Single Data Transfer Mode or Single Transmit Trial (see following sections) are available and can be individually selected.

24.5.11.2 Single Data Transfer Mode

Single Data Transfer Mode is a useful feature in order to broadcast data over the CAN bus without unintended duplication of information. Single Data Transfer Mode is selected via bit MOFCRn.SDT.

Message Reception

When a received message stored in a message object is overwritten by a new received message, the contents of the first message are lost and replaced with the contents of the new received message (indicated by MSGLST = 1).

If SDT is set (Single Data Transfer Mode activated), bit MSGVAL of the message object is automatically cleared by hardware after the storage of a received Data Frame. This prevents the reception of further messages.

After the reception of a Remote Frame, bit MSGVAL is not automatically cleared.

Message Transmission

When a message object receives a series of multiple remote requests, it transmits several Data Frames in response to the remote requests. If the data within the message object has not been updated in the time between the transmissions, the same data can be sent more than once on the CAN bus.

In Single Data Transfer Mode (SDT = 1), this is avoided because MSGVAL is automatically cleared after the successful transmission of a Data Frame.

After the transmission of a Remote Frame, bit MSGVAL is not automatically cleared.

24.5.11.3 Single Transmit Trial

If the bit STT in the message object function register is set (STT = 1), the transmission request is cleared (TXRQ = 0) when the frame contents of the message object have been copied to the internal transmit buffer of the CAN node. Thus, the transmission of the message object is not tried again when it fails due to CAN bus errors.

24.5.11.4 Message Object FIFO Structure

In case of high CPU load it may be difficult to process a series of CAN frames in time. This may happen if multiple messages are received or must be transmitted in short time.

Therefore, a FIFO buffer structure is available to avoid loss of incoming messages and to minimize the setup time for outgoing messages. The FIFO structure can also be used to automate the reception or transmission of a series of CAN messages and to generate a single message interrupt when the whole CAN frame series is done.

There can be several FIFOs in parallel. The number of FIFOs and their size are limited only by the number of available message objects. A FIFO can be installed, resized and de-installed at any time, even during CAN operation.

The basic structure of a FIFO is shown in **Figure 24-22**. A FIFO consists of one base object and n slave objects. The slave objects are chained together in a list structure (similar as in message object lists). The base object may be allocated to any list. Although **Figure 24-22** shows the base object as a separate part beside the slave objects, it is also possible to integrate the base object at any place into the chain of slave objects. This means that the base object is slave object, too (not possible for gateways). The absolute object numbers of the message objects have no impact on the operation of the FIFO.

The base object does not need to be allocated to the same list as the slave objects. Only the slave object must be allocated to a common list (as they are chained together). Several pointers (BOT, CUR and TOP) that are located in the Message Object n FIFO/Gateway Pointer Register MOFGPRn link the base object to the slave objects, regardless whether the base object is allocated to the same or to another **list** than the slave objects.

The smallest FIFO would be a single message object which is both, FIFO base and FIFO slave (not very useful). The biggest possible FIFO structure would include all message objects of the MultiCAN module. Any FIFO sizes between these limits are possible.

In the FIFO base object, the FIFO boundaries are defined. Bit field MOFGPRn.BOT of the base object points to (includes the number of) the bottom slave object in the FIFO structure. The MOFGPRn.TOP bit field points to (includes the number of) the top slave object in the FIFO structure. The MOFGPRn.CUR bit field points to (includes the number of) the slave object that is actually selected by the MultiCAN module for message transfer. When a message transfer takes place with this object, CUR is set to the next message object in the list structure of the slave objects (CUR = PNEXT of current object). If CUR was equal to TOP (top of the FIFO reached), the next update of CUR will result in CUR = BOT (wrap-around from the top to the bottom of the FIFO). This scheme represents a circular FIFO structure where the bit fields BOT and TOP establish the link from the last to the first element.

Bit field MOFGPRn.SEL of the base object can be used for monitoring purposes. It makes it possible to define a slave object within the list at which a message interrupt is

generated whenever the CUR pointer reaches the value of the SEL pointer. Thus SEL makes it possible to detect the end of a predefined message transfer series or to issue a warning interrupt when the FIFO becomes full.

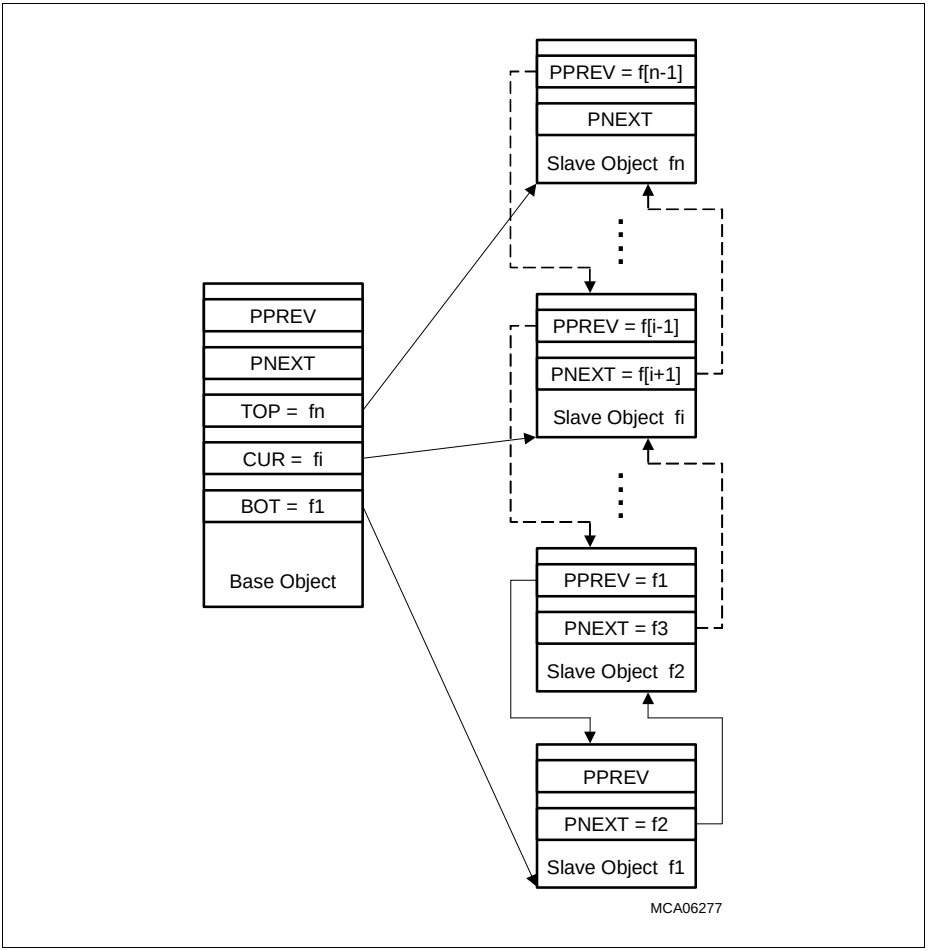


Figure 24-22 FIFO Structure with FIFO Base Object and n FIFO Slave Objects

24.5.11.5 Receive FIFO

The Receive FIFO structure is used to buffer incoming (received) Remote or Data Frames.

A Receive FIFO is selected by setting MOFCRn.MMC = 0001_B in the FIFO base object. This MMC code automatically designates a message object as FIFO base object. The message modes of the FIFO slave objects are not relevant for the operation of the Receive FIFO.

When the FIFO base object receives a frame from the CAN node it belongs to, the frame is not stored in the base object itself but in the message object that is selected by the base object's MOFGPRn.CUR pointer. This message object receives the CAN message as if it is the direct receiver of the message. However, MOFCRn.MMC = 0000_B is implicitly assumed for the FIFO slave object, and a standard message delivery is performed. The actual message mode (MMC setting) of the FIFO slave object is ignored. For the slave object, no acceptance filtering takes place that checks the received frame for a match with the identifier, IDE bit, and DIR bit.

With the reception of a CAN frame, the current pointer CUR of the base object is set to the number of the next message object in the FIFO structure. This message object will then be used to store the next incoming message.

If bit field MOFCRn.OVIE ("Overflow Interrupt Enable") of the FIFO base object is set and the current pointer MOFGPRn.CUR becomes equal to MOFGPRn.SEL, a FIFO overflow interrupt request is generated. This interrupt request is generated on interrupt node TXINP of the base object immediately after the storage of the received frame in the slave object. Transmit interrupts are still generated if TXIE is set.

A CAN message is stored in FIFO base and slave object only if MSGVAL = 1.

In order to avoid direct reception of a message by a slave message object, as if it was an independent message object and not a part of a FIFO, the bit RXEN of each slave object must be cleared. The setting of the bit RXEN is "don't care" only if the slave object is located in a list not assigned to a CAN node.

24.5.11.6 Transmit FIFO

The Transmit FIFO structure is used to buffer a series of Data or Remote Frames that must be transmitted. A transmit FIFO consists of one base message object and one or more slave message objects.

A Transmit FIFO is selected by setting MOFCRn.MMC = 0010_B in the FIFO base object. Unlike the Receive FIFO, slave objects assigned to the Transmit FIFO must explicitly set their bit fields MOFCRn.MMC = 0011_B. The CUR pointer in all slave objects must point back to the Transmit FIFO Base Object (to be initialized by software).

The MOSTATn.TXEN1 bits (Transmit Enable 1) of all message objects except the one which is selected by the CUR pointer of the base object must be cleared by software. TXEN1 of the message (slave) object selected by CUR must be set. CUR (of the base object) may be initialized to any FIFO slave object.

When tagging the message objects of the FIFO as valid to start the operation of the FIFO, then the base object must be tagged valid (MSGVAL = 1) first.

Before a Transmit FIFO becomes de-installed during operation, its slave objects must be tagged invalid (MSGVAL = 0).

The Transmit FIFO uses the TXEN1 bit in the Message Object Control Register of all FIFO elements to select the actual message for transmission. Transmit acceptance filtering evaluates TXEN1 for each message object and a message object can win transmit acceptance filtering only if its TXEN1 bit is set. When a FIFO object has transmitted a message, the hardware clears its TXEN1 bit in addition to standard transmit postprocessing (clear TXRQ, transmit interrupt etc.), and moves the CUR pointer in the next FIFO base object to be transmitted. TXEN1 is set automatically (by hardware) in the next message object. Thus, TXEN1 moves along the Transmit FIFO structure as a token that selects the active element.

If bit field MOFCRn.OVIE (“Overflow Interrupt Enable”) of the FIFO base object is set and the current pointer CUR becomes equal to MOFGPRn.SEL, a FIFO overflow interrupt request is generated. The interrupt request is generated on interrupt node RXINP of the base object after postprocessing of the received frame. Receive interrupts are still generated for the Transmit FIFO base object if bit RXIE is set.

24.5.11.7 Gateway Mode

The Gateway Mode makes it possible to establish an automatic information transfer between two independent CAN buses without CPU interaction.

The Gateway Mode operates on message object level. In Gateway mode, information is transferred between two message objects, resulting in an information transfer between the two CAN nodes to which the message objects are allocated. A gateway may be established with any pair of CAN nodes, and there can be as many gateways as there are message objects available to build the gateway structure.

Gateway Mode is selected by setting MOFCRs.MMC = 0100_B for the gateway source object s. The gateway destination object d is selected by the MOFGPRd.CUR pointer of the source object. The gateway destination object only needs to be valid (its MSGVAL = 1). All other settings are not relevant for the information transfer from the source object to the destination object.

Gateway source object behaves as a standard message object with the difference that some additional actions are performed by the MultiCAN module when a CAN frame has been received and stored in the source object (see **Figure 24-23**):

1. If bit MOFCRs.DLCC is set, the data length code MOFCRs.DLC is copied from the gateway source object to the gateway destination object.
2. If bit MOFCRs.IDC is set, the identifier MOARs.ID and the identifier extension MOARs.IDE are copied from the gateway source object to the gateway destination object.
3. If bit MOFCRs.DATC is set, the data bytes stored in the two data registers MODATALs and MODATAHs are copied from the gateway source object to the gateway destination object. All 8 data bytes are copied, even if MOFCRs.DLC indicates less than 8 data bytes.
4. If bit MOFCRs.GDFS is set, the transmit request flag MOSTATd.TXRQ is set in the gateway destination object.
5. The receive pending bit MOSTATd.RXPND and the new data bit MOSTATd.NEWDAT are set in the gateway destination object.
6. A message interrupt request is generated for the gateway destination object if its MOSTATd.RXIE is set.
7. The current object pointer MOFGPRs.CUR of the gateway source object is moved to the next destination object according to the FIFO rules as described on **Page 24-53**. A gateway with a single (static) destination object is obtained by setting MOFGPRs.TOP = MOFGPRs.BOT = MOFGPRs.CUR = destination object.

The link from the gateway source object to the gateway destination object works in the same way as the link from a FIFO base to a FIFO slave. This means that a gateway with an integrated destination FIFO may be created; in **Figure 24-22**, the object on the left is the gateway source object and the message object on the right side is the gateway destination objects.

The gateway operates equivalent for the reception of data frames (source object is receive object, i.e. DIR = 0) as well as for the reception of Remote Frames (source object is transmit object).

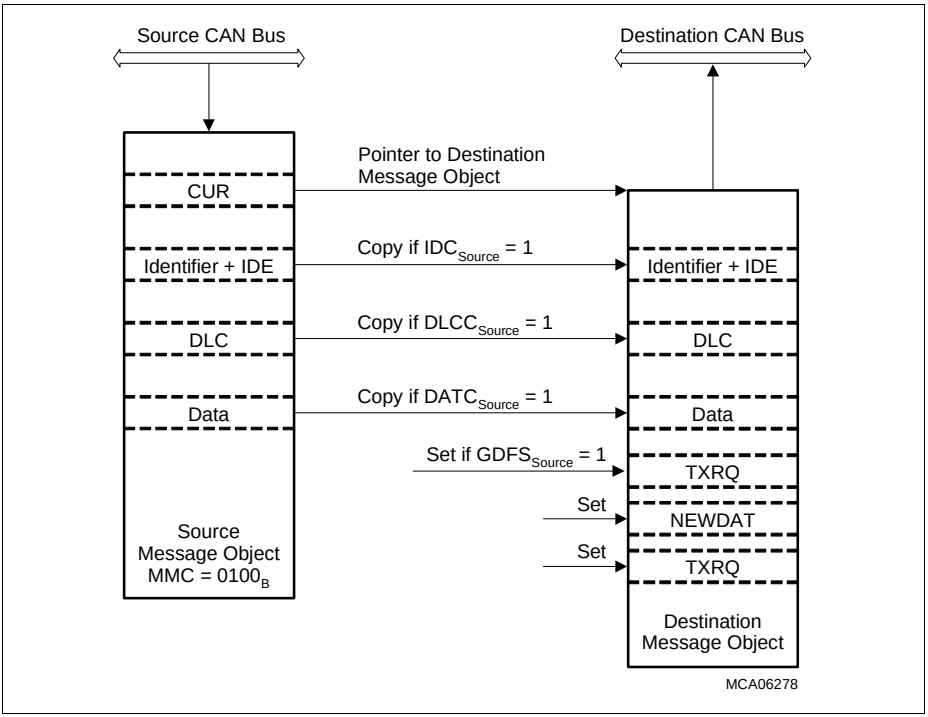


Figure 24-23 Gateway Transfer from Source to Destination

24.5.11.8 Foreign Remote Requests

When a Remote Frame has been received on a CAN node and is stored in a message object, a transmit request is set to trigger the answer (transmission of a Data Frame) to the request or to automatically issue a secondary request. If the Foreign Remote Request Enable bit MOFCRn.FRREN is cleared in the message object in which the remote request is stored, MOSTATn.TXRQ is set in the same message object.

If bit FRREN is set (FRREN = 1: foreign remote request enabled), TXRQ is set in the message object that is referenced by pointer MOFGPRn.CUR. The value of CUR is, however, not changed by this feature.

Although the foreign remote request feature works independently of the selected message mode, it is especially useful for gateways to issue a remote request on the source bus of a gateway after the reception of a remote request on the gateway destination bus. According to the setting of FRREN in the gateway destination object, there are two capabilities to handle remote requests that appear on the destination side (assuming that the source object is a receive object and the destination is a transmit object, i.e. DIR_{source} = 0 and $DIR_{destination}$ = 1):

FRREN = 0 in the Gateway Destination Object

1. A Remote Frame is received by gateway destination object.
2. TXRQ is set automatically in the gateway destination object.
3. A Data Frame with the current data stored in the destination object is transmitted on the destination bus.

FRREN = 1 in the Gateway Destination Object

1. A Remote Frame is received by gateway destination object.
2. TXRQ is set automatically in the gateway source object (must be referenced by CUR pointer of the destination object).
3. A remote request is transmitted by the source object (which is a receive object) on the source CAN bus.
4. The receiver of the remote request responds with a Data Frame on the source bus.
5. The Data Frame is stored in the source object.
6. The Data Frame is copied to the destination object (gateway action).
7. TXRQ is set in the destination object (assuming $GDFS_{source}$ = 1).
8. The new data stored in the destination object is transmitted on the destination bus, in response to the initial remote request on the destination bus.

24.6 MultiCAN Kernel Registers

This section describes the kernel registers of the MultiCAN module. All MultiCAN kernel register names described in this section are also referenced in other parts of the TC1798 User´s Manual by the module name prefix “CAN_”.

MultiCAN Kernel Register Overview

The MultiCAN Kernel include three blocks of registers:

- Global Module Registers
- Node Registers, for each CAN node x
- Message Object Registers, for each message object n

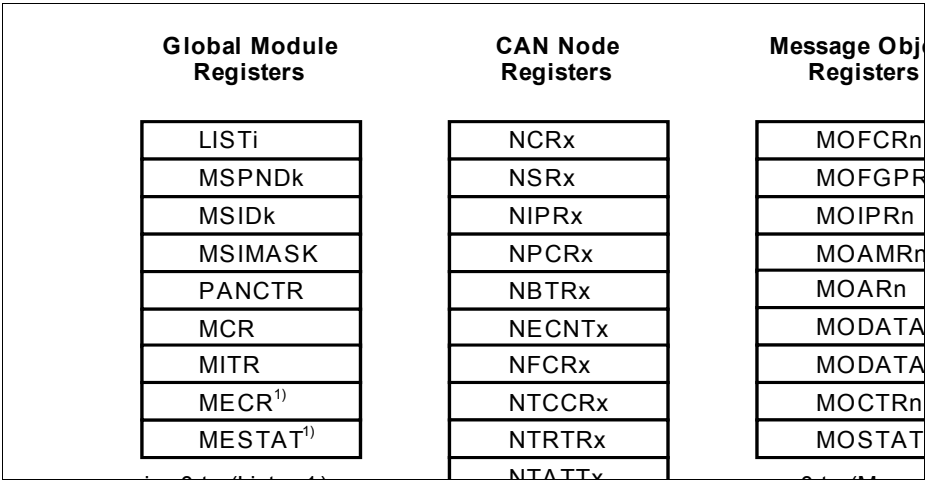


Figure 24-24 MultiCAN Kernel Registers

The registers of the MultiCAN module kernel are listed below.

Table 24-5 Registers Address Space - MultiCAN Kernel Registers

Module	Base Address	End Address	Note
CAN	F000 4000$_H$	F000 7FFF$_H$	-

Table 24-6 Registers Overview - MultiCAN Kernel Registers

Register Short Name	Register Long Name	Offset Address[1)]	Description see
LISTi	List Register i	$0100_H + i \times 4_H$	Page 24-71
MSPNDk	Message Pending Register k	$0140_H + k \times 4_H$	Page 24-73
MSIDk	Message Index Register k	$0180_H + k \times 4_H$	Page 24-74
MSIMASK	Message Index Mask Register	$01C0_H$	Page 24-75
ID	Module Identification Register	008_H	Page 24-64
PANCTR	Panel Control Register	$01C4_H$	Page 24-65
MCR	Module Control Register	$01C8_H$	Page 24-69
MITR	Module Interrupt Trigger Reg.	$01CC_H$	Page 24-70
NCRx	Node x Control Register	$0200_H + x \times 100_H$	Page 24-76
NSRx	Node x Status Register	$0204_H + x \times 100_H$	Page 24-80
NIPRx	Node x Interrupt Pointer Reg.	$0208_H + x \times 100_H$	Page 24-84
NPCRx	Node x Port Control Register	$020C_H + x \times 100_H$	Page 24-86
NBTRx	Node x Bit Timing Register	$0210_H + x \times 100_H$	Page 24-87
NECNTx	Node x Error Counter Register	$0214_H + x \times 100_H$	Page 24-89
NFCRx	Node x Frame Counter Register	$0218_H + x \times 100_H$	Page 24-90
MOFCRn	Message Object n Function Control Register	$1000_H + n \times 20_H$	Page 24-104
MOFGPRn	Message Object n FIFO/Gateway Pointer Register	$1004_H + n \times 20_H$	Page 24-109
MOIPRn	Message Object n Interrupt Pointer Register	$1008_H + n \times 20_H$	Page 24-102
MOAMRn	Message Object n Acceptance Mask Register	$100C_H + n \times 20_H$	Page 24-110
MODATALn	Message Object n Data Register Low	$1010_H + n \times 20_H$	Page 24-115
MODATAHn	Message Object n Data Register High	$1014_H + n \times 20_H$	Page 24-116
MOARn	Message Object n Arbitration Register	$1018_H + n \times 20_H$	Page 24-112
MOCTRn MOSTATn	Message Object n Control Reg. Message Object n Status Reg.	$101C_H + n \times 20_H$	Page 24-94 Page 24-97

1) The absolute register address is calculated as follows:
Module Base Address (**Table 24-5**) + Offset Address (shown in this column)
Further, the following ranges for parameters i, k, x, and n are valid: i = 0-7, k = 0-7, x = 0-3, n = 0-127.

Figure 24-25 shows the MultiCAN register address map, without TTCAN registers. They are shown in **Figure 24-38**.

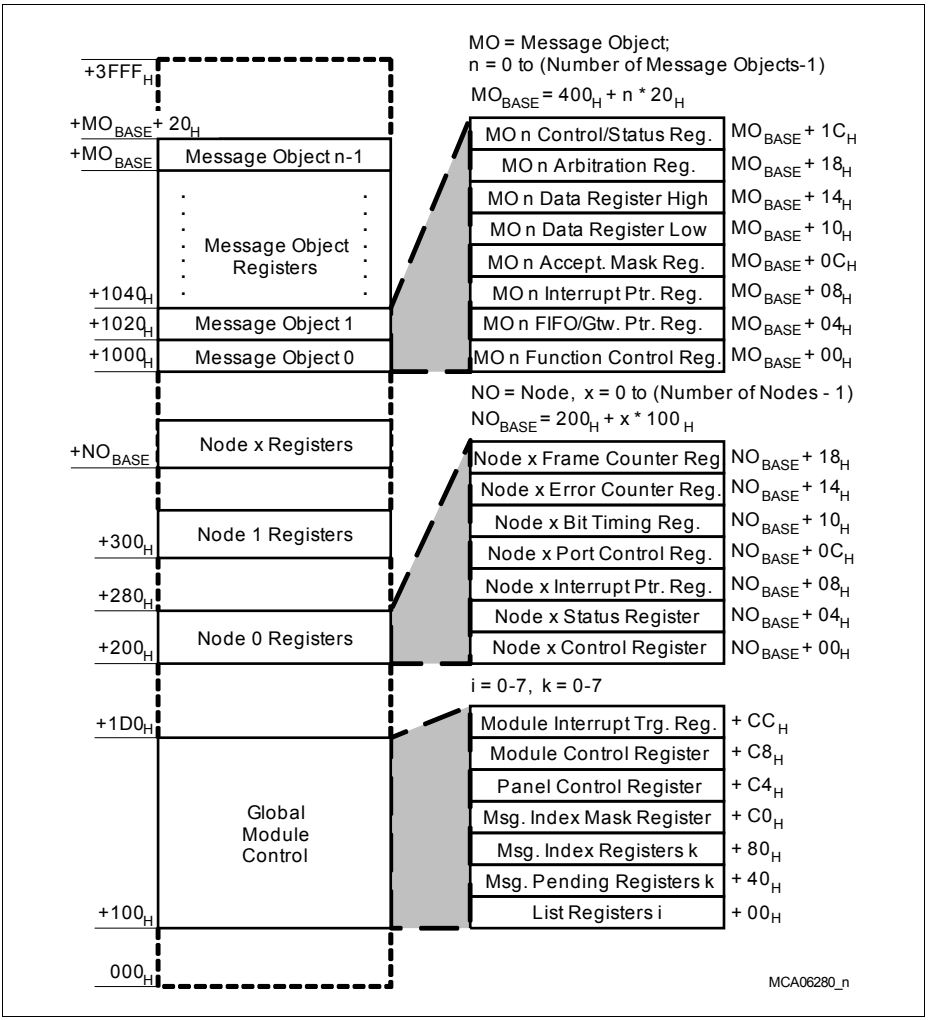


Figure 24-25 MultiCAN Register Address Map

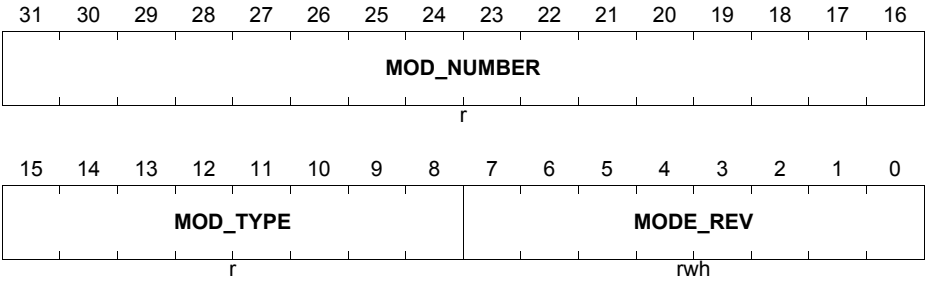
24.6.1 Global Module Registers

All list operations such as allocation, de-allocation and relocation of message objects within the list structure are performed via the Command Panel. It is not possible to modify the list structure directly by software by writing to the message objects and the LIST registers.

Module Identification Register .

ID

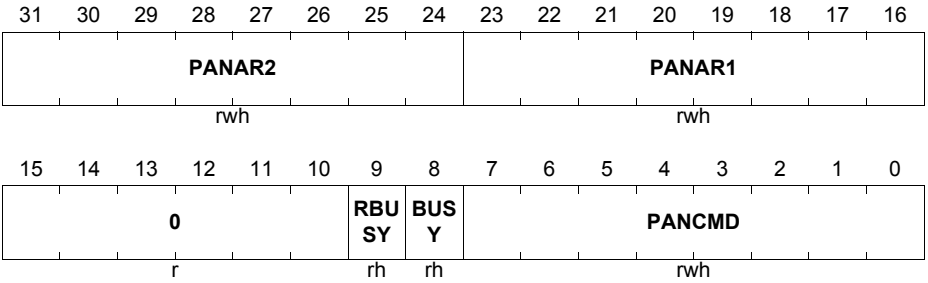
Module Identification Register (008_H) Reset Value: 002B C0XX$_H$



Field	Bits	Type	Description
MOD_REV	[7:0]	r	**Module Revision Number** MOD_REV defines the revision number. The value of a module revision starts with 01_H (first revision).
MOD_TYPE	[15:8]	r	**Module Type** $C0_H$ Define the module as a 32-bit module.
MOD_NUMBER	[31:16]	r	**Module Number Value** This bit field defines the MultiCAN module identification number (=002BH)

The Panel Control Register PANCTR is used to start a new command by writing the command arguments and the command code into its bit fields.

PANCTR
Panel Control Register **($1C4_H$)** **Reset Value: $0000\ 0301_H$**



Field	Bits	Type	Description
PANCMD	[7:0]	rwh	**Panel Command** This bit field is used to start a new command by writing a panel command code into it. At the end of a panel command, the NOP (no operation) command code is automatically written into PANCMD. The coding of PANCMD is defined in **Table 24-7**.
BUSY	8	rh	**Panel Busy Flag** 0_B Panel has finished command and is ready to accept a new command. 1_B Panel operation is in progress.
RBUSY	9	rh	**Result Busy Flag** 0_B No update of PANAR1 and PANAR2 is scheduled by the list controller. 1_B A list command is running (BUSY = 1) that will write results to PANAR1 and PANAR2, but the results are not yet available.
PANAR1	[23:16]	rwh	**Panel Argument 1** See **Table 24-7**.
PANAR2	[31:24]	rwh	**Panel Argument 2** See **Table 24-7**.
0	[15:10]	r	**Reserved** Read as 0; should be written with 0.

Panel Commands

A panel operation consists of a command code (PANCMD) and up to two panel arguments (PANAR1, PANAR2). Commands that have a return value deliver it to the PANAR1 bit field. Commands that return an error flag deliver it to bit 31 of the Panel Control Register, this means bit 7 of PANAR2.

Table 24-7 Panel Commands

PANCMD	PANAR2	PANAR1	Command Description
00_H	–	–	**No Operation** Writing 00_H to PANCMD has no effect. No new command is started.
01_H	**Result:** Bit 7: ERR Bit 6-0: undefined	–	**Initialize Lists** Run the initialization sequence to reset the CTRL and LIST fields of all message objects. List registers LIST[7:0] are set to their reset values. This results in the de-allocation of all message objects. The initialization command requires that bits NCRx.INIT and NCRx.CCE are set for all CAN nodes. Bit 7 of PANAR2 (ERR) reports the success of the operation: 0_B Initialization was successful 1_B Not all NCRx.INIT and NCRx.CCE bits are set. Therefore, no initialization is performed. The initialize lists command is automatically performed with each reset of the MultiCAN module, but with the exception that all message object registers are reset, too.
02_H	**Argument:** List Index	**Argument:** Message Object Number	**Static Allocate** Allocate message object to a list. The message object is removed from the list that it currently belongs to, and appended to the end of the list, given by PANAR2. This command is also used to deallocate a message object. In this case, the target list is the list of unallocated elements (PANAR2 = 0).

Table 24-7 Panel Commands (cont'd)

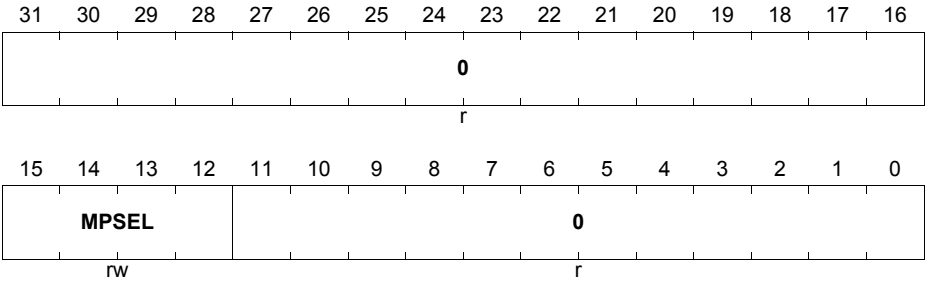
PANCMD	PANAR2	PANAR1	Command Description
03_H	**Argument:** List Index **Result:** Bit 7: ERR Bit 6-0: undefined	**Result:** Message Object Number	**Dynamic Allocate** Allocate the first message object of the list of unallocated objects to the selected list. The message object is appended to the end of the list. The message number of the message object is returned in PANAR1. An ERR bit (bit 7 of PANAR2) reports the success of the operation: 0_B Success. 1_B The operation has not been performed because the list of unallocated elements was empty.
04_H	**Argument:** Destination Object Number	**Argument:** Source Object Number	**Static Insert Before** Remove a message object (source object) from the list that it currently belongs to, and insert it before a given destination object into the list structure of the destination object. The source object thus becomes the predecessor of the destination object.
05_H	**Argument:** Destination Object Number **Result:** Bit 7: ERR Bit 6-0: undefined	**Result:** Object Number of inserted object	**Dynamic Insert Before** Insert a new message object before a given destination object. The new object is taken from the list of unallocated elements (the first element is chosen). The number of the new object is delivered as a result to PANAR1. An ERR bit (bit 7 of PANAR2) reports the success of the operation: 0_B Success. 1_B The operation has not been performed because the list of unallocated elements was empty.

Table 24-7 Panel Commands (cont'd)

PANCMD	PANAR2	PANAR1	Command Description
06_H	**Argument:** Destination Object Number	**Argument:** Source Object Number	**Static Insert Behind** Remove a message object (source object) from the list that it currently belongs to, and insert it behind a given destination object into the list structure of the destination object. The source object thus becomes the successor of the destination object.
07_H	**Argument:** Destination Object Number **Result:** Bit 7: ERR Bit 6-0: undefined	**Result:** Object Number of inserted object	**Dynamic Insert Behind** Insert a new message object behind a given destination object. The new object is taken from the list of unallocated elements (the first element is chosen). The number of the new object is delivered as result to PANAR1. An ERR bit (bit 7 of PANAR2) reports the success of the operation: 0_B Success. 1_B The operation has not been performed because the list of unallocated elements was empty.
08_H - FF_H	–	–	**Reserved**

The Module Control Register MCR contains basic settings that determine the operation of the MultiCAN module.

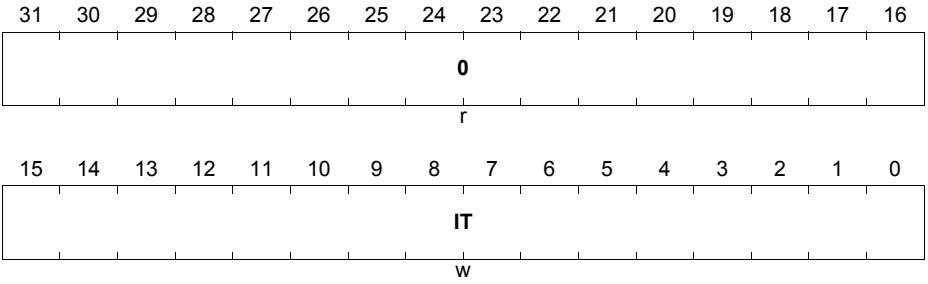
MCR
Module Control Register **($1C8_H$)** **Reset Value: $0000\ 0000_H$**



Field	Bits	Type	Description
MPSEL	[15:12]	rw	**Message Pending Selector** Bit field MPSEL makes it possible to select the bit position of the message pending bit after a message reception/transmission by a mixture of the MOIPRn register bit fields RXINP, TXINP, and MPN. Selection details are given in **Figure 24-19** on **Page 24-44**.
0	[31:16], [11:0]	r	**Reserved** Read as 0; should be written with 0.

The Interrupt Trigger Register ITR is used to trigger interrupt requests on each interrupt output line by software.

MITR
Module Interrupt Trigger Register ($1CC_H$) Reset Value: $0000\ 0000_H$



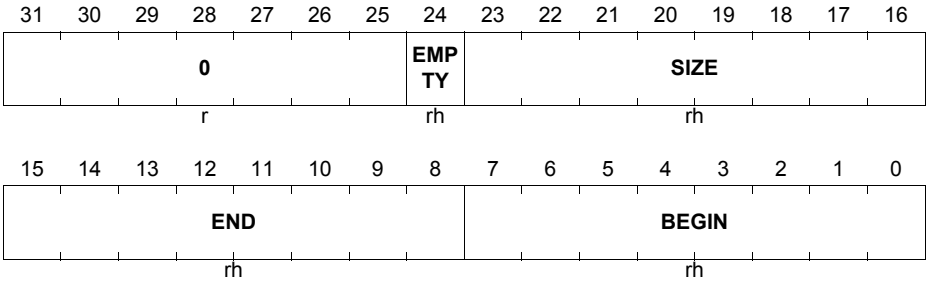
Field	Bits	Type	Description
IT	[15:0]	w	**Interrupt Trigger** Writing a 1 to IT[n] (n = 0-15) generates an interrupt request on interrupt output line INT_O[n]. Writing a 0 to IT[n] has no effect. Bit field IT is always read as 0. Multiple interrupt requests can be generated with a single write operation to MITR by writing a 1 to several bit positions of IT.
0	[31:16]	r	**Reserved** Read as 0; should be written with 0.

List Pointer and List Register

Each CAN node has a list that determines the allocated message objects. Additionally, a list of all unallocated objects is available. Furthermore, general purpose lists are available which are not associated to a CAN node. The List Registers are assigned in the following way:

- LIST0 provides the list of all unallocated objects
- LIST1 provides the list for CAN node 0
- LIST2 provides the list for CAN node 1
- LIST3 provides the list for CAN node 2
- LIST[7:4] are not associated to a CAN node (free lists)

LIST0
List Register 0 **(100_H)** **Reset Value: 007F 7F00$_H$**
LISTx (x = 1-7)
List Register x **(100_H+x*4_H)** **Reset Value: 0100 0000$_H$**



Field	Bits	Type	Description
BEGIN	[7:0]	rh	**List Begin** BEGIN indicates the number of the first message object in list i.
END	[15:8]	rh	**List End** END indicates the number of the last message object in list i.
SIZE	[23:16]	rh	**List Size** SIZE indicates the number of elements in the list i. SIZE = number of list elements - 1 SIZE = 0 indicates that list x is empty.

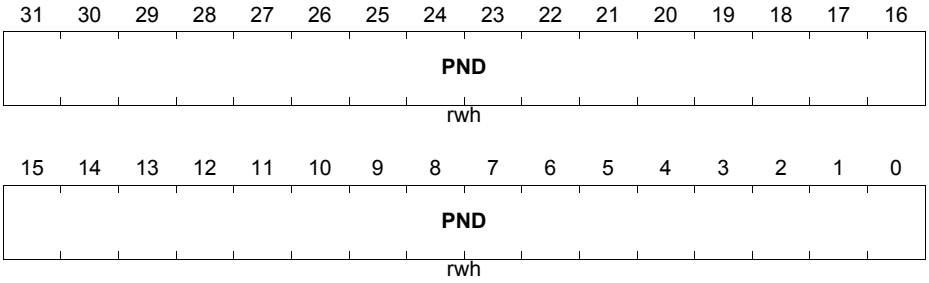
Field	Bits	Type	Description
EMPTY	24	rh	**List Empty Indication** 0_B At least one message object is allocated to list i. 1_B No message object is allocated to the list x. List x is empty.
0	[31:25]	r	**Reserved** Read as 0.

Message Notifications

When a message object n generates an interrupt request upon the transmission or reception of a message, then the request is routed to the interrupt output line selected by the bit field MOIPRn.TXINP or MOIPRn.RXINP of the message object n. As there are more message objects than interrupt output lines, an interrupt routine typically processes requests from more than one message object. Therefore, a priority selection mechanism is implemented in the MultiCAN module to select the highest priority object within a collection of message objects.

The Message Pending Register MSPNDk contains the pending interrupt notification of list i.

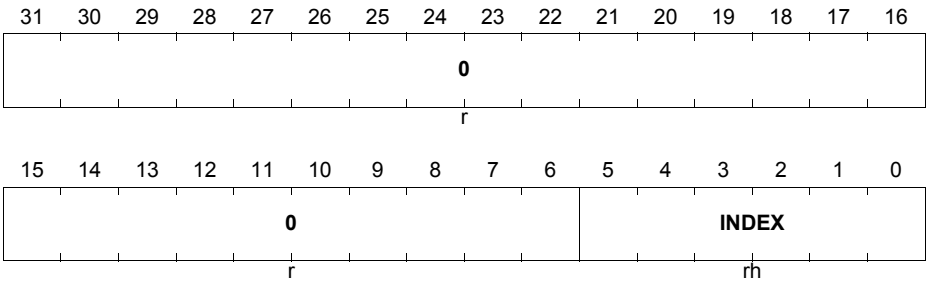
MSPNDk (k = 0-7)
Message Pending Register k **(140_H+k*4_H)** **Reset Value: 0000 0000_H**



Field	Bits	Type	Description
PND	[31:0]	rwh	**Message Pending** When a message interrupt occurs, the message object sets a bit in one of the MSPND register, where the bit position is given by the MPN[4:0] field of the IPR register of the message object. The register selection n is given by the higher bits of MPN. The register bits can be cleared by software (write 0). Writing a 1 has no effect.

Each Message Pending Register has a Message Index Register MSIDk associated with it. The Message Index Register shows the active (set) pending bit with lowest bit position within groups of pending bits.

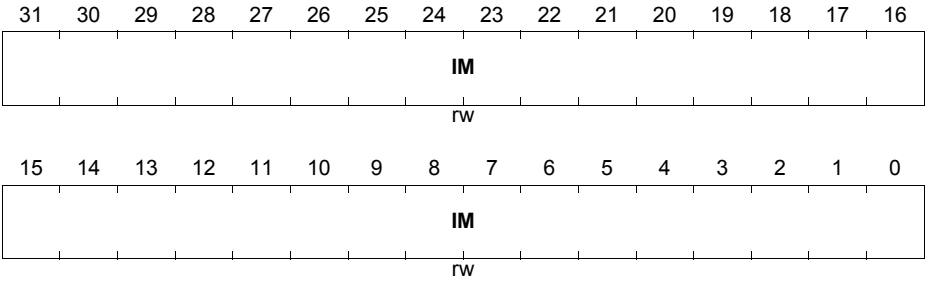
MSIDk (k = 0-7)
Message Index Register k **(180_H+k*4_H)** **Reset Value: 0000 0020_H**



Field	Bits	Type	Description
INDEX	[5:0]	rh	**Message Pending Index** The value of INDEX is given by the bit position i of the pending bit of MSPNDk with the following properties: 1. MSPNDk[i] & IM[i] = 1 2. i = 0 or MSPNDk[i-1:0] & IM[i-1:0] = 0 If no bit of MSPNDk satisfies these conditions then INDEX reads 100000_B. Thus INDEX shows the position of the first pending bit of MSPNDk, in which only those bits of MSPNDk that are selected in the Message Index Mask Register are taken into account.
0	[31:6]	r	**Reserved** Read as 0; should be written with 0.

The Message Index Mask Register MSIMASK selects individual bits for the calculation of the Message Pending Index. The Message Index Mask Register is used commonly for all Message Pending registers and their associated Message Index registers.

MSIMASK
Message Index Mask Register **($1C0_H$)** **Reset Value: $0000\ 0000_H$**



Field	Bits	Type	Description
IM	[31:0]	rw	**Message Index Mask** Only those bits in MSPNDk for which the corresponding Index Mask bits are set contribute to the calculation of the Message Index.

24.6.2 CAN Node Registers

The CAN node registers are built in for each CAN node of the MultiCAN module. They contain information that is directly related to the operation of the CAN nodes and are shared among the nodes.

The Node Control Register contains basic settings that determine the operation of the CAN node.

NCRx (x = 0-3)
Node x Control Register **(200_H+x*100_H)** **Reset Value: 0000 0001_H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0							SUSEN	CALM	CCE	0	CANDIS	ALIE	LECIE	TRIE	INIT
r							rw	rw	rw	r	rw	rw	rw	rw	rwh

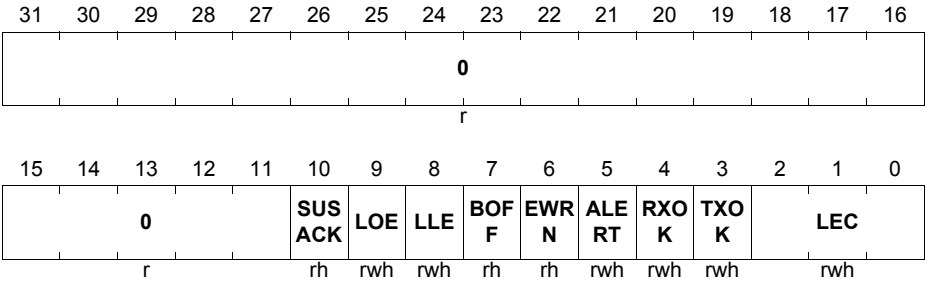
Field	Bits	Type	Description
INIT	0	rwh	**Node Initialization** 0_B Resetting bit INIT enables the participation of the node in the CAN traffic. If the CAN node is in the bus-off state, the ongoing bus-off recovery (which does not depend on the INIT bit) is continued. With the end of the bus-off recovery sequence the CAN node is allowed to take part in the CAN traffic. If the CAN node is not in the bus-off state, a sequence of 11 consecutive recessive bits must be detected before the node is allowed to take part in the CAN traffic. 1_B Setting this bit terminates the participation of this node in the CAN traffic. Any ongoing frame transfer is cancelled and the transmit line goes recessive. If the CAN node is in the bus-off state, then the running bus-off recovery sequence is continued. If the INIT bit is still set after the successful completion of the bus-off recovery sequence, i.e. after detecting 128 sequences of 11 consecutive recessive bits (11×1), then the CAN node leaves the bus-off state but remains inactive as long as INIT remains set. Bit INIT is automatically set when the CAN node enters the bus-off state (see **Page 24-28**).
TRIE	1	rw	**Transfer Interrupt Enable** TRIE enables the transfer interrupt of CAN node x. This interrupt is generated after the successful reception or transmission of a CAN frame in node x. 0_B Transfer interrupt is disabled. 1_B Transfer interrupt is enabled. Bit field NIPRx.TRINP selects the interrupt output line which becomes activated at this type of interrupt.

Field	Bits	Type	Description
LECIE	2	rw	**LEC Indicated Error Interrupt Enable** LECIE enables the last error code interrupt of CAN node x. This interrupt is generated with each update of bit field NSRx.LEC with LEC > 0 (CAN protocol error). 0_B Last error code interrupt is disabled. 1_B Last error code interrupt is enabled. Bit field NIPRx.LECINP selects the interrupt output line which becomes activated at this type of interrupt.
ALIE	3	rw	**Alert Interrupt Enable** ALIE enables the alert interrupt of CAN node x. This interrupt is generated by any one of the following events: • A change of bit NSRx.BOFF • A change of bit NSRx.EWRN • A List Length Error, which also sets bit NSRx.LLE • A List Object Error, which also sets bit NSRx.LOE • A Bit INIT is set by hardware 0_B Alert interrupt is disabled. 1_B Alert interrupt is enabled. Bit field NIPRx.ALINP selects the interrupt output line which becomes activated at this type of interrupt.
CANDIS	4	rw	**CAN Disable** Setting this bit disables the CAN node. The CAN node first waits until it is bus-idle or bus-off. Then bit INIT is automatically set, and an alert interrupt is generated if bit ALIE is set.
CCE	6	rw	**Configuration Change Enable** 0_B The Bit Timing Register, the Port Control Register, and the Error Counter Register may only be read. All attempts to modify them are ignored. 1_B The Bit Timing Register, the Port Control Register, and the Error Counter Register may be read and written.
CALM	7	rw	**CAN Analyze Mode** If this bit is set, then the CAN node operates in Analyze Mode. This means that messages may be received, but not transmitted. No acknowledge is sent on the CAN bus upon frame reception. Active-error flags are sent recessive instead of dominant. The transmit line is continuously held at recessive (1) level. Bit CALM can be written only while bit INIT is set.

Field	Bits	Type	Description
SUSEN	8	rw	**Suspend Enable** This bit makes it possible to set the CAN node into Suspend Mode via OCDS (on chip debug support): 0_B An OCDS suspend trigger is ignored by the CAN node. 1_B An OCDS suspend trigger disables the CAN node: As soon as the CAN node becomes bus-idle or bus-off, bit INIT is internally forced to 1 to disable the CAN node. The actual value of bit INIT remains unchanged. Bit SUSEN is reset via OCDS Reset.
0	[31:9], 5	r	**Reserved** Read as 0; should be written with 0.

The Node Status Register NSRx reports errors as well as successfully transferred CAN frames.

NSRx (x = 0-3)
Node x Status Register **(204_H+x*100_H)** **Reset Value: 0000 0000_H**



Field	Bits	Type	Description
LEC	[2:0]	rwh	**Last Error Code** This bit field indicates the type of the last (most recent) CAN error. The encoding of this bit field is described in **Table 24-8**.
TXOK	3	rwh	**Message Transmitted Successfully** 0_B No successful transmission since last (most recent) flag reset. 1_B A message has been transmitted successfully (error-free and acknowledged by at least another node). TXOK must be reset by software (write 0). Writing 1 has no effect.
RXOK	4	rwh	**Message Received Successfully** 0_B No successful reception since last (most recent) flag reset. 1_B A message has been received successfully. RXOK must be reset by software (write 0). Writing 1 has no effect.

Field	Bits	Type	Description
ALERT	5	rwh	**Alert Warning** The ALERT bit is set upon the occurrence of one of the following events (the same events which also trigger an alert interrupt if ALIE is set): • A change of bit NSRx.BOFF • A change of bit NSRx.EWRN • A List Length Error, which also sets bit NSRx.LLE • A List Object Error, which also sets bit NSRx.LOE • Bit INIT has been set by hardware ALERT must be reset by software (write 0). Writing 1 has no effect.
EWRN	6	rh	**Error Warning Status** 0_B No warning limit exceeded. 1_B One of the error counters REC or TEC reached the warning limit EWRNLVL.
BOFF	7	rh	**Bus-off Status** 0_B CAN controller is not in the bus-off state. 1_B CAN controller is in the bus-off state.
LLE	8	rwh	**List Length Error** 0_B No List Length Error since last (most recent) flag reset. 1_B A List Length Error has been detected during message acceptance filtering. The number of elements in the list that belongs to this CAN node differs from the list SIZE given in the list termination pointer. LLE must be reset by software (write 0). Writing 1 has no effect.
LOE	9	rwh	**List Object Error** 0_B No List Object Error since last (most recent) flag reset. 1_B A List Object Error has been detected during message acceptance filtering. A message object with wrong LIST index entry in the Message Object Control Register has been detected. LOE must be reset by software (write 0). Writing 1 has no effect.

Field	Bits	Type	Description
SUSACK	10	rh	**Suspend Acknowledge** 0_B The CAN node is not in Suspend Mode or a suspend request is pending, but the CAN node has not yet reached bus-idle or bus-off. 1_B The CAN node is in Suspend Mode: The CAN node is inactive (bit NCR.INIT internally forced to 1) due to an OCDS suspend request.
0	[31:11]	r	**Reserved** Read as 0; should be written with 0.

Encoding of the LEC Bit Field

Table 24-8 Encoding of the LEC Bit Field

LEC Value	Signification
000_B	**No Error:** No error was detected for the last (most recent) message on the CAN bus.
001_B	**Stuff Error:** More than 5 equal bits in a sequence have occurred in a part of a received message where this is not allowed.
010_B	**Form Error:** A fixed format part of a received frame has the wrong format.
011_B	**Ack Error:** The transmitted message was not acknowledged by another node.
100_B	**Bit1 Error:** During a message transmission, the CAN node tried to send a recessive level (1) outside the arbitration field and the acknowledge slot, but the monitored bus value was dominant.
101_B	**Bit0 Error:** Two different conditions are signaled by this code: 1. During transmission of a message (or acknowledge bit, active-error flag, overload flag), the CAN node tried to send a dominant level (0), but the monitored bus value was recessive. 2. During bus-off recovery, this code is set each time a sequence of 11 recessive bits has been monitored. The CPU may use this code as indication that the bus is not continuously disturbed.

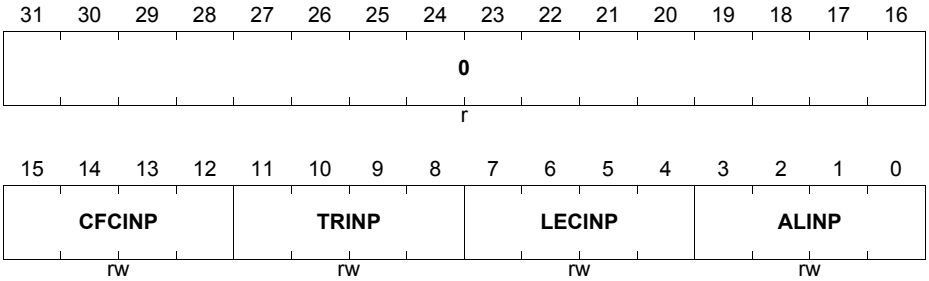
Table 24-8 Encoding of the LEC Bit Field (cont'd)

LEC Value	Signification
110_B	**CRC Error:** The CRC checksum of the received message was incorrect.
111_B	**CPU write to LEC:** Whenever the the CPU writes the value 111 to LEC, it takes the value 111. Whenever the CPU writes another value to LEC, the written LEC value is ignored.

The four interrupt pointers in the Node Interrupt Pointer Register NIPRx select one out of the sixteen interrupt outputs individually for each type of CAN node interrupt. See also **Page 24-29** for more CAN node interrupt details.

NIPRx (x = 0-3)
Node x Interrupt Pointer Register

(208_H+x*100_H) **Reset Value: 0000 0000_H**

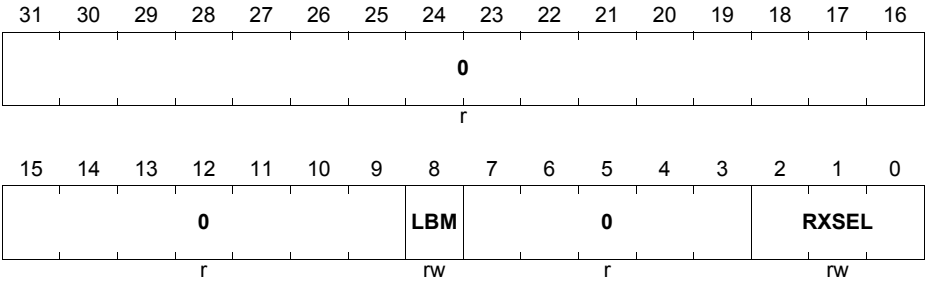


Field	Bits	Type	Description
ALINP	[3:0]	rw	**Alert Interrupt Node Pointer** ALINP selects the interrupt output line INT_Om (m = 0-15) for an alert interrupt of CAN Node x. 0000_B Interrupt output line INT_O0 is selected. 0001_B Interrupt output line INT_O1 is selected. $\ldots_B$ … 1110_B Interrupt output line INT_O14 is selected. 1111_B Interrupt output line INT_O15 is selected.
LECINP	[7:4]	rw	**Last Error Code Interrupt Node Pointer** LECINP selects the interrupt output line INT_Om (m = 0-15) for an LEC interrupt of CAN Node x. 0000_B Interrupt output line INT_O0 is selected. 0001_B Interrupt output line INT_O1 is selected. $\ldots_B$ … 1110_B Interrupt output line INT_O14 is selected. 1111_B Interrupt output line INT_O15 is selected.

Field	Bits	Type	Description
TRINP	[11:8]	rw	**Transfer OK Interrupt Node Pointer** TRINP selects the interrupt output line INT_Om (m = 0-15) for a transfer OK interrupt of CAN Node x. 0000_B Interrupt output line INT_O0 is selected. 0001_B Interrupt output line INT_O1 is selected. $\ldots_B$ … 1110_B Interrupt output line INT_O14 is selected. 1111_B Interrupt output line INT_O15 is selected.
CFCINP	[15:12]	rw	**Frame Counter Interrupt Node Pointer** CFCINP selects the interrupt output line INT_Om (m = 0-15) for a transfer OK interrupt of CAN Node x. 0000_B Interrupt output line INT_O0 is selected. 0001_B Interrupt output line INT_O1 is selected. $\ldots_B$ … 1110_B Interrupt output line INT_O14 is selected. 1111_B Interrupt output line INT_O15 is selected.
0	[31:16]	r	**Reserved** Read as 0; should be written with 0.

The Node Port Control Register NPCRx configures the CAN bus transmit/receive ports. NPCRx can be written only if bit NCRx.CCE is set.

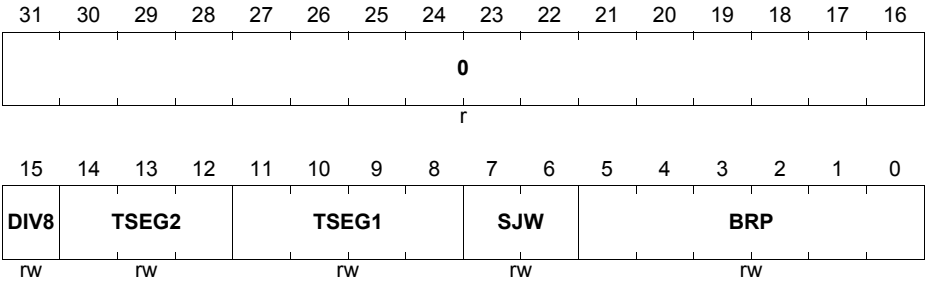
NPCRx (x = 0-3)
Node x Port Control Register **($20C_H$+x*100_H)** **Reset Value: 0000 0000_H**



Field	Bits	Type	Description
RXSEL	[2:0]	rw	**Receive Select** RXSEL selects one out of 8 possible receive inputs. The CAN receive signal is performed only through the selected input. *Note: In TC1798, only specific combinations of RXSEL are available (see also **"Receive Input Selection" on Page 24-209**).*
LBM	8	rw	**Loop-Back Mode** 0_B Loop-Back Mode is disabled. 1_B Loop-Back Mode is enabled. This node is connected to an internal (virtual) loop-back CAN bus. All CAN nodes which are in Loop-Back Mode are connected to this virtual CAN bus so that they can communicate with each other internally. The external transmit line is forced recessive in Loop-Back Mode.
0	[7:3], [31:9]	r	**Reserved** Read as 0; should be written with 0.

The Node Bit Timing Register NBTRx contains all parameters to set up the bit timing for the CAN transfer. NBTRx can be written only if bit NCRx.CCE is set.

NBTRx (x = 0-3)
Node x Bit Timing Register **(210_H+x*100_H)** **Reset Value: 0000 0000_H**

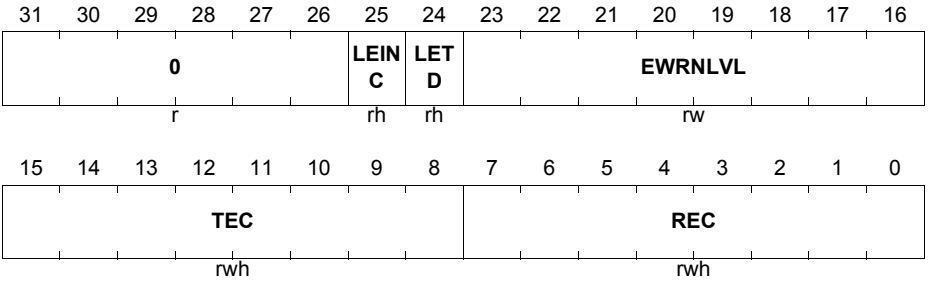


Field	Bits	Type	Description
BRP	[5:0]	rw	**Baud Rate Prescaler** The duration of one time quantum is given by (BRP + 1) clock cycles if DIV8 = 0. The duration of one time quantum is given by 8 × (BRP + 1) clock cycles if DIV8 = 1.
SJW	[7:6]	rw	**(Re) Synchronization Jump Width** (SJW + 1) time quanta are allowed for re-synchronization.
TSEG1	[11:8]	rw	**Time Segment Before Sample Point** (TSEG1 + 1) time quanta is the user-defined nominal time between the end of the synchronization segment and the sample point. It includes the propagation segment, which takes into account signal propagation delays. The time segment may be lengthened due to re-synchronization. Valid values for TSEG1 are 2 to 15.
TSEG2	[14:12]	rw	**Time Segment After Sample Point** (TSEG2 + 1) time quanta is the user-defined nominal time between the sample point and the start of the next synchronization segment. It may be shortened due to re-synchronization. Valid values for TSEG2 are 1 to 7.

Field	Bits	Type	Description
DIV8	15	rw	**Divide Prescaler Clock by 8** 0_B A time quantum lasts (BRP+1) clock cycles. 1_B A time quantum lasts 8 × (BRP+1) clock cycles.
0	[31:16]	r	**Reserved** Read as 0; should be written with 0.

The Node Error Counter Register NECNTx contains the CAN receive and transmit error counter as well as some additional bits to ease error analysis. NECNTx can be written only if bit NCRx.CCE is set.

NECNTx (x = 0-3)
Node x Error Counter Register (214_H+x*100_H) Reset Value: 0060 0000_H

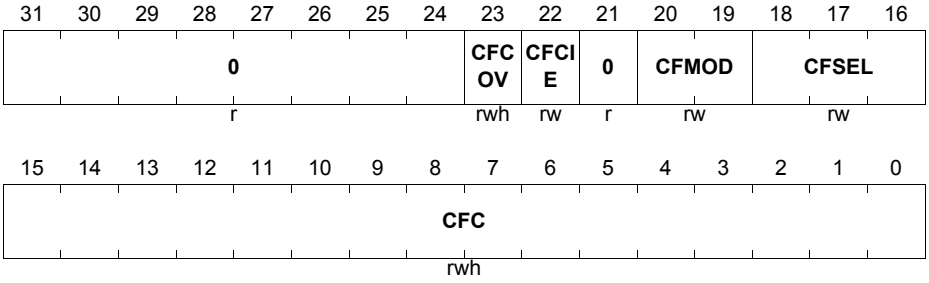


Field	Bits	Type	Description
REC	[7:0]	rwh	**Receive Error Counter** Bit field REC contains the value of the receive error counter of CAN node x.
TEC	[15:8]	rwh	**Transmit Error Counter** Bit field TEC contains the value of the transmit error counter of CAN node x.
EWRNLVL	[23:16]	rw	**Error Warning Level** Bit field EWRNLVL determines the threshold value (warning level, default 96) to be reached in order to set the corresponding error warning bit EWRN.
LETD	24	rh	**Last Error Transfer Direction** 0_B The last error occurred while the CAN node x was receiver (REC has been incremented). 1_B The last error occurred while the CAN node x was transmitter (TEC has been incremented).
LEINC	25	rh	**Last Error Increment** 0_B The last error led to an error counter increment of 1. 1_B The last error led to an error counter increment of 8.

Field	Bits	Type	Description
0	[31:26]	r	**Reserved** Read as 0; should be written with 0.

The Node Frame Counter Register NFCRx contains the actual value of the frame counter as well as control and status bits of the frame counter.

NFCRx (x = 0-3)
Node x Frame Counter Register (218_H+x*100_H) **Reset Value: 0000 0000_H**



Field	Bits	Type	Description
CFC	[15:0]	rwh	**CAN Frame Counter** In Frame Count Mode (CFMOD = 00_B), this bit field contains the frame count value. In Time Stamp Mode (CFMOD = 01_B), this bit field contains the captured bit time count value, captured with the start of a new frame. In all Bit Timing Analysis Modes (CFMOD = 10_B), CFC always displays the number of f_{CLC} clock cycles (measurement result) minus 1. Example: a CFC value of 34 in measurement mode CFSEL = 000_B means that 35 f_{CLC} clock cycles have been elapsed between the most recent two dominant edges on the receive input.

Field	Bits	Type	Description
CFSEL	[18:16]	rw	**CAN Frame Count Selection** This bit field selects the function of the frame counter for the chosen frame count mode. **Frame Count Mode** Bit 0 If Bit 0 of CFSEL is set, then CFC is incremented each time a foreign frame (i.e. a frame not matching to a message object) has been received on the CAN bus. Bit 1 If Bit 1 of CFSEL is set, then CFC is incremented each time a frame matching to a message object has been received on the CAN bus. Bit 2 If Bit 2 of CFSEL is set, then CFC is incremented each time a frame has been transmitted successfully by the node. **Time Stamp Mode** 000_B The frame counter is incremented (internally) at the beginning of a new bit time. The value is sampled during the SOF bit of a new frame. The sampled value is visible in the CFC field. **Bit Timing Mode** The available bit timing measurement modes are shown in Table 24-9. If CFCIE is set, then an interrupt on request node x (where x is the CAN node number) is generated with a CFC update.
CFMOD	[20:19]	rw	**CAN Frame Counter Mode** This bit field determines the operation mode of the frame counter. 00_B Frame Count Mode: The frame counter is incremented upon the reception and transmission of frames. 01_B Time Stamp Mode: The frame counter is used to count bit times. 10_B Bit Timing Mode: The frame counter is used for analysis of the bit timing.

Field	Bits	Type	Description
CFCIE	22	rw	**CAN Frame Count Interrupt Enable** CFCIE enables the CAN frame counter overflow interrupt of CAN node x. 0_B CAN frame counter overflow interrupt is disabled. 1_B CAN frame counter overflow interrupt is enabled. Bit field NIPRx.CFCINP selects the interrupt output line that is activated at this type of interrupt.
CFCOV	23	rwh	**CAN Frame Counter Overflow Flag** Flag CFCOV is set upon a frame counter overflow (transition from $FFFF_H$ to 0000_H). In bit timing analysis mode, CFCOV is set upon an update of CFC. An interrupt request is generated if CFCIE = 1. 0_B No overflow has occurred since last flag reset. 1_B An overflow has occurred since last flag reset. CFCOV must be reset by software.
0	21, [31:24]	r	**Reserved** Read as 0; should be written with 0.

Bit Timing Analysis Modes

Table 24-9 Bit Timing Analysis Modes (CFMOD = 10)

CFSEL	Measurement
000_B	Whenever a dominant edge (transition from 1 to 0) is monitored on the receive input, the time (measured in clock cycles) between this edge and the most recent dominant edge is stored in CFC.
001_B	Whenever a recessive edge (transition from 0 to 1) is monitored on the receive input the time (measured in clock cycles) between this edge and the most recent dominant edge is stored in CFC.
010_B	Whenever a dominant edge is received as a result of a transmitted dominant edge, the time (clock cycles) between both edges is stored in CFC.
011_B	Whenever a recessive edge is received as a result of a transmitted recessive edge, the time (clock cycles) between both edges is stored in CFC.
100_B	Whenever a dominant edge that qualifies for synchronization is monitored on the receive input, the time (measured in clock cycles) between this edge and the most recent sample point is stored in CFC.

Table 24-9 Bit Timing Analysis Modes (CFMOD = 10) (cont'd)

CFSEL	Measurement
101_B	With each sample point, the time (measured in clock cycles) between the start of the new bit time and the start of the previous bit time is stored in CFC[11:0]. Additional information is written to CFC[15:12] at each sample point: CFC[15]: Transmit value of actual bit time CFC[14]: Receive sample value of actual bit time CFC[13:12]: CAN bus information (see **Table 24-10**)
110_B	Reserved, do not use this combination.
111_B	Reserved, do not use this combination.

Table 24-10 CAN Bus State Information

CFC[13:12]	CAN Bus State
00_B	**NoBit** The CAN bus is idle, performs bit (de-) stuffing or is in one of the following frame segments: SOF, SRR, CRC, delimiters, first 6 EOF bits, IFS.
01_B	**NewBit** This code represents the first bit of a new frame segment. The current bit is the first bit in one of the following frame segments: Bit 10 (MSB) of standard ID (transmit only), RTR, reserved bits, IDE, DLC(MSB), bit 7 (MSB) in each data byte and the first bit of the ID extension.
10_B	**Bit** This code represents a bit inside a frame segment with a length of more than one bit (not the first bit of those frame segments that is indicated by NewBit). The current bit is processed within one of the following frame segments: ID bits (except first bit of standard ID for transmission and first bit of ID extension), DLC (3 LSB) and bits 6-0 in each data byte.
11_B	**Done** The current bit is in one of the following frame segments: Acknowledge slot, last bit of EOF, active/passive-error frame, overload frame. Two or more directly consecutive Done codes signal an Error Frame.

24.6.3 Message Object Registers

The Message Object Control Register MOCTRn and the Message Object Status Register MOSTATn are located at the same address offset within a message object address block (offset address $1C_H$). The MOCTRn is a write-only register that makes it possible to set/reset CAN transfer related control bits through software.

MOCTR0
Message Object 0 Control Register ($101C_H$) **Reset Value: $0100\ 0000_H$**
MOCTR127
Message Object 127 Control Register($1FFC_H$) **Reset Value: $7F7E\ 0000_H$**
MOCTRn (n = 1-126)
Message Object n Control Register
($101C_H+n*20_H$)
Reset Value: $((n+1)*01000000_H)+((n-1)*00010000_H)$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0				SET DIR	SET TXEN1	SET TXEN0	SET TXRQ	SET RXEN	SET RTSEL	SET MSGVAL	SET MSGLST	SET NEWDAT	SET RXUPD	SET TXPND	SET RXPND
w				w	w	w	w	w	w	w	w	w	w	w	w

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0				RES DIR	RES TXEN1	RES TXEN0	RES TXRQ	RES RXEN	RES RTSEL	RES MSGVAL	RES MSGLST	RES NEWDAT	RES RXUPD	RES TXPND	RES RXPND
w				w	w	w	w	w	w	w	w	w	w	w	w

Field	Bits	Type	Description
RESRXPND, SETRXPND	0, 16	w	**Reset/Set Receive Pending** These bits control the set/reset condition for RXPND (see **Table 24-11**).
RESTXPND, SETTXPND	1, 17	w	**Reset/Set Transmit Pending** These bits control the set/reset condition for TXPND (see **Table 24-11**).
RESRXUPD, SETRXUPD	2, 18	w	**Reset/Set Receive Updating** These bits control the set/reset condition for RXUPD (see **Table 24-11**).
RESNEWDAT, SETNEWDAT	3, 19	w	**Reset/Set New Data** These bits control the set/reset condition for NEWDAT (see **Table 24-11**).

Field	Bits	Type	Description
RESMSGLST, SETMSGLST	4, 20	w	**Reset/Set Message Lost** These bits control the set/reset condition for MSGLST (see **Table 24-11**).
RESMSGVAL, SETMSGVAL	5, 21	w	**Reset/Set Message Valid** These bits control the set/reset condition for MSGVAL (see **Table 24-11**).
RESRTSEL, SETRTSEL	6, 22	w	**Reset/Set Receive/Transmit Selected** These bits control the set/reset condition for RTSEL (see **Table 24-11**).
RESRXEN, SETRXEN	7, 23	w	**Reset/Set Receive Enable** These bits control the set/reset condition for RXEN (see **Table 24-11**).
RESTXRQ, SETTXRQ	8, 24	w	**Reset/Set Transmit Request** These bits control the set/reset condition for TXRQ (see **Table 24-11**).
RESTXEN0, SETTXEN0	9, 25	w	**Reset/Set Transmit Enable 0** These bits control the set/reset condition for TXEN0 (see **Table 24-11**).
RESTXEN1, SETTXEN1	10, 26	w	**Reset/Set Transmit Enable 1** These bits control the set/reset condition for TXEN1 (see **Table 24-11**).
RESDIR, SETDIR	11, 27	w	**Reset/Set Message Direction** These bits control the set/reset condition for DIR (see **Table 24-11**).
0	[15:12], [31:28]	w	**Reserved** Should be written with 0.

Table 24-11 Reset/Set Conditions for Bits in Register MOCTRn

RESy Bit[1)]	SETy Bit	Action on Write
Write 0	Write 0	Leave element unchanged
	No write	
No write	Write 0	
Write 1	Write 1	

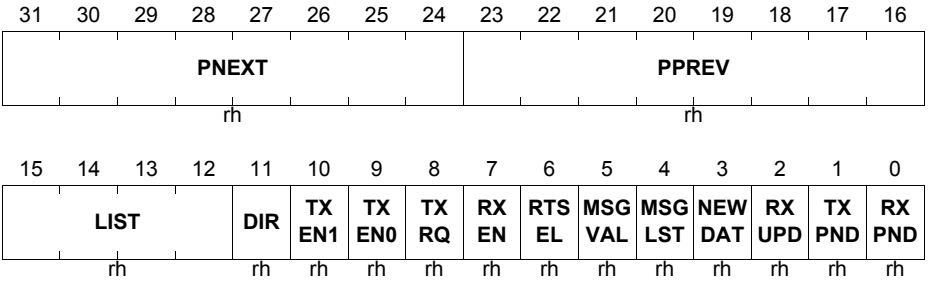
Table 24-11 Reset/Set Conditions for Bits in Register MOCTRn (cont'd)

RESy Bit[1)]	SETy Bit	Action on Write
Write 1	Write 0	Reset element
	No write	
Write 0	Write 1	Set element
No write		

1) The parameter "y" stands for the second part of the bit name ("RXPND", "TXPND", … up to "DIR").

The MOSTATn is a read-only register that indicates message object list status information such as the number of the current message object predecessor and successor message object, as well as the list number to which the message object is assigned.

MOSTAT0
Message Object 0 Status Register ($101C_H$) Reset Value: $0100\ 0000_H$
MOSTAT127
Message Object 127 Status Register ($1FFC_H$) Reset Value: $7F7E\ 0000_H$
MOSTATn (n = 1-126)
Message Object n Status Register
($101C_H+n*20_H$)
Rest Value: $((n+1)*01000000_H)+((n-1)*00010000_H)$



Field	Bits	Type	Description
RXPND	0	rh	**Receive Pending** 0_B No CAN message has been received. 1_B A CAN message has been received by the message object n, either directly or via gateway copy action. RXPND is not reset by hardware but must be reset by software.
TXPND	1	rh	**Transmit Pending** 0_B No CAN message has been transmitted. 1_B A CAN message from message object n has been transmitted successfully over the CAN bus. TXPND is reset by hardware but must be reset by software.

Field	Bits	Type	Description
RXUPD	2	rh	**Receive Updating** 0_B No receive update ongoing. 1_B Message identifier, DLC, and data of the message object are currently updated.
NEWDAT	3	rh	**New Data** 0_B No update of the message object n since last flag reset. 1_B Message object n has been updated. NEWDAT is set by hardware after a received CAN frame has been stored in message object n. NEWDAT is cleared by hardware when a CAN transmission of message object n has been started. NEWDAT should be set by software after the new transmit data has been stored in message object n to prevent the automatic reset of TXRQ at the end of an ongoing transmission.
MSGLST	4	rh	**Message Lost** 0_B No CAN message is lost. 1_B A CAN message is lost because NEWDAT has become set again when it has already been set.
MSGVAL	5	rh	**Message Valid** 0_B Message object n is not valid. 1_B Message object n is valid. Only a valid message object takes part in CAN transfers.

Field	Bits	Type	Description
RTSEL	6	rh	**Receive/Transmit Selected** 0_B Message object n is not selected for receive or transmit operation. 1_B Message object n is selected for receive or transmit operation. **Frame Reception:** RTSEL is set by hardware when message object n has been identified for storage of a CAN frame that is currently received. Before a received frame becomes finally stored in message object n, a check is performed to determine if RTSEL is set. Thus the CPU can suppress a scheduled frame delivery to this message object n by clearing RTSEL by software. **Frame Transmission:** RTSEL is set by hardware when message object n has been identified to be transmitted next. A check is performed to determine if RTSEL is still set before message object n is actually set up for transmission and bit NEWDAT is cleared. It is also checked that RTSEL is still set before its message object n is verified due to the successful transmission of a frame. RTSEL needs to be checked only when the context of message object n changes, and a conflict with an ongoing frame transfer shall be avoided. In all other cases, RTSEL can be ignored. RTSEL has no impact on message acceptance filtering. RTSEL is not cleared by hardware.
RXEN	7	rh	**Receive Enable** 0_B Message object n is not enabled for frame reception. 1_B Message object n is enabled for frame reception. RXEN is evaluated for receive acceptance filtering only.

Field	Bits	Type	Description
TXRQ	8	rh	**Transmit Request** 0_B No transmission of message object n is requested. 1_B Transmission of message object n on the CAN bus is requested. The transmit request becomes valid only if TXRQ, TXEN0, TXEN1 and MSGVAL are set. TXRQ is set by hardware if a matching Remote Frame has been received correctly. TXRQ is reset by hardware if message object n has been transmitted successfully and NEWDAT is not set again by software.
TXEN0	9	rh	**Transmit Enable 0** 0_B Message object n is not enabled for frame transmission. 1_B Message object n is enabled for frame transmission. Message object n can be transmitted only if both bits, TXEN0 and TXEN1, are set. The user may clear TXEN0 in order to inhibit the transmission of a message that is currently updated, or to disable automatic response of Remote Frames.
TXEN1	10	rh	**Transmit Enable 1** 0_B Message object n is not enabled for frame transmission. 1_B Message object n is enabled for frame transmission. Message object n can be transmitted only if both bits, TXEN0 and TXEN1, are set. TXEN1 is used by the MultiCAN module for selecting the active message object in the Transmit FIFOs.

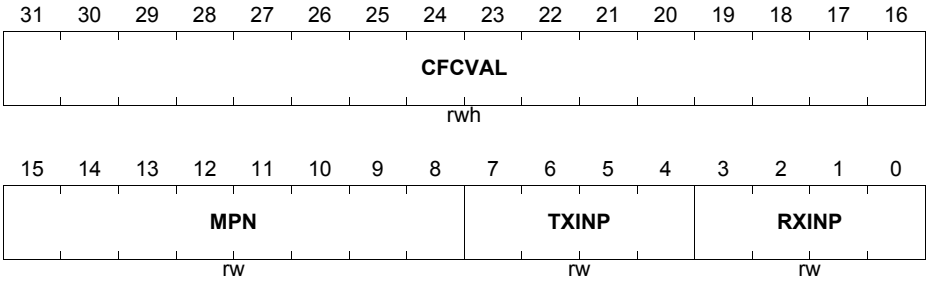
Field	Bits	Type	Description
DIR	11	rh	**Message Direction** 0_B Receive Object selected: With TXRQ = 1, a Remote Frame with the identifier of message object n is scheduled for transmission. On reception of a Data Frame with matching identifier, the message is stored in message object n. 1_B Transmit Object selected: If TXRQ = 1, message object n is scheduled for transmission of a Data Frame. On reception of a Remote Frame with matching identifier, bit TXRQ is set.
LIST	[15:12]	rh	**List Allocation** LIST indicates the number of the message list to which message object n is allocated. LIST is updated by hardware when the list allocation of the object is modified by a panel command.
PPREV	[23:16]	rh	**Pointer to Previous Message Object** PPREV holds the message object number of the previous message object in a message list structure.
PNEXT	[31:24]	rh	**Pointer to Next Message Object** PNEXT holds the message object number of the next message object in a message list structure.

Table 24-12 MOSTATn Reset Values

Message Object	PNEXT	PPREV	Reset Value
0	1	0	$0100\ 0000_H$
1	2	0	$0200\ 0000_H$
2	3	1	$0301\ 0000_H$
3	4	2	$0402\ 0000_H$
…	…	…	…
60	61	59	$3D3B\ 0000_H$
61	62	60	$3E3C\ 0000_H$
62	63	61	$3F3D\ 0000_H$
63	63	62	$3F3E\ 0000_H$

The Message Object Interrupt Pointer Register MOIPRn holds the message interrupt pointers, the message pending number, and the frame counter value of message object n.

MOIPRn (n = 0-127)
Message Object n Interrupt Pointer Register
(1008_H+n*20_H) **Reset Value: 0000 0000_H**



Field	Bits	Type	Description
RXINP	[3:0]	rw	**Receive Interrupt Node Pointer** RXINP selects the interrupt output line INT_Om (m = 0-15) for a receive interrupt event of message object n. RXINP can also be taken for message pending bit selection (see **Page 24-44**). 0000_B Interrupt output line INT_O0 is selected. 0001_B Interrupt output line INT_O1 is selected. …$_B$ … 1110_B Interrupt output line INT_O14 is selected. 1111_B Interrupt output line INT_O15 is selected.
TXINP	[7:4]	rw	**Transmit Interrupt Node Pointer** TXINP selects the interrupt output line INT_Om (m = 0-15) for a transmit interrupt event of message object n. TXINP can also be taken for message pending bit selection (see **Page 24-44**). 0000_B Interrupt output line INT_O0 is selected. 0001_B Interrupt output line INT_O1 is selected. …$_B$ … 1110_B Interrupt output line INT_O14 is selected. 1111_B Interrupt output line INT_O15 is selected.

Field	Bits	Type	Description
MPN	[15:8]	rw	**Message Pending Number** This bit field selects the bit position of the bit in the Message Pending Register that is set upon a message object n receive/transmit interrupt.
CFCVAL	[31:16]	rwh	**CAN Frame Counter Value** When a message is stored in message object n or message object n has been successfully transmitted, the CAN frame counter value NFCRx.CFC is then copied to CFCVAL.

The Message Object Function Control Register MOFCRn contains bits that select and configure the function of the message object. It also holds the CAN data length code.

MOFCRn (n = 0-127)
Message Object n Function Control Register
(1000_H+n*20_H) **Reset Value: 0000 0000_H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0				DLC				STT	SDT	RMM	FRR EN	0	OVIE	TXIE	RXIE
rw				rwh				rw	rw	rw	rw	rw	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0				DAT C	DLC C	IDC	GDF S	0				MMC			
rw				rw	rw	rw	rw	rw				rw			

Field	Bits	Type	Description
MMC	[3:0]	rw	**Message Mode Control** MMC controls the message mode of message object n. 0000_B Standard Message Object 0001_B Receive FIFO Base Object 0010_B Transmit FIFO Base Object 0011_B Transmit FIFO Slave Object 0100_B Gateway Source Object $..._B$ Reserved
GDFS	8	rw	**Gateway Data Frame Send** 0_B TXRQ is unchanged in the destination object. 1_B TXRQ is set in the gateway destination object after the internal transfer from the gateway source to the gateway destination object. Applicable only to a gateway source object; ignored in other nodes.

Field	Bits	Type	Description
IDC	9	rw	**Identifier Copy** 0_B The identifier of the gateway source object is not copied. 1_B The identifier of the gateway source object (after storing the received frame in the source) is copied to the gateway destination object. Applicable only to a gateway source object; ignored in other nodes.
DLCC	10	rw	**Data Length Code Copy** 0_B Data length code is not copied. 1_B Data length code of the gateway source object (after storing the received frame in the source) is copied to the gateway destination object. Applicable only to a gateway source object; ignored in other nodes.
DATC	11	rw	**Data Copy** 0_B Data fields are not copied. 1_B Data fields in registers MODATALn and MODATAHn of the gateway source object (after storing the received frame in the source) are copied to the gateway destination. Applicable only to a gateway source object; ignored in other nodes.
RXIE	16	rw	**Receive Interrupt Enable** RXIE enables the message receive interrupt of message object n. This interrupt is generated after reception of a CAN message (independent of whether the CAN message is received directly or indirectly via a gateway action). 0_B Message receive interrupt is disabled. 1_B Message receive interrupt is enabled. Bit field MOIPRn.RXINP selects the interrupt output line which becomes activated at this type of interrupt.

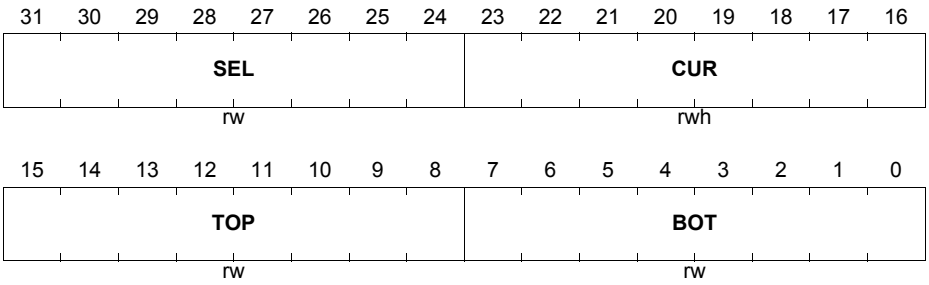
Field	Bits	Type	Description
TXIE	17	rw	**Transmit Interrupt Enable** TXIE enables the message transmit interrupt of message object n. This interrupt is generated after the transmission of a CAN message. 0_B Message transmit interrupt is disabled. 1_B Message transmit interrupt is enabled. Bit field MOIPRn.TXINP selects the interrupt output line which becomes activated at this type of interrupt.
OVIE	18	rw	**Overflow Interrupt Enable** OVIE enables the FIFO full interrupt of message object n. This interrupt is generated when the pointer to the current message object (CUR) reaches the value of SEL in the FIFO/Gateway Pointer Register. 0_B FIFO full interrupt is disabled. 1_B FIFO full interrupt is enabled. If message object n is a Receive FIFO base object, bit field MOIPRn.TXINP selects the interrupt output line which becomes activated at this type of interrupt. If message object n is a Transmit FIFO base object, bit field MOIPRn.RXINP selects the interrupt output line which becomes activated at this type of interrupt. For all other message object modes, bit OVIE has no effect.
FRREN	20	rw	**Foreign Remote Request Enable** Specifies whether the TXRQ bit is set in message object n or in a foreign message object referenced by the pointer CUR. 0_B TXRQ of message object n is set on reception of a matching Remote Frame. 1_B TXRQ of the message object referenced by the pointer CUR is set on reception of a matching Remote Frame.

Field	Bits	Type	Description
RMM	21	rw	**Transmit Object Remote Monitoring** 0_B Remote monitoring is disabled: Identifier, IDE bit, and DLC of message object n remain unchanged upon the reception of a matching Remote Frame. 1_B Remote monitoring is enabled: Identifier, IDE bit, and DLC of a matching Remote Frame are copied to transmit object n in order to monitor incoming Remote Frames. Bit RMM applies only to transmit objects and has no effect on receive objects.
SDT	22	rw	**Single Data Transfer** If SDT = 1 and message object n is not a FIFO base object, then MSGVAL is reset when this object has taken part in a successful data transfer (receive or transmit). If SDT = 1 and message object n is a FIFO base object, then MSGVAL is reset when the pointer to the current object CUR reaches the value of SEL in the FIFO/Gateway Pointer Register. With SDT = 0, bit MSGVAL is not affected.
STT	23	rw	**Single Transmit Trial** If this bit is set, then TXRQ is cleared on transmission start of message object n. Thus, no transmission retry is performed in case of transmission failure.
DLC	[27:24]	rwh	**Data Length Code** Bit field determines the number of data bytes for message object n. Valid values for DLC are 0 to 8. A value of DLC > 8 results in a data length of 8 data bytes. If a frame with DLC > 8 is received, the received value is stored in the message object.

Field	Bits	Type	Description
MSC	[31:28]	rwh	**Message Status Count (TTCAN only)** MSC can have values between 0000_B and 0111_B. An increment of MSC = 0111_B results in MSC = 0111_B (no overflow). A decrement of MSC = 0000_B results in MSC = 0000_B (no underflow). **Transmission:** When message object n is scheduled for transmission in an exclusive time window and the transmission is successful within this time window and the TTCAN is in error state S0 or S1, MSC is decremented by one. If the transmission fails, bit field MSC is incremented by one. If the TTCAN is in error state S2 and detects CAN bus-idle during the transmit enable window for message object n, MSC is decremented by one (although this message object is not transmitted). **Reception:** When message object n is scheduled for reception in an exclusive time window and the reception is successful within this time window, MSC is decremented by one. If the reception does not take place within this time window, MSC is incremented by one. If TTCAN function is not available/enabled, bit field MSC is unchanged.
0	[7:4], [15:12], 19	rw	**Reserved** Read as 0 after reset; value last written is read back; should be written with 0.

The Message Object FIFO/Gateway Pointer register MOFGPRn contains a set of message object link pointers that are used for FIFO and gateway operations.

MOFGPRn (n = 0-127)
Message Object n FIFO/Gateway Pointer Register
(1004_H+n*20_H) **Reset Value: 0000 0000_H**



Field	Bits	Type	Description
BOT	[7:0]	rw	**Bottom Pointer** Bit field BOT points to the first element in a FIFO structure.
TOP	[15:8]	rw	**Top Pointer** Bit field TOP points to the last element in a FIFO structure.
CUR	[23:16]	rwh	**Current Object Pointer** Bit field CUR points to the actual target object within a FIFO/Gateway structure. After a FIFO/gateway operation CUR is updated with the message number of the next message object in the list structure (given by PNEXT of the message control register) until it reaches the FIFO top element (given by TOP) when it is reset to the bottom element (given by BOT).
SEL	[31:24]	rw	**Object Select Pointer** Bit field SEL is the second (software) pointer to complement the hardware pointer CUR in the FIFO structure. SEL is used for monitoring purposes (FIFO interrupt generation).

Message Object n Acceptance Mask Register MOAMRn contains the mask bits for the acceptance filtering of the message object n.

MOAMRn (n = 0-127)
Message Object n Acceptance Mask Register
($100C_H$+n*20_H) **Reset Value: 3FFF FFFF$_H$**

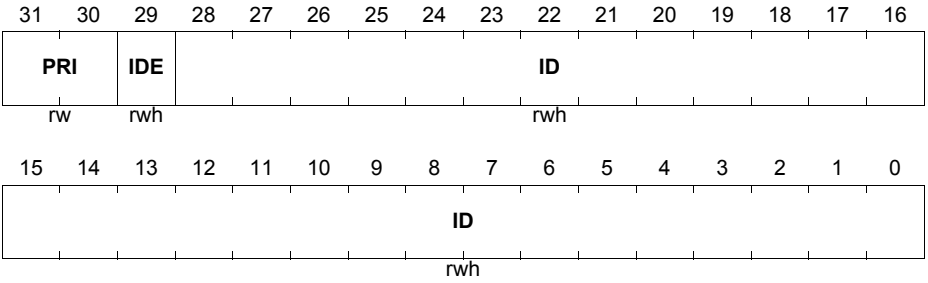
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0		MIDE	AM												
rw		rw	rw												

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AM															
rw															

Field	Bits	Type	Description
AM	[28:0]	rw	**Acceptance Mask for Message Identifier** Bit field AM is the 29-bit mask for filtering incoming messages with standard identifiers (AM[28:18]) or extended identifiers (AM[28:0]). For standard identifiers, bits AM[17:0] are “don’t care”. For TTC based transmit acceptance filtering (MOARn.PRI = 00_B) register MOAMRn is used to specify the transmit column/row in which this message object may be transmitted in a time-triggered communication. It is then no longer used as an identifier mask. This means that all identifier bits are used for receive acceptance filtering. In this case AMR contains the following information: • MOAMR[5:0] = CYCLE • MOAMR[13:8] = MCYCLE • MOAMR[21:16] = COLUMN • MOAMR[29:24] = MCOLUMN where CYCLE is the cycle count (transmit row) and COLUMN is the transmission column of the system matrix. MCYCLE and MCOLUMN are acceptance masks for matching CYCLE and COLUMN against the actual position within the system matrix of the time-triggered communication network. Message object n may be transmitted only if CYCLE and COLUMN match the actual matrix position (given by CYCTMR.BCC and CYCTMR.CSM). If more than one object with valid transmit request matches a given matrix position, the actually transmitted message object is chosen by list order.
MIDE	29	rw	**Acceptance Mask Bit for Message IDE Bit** 0_B Message object n accepts the reception of both, standard and extended frames. 1_B Message object n receives frames only with matching IDE bit.
0	[31:30]	rw	**Reserved** Read as 0 after reset; value last written is read back; should be written with 0.

Message Object n Arbitration Register MOARn contains the CAN identifier of the message object.

MOARn (n = 0-127)
Message Object n Arbitration Register
(1018_H+n*20_H) **Reset Value: 0000 0000_H**



Field	Bits	Type	Description
ID	[28:0]	rwh	**CAN Identifier of Message Object n** Identifier of a standard message (ID[28:18]) or an extended message (ID[28:0]). For standard identifiers, bits ID[17:0] are “don’t care”.
IDE	29	rwh	**Identifier Extension Bit of Message Object n** 0_B Message object n handles standard frames with 11-bit identifier. 1_B Message object n handles extended frames with 29-bit identifier.

Field	Bits	Type	Description
PRI	[31:30]	rw	**Priority Class** PRI assigns one of the four priority classes 0, 1, 2, 3 to message object n. A lower PRI number defines a higher priority. Message objects with lower PRI value always win acceptance filtering for frame reception and transmission over message objects with higher PRI value. Acceptance filtering based on identifier/mask and list position is performed only between message objects of the same priority class. PRI also determines the acceptance filtering method for transmission: 00_B Time-Triggered CAN (TTCAN): The Message Object Mask Register specifies the position(s) within the transmission matrix at which the message object n may be transmitted. Transmit acceptance filtering is based on the list order. This means that message object n is considered for transmission only if there is no other message object with valid transmit request (MSGVAL & TXEN0 & TXEN1 = 1) that matches the actual position within the transmission matrix somewhere before this object in the list. 01_B Transmit acceptance filtering is based on the list order. This means that message object n is considered for transmission only if there is no other message object with valid transmit request (MSGVAL & TXEN0 & TXEN1 = 1) somewhere before this object in the list. 10_B Transmit acceptance filtering is based on the CAN identifier. This means, message object n is considered for transmission only if there is no other message object with higher priority identifier + IDE + DIR (with respect to CAN arbitration rules) somewhere in the list (see **Table 24-13**). 11_B Transmit acceptance filtering is based on the list order (as PRI = 01_B).

Transmit Priority of Msg. Objects based on CAN Arbitration Rules

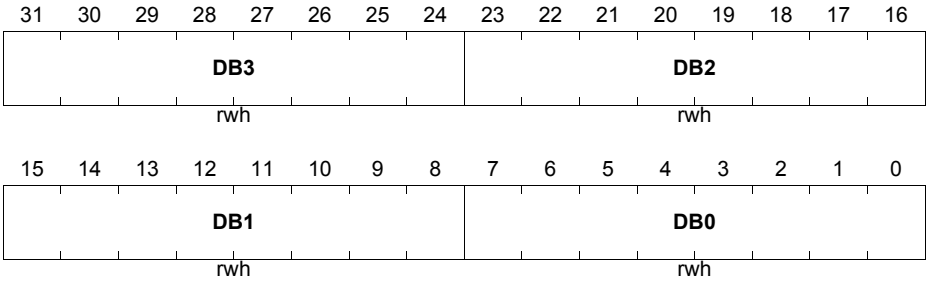
Table 24-13 Transmit Priority of Msg. Objects Based on CAN Arbitration Rules

Settings of Arbitrarily Chosen Message Objects A and B, (A has higher transmit priority than B)	Comment
A.MOAR[28:18] < B.MOAR[28:18] (11-bit standard identifier of A less than 11-bit standard identifier of B)	Messages with lower standard identifier have higher priority than messages with higher standard identifier. MOAR[28] is the most significant bit (MSB) of the standard identifier. MOAR[18] is the least significant bit of the standard identifier.
A.MOAR[28:18] = B.MOAR[28:18] A.MOAR.IDE = 0 (send Standard Frame) B.MOAR.IDE = 1 (send Extended Frame)	Standard Frames have higher transmit priority than Extended Frames with equal standard identifier.
A.MOAR[28:18] = B.MOAR[28:18] A.MOAR.IDE = B.MOAR.IDE = 0 A.MOCTR.DIR = 1 (send Data Frame) B.MOCTR.DIR = 0 (send Remote Fame)	Standard Data Frames have higher transmit priority than standard Remote Frames with equal identifier.
A.MOAR[28:0] = B.MOAR[28:0] A.MOAR.IDE = B.MOAR.IDE = 1 A.MOCTR.DIR = 1 (send Data Frame) B.MOCTR.DIR = 0 (send Remote Frame)	Extended Data Frames have higher transmit priority than Extended Remote Frames with equal identifier.
A.MOAR[28:0] < B.MOAR[28:0] A.MOAR.IDE = B.MOAR.IDE = 1 (29-bit identifier)	Extended Frames with lower identifier have higher transmit priority than Extended Frames with higher identifier. MOAR[28] is the most significant bit (MSB) of the overall identifier (standard identifier MOAR[28:18] and identifier extension MOAR[17:0]). MOAR[0] is the least significant bit (LSB) of the overall identifier.

Message Object n Data Register Low MODATALn contains the lowest four data bytes of message object n. Unused data bytes are set to zero upon reception and ignored for transmission.

MODATALn (n = 0-127)
Message Object n Data Register Low

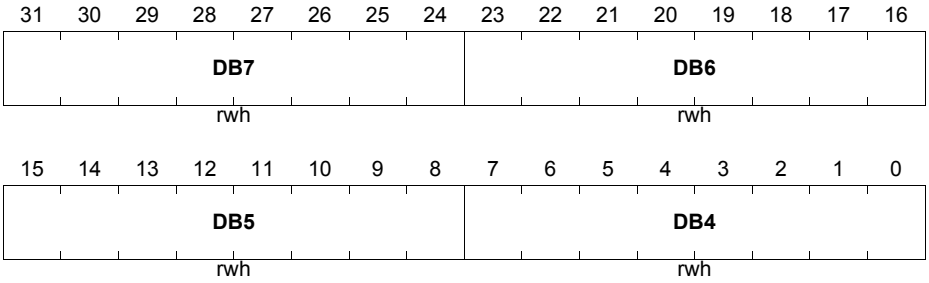
(1010_H+n*20_H) **Reset Value: 0000 0000_H**



Field	Bits	Type	Description
DB0	[7:0]	rwh	**Data Byte 0 of Message Object n**
DB1	[15:8]	rwh	**Data Byte 1 of Message Object n**
DB2	[23:16]	rwh	**Data Byte 2 of Message Object n**
DB3	[31:24]	rwh	**Data Byte 3 of Message Object n**

Message Object n Data Register High MODATAH contains the highest four data bytes of message object n. Unused data bytes are set to zero upon reception and ignored for transmission.

MODATAHn (n = 0-127)
Message Object n Data Register High
(1014_H+n*20_H) **Reset Value: 0000 0000_H**



Field	Bits	Type	Description
DB4	[7:0]	rwh	**Data Byte 4 of Message Object n**
DB5	[15:8]	rwh	**Data Byte 5 of Message Object n**
DB6	[23:16]	rwh	**Data Byte 6 of Message Object n**
DB7	[31:24]	rwh	**Data Byte 7 of Message Object n**

24.7 Time-Triggered Extension (TTCAN Controller)

24.7.1 Generation of the Local Time

The Nominal Time Unit (NTU) of the TTCAN controller is generated by the NTU timer with a clock derived from the fractional divider (an NTU timer action takes place with t_q or with a multiple of $1/f_{CAN}$). The sum of the NTU is the local time LT, which is a 16-bit value (to be considered as integer number) and a fractional part LTFR.

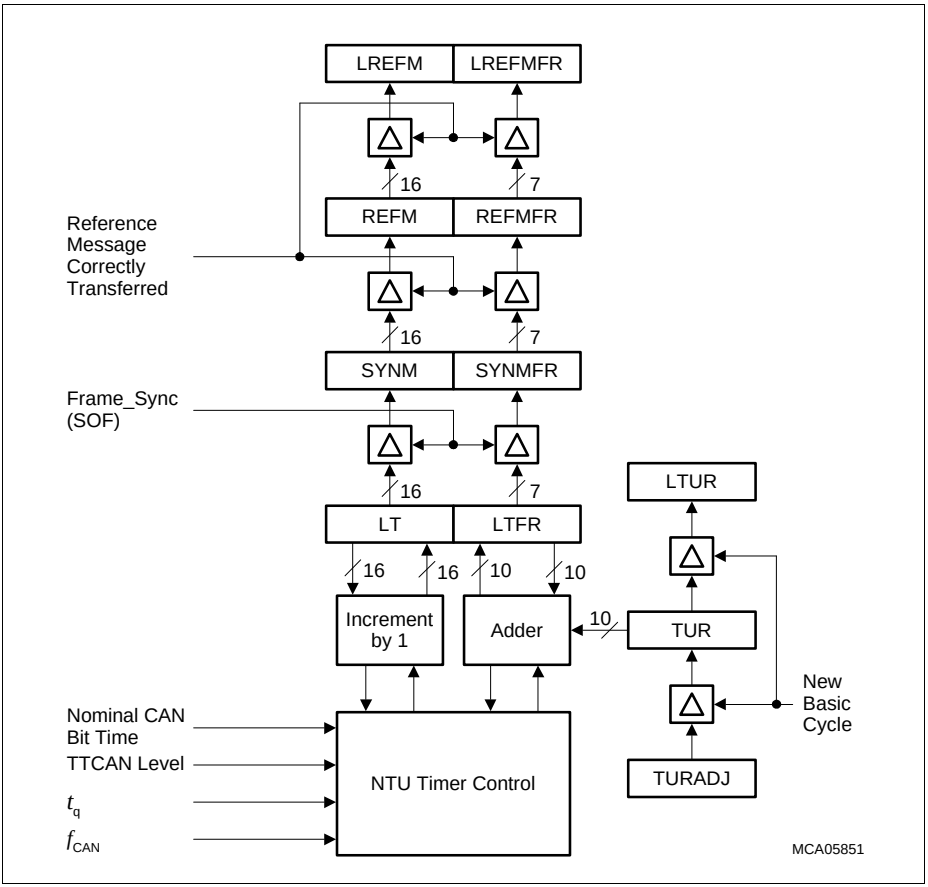


Figure 24-26 Generation of the Local Time

Note: Register LTUR is used for the internal automatic calculation of the new TURADJ value. It is not visible for the user.

In TTCAN level 1, the LT counter is incremented once per CAN bit time. The fractional part LTFR of the local time and the TUR are not taken into account.
In TTCAN level 2, the LT is extended by its fractional part LTFR. The TUR value is added to the LTFR value with the update period t_{upd} in order to generate a new LT value. If an overflow occurs (carry active) after an addition of LTFR and TUR, the value of LT is incremented by 1. As a result, the value of LT can change only in steps of 1, whereas the value of LTFR changes in steps of TUR.

In order to cover a wide range of CAN baud rates with the same counting range of the local timer, the counting can take place every CAN time quantum t_q ($t_{upd} = t_q$). If another resolution of the NTU is desired, the local time generation can also be based on the clock f_{CAN}, divided by a programmable factor that is independent from the CAN bit timing.

After the update period t_{upd} has elapsed N times, the difference in local time dt has elapsed to: dt = TURR.TUR/1024 $\times$ N $\times$ t_{upd}.

24.7.2 Automatic TUR Adjust

It is possible to automatically calculate the new value written to TURADJ for adjusting the correct value for the local time on TTCAN level 2. Each time a new reference message is correctly received, the difference is calculated between the time values in the reference message (GMR) and the previous reference message (LGMR). This difference, divided by the amount of own NTUs for a complete basic cycle multiplied by LTUR, provides the TURADJ value (including fractional parts).

TURADJ = LTUR $\times$ (GM - LGM) / (REFM - LREFM)

The automatic TUR adjust is not made when a discontinuity has been signaled between the reference messages. The automatic calculation of the new value for TURADJ takes place during the basic cycle.

The value of TUR is updated at the beginning of each basic cycle. The new value that is written to TUR to adjust the timing is stored in the bit field TURADJ.

24.7.3 Cycle Time

The cycle time is always positive and represents the time elapsed in the current basic cycle, starting from 0.

24.7.3.1 Local Time and Synchronization Marks

The cycle time is the difference between the local time (stored in bit field LT) and its last reference mark (stored in bit field REFM). The result is available in the bit field CYCTM. The value of the local time LT is captured at the start of each message as a synchronization mark SYNM. If the correctly received message has been a reference

message, the captured value becomes the reference mark REFM. The REFM value of the previous reference mark is stored in LREFM.

The cycle time is still incremented while the reference message is received. After the end of the correctly received reference message, the cycle time takes the value corresponding to the length of this reference message. As a result, the cycle time seems to start from zero each time a reference message starts (= with each new basic cycle).

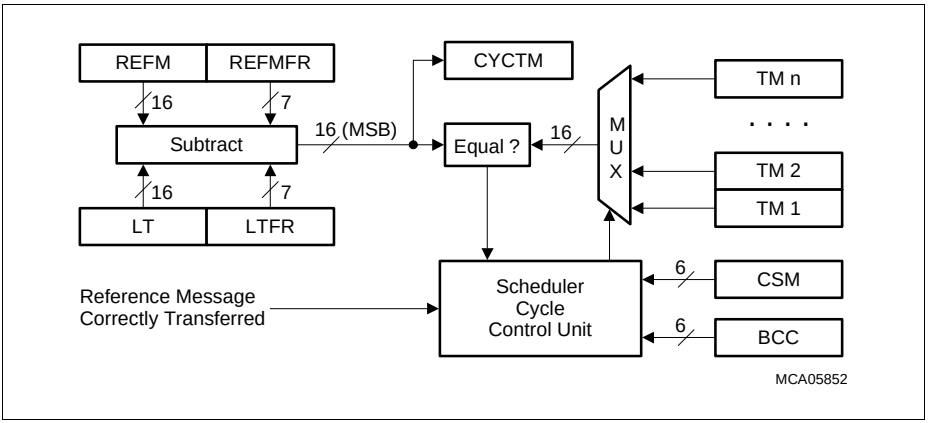


Figure 24-27 Generation of the Cycle Time

The cycle control unit also delivers the values for the basic cycle and matrix cycle handling, and provides the possibility to generate an interrupt if a new basic cycle has started or a new matrix cycle has started. If the TTCAN node receives a reference message, the value for BCC is taken from the reference message.

24.7.3.2 Time Marks

Each time a reference message is received correctly, the cycle control unit starts again comparing the cycle time to the first time mark (TM 1). If one time mark is reached, it continues with the next one. In order to be able to do an “equal-to” comparison, the time marks have to be programmed in increasing order and the first time mark must not be lower than the maximum length of the reference message plus 5 bit times.
The cycle time is used to determine the different columns of the system matrix (CSM = column of the system matrix). These columns are defined by the time marks. These time marks can be programmed and are valid for all columns of the system matrix.
The cycle control unit also checks the number of the current basic cycle that is indicated by the basic cycle count BCC. The value of BCC and the value of CSM, taken together, clearly identify each time window in the matrix cycle.

In master mode, the value BCC is transmitted as part of the reference message.

24.7.3.3 Watch Trigger

The watch trigger is used to check if the elapsed time since the last reference message was received is too long. This is done by comparing the programmed watch trigger value to the cycle time. This information can generate an interrupt to the system. The watch trigger value is defined by the scheduler entry for the end of the basic cycle.

24.7.4 Master Reference Mark (Level 2 only)

The time master sends the sum of its reference mark SYNM (integer part) and SYNMFR (fractional part) and its local offset LOF (integer part) and LOFFR (fractional part) as master reference mark (MRM), which is stored in the global mark register GMR.
If the master's clock or its local time has been corrected and a discontinuity has been introduced, the discontinuity bit DISC is automatically set until the next reference message is started. The discontinuity bit is set if a write access to LOF or LOFFR occurs. As a result, the reference message will contain the new reference mark and the discontinuity bit DISC set for the current time master.

24.7.5 Transmit Enable Window

The transmit enable window determines the number of CAN bit times that may elapse between the transmit trigger event (time marks in the scheduler) and the real start of the message on the bus. If this time expires without starting the transmission of the triggered message, no new transmission attempt will be made in this time window (if it was an exclusive one or a short arbitration one). The transmit trigger is deleted and an interrupt may be generated. If the time window is a long, merged arbitration window, the transmit enable window is not taken into account.

24.7.6 Local Offset and Global Time

On TTCAN level 2, the local offset of a TTCAN node (not of the time master) is defined as the difference between the Master_Ref_Mark (also named Global_Ref_Mark) and the node's reference mark Ref_Mark. For the time master, the sum of the local time and the local offset is stored as Global_Sync_Mark when the frame synchronization is reached. The Global_Sync_Mark (for the time master) and the Global_Ref_Mark (for all other nodes) are stored in the Global Mark Register GMR. The Local_Offset is stored in the local offset register LOR.

When a TTCAN node receives a reference message, the global mark register is updated by the received value. The value that has been received in the previous reference message is automatically transferred from the global mark register to the last global mark register. The difference between these two values represents the time elapsed between the last two reference messages from the time master's point of view.

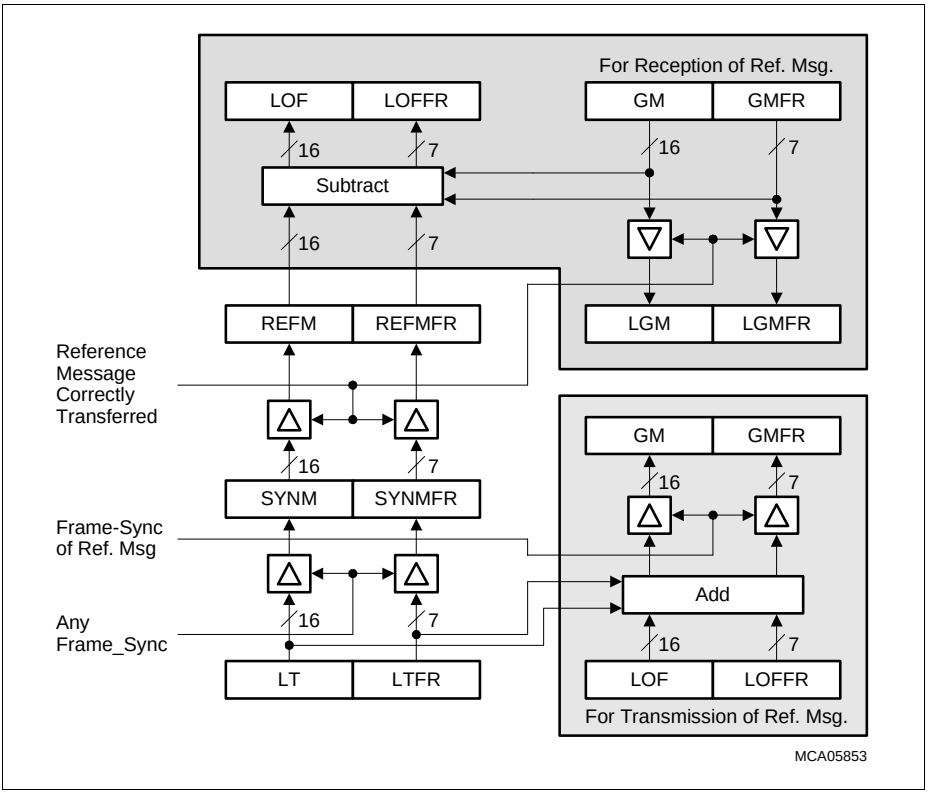


Figure 24-28 Local Offset and Global Time

Due to possible variations of the LOF values from one reference mark to the other, the current global time may contain discontinuities. In order to get a smooth (continuous) behavior, a SW filter can be used for receiving nodes. The global time can be calculated as shown below:

- Local Time + Local Offset or
- Cycle Time + Reference Mark + Local Offset

24.7.7 Transmit Trigger

The TTCAN feature of a CAN node implies the counting of transmission requests for messages to be sent in exclusive time windows. The number of messages to be transmitted in exclusive time windows is defined by system application design for the entire system matrix (expected transmit triggers EXPTT). This theoretical value is used to verify if the real TTCAN node also requests the same amount of transmissions. If fewer or more transmit triggers have been counted by the transmit trigger counter TTCNT at the end of a system matrix, a transmit trigger error interrupt can be generated (if enabled by TTIEN). This is indicated by the bits transmit trigger underflow TTUF and transmit trigger overflow TTOF.

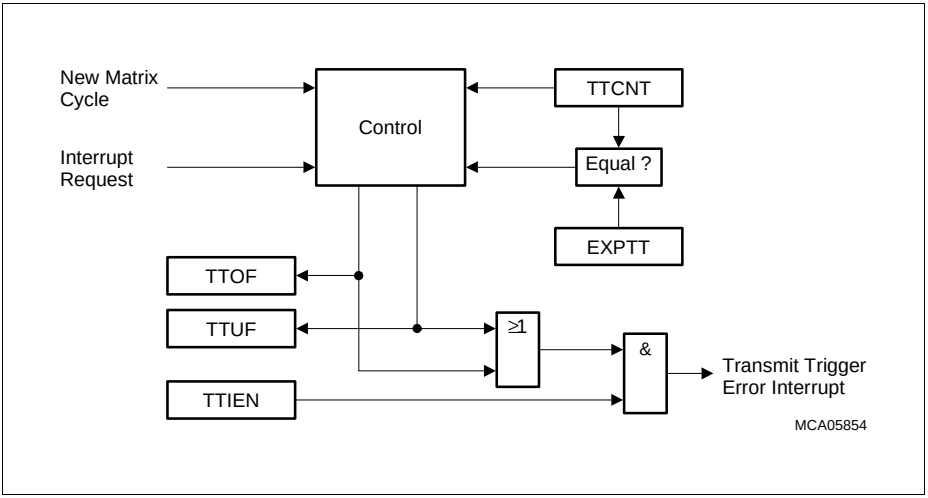


Figure 24-29 Transmit Trigger Monitoring

24.7.8 Reference Message

The reference message object has a special role in the TTCAN system. It is the first entry in the message object list for the TTCAN node (node 0 in the TC1798).

24.7.8.1 Differences to Normal CAN Messages

There are several differences between the behavior of a reference message and a normal CAN message:

- If a reference message is disturbed by an error during transmission, it is retransmitted immediately.
- If a reference message loses arbitration, it is not retransmitted, but the message on the bus is received (arbitration of potential time masters).
- For reception, no identifier bits (except the 3 least significant bits ID[2:0]) use an acceptance mask (must be set by software). The entire identifier of the latest correct reference message on the bus is stored in the reference message object.
- For reception, the 3 least significant bits of the identifier always use the acceptance mask 000_B (must be set by software).
- Its transmission request, indicated by the flag TTSR.REFTRG, is related only to a reference time mark or to an external event (for synchronization). If a correct reference message is received while REFTRG is set, REFTRG is automatically cleared.
- For transmission, the identifier bits of the reference message object are taken, except the 3 least significant bits (ID[2:0]). They are taken from the bit field TMCR.TMPRIO.
- The corresponding parts of its eight data bytes are directly connected to the TTCAN internal values (cycle_count, master_ref_mark, etc.) according to the selected level of the TTCAN protocol. The remaining bytes are available for free use.
- The DLC of a reference message to be sent out is determined by the bit field TTCR.RMDLC. This bit field must be at least 1 in TTCAN level 1 and at least 4 in TTCAN level 2.

A reference message object is used by a time master, a potential time master, and a receiving device (not a time master).

The reference message object must be initialized as a receive object (but the transmission of this object leads to the reference frame). This is due to the fact that the reception of a reference message is determined by the normal receive acceptance filtering, whereas the transmission is a specific action, triggered by the TTCAN extension.

Reference messages can also be transmitted by time masters that are in S2 error state or after the Init_Watch_Trigger has been reached.

24.7.8.2 Transmit Trigger for a Reference Message

The transmission of a reference message can be triggered by a time mark or by an external event. If it is triggered by a time mark, the “Next is Gap” bit (TTSR.NIG) of the previous reference message has been 0. If it is triggered by an external event, the “Next is Gap” bit of the previous reference message has been 1.

The software can set bit TTSR.NIG in order to initiate the synchronization of a reference message to an event. This event can be an edge at an external input or a software action (write bit TTFMR.STE = 1, software trigger event).

When TTSR.NIG is set, it will be transmitted with the next reference message in order to indicate the following synchronization gap to the other CAN nodes. The value of TTSR.NIG is copied to bit TTSR.ETR (external trigger request) and cleared automatically when the reference message has been correctly transmitted. Bit TTSR.ETR = 1 indicates that the next reference message will be transferred as soon as the corresponding time mark is reached (respecting the gap), or when the selected trigger event (ETREV) is pending. The evaluation of ETREV is started after the end of the transmit enable window of the last transfer window (valid RME found).

The transmit trigger generation logic for the reference message is shown in **Figure 24-30**. The edge detection for ECTTx contains a synchronization stage.

The trigger event can be selected by bit field ETESEL (external trigger event selection). Only trigger events are taken into account for the transfer of a reference message that have been detected after the start of the current basic cycle.

The synchronization of more than one TTCAN node to other TTCAN nodes can be achieved by setting ETESEL = 00_B. In this case, the trigger of the reference message of TTCAN nodes 0-7 (TRMCx) is used to trigger the transmission of the reference message. As a result, the reference messages can be synchronized between several TTCAN nodes of the MultiCAN/TTCAN. If not all possible TTCAN nodes are implemented, the TRMCx of not implemented nodes are 0.

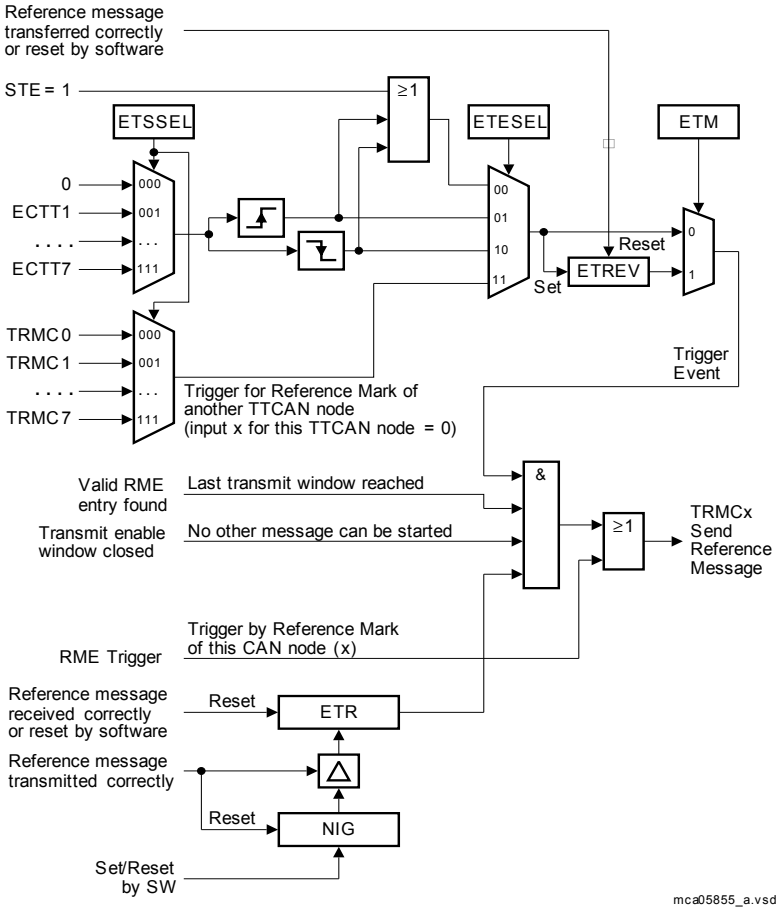


Figure 24-30 External Trigger Generation an Transmit Trigger for the Reference Message

24.8 TTCAN Scheduler

24.8.1 Overview

The message transmission and reception of the time-triggered part TTCAN is controlled by a scheduler mechanism. This scheduler is based on the cycle time and delivers the time marks. The time marks are defined by the time mark entries TMEx. Whenever a time mark is reached, programmable actions (defined by scheduler memory instruction entries INSTRxy) can take place. Typical instructions include, for example, starting the transmission of a message, checking if a message has been received, opening or closing arbitration windows, or generating interrupts.

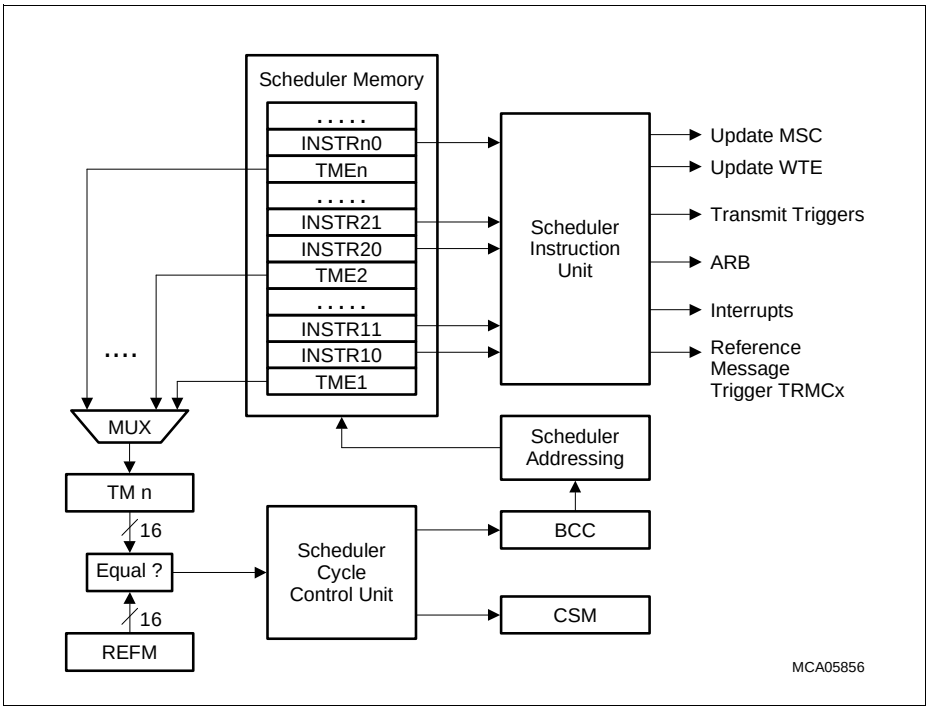


Figure 24-31 Scheduler Overview

The instructions following a time mark are read by the scheduler until the next time mark entry is found. Then, the instruction collection process is stopped until the next time mark is reached.

Note: The time mark values in the scheduler entries must be in increasing order.

24.8.2 Scheduler Memory

The scheduler contains a memory block in which the time mark entries (TMEx) and the scheduler instruction entries (INSTRnx) are stored. Each time mark entry can be followed by a number of scheduler instructions. The scheduler memory is organized as a 32-bit wide memory holding the 32-bit wide time mark entries and the 32-bit wide scheduler instruction entries.

The total number of time mark entries and scheduler instruction entries that can be stored is limited by the size of the scheduler memory. In the TC1798, the scheduler memory has a size of 128 words (32-bits).

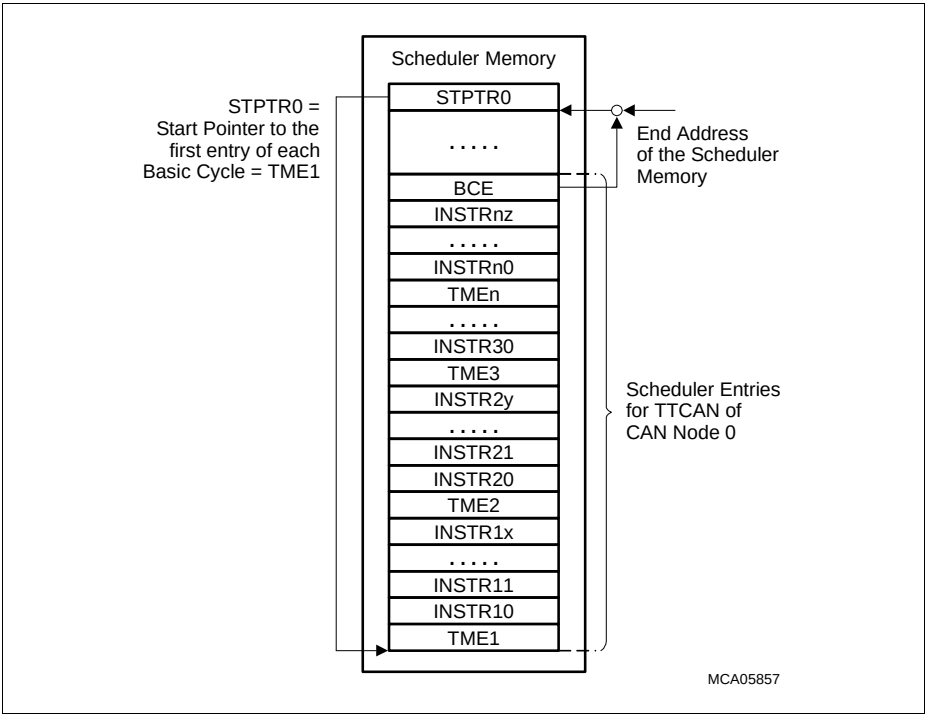


Figure 24-32 TTCAN Scheduler Memory

The last word address of the scheduler memory is reserved for the start pointer STPTR0. The value written at this address determines the start location of the first entry for the TTCAN node (= CAN node 0 in the TC1798). STPTR0 indicates how many 32-bit (word) entries below SPTR0 the first time mark entry (TME1) is located.

When the basic cycle end entry BCE (with GM = 0) is read by the scheduler, it prepares the next scheduler instructions (read from scheduler memory) starting again with TME1.

Therefore, the first entry read after BCE is STPTR0 in order to obtain the address where TME1 is located.

24.8.2.1 Scheduler Entry Types

The scheduler instruction entries are located after the time mark entry. The time mark entry determines the behavior of the TTCAN when the next time mark is reached. The scheduler instructions after the time mark entry are valid for the time mark they follow. The scheduler control reads the time mark entry and sets up the compare action (compare between the new time mark with the cycle time). Then, the scheduler reads the following instructions and sets up the transfer behavior of the TTCAN node. The scheduler stops reading from the scheduler memory when a new time mark entry is found.

The transfer behavior set up can change with each scheduler instruction. There is no built-in consistency check for scheduler instructions. Previously read scheduler instructions can be overwritten by subsequent ones. With each time mark, the settings are cleared and must be set up by new scheduler instructions (if desired).

The complete scheduler information must be finished with a basic cycle end entry that fixes the value for the watch trigger event.

Each entry in the scheduler memory contains a 4-bit wide code field that determines the type of the entry. The possible scheduler memory entry types are listed in **Table 24-14**.

Table 24-14 Scheduler Memory Entry Types

Entry Code EC Bits [31:28]	Short Name	Entry Type	Defined at
0001_B	TME	Time mark entry	see **Page 24-129**
0010_B	ICE	Interrupt control entry	see **Page 24-132**
0011_B	ARBE	Arbitration entry	see **Page 24-134**
0100_B	TCE	Transmit control entry	see **Page 24-136**
0101_B	RCE	Receive control entry	see **Page 24-139**
0110_B	RME	Reference message entry	see **Page 24-141**
0111_B	BCE	Basic cycle end entry	see **Page 24-143**
other combinations	EOS	End of scheduler memory entry	see **Page 24-144**

The general transmit trigger control for the message objects to be transmitted when a time mark is reached is performed by the message objects themselves. In order to increase the flexibility, the result of the acceptance filtering done with the message objects can be overruled by control entries. A reference message can be transmitted only when the TTCAN node is enabled as time master.

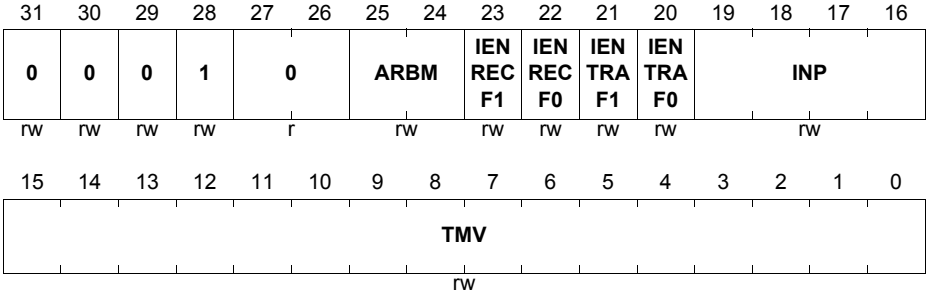
Note: The number of scheduler entries following a time mark should not exceed the number of 10. In order to minimize the required accesses to the scheduler memory by the scheduler control part, the user should set up the system carefully.

24.8.2.2 Scheduler Entry Type Description

Time Mark Entry

A time mark entry is defined as follows:

TME
Time Mark Entry



Field	Bits	Type	Description
TMV[1)]	[15:0]	rw	**Time Mark Value** This bit field determines the compare value used for the next compare action with the cycle time.
INP	[19:16]	rw	**Interrupt Node Pointer** INP selects the interrupt output line INT_Om (m = 0-15) that will be activated when a match is detected between the cycle time and the time mark value defined by TMV and if at least one of the four interrupt conditions is met and enabled. 0000_B Interrupt output line INT_O0 is selected. 0001_B Interrupt output line INT_O1 is selected. $\ldots_B$ … 1110_B Interrupt output line INT_O14 is selected. 1111_B Interrupt output line INT_O15 is selected.

Field	Bits	Type	Description
IENTRAF0	20	rw	**Interrupt Enable if TRAF = 0** This bit enables the generation of an interrupt when bit TTSR.TRAF = 0 and a match is detected between the cycle time and the time mark value defined by TMV. 0_B Interrupt generation is disabled. 1_B Interrupt generation is enabled.
IENTRAF1	21	rw	**Interrupt Enable if TRAF = 1** This bit enables the generation of an interrupt when bit TTSR.TRAF = 1 and a match is detected between the cycle time and the time mark value defined by TMV. 0_B Interrupt generation is disabled. 1_B Interrupt generation is enabled.
IENRECF0	22	rw	**Interrupt Enable if RECF = 0** This bit enables the generation of an interrupt when when bit TTSR.RECF = 0 and a match is detected between the cycle time and the time mark value defined by TMV. 0_B Interrupt generation is disabled. 1_B Interrupt generation is enabled.
IENRECF1	23	rw	**Interrupt Enable if RECF = 1** This bit enables the generation of an interrupt when when bit TTSR.RECF = 1 and a match is detected between the cycle time and the time mark value defined by TMV. 0_B Interrupt generation is disabled. 1_B Interrupt generation is enabled.

Field	Bits	Type	Description
ARBM	[25:24]	rw	**Arbitration Mode** This bit field determines the action that is taken with an arbitration window. 00_B No action taken; the status of the arbitration window is not changed. 01_B A merged (long) arbitration window will be opened. If it is already opened, it is kept open. 10_B A merged (long) transfer window will be closed. Closing a merged transfer window leads to a single (short) arbitration window (transmission possible only during the transmit enable window). The short arbitration window is automatically closed after one time window. If there is no arbitration window open, this entry will be ignored. 11_B A single (short) arbitration window (transmission possible only during the transmit enable window) is opened. A short arbitration window is automatically closed after one time window.
EC	[31:28]	rw	**Entry Code** The entry code EC = 0001_B defines this scheduler memory entry as a time mark entry.
0	[27:26]	r	**Reserved;** read as 0; should be written with 0. Bits are “don’t care” for scheduler operation when EC = 0001_B.

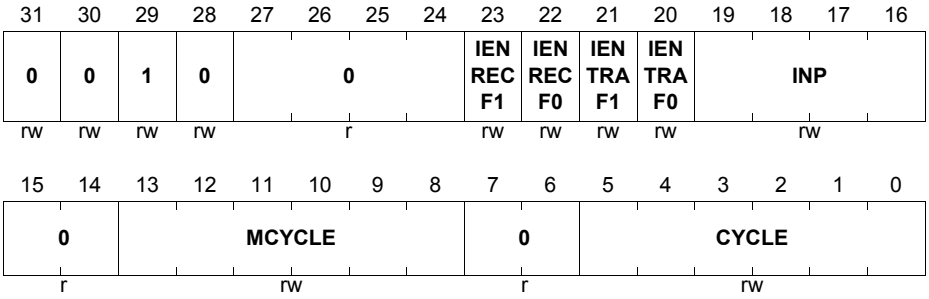
1) In order to be able to detect each time mark correctly, the first time mark of a basic cycle must not be set to a value below the length of the reference message under worst case conditions.

Note: The interrupt settings given by the time mark entry can be overruled by a subsequent valid interrupt control entry. The settings are valid until the next time mark is reached. For the time after the next time mark, the settings read from the next time mark entry become valid.

Interrupt Control Entry

An interrupt control entry is defined as follows:

ICE
Interrupt Control Entry



Field	Bits	Type	Description
CYCLE	[5:0]	rw	**Basic Cycle Number** This bit field determines the number of the basic cycle during which this interrupt control entry is valid. The value of CYCLE is compared (bit-wise) to the current value of the bit field CYCTMR.BCC. The result is then masked with the value given by the bit field MCYCLE in order to determine the repetition rate for this scheduler entry inside the matrix cycle. This bit field is equivalent to the corresponding part of the MOAMRn.AM bit field (see **Page 24-110**).
MCYCLE	[13:8]	rw	**Mask for Cycle Comparison** This bit field determines the mask that is used to determine the repetition rate for this scheduler entry. This bit field is equivalent to the corresponding part of the MOAMRn.AM bit field (see **Page 24-110**).

Field	Bits	Type	Description
INP	[19:16]	rw	**Interrupt Node Pointer** INP selects the interrupt output line INT_Om (m = 0-15) that will be activated when a match is detected between the cycle time and the time mark value defined by TMV and if at least one of the four interrupt conditions is met and enabled. 0000_B Interrupt output line INT_O0 is selected. 0001_B Interrupt output line INT_O1 is selected. … … 1110_B Interrupt output line INT_O14 is selected. 1111_B Interrupt output line INT_O15 is selected.
IENTRAF0	20	rw	**Interrupt Enable if TRAF = 0** This bit enables the generation of an interrupt when a match is detected between the cycle time and the time mark value defined by TMV and bit TRAF = 0. 0_B An interrupt will not be generated. 1_B An interrupt will be generated.
IENTRAF1	21	rw	**Interrupt Enable if TRAF = 1** This bit enables the generation of an interrupt when a match is detected between the cycle time and the time mark value defined by TMV and bit TRAF = 1. 0_B An interrupt will not be generated. 1_B An interrupt will be generated.
IENRECF0	22	rw	**Interrupt Enable if RECF = 0** This bit enables the generation of an interrupt when a match is detected between the cycle time and the time mark value defined by TMV and bit RECF = 0. 0_B An interrupt will not be generated. 1_B An interrupt will be generated.
IENRECF1	23	rw	**Interrupt Enable if RECF = 1** This bit enables the generation of an interrupt when a match is detected between the cycle time and the time mark value defined by TMV and bit RECF = 1. 0_B An interrupt will not be generated. 1_B An interrupt will be generated.
EC	[31:28]	rw	**Entry Code** The entry code EC = 0010_B defines this scheduler memory entry as an interrupt control entry.

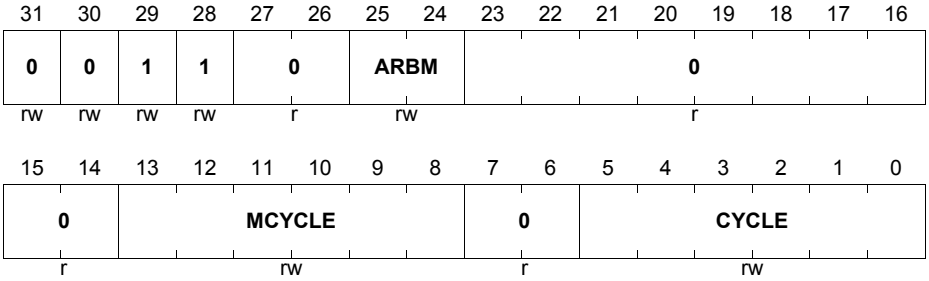
Field	Bits	Type	Description
0	[7:6], [15:14], [27:24]	r	**Reserved;** read as 0; should be written with 0. Bits are “don’t care” for scheduler operation when EC = 0011_B.

Note: The interrupt settings of a valid interrupt control entry overrule the previously stored interrupt settings for the next time mark. As a result, the use of more than one valid interrupt control entry between two time mark entries should be avoided.

Arbitration Entry

The arbitration entry is defined as follows:

ARBE
Arbitration Entry



Field	Bits	Type	Description
CYCLE	[5:0]	rw	**Basic Cycle Number** This bit field determines the number of the basic cycle during which this arbitration entry is valid. The value of CYCLE is compared (bit-wise) with the **current** value of bit field CYCTMR.BCC. The result is then masked with the value given by the bit field MCYCLE in order to determine the repetition rate for this scheduler entry inside the matrix cycle. This bit field is equivalent to the corresponding part of the MOAMRn.AM bit field (see **Page 24-110**).

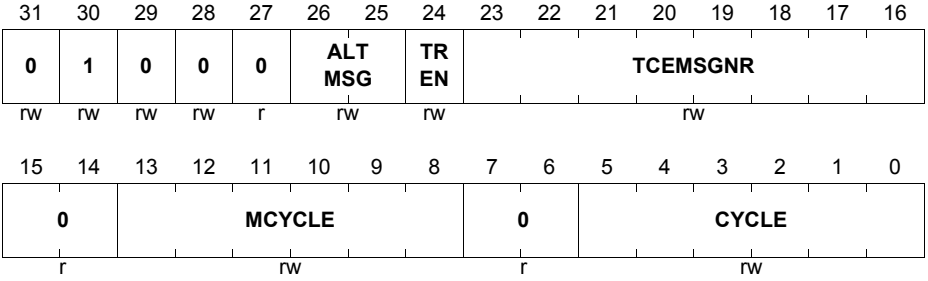
Field	Bits	Type	Description
MCYCLE	[13:8]	rw	**Mask for Cycle Comparison** This bit field determines the mask used to determine the repetition rate for this arbitration entry. This bit field is equivalent to the corresponding part of the MOAMRn.AM bit field (see **Page 24-110**).
ARBM	[25:24]	rw	**Arbitration Mode** This bit field determines the action that is taken with an arbitration window. 00_B No action is taken; the status of the window is not changed. 01_B A merged (long) arbitration window will be opened. If it is already opened, it is kept open. 10_B A merged (long) transfer window will be closed. Closing a merged transfer window leads to a single (short) arbitration window (transmission possible only during the transmit enable window). The short arbitration window is automatically closed after one time window. 11_B A single (short) arbitration window (transmission possible only during the transmit enable window) is opened. A short arbitration window is automatically closed after one time window.
EC	[31:28]	rw	**Entry Code** The entry code EC = 0011_B defines this scheduler memory entry as an arbitration entry.
0	[7:6], [23:14], [27:26]	r	**Reserved;** read as 0; should be written with 0. Bits are “don’t care” for scheduler operation when EC = 0011_B.

Note: The arbitration settings of a valid arbitration entry overrule the previously stored arbitration settings for the next time mark. As a result, the use of more than one valid arbitration entry between two time mark entries should be avoided.

Transmit Control Entry

The transmit control entry is defined as follows:

TCE
Transmit Control Entry



Field	Bits	Type	Description
CYCLE	[5:0]	rw	**Basic Cycle Number** This bit field determines the number of the basic cycle during which this transmit control entry is valid. The value of CYCLE is compared (bit-wise) to the current value of the bit field CYCTMR.BCC. The result is then masked with the value given by the bit field MCYCLE in order to determine the repetition rate for this transmit control entry inside the matrix cycle. This bit field is equivalent to the corresponding part of the MOAMRn.AM bit field (see **Page 24-110**).
MCYCLE	[13:8]	rw	**Mask for Cycle Comparison** This bit field determines the mask that is used to determine the repetition rate for this transmit control entry. This bit field is equivalent to the corresponding part of the MOAMRn.AM bit field (see **Page 24-110**).

Field	Bits	Type	Description
TCEMSGNR	[23:16]	rw	**TCE Message Number** This bit field determines the number of the message object to be transmitted when the next time mark is reached. The object will be transferred only if it is tagged valid for transmission. With this scheduler instruction, the number of the message object is defined directly, without taking into account to which CAN node it is currently assigned. Even if it is assigned to another CAN node, the selected message object will be transmitted. If the CAN message transmit acceptance filtering delivers an object number to be transmitted, it is overruled by a valid transmit control entry according to ALTMSG. If the message object delivered by the transmit control entry is not valid for transmission, no transmission will be started.
TREN	24	rw	**Transmission Enable** This bit enables transmission of a message object in the next time window due to the TTCAN transmit trigger. 0_B Neither a TTCAN transmit trigger nor the message object transmit acceptance will lead to a transmission of a message object in the next time window. 1_B If a TTCAN transmit trigger occurs or the message object transmit acceptance filtering delivers a valid message object, the transmission of a message object in the next time window is enabled.

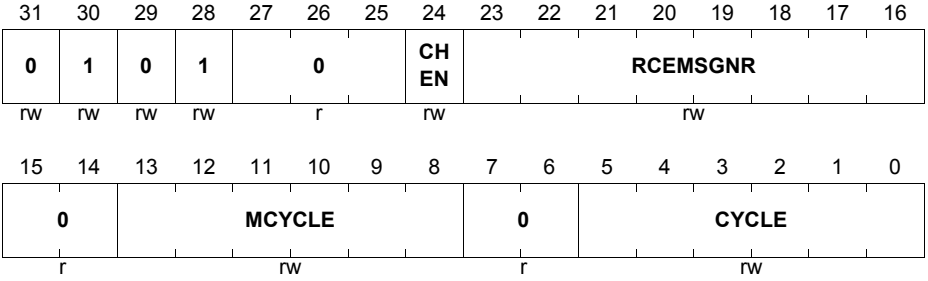
Field	Bits	Type	Description
ALTMSG	[26:25]	rw	**Alternative Message** This bit field determines which message object will be transmitted. 00_B If the message object number delivered by this entry is not valid for transmission, no message will be sent. 01_B The message object number delivered by this entry is not taken into account for transmission, the message object found by the transmit acceptance filtering will be sent if it is valid. 10_B If the message object delivered by this entry is not valid for transmission, while the message object transmit acceptance filtering delivered a valid object, the latter one will be sent out. 11_B Reserved
EC	[31:28]	rw	**Entry Code** The entry code EC = 0100_B defines this scheduler memory entry as a transmit control entry.
0	[7:6], [15:14], 27	r	**Reserved;** read as 0; should be written with 0. Bits are “don’t care” for scheduler operation when EC = 0100_B.

Note: The message transmit settings of a valid transmit control entry overrule the previously stored transmit settings and may also overrule the transmit acceptance filtering of the message objects for the next time mark (depending on bit ALTMSG). As a result, the use of more than one valid transmit control entry between two time mark entries should be avoided.

Receive Control Entry

The receive control entry is defined as follows:

RCE
Receive Control Entry



Field	Bits	Type	Description
CYCLE	[5:0]	rw	**Basic Cycle Number** This bit field determines the number of the basic cycle during which this receive control entry is valid. The value of CYCLE is compared (bit-wise) to the current value of the bit field CYCTMR.BCC. The result is then masked with the value given by the bit field MCYCLE in order to determine the repetition rate for this scheduler entry inside the matrix cycle. This bit field is equivalent to the corresponding part of the MOAMRn.AM bit field (see **Page 24-110**).
MCYCLE	[13:8]	rw	**Mask for Cycle Comparison** This bit field determines the mask that is used to determine the repetition rate for this scheduler entry. This bit field is equivalent to the corresponding part of the MOAMRn.AM bit field (see **Page 24-110**).

Field	Bits	Type	Description
RCEMSGNR	[23:16]	rw	**RCE Message Number** This bit field determines the number of the message object that is checked for correct reception of a message during the last transfer window. A received message is always stored in the message object that is determined by acceptance filtering. When reaching a new time mark, an RCE can be used to check if a desired message has actually been received in the desired message object.
CHEN	24	rw	**Check Enable** Only time windows with an active receive control entry with CHEN=1 will handle the update of the MSC bit field in the message object indicated by RCEMSGNR. If a frame has been received correctly and also stored in the indicated message object, then the reception is considered as correct; otherwise, it is an error. 0_B The MSC bit field of the indicated message object is not updated. 1_B The MSC bit field of the indicated message object is updated.
EC	[31:28]	rw	**Entry Code** The entry code EC = 0101_B defines this scheduler memory entry as a receive control entry.
0	[7:6], [15:14], [27:25]	r	**Reserved;** read as 0; should be written with 0. Bits are “don’t care” for scheduler operation when EC = 0101_B.

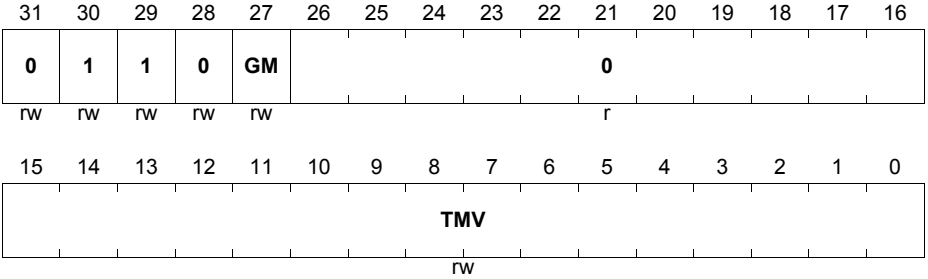
Note: The settings of a valid receive control entry overrule the previously stored information. As a result, the use of more than one valid receive control entry between two time mark entries should be avoided.

Note: If no receive control entry has been found valid for the current time window, the reception and storage of messages depends only on the message object receive acceptance filtering. Only message objects receiving messages with a valid receive control entry modify their MSC bit field accordingly. The MSC bit field of a receiving object is not modified without a valid receive control entry.

Reference Message Entry

The reference message is defined as follows:

RME
Reference Message Entry



Field	Bits	Type	Description
TMV	[15:0]	rw	**Time Mark Value** These bits determine the compare value for the next time mark. This value is used for the next compare action with the cycle time. If the CAN node is a time master, the reference message will be sent out when the time mark is reached (see also TMR.RTO).
GM	27	rw	**Gap Mode** This bit determines how the scheduler of a time master proceeds if the TTCAN node is “in a gap”. 0_B The reference message will be sent according to this RME entry (without respecting a possible gap). 1_B If the TTCAN node is “in a gap”, this RME entry is discarded and the following entries are read.
EC	[31:28]	rw	**Entry Code** The entry code EC = 0110_B defines this scheduler memory entry as a reference message entry.
0	[26:16]	r	**Reserved;** read as 0; should be written with 0. Bits are “don’t care” for scheduler operation when EC = 0110_B.

Note: This entry is taken into account for a time master. In the case that more valid reference message entries are detected, the settings of the previously found reference message entries are overruled by a subsequent one.

If the TTCAN node is not configured as time master and the scheduler reads an RME, a configuration error is generated.

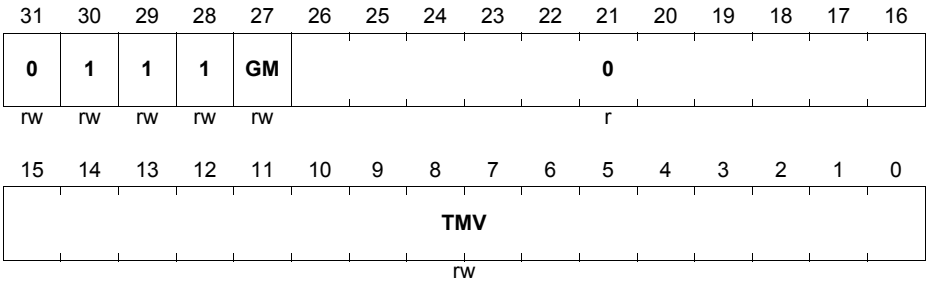
While the system is in the synchronization state, an RME entry with GM = 1 is not taken into account.

Basic Cycle End Entry

The basic cycle end entry defines the time mark value that is used as a watch trigger time mark. In the case that the TTCAN system is waiting for a reference message while the system is normally synchronized (not in a gap = not waiting for another event to synchronize). If the system is in a gap with GM set, the following entries can be read.

The basic cycle end is defined as follows:

BCE
Basic Cycle End Entry



Field	Bits	Type	Description
TMV	[15:0]	rw	**Time Mark Value** This bit field determines the compare value for the next time mark that is used for the next compare action with the cycle time. TMV determines the watch trigger that is used to generate a watch trigger event WTE when the cycle time reaches TMV. The value written into TMV must meet the condition that a minimum of one CAN frame length is in between the last time mark and the basic cycle end entry. For this calculation, the reference trigger offset TMR.RTO for the reference message entry must also be taken into account.

Field	Bits	Type	Description
GM	27	rw	**Gap Mode** This bit determines how the scheduler proceeds when the TTCAN node is “in a gap” and waits for a trigger event to send the reference message (for the current time master) or when it waits for the reception of a reference message. 0_B The watch trigger event will be generated according to this BCE entry (without respecting a possible gap). 1_B If the TTCAN node is “in a gap”, this basic cycle end entry is discarded and the following entries are read.
EC	[31:28]	rw	**Entry Code** The entry code EC = 0111_B defines this scheduler memory entry as a basic cycle end entry.
0	[26:16]	r	**Reserved;** read as 0; should be written with 0. Bits are “don’t care” for scheduler operation when EC = 0111_B.

Note: The BCE determines the end of the scheduler entries in the scheduler memory when the system is normally synchronized. When the time mark of this entry is reached, the TTCAN node will automatically enter the Configuration Mode. It will continue with the first time mark when a reference message has been correctly transferred on the CAN bus.

While the system is in the synchronization state, a BCE entry with GM = 1 is not taken into account.

24.8.2.3 End of Scheduler Memory Entry

The end of scheduler memory entry EOS is defined by entry codes EC = 0000_B or EC = $1XXX_B$ (see **Table 24-14**). An EOS immediately stops the reading of entries in the scheduler memory and sets the TTCAN node into Configuration Mode.

EOS can be regarded as a kind of emergency stop entry. It should not be used to control the scheduler itself but represents a security mechanism for the case that a scheduler entry does not show a valid EC bit field.

24.8.3 Setup of the Scheduler Entries

The entries in the scheduler memory can be set up only when all bits NCRx.CCE of the TTCAN nodes sharing the scheduler memory are set at the same time. Write actions to the scheduler memory while not all corresponding bits NCRx.CCE = 1 are not taken into account. The scheduler entries can always be read out for verification purposes.

24.8.4 Reading the Scheduler Entries

After a time mark has been reached, the scheduler instructions for the following time window are read by the scheduler. This “collected” information can be read out from the scheduler timing status and from the scheduler instruction status register. The information becomes valid when the next time mark is reached. The information collected between time mark n-1 and time mark n becomes valid when the time mark n is reached.

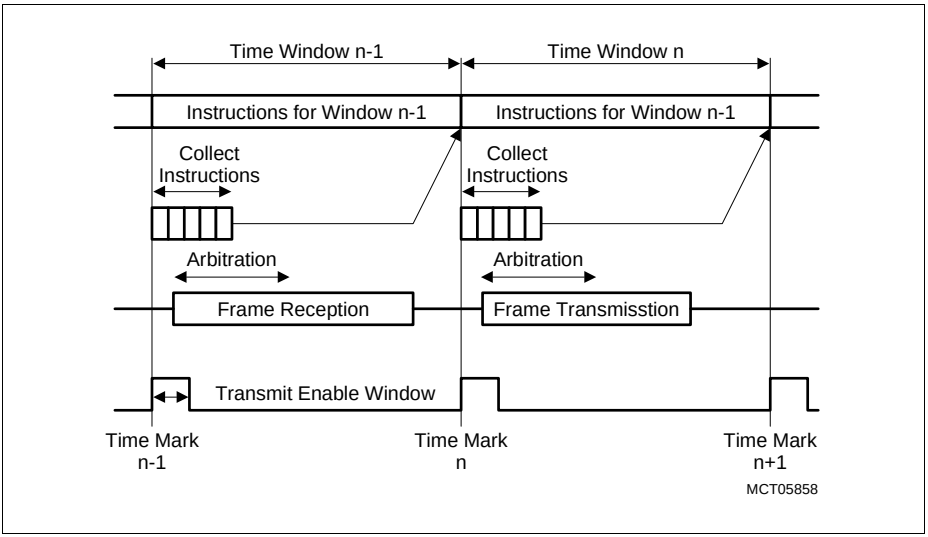


Figure 24-33 Collecting the Instructions

24.8.4.1 Instructions During a Basic Cycle

The handling of entries collected between the time marks n-1 and n is defined as follows:

- Time Mark Entry:
  The time mark value is defining the compare value for the time mark n.
- Interrupt Entry:
  Valid interrupt information (INP+ 4 enable bits) can generate an interrupt when the time mark n is reached, depending on the flags RECF and TRAF (they are

automatically cleared when the time mark is reached). As a result, this interrupt indicates that a (no) message has been sent /received in the time window between the time marks n-1 and n.

- Receive Control Entry:
  Valid receive control information (CHEN, RCEMSGNR) controls the storage of a message in the time window between the time marks n-1 and n.
- Arbitration Entry:
  Valid arbitration information (ARBM) determines the behavior of the time window starting with the time mark n.
- Transmit Control Entry:
  Valid transmit control information (TREN, ALTMSG, TCEMSGNR) defines a message to be transmitted after the time mark n. The transmission start is possible while the transmit enable window is active for an exclusive window or for a short (single) arbitration window or for the end of a merged arbitration window. For a merged (long) arbitration window, the transmission can start during the complete time window.
- Reference Message Entry:
  not used in this time window
- Basic Cycle End Entry:
  not used in this time window

The TMV value collected after time mark n-1 will become the new compare value for the time mark n.

The value of CYCTMR.CSM equals the time mark number of the last time mark reached (CSM = n after time mark n has been reached). The value of CYCTMR.BCC is number of the current basic cycle. This information is needed to correctly set up the scheduler entries (bit fields CYCLE, MCYCLE) and the message objects (bit fields CYCLE, MCYCLE, COLUMN, MCOLUMN).

24.8.4.2 Instructions at the End of a Basic Cycle

The collection of instructions for the last time window of a basic cycle starts when the time mark before is reached and stops when the entry TME2 is found. Handling of the entries collected during the last time window of a basic cycle:

- Time Mark Entry:
  After a valid BCE has been read, the first time mark TME1 is read and its value is defining the compare value for the time mark 1 (first time mark after the reference message = start of a new basic cycle).
- Interrupt Entry:
  Valid interrupt information (INP+ 4 enable bits) collected during the last time window of a basic cycle can generate an interrupt when the time mark 1 is reached, depending on the flags RECF and TRAF (they are automatically cleared when the time mark is reached). These flags do not apply to the reference message (the

transfer of a reference message does not modify these flags). As a result, this interrupt indicates that a (no) message has been sent /received in the last time window of the basic cycle. The ICE for the last time window of a basic cycle must be written into the scheduler memory after the entry TME1.

- Receive Control Entry:
  Valid receive control information (CHEN, RCEMSGNR) collected during the last time window of a basic cycle controls the storage of a message in the last time window (not applicable to reference message). The RCE for the last time window of a basic cycle must be written into the scheduler memory after the entry TME1.
- Arbitration Entry:
  Valid arbitration information (ARBM) determines the behavior of the time window starting with the time mark 1. This entry must be written into the scheduler memory after the entry TME1.
- Transmit Control Entry:
  Valid transmit control information (TREN, ALTMSG, TCEMSGNR) defines a message to be transmitted after the time mark 1. The transmission start is possible while the transmit enable window is active for an exclusive window or for a short (single) arbitration window. For a merged (long) arbitration window, the transmission can start during the complete time window. This entry must be written into the scheduler memory after the entry TME1.
- Reference Message Entry:
  The time mark value of a valid RME is defining the compare value for the reference time mark. When this reference time mark plus the reference trigger offset is reached, a reference message will be sent out (depending on the gap state of the system). This entry must be written into the scheduler memory before a valid entry BCE.
- Basic Cycle End Entry:
  The time mark value of a valid BCE is defining the compare value for the watch trigger event. When this time value is reached, a watch trigger event can be generated (depending on the gap state of the system). A valid BCE always finishes the scheduler entries for each TTCAN node.

Before the reference message has been correctly transferred:
The value of CYCTMR.CSM equals the time mark number of the last time mark reached (CSM = n after time mark n has been reached). The value of CYCTMR.BCC is number of the current basic cycle. This information is needed to correctly set up the scheduler entries RCE and ICE (bit fields CYCLE, MCYCLE).

After the reference message has been correctly transferred, but the time mark 1 has not yet been reached:
The value of CYCTMR.CSM is 0. The value of CYCTMR.BCC is number of the new basic cycle. This information is needed to correctly set up the scheduler entries ARBE and TCE (bit fields CYCLE, MCYCLE) and the message objects (bit fields CYCLE, MCYCLE, COLUMN, MCOLUMN).

As a result, the ICE and the RCE describing the reception / transmission of a message in the last time window of a basic cycle lead to actions (interrupts, etc.) when time mark 1 is reached.

24.8.5 Scheduler Instruction Sequence

24.8.5.1 BCC and CSM

In order to set up the scheduler instructions correctly, the values of CSM and BCC in register CYCTMR must be respected carefully, especially for the last time window of a basic cycle.

In order to set up the scheduler instructions correctly, the values of CSM and BCC in register CYCTMR must be respected carefully, especially for the last time window of a basic cycle. When leaving the Configuration Mode, BCC and CSM are 0 and the scheduler starts with time mark 1. The values for BCC and CSM in **Figure 24-34** represent the internal values that are updated after the correct transfer of a reference message.

The message triggered by the last time reference mark in a basic cycle is the reference message (see RME description). In **Figure 24-34**, this corresponds to the message after the time window n. The reference time mark follows after the time window n and the reference message starts a new basic cycle.

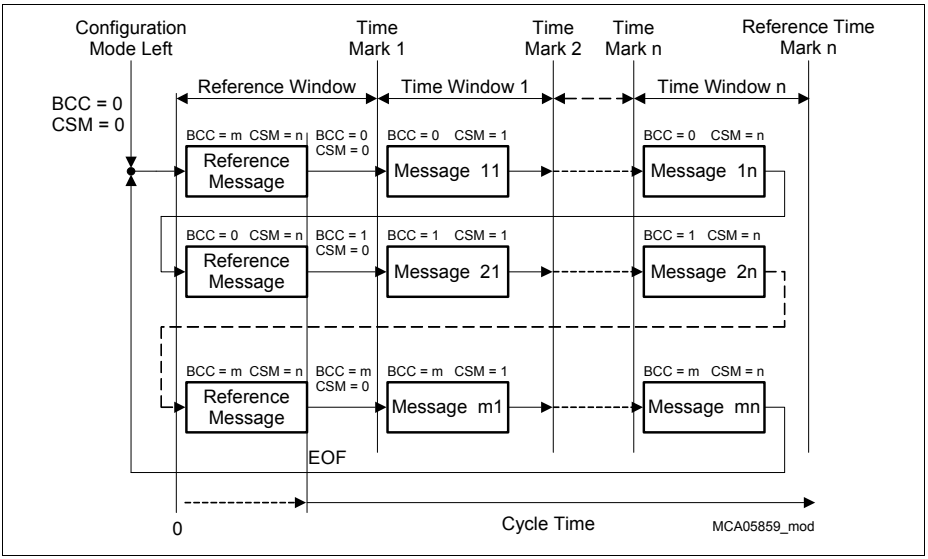


Figure 24-34 BCC and CSM in a Matrix Cycle

The cycle time of each basic cycle starts with 0 (virtual value). The start of a new basic cycle can only be detected after the correct transfer of a reference message. As a result, the cycle time value can be considered as valid after the reference message has been correctly transferred.

24.8.5.2 General Instruction Sequence Rules

The settings of already read scheduler instructions can be overwritten by following valid scheduler instructions. The following order of scheduler entry types must be respected to set up the scheduler correctly (starting with the first):

- TME then RCE or ICE or TCE or ARBE
- RME then BCE (for time masters)
- BCE (for slave devices)

The scheduler entries must always be closed with a BCE with GM = 0.

For time masters, the following sequence can be set up to close the scheduler entries:

- RME (GM = 1) then BCE (GM = 1) then RME (GM = 0) then BCE (GM = 0)
  (the entries RME(GM = 0) and BCE(GM = 0) are mandatory)

If the system is in-a-gap, the first RME and BCE entries (both with GM = 1) are not taken into account. With these entries, the standard (not in-a-gap) timing values can be adjusted. A second RME (with GM = 0) can be set up to send an emergency reference message while the system is in-a-gap and the synchronization event takes too long. The

scheduler entries are then closed again with a BCE with GM = 0 (e.g. with a longer timing value as a time-out criteria for a missing synchronization event).

24.8.5.3 Scheduler Sequence Example

The values given for CSM and BCC (both bit fields are located in register CYCTMR) lead to valid scheduler entries RCE, TCE, ICE and ARBE (bit fields CYCLE, MCYCLE) and the transmit control of the message objects (bit fields CYCLE, MCYCLE, COLUMN, MCOLUMN). In the case that the programmed values for CYCLE, MCYCLE, etc. do not match the given values of CSM and BCC, the respective entry is considered invalid and its information is not taken into account for the corresponding time window. The following example shows a scheduler instruction sequence for the basic cycle m with n time mark entries:

- TME1
- RCE, ICE (CSM = n, BCC = m-1 or CSM = BCC = 0 when the Configuration Mode is left)
- TCE, ARBE (CSM = 0, BCC = m)

- TME2
- RCE, ICE (CSM = 1, BCC = m)
- TCE, ARBE (CSM = 1, BCC = m)
- TME3
- RCE, ICE (CSM = 2, BCC = m)
- TCE, ARBE (CSM = 2, BCC = m)

- other time marks and instructions

- TMEn
- RCE, ICE (CSM = n-1, BCC = m)
- TCE, ARBE (CSM = n-1, BCC = m)

- RME (GM = 1, only for time masters)
- BCE (GM = 1, for time masters and slaves)

- RME (GM = 0, only for time masters)
- BCE (GM = 0, for time masters and slaves)

24.9 TTCAN Operation

24.9.1 Configuration

After a reset operation, the TTCAN extension must be configured. The Configuration Mode is entered automatically after reset or can be initiated through software by writing TTFMR.CFGMEL = 01_B. The Configuration Mode can be left only by software by writing TTFMR.CFGMEL = 10_B. The status flag TTSR.CFGM indicates whether or not the Configuration Mode is active. This flag is automatically set when the corresponding CAN node turns off its clock (disable request).

In Configuration Mode of the TTCAN node (CAN node 0 in TC1798), the following actions must be performed, as indicated, by software or hardware:

For all nodes:

- The local time, the global time, and the cycle time are set to 0 (hardware).
- Transmission or reception of messages of TTCAN node is not possible, because the results of the acceptance filtering are not enabled (hardware).
- An appropriate TUR value must be written to bit field TURR.TURADJ (software). This value is automatically transferred to TURR.TUR (hardware).
- The scheduler memory entries must be initialized (software).
- The TTCAN control information (ID of reference message, etc.) and the TTCAN node itself must be set up completely and enabled for CAN message transfer (software).
- After the complete configuration (software), TTFMR.CFGMEL must be set to 10_B (software).
- The local time starts after leaving the Configuration Mode (hardware).
- The synchronization phase is entered automatically when the Configuration Mode is left (hardware). This is indicated by bit field TTSR.SYNCS = 01_B (hardware).
- For time masters, the transmission of the reference messages is scheduled as in a gap while the TTCAN node is in the “synchronizing” state. The scheduler entries RME with GM = 1 are taken into account only while the TTCAN node is in the “in schedule” state.
- For time masters and for time slaves, the scheduler entries BCE with GM = 1 are taken into account only while the TTCAN node is in the “in schedule” state.

24.9.2 Configuration Error

During the scheduler actions, some conditions lead to a configuration error:

- At the end of a basic cycle, a merged arbitration window is still open.
- An RME entry is found for a slave device.
- No time mark is found during instruction collection.
- An RCE, ICE, TCE or ARBE has been found before TME1 (after start or at the end of a basic cycle).

- Another entry (except EOS) than an RME or a BCE has been found after the first RME.
- A reference message object is not valid when it is requested for transmission.

24.9.3 Synchronization Phase

When starting a TTCAN system (e.g. after reset), the entire system must be synchronized after completing the configuration phase. During the synchronization phase (indicated by bit field TTSR.SYNCS = 01_B), the following actions must be taken (or are taken automatically):

The Init_Watch_Trigger is taken into account until the first message is correctly received or transmitted. An Init_Watch_Trigger event is detected when the cycle time reaches the value of 2^{16} -1. This event is indicated by IWTE = 1 and it only leads to an interrupt.

The watch trigger value given by the basic cycle end entry is taken into account only after the first correct transfer of a message. When a watch trigger event occurs after transferring a message correctly on the bus, the transmission and the reception of Data Frames or Remote Frames are disabled (the TTCAN node is set to Configuration Mode).

During the synchronization phase, the scheduler entries RME or BCE with GM = 1 are not taken into account.

24.9.4 Time Masters

24.9.4.1 State of a Time Master

A potential time master is a device that can transmit a reference message. A backup time master is a potential time master that has received a reference message that was not its own. The current time master is the device that has successfully sent its own reference message. There is only one current time master in a TTCAN system.

If the current time master receives a reference message that is not its own, then it becomes a backup time master. If a backup time master has successfully transmitted its own reference message, it becomes the new current time master.

When a priority conflict between the TTCAN node and the actual time master is detected, the value of RTO is automatically modified (decrement by 1). This means that the priority of the actual time master (given by bits ID[2:0]) of the latest received reference message is lower than the programmed TMPRIO value.

24.9.4.2 Strictly Time-Triggered Behavior

A strictly time-triggered behavior (gaps are not allowed) can be achieved if the scheduler entries RME and BCE with GM = 0 are only used. In this case, the gap condition is “ignored” for the transfer of a reference message. In order to avoid unintentional

transfers of reference messages, the external trigger generation should be switched off in this case.

24.9.5 Error Handling

The TTCAN error handling distinguishes among four levels of error severity:

- S0:
  No Error: Normal functionality
- S1:
  Warning: Only notification of the application by an interrupt (ERRS1).
  Source: Scheduling Error 1 (MSCmax - MSCmin > 2 or when MSC of a receive object equal 7), Tx_Underflow
- S2:
  Error: Notification of the application by an interrupt (ERRS2). All transmissions are disabled (except for reference messages), TTCFGR.RTO is set to 127.
  Source: Scheduling Error 2 (MSC of a transmit object reaches 7), Tx_overflow
  Impact: The transmit enable window will not be opened (for exclusive and for arbitration windows).
- S3:
  Severe Error: Notification of the application by an interrupt (ERRS3). All CAN bus actions are stopped (no dominant values are transmitted on the bus). The configuration phase is entered automatically (CFGM is set).
  Source: Application Watchdog, Bus Off, Config Error, Watch Trigger Event
  Impact: Bit INIT of the CAN node will be set (the CAN node stops actions on the bus).

Note: Any change of the error state can generate an interrupt.

24.9.6 Application Watchdog

The application watchdog provides the possibility of checking for the TTCAN module if the main system is still running. The application watchdog counter counts in steps of 256 NTUs.

Each time 256 NTUs have elapsed, the value AWDR.AWDV is decremented by one. If the value 0 is reached after decrementing, an S3 error is signaled by bit AWDERR. The falling edge of bit LTR.LT.7 (transition from 1 to 0) indicates that the time of 256 NTUs has elapsed and the application watch dog value is decremented.
The application watchdog is serviced by the program by writing a new value to the bit field AWDR.AWDE.

24.9.7 MSC Handling

The MSC bit field is updated only for those message objects that are indicated by the valid RCE or TCE entry while the corresponding bit MSGVAL is set. The message number taken into account for an update is defined in the respective bit fields RCEMSGNR or TCEMSGNR.
Checking for the receive/transmit condition takes place when the end of the transmit enable window of the following time marks is reached. Because the transmit enable window length is known after each time mark (even if no message shall be sent out), this point in time can be used for the receive and the transmit check.
This feature makes it possible to have a positive check result even if the message in the preceding time window finishes during the transmit enable window.

A transmission attempt is defined as failed if a message object valid for transmission could not be transferred on the CAN bus. A transmit trigger being active without a valid message object being found is not considered as a transmission attempt.

24.9.8 TTCAN Interrupt Control

Figure 24-35 and **Figure 24-36** show the configurations of the three TTCAN interrupts.

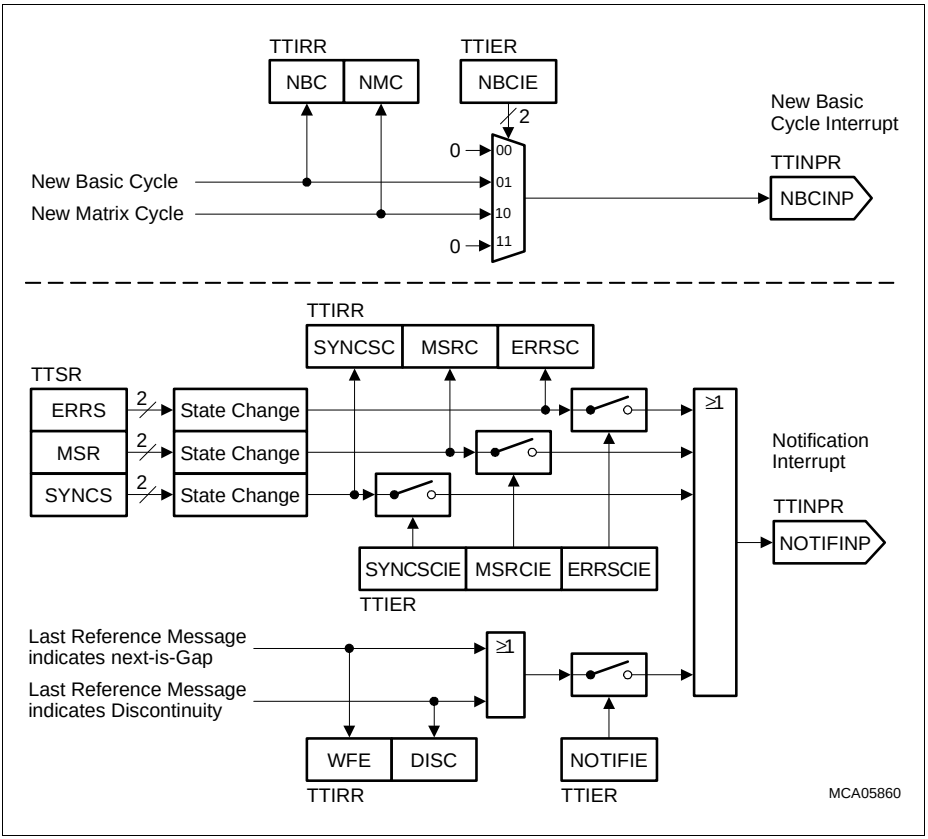


Figure 24-35 New Basic Cycle and Notification Interrupt Structure

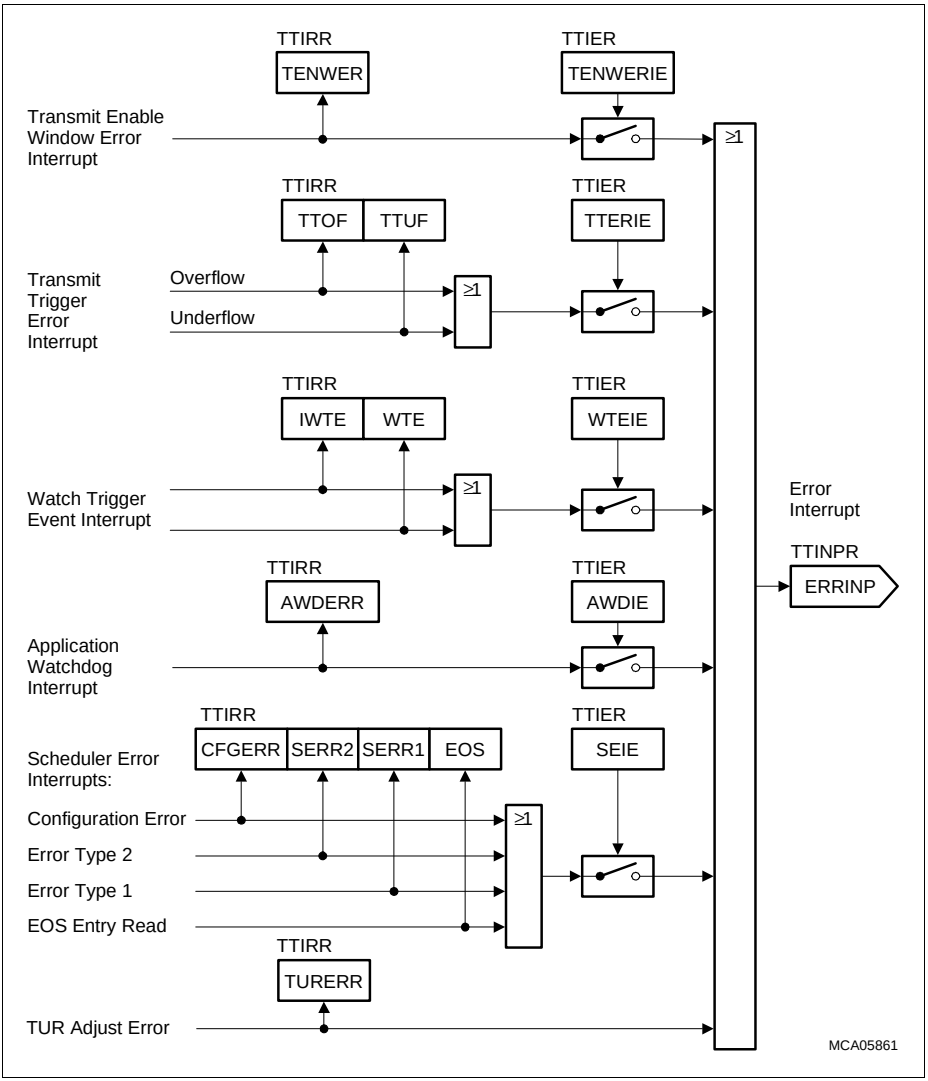


Figure 24-36 Error Interrupt Structure

See also **"Interrupt Control" on Page 24-211** for further processing of the TTCAN interrupts.

24.10 TTCAN Registers

All TTCAN register names described in this section are referenced by the module name prefix “CAN_” in other parts of the document.

TTCAN Register Overview

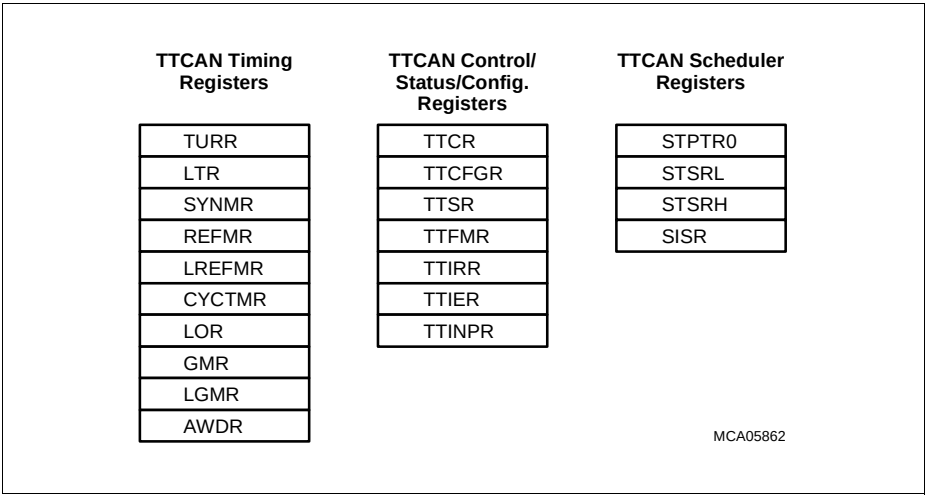


Figure 24-37 TTCAN Registers

Table 24-15 TTCAN Registers

Register Short Name	Register Long Name	Offset Address	Description see
LTR	Local Time Register	280_H	Page 24-162
SYNMR	Synchronization Mark Register	284_H	Page 24-163
REFMR	Reference Mark Register	288_H	Page 24-164
LREFMR	Last Reference Mark Register	$28C_H$	Page 24-165
TURR	Time Unit Ratio Register	290_H	Page 24-160
CYCTMR	Cycle Time Register	294_H	Page 24-166
LOR	Local Offset Register	298_H	Page 24-167
GMR	Global Mark Register	$29C_H$	Page 24-169
LGMR	Last Global Mark Register	$2A0_H$	Page 24-170
AWDR	Application Watchdog Register	$2A4_H$	Page 24-171

Table 24-15 TTCAN Registers (cont'd)

Register Short Name	Register Long Name	Offset Address	Description see
TTCR	Time Trigger Control Register	$2C0_H$	Page 24-172
TTCFGR	Time Trigger Configuration Register	$2C4_H$	Page 24-176
TTSR	Time Trigger Status Register	$2C8_H$	Page 24-178
TTFMR	Time Trigger Flag Modification Register	$2CC_H$	Page 24-183
TTIRR	Time Trigger Interrupt Request Register	$2D0_H$	Page 24-185
TTIER	Time Trigger Interrupt Enable Register	$2D4_H$	Page 24-189
TTINPR	Time Trigger Interrupt Node Pointer Register	$2D8_H$	Page 24-193
STSRL	Scheduler Timing Status Register Low	$2F0_H$	Page 24-196
STSRH	Scheduler Timing Status Register High	$2F4_H$	Page 24-197
SISR	Scheduler Instruction Status Register	$2F8_H$	Page 24-198
STPTR0	Scheduler Start Pointer Node 0 Register	$3FFC_H$	Page 24-195

Figure 24-38 shows the TTCAN register address map.

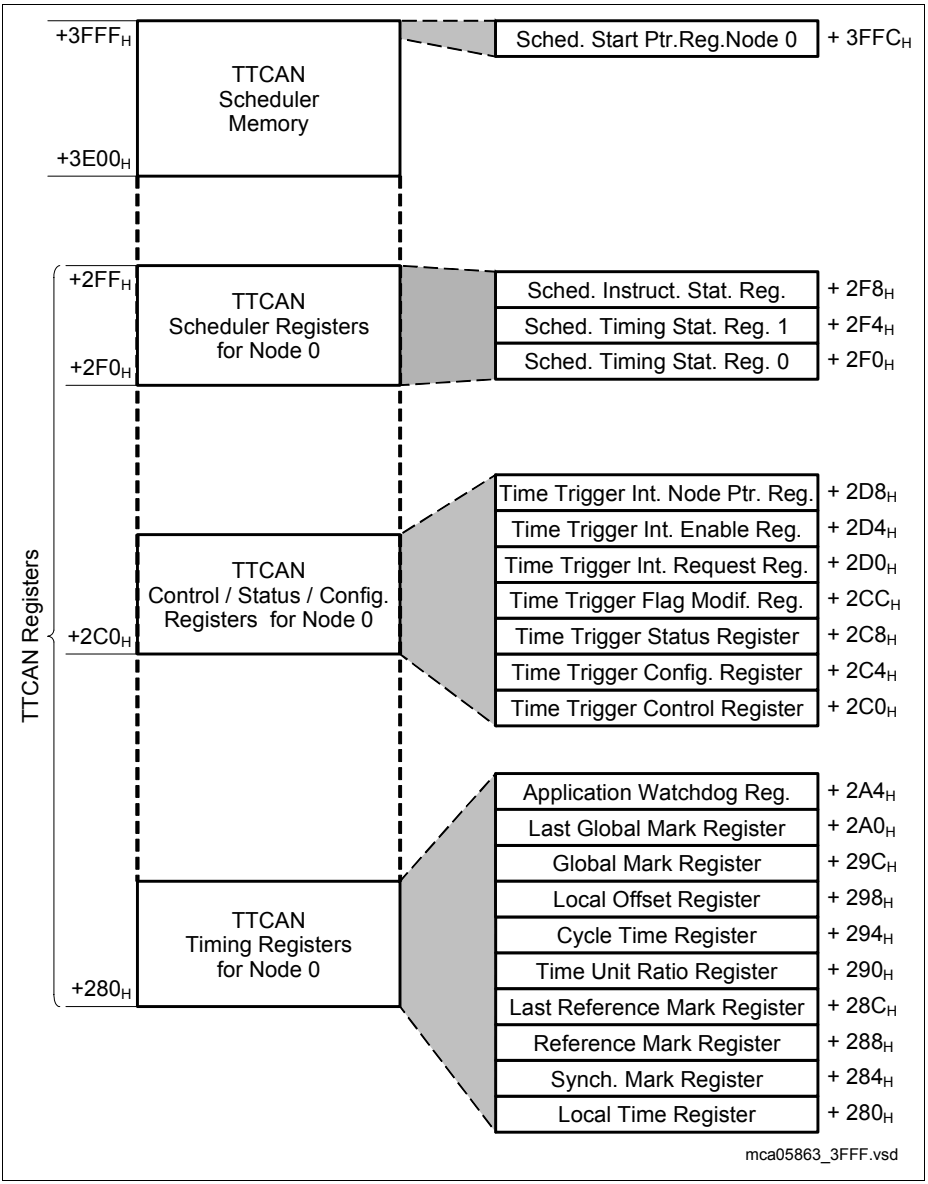


Figure 24-38 TTCAN Register Address Map

24.10.1 TTCAN Timing Registers

TURR
Time Unit Ratio Register **(290_H)** **Reset Value: $0000\ 0000_H$**

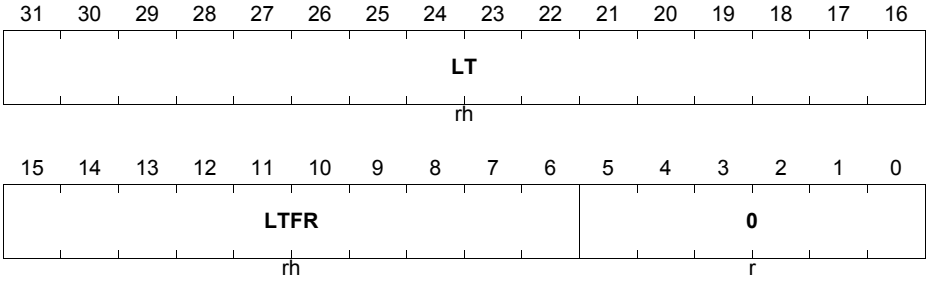
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TUR										0	LTDIV			LTCS	VAL
rh										r	rw			rw	rh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TURADJ										0					ADJEN
rwh										r					rwh

Field	Bits	Type	Description
ADJEN	0	rwh	**Adjust Enable** This bit enables automatic calculation of a new TURADJ value when a new reference message has been received (not for the current time master). A time unit ratio adjust error interrupt will be generated and bit ADJEN will be automatically cleared when an overflow or an underflow of the automatically calculated value occurs. 0_B The automatic TUR calculation is disabled. The new value for time unit ratio for TURADJ must be calculated and written by software. 1_B The automatic TUR calculation is enabled. After receiving a reference message, a new value for TURADJ is calculated by hardware. The calculated value is checked for overflow or underflow.
TURADJ	[15:6]	rwh	**Time Unit Ratio Adjust** This bit field holds the time unit ratio value that will be used for the next basic cycle. In the case of an automatic time unit ratio calculation with an underflow (overflow), TURADJ is written with all 0s (1s), ADJEN is cleared and a time unit ratio adjust error interrupt is generated. A hardware calculated TURADJ value can be overwritten by software.

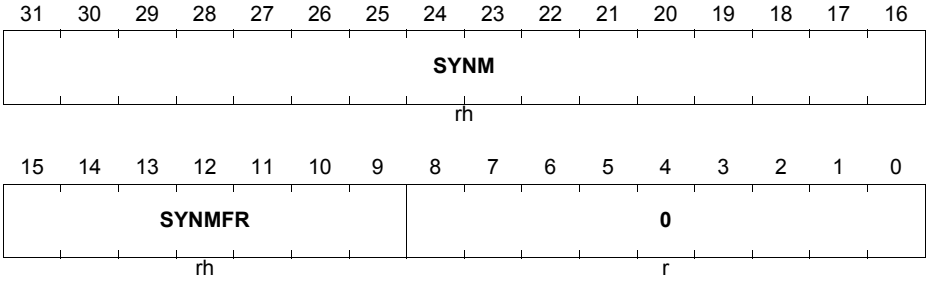
Field	Bits	Type	Description
VAL	16	rh	**Valid** This bit indicates that a new value of TURADJ is available. VAL becomes set when the hardware has finished its automatic calculation (with a correct result without overflow or underflow) or when the software writes to TURADJ. An automatic calculation does not take place while VAL = 1. VAL is cleared when the value of TURADJ is copied to TUR. 0_B The value of TURADJ has not been updated and no automatic update of TUR by the value of TURADJ takes place. 1_B The value of TURADJ has been updated by software or by hardware and it will be copied to TUR at the start of the next basic cycle.
LTCS	17	rw	**Local Time Clock Source** This bit determines the clock source for the local time generation (addition of TUR to LT, LTFR) for TTCAN level 2. 0_B A new local time value is generated with each time quantum t_q of the corresponding CAN node (depending on the CAN bit timing). 1_B The local time generation is based on the CAN module clock f_{CAN} (independent from the CAN bit timing). The update rate t_{upd} is based on the divider factor given by the bit field LTDIV according to: $t_{upd} = 2^{LTDIV} / f_{CAN}$
LTDIV	[20:18]	rw	**Local Time Divider** This bit field determines the divider factor for the local time generation (if f_{CAN} is selected by LTCS = 1). The divider factor is given by 2^{LTDIV}. 000_B Divider factor = 1 selected. 001_B Divider factor = 2 selected. $\ldots_B$ ... 111_B Divider factor = 128 selected.
TUR	[31:22]	rh	**TUR** This bit field contains the currently active time unit ratio value.
0	[5:1], 21	r	**Reserved** Read as 0; should be written with 0.

LTR
Local Time Register **(280_H)** **Reset Value: $0000\ 0000_H$**



Field	Bits	Type	Description
LTFR	[15:6]	rh	**Local Time Fraction** This bit field contains the fractional part of the NTU counter (TTCAN level 2 only). In the case of an overflow after the addition of the TUR value, the value of LT is incremented by one.
LT	[31:16]	rh	**Local Time** This bit field contains the integer part of the NTU counter. In TTCAN level 1, it is incremented with each CAN bit time, in level 2 it is incremented each time the fractional part LTFR has an overflow.
0	[5:0]	r	**Reserved** Read as 0; should be written with 0.

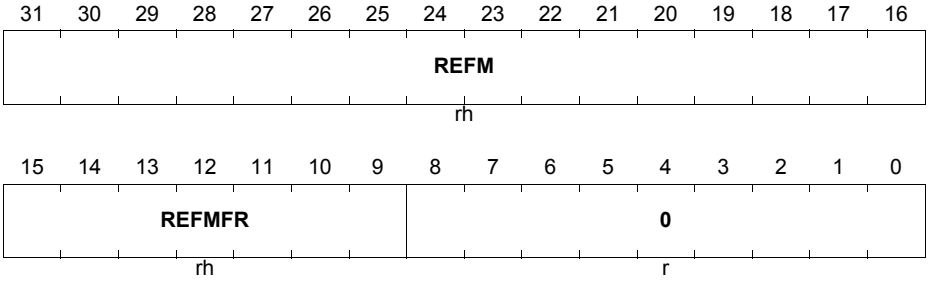
SYNMR
Synchronization Mark Register (284_H) Reset Value: 0000 0000$_H$



Field	Bits	Type	Description
SYNMFR	[15:9]	rh	**Synchronization Mark Fraction** This bit field contains the fractional part of the synchronization mark. SYNMFR is the bit field LTR.LTFR captured with the frame synchronization pulse.
SYNM	[31:16]	rh	**Synchronization Mark** This bit field contains the integer part of the synchronization mark. SYNM is the bit field LTR.LT captured with the frame synchronization pulse.
0	[8:0]	r	**Reserved** Read as 0; should be written with 0.

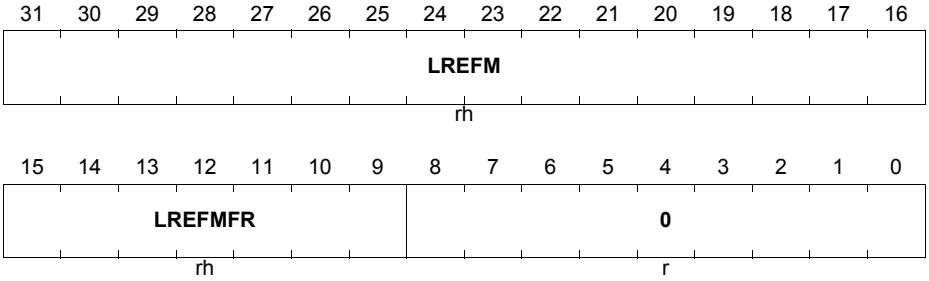
Note: If the CAN node is time master, the contents of register SYNMR are used as timing data transferred in the reference message.

REFMR
Reference Mark Register **(288_H)** **Reset Value: 0000 0000_H**



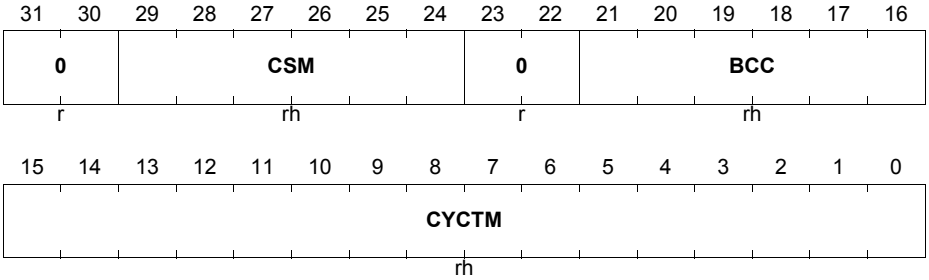
Field	Bits	Type	Description
REFMFR	[15:9]	rh	**Reference Mark Fraction** This bit field contains the fractional part of the reference mark. REFMFR is the bit field SYNMR.SYNMFR captured with the correct end of the reference message.
REFM	[31:16]	rh	**Reference Mark** This bit field contains the integer part of the reference mark. REFM is the bit field SYNMR.SYNM captured with the correct end of the reference message.
0	[8:0]	r	**Reserved** Read as 0; should be written with 0.

LREFMR
Last Reference Mark Register **($28C_H$)** **Reset Value: 0000 0000_H**



Field	Bits	Type	Description
LREFMFR	[15:9]	rh	**Last Reference Mark Fraction** This bit field contains the fractional part of the last reference mark. LREFMFR is the bit field REFMR.REFMFR captured with the correct end of the reference message.
LREFM	[31:16]	rh	**Last Reference Mark** This bit field contains the integer part of the last reference mark. LREFM is the bit field REFMR.REFM captured with the correct end of the reference message.
0	[8:0]	r	**Reserved** Read as 0; should be written with 0.

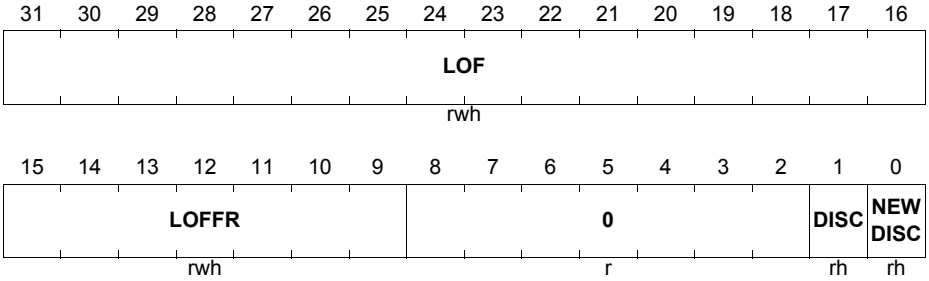
CYCTMR
Cycle Time Register **(294_H)** **Reset Value: $0000\ 0000_H$**



Field	Bits	Type	Description
CYCTM	[15:0]	rh	**Cycle Time** The cycle time indicates the time already elapsed in the current basic cycle. It is calculated by LTR.LT - REFMR.REFM. In the case of a negative result (overflow of LTR.LT), the result is corrected.
BCC	[21:16]	rh	**Basic Cycle Count** This bit field indicates the number of the current basic cycle. It is incremented after each correctly transferred reference message.
CSM	[29:24]	rh	**Column of System Matrix** This bit field indicates the number of the current column of the system matrix. It is incremented when the current cycle time becomes equal to the stored time mark (indicating the start of the next column).
0	[23:22], [31:30]	r	**Reserved** Read as 0; should be written with 0.

Note: With a reference message, the counting of the columns restarts at 0.

LOR
Local Offset Register **(298_H)** **Reset Value: 0000 0000_H**

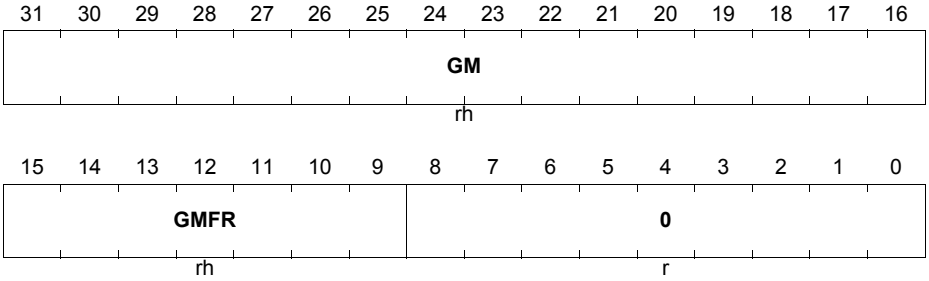


Field	Bits	Type	Description
NEWDISC	0	rh	**New Discontinuity Bit** This bit indicates that the register LOR has been the target of a write access for a time master (and that the contents of LOF or LOFFR could have been changed). This bit indicates that the next reference message will be sent with a discontinuity in the reference mark. It is set automatically when a write action to LOR is detected. It is cleared when the local time is captured (at SOF) for the transmission of the reference message. 0_B A write access to LOR has not occurred. 1_B A write access to LOR has occurred.
DISC	1	rh	**Discontinuity Bit** This bit contains the DISC bit of the reference message that is sent out (taken into account for a time master). This bit is set if the NEWDISC bit is 1 when the global time is captured (at SOF) for the transmission of the reference message. It is cleared when the reference message has been transferred correctly. 0_B The DISC bit in the reference message of the current time master is 0. 1_B The DISC bit in the reference message of the current time master is 1.
LOFFR	[15:9]	rwh	**Local Offset Fraction** This bit field contains the fractional part of the local offset.

Field	Bits	Type	Description
LOF	[31:16]	rwh	**Local Offset** This bit field contains the integer part of the local offset. Time master (transmitting reference messages): The sum of the local offset and the local time is stored as global time in the register GMR. Not time master (receiving reference messages): The local offset is the received global time information minus the local reference mark (in REFMR).
0	[8:2]	r	**Reserved** Read as 0; should be written with 0.

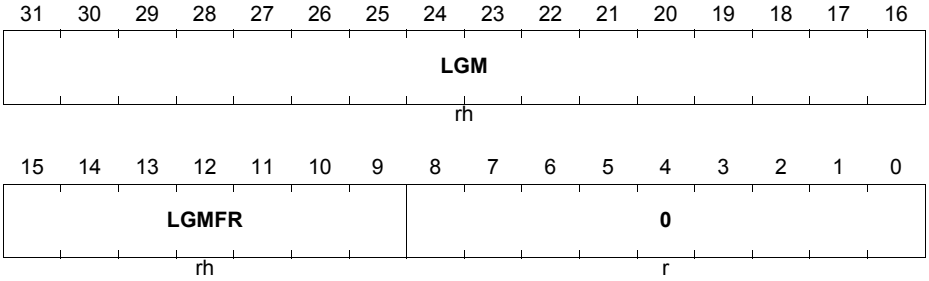
Note: Register LOR can be written by software only if the CAN node is the current time master or in Configuration Mode; otherwise, the write action is not taken into account. Because the written local offset is only taken into account for the transmission of the reference message, bit DISC is set automatically.

GMR
Global Mark Register **($29C_H$)** **Reset Value: 0000 0000$_H$**



Field	Bits	Type	Description
GMFR	[15:9]	rh	**Global Mark Fraction** This bit field contains the fractional part of the global mark.
GM	[31:16]	rh	**Global Mark** This bit field contains the integer part of the global mark. Time master (transmitting reference messages): The sum of the local offset and the local time is stored as global time (Global_Sync_Mark) in register GMR at the beginning of the reference message. Not time master (receiving reference messages): The global time information in GMR is received as Global_Ref_Mark by reference message.
0	[8:0]	r	**Reserved** Read as 0; should be written with 0.

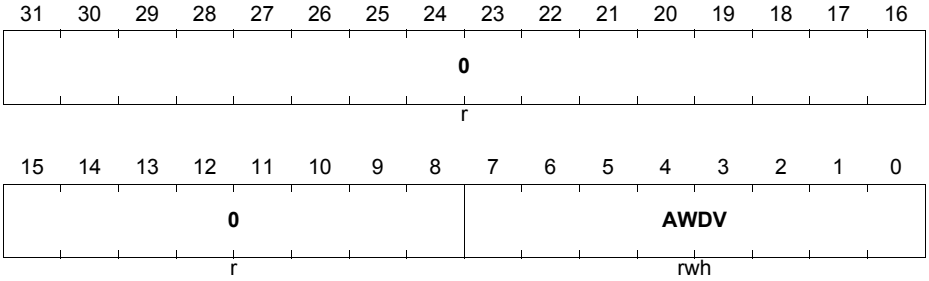
LGMR
Last Global Mark Register **($2A0_H$)** **Reset Value: $0000\ 0000_H$**



Field	Bits	Type	Description
LGMFR	[15:9]	rh	**Last Global Mark Fraction** This bit field contains the value of GMFR of the last reference mark.
LGM	[31:16]	rh	**Last Global Mark** This bit field contains the value of GM of the last reference mark.
0	[8:0]	r	**Reserved** Read as 0; should be written with 0.

Note: The difference between the actual global mark and the last one can be used to determine the value required for the TURR.TUR update (not for the actual time master).

AWDR
Application Watchdog Register ($2A4_H$) Reset Value: $0000\ 0000_H$

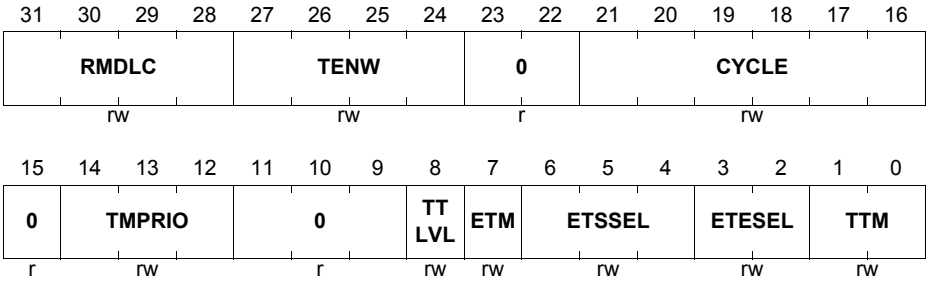


Field	Bits	Type	Description
AWDV	[7:0]	rwh	**Application Watchdog Value** This bit field contains the current value of the application watchdog. The falling edge of bit LTR.LT[7] (1-to-0 transition) indicates that the time of 256 NTUs has elapsed and the application watchdog value is automatically decremented by 1. If the value 0 is reached after decrementing, an S3 error is signaled by bit TTIRR.AWDERR. AWDV is not decremented below 0. The application watchdog is serviced by the program by writing a new value to the bit field AWDV. In the case of a collision between the write by software and the automatic decrement, the write is taken into account. Due to the fact that the counter counting the NTU (register LTR) is not reset when the application watchdog is serviced, the total time between the write to AWDV and the signaling of an S3 error has an uncertainty of one step of AWDV.
0	[31:8]	r	**Reserved** Read as 0; should be written with 0.

The application watchdog event occurs when the value of AWDV is decremented and reaches zero. When writing 0 to AWDV by software, the application watchdog is switched off without generating an application watchdog event.

24.10.2 TTCAN Control / Status / Configuration Registers

TTCR
Time Trigger Control Register **($2C0_H$)** **Reset Value: $0000\ 0000_H$**



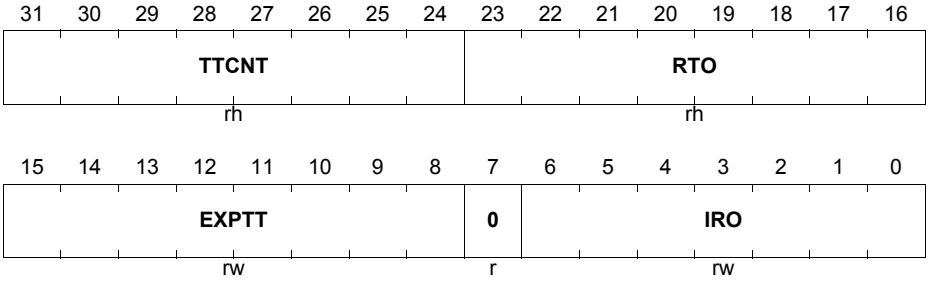
Field	Bits	Type	Description
TTM	[1:0]	rw	**Time Trigger Mode** This bit determines the behavior of the TTCAN node concerning the time trigger and the time master functionality. 00_B CAN node is disabled for TTCAN operation and operates in event triggered mode (other settings for TTCAN are inactive). The reference message object operates for reception or transmission as any other message object. 01_B CAN node is enabled for TTCAN operation as a receiving device. Reference messages cannot be transmitted by the CAN node. 10_B CAN node is enabled for TTCAN operation as the actual or a potential time master. The CAN node is able to transmit the reference message. 11_B Reserved; do not use this combination.

Field	Bits	Type	Description
ETESEL	[3:2]	rw	**External Trigger Event Selection** This bit field determines the source of the external trigger event that can be used to trigger a transmission of the reference message. The transmission of the reference message will be triggered only when the external event is detected and the external trigger request bit TTSR.ETR is set (= 1). 00_B Reserved; external trigger does not trigger the transmission of the reference message. 01_B A negative edge at an external trigger input ECTTx (as selected by ETSSEL) triggers the transmission of the reference message. 10_B A positive edge at an external trigger input ECTTx (as selected by ETSSEL) triggers the transmission of the reference message. 11_B A negative or positive edge at an external trigger input ECTTx (as selected by ETSSEL) triggers the transmission of the reference message.
ETSSEL	[6:4]	rw	**External Trigger Source Selection** This bit fields selects the input source for the external reference message trigger. 000_B No external trigger possible. 001_B External trigger input line ECTT1 selected. 010_B External trigger input line ECTT2 selected. 010_B External trigger input line ECTT3 selected. 100_B External trigger input line ECTT4 selected. 101_B External trigger input line ECTT5 selected. 110_B External trigger input line ECTT6 selected. 111_B External trigger input line ECTT7 selected.

Field	Bits	Type	Description
ETM	7	rw	**External Trigger Mode** This bit determines the external trigger mode. The transfer of a reference message is started if the selected trigger condition is met when the bus is idle after the end of the transmit enable window of the last time window of a basic cycle. The trigger event is stored in ETREV. 0_B The trigger event itself is taken into account if it occurs after the end of the transmit enable window of the last time window of a basic cycle. 1_B The trigger event stored in ETREV is taken into account after the end of the transmit enable window of the last time window of a basic cycle.
TTLVL	8	rw	**Time Trigger Level** This bit determines the level of the TTCAN functionality. 0_B TTCAN level 1 is selected. 1_B TTCAN level 2 is selected.
TMPRIO	[14:12]	rw	**Time Master Priority** This bit field determines the priority of the potential time master. This value will be used for the transmission of the ID bits [2:0] of the reference message. In the case that the TTCAN node looses arbitration against another reference mark on the bus or receives a reference mark while its own reference trigger is set, the reference trigger is reset and the received ID is stored in the reference message object's ID bit field.
CYCLE	[21:16]	rw	**Basic Cycle Number** This bit field determines the number of the last basic cycle in the matrix cycle. For time masters, the value of CYCLE is compared to the current value of the bit field CYCTMR.BCC. If the comparison detects a match, the reference message is sent out with a new basic cycle count of 0. For slave devices, the value is used to detect the expected end of a matrix cycle.

Field	Bits	Type	Description
TENW	[27:24]	rw	**Transmit Enable Window** This bit field determines how many CAN bit times can elapse before a pending transmit trigger is discarded. 0000_B One CAN bit time can elapse. 0001_B Two CAN bit times can elapse. $\cdots_B$ ... 1110_B Fifteen CAN bit times can elapse. 1111_B Sixteen CAN bit times can elapse.
RMDLC	[31:28]	rw	**Reference Message DLC** This bit field determines the data length code DLC of reference messages sent out by this CAN node if it is a time master. The DLC bit field in the reference message object contains the DLC of the previously received reference message. Note that RMDLC must be programmed only to values from 1 to 8 for TTCAN level 1 and to values from 4 to 8 for TTCAN level 2. Other values must not be programmed.
0	[11:9], 15, [23:22]	r	**Reserved** Read as 0; should be written with 0.

TTCFGR
Time Trigger Configuration Register (2C4$_H$) **Reset Value: 0000 0000$_H$**



Field	Bits	Type	Description
IRO	[6:0]	rw	**Initial Reference Offset** This bit field determines the initial reference trigger offset. The value is considered as 2's complement and can reach values between 0 and 127.
EXPTT	[15:8]	rw	**Expected Transmit Triggers** This bit field determines how many transmit requests are expected in a matrix cycle.
RTO	[23:16]	rh	**Reference Trigger Offset** This bit field indicates the actual reference trigger offset. This value is considered as 2's complement and can reach values between -127 and 127. It is added to the time mark (given by the basic cycle end entry in the scheduler memory) for the trigger of the reference message. The modification and the corresponding conditions are listed in **Table 24-16**.
TTCNT	[31:24]	rh	**Transmit Trigger Counter** The transmit trigger counter is incremented by 1 each time a transmit trigger is requested for a TTCAN node. When reaching the value of EXPTT, it is no longer incremented and further transmit requests are not serviced (messages are not transferred). It is reset at the beginning of each new matrix cycle (after correct transfer on the reference message of basic cycle 0).

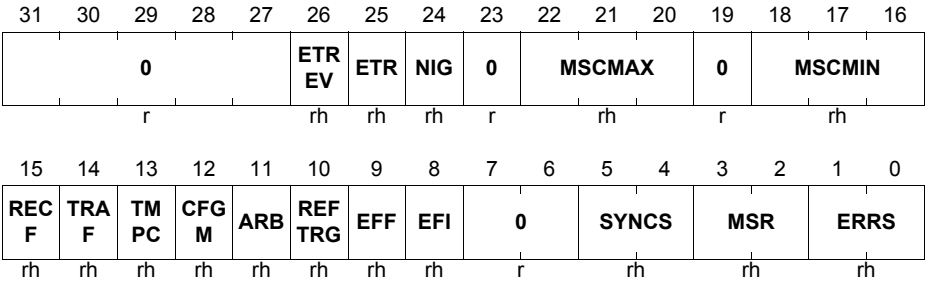
Field	Bits	Type	Description
0	7	r	**Reserved** Read as 0; should be written with 0.

Table 24-16 Modification by Hardware of Bit Field RTO

Modification	Condition
Set to TTCFGR.IRO	During reset (TTCFGR.IRO = 0) and Configuration Mode (write of TTCFGR.IRO by software)
Set to TTCFGR.IRO	Each time a potential time master receives a reference message with a higher priority than its own
Decrement by 1	Each time a potential time master receives a reference message with a lower priority than its own until -127 is reached
Set to 127	When the S2 state is entered
Set to 0	When the TTCAN node has correctly transmitted its reference message (it is the current time master) or when a potential master receives a reference message with a priority lower than its own and its RTO is positive

The Time Trigger Status Register TTSR contains the time trigger status information that does not lead directly to interrupt events.

TTSR
Time Trigger Status Register **($2C8_H$)** **Reset Value: $0000\ 1000_H$**



Field	Bits	Type	Description
ERRS	[1:0]	rh	**Error State** This bit field indicates the current error severity level. 00_B No error 01_B Warning 10_B Error 11_B Severe error
MSR	[3:2]	rh	**Master-Slave Relation** This bit field indicates the current master to slave relation of the TTCAN node. 00_B Master off 01_B Slave (receiving device) 10_B Potential time master 11_B Current time master
SYNCS	[5:4]	rh	**Synchronization State** This bit field indicates the current synchronization state of the TTCAN node. 00_B Sync off 01_B Synchronizing 10_B In gap 11_B In schedule

Field	Bits	Type	Description
EFI	8	rh	**Error Frame Indication** This bit is set when an error condition in the bitstream of a CAN frame is detected and an Error Frame will be sent out. It is automatically cleared when the next time mark is reached and its status at this moment is monitored by bit EFF. 0_B Since the last time mark, the CAN node has detected no error condition in the CAN bitstream. 1_B Since the last time mark, the CAN node has detected an error condition in the CAN bitstream. When EFI becomes set, a LEC interrupt can be generated by the CAN node.
EFF	9	rh	**Error Frame Flag** This bit monitors the Error Frame indication EFI when a time mark is reached. 0_B No CAN error has been detected in the last time window. 1_B A CAN error has been detected in the last time window.
REFTRG	10	rh	**Reference Trigger Flag** This bit is set when the reference message of a TTCAN node is intended to be sent. It is cleared when the reference message has been sent out correctly or a reference message has been received correctly (sent by another time master).
ARB	11	rh	**Arbitration Window Flag** This bit is set when an arbitration window is opened. It is cleared when the arbitration window is closed. 0_B The current time window is a time-triggered window. 1_B The current time window is an arbitration window.

Field	Bits	Type	Description
CFGM	12	rh	**Configuration Mode Flag** This bit indicates whether or not Configuration Mode is active. 0_B The TTCAN node is not in Configuration Mode. 1_B The TTCAN node is in Configuration Mode. It will not transmit messages and it will not update the MSC bit fields.
TMPC	13	rh	**Time Master Priority Conflict** This bit indicates if there is a priority conflict between the current time master and this TTCAN node. A priority conflict occurs if the current time master has a lower priority than the TTCAN node itself (potential time master). 0_B A priority conflict has not been detected for the last reference message. 1_B The TTCAN node is a potential time master with a priority conflict (the last reference message has been received with a lower priority than TTCR.TMPRIO).
TRAF	14	rh	**Transmission Finished Flag** This bit is set when the CAN node correctly finishes a transmission of a message that is not the reference message. It is reset when the next time mark is reached. This flag is used for the interrupt generation of the time mark entries and the interrupt entries. 0_B Since the last time mark has been reached, the CAN node has not yet correctly finished a transmission. 1_B Since the last time mark has been reached, the CAN node has correctly finished a transmission (it is not set by the transmission of a reference message).

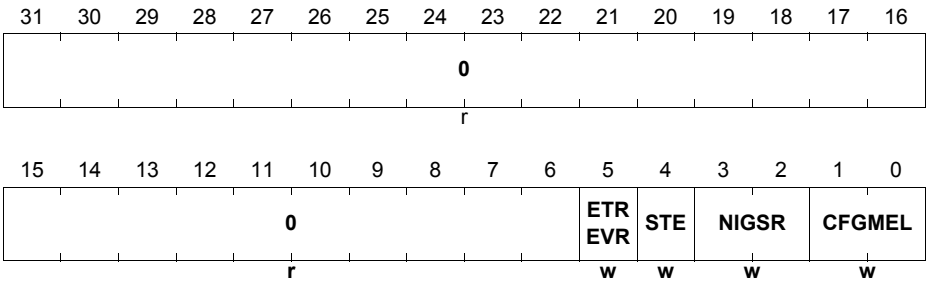
Field	Bits	Type	Description
RECF	15	rh	**Reception Finished Flag** TThis bit is set when the CAN node correctly finishes a reception of a message (= a correct message has been seen on the bus) that is not the reference message. It is reset when the next time mark is reached. This flag is used for the interrupt generation of the time mark entries and the interrupt entries. 0_B Since the last time mark has been reached, the CAN node has not yet received a message. 1_B Since the last time mark has been reached, the CAN node has received a message (it is not set by the reference message).
MSCMIN	[18:16]	rh	**Minimum of MSC Bit Fields** This bit field indicates the minimum value of the MSC bit fields of the message objects activated in exclusive time windows. This value is set to 7 at the beginning of a new matrix cycle. It is updated according to: *Note: if MSC_cur < MSCMIN then* *MSCMIN:= MSC_cur* The value MSC_cur is the MSC value of the currently activated message object.
MSCMAX	[22:20]	rh	**Maximum of MSC Bit Fields** This bit field indicates the maximum value of the MSC bit fields of the message objects activated in exclusive time windows. This value is set to 0 at the beginning of a new matrix cycle. It is updated according to: *Note: if MSC_cur > MSCMAX then* *MSCMAX:= MSC_cur* The value MSC_cur is the MSC value of the currently activated message object.

Field	Bits	Type	Description
NIG	24	rh	**Next Is Gap** This bit indicates the condition leading to the transmission of the reference message coming after the next one (only for the current time master). This bit will be transmitted with the next reference message. 0_B The reference message after the next one will be transmitted when the corresponding time mark is reached. 1_B The reference message after the next one will be transmitted when the selected trigger event occurs. Bit NIG will be cleared and bit ETR will be set when the next reference message is correctly transferred (received or transmitted).
ETR	25	rh	**External Trigger Request** This bit indicates the condition leading to the transmission of the next reference message (only for the current time master).The value of NIG is copied to ETR when a reference message is correctly transmitted. It will be cleared automatically when the next reference message is correctly received. 0_B The next reference message will be transmitted when the corresponding time mark is reached. 1_B The next reference message will be transmitted when the selected trigger or the RME trigger event occurs.
ETREV	26	rh	**External Trigger Event** This bit indicates that the external trigger event has been detected. It is automatically cleared when a reference message has been transferred correctly on the bus. 0_B The selected external trigger event has not yet been detected. 1_B The selected external trigger event has been detected.
0	[7:6], 19, 23, [31:27]	r	**Reserved** Read as 0; should be written with 0.

TTCAN status bits/flags can be modified when executing a write operation to the Time Trigger Flag Modification Register TTFMR.

TTFMR
Time Trigger Flag Modification Register

($2CC_H$) **Reset Value: $0000\ 0000_H$**



Field	Bits	Type	Description
CFGMEL	[1:0]	w	**Configuration Mode Enter/Leave** This bit field is used to enter/leave the Configuration Mode. 00_B No action 01_B The Configuration Mode will be entered (set TTSR.CFGM). 10_B The Configuration Mode will be left (clear TTSR.CFGM). 11_B No action
NIGSR	[3:2]	w	**Next Is Gap Flag Set/Reset** This bit field can set/clear the bit TTSR.NIG and can clear the bit TTSR.ETR. 00_B No action 01_B Bit TTSR.NIG will be set. 10_B Bits TTSR.NIG and TTSR.ETR will be cleared. 11_B No action

Field	Bits	Type	Description
STE	4	w	**Software Trigger Event** This bit can be used to synchronize a TTCAN node by software. 0_B No action 1_B The transmission of a reference message is triggered if TTCR.ETESEL = 11 and the system is in-a-gap.
ETREVR	5	w	**Reset External Trigger Event** This bit clears the external trigger event flag. 0_B No action. 1_B The bit TTSR.ETREV is cleared.
0	[31:6]	r	**Reserved** Read as 0; should be written with 0.

The Time Trigger Interrupt Request Register TTIRR contains the time trigger status information related to interrupt events. Note that all bits in TTIRR can be cleared by software by writing 0 to it. Writing a 1 to the bits has no effect.

TTIRR
Time Trigger Interrupt Request Register

($2D0_H$) **Reset Value: $0000\ 0000_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0														TURERR	CFGERR
r														rwh	rwh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SERR2	SERR1	DISC	WFE	EOS	SYNCSC	MSRC	ERRSC	AWDERR	IWTE	WTE	TTOF	TTUF	TENWER	NBC	NMC
rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh

Field	Bits	Type	Description
NMC	0	rwh	**New Matrix Cycle** This bit indicates that a new matrix cycle has started. It is set when a reference message with the cycle count = 0 has been transferred correctly. 0_B A new matrix cycle has not yet been detected. 1_B A new matrix cycle has been detected.
NBC	1	rwh	**New Basic Cycle** This bit indicates that a new basic cycle has started. 0_B A new basic cycle has not yet been detected. 1_B A new basic cycle has been detected.
TENWER	2	rwh	**Transmit Enable Window Error** This bit indicates that the specified time elapsed after the transmit trigger without starting the transmission of a message. 0_B The triggered messages have been sent out before the transmit enable window elapsed. 1_B A triggered message was not started before the transmit enable window elapsed.

Field	Bits	Type	Description
TTUF	3	rwh	**Transmit Trigger Underflow** This bit indicates that fewer transmit triggers have been requested during a matrix cycle than specified in TTCFGR.EXPTT. 0_B The expected number or more transmit triggers have been requested. 1_B Less transmit triggers have been requested.
TTOF	4	rwh	**Transmit Trigger Overflow** This bit indicates that more transmit triggers have been requested during a matrix cycle than specified in TTCFGR.EXPTT. 0_B The expected number or less transmit triggers have been requested. 1_B More transmit triggers have been requested.
WTE	5	rwh	**Watch Trigger Event**[1)] This bit indicates a watch trigger event WTE. This event is detected when the cycle time in CYCTMR.CYCTM becomes equal to the watch trigger value given by the time mark of the BCE entry. 0_B The cycle time has not been equal to WTV. 1_B The cycle time has been equal to WTV.
IWTE	6	rwh	**Init Watch Trigger Event**[2)] This bit indicates a watch trigger event WTE with the value of the Init_Watch_Trigger. This event is detected when the cycle time in CYCTMR.CYCTM becomes equal to the init watch trigger value of 2^{16} - 1. 0_B The cycle time has not been equal to 2^{16} - 1. 1_B The cycle time has been equal to 2^{16} - 1.
AWDERR	7	rwh	**Application Watchdog Error** This bit indicates that the application watchdog has been decremented to 0 without being serviced. 0_B AWDR.AWDV has not yet reached 00_H. 1_B AWDR.AWDV has reached 00_H. This is an S3 error condition.

Field	Bits	Type	Description
ERRSC	8	rwh	**Error State Change** This bit indicates that the bit field TTSR.ERRS has changed. 0_B TTSR.ERRS has not changed. 1_B TTSR.ERRS has changed.
MSRC	9	rwh	**Master-Slave Relation Change** This bit indicates that the bit field MSR has changed. 0_B TTSR.MSR has not changed. 1_B TTSR.MSR has changed.
SYNCSC	10	rwh	**Synchronization State Change** This bit indicates that the bit field TTSR.SYNCS has changed. 0_B TTSR.SYNCS has not changed. 1_B TTSR.SYNCS has changed.
EOS	11	rwh	**End Of Scheduler Entry Flag** This bit is set when the TTCAN scheduler reads an EOS entry. In this case, bit TTSR.CFGM is automatically set. 0_B The TTCAN scheduler has not yet read an EOS entry. 1_B The TTCAN scheduler has read an EOS entry.
WFE	12	rwh	**Wait For Event Flag** This bit is set when a reference message is received indicating a next-is-gap (not for the current time master). This event can generate a notification interrupt. 0_B The last reference message received was not indicating next-is-gap. 1_B The last reference message received was indicating next-is-gap.
DISC	13	rwh	**Discontinuity Flag** This bit is set when a reference message is received indicating a discontinuity (not for the current time master). This event can generate a notification interrupt. 0_B The last reference message received was not indicating a discontinuity. 1_B The last reference message received was indicating a discontinuity.

Field	Bits	Type	Description
SERR1	14	rwh	**Scheduler Error 1 Flag** This bit is set when a scheduler error type 1 is detected. The scheduler error can change the TTCAN error state and, as a result, can be indicated by an error state change interrupt. 0_B A scheduler error type 1 has not been detected. 1_B A scheduler error type 1 has been detected.
SERR2	15	rwh	**Scheduler Error 2 Flag** This bit is set when a scheduler error type 2 is detected. The scheduler error can change the TTCAN error state and, as a result, can be indicated by an error state change interrupt. 0_B A scheduler error type 2 has not been detected. 1_B A scheduler error type 2 has been detected.
CFGERR	16	rwh	**Configuration Error** This bit indicates that a configuration error has been detected by the scheduler. A configuration error is detected when an arbitration window is not closed when the BCE is reached. When RME.TMV is reached, no other scheduler entries as RME and BCE are allowed. See also EOSERR. 0_B A configuration error has not been detected. 1_B A configuration error has been detected (S3 error condition).
TURERR	17	rwh	**TUR Adjust Error** This bit indicates that a TUR adjust error has been detected. A TUR adjust error is detected when the automatic TUR adjustment is enabled and an overflow or an underflow of the calculated TURADJ value occurs. 0_B A TUR adjust error has not been detected. 1_B A TUR adjust error has been detected.
0	[31:18]	r	**Reserved** Read as 0; should be written with 0.

1) The WTE can be generated only after the first message has been transferred on the bus.

2) The IWTE can be generated only until the first message has been transferred on the bus.

TTIER

Time Trigger Interrupt Enable Register

(2D4$_H$) **Reset Value: 0000 0000$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0			NOTIFIE	SEIE	SYNCSCIE	MSRCIE	ERRSCIE	AWDIE	WTEIE	0		TTERIE	TENWERIE	NBCIE	
r			rw	rw	rw	rw	rw	rw	rw	r		rw	rw	rw	

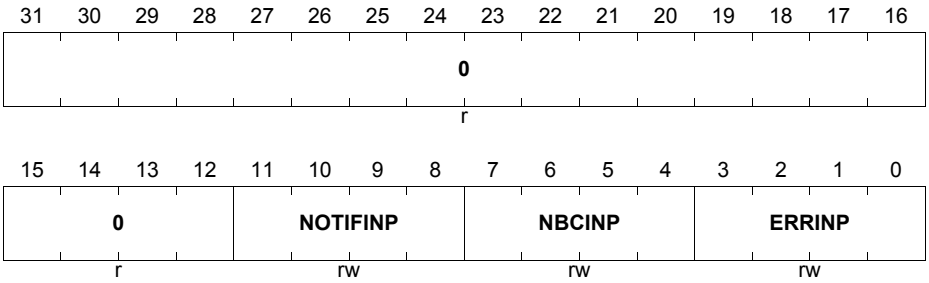
Field	Bits	Type	Description
NBCIE	[1:0]	rw	**New Basic Cycle Interrupt Enable** NBCIE enables the new basic or matrix cycle interrupt. This interrupt is generated when either bit TTIRR.NBC or bit TTIRR.NMC become set (independent of its current state). 00_B A new basic or matrix cycle interrupt is disabled. 01_B A basic cycle interrupt is generated whenever TTIRR.NBC becomes set. 10_B A matrix cycle interrupt is generated whenever TTIRR.NMC becomes set. 11_B Reserved Bit field TTINPR.NBCINP selects the interrupt output line that becomes activated at this type of interrupt.
TENWERIE	2	rw	**Transmit Enable Window Error Interrupt Enable** TENWERIE enables the transmit enable window error interrupt. This interrupt is generated when bit TTIRR.TENWER is set. 0_B Transmit enable window error interrupt is disabled. 1_B Transmit enable window error interrupt is enabled. Bit field TTINPR.ERRINP selects the interrupt output line that becomes activated at this type of interrupt.

Field	Bits	Type	Description
TTERIE	3	rw	**Transmit Trigger Error Interrupt Enable** TTERIE enables the transmit trigger error interrupt. This interrupt is generated when TTIRR.TTOF or TTIRR.TTUF become set (independent of its current state). 0_B Transmit trigger error interrupt is disabled. 1_B Transmit trigger error interrupt is enabled. Bit field TTINPR.ERRINP selects the interrupt output line that becomes activated at this type of interrupt.
WTEIE	6	rw	**Watch Trigger Event Interrupt Enable** WTEIE enables the watch trigger event interrupt. This interrupt is generated when TTIRR.IWTE or TTIRR.WTE become set (independent of its current state). 0_B Watch trigger event interrupt is disabled. 1_B Watch trigger event interrupt is enabled. Bit field TTINPR.ERRINP selects the interrupt output line that becomes activated at this type of interrupt.
AWDIE	7	rw	**Application Watchdog Interrupt Enable** AWDIE enables the application watchdog interrupt. This interrupt is generated when TTIRR.AWDERR becomes set (independent of its current state). 0_B Application watchdog interrupt is disabled. 1_B Application watchdog interrupt is enabled. Bit field TTINPR.ERRINP selects the interrupt output line that becomes activated at this type of interrupt.
ERRSCIE	8	rw	**Error State Change Interrupt Enable** ERRSCIE enables the error state change interrupt. This interrupt is generated when bit field TTSR.ERRSC changes its state. 0_B Error state change interrupt is disabled. 1_B Error state change interrupt is enabled. Bit field TTINPR.NOTIFINP selects the interrupt output line that becomes activated at this type of interrupt.

Field	Bits	Type	Description
MSRCIE	9	rw	**Master Slave Relation Change Interrupt Enable** MSRSCIE enables the master slave relation change interrupt. This interrupt is generated when bit field TTSR.MSRC changes its state. 0_B Master slave relation change interrupt is disabled. 1_B Master slave relation change interrupt is enabled. Bit field TTINPR.NOTIFINP selects the interrupt output line that becomes activated at this type of interrupt.
SYNCSCIE	10	rw	**Synchronization State Change Interrupt Enable** SYNCSCIE enables the synchronization state change interrupt. This interrupt is generated when bit field TTSR.SYNCSC changes its state. 0_B Synchronization state change interrupt is disabled. 1_B Synchronization state change interrupt is enabled. Bit field TTINPR.NOTIFINP selects the interrupt output line that becomes activated at this type of interrupt.
SEIE	11	rw	**Scheduler Error Interrupt Enable** SEIE enables the scheduler error interrupt. This interrupt is generated whenever bits EOS or SERR1 or SERR2 or CFGERR of register TTSR are set by hardware. 0_B Scheduler error interrupt generation is disabled. 1_B Scheduler error interrupt generation is enabled. Bit field TTINPR.ERRINP selects the interrupt output line that becomes activated at this type of interrupt.

Field	Bits	Type	Description
NOTIFIE	12	rw	**Notification Interrupt Enable** NOTIFIE enables the notification interrupt. This interrupt is generated whenever bits TTIRR.WFE or TTIRR.DISC are set by hardware. 0_B Notification interrupt is disabled. 1_B Notification interrupt is enabled. Bit field TTINPR.NOTIFINP selects the interrupt output line which becomes activated at this type of interrupt.
0	[5:4], [31:13]	r	**Reserved** Read as 0; should be written with 0.

TTINPR
Time Trigger Interrupt Node Pointer Register
($2D8_H$) **Reset Value: $0000\ 0000_H$**



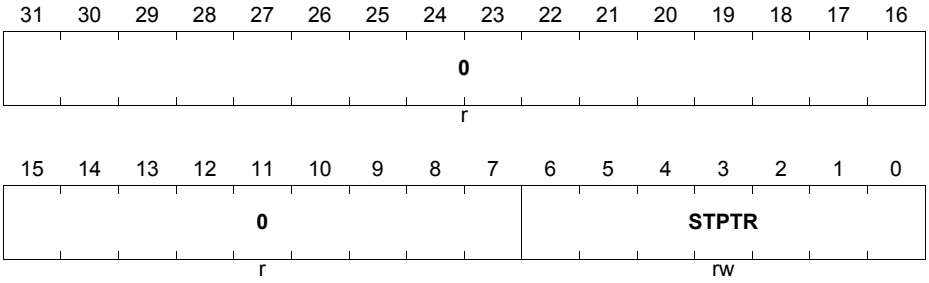
Field	Bits	Type	Description
ERRINP	[3:0]	rw	**Error Interrupt Node Pointer** ERRINP selects the interrupt output line INT_Om (m = 0-15) for an error interrupt. Possible error events for this interrupt node pointer are: • Transmit enable window error event • Transmit trigger error event • (Initial) Watch trigger event • Application watchdog event • TUR adjust error • Scheduler error event 0000_B Interrupt output line INT_O0 is selected. 0001_B Interrupt output line INT_O1 is selected. $\cdots_B$ … 1110_B Interrupt output line INT_O14 is selected. 1111_B Interrupt output line INT_O15 is selected.
NBCINP	[7:4]	rw	**New Basic Cycle Interrupt Node Pointer** NBCINP selects the interrupt output line INT_Om (m = 0-15) for a new basic or matrix cycle interrupt. 0000_B Interrupt output line INT_O0 is selected. 0001_B Interrupt output line INT_O1 is selected. $\cdots_B$ … 1110_B Interrupt output line INT_O14 is selected. 1111_B Interrupt output line INT_O15 is selected.

Field	Bits	Type	Description
NOTIFINP	[11:8]	rw	**Notification Interrupt Node Pointer** NOTIFINP selects the interrupt output line INT_Om (m = 0-15) for a notification interrupt. Possible notification events for this interrupt node pointer are: • bit field TTSR.ERRS changes • bit field TTSR.MSR changes • bit field TTSR.SYNCS changes • bit TTIRR.WFE is set • bit TTIRR.DISC is set 0000_B Interrupt output line INT_O0 is selected. 0001_B Interrupt output line INT_O1 is selected. $\ldots_B$ … 1110_B Interrupt output line INT_O14 is selected. 1111_B Interrupt output line INT_O15 is selected.
0	[31:12]	r	**Reserved** Read as 0; should be written with 0.

24.10.3 Scheduler Registers

STPTR0
Scheduler Start Pointer Node 0 Register

(3FFC$_H$) **Reset Value: 0000 0000$_H$**

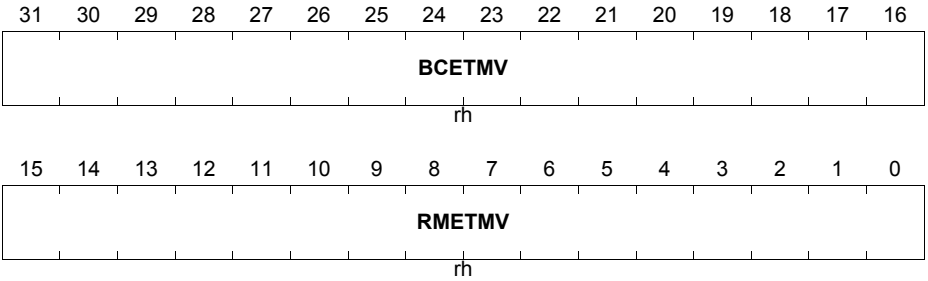


Field	Bits	Type	Description
STPTR	[6:0]	rh	**Start Pointer** This bit field determines the location of the first scheduler entry for TTCAN node 0. The value determines how many entries (counted in units of 32 bits) the first TME entry (TME1) for this TTCAN node is located below the last address of the scheduler memory. If two or more TTCAN nodes are implemented, all start pointers refer to the end (last address) of the scheduler memory.
0	[31:7]	r	**Reserved** Read as 0; should be written with 0.

The TMV bit fields in the scheduler timing status registers monitor the time mark information for the start of the next time window after the instruction collection phase of the scheduler (collected from the TME, RME or BCE entries).

STSRL
Scheduler Timing Status Register Low

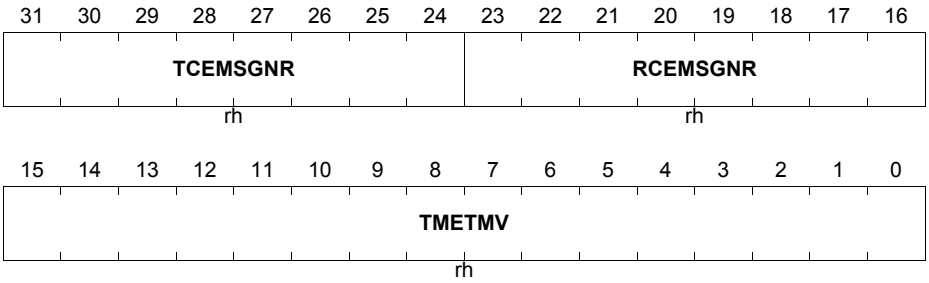
($2F0_H$) **Reset Value: 0000 0000_H**



Field	Bits	Type	Description
RMETMV	[15:0]	rh	**Time Mark Value from RME** This bit field indicates the compare value for the next time mark defined by an RME. This value is valid only if SISR.ICF = 1 and SISR.RMEV = 1.
BCETMV	[31:16]	rh	**Time Mark Value from BCE** This bit field indicates the compare value for the next time mark defined by an BCE. This value is valid only if SISR.ICF = 1 and SISR.BCEV = 1.

STSRH
Scheduler Timing Status Register High

(2F4$_H$) Reset Value: 0000 0000$_H$



Field	Bits	Type	Description
TMETMV	[15:0]	rh	**Time Mark Value from TME** This bit field indicates the compare value for the next time mark defined by an TME. This value is valid only if SISR.ICF = 1 and SISR.TMEV = 1.
RCEMSGNR	[23:16]	rh	**Receive Control Entry Message Number** This bit field indicates the collected RCEMSGNR information from an RCE. This value is taken into account only if SISR.ICF = 1 and SISR.RCEV = 1.
TCEMSGNR	[31:24]	rh	**Transmit Control Entry Message Number** This bit field indicates the collected TCEMSGNR information from an TCE. This value is taken into account only if SISR.ICF = 1 and SISR.TCEV = 1.

The bits in the scheduler instruction status register monitor the information during and after the instruction collection phase of the scheduler. These values will become valid when the next time mark is reached.

SISR
Scheduler Instruction Status Register

($2F8_H$) **Reset Value: $0000\ 0000_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0									BCEV	RMEV	TMEV	ARBV	ICEV	TCEV	RCEV
r									rh	rh	rh	rh	rh	rh	rh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ICF	GM	ARBM		ALTMSG		TREN	CHEN	IENRECF1	IENRECF0	IENTRAF1	IENTRAF0	INP			
rh	rh	rh		rh		rh	rh	rh	rh	rh	rh	rh			

Field	Bits	Type	Description
INP	[3:0]	rh	**Interrupt Node Pointer** This bit field indicates the collected INP information. This value is taken into account only when at least one of the four interrupt requests is enabled.
IENTRAF0	4	rh	**Interrupt Enable if TRAF = 0** This bit field indicates the collected IENTRAF0 information.
IENTRAF1	5	rh	**Interrupt Enable if TRAF = 1** This bit field indicates the collected IENTRAF1 information.
IENRECF0	6	rh	**Interrupt Enable if RECF = 0** This bit field indicates the collected IENRECF0 information.
IENRECF1	7	rh	**Interrupt Enable if RECF = 1** This bit field indicates the collected IENRECF1 information.
CHEN	8	rh	**Check Enable** This bit field indicates the collected CHEN information from an RCE.

Field	Bits	Type	Description
TREN	9	rh	**Transmit Enable** This bit field indicates the collected TREN information from an TCE.
ALTMSG	[11:10]	rh	**Alternative Message** This bit field indicates the collected ALTMSG information from an TCE.
ARBM	[13:12]	rh	**Arbitration Mode** This bit field indicates the collected ARBM information from an TME or an ARBE.
GM	14	rh	**Gap Mode** This bit field indicates the collected GM information from an RME or an BCE (only valid if RME or a BCE has been found).
ICF	15	rh	**Instruction Collection Finished** This bit field indicates that the instruction collection is finished for a time window. It is automatically cleared when a time mark is reached. It is set when the instruction collection is terminated. 0_B The instruction collection is not yet terminated. All other values in registers SISR, STSRL and STSR4 are invalid. 1_B The instruction collection is terminated. All other values in registers SISR, STSRL and STSRH are valid.
RCEV	16	rh	**Receive Control Entry Valid** This bit indicates that a valid receive control information has been found during the instruction collection for this time window. It is automatically cleared when a time mark is reached. 0_B The bit fields CHEN and RCEMSGNR are invalid. They are not taken into account for the next time window. 1_B The bit fields CHEN and RCEMSGNR are valid. They are taken into account for the next time window.

Field	Bits	Type	Description
TCEV	17	rh	**Transmit Control Entry Valid** This bit indicates that valid transmit control information has been found during the instruction collection for this time window. It is automatically cleared when a time mark is reached. 0_B The bit fields TREN, ALTMSG and TCEMSGNR are invalid. They are not taken into account for the next time window. 1_B The bit fields TREN, ALTMSG and TCEMSGNR are valid. They are taken into account for the next time window.
ICEV	18	rh	**Interrupt Control Entry Valid** This bit indicates that a valid interrupt control entry has been found during the instruction collection for this time window. It is automatically cleared when a time mark is reached. 0_B No valid ICE has been found 1_B A valid ICE has been found
ARBV	19	rh	**Arbitration Entry Valid** This bit indicates that a valid arbitration entry has been found during the instruction collection for this time window. It is automatically cleared when a time mark is reached. 0_B No valid ARBE has been found 1_B A valid ARBE has been found
TMEV	20	rh	**Time Mark Entry Valid** This bit indicates that a valid time mark entry has been found during the instruction collection for this time window. It is automatically cleared when a time mark is reached. 0_B No valid TME has been found 1_B A valid TME has been found
RMEV	21	rh	**Reference Mark Entry Valid** This bit indicates that a valid reference mark entry has been found during the instruction collection for this time window. It is automatically cleared when a time mark is reached. 0_B No valid RME has been found 1_B A valid RME has been found

Field	Bits	Type	Description
BCEV	22	rh	**Basic Cycle End Entry Valid** This bit indicates that a valid basic cycle end entry has been found during the instruction collection for this time window. It is automatically cleared when a time mark is reached. 0_B No valid BCE has been found 1_B A valid BCE has been found
0	[31:23]	r	**Reserved** Read as 0; should be written with 0.

Note: This register is reset at the start of a new instruction collection phase.

24.11 MultiCAN Module Implementation

This section describes CAN module interfaces with the clock control, port connections, interrupt control, and address decoding.

24.11.1 Interfaces of the MultiCAN Module

Figure 24-39 shows the TC1798 specific implementation details and interconnections of the MultiCAN module. The four I/O lines of the MultiCAN module (two I/O lines of each CAN node) are connected to I/O lines of Port 3. The MultiCAN module is also supplied by clock control, interrupt control, and address decoding logic. MultiCAN interrupts can be directed to the DMA controller and the GPTA modules. CAN interrupts are able to trigger DMA transfers and GPTA operations.

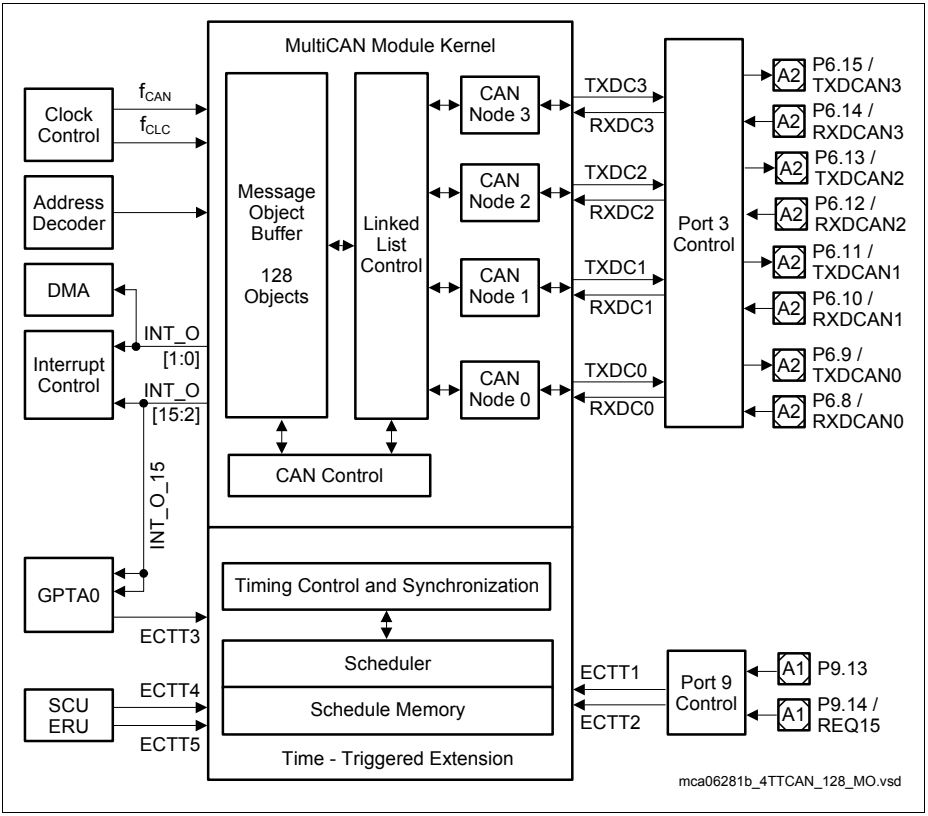


Figure 24-39 CAN with TTCAN Extension, Implementation / Interconnections

24.11.2 MultiCAN Module External Registers

The registers listed in **Figure 24-40** are not included in the MultiCAN module kernel but must be programmed for proper operation of the MultiCAN module.

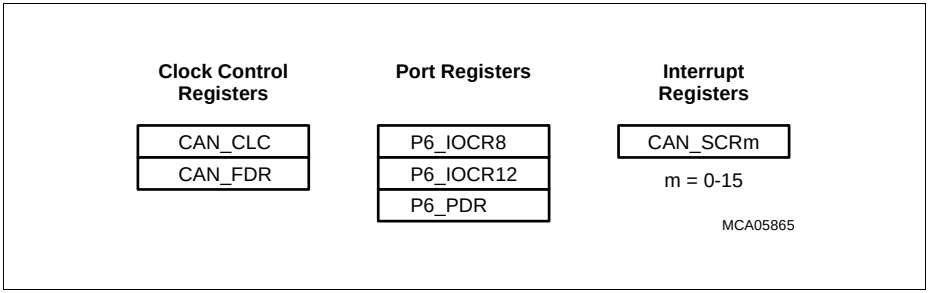


Figure 24-40 CAN Implementation-specific Special Function Registers

24.11.3 Module Clock Generation

As shown in **Figure 24-41**, the clock signals for the MultiCAN module are generated and controlled by a clock control unit. This clock generation unit is responsible for the enable/disable control, the clock frequency adjustment, and the debug clock control. This unit includes two registers:

- CAN_CLC: generation of the module control clock f_{CLC}
- CAN_FDR: frequency control of the module timer clock f_{CAN}

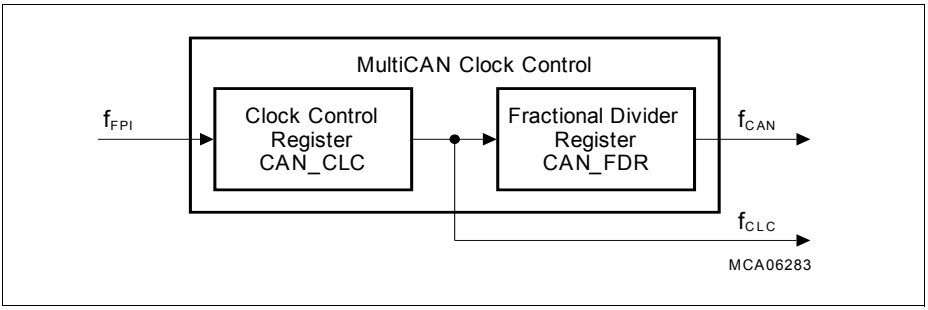


Figure 24-41 MultiCAN Module Clock Generation

The module control clock f_{CLC} is used inside the MultiCAN module for control purposes such as clocking of control logic and register operations. The frequency of f_{CLC} is identical to the system clock frequency f_{FPI}. The clock control register CAN_CLC makes it possible to enable/disable f_{CLC} under certain conditions.

The module timer clock f_{CAN} is used inside the MultiCAN module as input clock for all timing relevant operations (e.g. bit timing). The settings in the CAN_FDR register determine the frequency of the module timer clock f_{CAN} according the following two formulas:

$$f_{CAN} = f_{FPI} \times \frac{1}{n} \quad \text{with n = 1024 - CAN\_FDR.STEP} \qquad (24.1)$$

$$f_{CAN} = f_{FPI} \times \frac{n}{1024} \quad \text{with n = 0-1023} \qquad (24.2)$$

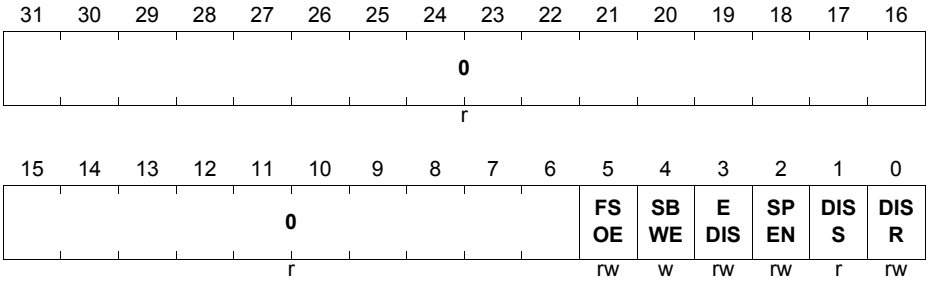
Equation (24.1) applies to normal divider mode (CAN_FDR.DM = 01_B) of the fractional divider. **Equation (24.2)** applies to fractional divider mode (CAN_FDR.DM = 10_B).

Note: The CAN module is disabled after reset. In general, after reset, the module control clock f_{CLC} must be switched on (writing to register CAN_CLC) before the frequency of the module timer clock f_{CAN} is defined (writing to register CAN_FDR).

24.11.3.1 CAN Clock Control Register

The clock control registers makes it possible to control (enable/disable) the module control clock f_{CLC}.

CAN_CLC
CAN Clock Control Register **(000_H)** **Reset Value: 0000 0003$_H$**

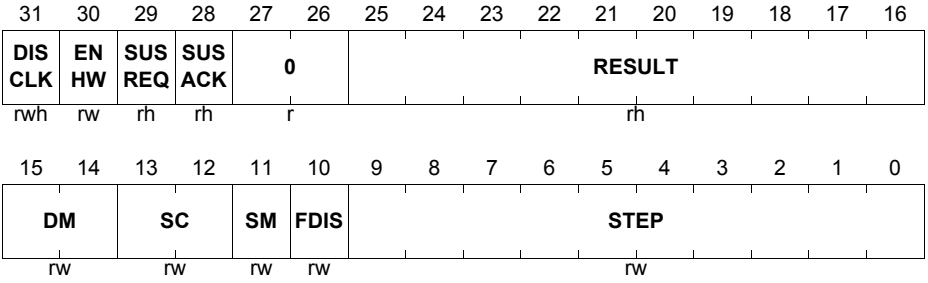


Field	Bits	Type	Description
DISR	0	rw	**Module Disable Request Bit** Used for enable/disable control of the module.
DISS	1	r	**Module Disable Status Bit** Bit indicates the current status of the module.
SPEN	2	rw	**Module Suspend Enable for OCDS** Used to enable the suspend mode.
EDIS	3	rw	**Sleep Mode Enable Control** Used to control module's sleep mode.
SBWE	4	w	**Module Suspend Bit Write Enable for OCDS** Determines whether SPEN and FSOE are write-protected.
FSOE	5	rw	**Fast Switch Off Enable** Used to switch off fast clock in Suspend Mode.
0	[31:6]	r	**Reserved** Read as 0; should be written with 0.

Note: In disabled state, no registers of CAN module can be read or written except the CAN_CLC register.

The fractional divider register allows the programmer to control the clock rate of the module timer clock f_{CAN}.

CAN_FDR
CAN Fractional Divider Register ($00C_H$) Reset Value: $0000\ 0000_H$



Field	Bits	Type	Description
STEP	[9:0]	rw	**Step Value** Reload or addition value for RESULT.
FDIS	10	rw	**Freeze Disable** This bit controls the freeze function for this module. 0_B Module operates on corrected clock, with reduced modulation jitter. 1_B Module operates on uncorrected clock, with full modulation jitter.
SM	11	rw	**Suspend Mode** SM selects between granted or immediate Suspend Mode.
SC	[13:12]	rw	**Suspend Control** This bit field determines the behavior of the fractional divider in Suspend Mode.
DM	[15:14]	rw	**Divider Mode** This bit field selects normal divider mode, fractional divider mode, and off-state.
RESULT	[25:16]	rh	**Result Value** Bit field for the addition result.
SUSACK	28	rh	**Suspend Mode Acknowledge** Indicates state of SPNDACK signal.
SUSREQ	29	rh	**Suspend Mode Request** Indicates state of SPND signal.

Field	Bits	Type	Description
ENHW	30	rw	**Enable Hardware Clock Control** Controls operation of ECEN input and DISCLK bit.
DISCLK	31	rwh	**Disable Clock** Hardware controlled disable for f_{OUT} signal.
0	[27:26]	r	**Reserved** Read as 0; should be written with 0.

24.11.4 Port and I/O Line Control

The interconnections between the MultiCAN module and the port I/O lines are controlled in the port logic. Additionally to the port input selection, the following port control operations must be executed:

- Input/output function selection (IOCR registers)
- Pad driver characteristics selection for the outputs (PDR registers)

24.11.4.1 Input/Output Function Selection in Ports

The port input/output control registers contain the bit fields that select the digital output and input driver characteristics such as pull-up/down devices, port direction (input/output), open-drain, and alternate output selections. The I/O lines for the MultiCAN module are controlled by the port input/output control registers P6_IOCR8 and P6_IOCR12.

Table 24-17 shows how bits and bit fields must be programmed for the required I/O functionality of the CAN I/O lines.

Table 24-17 MultiCAN I/O Control Selection and Setup

Module	Port Lines	Input/Output Control Register Bits	I/O
CAN	P6.8 / RXDCAN0	P6_IOCR8.PC8 = $0XXX_B$	Input
	P6.9 / TXDCAN0	P6_IOCR8.PC9 = $1X01_B$	Output
	P6.10 / RXDCAN1	P6_IOCR8.PC10 = $0XXX_B$	Input
	P6.11 / TXDCAN1	P6_IOCR8.PC11 = $1X01_B$	Output
	P6.12 / RXDCAN2	P6_IOCR12.PC12 = $0XXX_B$	Input
	P6.13 / TXDCAN2	P6_IOCR12.PC13 = $1X01_B$	Output
	P6.14 / RXDCAN3	P6_IOCR12.PC14 = $0XXX_B$	Input
	P6.15 / TXDCAN3	P6_IOCR12.PC15 = $1X01_B$	Output

24.11.4.2 Node Receive Input Selection

Additionally to the I/O control selection, as defined in **Table 24-17**, the selection of a CAN node's receive input line requires that bit field RXSEL in its node port control register NPCRx must be set according to **Table 24-18**. Values for NPCRx.RXSEL other than those of **Table 24-18** result in a recessive receive input for node x.

This feature allows, for example, a CAN node which operates in analyzer mode to monitor the receive operations of its neighbor CAN node. The default setting after reset of a node's NPCRx.RXSEL bit field connect node x with RXDCANx I/O line (x = 0-2).

Table 24-18 Receive Input Selection

Receive Input of	Connected to	Selected by
CAN Node 0	P6.8 / RXDCAN0	NPCR0.RXSEL = 000_B
	P6.10 / RXDCAN1	NPCR0.RXSEL = 001_B
CAN Node 1	P6.10 / RXDCAN1	NPCR1.RXSEL = 000_B
	P6.12 / RXDCAN2	NPCR1.RXSEL = 001_B
CAN Node 2	P6.12 / RXDCAN2	NPCR2.RXSEL = 000_B
	P6.14 / RXDCAN3	NPCR2.RXSEL = 001_B
CAN Node 3	P6.14 / RXDCAN3	NPCR3.RXSEL = 000_B
	P6.8 / RXDCAN0	NPCR3.RXSEL = 001_B

24.11.4.3 External CAN Time Trigger Inputs

The external CAN time trigger inputs ECTT[7:1] can be used as a transmit trigger for a reference message. In the TC1798, these input lines are connected as shown in **Table 24-19**.

Table 24-19 External CAN Time Trigger Inputs

Receive Input	Connected to	From Module
ECTT1	P9.13	Port 9
ECTT2	P9.14 / REQ15 Input	Port 9 / External Request Unit (SCU)
ECTT3	Output OUT5	GPTA0
ECTT4	Output IOUT2	External Request Unit (SCU)
ECTT5	Output IOUT3	External Request Unit (SCU)
ECTT6	-	-
ECTT7	-	-

24.11.4.4 DMA Request Outputs

The interrupt output lines INT_O0 to INT_O1 of the MultiCAN module can be used as a DMA requestor and are able to trigger DMA transfers. INT_O[1:0] are connected to the DMA controller as shown in **Table 24-20**.

Table 24-20 CAN-to-DMA Request Connections

DMA Channel	Connected to CAN Interrupt Output	Selected in DMA Controller by programming
06	INT_O0	CHCR06.PRSEL = 011_B
07	INT_O1	CHCR07.PRSEL = 010_B

24.11.4.5 Connectons to GPTA0 Inputs

The interrupt output line INT_O15 is connected to the GPTA module, see **Table 24-21**.

Table 24-21 CAN-to-GPTA0 Request Connections

GPTA Input	Connected to CAN Interrupt Output
INT0	INT_O15

24.11.5 Interrupt Control

The interrupt control logic in the MultiCAN module uses an interrupt compressing scheme that allows high flexibility in interrupt processing. There are 140 hardware interrupt sources and one software interrupt source available:

- CAN node interrupts:
  - Four different interrupt sources for each of the three CAN nodes = 12 interrupt sources
- Message object interrupts:
  - Two interrupt source for each message object = 128 interrupt sources
- One software initiated interrupt (register MITR)

Each of the 140 hardware initiated interrupt sources is controlled by a 4-bit interrupt pointer that directs the interrupt source to one of the sixteen interrupt outputs INT_Om (m = 0-15). This makes it possible to connect more than one interrupt source (between one and all) to one interrupt output line. The interrupt wiring matrix shown in **Figure 24-42** is built up according to the following rules:

- Each output of the 4-bit interrupt pointer demultiplexer is connected to exactly one OR-gate input of the INT_Om line. The number “m” of the corresponding selected INT_Om interrupt output line is defined by the interrupt pointer value.
- Each INT_Om output line has an input OR gate which is connected to all interrupt pointer demultiplexer outputs which are selected by an identical 4-bit pointer value.

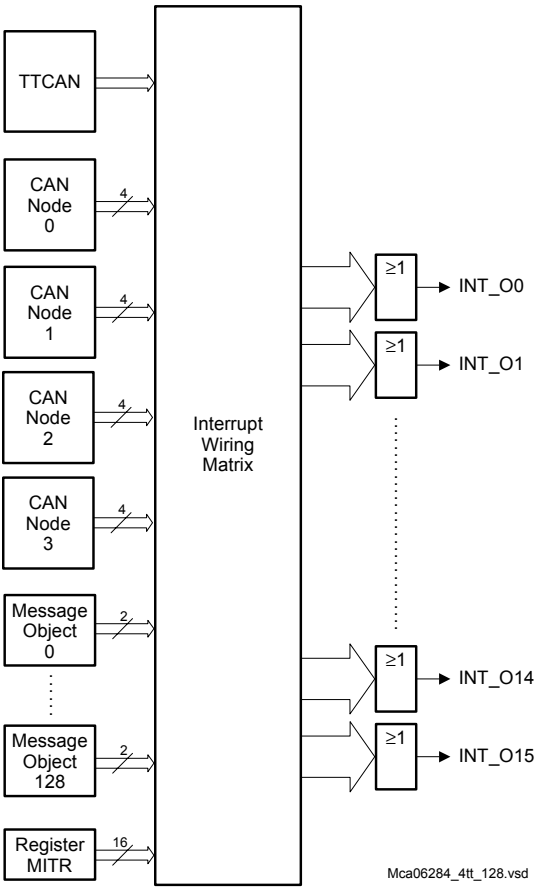
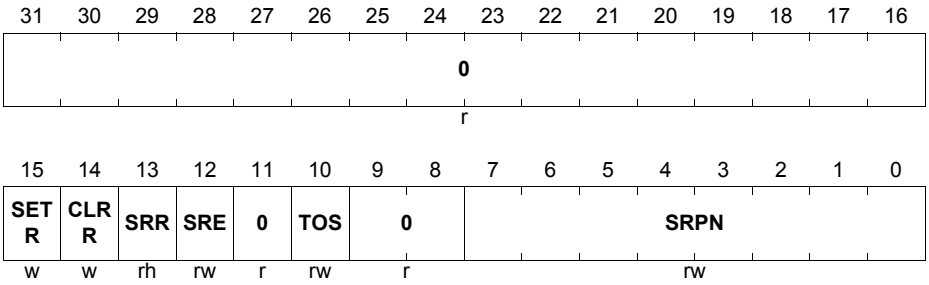


Figure 24-42 Interrupt Compressor

24.11.5.1 CAN Service Request Control Register

Each of the sixteen interrupt outputs INT_Om of the MultiCAN module is controlled by its service request control registers.

CAN_SRCm (m = 0-15)
CAN Service Request Control Register m
($0FC_H$-m*4_H) **Reset Value: $0000\ 0000_H$**



Field	Bits	Type	Description
SRPN	[7:0]	rw	**Service Request Priority Number**
TOS	10	rw	**Type of Service Control**
SRE	12	rw	**Service Request Enable**
SRR	13	rh	**Service Request Flag**
CLRR	14	w	**Request Clear Bit**
SETR	15	w	**Request Set Bit**
0	[9:8], 11, [31:16]	r	**Reserved** Read as 0; should be written with 0.

Note: Additional details on service request nodes and the service request control registers are described in section "Service Request Nodes" of the TC1798 System Units part.

Some of the sixteen interrupt outputs of the MultiCAN module can be used to trigger operations in the DMA controller.

24.11.6 MultiCAN Module Register Address Map

In addition to the MultiCAN register address map from **Page 24-63**, the complete MultiCAN module register address map of **Figure 24-43** also shows the general implementation-specific registers for clock control, module identification, and interrupt service request control and adds the absolute address information. The address map of TTCAN registers only is shown in **Figure 24-38**.

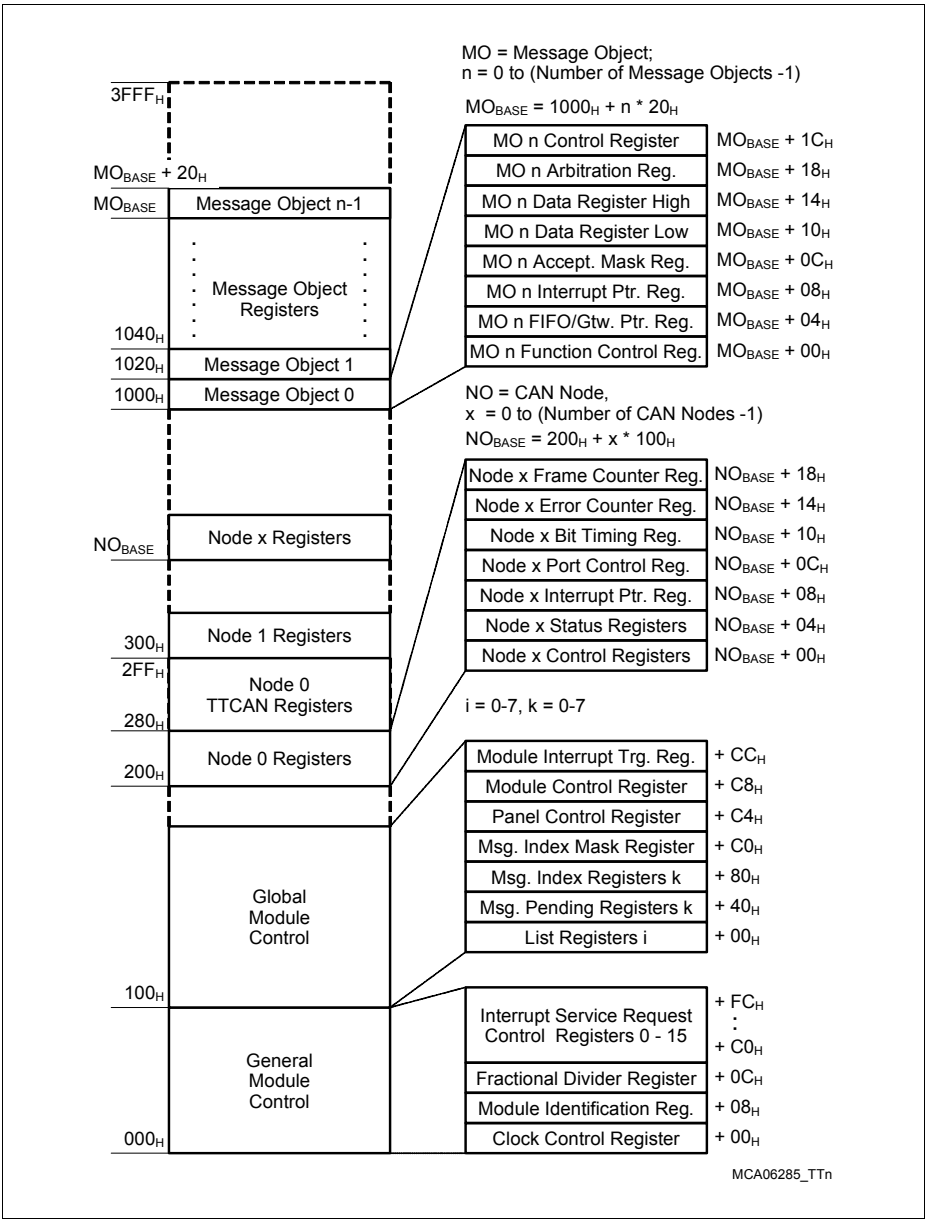


Figure 24-43 MultiCAN Module Register Map

25 Single Edge Nibble Transmission (SENT)

This chapter describes the SENT Interface of the TC1798. It contains the following sections:

- Functional description of the SENT kernel (see **"Overview" on Page 25-2**)
- SENT kernel register descriptions (see **"SENT Kernel Registers" on Page 25-22**)
- TC1798 implementation-specific details and registers of the SENT module (port connections and control, interrupt control, address decoding, and clock control, see **"SENT Module Implementation" on Page 25-64**

25.1 SENT Kernel Description

Figure 25-1 shows a global view of the SENT interface.

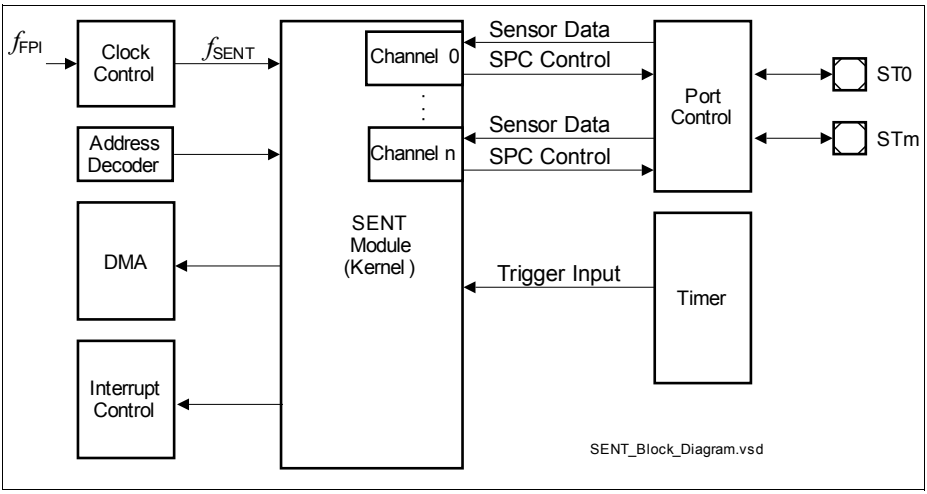


Figure 25-1 General Block Diagram of the SENT Interface

The SENT module communicates with the external world via one I/O line for each channel. The STx lines are the receive data input signals. They can overlay ADC inputs. If the optional SPC mode is used, they can be used on a port configured with an open drain transistor. This way the optional SPC data can be transmitted and the line is used bidirectionally. In case of an external transceiver, receive and transmit path can be routed to two different ports.

25.1.1 Overview

The SENT interface provides a serial communication link typically used to connect sensors or other peripheral devices.

Clock control, address decoding, and service request control are managed by the SENT module kernel.

The SENT IP-module performs communication according to the SENT specification J2716 FEB2008 Rev. 3 2009-06-24.

While staying compliant to this standard, it is able to cover as well the Short PWM Code (SPC) protocol extensions. This enhances the standardized SENT protocol defined by J2716 FEB2008 Rev. 3 2009-06-24. SPC enables the use of enhanced protocol functionality like “synchronous”, “range selection” and “ID selection” protocol mode.

Receive data on a SENT channel can be set up according to the underlying application. In particular the number of nibbles forming one value is configurable.

The message storage consists of two 32-bit registers for each channel, representing a flexible double buffer system.

In SPC mode, maintaining the sample and transmission schedule as well as providing message status information is support.

The register set of the SENT module can be accessed directly by the CPU for configuration, data read out and status query.

The SENT IP-module supports the following features:

Features

- Conformance with SENT protocol specification J2716 FEB2008 Rev. 3 2009-06-24
- Data rates of up to 65,8 kbit/s at 3 µs tick length and 6 data nibbles on each channel
- Support of standard tick times (3 µs through 90 µs) and
- Message tick time programmable between 1 µs and 90 µs
- 8 SENT channels working independently in parallel
- Status nibble optionally included in the checksum (default not included)
- Sticky interrupt flags, error interrupt optional (default disabled)
- Configurable frame length (default is 24 bit), max data size is 32 bits
- Serial data processing optional (default: disabled)
- Option for bigger frame lengths (must still be fix for each application)
- transparent mode (nibble CRCs are written to the receive control register for SW processing)
- Support of SPC
- Support of trailing Pause Nibble of any length (even longer than 70 ticks)
- Indication of system status: STOP, INITIALIZED, RUNNING, SYNCHRONIZED
- The receiver module will monitor the message for the following error conditions:
  - Calibration pulse length deviates more than +/-25% from the nominal 56 ticks
  - Too many or too few nibbles between calibration pulses.
  - Checksum error.
  - Successive calibration pulse differ by more than 1.5625%
  - Any nibble data values measured as < 0 or >15.
- When any of those errors is detected, the receiver module shall declare that a message error has occurred and ignore the entire message.
- Any of those errors shall cause the receiver to begin searching for a valid calibration pulse to re synchronize.
- Option to enable/disable the check of the next calibration pulse before validation of received data
- Digital Glitch filter suppressing noise
- Buffer overrun detection
- Optional output inversion for use of external open drain transistor
- Optional input inversion for use of external open transistor for level shifting
- Interrupt on status nibble violation
- Programmable Nibble sorting to support LSN or HSN first and relief CPU

25.1.2 General Operation

The Single Edge Nibble Transmission encoding scheme (SENT) is intended for use in applications where high resolution sensor data needs to be communicated from a sensor to an Engine Control Unit (ECU). It is intended as a replacement for the lower resolution methods of 10 bit A/D converters and PWM and as a simpler low cost alternative to CAN or LIN. The implementation assumes that the sensor is a smart sensor containing a microprocessor or dedicated logic device (ASIC) to create the signal.

Figure 25-3 shows a typical TC1798 application in which a SENT interface reads a sensor device.

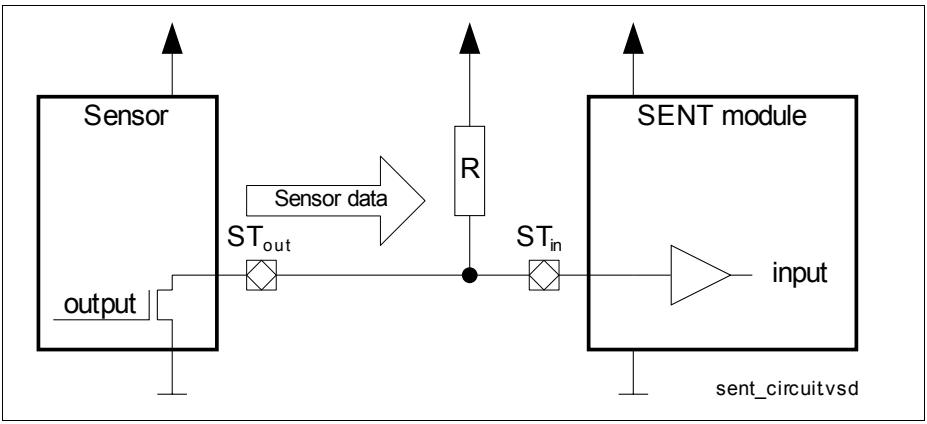


Figure 25-2 SENT to External Device Connection

SENT communication is unidirectional from sensor to controller without any synchronization. The sensor signal is transmitted as a series of PWM blocks measured as falling to falling edge times.

The Short PWM Code (SPC) extension overcomes the drawback of unidirectionality as said above while keeping conformance to the standard.

Figure 25-3 shows a typical TC1798 application in which an SPC enabled SENT ECU reads an SPC enabled SENT sensor device.

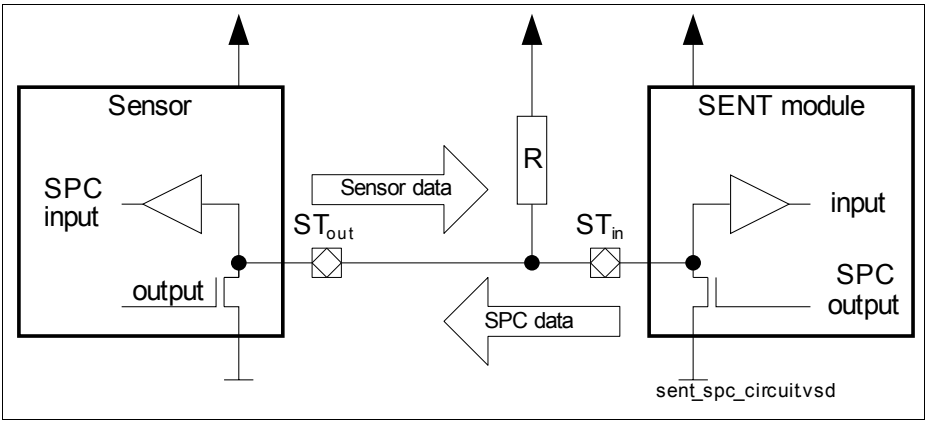


Figure 25-3 SENT SPC to External Device Connection

Some applications are:

- Read out of the external throttle position sensor (e.g. SENT enabled linear hall sensor)
- Receiving pedal position
- Synchronize sampling and read out of up to four sensors on one single line (SPC)
- Selection of 1 out of 4 sensors connected to a single SENT channel.
- Serial connections of the TC1798 to other peripheral devices

25.1.2.1 Definitions

SENT: Single Edge Nibble Transmission

Nibble: Four Bit value between 0 and 15 = half a Byte = one character in hex (0 to F)

SPC: Short PWM Code

PWM: Pulse Width Modulation

ASIC: Application Specific Integrated Circuit

CAN: Controller Area Network

LIN: Local Interconnect Network

ISO: International Organization for Standardization

ECU: Electronic Control Unit

FSM: Finite State Machine

25.1.3 Standard SENT Operation

Standard SENT Mode supports communication fully compliant to J2716 FEB2008 Rev. 3 2009-06-24, in which only the external device is sending and the ECU is receiving. In this unidirectional communication, both transmitter and receiver use the same data frame format and have the same baud rate. These settings are defined at system integration time and do not change for a given application. Data is received on pin ST. **Figure 25-4** shows the block diagram of the SENT Module when operating in Standard SENT Mode.

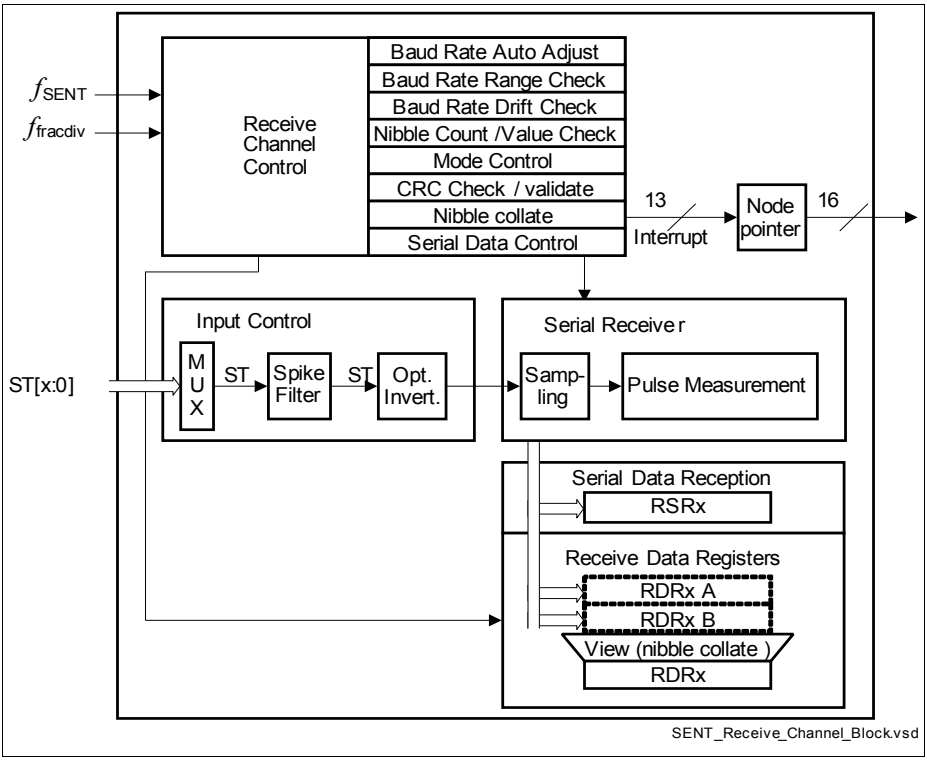


Figure 25-4 Standard SENT Mode Operation

25.1.3.1 Frame Formats and Definitions

This section describes the frame formats and definitions of the SENT protocol.

Basic Definitions

Figure 25-5 shows the layout and definitions of a standard SENT frame. Note that the SENT standard does not specify whether the most significant nibble or the least significant nibble is sent out first.

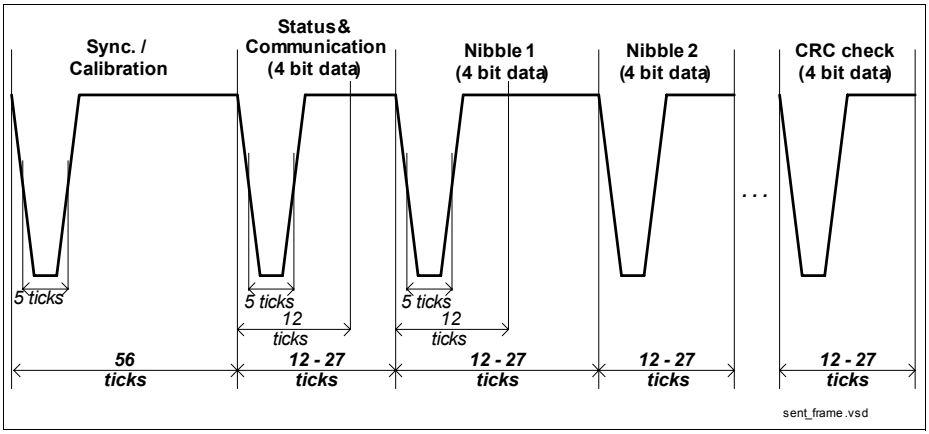


Figure 25-5 Standard Encoding Frame

Standard Serial Data Encoding

The serial data is transmitted bit wise per frame in bit 2 of the Status and Communication nibbles of consecutive messages from the transmitter.

Bit Number	Bit Function
0	Reserved for specific application
1	Reserved for specific application
2	Serial Data message bits
3	Message start = 1, otherwise = 0

Figure 25-6 Standard Serial Data Encoding

Standard Serial Data Frame

Serial data is communicated in a 16-bit sequence as shown in **Figure 25-7**. The staring bit of a serial message is indicated by a 1 in bit 3 o the Status and Communication nibble. That SENT message and the next 15 must be successfully transmitted (no errors) for the serial value to be received. The CRC generation is identical with the CRC generation on the data nibbles.

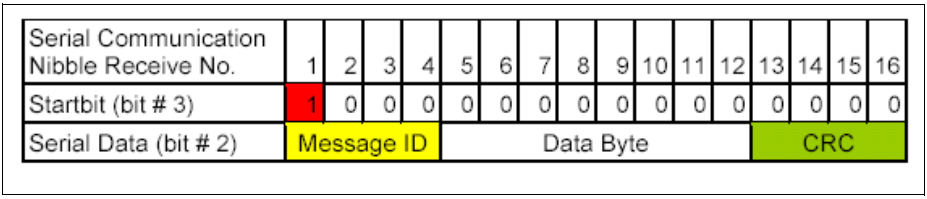


Figure 25-7 Serial Data Frame

CRC Calculation

The Signal data and the Serial data is secured with a 4 bit CRC. The standard CRC calculation method is well defined in the J2716 FEB2008 Rev. 3 2009-06-24.

Note: RCR.CRZ defines, if a zero nibble is added for calculation or not.

The alternative checksum nibble is a 4-bit CRC of the data nibbles (including the status nibble if RCR.SNI is set, as used in sensor TLE4998). The CRC is calculated using a polynomial x^4 +x^3 + x^2 + 1 with a seed value of 0101.

In order to facilitate CRC implementations and to avoid ambiguities, an example implementation of the alternative 4-bit CRC is given below. This is used e.g. in the sensor TLE4998 for the signal data. See **Figure 25-8** for details.

```
// Fast way for any µC with low memory and compute capabilities
// contains input data (status nibble, 6 data nibble, CRC)
char Data[8] = {…};
// required variables and LUT
char CheckSum, i;
char CrcLookup[16] = {0, 13, 7, 10, 14, 3, 9, 4, 1, 12, 6, 11, 15,
2, 8, 5};
CheckSum= 5; // initialize checksum with seed “0101”
for (i=0; i<7; i++) {
     CheckSum = CheckSum ^ Data[i];
     CheckSum = CrcLookup[CheckSum];
};
// finally check if Data[7] is equal to CheckSum
```

Note: For the “Extended Serial Message Frame Format”, an own 6-bit CRC calculation method is defined by the standard.

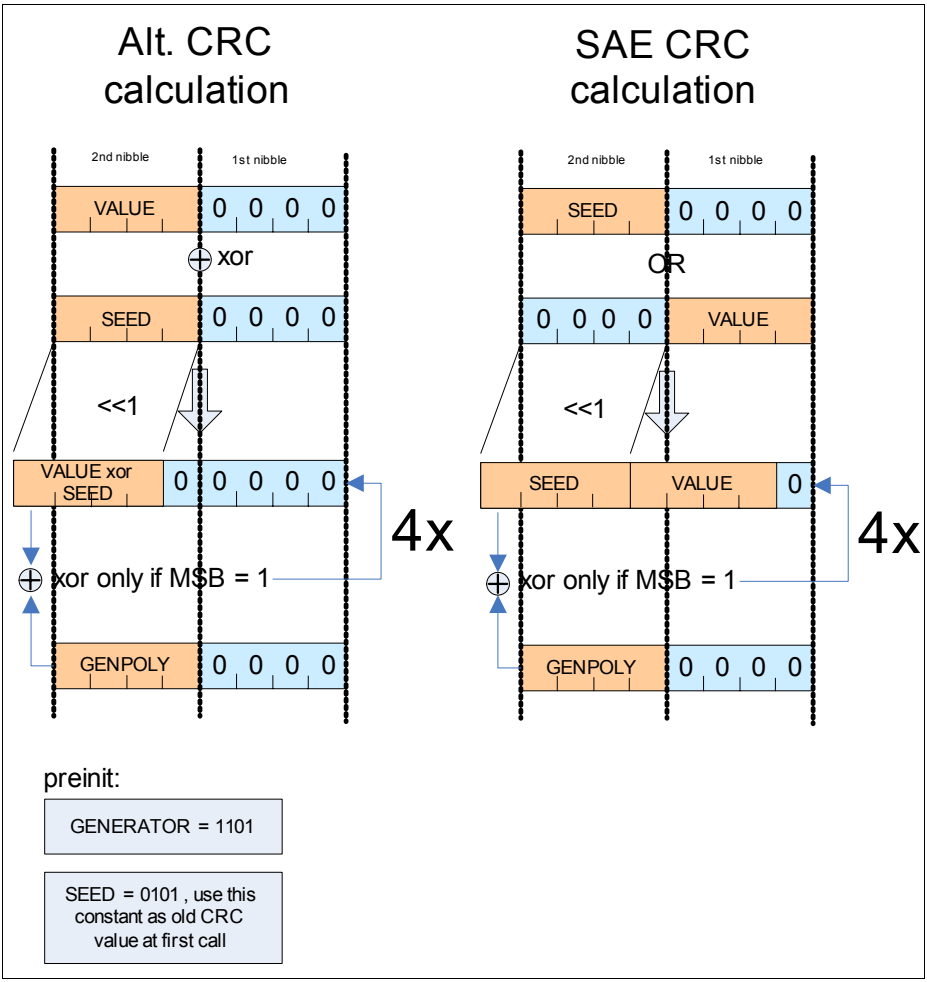


Figure 25-8 Alternate vs. SAE CRC Calculation

Extended Serial Data Encoding

The serial data is transmitted bit wise per frame in bits [3:2] of the Status and Communication nibbles of 18 consecutive messages from the transmitter.

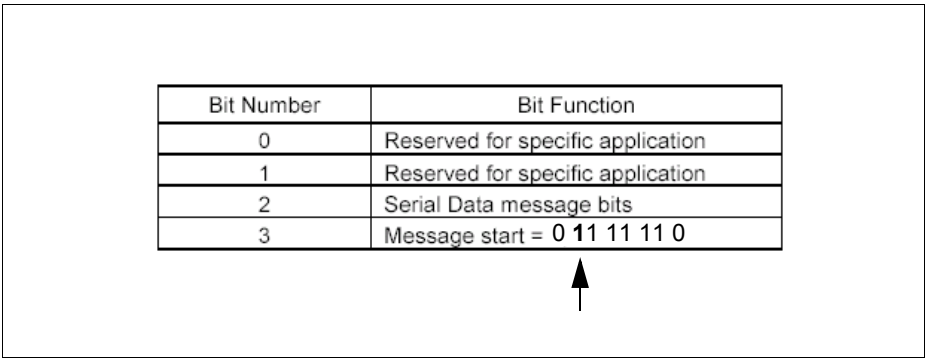


Figure 25-9 Extended Serial Data Encoding

Extended Serial Data Frame

Serial data is communicated in a 18-bit sequence as shown in **Figure 25-10**. The frame start of a serial message is indicated by the unique pattern “01111110” in bit #3 of the status and communication nibble. The first “1” in a series of six ones (after a “0”) indicates the first nibble of a serial message frame. Serial data bit #3 of serial communication nibbles 1 - 6 are set to “1”. Serial data bit #3 of serial communication nibbles 7, 13 and 18 are set to “0”. 18 consecutive SENT messages must be successfully transmitted (no errors) for the serial value to be received. The CRC generation is different from the CRC generation on the data nibbles. (See SENT Standard)

The serial message frame contains 21 bits of message data and a 6-bit frame-check sequence. Two different configurations can be chosen:

- 12-bit data and 8-bit message ID
- 16-bit data and 4-bit message ID

A configuration bit (serial data bit #3, serial communication nibble No. 8) determines the configuration of the enhanced serial message frame. It determines how the SENT module automatically interprets the serial data.

- Configuration bit = 0: 12-bit data and 8-bit message ID
- Configuration bit = 1: 16-bit data and 4-bit message ID

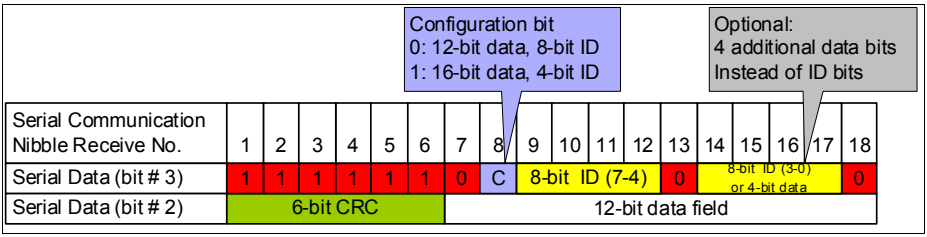


Figure 25-10 Extended Serial Data Frame

Figure 25-11 shows in detail the frame structure for Extended Serial Data Frames with Configuration Bit = 0.

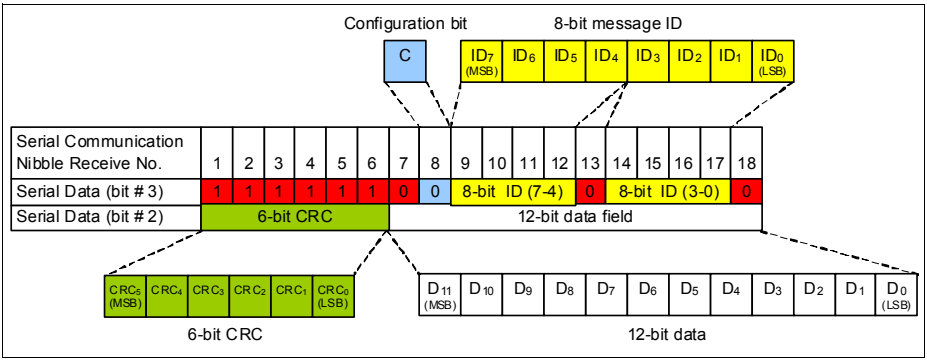


Figure 25-11 Configuration Bit = 0

Figure 25-12 shows in detail the frame structure for Extended Serial Data Frames with Configuration Bit = 1.

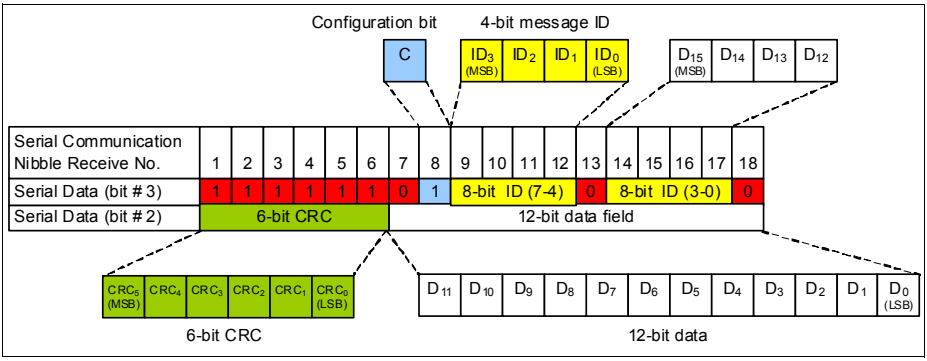


Figure 25-12 Configuration Bit = 1

25.1.4 SPC Operation

The module supports a SPC (Short PWM Code) protocol, which enhances the standardized SENT protocol (Single Edge Nibble Transmission) defined by J2716 FEB2008 Rev. 3 2009-06-24. SPC enables the use of enhanced protocol functionality due to the ability to select between “synchronous”, “range selection” and “ID selection” protocol mode or even “bidirectional transmit mode”.

25.1.4.1 Synchronous Transmission

In the “synchronous” mode, the sensor (slave) starts to transfer a complete data frame only after a low pulse is forced by the master on the OUT pin. This means that the data line is bidirectional - an open drain output of the micro controller (master) sends the trigger pulse. The sensor then initiates a sync pulse and starts to calculate the new output data value. After the synchronization period, the data follows in form of a standard SENT frame, starting with the status, data and CRC nibbles. At the end, an end pulse allows the CRC nibble decoding and indicates that the data line is idle again. The timing diagram in **Figure 25-13** visualizes a synchronous transmission

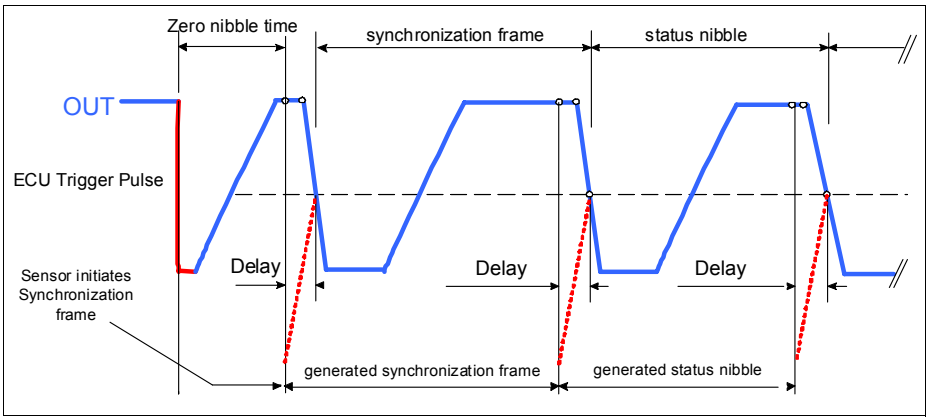


Figure 25-13 Synchronous Transmission (SPC)

25.1.4.2 Range Selection

The low time duration of the master can be used to select the range of the sensor in SPC dynamic range selection mode.

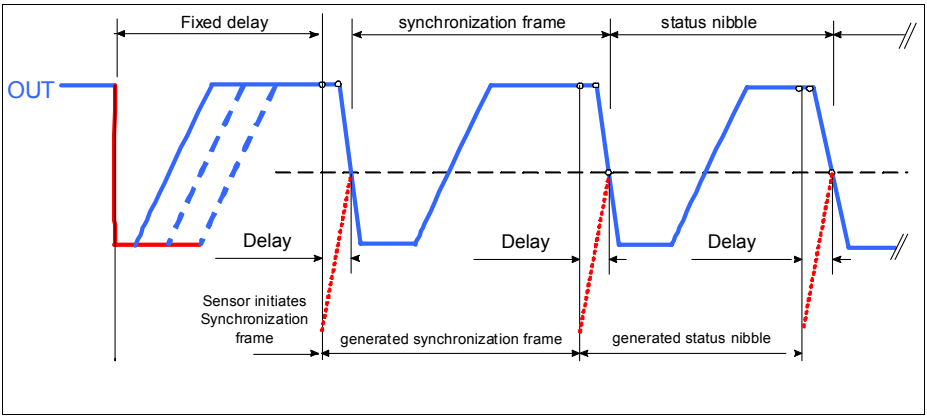


Figure 25-14 Range (SPC)

25.1.4.3 ID Selection

This functionality is similar to the previous mode, but instead of switching the range of one sensor, one of up to four sensors are selectable on a bus (bus mode, 1 master with up to 4 slaves). This allows parallel connection of up to 4 sensors using only three lines (VDD, GND, OUT), as illustrated in **Figure 25-15**.

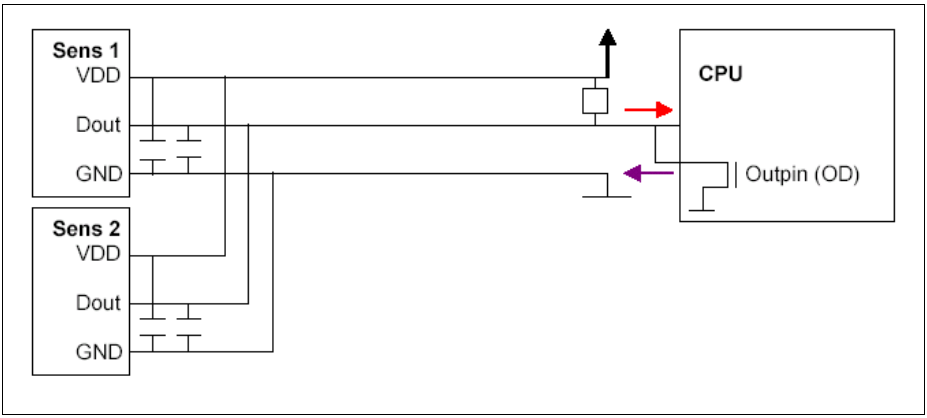


Figure 25-15 ID Selection (SPC)

25.1.4.4 Bidirectional Transmit Mode

After addressing the sensor the ECU interrupts the sensor sync pulse by pulling down the line. The ECU starts to transmit own nibbles on the time base of the selected sensor. The ECU has to adapt the sensors timing from an earlier received cycle.

The sensor detects the falling edge that infringes the protocol and switches to receive mode as illustrated in **Figure 25-16**.

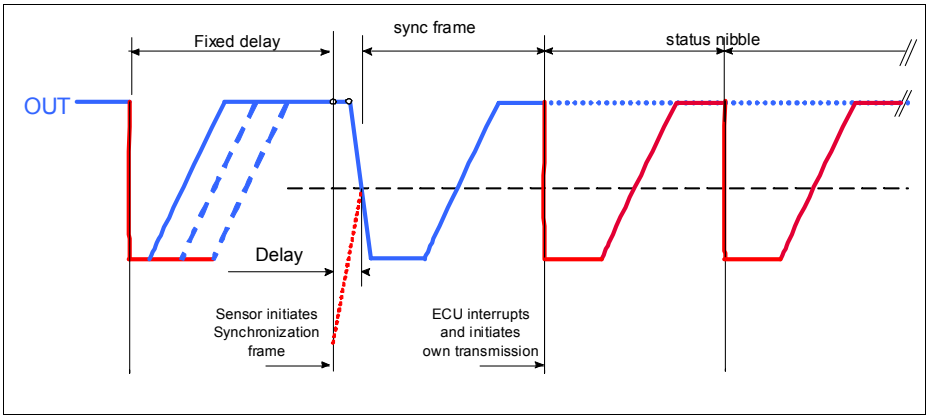


Figure 25-16 Bidirectional Transmit Mode (SPC)

25.1.4.5 SPC Timing

An SPC transmission is initiated by a Master pulse on the OUT pin. To detect a low level on the OUT pin, the voltage must be below a threshold Vthf. The sensor detects that the OUT line has been released as soon as Vthr is crossed. **Figure 25-17** shows the timing definitions for the master pulse. The master low time tmlow as well as the total trigger time tmtr are individual for the different SPC modes and are given in the sensors specifications.It is recommended to chose the typical master low time exactly between the minimum and the maximum possible time given by the connected sensor: tmlow,typ = (tmlow,min + tmlow,max) / 2.

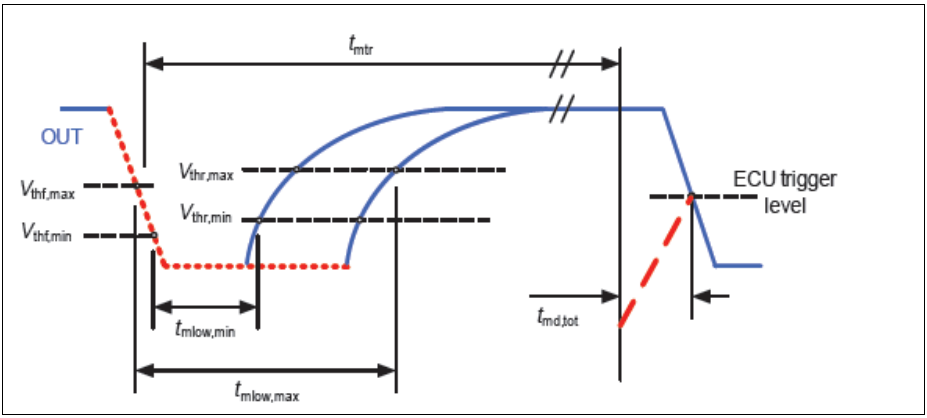


Figure 25-17 Timing (SPC)

25.1.4.6 Abort of Frames

Only a reset condition of the device or choosing Mode 0 by clearing bit field SCRx.TRIG can abort a current transmission. The SENT module does not start a new frame transmission when the channel becomes disabled, the suspend mode is requested, or the sleep mode is entered. If one of these three conditions becomes active during a running frame transmission, the frame transmission is completely finished before the requested abort state is entered. Note that in this case no frame finished interrupt is generated any more.

Note: Received frames are aborted immediately on a disable, suspend or sleep request.

25.1.5 Baud Rate Generation

The nominal baud rate of each channel is individually adjustable. This is required as it is depending from the connected sensor and its current deviation from nominal frequency.

The actual baud rate of the channel follows automatically the baud rate of the connected device and its current deviation from nominal frequency. The adaptation range is +- 25% as specified in J2716 FEB2008 Rev. 3 2009-06-24.

Chapter 25.1.5 shows in detail how the baud rate for each channel is adjusted. 1 / f_{tick_x} defines the resulting tick length.

In the first stage, a global fractional divider serves as pre divider. Its intermediate frequency $f_{fracdiv}$ can be set up so that it is handy as input frequency for the different SENT channels. The clock signal f_{pdiv} of a channel must always be at least 20 times the nominal tick frequency of the channel. This is to allow for the highly flexible and big tolerance of +-25% versus the sending device. In addition the module must be able to detect a deviation in the length of 2 consecutive Synchronization / Calibration pulses of 1.5625% (1/64) and adapt the own baud rate. The tick time is typically 3 µs but can vary by standard and take values up to 10 µs. Future application might require even shorter tick times for higher repetition rates. This is why this implementation allows for an even extended range of 1 … 90 µs. To achieve this each channel has its own fractional divider. This allows to downscale the frequency of f_{tick} precisely to the required tick frequency. For details on the principles of a fractional divider, please refer to the SCU chapter of TC1798 section “Clock Control”.

The SENT module provides two clock signals to the channels (**Figure 25-18**):

- f_{SENT}
  This is the module clock that is used inside the SENT kernel for control purposes such as clocking of control logic and register operations. The frequency of f_{SENT} is always identical to the system clock frequency f_{FPI}. The clock control register SENT_CLC makes it possible to enable/disable f_{SENT} under certain conditions.
- $f_{fracdiv}$
  This clock is the module clock that is used inside the SENT kernel for baud rate generation of the serial channels. The fractional divider register SENT_FDR controls the frequency of $f_{fracdiv}$. Usually not required and set to 1.

The channels generate two local clock signals:

- f_{pdiv_x}
  This clock is the channel clock that is used inside the SENT channel x for baud rate generation of the serial channel. The divider register SENT_CPDRx controls the frequency of f_{pdiv_x}.
- f_{tick_x}
  This clock is the channel clock that is used inside the SENT channel as the baud rate frequency. The fractional divider register SENT_CFDRx controls the frequency of

f_{tick_x}.The higher the value of DIV the higher the precision with which the Synchronization / Calibration pulse and the deviation in the length of 2 consecutive Synchronization / Calibration pulses (drift) can be measured.
DIV must be set in an interval of [560, 3276].

•

Each time a Synchronization / Calibration pulse starts DIVM is measured. DIVM is the result of measuring the calibration pulse duration with f_{pdiv_x}. At the end of the Synchronization / Calibration pulse this value is taken as new divider of the CFDR.

Each time a pulse starts, the internal accumulator of the CFDR is preset with DIVM / 2. This is required to center the data eye and to make the margin symmetrical.

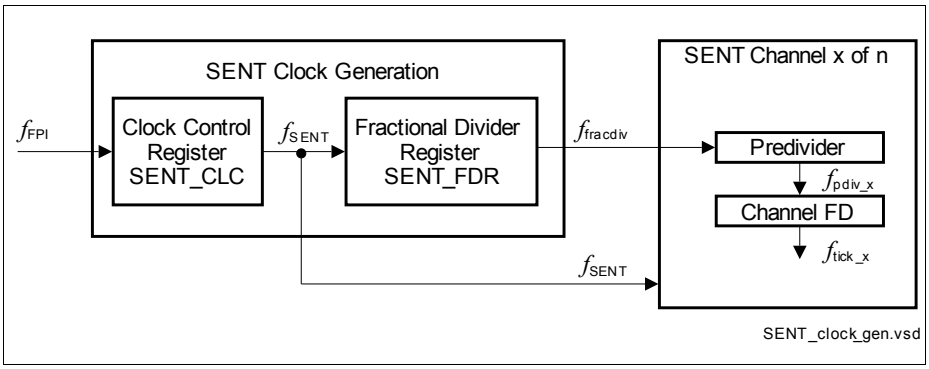


Figure 25-18 SENT Module Clock Generation

The following two formulas define the frequency of $f_{fracdiv}$:

$f_{fracdiv} = f_{SENT}$ / (1024 - SENT_FDR.STEP); FDR.DM = 01_B (25.1)

$f_{fracdiv} = f_{SENT}$ x SENT_FDR.STEP / 1024 with STEP = 0 … 1023; FDR.DM = 10_B (25.2)

The following formula defines the frequency of f_{pdiv_x}:

$f_{pdiv\_x} = f_{fracdiv}$ / (SENT_CPDRx.PDIV + 1) (25.3)

The following formula defines the nominal frequency of f_{tick_x}. For the actual frequency of f_{tick_x} DIV is replaced by DIVM after the current sensor frequency was validly measured.

$f_{tick\_x} = f_{pdiv\_x}$ x 56 / SENT_CFDRx.DIV with DIV = 560 … 3276 (25.4)

25.1.6 Error Detection Capabilities

Each SENT channel can detect and signal the following error conditions:

Protocol Level:

- Calibration pulse length deviates more than +/-25% from the nominal 56 ticks
- Too many or too few nibbles between calibration pulses
- Checksum error
- Successive calibration pulse differ by more than 1.5625%
- Any nibble data values measured as < 0 or >15
- Wrong Status and Communication nibbles
- Serial Communication CRC error

Transfer Management Level:

- Receive Data Buffer Overrun
- SPC Data Buffer Underrun

25.1.7 Digital Glitch Filter

Very slow slopes and signal noise can lead to fast transitions of the input signal. These unwanted transitions are suppressed by a digital glitch filter similar to a Filter and Prescaler Cell (FPC) of Infineons GPTA® in Delayed Debounce Filter Mode with up and down (no reset).

It is built for filtering very fast transitions only. The filter calculates the integral of the signal. If the integral reaches a programmable saturation point, the signal change is notified to the pulse measurement unit. Thus it helps to find the exact pulse length for said slow slopes in noisy environment.

The glitch filter is clocked with f_{pdiv}. If the state of the input sample differs from the current output signal value, the internal counter is incremented by one. When the state of the input sample matches the current output signal value and the timer is not in idle, the timer is decremented by one. When the timer matches the compare value stored in IOCRx.DEPTH, the level of the output signal line is inverted. The timer will be reset and set to idle state again.

The depth of the filter can be programmed to a value between 1 and 15. Typically a depth of 3 to 5 T_{pdiv} is sufficient. By default it is cleared. If IOCRx.DEPTH is cleared the filter is inactive. Nevertheless, the input signal is sampled with f_{pdiv}.

The internal signal after the filter will change value not before the new value was sampled DEPTH times. If during this period a spike occurs, it takes 2 x T_{pdiv} times longer for the internal signal to change value. The filters principal implies a delay of the signal by (DEPTH x T_{pdiv}).

Upon detection of glitch during rising or falling edge, IOCRx.REG or IOCRx.FEG is set. The rising / falling edge glitch flags must be reset by software.

Figure 25-19 shows the digital glitch filter:

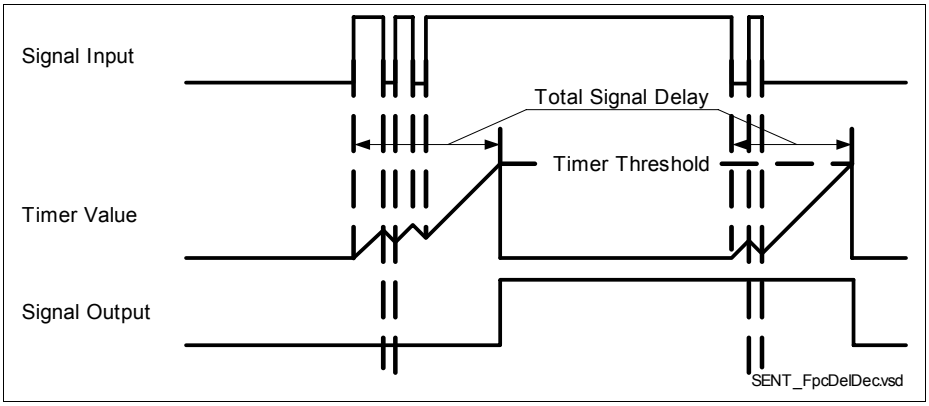


Figure 25-19 Digital Glitch Filter

25.1.8 Interrupts

4 Interrupt sources are available for the SENT module. Four interrupt sources for any 8 channels are provided by the SENT Module.

RDI indicates a receive data interrupt. It is activated when a received frame is moved to a Receive Data Register RDR. RSI indicates a receive frame success interrupt, i.e. the CRC was successful. Both RDI and RSI will be issued together in normal use cases where the frame size is not bigger than 8 nibbles and CRC is correct. RBI indicates a receive buffer overrun interrupt. It is activated when a new frame is transferred to a Receive Data Register RDR while the old value was still not read by the host (“overwrite”), i.e. the kernel wants to set any of the two interrupts RSI and RDI and finds any of these two interrupts already set. TDI indicates a transmit interrupt. It is activated when data is moved from a SCR to a transmit shift register. TBI indicates a transfer buffer under run interrupt. It is set after data has been completely transferred (PLEN exceeded) and no new data was written to SCRx. In addition the protocol error interrupts are available: FRI, FDI, NNI, NVI, CRCI. If one of the protocol interrupts is activated, data is to be treated as invalid according to J2716 FEB2008 Rev. 3 2009-06-24. WSI, SDI SCRI treat the interrupts referring to the Status and Communication nibble.

For acceleration of the interrupt service routine, a Register INTOV for any 32 channels is implemented that holds a flag for each channel. This flag is automatically set if there is an interrupt pending for the channel which is enabled. It is automatically reset, if no more enabled interrupt is pending for this channel.

The interrupt structure is shown in **Figure 25-20**. The interrupt request or the corresponding interrupt set bit (in register INTSET) can trigger the interrupt generation at the selected interrupt node. The service request pulse is generated independently from the interrupt flag in register INTSTATx. The interrupt flag can be cleared by software by writing to the corresponding bit in register INTCLR.
If more than one interrupt source is connected to the same interrupt node pointer (in register INPx), the requests are combined to one common line.

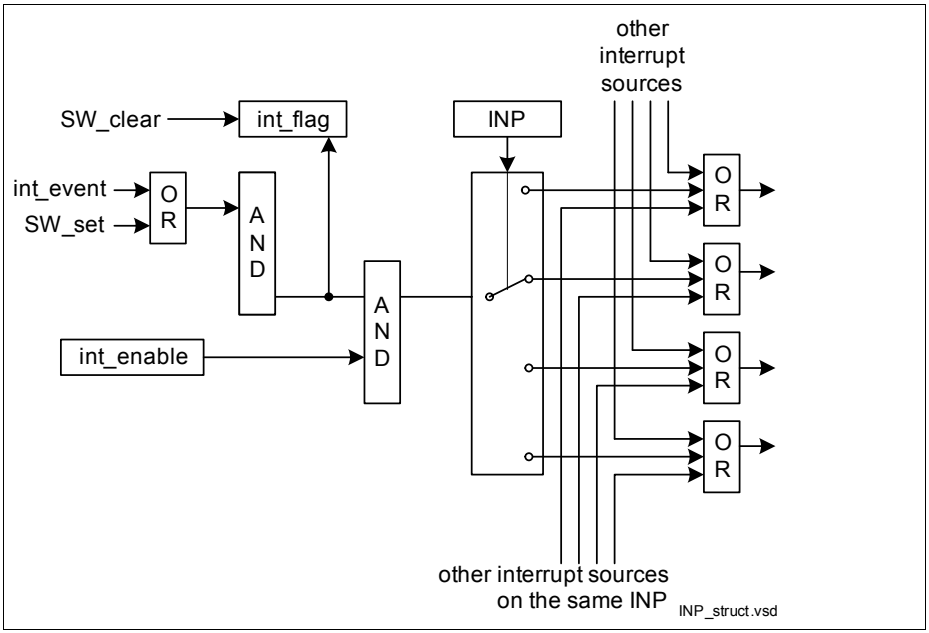


Figure 25-20 Interrupt Generation

25.1.9 Trigger Outputs

Any interrupt source can be used as trigger output TRIGO outside the module. Each TRIGO is connected to a DMA input. See **Table 25-3 "Service Request Lines of SENT" on Page 25-65**.

25.2 SENT Kernel Registers

This section describes the kernel registers of the SENT module. All SENT kernel register names described in this section will be referenced in other parts of the TC1798 User´s Manual by the module name prefix “SENT_” for the SENT interface.

All registers in the SENT address spaces are reset with the application reset (definition see SCU section “Reset Operation”).

SENT Kernel Register Overview

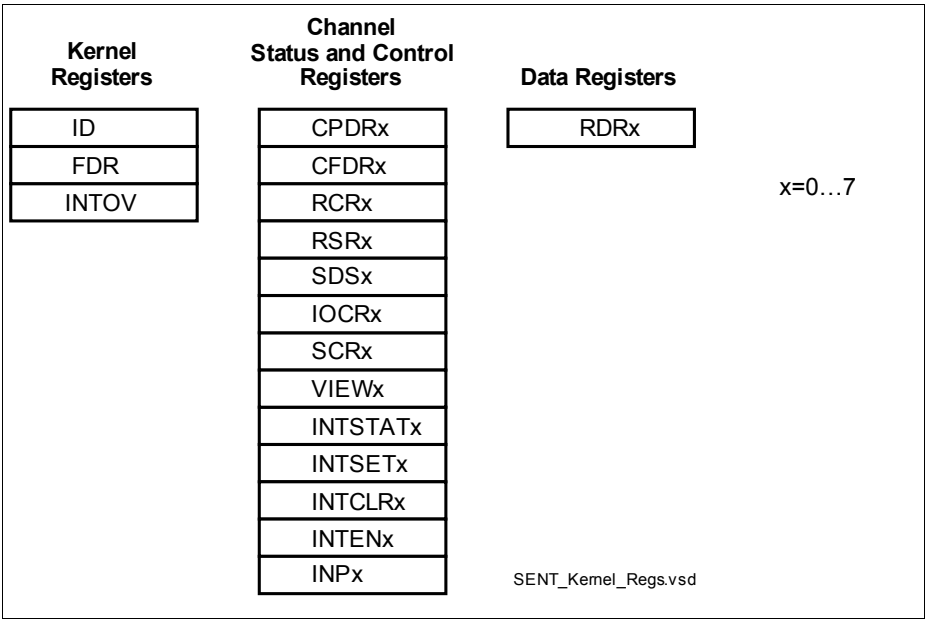


Figure 25-21 SENT Kernel Registers

The complete and detailed address map of the SENT module is described in **Table 25-1** on **Page 25-22**.

Note: x can take the values 0 … 7

Table 25-1 Registers Address Space - SENT Kernel Registers

Module	Base Address	End Address	Note
SENT	$F032\ 1000_H$	$F032\ 19FF_H$	–

Table 25-2 Registers Overview - SENT Kernel Registers

Register Short Name	Register Long Name	Offset Address [1]	Access Mode		Description see
			Read	Write	
SENT_CLC	SENT Clock Control Register	00_H	SV, U	SV, E	Page 25-26
-	reserved	04_H - 07_H	nBE	nBE	
SENT_ID	Module Identification Register	08_H	SV, U	nBE	Page 25-25
SENT_FDR	Module Fractional Divider	$0C_H$	SV, U	E	Page 25-27
-	reserved	10_H	nBE	nBE	
SENT_INTOV	Interrupt Overview Register	14_H	SV, U	SV, U	Page 25-48
-	reserved	18_H - $7C_H$	nBE	nBE	
SENT_RDRx	Receive Data Register 0	80_H - $9C_H$	SV, U	SV, U	Page 25-42
-	reserved	$A0_H$ - FC_H	nBE	nBE	
SENT_CPDRx	Channel Pre Divider Register 0	$100_H + x * 40_H$	SV, U	SV, U	Page 25-29
SENT_CFDRx	Channel Fractional Divider Register 0	$104_H + x * 40_H$	SV, U	SV, U	Page 25-30
SENT_RCRx	Receiver Control Register 0	$108_H + x * 40_H$	SV, U	SV, U	Page 25-31
SENT_RSRx	Receive Status Register 0	$10C_H + x * 40_H$	SV, U	SV, U	Page 25-37
SENT_SDSx	Serial Data and Status Register 0	$110_H + x * 40_H$	SV, U	SV, U	Page 25-38
SENT_IOCRx	Input and Output Control Register 0	$114_H + x * 40_H$	SV, U	SV, U	Page 25-39
SENT_SCRx	SPC Control Register 0	$118_H + x * 40_H$	SV, U	SV, U	Page 25-46
SENT_VIEWx	Receive Data View Register 0	$11C_H + x * 40_H$	SV, U	SV, U	Page 25-44
SENT_INTSTATx	Interrupt Status Register 0	$120_H + x * 40_H$	SV, U	SV, U	Page 25-49

Table 25-2 Registers Overview - SENT Kernel Registers (cont'd)

Register Short Name	Register Long Name	Offset Address [1]	Access Mode		Description see
			Read	Write	
SENT_INTSETx	Interrupt Set Register 0	124_H + x * 40_H	SV, U	SV, U	Page 25-55
SENT_INTCLRx	Interrupt Clear Register 0	128_H + x * 40_H	SV, U	SV, U	Page 25-57
SENT_INTENx	Interrupt Enable Register 0	$12C_H$ + x * 40_H	SV, U	SV, U	Page 25-59
SENT_INPx	Interrupt Node Pointer Register 0	130_H + x * 40_H	SV, U	SV, U	Page 25-62
-	reserved	134_H + x * 40_H - $13F_H$ + x * 40_H	nBE	nBE	
SENT_SRC3	Service Request Control 3 Register	$9F0_H$	SV, U	SV, U	Page 25-71
SENT_SRC2	Service Request Control 2 Register	$9F4_H$	SV, U	SV, U	Page 25-71
SENT_SRC1	Service Request Control 1 Register	$9F8_H$	SV, U	SV, U	Page 25-71
SENT_SRC0	Service Request Control 0 Register	$9FC_H$	SV, U	SV, U	Page 25-71

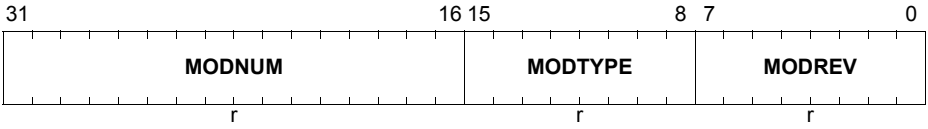
1) The absolute register address is calculated as follows:
Module Base Address (Table 25-1) + Offset Address (shown in this column)

25.2.1 Module Control

Module Identification Register

The SENT Module Identification Register ID contains read-only information about the module version.

ID
Module Identification Register **(08_H)** **Reset Value: $0080\ C0XX_H$**

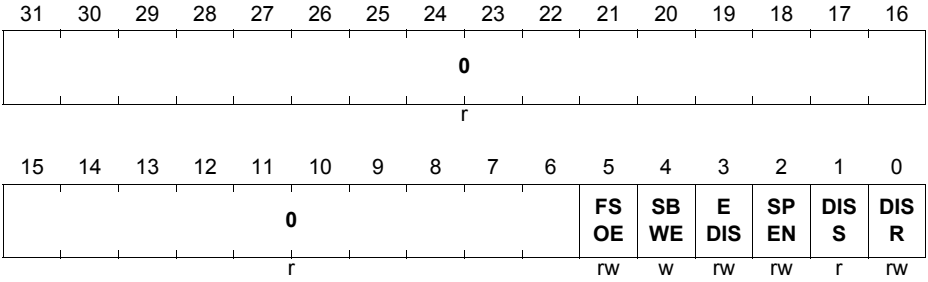


Field	Bits	Type	Description
MODREV	[7:0]	r	**Module Revision Number** This bit field defines the module revision number. The value of a module revision starts with 01_H (first revision).
MODTYPE	[15:8]	r	**Module Type** This bit field defines the module as a 32-bit module: $C0_H$
MODNUM	[31:16]	r	**Module Number Value** This bit field defines the module identification number for the SENT: 0080_H

Clock Control Register

This chapter summarizes the features of clock control. CLC controls in general switching on and off of the module. Please refer to Chapter “Module Clock Generation” of TC1798 for more details.

SENT_CLC
SENT Clock Control Register **(00_H)** **Reset Value: 0000 0003$_H$**



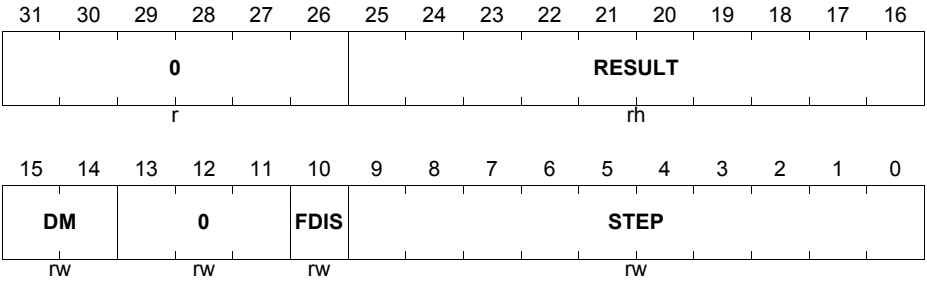
Field	Bits	Type	Description
DISR	0	rw	**Module Disable Request Bit** Used for enable/disable control of the module.
DISS	1	r	**Module Disable Status Bit** Bit indicates the current status of the module.
SPEN	2	rw	**Module Suspend Enable for OCDS** Used to enable the suspend mode
EDIS	3	rw	**Sleep Mode Enable Control** Used to control module’s sleep mode.
SBWE	4	w	**Module Suspend Bit Write Enable for OCDS** Determines whether SPEN and FSOE are write-protected.
FSOE	5	rw	**Fast Switch Off Enable** Used to switch off fast clock in Suspend Mode.
0	[31:6]	r	**Reserved** Read as 0; should be written with 0.

Note: After a hardware reset operation, the f_{SENT} and $f_{fracdiv}$ clocks are switched off and the SENT module is disabled (DISS set).

Fractional Divider Register

The Fractional Divider Register controls the input clock $f_{fracdiv}$ of all SENT channels.

SENT_FDR
SENT Fractional Divider Register ($0C_H$) Reset Value: $0000\ 0000_H$



Field	Bits	Type	Description
STEP	[9:0]	rw	**Step Value** Reload or addition value for RESULT.
FDIS	10	rw	**Freeze Disable** This bit controls the freeze function for this module. For more details please refer to SCU chapter, section Clock Control. 0_B Module operates on corrected clock, with reduced modulation jitter (default) 1_B Module operates on uncorrected clock with full modulation jitter
DM	[15:14]	rw	**Divider Mode** DM selects normal or fractional divider mode. 00_B Fractional divider is switched off; no output clock is generated. The Reset External Divider signal is 1. RESULT is not updated (default after System Reset). 01_B Normal Divider Mode selected. 10_B Fractional Divider Mode selected. 11_B Fractional divider is switched off; no output clock is generated. RESULT is not updated.
RESULT	[25:16]	rh	**Result Value** Bit field for the addition result.

Field	Bits	Type	Description
0	[13:11], [31:26]	r	**Reserved** Read as 0; should be written with 0.

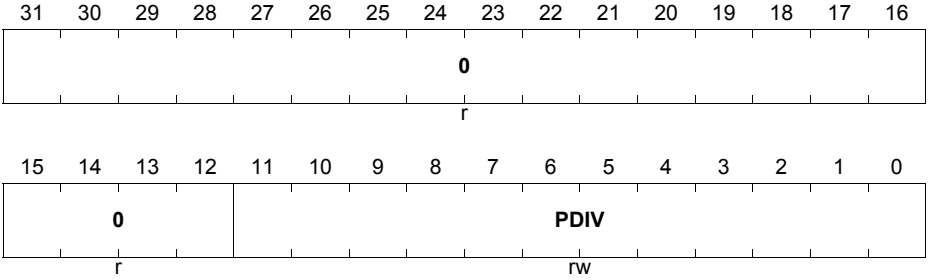
25.2.2 Channel Baud Rate Registers

Channel Pre Divider Register

The Channel Pre Divider Register CPDRx contains the pre divider that is related to the SENT channel baud rate.

See **Equation (25.3)**

CPDRx (x = 0-7)
Channel Pre Divider Register x **(100_H+40_H*x)** **Reset Value: 0000 0000_H**



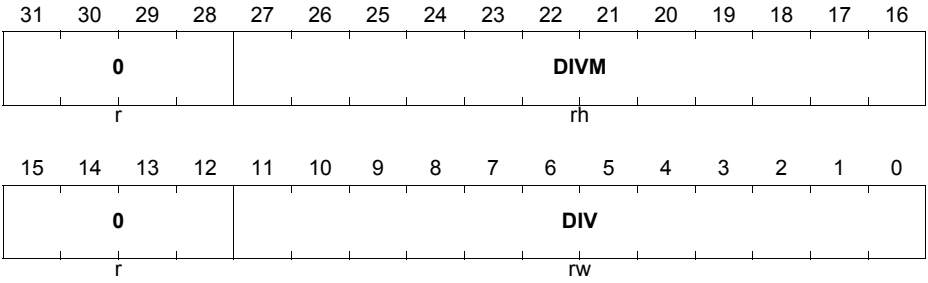
Field	Bits	Type	Description
PDIV	[11:0]	rw	**Divider Factor of Pre Divider for Channel x** Divides $f_{fracdiv}$ by (PDIV + 1) and delivers f_{pdiv_x} to the Channel Fractional Divider. RCR.CEN must be cleared before changing CPDR.PDIV or CFDR.DIV.
0	[31:12]	r	**Reserved** Read as 0; should be written with 0.

Channel Fractional Divider Register

The Channel Fractional Divider Register CFDRx contains control bits/bit fields that are related to the SENT channel baud rate.

See **Equation (25.4)** in **Chapter 25.1.5** for a detailed description.

CFDRx (x = 0-7)
Channel Fractional Divider Register x(104_H+40_H*x) **Reset Value: 0000 0000_H**



Field	Bits	Type	Description
DIV	[11:0]	rw	**Divider Value** Initial and reference divider value for the CFDR. DIV must be programmed > 0. If cleared, DIV becomes 1. If written, DIVM is updated automatically with the same value.RCR.CEN must be cleared before changing CPDR.PDIV or CFDR.DIV.
DIVM	[27:16]	rh	**Measured Divider Value** DIVM is automatically updated by HW to adjust the receiver frequency to the current sender frequency. This value is kept automatically in the range of 75% DIV < DIVM < 125% DIV Write data is ignored.
0	[15:12], [31:28]	r	**Reserved** Read as 0; should be written with 0.

25.2.3 Receiver Control and Status Registers

Receiver Control Register

The Receiver Control Register RCRx contains control bits/bit fields that are related to the SENT receiver operation.

RCRx (x = 0-7)
Receiver Control Register x **(108_H+40_H*x)** **Reset Value: 0000 0000_H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0												SUS EN	IDE	ESF	CRZ
r												rw	rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FRL								CFC	CDIS	SC DIS	SDP	SNI	ACE	IEP	CEN
rw								rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
CEN	0	rw	**Channel Enable** When CEN is set, the receiver of channel x is enabled. The internal receiver state machine can be initialized by switching the channel off and on. This does not change the current register content. 0_B channel x disabled (default) 1_B channel x enabled
IEP	1	rw	**Ignore End Pulse** When IEP is set, an end pulse is ignored. An end pulse can be generated in SPC mode or as pause pulse. 0_B End Pulse not ignored (default) 1_B End Pulse ignored For systems with an end pulse, during synchronize or re-synchronize of reception, if calibration pulses are detected one immediately following the other, the first calibration pulse shall be ignored as it may be a pause pulse with duration matching the calibration pulse range.

Field	Bits	Type	Description
ACE	2	rw	**Alternative CRC Mode Enable** When ACE is set, the CRC is calculated in an alternative way for both: fast (signal) and slow (serial message) data path. *Note: If ESF is set, the standard 6 bit CRC is always used for the serial message and ACE is ignored.* 0_B Serial CRC calculation as specified in J2716 FEB2008 Rev. 3 2009-06-24 (default) 1_B Alternative: 4 bit in parallel CRC calculation as used e.g. in hall sensor TLE4998C.
SNI	3	rw	**Status Nibble Included in CRC** When SNI is set, the status Nibble is included in (signal data) CRC. 0_B Status Nibble not included in CRC (default) 1_B Status Nibble included in CRC (as used e.g. in hall sensor TLE4998C).
SDP	4	rw	**Serial Data Processing Mode** This bit switches automatic serial data processing on. 0_B Automatic Serial Data Processing is disabled. Status and Communication nibble can be read from RSRx for SW processing. (default) 1_B Automatic Serial Data Processing is enabled. Status and Communication nibble can be read from RSRx; Message ID, Serial Data and SCRC can be read from SDSx after serial data interrupt SDI is activated.
SCDIS	5	rw	**CRC for Serial Data Disabled Mode** This bit selects the CRC disabled mode. 00_B CRC is enabled (default) 01_B CRC is disabled CRC nibble can be read from SDSx. The CPU must perform the CRC on the current data by SW.

Field	Bits	Type	Description
CDIS	6	rw	**CRC Disabled Mode** This bit selects the CRC disabled mode. 00_B CRC is enabled (default) 01_B CRC is disabled CRC nibble can be read from RSRx. The CPU must perform the CRC on the current data by SW.

Field	Bits	Type	Description
CFC	7	rw	**Consecutive Frame Check** This bit determines the way the most recently received frame buffer is indicated as valid. 0_B **Check against Past Sync Pulse** The current Synchronization / Calibration Pulse is compared to the Synchronization / Calibration Pulse received immediately before. The whole frame is invalid if the Synchronization / Calibration Pulse length differs from the length of the Synchronization / Calibration Pulse before by more than 1.5625%. In this case of error, its length is not used as new reference. In case the check passes and no other error occurs the Frame Buffer is indicated valid immediately after CRC calculation result is correct. Resynchronization: On the third successive calibration pulse error, the current calibration pulse value is considered as valid and the message accepted unless the message frame contains other errors. In both cases a receive data interrupt (RDI), or a referring error interrupt is issued. 1_B **Check against Future Sync Pulse** The current Synchronization / Calibration Pulse is compared with the Synchronization / Calibration Pulse received immediately after the current frame. The whole frame is invalid if the Synchronization / Calibration Pulse length differs from the length of the following Synchronization / Calibration Pulse by more than 1.5625%. Resynchronization: In this case of error, the current length is used as new reference. Note: The whole frame can be indicated valid only after additionally measuring the Synchronization / Calibration Pulse of the successive frame.

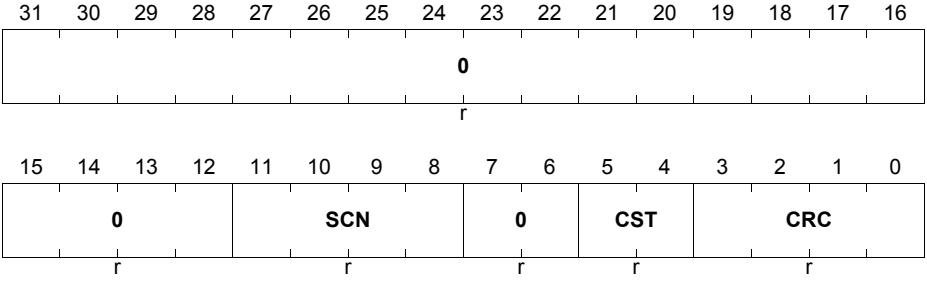
Field	Bits	Type	Description
FRL	[15:8]	rw	**Frame Length** FRL determines the number of data nibbles per frame that the SENT channel x is setup for. Note that FRL does not include the Synchronization / Calibration Pulse, the Status and Communication nibble, the CRC nibble nor the additional zero length nibble that might be introduced by use of SPC. 00000000_B No data nibble 00000001_B 1 data nibble 00000010_B 2 data nibbles 00000011_B 3 nibbles …B … 00001000_B 8 nibbles Maximum in normal length mode …B … 11111111_B 255 nibbles If more than 8 nibbles are configured, please note: In addition to the receive success interrupt RSI at the successfully received end of a frame, a receive data interrupt RDI is issued each time 8 nibbles have been transferred to the Receive Data Register RDRx. At the end of a frame, RDI is issued if RSI is issued. If an error occurred, RDI is not set at the end of a frame. If no CRC has been received at the point in time where RDI is issued, the receive data interrupt is no indication whether or not the transfer was successful so far. A CRC Error Interrupt is issued at the end of the frame if Automatic CRC check is enabled and the CRC is wrong.
CRZ	16	rw	**CRC with Zero Nibble for Serial Data** This bit selects the CRC method. If set, a ZERO NIBBLE at the end of CRC calculation (and only in calculation) is added. E.g. as 7th nibble (in case of 6 data nibbles) 00_B Trailing zero nibble added in calculation, recommended by standard (default) 01_B NO trailing zero nibble added in calculation, legacy mode by standard. Background: if the common slope of last nibble and CRC moves in error, the error correction is worse for the last nibble than for all other nibbles. Setting CRZ overcomes this problem.

Field	Bits	Type	Description
ESF	17	rw	**Extended Serial Frame Mode** This bit selects the serial frame structure. 0_B standard (16 frames, 4 bit ID, 8 bit data, 4 bit CRC) 1_B extended (18 frames, 4 or 8 bit ID, 12 or 16 bit data, 6 bit CRC)
IDE	18	rw	**Ignore Drift Error Mode** This bit selects if drift errors lead to frame rejection and if an interrupt (INTSTAT.FDI) is generated. Used, if sensors are triggered by SPC. During a long pause period the accumulated drift could be more than 1.5625%. In this special case setting IDE is useful. 0_B Drift Errors enabled (default) 1_B Drift Errors disabled
SUSEN	19	rw	**Suspend Enable** This bit makes it possible to set the SENT channel into Suspend Mode via OCDS (on chip debug support): 0_B An OCDS suspend trigger is ignored by this SENT channel. 1_B An OCDS suspend trigger disables the SENT channel: As soon as the SPC sender logic of the SENT channel becomes idle, the module is stopped while all registers of the channel stay readable. The receiver is stopped unconditionally. A partly received frame is discarded. Bit SUSEN is reset via OCDS Reset.
0	[31:20]	r	**Reserved** Read as 0; should be written with 0.

Receiver Status Register

The Receive Status Register provides the status information of channel x.

RSRx (x = 0-7)
Receive Status Register x **($10C_H$+40_H*x)** **Reset Value: 0000 0000_H**

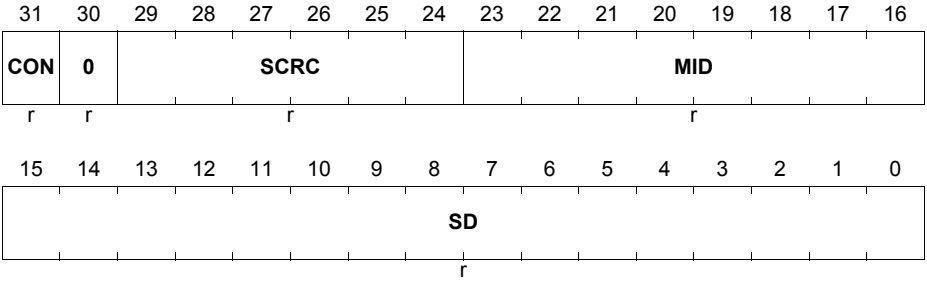


Field	Bits	Type	Description
CRC	[3:0]	r	**CRC** of last frame. CRC_0 is on bit position 0.
CST	[5:4]	r	**Channel Status** CST shows the current status of channel x. 00_B STOP Channel is disabled and can be configured 01_B INITIALIZED Channel is configured and enabled and no Synchronization / Calibration Pulse was received since last enable. 10_B RUNNING one or more Synchronization / Calibration Pulses were received and Frequency Range or Frequency Drift not or no longer in range. Fallback status from SYNCHRONIZED. 11_B SYNCHRONIZED Frequency Range and Frequency Drift in range
SCN	[11:8]	r	**Status and Communication Nibble** of last frame. SCN_0 is on bit position 8.
0	[7:6], [31:12]	r	**Reserved** Read as 0; should be written with 0.

Serial Data and Status Register

The Serial (Receive) Data and Status Register provides the data and status information of channel x.

SDSx (x = 0-7)
Serial Data and Status Register x (110_H+40_H*x) **Reset Value: 0000 0000_H**



Field	Bits	Type	Description
SD	[15:0]	r	**Serial Data** of last serial data frame. SD_0 is on bit position 0. If RCR.ESF is cleared 8 bits of data are available and bits [15:8] are zero. If RCR.ESF is set and if SDS.CON is cleared 12 bits of data are available and bits [15:12] are zero.
MID	[23:16]	r	**Message ID** of last serial data frame. ID_0 is on bit position 16. If RCR.ESF is cleared, or if SDS.CON is set, bits [23:20] are zero.
SCRC	[29:24]	r	**SCRC** CRC of last serial data frame. CRC_0 is on position 24. If RCR.ESF is cleared, bits [29:28] are always zero.
CON	31	r	**Configuration bit** of last serial frame. 0_B 12-bit data and 8-bit message ID 1_B 16-bit data and 4-bit message ID
0	30	r	**Reserved** Read as 0; should be written with 0.

25.2.4 Input and Output Control

Input and Output Control Register Functions

The Input and Output Control Register IOCRx determines for the SENT channel x:

for the receiver:

- the alternate input
- the filter depth
- the input signal polarity

for the SPC Unit

- the trigger source
- the output signal polarity

IOCRx (x = 0-7)
Input and Output Control Register x(114_H+40_H*x) **Reset Value: 0000 0000_H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TXM	RXM	TRM	CTR	0									ETS		
rh	rh	rh	rw	r									rw		

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C FEG	C REG	FEG	REG	0		IIE	OIE	DEPTH				0		ALTI	
rw	rw	rh	rh	r		rw	rw	rw				r		rw	

Field	Bits	Type	Description
ALTI	[1:0]	rw	**Alternate Input Select** Selects the alternate input for channel y: 0000_BAlternate Input 0 selected 0001_BAlternate Input 1 selected …$_B$ … 0011_BAlternate Input 3 selected

Field	Bits	Type	Description
DEPTH	[7:4]	rw	**Digital Glitch Filter Depth** DEPTH determines the number of port input samples clocked with f_{pdiv} that are taken into account for the calculation of the floating average. The higher DEPTH is chosen to be, the longer the glitches that are suppressed and the longer the delay of the input signal introduced by this filter. 0000_B off, default 0001_B 1 T_{pdiv} 0010_B 2 0011_B 3 …B … 1111_B 15
OIE	8	rw	**Output Inverter Enable Channel x** Selects the Pulse Polarity of the output of channel x 0_B Pulse polarity is active low 1_B Pulse polarity is active high
IIE	9	rw	**Input Inverter Enable Channel x** Selects the Pulse Polarity of the input of channel x 0_B Pulse polarity is active low 1_B Pulse polarity is active high
REG	12	rh	**Rising Edge Glitch Flag for Channel x** Shows the status of the glitch detection of channel x 0_B No Glitch detected on rising edge 1_B Glitch detected on rising edge REG is cleared by setting CREG.
FEG	13	rh	**Falling Edge Glitch Flag for Channel x** Shows the status of the glitch detection of channel x 0_B No Glitch detected on falling edge 1_B Glitch detected on falling edge FEG is cleared by setting CFEG.
CREG	14	rw	**Clear Rising Edge Glitch Flag for Channel x** Clears the status flag REG 0_B REG is not cleared 1_B REG is cleared CREG always read zero.

Field	Bits	Type	Description
CFEG	15	rw	**Clear Falling Edge Glitch Flag for Channel x** Clears the status flag FEG 0_B FEG is not cleared 1_B FEG is cleared CFEG always read zero.
ETS	[18:16]	rw	**External Trigger Select** Selects the external trigger line if SCRx.TRIG is programmed to 11_B. 000_B TRIG0 001_B TRIG1 …B … 111_B TRIG7
CTR	28	rw	**Clear Trigger Monitor Flag for Channel x** Clears the status flag TRM 0_B TRM is not cleared 1_B TRM is cleared CTR always read zero.
TRM	29	rh	**Trigger Monitor Flag for Channel x** Shows the status of the trigger detection of channel x 0_B No Trigger detected 1_B Trigger detected (one or several) TRM is cleared by setting CTR.
RXM	30	rh	**Receive Monitor for Channel x** Shows the status of the receive signal of channel x after glitch filtering and inverted as specified by IIE. 0_B Current signal is low. 1_B Current signal is high.
TXM	31	rh	**Transmit Monitor for Channel x** Shows the status of the transmit signal of channel x inverted as specified by OIE. 0_B Current signal is low. 1_B Current signal is high.
0	[3:2], [11:10], [27:19]	r	**Reserved** Read as 0; should be written with 0.

25.2.5 Receive Data Registers

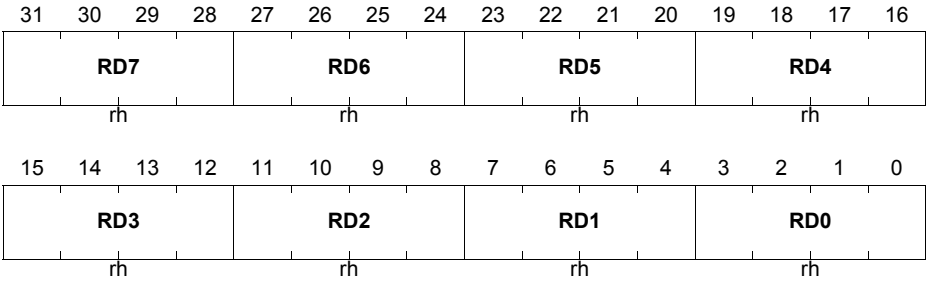
Receive Data Registers RDRx

The Receive Data Registers RDRx for channel x shows the data content of a received data frame. Register VIEWx is used to sort the nibbles.

Note: Register VIEW must be set up correctly to see all data nibbles of the frame! By default the application software set VIEW to 7654 3210$_H$.

Note: The internal receive buffer is always cleared (0x0000 0000$_H$) at each frame start. Thus unused nibbles are always read as zero.

RDRx (x = 0-7)
Receive Data Register x **(80_H+x*4_H)** **Reset Value: 0000 0000_H**



Field	Bits	Type	Description
RDy (y = 0-7)	[4*y+3 :4*y]	rh	**Receive Data Nibble y** RDy shows the nibble from the received frame that is sorted to this position. It can be selected by any of VIEWx.RDNPy (y = 0-7). By default all nibbles are sorted to RD0 as the reset value of VIEW is 0x0000 0000_H. I.e. at the end of frame reception RD0 contains the last data nibble of the frame.

Receive Data View Register VIEWx

The Receive Data View Registers VIEWx stores the nibble pointers. They determine the sequence in which the received data nibbles are presented to the host. This reduces the SW effort to sort the nibbles.
The data nibble that is received first in the received frame is moved to the location given in register VIEW.RDNP0, the second to VIEW.RDNP1 and so on until VIEW.RDNP7.
If more than one VIEW.RDNPx point to a certain location in RDR, the last one will overwrite the previous ones.
Example: two 12 bit values are transmitted. One with highest significant nibble first and one with lowest significant nibble first. The frame looks like this: 456321_H. Note that the 1 is received as first data nibble and the 4 comes in as last data nibble.
The actual signal values are $0x123_H$ and $0x456_H$. By using VIEWx this can be sorted out into two 16bit values by HW. In the example VIEWx would be set to: 73 654 012_H. 73 is a dummy value and is not regarded if not more than 6 nibbles are received in a frame. The Register RDRx looks like this: 0x0456 0123_H to the host.

In the example RDR nibbles 3 and 7 contain $0x0000_B$ as the Receive Buffer is always cleared (0x0000 0000_H) before new data is received.

If a frame contains more than eight nibbles and the sorting can not be specified statically, VIEW can be set to e.g. 7654 3210_H.

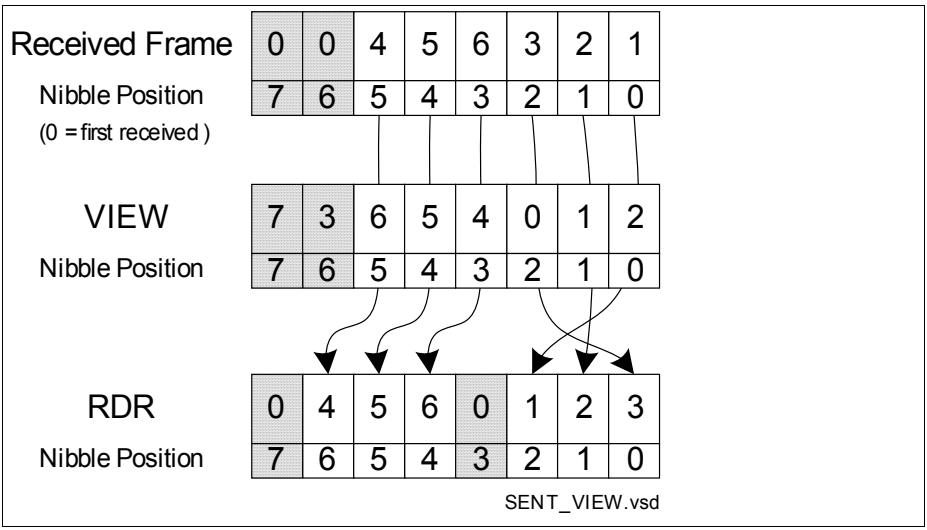


Figure 25-22 Functionality of VIEW Register

VIEWx (x = 0-7)
Receive Data View Register x **($11C_H$+40_H*x)** **Reset Value: 0000 0000_H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	RDNP7			0	RDNP6			0	RDNP5			0	RDNP4		
r	rw			r	rw			r	rw			r	rw		

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	RDNP3			0	RDNP2			0	RDNP1			0	RDNP0		
r	rw			r	rw			r	rw			r	rw		

Field	Bits	Type	Description
RDNPy (y = 0-7)	[4*y+2 :4*y]	rw	**Receive Data Target Nibble Pointer y** RDNPy points to the Nibble in Receive Data Register RDRx where the nibble y from the received frame is sorted to. Nibble 0 is the first data nibble in the frame. It gets moved to the position defined in RDNP0. And on. 000_B Nibble 0 selected 001_B Nibble 1 selected $\ldots_B$ … 111_B Nibble 7 selected *Note: RDNPy must be written before first frame reception. All RDNPy must have different values. (Higher RDNPy overwrite lower RDNPy.)*
0	3, 7, 11, 15, 19, 23, 27, 31	r	**Reserved** Read as 0; should be written with 0.

25.2.6 SPC Control

SPC Control Registers SCRx

The SPC Control Register SCR contains data to be transmitted during the sync pulse of the data frames. It contains as well the trigger control bits required for sending nibbles from the SENT module to the sensor / external SENT device.

The SPC Control Register is used to control the trigger mode and time base of the SPC channel transmission.

Data and the control bits are collected in this single register to ease transfer of multiple pulses in cases where dynamic switching of the trigger condition is required.

The SPC Control Register is build to control single pulse transfers only.

Thus it is possible to change the control settings of an individual channel from pulse to pulse as it is required in SPC mode “Bidirectional transmit”. Here it might be considered useful to change trigger mode between Mode 1 (immediately) and Mode 2 (falling edge of next Synchronization / Calibration Pulse with programmable delay).

In addition repeating transfers with the same control settings are supported. For a pulse transfer to be initiated a synchronization signal can be sufficient and no further SW intervention is required. Here the data can be changed (“ID-Selection” Mode) or simply left constant (“Sync” Mode). Only a HW trigger needs to be set up.

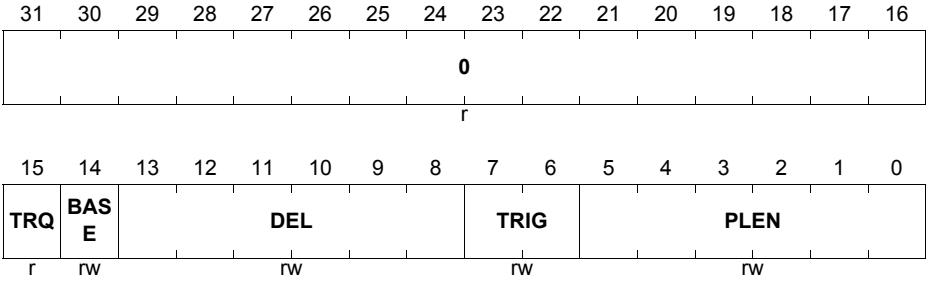
In Mode 0, SPC is deactivated for this channel. A write access to SCRx does not initiate an SPC pulse transmission. All state transmitter machines are initialized.

In Mode 1, an SPC pulse is sent, each time SPC Control Register SCRx is written to. If a transfer is ongoing, the channel waits automatically until the internal transmission register is ready. Transmit Buffer Underflow bit TBIx is set after data has been completely transferred (PLEN exceeded) and no new data was written to SCRx. After the data was transferred to the internal transmission register, interrupt TDIx signals that a new value can be written. INTSTATx.TDIx must be cleared by SW. Independently from this interrupt pending bit, a new interrupt pulse is generated on each transfer of an SPC pulse.
This mode is important for back to back transfers of several nibbles as in bidirectional SPC mode.

In Mode 2, an SPC pulse is sent, each time the first falling edge of any Synchronization / Calibration Pulse is received. In this mode, the programmable delay DEL is most useful. In SPC mode “Bidirectional Transmit” this mode is useful to synchronize the transmission. TDIx and TBIx work as in Mode 1.

In Mode 3, an SPC pulse is sent (with current DEL and PLEN) after each external trigger event (defined by IOCRx.ETS). This is most useful in SPC “sync” mode. TDIx and TBIx work as in Mode 1.

SCRx (x = 0-7)
SPC Control Register x **(118_H+40_H*x)** **Reset Value: 0000 0000_H**

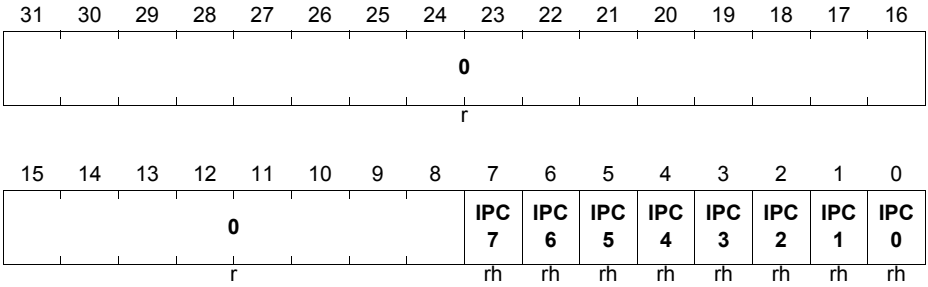


Field	Bits	Type	Description
PLEN	[5:0]	rw	**Pulse Length** Defines the length of the pulse in tick times. The time base is the measured tick time of the latest received frame if selected so by BASE. In case this measured tick time was invalid or not already available after enable of the channel, the nominal time base of the module is used. 000000_B Pulse length is 0 ticks 000001_B Pulse length is 1 tick ... ... 111111_B Pulse length is 63 ticks

Field	Bits	Type	Description
TRIG	[7:6]	rw	**Trigger Source and Mode Selection** Selects the Trigger Source and Mode. The internal sender state machine can be initialized by switching the channel off (TRIG is cleared) and on. This does not change the current register content. 00_B No Pulse is generated, OFF When cleared, an ongoing transfer is stopped immediately and the transmit output is driven recessive. 01_B Pulse starts immediately (no auto repetition) 10_B Pulse starts each time the first falling edge of any Synchronization / Calibration Pulse is received (auto repetition on next Sync. / Cal. Pulses) 11_B Pulse starts after each external trigger event. (auto repetition on next trigger) IOCRx.ETS selects the source of this event.
DEL	[13:8]	rw	**Delay Length** Selects how long the SPC pulse is delayed after the trigger condition. The time base is the measured tick time of the latest received frame if selected so by BASE. In case this measured tick time was invalid or not already available after enable of the channel, the nominal time base of the module is used. 000000_B Pulse is not delayed 000001_B Pulse is delayed by 1 tick ... ... 111111_B Pulse is delayed by 63 ticks
BASE	14	rw	**Time Base** Selects the Pulse Time Base 0_B Pulse is based on measured frequency of last Synchronization/Calibration Pulse 1_B Pulse is based on nominal frequency
TRQ	15	r	**Transfer Request in Progress** While an SPC Pulse is being sent this bit is set. Write access is ignored.
0	[31:16]	r	**Reserved** Read as 0; should be written with 0.

25.2.7 Interrupt Control Registers

INTOV
Interrupt Overview Register **(14_H)** **Reset Value: 0000 0000$_H$**



Field	Bits	Type	Description
IPCy (y = 0-7)	y	rh	**Interrupt Pending on Channel y** If any interrupt requested flag is set for channel y in register INTSTATy AND the referring interrupt is enabled in INTENx then IPCy is set. It is automatically reset if all flags in INTSTATy are cleared for which the referring interrupt is enabled in INTENx.
0	[31:8]	r	**Reserved** Read as 0.

Interrupt Status Register

The Interrupt Status Register INTSTATx contains status bits that show the status of any interrupt of SENT channel x.

Note: The bits are set independently from the referring Interrupt Enable in Register INTENx. Thus they can be used as status bits as well e.g. by a SW based on polling.

INTSTATx (x = 0-7)
Interrupt Status Register x **(120_H+40_H*x)** **Reset Value: 0000 0000_H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	**0**	**0**	**SCRI**	**SDI**	**WSI**	**CRCI**	**NVI**	**NNI**	**FDI**	**FRI**	**TBI**	**TDI**	**RBI**	**RDI**	**RSI**
r	r	r	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh

Field	Bits	Type	Description
RSI	0	rh	**Receive Success Interrupt Request Flag** This bit is set at the successfully received end of a frame. Depending on bit RCRx.CDIS this indicates a successful check of the CRC. 0_B No interrupt was requested since this bit was cleared the last time 1_B An interrupt was requested since this bit was cleared the last time This bit can be cleared by bit INTCLRx.RSI. This bit can be set by bit INTSETx.RSI. This bit is set independently from INTENx.

Field	Bits	Type	Description
RDI	1	rh	**Receive Data Interrupt Request Flag** RDI is activated when a received frame is moved to a Receive Data Register RDR. Both RDI and RSI will be issued together in normal use cases where the frame size is not bigger than 8 nibbles and CRC is correct or not checked (if RCRx.CDIS is cleared). 0_B No interrupt was requested since this bit was cleared the last time 1_B An interrupt was requested since this bit was cleared the last time This bit can be cleared by bit INTCLRx.RDI. This bit can be set by bit INTSETx.RDI. This bit is set independently from INTENx.
RBI	2	rh	**Receive Buffer Overflow Interrupt Request Flag** This bit is set after a frame has been received while the old one was not read from RDRx. I.e. the kernel wants to set any of the two interrupts RSI and RDI and finds any of these two interrupts already set.The old data is overwritten by the new data. 0_B No interrupt was requested since this bit was cleared the last time 1_B An interrupt was requested since this bit was cleared the last time This bit is NOT cleared by reading RDRx. This bit can be cleared by bit INTCLRx.RBI. This bit can be set by bit INTSETx.RBI. This bit is set independently from INTENx.
TDI	3	rh	**Transfer Data Interrupt Request Flag** This bit is set after the trigger condition was detected. Data to be transferred has been moved internally. Thus a new value can be written to SCRx. This can be used for back to back transfers. 0_B No interrupt was requested since this bit was cleared the last time 1_B An interrupt was requested since this bit was cleared the last time This bit is automatically cleared by writing SCRx. This bit can be cleared by bit INTCLRx.TDI. This bit can be set by bit INTSETx.TDI. This bit is set independently from INTENx.

Field	Bits	Type	Description
TBI	4	rh	**Transmit Buffer Underflow Interrupt Request Flag** This bit is set after data has been completely transferred (PLEN exceeded) and no new data was written to SCRx. 0_B No interrupt was requested since this bit was cleared the last time 1_B An interrupt was requested since this bit was cleared the last time This bit is NOT cleared by writing SCRx. This bit can be cleared by bit INTCLRx.TBI. This bit can be set by bit INTSETx.TBI. This bit is set independently from INTENx.
FRI	5	rh	**Frequency Range Interrupt Request Flag** This bit is set after a Synchronization / Calibration pulse was received that deviates more than +- 25% from the nominal value. The referring data is ignored. 0_B No interrupt was requested since this bit was cleared the last time 1_B An interrupt was requested since this bit was cleared the last time This bit can be cleared by bit INTCLRx.FRI. This bit can be set by bit INTSETx.FRI. This bit is set independently from INTENx.
FDI	6	rh	**Frequency Drift Interrupt Request Flag** This bit is set after a subsequent Synchronization / Calibration pulse was received that deviates more than 0.15625% (1/64) from its predecessor. (See RCR.CFC) 0_B No interrupt was requested since this bit was cleared the last time 1_B An interrupt was requested since this bit was cleared the last time This bit can be cleared by bit INTCLRx.FDI. This bit can be set by bit INTSETx.FRI. This bit is set independently from INTENx.

Field	Bits	Type	Description
NNI	7	rh	**Number of Nibbles Wrong Request Flag** This bit is set after a more nibbles have been received than expected or a Synchronization / Calibration Pulse is received too early thus too few nibbles have been received. 0_B No interrupt was requested since this bit was cleared the last time 1_B An interrupt was requested since this bit was cleared the last time This bit can be cleared by bit INTCLRx.NNI. This bit can be set by bit INTSETx.NNI. This bit is set independently from INTENx.
NVI	8	rh	**Nibbles Value out of Range Request Flag** This bit is set after a too long or too short nibble pulse has been received. I.e. value < 0 or value > 15. 0_B No interrupt was requested since this bit was cleared the last time 1_B An interrupt was requested since this bit was cleared the last time This bit can be cleared by bit INTCLRx.NVI. This bit can be set by bit INTSETx.NVI. This bit is set independently from INTENx.
CRCI	9	rh	**CRC Error Request Flag** This bit is set if the CRC fails. 0_B No interrupt was requested since this bit was cleared the last time 1_B An interrupt was requested since this bit was cleared the last time This bit can be cleared by bit INTCLRx.CRCI. This bit can be set by bit INTSETx.CRCI. This bit is set independently from INTENx.

Field	Bits	Type	Description
WSI	10	rh	**Wrong Status and Communication Nibble Error Request Flag** In standard Serial Frame Mode (RCR.ESF is cleared), this bit is set if the Status and Communication nibble shows a start bit in a frame other than frame number n x 16. In Extended Serial Frame Mode this bit is without function. 0_B No interrupt was requested since this bit was cleared the last time 1_B An interrupt was requested since this bit was cleared the last time This bit can be cleared by bit INTCLRx.WSI. This bit can be set by bit INTSETx.WSI. This bit is set independently from INTENx.
SDI	11	rh	**Serial Data Receive Interrupt Request Flag** This bit is set after all serial data bits have been received via the Status and Communication nibble. Depending on bit RCRx.SCDIS this indicates a successful check of the CRC. 0_B No interrupt was requested since this bit was cleared the last time 1_B An interrupt was requested since this bit was cleared the last time This bit can be cleared by bit INTCLRx.SDI. This bit can be set by bit INTSETx.SDI. This bit is set independently from INTENx.
SCRI	12	rh	**Serial Data CRC Error Request Flag** This bit is set if the CRC of the serial message fails. In Extended Serial Message Format, this includes a check of the Serial Communication Nibble for correct 0 values of bit 3 in frames 7, 13 and 18. 0_B No interrupt was requested since this bit was cleared the last time 1_B An interrupt was requested since this bit was cleared the last time This bit can be cleared by bit INTCLRx.SCRI. This bit can be set by bit INTSETx.SCRI. This bit is set independently from INTENx.

Field	Bits	Type	Description
0	[31:13]	r	**Reserved** Read as 0.

Interrupt Set Register

The Interrupt Set Register INTSETx contains control bits that trigger an interrupt pulse for any interrupt of SENT channel x.

INTSETx (x = 0-7)
Interrupt Set Register x **(124_H+40_H*x)** **Reset Value: 0000 0000_H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	SCRI	SDI	WSI	CRCI	NVI	NNI	FDI	FRI	TBI	TDI	RBI	RDI	RSI
r	r	r	w	w	w	w	w	w	w	w	w	w	w	w	w

Field	Bits	Type	Description
RSI	0	w	**Set Interrupt Request Flag RSI** Setting this bit set bit INTSTATx.RSI. Clearing this bit has no effect. Reading this bit returns always zero.
RDI	1	w	**Set Interrupt Request Flag RDI** Setting this bit set bit INTSTATx.RDI. Clearing this bit has no effect. Reading this bit returns always zero.
RBI	2	w	**Set Interrupt Request Flag RBI** Setting this bit set bit INTSTATx.RBI. Clearing this bit has no effect. Reading this bit returns always zero.
TDI	3	w	**Set Interrupt Request Flag TDI** Setting this bit set bit INTSTATx.TDI. Clearing this bit has no effect. Reading this bit returns always zero.
TBI	4	w	**Set Interrupt Request Flag TBI** Setting this bit set bit INTSTATx.TBI. Clearing this bit has no effect. Reading this bit returns always zero.

Field	Bits	Type	Description
FRI	5	w	**Set Interrupt Request Flag FRI** Setting this bit set bit INTSTATx.FRI. Clearing this bit has no effect. Reading this bit returns always zero.
FDI	6	w	**Set Interrupt Request Flag FDI** Setting this bit set bit INTSTATx.FDI. Clearing this bit has no effect. Reading this bit returns always zero.
NNI	7	w	**Set Interrupt Request Flag NNI** Setting this bit set bit INTSTATx.NNI. Clearing this bit has no effect. Reading this bit returns always zero.
NVI	8	w	**Set Interrupt Request Flag NVI** Setting this bit set bit INTSTATx.NVI. Clearing this bit has no effect. Reading this bit returns always zero.
CRCI	9	w	**Set Interrupt Request Flag CRCI** Setting this bit set bit INTSTATx.CRCI. Clearing this bit has no effect. Reading this bit returns always zero.
WSI	10	w	**Set Interrupt Request Flag WSI** Setting this bit set bit INTSTATx.WSI. Clearing this bit has no effect. Reading this bit returns always zero.
SDI	11	w	**Set Interrupt Request Flag SDI** Setting this bit set bit INTSTATx.SDI. Clearing this bit has no effect. Reading this bit returns always zero.
SCRI	12	w	**Set Interrupt Request Flag SCRI** Setting this bit set bit INTSTATx.SCRI. Clearing this bit has no effect. Reading this bit returns always zero.
0	[31:13]	r	**Reserved** Read as 0; should be written with 0.

Interrupt Clear Register

The Interrupt Clear Register INTCLRx contains control bits that clear the status of any interrupt of SENT channel x.

INTCLRx (x = 0-7)
Interrupt Clear Register x **(128_H+40_H*x)** **Reset Value: 0000 0000_H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0	SCRI	SDI	WSI	CRCI	NVI	NNI	FDI	FRI	TBI	TDI	RBI	RDI	RSI
r	r	r	w	w	w	w	w	w	w	w	w	w	w	w	w

Field	Bits	Type	Description
RSI	0	w	**Clear Interrupt Request Flag RSI** Setting this bit clears bit INTSTATx.RSI. Clearing this bit has no effect. Reading this bit returns always zero.
RDI	1	w	**Clear Interrupt Request Flag RDI** Setting this bit clears bit INTSTATx.RDI. Clearing this bit has no effect. Reading this bit returns always zero.
RBI	2	w	**Clear Interrupt Request Flag RBI** Setting this bit clears bit INTSTATx.RBI. Clearing this bit has no effect. Reading this bit returns always zero.
TDI	3	w	**Clear Interrupt Request Flag TDI** Setting this bit clears bit INTSTATx.TDI. Clearing this bit has no effect. Reading this bit returns always zero.
TBI	4	w	**Clear Interrupt Request Flag TBI** Setting this bit clears bit INTSTATx.TBI. Clearing this bit has no effect. Reading this bit returns always zero.

Field	Bits	Type	Description
FRI	5	w	**Clear Interrupt Request Flag FRI** Setting this bit clears bit INTSTATx.FRI. Clearing this bit has no effect. Reading this bit returns always zero.
FDI	6	w	**Clear Interrupt Request Flag FDI** Setting this bit clears bit INTSTATx.FDI. Clearing this bit has no effect. Reading this bit returns always zero.
NNI	7	w	**Clear Interrupt Request Flag NMI** Setting this bit clears bit INTSTATx.NMI. Clearing this bit has no effect. Reading this bit returns always zero.
NVI	8	w	**Clear Interrupt Request Flag NVI** Setting this bit clears bit INTSTATx.NVI. Clearing this bit has no effect. Reading this bit returns always zero.
CRCI	9	w	**Clear Interrupt Request Flag CRCI** Setting this bit clears bit INTSTATx.CRCI. Clearing this bit has no effect. Reading this bit returns always zero.
WSI	10	w	**Clear Interrupt Request Flag WSI** Setting this bit clears bit INTSTATx.WSI. Clearing this bit has no effect. Reading this bit returns always zero.
SDI	11	w	**Clear Interrupt Request Flag SDI** Setting this bit clears bit INTSTATx.SDI. Clearing this bit has no effect. Reading this bit returns always zero.
SCRI	12	w	**Clear Interrupt Request Flag SCRI** Setting this bit clears bit INTSTATx.SCRI. Clearing this bit has no effect. Reading this bit returns always zero.
0	[31:13]	r	**Reserved** Read as 0; should be written with 0.

Interrupt Enable Register

The Interrupt Enable Register INTENx contains control bits that enable the interrupt source of any interrupt of SENT channel x.

Note: The Interrupt Status bits in register INTSTATx are set independently from the Interrupt Enable in Register INTENx.

INTENx (x = 0-7)
Interrupt Enable Register x **($12C_H$+40_H*x)** **Reset Value: 0000 0000_H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0			SCRI	SDI	WSI	CRCI	NVI	NNI	FDI	FRI	TBI	TDI	RBI	RDI	RSI
r			rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
RSI	0	rw	**Enable Interrupt Request RSI** 0_B No interrupt request can be generated for this source 1_B An interrupt request can be generated for this source
RDI	1	rw	**Enable Interrupt Request RDI** 0_B No interrupt request can be generated for this source 1_B An interrupt request can be generated for this source
RBI	2	rw	**Enable Interrupt Request RBI** 0_B No interrupt request can be generated for this source 1_B An interrupt request can be generated for this source

Field	Bits	Type	Description
TDI	3	rw	**Enable Interrupt Request TDI** 0_B No interrupt request can be generated for this source 1_B An interrupt request can be generated for this source
TBI	4	rw	**Enable Interrupt Request TBI** 0_B No interrupt request can be generated for this source 1_B An interrupt request can be generated for this source
FRI	5	rw	**Enable Interrupt Request FRI** 0_B No interrupt request can be generated for this source 1_B An interrupt request can be generated for this source
FDI	6	rw	**Enable Interrupt Request FDI** 0_B No interrupt request can be generated for this source 1_B An interrupt request can be generated for this source
NNI	7	rw	**Enable Interrupt Request NNI** 0_B No interrupt request can be generated for this source 1_B An interrupt request can be generated for this source
NVI	8	rw	**Enable Interrupt Request NVI** 0_B No interrupt request can be generated for this source 1_B An interrupt request can be generated for this source
CRCI	9	rw	**Enable Interrupt Request CRCI** 0_B No interrupt request can be generated for this source 1_B An interrupt request can be generated for this source

Field	Bits	Type	Description
WSI	10	rw	**Enable Interrupt Request WSI** 0_B No interrupt request can be generated for this source 1_B An interrupt request can be generated for this source
SDI	11	rw	**Enable Interrupt Request SDI** 0_B No interrupt request can be generated for this source 1_B An interrupt request can be generated for this source
SCRI	12	rw	**Enable Interrupt Request SCRI** 0_B No interrupt request can be generated for this source 1_B An interrupt request can be generated for this source
0	[31:13]	r	**Reserved** Read as 0; should be written with 0.

Interrupt Node Pointer Register

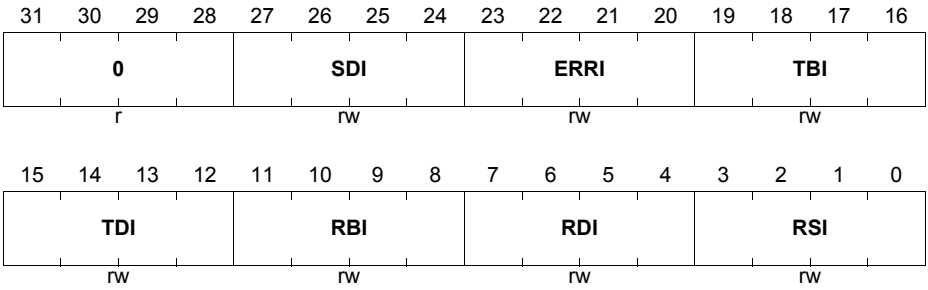
The Interrupt Node Pointer Register INPx contains the node pointers of SENT channel x.

Note: Node Pointer ERRI is one single node pointer for the following error interrupts:

- FRI
- FDI
- NNI
- NVI
- CRCI
- WSI
- SCRI

INPx (x = 0-7)

Interrupt Node Pointer Register x (130_H+40_H*x) **Reset Value: 0000 0000_H**



Field	Bits	Type	Description
RSI	[3:0]	rw	**Interrupt Node Pointer for Interrupt RSI** This bit field defines the interrupt node, that is requested due to the set condition for bit INTSTATx.RSI (if enabled by bit INTENx.RSI). 0000_B Interrupt node 0 is selected 0001_B Interrupt node 1 is selected 0010_B Interrupt node 2 is selected 0011_B Interrupt node 3 is selected 0100_B Trigger Output TRIGO 0 is selected 0101_B Trigger Output TRIGO 1 is selected ... ... 1101_B Trigger Output TRIGO 7 is selected 1110_B reserved ... ... 1111_B reserved

Field	Bits	Type	Description
RDI	[7:4]	rw	**Interrupt Node Pointer for Interrupt RDI** This bit field defines the interrupt node, that is requested due to the set condition for bit INTSTATx.RDI (if enabled by bit INTENx.RDI). For bit field definition, see RSI.
RBI	[11:8]	rw	**Interrupt Node Pointer for Interrupt RBI** This bit field defines the interrupt node, that is requested due to the set condition for bit INTSTATx.RBI (if enabled by bit INTENx.RBI). For bit field definition, see RSI.
TDI	[15:12]	rw	**Interrupt Node Pointer for Interrupt TDI** This bit field defines the interrupt node, that is requested due to the set condition for bit INTSTATx.TDI (if enabled by bit INTENx.TDI). For bit field definition, see RSI.
TBI	[19:16]	rw	**Interrupt Node Pointer for Interrupt TBI** This bit field defines the interrupt node, that is requested due to the set condition for bit INTSTATx.TBI (if enabled by bit INTENx.TBI). For bit field definition, see RSI.
ERRI	[23:20]	rw	**Interrupt Node Pointer for Interrupt FRI, FDI, NNI, NVI, CRCI, WSI, SCRI** This bit field defines the interrupt node, that is requested due to the set condition for bit INTSTATx.FRI (if enabled by bit INTENx.FRI) or INTSTATx.FDI (if enabled by bit INTENx.FDI) or INTSTATx.NNI (if enabled by bit INTENx.NNI) or INTSTATx.NVI (if enabled by bit INTENx.NVI) or INTSTATx.CRCI (if enabled by bit INTENx.CRCI) or INTSTATx.WSI (if enabled by bit INTENx.WSI) or INTSTATx.SCRI (if enabled by bit INTENx.SCRI) For bit field definition, see RSI.
SDI	[27:24]	rw	**Interrupt Node Pointer for Interrupt SDI** This bit field defines the interrupt node, that is requested due to the set condition for bit INTSTATx.SDI (if enabled by bit INTENx.SDI). For bit field definition, see RSI.
0	[31:28]	r	**Reserved** Read as 0; should be written with 0.

25.3 SENT Module Implementation

This section describes the SENT module interface as it is implemented in the TC1798. It especially covers clock control, port and on-chip connections, interrupt control, and address decoding.

25.3.1 Interface Connections of the SENT Module

Figure 25-23 shows the TC1798-specific implementation details and interconnections of the SENT module.

The SENT module is supplied with a separate clock control, address decoding, and interrupt control logic. The 4 modules' service request outputs are connected with interrupt nodes, and each of the 8 channels with the DMA controller. Outputs of the GPTA module are connected to the 8 timer inputs.

The serial data inputs of the receive channels of the SENT module as well as the SPC outputs (SPCn) are connected to GPIO lines. If SPC outputs are used, they are usually mapped to the same port pin like the referring SENT data input line as this minimizes the pin count requirement.

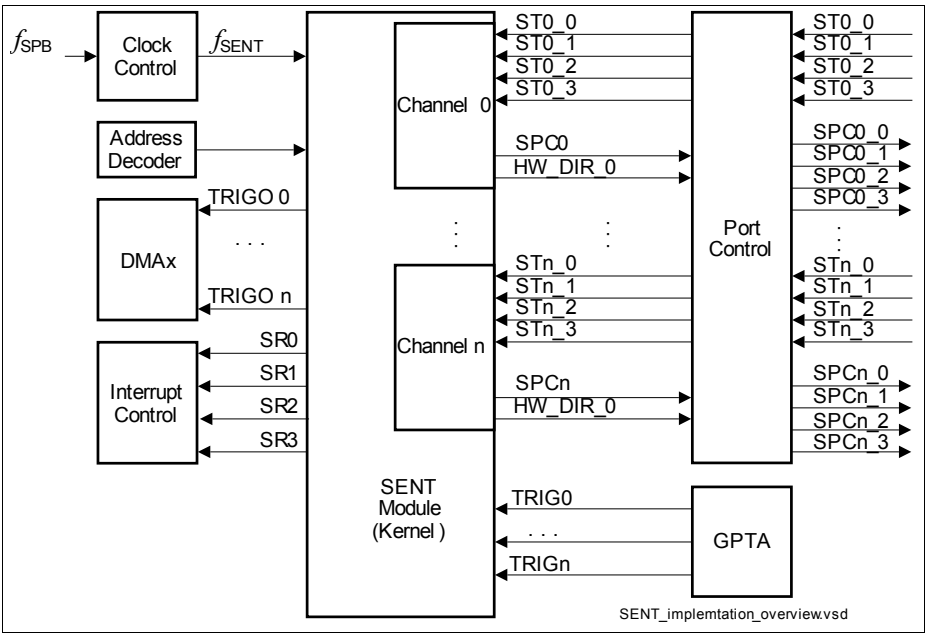


Figure 25-23 SENT Module Implementation and Interconnections

25.3.2 On-Chip Connections

This section describes the on-chip connections of the SENT module.

25.3.2.1 Interrupt and DMA Controller Service Requests

The module has 4 Service Request Nodes connecting it to the interrupt system. The trigger outputs of the SENT module are connected as DMA request input to the DMA controller. The DMA request lines are connected to the DMA controller as shown in Table 25-3.

Table 25-3 Service Request Lines of SENT

INP value	Request Line	Connected to	Description
0000_b	SR0	SENT_SRC0	SENT Service Request Node 0
0001_b	SR1	SENT_SRC1	SENT Service Request Node 1
0010_b	SR2	SENT_SRC2	SENT Service Request Node 2
0011_b	SR3	SENT_SRC3	SENT Service Request Node 3
0100_b	TRIGO0	CH00_REQI02	SDMA Channel 00 Request Input 2
0101_b	TRIGO1	CH01_REQI02	SDMA Channel 01 Request Input 2
0110_b	TRIGO2	CH02_REQI02	SDMA Channel 02 Request Input 2
0111_b	TRIGO3	CH03_REQI02	SDMA Channel 03 Request Input 2
1000_b	TRIGO4	CH04_REQI02	SDMA Channel 04 Request Input 2
1001_b	TRIGO5	CH05_REQI02	SDMA Channel 05 Request Input 2
1010_b	TRIGO6	CH06_REQI02	SDMA Channel 06 Request Input 2
1011_b	TRIGO7	CH07_REQI02	SDMA Channel 07 Request Input 2

25.3.2.2 Trigger Inputs

The module has 8 Sent Channels and the same number of trigger inputs which can be randomly chosen by programming IOCRx.ETS. The trigger inputs (TRIG[7:0]) of the SENT module are connected to the GPTA as shown in **Table 25-4**.

Table 25-4 Trigger Input Lines of SENT

Request Line	Connected to	Description
TRIG0	TRIG0	GPTA Trigger Line TRIG0
TRIG1	TRIG1	GPTA Trigger Line TRIG1
TRIG2	TRIG2	GPTA Trigger Line TRIG2
TRIG3	TRIG3	GPTA Trigger Line TRIG3
TRIG4	TRIG4	GPTA Trigger Line TRIG4
TRIG5	TRIG5	GPTA Trigger Line TRIG5
TRIG6	TRIG6	GPTA Trigger Line TRIG6
TRIG7	TRIG7	GPTA Trigger Line TRIG7

25.3.3 SENT Module-Related External Registers

The registers listed in **Figure 25-24** are not included in the SENT module kernel but must be programmed for proper operation of the SENT module.

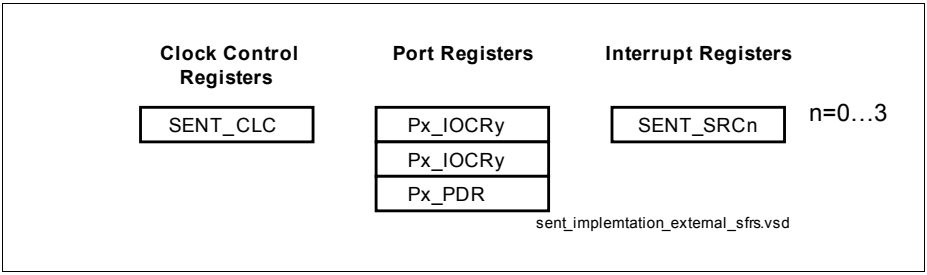


Figure 25-24 SENT Implementation-specific Special Function Registers

25.3.3.1 Port Control

The SENT input channels are overlaid with standard ADC channels as they are replacing former analog signals. Each channel is connected to two ADC channels that can be chosen alternatively. In addition each channel is connected to general purpose I//O lines as well. Each channel is connected to two different general purpose I/O lines that can be chosen alternatively. The selection from on of these 4 alternatives is done by application SW by programming SENT_IOCRx.ALTI respectively.

The SPC output lines are connected to the same I/O ports as the referring input channel. The ADC channels do not provide output functionality. The SPC I/O ports are controlled in the port logic (see also **Figure 25-23**). The following port control operations and selections must be executed for these I/O lines:

- Input/output function selection (Port IOCR registers)
- Pad driver characteristics selection for the outputs (Port PDR registers)

Input/Output Function Selection

SENT can be used in three different ways:

- ADC input (dedicated for ADC) overlaid with SENT digital input and no output option on this pin.
- SENT configured digital I/O lines (open drain, no push/pull, uses SDIR, single pin hardware direction control HW_DIR, SDIR is controlled by the data value: 0 = active out, 1 = passive/open drain, input)
- Standard general purpose input/output function on two lines for each channel (input on ADC alternative 1 or 2, or on I/O port alternative 1 while the output is chosen to be on I/O ports alternative 2.

The SENT module overlays dedicated analog to digital converter (ADC) pins as digital input port.

Note: Note that only the ADC input pins are 5V capable while the standard digital I/O provides 3.3V inputs.

The SENT module can be configured to use input/output ports configured for use with SENT. These control settings for the port pins differ from the standard general purpose I/O lines in so far as

- they are controlled by the SENT module output data via their HW_DIR line
- they are configured to use no push/pull devices and to work in open drain mode if the output function is selected by the HW_DIR line of the port

The SENT module can be configured to use standard (push pull) general purpose I/O lines as well. Different port pins can be selected for input and for output. This allows the use of external transceiver devices.

The port input/output control registers contain the bit fields that select the digital output and input driver characteristics such as port direction (input/output) with alternate output selection, pull-up/down devices, and open-drain selections. The I/O lines for the SENT module are controlled by the Port input/output control registers shown below.

Table 25-5 shows an overview how bits and bit fields must be programmed for the required I/O functionality of the SENT I/O lines.

Table 25-5 SENT I/O Control Selection and Setup

SENT Channel	Port Lines	Input Select Register	Input/Output Control Register Bits	I/O
0	ST0/AN8	SENT_IOCR0.ALTI = 0000_B	P17_PDISC.PDIS0 = 0_B	I
	ST0/AN36	SENT_IOCR0.ALTI = 0001_B	P17_PDISC.PDIS8 = 0_B	I
	ST0/P8.0	SENT_IOCR0.ALTI = 0010_B	P8_IOCR0.PC0 = $0XXX_B$	I
	ST0/P9.9	SENT_IOCR0.ALTI = 0011_B	P9_IOCR8.PC9 = $0XXX_B$	I
	ST0/P9.9	not applicable	P9_IOCR8.PC9 = $1X10_B$	O
1	ST1/AN9	SENT_IOCR1.ALTI = 0000_B	P17_PDISC.PDIS1 = 0_B	I
	ST1/AN37	SENT_IOCR1.ALTI = 0001_B	P17_PDISC.PDIS9 = 0_B	I
	ST1/P8.1	SENT_IOCR1.ALTI = 0010_B	P8_IOCR0.PC1 = $0XXX_B$	I
	ST1/P9.5	SENT_IOCR1.ALTI = 0011_B	P9_IOCR4.PC5 = $0XXX_B$	I
	ST1/P8.1	not applicable	P8_IOCR0.PC1 = $1X11_B$	O

Table 25-5 SENT I/O Control Selection and Setup (cont'd)

SENT Channel	Port Lines	Input Select Register	Input/Output Control Register Bits	I/O
2	ST2/AN10	SENT_IOCR2.ALTI = 0000_B	P17_PDISC.PDIS2 = 0_B	I
	ST2/AN38	SENT_IOCR2.ALTI = 0001_B	P17_PDISC.PDIS10 = 0_B	I
	ST2/P8.2	SENT_IOCR2.ALTI = 0010_B	P8_IOCR0.PC2 = $0XXX_B$	I
	ST2/P9.11	SENT_IOCR2.ALTI = 0011_B	P9_IOCR8.PC11 = $0XXX_B$	I
	ST2/P9.11	not applicable	P9_IOCR8.PC11 = $1X10_B$	O
3	ST3/AN11	SENT_IOCR3.ALTI = 0000_B	P17_PDISC.PDIS3 = 0_B	I
	ST3/AN39	SENT_IOCR3.ALTI = 0001_B	P17_PDISC.PDIS11 = 0_B	I
	ST3/P8.3	SENT_IOCR3.ALTI = 0010_B	P8_IOCR0.PC3 = $0XXX_B$	I
	ST3/P9.6	SENT_IOCR3.ALTI = 0011_B	P9_IOCR4.PC6 = $0XXX_B$	I
	ST3/P9.6	not applicable	P9_IOCR4.PC6 = $1X10_B$	O
4	ST4/AN12	SENT_IOCR4.ALTI = 0000_B	P17_PDISC.PDIS4 = 0_B	I
	ST4/AN40	SENT_IOCR4.ALTI = 0001_B	P17_PDISC.PDIS12 = 0_B	I
	ST4/P8.4	SENT_IOCR4.ALTI = 0010_B	P8_IOCR4.PC4 = $0XXX_B$	I
	ST4/P9.7	SENT_IOCR4.ALTI = 0011_B	P9_IOCR4.PC7 = $0XXX_B$	I
	ST4/P9.7	not applicable	P9_IOCR4.PC7 = $1X10_B$	O
5	ST5/AN13	SENT_IOCR05ALTI = 0000_B	P17_PDISC.PDIS5 = 0_B	I
	ST5/AN41	SENT_IOCR5.ALTI = 0001_B	P17_PDISC.PDIS13 = 0_B	I
	ST5/P8.5	SENT_IOCR5.ALTI = 0010_B	P8_IOCR4.PC5 = $0XXX_B$	I
	ST5/P9.12	SENT_IOCR5.ALTI = 0011_B	P9_IOCR12.PC12 = $0XXX_B$	I
	ST5/P9.12	not applicable	P9_IOCR12.PC12 = $1X10_B$	O
6	ST6/AN14	SENT_IOCR6.ALTI = 0000_B	P17_PDISC.PDIS6 = 0_B	I
	ST6/AN42	SENT_IOCR6.ALTI = 0001_B	P17_PDISC.PDIS14 = 0_B	I
	ST6/P8.6	SENT_IOCR6.ALTI = 0010_B	P8_IOCR4.PC6 = $0XXX_B$	I
	ST6/P9.8	SENT_IOCR6.ALTI = 0011_B	P9_IOCR8.PC8 = $0XXX_B$	I
	ST6/P9.8	not applicable	P9_IOCR8.PC8 = $1X10_B$	O

Table 25-5 SENT I/O Control Selection and Setup (cont'd)

SENT Channel	Port Lines	Input Select Register	Input/Output Control Register Bits	I/O
7	ST7/AN15	SENT_IOCR7.ALTI = 0000_B	P17_PDISC.PDIS7 = 0_B	I
	ST7/AN43	SENT_IOCR7.ALTI = 0001_B	P17_PDISC.PDIS15 = 0_B	I
	ST7/P8.7	SENT_IOCR7.ALTI = 0010_B	P8_IOCR4.PC7 = $0XXX_B$	I
	ST7/P9.10	SENT_IOCR7.ALTI = 0011_B	P9_IOCR8.PC10 = $0XXX_B$	I
	ST7/P9.10	not applicable	P9_IOCR8.PC10 = $1X10_B$	O

25.3.3.2 Service Request Control Registers

The Service Request Control Registers contain the system specific service control bits.

SRC0
Service Request Control 0 Register ($9FC_H$) Reset Value: $0000\ 0000_H$
SRC1
Service Request Control 1 Register ($9F8_H$) Reset Value: $0000\ 0000_H$
SRC2
Service Request Control 2 Register ($9F4_H$) Reset Value: $0000\ 0000_H$
SRC3
Service Request Control 3 Register ($9F0_H$) Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SETR	CLRR	SRR	SRE	0	TOS	0		SRPN							
w	w	rh	rw	r	rw	r		rw							

Field	Bits	Type	Description
SRPN	[7:0]	rw	**Service Request Priority Number** 00_H Service request is never serviced 01_H Service request is on lowest priority ... FF_H Service request is on highest priority
TOS	10	rw	**Type of Service Control** 0_B CPU service is initiated 1_B PCP request is initiated
SRE	12	rw	**Service Request Enable** 0_B Service request is disabled 1_B Service request is enabled
SRR	13	rh	**Service Request Flag** 0_B No service request is pending 1_B A service request is pending

Field	Bits	Type	Description
CLRR	14	w	**Request Clear Bit** CLRR is required to clear SRR. 0_B No action 1_B Clear SRR; bit value is not stored; read always returns 0; no action if SETR is set also.
SETR	15	w	**Request Set Bit** SETR is required to set SRR. 0_B No action 1_B Set SRR; bit value is not stored; read always returns 0; no action if CLRR is set also.
0	[9:8], 11, [31:16]	r	**Reserved** Read as 0; should be written with 0.

25.3.4 SENT Register Address Map

The SENT register map shown in **Figure 25-25**.

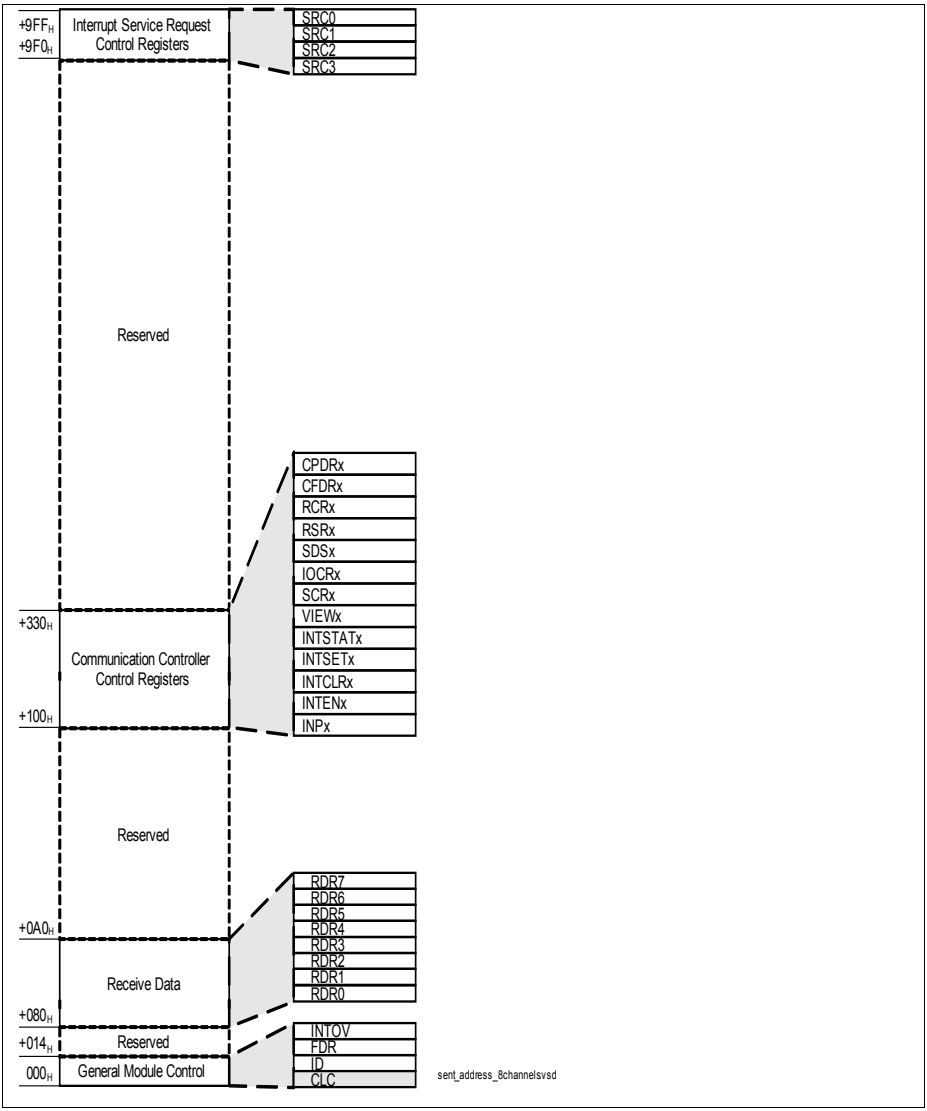


Figure 25-25 SENT Register Map

25.4 Revision History

This User´s Manual is based on: SAE Standard “SENT **Revision J2716 FEB2008 Rev. 3 2009-06-24**”.

Table 25-6 Revision History

Version Number	Changes to Previous Version
Rev_0.1D	First Draft (Bullet Points ++)
Rev_0.2D	Second Draft (Bullet Points ++)
Rev_0.3D	First Review Version
Rev_0.4D	• RCRx.NINT removed as unnecessary FIFO support • Spelling Checked • Renamed INTNP to INP (request DE) • One common error node pointer in INP for FRI, FDI, NNI, NVI, CRCI, WSI, SCRI (reduce DE effort) • Interrupt Node Pointer in INPx increased from 2 bit to 4 bit • Renamed PVAL to PDIV in register CPDRx • RCRx.ASP “Additional Sync/Cal Pulse expected” deleted, not required • RCRx.ACE “Alternate CRC Mode” added, request customer • cleanup Register SCR • ISR0 (Input select register) deleted • AltIn and Filter DEPTH moved to IOCRx • SCRx.DEL moved to SDRx • SCRx deleted, BASE and TRQ moved to SDR • Restructured Chapters (interrupts after functional registers, implementation chapter cleaned up) • Simplified Baud rate generation (Fdtick removed)
Rev_0.5D	• Clean up Glitch filter Chapter • Detailed Baud Rate Generation • Added Address overview table

Table 25-6 Revision History (cont'd)

Version Number	Changes to Previous Version
Rev_0.6D	• Channel **Fractional Divider with variable divider** instead of variable dividend • Glitch filter based on F_pdiv and no longer on F_sent • Glitch detection added • Pre divider = PDIV and no longer PDIV + 1 • Compressed address overview table • Interrupt generation updated **Figure 25-20 "Interrupt Generation" on Page 25-21** • Trigger outputs renamed (RSI and SDI, no more TRIGO) and completed • RDI simplified - now independent from RSI • ETS wording corrected • INTOV now only updated for enabled interrupts (before: any change) • Renamed "SPC Data Register SDR" to "SPC Control Register SCR", it contains both data and control information • TDI wording optimized • External Registers Overview corrected • KSCFG removed
Rev_1.0D	First complete revision (To be done)
Rev_1.1D	• Moved Base Address to F032_1000 - F032_19FF (10x256 bytes) • Serial message ID added. SDSx.SCN moved to [19:16], SDSx.SCRC moved to [15:12], SDSx.MID placed at [11:8]. • RSI and TDI as trigger outputs replaced by 8 Trigger Outputs programmable in the INPs. • implemented first port mapping proposal from product
Rev_1.2	• Added hint to RCR.CEN that FSMs are initialized during enable • Port mapping updated to latest changes of CW08/47

Table 25-6 Revision History (cont'd)

Version Number	Changes to Previous Version
Rev_1.3	• Fixed INTENx Bit descriptions: all bits are rw and high active (typo) • added to feature list: "Programmable Nibble sorting to support LSN or HSN first and relief CPU" (was missing) • SENT_FDR.DM[1:0] added description of all 4 states of this bit field. (same as system level) • IOCR.DEPTH corrected f_{SENT} sent to f_{pdiv} (longer glitch tolerance) • Add Freeze-Disable Bit [10] to SENT_FDR (system requirement) • Pre divider factor is (PDIV + 1) and no longer PDIV (ease design) • Resulting Channel Fractional Divider is (DIV + 1) and no longer DIV • Add IOCR.TXM, RXM and TRM monitor bits (ease of validation) • RDRx added explanation: unused nibbles are shown as '0' (for clarity) • RDI and RSI: Read clears these bits NOT (request from AE) • Renamed Transmit Buffer Overflow to UNDER-Flow with change to respective functionality (data completely transmitted without new write) • RCRx.CFC: Wording improved and details added
Rev_1.4	• Added column Access Modes to Register Table • Updated **Figure 25-2**, **Figure 25-3**, **Figure 25-4** (beautification) • The clock signal f_{pdiv} of a channel must always be at least 20 (old value 10) times the nominal tick frequency, to cater for worst case. • INPx: Added reserved values • Corrected **Figure 25-20**, no more separate DMA TRIGO lines. • RCRx, VIEWx and CFDRx Reset value corrected to 0x0000 0000 hex • Added explanations to RDRx and VIEWx • AI00050230 - SENT_FDR register located at "unusual" address: Moved CLC to offset 0x0Ch for consistency with other modules • Reduced ETS to 3 bit and ALTI to 2 bit width • "Zero Nibble Insertion in CRC" covered. See RCR.CRZ. • UTP AI00050205 - "Extended Serial Frame" covered. Added description of extended serial frame. SDS.SCN moved to RSR.SCN (Allows for an aligned representation of ID and Data as well as a fixed position for SCN) SDS.SD, SDS.MID, SDS.SCRC enlarged (to 16, 8 and 6 bit width) SDS.CON and RCR.ESF added • Resulting Channel Fractional Divider is DIV and no longer (DIV + 1)

Table 25-6 Revision History (cont'd)

Version Number	Changes to Previous Version
Rev_1.5	• Corrected TBIx description on Page 50. • SCR.TRQ corrected (deleted "Reads back zero") • Added hint to definition of Alternate CRC Mode (ACE) • Detailed RBI behavior. It is set if kernel wants to set RSI or RDI and finds RSI or RDI already set. • Detailed that RCR.CEN resets the receiver state machines only while SCR.TRIG resets the sender state machines. • RCR.WSI updated wrt. the special case "extended serial frame" (2009-06-24) • INSTAT.SCRI detailed wrt.: CRC check must include check for correct 0 values in Extended Serial Frame Format (2009-06-24) • Message tick time prolonged to 90 µs according to new standard (2009-06-24) • RCR.CFC (successive calibration pulse detection) adopted to new standard. (2009-06-24) • Updated INTSTAT.FDI wrt.: new additional error diagnostics (total frame length variation and ration calibration pulse/total frame length) in new standard. (2009-06-24)
Rev_1.6	• Added bit RCR.IDE (Ignore Drift Error) to cater for rare triggers by SPC. • Removed SV protection from SENT_FDR. • VIEW.RDNP must be set before reception. • SCR.TRQ spec' ed not active from request to pulse start. • Added "alternative CRC" spec from TLE4998 . • Changed wording for RBI. • New additional error diagnostics (total frame length variation and ration calibration pulse/total frame length) removed.
Rev_1.7	• Added note: RCR.CEN must be cleared before changing CPDR.PDIV or CFDR.DIV. • SCRI typo: frame 8, not 7 contains a zero value. • **Chapter 25.1.5** typo corrected: replaced f_{SENT} with $f_{fracdiv}$ • **Chapter 25.1.3.1** note added on *RCR.CRZ.* • Added hint to Chapter "Module Clock Generation" for details on CLC. • Updated Port connections and Trigger Output connections
Rev_1.8	• Changed functionality of VIEW. • Changed functionality of WSI.

26 FlexRay™ Protocol Controller (E-Ray)

The E-Ray IP-module performs communication according to the FlexRay™ [1] protocol specification v2.1. With maximum specified clock the bitrate can be programmed to values up to 10 Mbit/s. Additional bus driver (BD) hardware is required for connection to the physical layer.

26.1 E-Ray Kernel Description

Figure 26-1 shows a global view of the E-Ray interface.

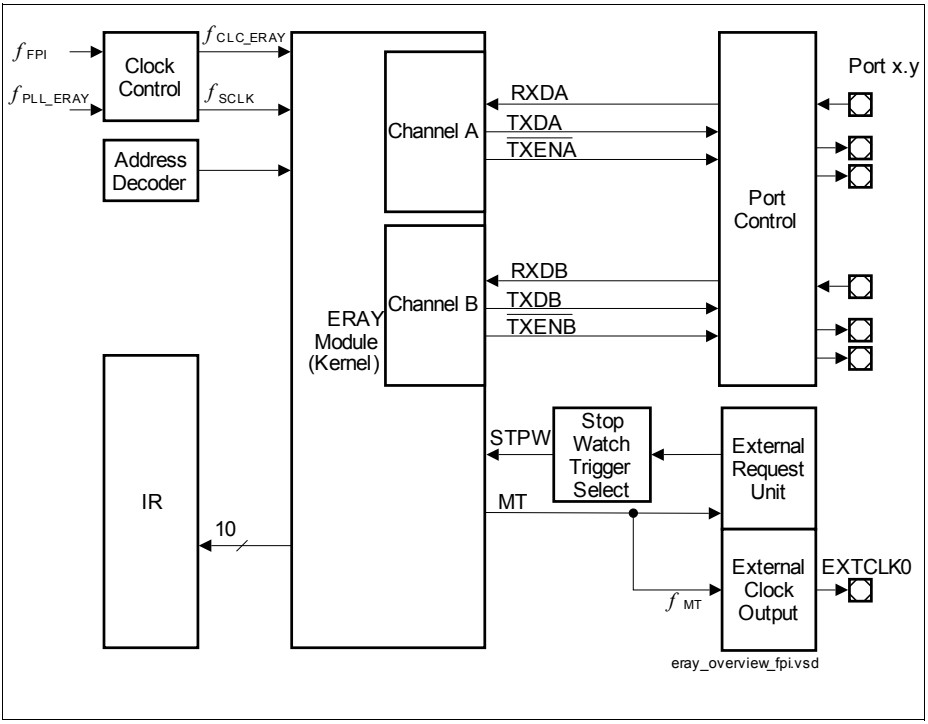


Figure 26-1 General Block Diagram of the E-Ray Interface

The E-Ray module communicates with the external world via three I/O lines each channel. The RXDAx and RXDBx lines are the receive data input signals, TXDA and

1) *Infineon®, Infineon Technologies®, are trademarks of Infineon Technologies AG. FlexRay™* is a trademark of FlexRay Consortium.

TXDB lines are the transmit output signals, $\overline{\text{TXENA}}$ and $\overline{\text{TXENB}}$ the transmit enable signals.

Clock control, address decoding, and service request control are managed outside the E-Ray module kernel.

26.2 Overview

For communication on a FlexRay™ network, individual Message Buffers with up to 254 data byte are configurable. The message storage consists of a single-ported Message RAM that holds up to 128 Message Buffers. All functions concerning the handling of messages are implemented in the Message Handler. Those functions are the acceptance filtering, the transfer of messages between the two FlexRay™ Channel Protocol Controllers and the Message RAM, maintaining the transmission schedule as well as providing message status information.

The register set of the E-Ray IP-module can be accessed directly by an external Host via the module's Host interface. These registers are used to control/configure/monitor the FlexRay™ Channel Protocol Controllers, Message Handler, Global Time Unit, System Universal Control, Frame and Symbol Processing, Network Management, Service Request Control, and to access the Message RAM via Input / Output Buffer.

The E-Ray IP-module supports the following features:

- Conformance with FlexRay™ protocol specification v2.1
- Data rates of up to 10 Mbit/s on each channel
- Up to 128 Message Buffers configurable
- 8 Kbyte of Message RAM for storage of e.g. 128 Message Buffers with max. 48 byte data field or up to 30 Message Buffers with 254 byte Data Sections
- Configuration of Message Buffers with different payload lengths possible
- One configurable receive FIFO
- Each Message Buffer can be configured as receive buffer, as transmit buffer or as part of the receive FIFO
- Host access to Message Buffers via Input and Output Buffer.
  Input Buffer: Holds message to be transferred to the Message RAM
  Output Buffer: Holds message read from the Message RAM
- Filtering for slot counter, cycle counter, and channel
- Maskable module service requests
- Network Management supported
- Four service request lines
- Automatic delayed read access to Output Command Request Register (OBCR) if a data transfer from Message RAM to Output Shadow Buffer (initiated by a previous write access to the OBCR) is ongoing.
- Automatic delayed read access to Input Command Request Register (IBCR) if a data transfer from Input Shadow Buffer to Message RAM to (initiated by a previous write access to the IBCR) is ongoing.

- Four Input Buffer for building up transmission Frames in parallel.
- Flag indicating which Input Buffer is currently accessible by the host.

26.3 Definitions

FlexRay™ Frame: Header Segment + Payload Segment

Message Buffer: Header Section + Data Section

Message RAM: Header Partition + Data Partition

Data Frame: FlexRay™ Frame that is not a NULL Frame

26.4 Block Diagram

The E-Ray is built up by the following main submodules:

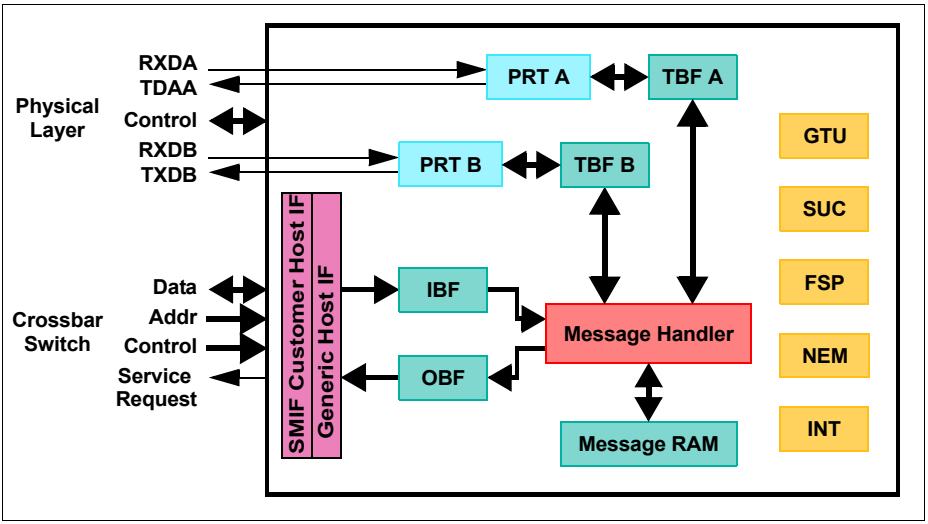


Figure 26-2 E-Ray Block Diagram

Customer Host Interface (CIF)

Connects the FPI Bus to the E-Ray IP-module via the Generic Host Interface.

Generic Host Interface (GIF)

The E-Ray IP-module is provided with an 8/16/32-bit Generic Host Interface prepared for the connection to a wide range of customer-specific Hosts. Configuration registers, status registers, and service request registers are attached to the respective blocks and can be accessed via the Generic Host Interface.

Input Buffer (IBF)

For write access to the Message Buffers configured in the Message RAM, the Host can write the Header and Data Section for a specific Message Buffer to the Input Buffer. The Message Handler then transfers the data from the Input Buffer to the selected Message Buffer in the Message RAM.

Because the Input Buffer (IBF) Scheme does only allow to write the entire Message Frame, not only parts of it, the number of IBF has been increased from originally 2 to 4. This enables to fill the buffer partly and at the end request transfer into Message RAM. Therefore 2 extra bits allow to switch between the two banks of IBF and one status bit signals the IBF currently active for Host writes.

Output Buffer (OBF)

For read access to a Message Buffer configured in the Message RAM the Message Handler transfers the selected Message Buffer to the Output Buffer. After the transfer has completed, the Host can read the Header and Data Section of the transferred Message Buffer from the Output Buffer.

Message Handler (MHD)

The E-Ray Message Handler controls data transfers between the following components:

- Input / Output Buffer and Message RAM
- Transient Buffer RAMs of the two FlexRay™ Protocol Controllers and Message RAM

Message RAM (MRAM)

The Message RAM consists of a single-ported RAM that stores up to 128 FlexRay™ Message Buffers together with the related configuration data (Header and Data Partition).

Transient Buffer RAM (TBF 1/2)

Stores the Data Section of two complete messages.

FlexRay™ Channel Protocol Controller (PRT A/B)

The FlexRay™ Channel Protocol Controllers consist of shift register and FlexRay™ protocol FSM. They are connected to the Transient Buffer RAMs for intermediate message storage and to the physical layer via bus driver BD.

They perform the following functionality:

- Control and check of bit timing
- Reception and transmission of FlexRay™ Frames and symbols
- Check of Header CRC
- Generation / check of Frame CRC

- Interfacing to bus driver

The FlexRay™ Channel Protocol Controllers have interfaces to:

- Physical Layer (bus driver)
- Transient Buffer RAM
- Message Handler
- Global Time Unit
- System Universal Control
- Frame and Symbol Processing
- Network Management
- Service Request Control

Global Time Unit (GTU)

The Global Time Unit performs the following functions:

- Generation of Microtick
- Generation of Macrotick
- Fault tolerant clock synchronization by FTM algorithm
  - Rate correction
  - Offset correction
- Cycle counter
- Timing control of static segment
- Timing control of dynamic segment (minislotting)
- Support of external clock correction

System Universal Control (SUC)

The System Universal Control controls the following functions:

- Configuration
- Wakeup
- Startup
- Normal Operation
- Passive Operation
- Monitor Mode

Frame and Symbol Processing (FSP)

The Frame and Symbol Processing controls the following functions:

- Checks the correct timing of Frames and symbols
- Tests the syntactical and semantical correctness of received Frames
- Sets the slot status flags

Network Management (NEM)

Handles of the Network Management vector

Service Request Control (INT)

The Service Request Controller performs the following functions:

- Provides error and status service request flags
- Enables and disables service request sources
- Assignment of service request sources to one of the two module service request lines
- Enables and disables module service request lines
- Manages the two service request timers
- Stop watch time capturing

26.5 Programmer's Model

The programmer's model of the E-Ray module follows the principle of memory mapped peripheral. Some portion of the memory follows the principle of segmented/paged memory organization.

26.5.1 Register Map

The E-Ray module allocates an address space of 4 Kbyte (000_H to $FFFF_H$). The registers are organized as 32-bit registers. 8/16-bit accesses are also supported. Host access to the Message RAM is done via the Input and Output Buffers. They buffer data to be transferred to and from the Message RAM under control of the Message Handler, avoiding conflicts between Host accesses and message reception / transmission. Addresses 0004_H - $000F_H$,$03C8_H$ - $03EC_H$ and 0800_H - $0FFF_H$ are reserved for customer specific purposes. All functions related to these addresses are located in the Customer Host Interface. The test registers located on address 0010_H and 0014_H are writable only under the conditions described in **"Special Registers" on Page 26-23**.

The assignment of the Message Buffers is done according to the scheme shown in **Table 26-1** below. The number N of available Message Buffers depends on the payload length of the configured Message Buffers. The maximum number of Message Buffers is 128. The maximum payload length supported is 254 byte.

The Message Buffers are separated into three consecutive groups:

- Static Buffers: Transmit / Receive Buffers assigned to static segment
- Static and Dynamic Buffers: Transmit / Receive Buffers assigned to static or dynamic segment
- FIFO- Receive FIFO

The Message Buffer separation configuration can be changed only in "DEFAULT_CONFIG" or "CONFIG" state only by programming the Message RAM Configuration register (MRC).

The first group starts with Message Buffer 0 and consists of static Message Buffers only. Message Buffer 0 is dedicated to hold the startup / SYNC Frame or the single slot Frame, if node transmit one, as configured by SUCC1.TXST, SUCC1.TXSY, and SUCC1.TSM

in the SUC Configuration Register 1 (SUCC1). In addition, Message Buffer 1 may be used for SYNC Frame transmission in case that SYNC Frames or single-slot Frames should have different payloads on the two channels. In this case bit MRC.SPLM has to be programmed to 1 and Message Buffers 0 and 1 have to be configured with the key slot ID and can be (re)configured in “DEFAULT_CONFIG” or “CONFIG” state only.

The second group consists of Message Buffers assigned to the static or to the dynamic segment. Message Buffers belonging to this group may be reconfigured during run time from dynamic to static or vice versa depending on the state of MRC.SEC.

The Message Buffers belonging to the third group are concatenated to a single receive FIFO.

Table 26-1 Assignment of Message Buffers

Message Buffer 0	⇓ Static Buffers	
Message Buffer 1		
…		
	⇓ Static + Dynamic Buffers	⇐ **FDB**
	⇓ FIFO	⇐ **FFB**
Message Buffer N-1		
Message Buffer N		⇐ **LCB**

26.5.2 E-Ray Kernel Registers

This chapter describes all registers of the E-Ray kernel.

Table 26-2 Registers Address Space E-Ray Kernel Register Address Space

Module	Base Address	End Address	Note
ERAY	$F0010000_H$	$F0010FFF_H$	4Kbyte

Table 26-3 Registers OverviewE-Ray Kernel Registers

Register Short Name	Register Long Name	Offset Addr.[1)]	Access Mode		Reset Class	Description see
			Read	Write		
Customer Registers						
ERAY_CLC	E-Ray Clock Control Register	0000_H	SV,U	SV,E	3	Page 26-268
CUST1	Busy and Input Buffer Control Register	0004_H	SV,U	SV,U	3	Page 26-17
ID	Module Identification Register	0008_H	SV,U	SV,U	3	Page 26-16
CUST3	Customer Interface Timeout Counter	$000C_H$	SV,U	SV,U	3	Page 26-20
Special Registers						
TEST1	Test Register 1	0010_H	SV,U	SV,U	3	Page 26-23
TEST2	Test Register 2	0014_H	SV,U	SV,U	3	Page 26-28
-	Reserved	0018_H	nBE	nBE	-	-
LCK	Lock Register	$001C_H$	SV,U	SV,U	3	Page 26-39
Service Request Registers						
EIR	Error Service Request Register	0020_H	SV,U	SV,U	3	Page 26-41
SIR	Status Service Request Register	0024_H	SV,U	SV,U	3	Page 26-47
EILS	Error Service Request Line Select	0028_H	SV,U	SV,U	3	Page 26-52
SILS	Status Service Request Line Select	$002C_H$	SV,U	SV,U	3	Page 26-56

Table 26-3 Registers OverviewE-Ray Kernel Registers (cont'd)

Register Short Name	Register Long Name	Offset Addr.[1)]	Access Mode		Reset Class	Description see
			Read	Write		
EIES	Error Service Request Enable Set	0030_H	SV,U	SV,U	3	Page 26-60
EIER	Error Service Request Enable Reset	0034_H	SV,U	SV,U	3	Page 26-65
SIES	Status Service Request Enable Set	0038_H	SV,U	SV,U	3	Page 26-70
SIER	Status Service Request Enable Reset	$003C_H$	SV,U	SV,U	3	Page 26-75
ILE	Service Request Line Enable	0040_H	SV,U	SV,U	3	Page 26-80
T0C	Timer 0 Configuration	0044_H	SV,U	SV,U	3	Page 26-81
T1C	Timer 1 Configuration	0048_H	SV,U	SV,U	3	Page 26-83
STPW1	Stop Watch Register 1	$004C_H$	SV,U	SV,U	3	Page 26-85
STPW2	Stop Watch Register 2	0050_H	SV,U	SV,U	3	Page 26-87
-	Reserved	0054_H - $007C_H$	nBE	nBE	-	-
Communication Controller Control Registers						
SUCC1	SUC Configuration Register 1	0080_H	SV,U	SV,U	3	Page 26-88
SUCC2	SUC Configuration Register 2	0084_H	SV,U	SV,U	3	Page 26-96
SUCC3	SUC Configuration Register 3	0088_H	SV,U	SV,U	3	Page 26-97
NEMC	NEM Configuration Register	$008C_H$	SV,U	SV,U	3	Page 26-98
PRTC1	PRT Configuration Register 1	0090_H	SV,U	SV,U	3	Page 26-99
PRTC2	PRT Configuration Register 2	0094_H	SV,U	SV,U	3	Page 26-101
MHDC	MHD Configuration Register	0098_H	SV,U	SV,U	3	Page 26-102
-	Reserved	$009C_H$	nBE	nBE	-	-

Table 26-3 Registers OverviewE-Ray Kernel Registers (cont'd)

Register Short Name	Register Long Name	Offset Addr.[1)]	Access Mode		Reset Class	Description see
			Read	Write		
GTUC01	GTU Configuration Register 1	$00A0_H$	SV,U	SV,U		Page 26-103
GTUC02	GTU Configuration Register 2	$00A4_H$	SV,U	SV,U	3	Page 26-104
GTUC03	GTU Configuration Register 3	$00A8_H$	SV,U	SV,U	3	Page 26-105
GTUC04	GTU Configuration Register 4	$00AC_H$	SV,U	SV,U	3	Page 26-106
GTUC05	GTU Configuration Register 5	$00B0_H$	SV,U	SV,U	3	Page 26-107
GTUC06	GTU Configuration Register 6	$00B4_H$	SV,U	SV,U	3	Page 26-108
GTUC07	GTU Configuration Register 7	$00B8_H$	SV,U	SV,U	3	Page 26-109
GTUC08	GTU Configuration Register 8	$00BC_H$	SV,U	SV,U	3	Page 26-110
GTUC09	GTU Configuration Register 9	$00C0_H$	SV,U	SV,U	3	Page 26-111
GTUC10	GTU Configuration Register 10	$00C4_H$	SV,U	SV,U	3	Page 26-112
GTUC11	GTU Configuration Register 11	$00C8_H$	SV,U	SV,U	3	Page 26-113
-	Reserved	$00CC_H$ - $00FC_H$	nBE	nBE	-	-
Communication Controller Status Registers						
CCSV	Communication Controller Status Vector	0100_H	SV,U	nBE	3	Page 26-115
CCEV	Communication Controller Error Vector	0104_H	SV,U	nBE	3	Page 26-120
-	Reserved	0108_H	nBE	nBE	-	-
-	Reserved	$010C_H$	nBE	nBE	-	-
SCV	Slot Counter Value	0110_H	SV,U	nBE	3	Page 26-121

Table 26-3 Registers OverviewE-Ray Kernel Registers (cont'd)

Register Short Name	Register Long Name	Offset Addr.[1)]	Access Mode		Reset Class	Description see
			Read	Write		
MTCCV	Macrotick and Cycle Counter Value	0114_H	SV,U	nBE	3	Page 26-122
RCV	Rate Correction Value	0118_H	SV,U	nBE	3	Page 26-123
OCV	Offset Correction Value	$011C_H$	SV,U	nBE	3	Page 26-124
SFS	SYNC Frame Status	0120_H	SV,U	nBE	3	Page 26-125
SWNIT	Symbol Window and Network Idle Time Status	0124_H	SV,U	nBE	3	Page 26-127
ACS	Aggregated Channel Status	0128_H	SV,U	SV,U	3	Page 26-130
-	Reserved	$012C_H$	nBE	nBE	-	-
ESIDnn	Even Sync ID Symbol Window nn	0130_H - 0168_H	SV,U	nBE	3	Page 26-133
-	Reserved	$016C_H$	SV,U	nBE	-	-
OSIDnn	Odd Sync ID Symbol Window nn	0170_H - $01A8_H$	SV,U	nBE	3	Page 26-135
-	Reserved	$01AC_H$	SV,U	nBE	-	-
NMVx	Network Management Vector [1…3]	$01B0_H$ - $01B8_H$	SV,U	nBE	3	Page 26-137
-	Reserved	$01BC_H$ - $02FC_H$	nBE	nBE	-	-
Message Buffer Control Registers						
MRC	Message RAM Configuration	0300_H	SV,U	SV,U	3	Page 26-138
FRF	FIFO Rejection Filter	0304_H	SV,U	SV,U	3	Page 26-141
FRFM	FIFO Rejection Filter Mask	0308_H	SV,U	SV,U	3	Page 26-143
FCL	FIFO Critical Level	$030C_H$	SV,U	SV,U	3	Page 26-144
Message Buffer Status Registers						
MHDS	Message Handler Status	0310_H	SV,U	SV,U	3	Page 26-145
LDTS	Last Dynamic Transmit Slot	0314_H	SV,U	SV,U	3	Page 26-148

Table 26-3 Registers OverviewE-Ray Kernel Registers (cont'd)

Register Short Name	Register Long Name	Offset Addr.[1]	Access Mode		Reset Class	Description see
			Read	Write		
FSR	FIFO Status Register	0318_H	SV,U	SV,U	3	Page 26-149
MHDF	Message Handler Constraints Flags	$031C_H$	SV,U	nBE	3	Page 26-151
TXRQ1	Transmission Request Register 1	0320_H	SV,U	nBE	3	Page 26-154
TXRQ2	Transmission Request Register 2	0324_H	SV,U	nBE	3	Page 26-155
TXRQ3	Transmission Request Register 3	0328_H	SV,U	nBE	3	Page 26-156
TXRQ4	Transmission Request Register 4	$032C_H$	SV,U	nBE	3	Page 26-157
NDAT1	New Data Register 1	0330_H	SV,U	nBE	3	Page 26-158
NDAT2	New Data Register 2	0334_H	SV,U	nBE	3	Page 26-159
NDAT3	New Data Register 3	0338_H	SV,U	nBE	3	Page 26-160
NDAT4	New Data Register 4	$033C_H$	SV,U	nBE	3	Page 26-161
MBSC1	Message Buffer Status Changed 1	0340_H	SV,U	nBE	3	Page 26-162
MBSC2	Message Buffer Status Changed 2	0344_H	SV,U	nBE	3	Page 26-163
MBSC3	Message Buffer Status Changed 3	0348_H	SV,U	nBE	3	Page 26-164
MBSC4	Message Buffer Status Changed 4	$034C_H$	SV,U	nBE	3	Page 26-165
-	Reserved	0350_H - $03A4_H$	nBE	nBE	-	-
NDIC1	New Data Interrupt Control 1	$03A8_H$	SV,U	SV,U	3	Page 26-270
NDIC2	New Data Interrupt Control 2	$03AC_H$	SV,U	SV,U	3	Page 26-271
NDIC3	New Data Interrupt Control 3	$03B0_H$	SV,U	SV,U	3	Page 26-272

Table 26-3 Registers OverviewE-Ray Kernel Registers (cont'd)

Register Short Name	Register Long Name	Offset Addr.[1)]	Access Mode		Reset Class	Description see
			Read	Write		
NDIC4	New Data Interrupt Control 4	$03B4_H$	SV,U	SV,U	3	Page 26-273
MSIC1	Message Buffer Status Changed Interrupt Control 1	$03B8_H$	SV,U	SV,U	3	Page 26-274
MSIC2	Message Buffer Status Changed Interrupt Control 2	$03BC_H$	SV,U	SV,U	3	Page 26-275
MSIC3	Message Buffer Status Changed Interrupt Control 3	$03C0_H$	SV,U	SV,U	3	Page 26-276
MSIC4	Message Buffer Status Changed Interrupt Control 4	$03C4_H$	SV,U	SV,U	3	Page 26-273
IBUSYSRC	Input Buffer Busy Service Request Control Register	$03C8_H$	SV,U	SV,U	3	Page 26-279
OBUSYSRC	Output Buffer Busy Service Request Control Register	$03CC_H$	SV,U	SV,U	3	Page 26-279
MBSC1SRC	Message Buffer Status Changed 1 Service Request Control Register	$03D0_H$	SV,U	SV,U	3	Page 26-279
MBSC0SRC	Message Buffer Status Changed 0 Service Request Control Register	$03D4_H$	SV,U	SV,U	3	Page 26-279
NDAT1SRC	New Data 1 Service Request Control Register	$03D8_H$	SV,U	SV,U	3	Page 26-279
NDAT0SRC	New Data 0 Service Request Control Register	$03DC_H$	SV,U	SV,U	3	Page 26-279
TINT1SRC	Timer Interrupt 1 Service Request Control Register	$03E0_H$	SV,U	SV,U	3	Page 26-279
TINT0SRC	Timer Interrupt 0 Service Request Control Register	$03E4_H$	SV,U	SV,U	3	Page 26-279

Table 26-3 Registers OverviewE-Ray Kernel Registers (cont'd)

Register Short Name	Register Long Name	Offset Addr.[1)]	Access Mode		Reset Class	Description see
			Read	Write		
INT1SRC	Interrupt 1 Service Request Control Register	$03E8_H$	SV,U	SV,U	3	Page 26-279
INT0SRC	Interrupt 0 Service Request Control Register	$03EC_H$	SV,U	SV,U	3	Page 26-279
Identification Registers						
CREL	Core Release Registers	$03F0_H$	SV,U	nBE	3	Page 26-166
ENDN	Endian Register	$03F4_H$	SV,U	nBE	3	Page 26-168
-	Reserved	$03F6_H$ - $03FC_H$	nBE	nBE	-	-
Input Buffer						
WRDSn	Write Data Section [1…64]	0400_H - $04FC_H$	SV,U	SV,U	3	Page 26-169
WRHS1	Write Header Section 1	0500_H	SV,U	SV,U	3	Page 26-170
WRHS2	Write Header Section 2	0504_H	SV,U	SV,U	3	Page 26-173
WRHS3	Write Header Section 3	0508_H	SV,U	SV,U	3	Page 26-174
	Reserved	$050C_H$	nBE	nBE	-	
IBCM	Input Buffer Command Mask	0510_H	SV,U	SV,U	3	Page 26-175
IBCR	Input Buffer Command Request	0514_H	SV,U	SV,U	3	Page 26-177
	Reserved	0518_H - $05FC_H$	nBE	nBE	-	
Output Buffer						
RDDSn	Read Data Section [1…64]	0600_H - $06FC_H$	SV,U	nBE	3	Page 26-179
RDHS1	Read Header Section 1	0700_H	SV,U	nBE	3	Page 26-180
RDHS2	Read Header Section 2	0704_H	SV,U	nBE	3	Page 26-182
RDHS3	Read Header Section 3	0708_H	SV,U	nBE	3	Page 26-184
MBS	Message Buffer Status	$070C_H$	SV,U	nBE	3	Page 26-186
OBCM	Output Buffer Command Mask	0710_H	SV,U	SV,U	3	Page 26-191

Table 26-3 Registers OverviewE-Ray Kernel Registers (cont'd)

Register Short Name	Register Long Name	Offset Addr.[1]	Access Mode		Reset Class	Description see
			Read	Write		
OBCR	Output Buffer Command Request	0714_H	SV,U	SV,U	3	Page 26-194
	Reserved	0718_H -	nBE	nBE	-	-
ECC Control						
SECCON	Single Bit Error Correction Control	0800_H	SV,U	SV,E	3	Page 26-31
SEDCON	Single Bit Error Detection Control	0804_H	SV,U	SV,E	3	Page 26-33
DEDCON	Double Bit Error Correction Control	0808_H	SV,U	SV,E	3	Page 26-35
ECCR	ECC Data Read	$080C_H$	SV,U	SV,U	3	Page 26-37
ECCW	ECC Data Write	0810_H	SV,U	SV,U	3	Page 26-38
	Reserved	0814_H -	nBE	nBE	-	-

1) The absolute register address is calculated as follows:
Module Base Address + Offset Address (shown in this column)

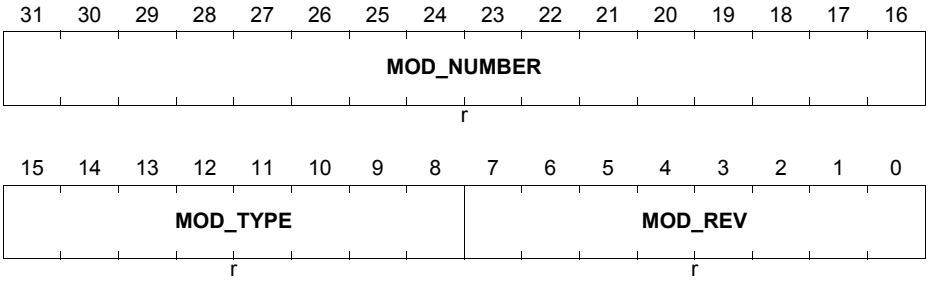
26.5.2.1 Customer Registers

The addresses 0004_H - $000F_H$,$03C8_H$ - $03EC_H$ and 0800_H - $0FFF_H$ are reserved for customer-specific registers.

Module Identification Register (ID)

This register contains bit fields identifying the E-Ray module in Infineons Module portfolio and is read only.

ID
Module Identification Register (0008_H) Reset Value: 0044 C0XX$_H$



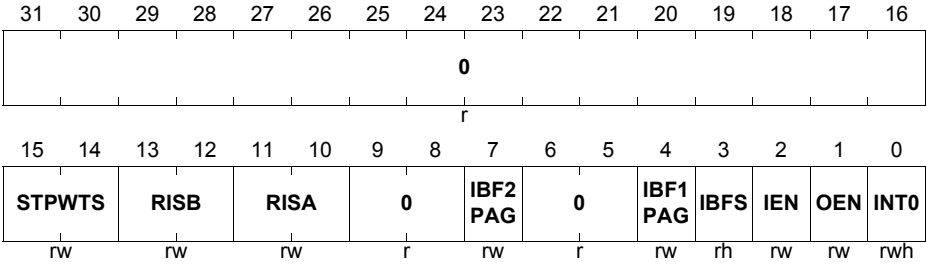
Field	Bits	Type	Description
MOD_REV	[7:0]	r	**Module Revision Number** MOD_REV defines the module revision number. The value of a module revision starts with 01_H (first revision).
MOD_TYPE	[15:8]	r	**Module Type** The value of this bit field is $C0_H$. It defines the module as a 32-bit module.
MOD_NUMBER	[31:16]	r	**Module Number Value** This bit field defines a module identification number. For the E-Ray module the module identification number is 44_H.

Busy Control Register (CUST1)

The Busy Control Register enables the automatic delay scheme. Furthermore it signals a time-out service request for the automatic delay scheme.

CUST1
Busy and Input Buffer Control Register

(0004_H) **Reset Value: $0000\ 0000_H$**



Field	Bits	Type	Description
INT0	0	rwh	**CIF Timeout Service Request Status** INT0 will be set if a timeout has occurred during the auto delay scheme and must be reset by writing zero to INT0. *Note: In case hardware sets INT0 and at the same point of time software clears INT0, INT0 is cleared.*
OEN	1	rw	**Enable auto delay scheme for Output Buffer Control Register (OBCR)** This control bit controls the delay scheme for Output Buffer Control Register (OBCR) read accesses. 0_B Disable auto delay scheme for Output Buffer Control Register (OBCR) 1_B Enable auto delay scheme for Output Buffer Control Register (OBCR)
IEN	2	rw	**Enable auto delay scheme for Input Buffer Control Register (IBCR)** This control bit controls the auto delay scheme for Input Buffer Control Register (IBCR) read accesses. 0_B Disable auto delay scheme for Input Buffer Control Register (IBCR) 1_B Enable auto delay scheme for Input Buffer Control Register (IBCR)

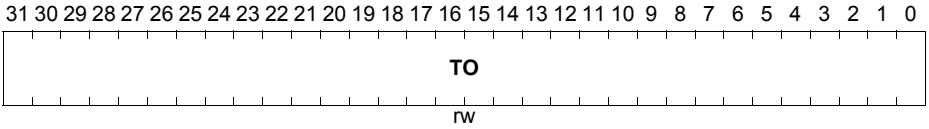
Field	Bits	Type	Description
IBFS	3	rh	**Input Buffer Status Register** This status bit indicates which of the two Input Buffer RAMs (IBF) is accessible by the host (via CIF) as Input Buffer. The other non accessible buffer RAM is currently used as shadow buffer RAM by the ERAY message handler and therefore not accessible by the host. 0_B Input Buffer RAM 2 (IBF2) is accessible as Input Buffer by the host (CIF) 1_B Input Buffer RAM 1 (IBF1) is accessible as Input Buffer by the host (CIF)
IBF1PAG	4	rw	**Input Buffer 1 Page Select Register** This control bit selects if the upper page or lower page of Input Buffer 1 (IBF1) currently active. Read: 0_B Lower Page (256 Bytes) of Input Buffer RAM 1 selected 1_B Upper Page (256 Bytes) of Input Buffer RAM 1 selected Write: 0_B Select Lower Page (256 Bytes) of Input Buffer RAM 1 1_B Select Upper Page (256 Bytes) of Input Buffer RAM 1 *Note: Write is only possible, if Input Buffer RAM 1 is currently accessible by the host (via CIF) and therefore IBFS set.*
IBF2PAG	7	rw	**Input Buffer 2 Page Select Register** This control bit selects if the upper page or lower page of Input Buffer 2 (IBF2) currently active. Read: 0_B Lower Page (256 Bytes) of Input Buffer RAM 2 selected 1_B Upper Page (256 Bytes) of Input Buffer RAM 2 selected Write: 0_B Select Lower Page (256 Bytes) of Input Buffer RAM 2 1_B Select Upper Page (256 Byte) of Input Buffer RAM 2 *Note: Write is only possible, if Input Buffer RAM 2 is currently accessible by the host (via CIF) and therefore IBFS cleared.*

Field	Bits	Type	Description
RISA	[11:10]	rw	**Receive Input Select Channel A** 00_B Channel A receiver input RXDA0 selected 01_B Channel A receiver input RXDA1 selected 10_B Channel A receiver input RXDA2 selected 11_B Channel A receiver input RXDA3 selected
RISB	[13:12]	rw	**Receive Input Select Channel B** 00_B Channel B receiver input RXDB0 selected 01_B Channel B receiver input RXDB1 selected 10_B Channel B receiver input RXDB2 selected 11_B Channel B receiver input RXDB3 selected
STPWTS	[15:14]	rw	**Stop Watch Trigger Input Select** 00_B Stop Watch Trigger input STPWT0 selected 01_B Stop Watch Trigger input STPWT1 selected 10_B Stop Watch Trigger input STPWT2 selected 11_B Stop Watch Trigger input STPWT3 selected
0	[6:5], [9:8], [31:16]	r	**Reserved** Returns 0 if read; should be written with 0.

Customer Interface Time-out Counter Register (CUST3)

The Time-out Counter Register is realizing the time-out counter reload (startup) value for the automatic delay scheme (not the time-out down counter itself).

CUST3
Customer Interface Timeout Counter ($000C_H$) **Reset Value: $0000\ 0000_H$**



Field	Bits	Type	Description
TO	[31:0]	rw	**CIF Timeout Reload Value** The 32-bit down counter reload (start-up) value must be setup for the automatic delay scheme.

Automatic Delayed Write Access to OBCR and IBCR

Write and read accesses to the Output Buffer Control Register (OBCR) can be automatically stalled due to a ongoing transfer from the Message Buffer to the Output Buffer. Also write and read accesses to the Input Buffer Control Register (IBCR) may be automatically delayed due to a ongoing transfer from the Input Buffer to the Message Buffer.

This delay scheme can be controlled (enabled or disabled) by CUST1.IEN and CUST1.OEN. The maximum time to stall a write or read access is determined by a single time-out counter preluded with the 32-bit value specified in the bit field CUST3.TO. If the time-out counter counts down to zero before the transfer to/from the Message Buffer is completed, the access (read or write) will be canceled and a service request will be generated. A canceled read access provides a 0 value. A canceled write access does not modify any bits in the OBCR or IBCR. In addition the bit CUST1.INT0 of the service request status register will be set and must be reset by the host to disable the service request line.

The read and write access to the Output Buffer Control Register (OBCR) may be configured without automatic delay by clearing CUST1.OEN. Setting OBCR.REQ and immediately afterwards reading or writing OBCR, e.g. to set OBCR.VIEW will lead to a canceled read or write operation, e.g. OBCR.VIEW remains cleared, and an error is signalled by a set EIR.IOBA. Besides canceling the erroneous read or write operation, and setting the error bit, no further state change happens. So full operation is granted. OBCR remains read and write inaccessible until the transfer of data from the Message Buffer to the Output Buffer (MBF⇒OBF) is completed. During this time span all read and

write accesses to the Output Buffer Control Register (OBCR) are canceled. The transfer is completed when OBCR.OBSYS is cleared. Additionally signal TOBC may be used, e.g. for service request triggering, DMA triggering, or driving a pin, to communicate the access status.

The read and write access to the Output Buffer Control Register (OBCR) may be configured to be automatic delayed by setting CUST1.OEN and configuring CUST3.TO to the maximum stall time acceptable to the system. If setting OBCR.REQ and immediately afterwards reading or writing to OBCR, e.g. to set the OBCR.VIEW bit, this read or write will be stalled until either the maximum delay time elapsed (in this case the read or write operation is cancelled after the stall time, e.g. OBCR.VIEW remains cleared, and an error is signalled by setting EIR.IOBA) or the read or write completes normally, e.g. set OBCR.VIEW after the transfer of data from the Message Buffer to the Output Buffer (MBF⇒OBF) is finalized. During this time the bus is locked and no further access to the E-Ray module is possible due to the ongoing stalled read or write operation. Because no access is possible to the E-Ray module, read or write stall may only be detected through the signal TOBC or due to other not processed read or write accesses to the E-Ray module.

The read and write access to the Input Buffer Control Register (IBCR) may also be configured without automatic delay by clearing CUST1.IEN. By writing to IBCR.IBRH the Input Buffers are swapped (shadow IBF changes to host IBF and host IBF to shadow IBF), the content of the shadow IBF is copied into the MBF (IBF⇒MBF), and IBCR.IBSYS is set. Writing to IBCR.IBRH a second time while IBCR.IBSYS remained set (previously initiated copy process IBF⇒MBF ongoing) will correctly update IBCR.IBRH and set IBCR.IBSYH. This will set the signal IBUSY. A third access, read or write, to IBCR while IBCR.IBSYH remains set will cancel this third access and an error is signalled by setting EIR.IIBA. Besides canceling this last access to IBCR and setting the error bit, no further state change happens. So full operation is granted. IBCR remains read and write inaccessible until the transfer of data from the Input Shadow Buffer to the Message Buffer (IBF⇒MBF) is completed and once more the Input Buffers are swapped (shadow IBF changes to host IBF and host IBF to shadow IBF). During this time span all read and write accesses to the Input Buffer Control Register (IBCR) are canceled. The transfer is completed when IBCR.IBSYH is cleared. Additionally signal TIBC may be used, e.g. for service request triggering, DMA triggering, or driving a pin, to communicate the access status.

The read and write access to the Input Buffer Control Register (IBCR) may be configured for being automatically delayed by setting CUST1.IEN and configuring CUST3.TO to the maximum stall time acceptable to the system. By writing to IBCR.IBRH the Input Buffers are swapped (shadow IBF changes to host IBF and host IBF to shadow IBF), the content of the shadow IBF copied into the MBF, and IBCR.IBSYS is set. Writing to IBCR.IBRH a second time while IBCR.IBSYS remains set (previously initiated copy process ongoing) will correctly update IBCR.IBRH and set IBCR.IBSYH. A third access to IBCR while IBCR.IBSYH remains set will stall this read or write until either the maximum delay

time elapsed (in this case the read or write operation is cancelled after the stall time and an error is signalled by setting EIR.IOBA) or the read or write completes normally, after the transfer of data from the Input Shadow Buffer to the Message Buffer (IBF⇒MBF) is finalized and once more the Input Buffers are swapped (shadow IBF changes to host IBF and host IBF to shadow IBF). During this time the bus is locked and no further access to E-Ray module is possible due to the ongoing stalled read or write operation. Because no access is possible to the E-Ray module, read or write stall may only be detected through the signal TIBC or due to other not processed read or write accesses to the E-Ray module.

So setting CUST3.TO = $FFFFFFFF_H$, CUST1.IEN = 1, and CUST1.OEN = 1 will always grant a consistent data access of the host to the Output and Input Buffers without the need of reading and taking into account the status of OBCR.OBSYS or IBCR.IBSYH. But this simplified access may cause system latencies and system performance loss.

26.5.2.2 Special Registers

Test Register 1 (TEST1)

The Test Register 1 holds the control bits to configure the test modes of the E-Ray module. Write access to these bits is only possible if bit TEST1.WRTEN is set.

The Test Register 1 bits therefore can be used to test the interface to the physical layer (connectivity test) by driving / reading the respective pins.

When the E-Ray IP is operated in one of its test modes that requires TEST1.WRTEN to be set (RAM Test Mode, I/O Test Mode, Asynchronous Transmit Mode, and Loop Back Mode) only the selected test mode functionality is available.

The test functions are not available in addition to the normal operational mode functions, they change the functions of parts of the E-Ray module. Therefore normal operation as specified outside this chapter and as required by the FlexRay™ protocol specification and the FlexRay™ conformance test is not possible. Test mode functions may not be combined with each other or with FlexRay™ protocol functions.

The test mode features are intended for hardware testing or for FlexRay™ bus analyzer tools. They are not intended to be used in FlexRay™ applications

TEST1
Test Register 1 **(0010_H)** **Reset Value: $0000\ 0300_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CERB				CERA				0		TXENB	TXENA	TXB	TXA	RXB	RXA
rh				rh				r		rwh	rwh	rwh	rwh	rh	rh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0						AOB	AOA	0		TMC		0		ELBE	WRTEN
r						rh	rh	r		rw		r		rw	rw

Field	Bits	Type	Description
WRTEN	0	rw	**Write Test Register Enable** Enables write access to the test registers. To set the bit from 0 to 1 the test mode key has to be written as defined on **"Lock Register (LCK)" on Page 26-39**. The unlock sequence is not required when TEST1.WRTEN is kept at 1 while other bits of the register are changed. The bit can be reset to 0 at any time. 0_B Write access to test registers disabled. 1_B Write access to test registers enabled.

Field	Bits	Type	Description
ELBE	1	rw	**External Loop Back Enable** There are two possibilities to perform a loop back test. External loop back via physical layer or internal loop back for in-system self-test (default). In case of an internal loop back pins TXENA and TXENB are in their inactive state, pins TXDA and TXDB are set to HIGH, pins RXDA and RXDB are not evaluated. Bit ELBE is evaluated only when POC is in loop back mode and test multiplexer control is in non multiplexed mode TMC = 00. 0_B Internal loop back (default) 1_B External loop back
TMC	[5:4]	rw	**Test Multiplexer Control** 00_B Normal signal path (default). 01_B RAM Test Mode: Internal busses are multiplexed to make all RAM blocks of the E-Ray module directly accessible by the Host. This mode is intended to enable testing of the embedded RAM blocks during production testing. 10_B I/O Test Mode: Output pins are driven to the values defined by bits TXA, TXB, TXENA, TXENB. The values applied to the input pins can be read from register bits RXA and RXB. 11_B Reserved; should not be used.
AOA	8	rh	**Activity on A** The channel idle condition is specified in the FlexRay™ protocol spec v2.1, chapter 3, BITSTRB process (zChannelIdle). 0_B No activity detected, channel A idle 1_B Activity detected, channel A not idle
AOB	9	rh	**Activity on B** The channel idle condition is specified in the FlexRay™ protocol spec v2.1, chapter 3, BITSTRB process (zChannelIdle). 0_B No activity detected, channel B idle 1_B Activity detected, channel B not idle
RXA	16	rh	**Read Channel A Receive Pin** 0_B RXDA = 0 1_B RXDA = 1

Field	Bits	Type	Description
RXB	17	rh	**Read Channel B Receive Pin** 0_B RXDB = 0 1_B RXDB = 1
TXA	18	rwh	**Read or Write to Channel A Transmit Pin** 0_B TXDA = 0 1_B TXDA = 1
TXB	19	rwh	**Read or Write to Channel B Transmit Pin** 0_B TXDB = 0 1_B TXDB = 1
TXENA	20	rwh	**Read or Write to Channel A Transmit Enable Pin** 0_B $\overline{\text{TXENA}}$= 0 1_B $\overline{\text{TXENA}}$= 1
TXENB	21	rwh	**Read or Write to Channel B Transmit Enable Pin** 0_B $\overline{\text{TXENB}}$ = 0 1_B $\overline{\text{TXENB}}$= 1
CERA	[27:24]	rh	**Coding Error Report Channel A**[1)] Set when a coding error is detected on channel A. Reset to zero when register TEST1 is read or written. Once the CERA is set it will remain unchanged until the Host accesses the TEST1 register. 0000_B No coding error detected 0001_B Header CRC error detected 0010_B Frame CRC error detected 0011_B Frame Start Sequence FSS too long 0100_B First bit of Byte Start Sequence BSS seen LOW 0101_B Second bit of Byte Start Sequence BSS seen HIGH 0110_B First bit of Frame End Sequence FES seen HIGH 0111_B Second bit of Frame End Sequence FES seen LOW 1000_B CAS / MTS symbol seen too short 1001_B CAS / MTS symbol seen too long Other combinations are reserved.

Field	Bits	Type	Description
CERB	[31:28]	rh	**Coding Error Report Channel B**[1)] Set when a coding error is detected on channel B. Reset to zero when register TEST1 is read or written. Once the CERB is set it will remain unchanged until the Host accesses the TEST1 register. 0000_B No coding error detected 0001_B Header CRC error detected 0010_B Frame CRC error detected 0011_B Frame Start Sequence FSS too long 0100_B First bit of Byte Start Sequence BSS seen LOW 0101_B Second bit of Byte Start Sequence BSS seen HIGH 0110_B First bit of Frame End Sequence FES seen HIGH 0111_B Second bit of Frame End Sequence FES seen LOW 1000_B CAS / MTS symbol seen too short 1001_B CAS / MTS symbol seen too long Other combinations are reserved.
0	[3:2], [7:6], [15:10], [23:22]	r	**Reserved** Returns 0 if read; should be written with 0.

1) Coding errors are also signalled when the Communication Controller is in “MONITOR_MODE”. The error codes regarding CAS / MTS symbols concern only the monitored bit pattern, irrelevant whether those bit patterns are seen in the symbol window or elsewhere.

Asynchronous Transmit Mode (ATM)

The asynchronous transmit mode is entered by writing 1110_B to the CHI Command Vector SUCC1.CMD in the SUC Configuration Register 1 (CHI command: ATM) while the Communication Controller is in “CONFIG” state and bit TEST1.WRTEN in the Test Register 1 is set. This write operation has to be directly preceded by two consecutive write accesses to the Configuration Lock Key (unlock sequence). When called in any other state or when bit TEST1.WRTEN is not set, SUCC1.CMD will be reset to 0000_B = “COMMAND_NOT_ACCEPTED”. CCSV.POCS in the Communication Controller Status Vector will return 1110_B while the E-Ray module is in ATM mode. Asynchronous Transmit mode can be left by writing 0001_B (CHI command: “CONFIG”) to the CHI Command Vector SUCC1.CMD in the SUC Configuration Register 1.

In ATM mode transmission of a FlexRay™ Frame is triggered by writing the number of the respective Message Buffer to the Input Buffer Command Request register (IBCR.IBRH) while bit IBCM.STXRS in the Input Buffer Command Mask register is set to 1. In this mode wake-up, startup, and clock synchronization are bypassed. The CHI command SEND_MTS results in the immediate transmission of an MTS symbol.

The cycle counter value of Frames send in ATM mode can be programmed via MTCCV.CCV (writable in ATM and loop back mode only).

Loop Back Mode

The loop back mode is entered by writing 1111_B to the CHI Command Vector SUCC1.CMD in the SUC Configuration Register 1 (CHI command: LOOP_BACK) while the Communication Controller is in “CONFIG” state and bit TEST1.WRTEN in the Test Register 1 is set. This write operation has to be directly preceded by two consecutive write accesses to the Configuration Lock Key (unlock sequence). When called in any other state or when bit TEST1.WRTEN is not set, SUCC1.CMD will be reset to 0000_B = “COMMAND_NOT_ACCEPTED”. CCSV.POCS in the Communication Controller Status Vector will show $0000\ 1101_H$ while the E-Ray module is in loop back mode.

Loop Back mode can be left by writing 0001_B (CHI command: “CONFIG”) to the CHI Command Vector SUCC1.CMD in the SUC Configuration Register 1.

The loop back test mode is intended to check the module’s internal data paths. Normal, time triggered operation is not possible in loop back mode.

There are two possibilities to perform a loop back test. External loop back via physical layer (TEST1.ELBE = 1) or internal loop back for in-system self-test (TEST1.ELBE = 0). In case of an internal loop back pins $\overline{\text{TXENA}}$, $\overline{\text{TXENB}}$ are in their inactive state, pins TXDA and TXDB are set to HIGH, pins RXDAn and RXDBn are not evaluated.

When the Communication Controller is in loop back mode, a loop back test is started by the Host writing a message to the Input Buffer and requesting the transmission by writing to the Input Buffer Command Request register IBCR. The Message Handler will transfer the message into the Message RAM and then into the Transient Buffer of the selected channel. The Channel Protocol Controller (PRT) will read (in 32-bit words) the message from the transmit part of the Transient Buffer and load it into its Rx / Tx shift register. The serial transmission is looped back into the shift register; its content is written into the receive part of the channels’s Transient Buffer before the next word is loaded.

The PRT and the Message Handler will then treat this transmitted message like a received message, perform an acceptance filtering on Frame ID and receive channel, and store the message into the Message RAM if it passed acceptance filtering. The loop back test ends with the Host requesting this received message from the Message RAM and then checking the contents of the Output Buffer.

Each FlexRay™ channel is tested separately. The E-Ray cannot receive messages from the FlexRay™ bus while it is in the loop back mode.

The cycle counter value of Frames used in loop back mode can be programmed via MTCCV.CCV (writable in ATM and loop back mode only).

Note that in case of an odd payload the last two bytes of the looped-back payload will be shifted by 16 bits to the right inside the last 32-bit data word.

Test Register 2 (TEST2)

The Test Register 2 holds all bits required for the RAM test of the seven embedded RAM blocks of the E-Ray module. Write access to this register is only possible when TEST1.WRTEN in the Test Register 1 is set to 1.

TEST2
Test Register 2 **(0014_H)** **Reset Value: $0000\ 0000_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	WR ECC	0							SSEL			0	RS		
r	rw	r							rw			r	rw		

Field	Bits	Type	Description
RS	[2:0]	rw	**RAM Select** In RAM Test mode the RAM blocks selected by RS are mapped to module address $0000\ 0400_H$ to $0000\ 07FF_H$ (1024 byte addresses). 000_B Input Buffer RAM 1 (IBF1) 001_B Input Buffer RAM 2 (IBF2) 010_B Output Buffer RAM 1 (OBF1) 011_B Output Buffer RAM 2 (OBF2) 100_B Transient Buffer RAM A (TBF1) 101_B Transient Buffer RAM B (TBF2) 110_B Message RAM (MBF) 111_B Reserved; should not be used.

Field	Bits	Type	Description
SSEL	[6:4]	rw	**Segment Select** To enable access to the complete Message RAM (8192 byte addresses) the Message RAM is segmented. 000_B access to RAM byte 0000_H to $03FF_H$ enabled 001_B access to RAM byte 0400_H to $07FF_H$ enabled 010_B access to RAM byte 0800_H to $0BFF_H$ enabled 011_B access to RAM byte $0C00_H$ to $0FFF_H$ enabled 100_B access to RAM byte 1000_H to $11FF_H$ enabled 101_B access to RAM byte 1400_H to $17FF_H$ enabled 110_B access to RAM byte 1800_H to $1BFF_H$ enabled 111_B access to RAM byte $1C00_H$ to $1FFF_H$ enabled
WR ECC	14	rw	**Write ECC Data Enable** Content of ECCW is transferred to the RAM: 0_B disabled 1_B enabled *Note: Test mode must be entered. See* ***"Test Register 1 (TEST1)" on Page 26-23***
0	3, [13:7], 15, [31:16]	r	**Reserved** Returns 0 if read; should be written with 0.

RAM Test Mode

In RAM test mode (TEST1.TMC = 1), one of the seven RAM blocks can be selected for direct RD/WR access by programming TEST2.RS.

For external access the selected RAM block is mapped to address space 400_H to $7FF_H$ (1024 byte addresses or 256 word addresses).

Because the length of the Message RAM exceeds the available address space, the Message RAM is segmented into segments of 1024 byte. The segments can be selected by programming TEST2.SSEL in the Test Register 2.

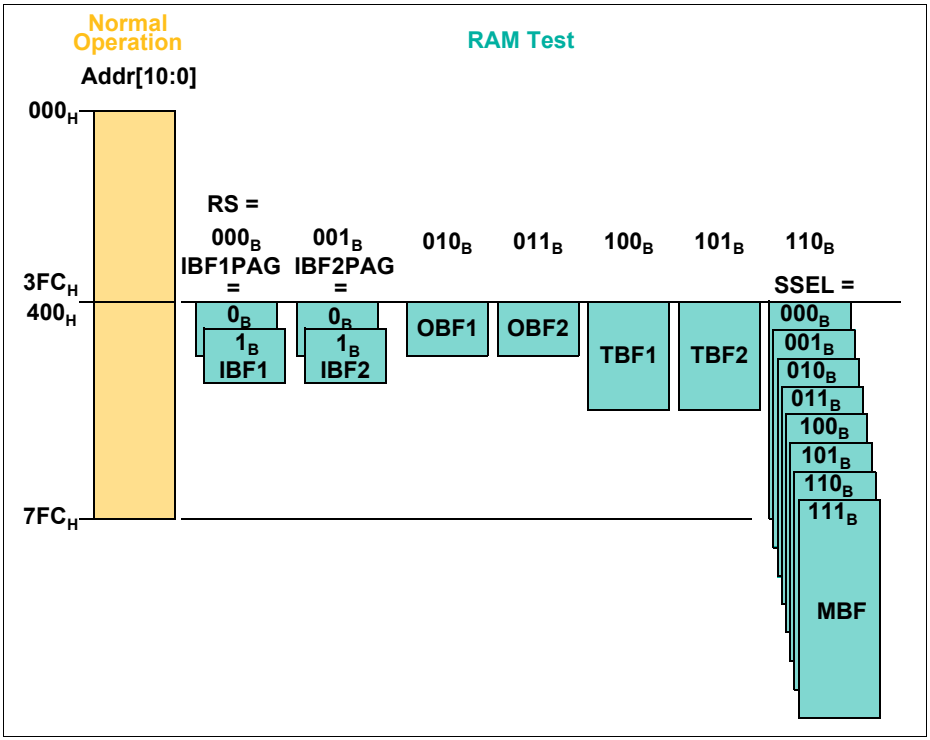


Figure 26-3 RAM test mode Access to E-Ray RAM Blocks

SECCON

The Single Bit Error Correction Control Register holds the bits required for enabling the single bit error correction for each respective RAM block of the E-Ray module. It can only be written if PRDCFG2.SENAV is set. In TC1798 this PRDCFG2 bit is reset by SSW from a parameter stored in the config sector. Thus the user has not access to turn on/off single error correction. In TC1798 the SEC bits are tied to “enabled”. It is supervisor and endinit protected.

SECCON
SEC Control **(0800_H)** **Reset Value: 0000 007F_H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0									SEC I2 EN	SEC I1 EN	SEC O2 EN	SEC O1 EN	SEC T2 EN	SEC T1 EN	SEC M EN
r									rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
SEC M EN	0	rw	**Single Bit Error Correction for Message Buffer (MBF) RAM Enable/Test Disable** 0_B OFF 1_B ON
SEC T1 EN	1	rw	**Single Bit Error Correction for Transfer Buffer 1 (TBF1) RAMs Enable/Test Disable** 0_B OFF 1_B ON
SEC T2 EN	2	rw	**Single Bit Error Correction for Transfer Buffer 2 (TBF2) RAMs Enable/Test Disable** 0_B OFF 1_B ON
SEC O1 EN	3	rw	**Single Bit Error Correction for Output Buffer 1 (OBF1) RAM Enable/Test Disable** 0_B OFF 1_B ON

Field	Bits	Type	Description
SECO2EN	4	rw	**Single Bit Error Correction for Output Buffer 2(OBF2) RAM Enable/Test Disable** 0_B OFF 1_B ON
SECI1EN	5	rw	**Single Bit Error Correction for Input Buffer 1 (IBF1) RAM Enable/Test Disable** 0_B OFF 1_B ON
SECI2EN	6	rw	**Single Bit Error Correction for Input Buffer 2 (IBF2) RAM Enable/Test Disable** 0_B OFF 1_B ON
0	[31:7]	r	**Reserved** Returns 0 if read; should be written with 0.

SEDCON

The Single Bit Error Detection Control Register holds the bits required for enabling the single bit error detection for each respective RAM block of the E-Ray module. It can only be written if PRDCFG2.SENAV is set. In TC1798 this PRDCFG2 bit is reset by SSW from a parameter stored in the config sector. Thus the user has not access to turn on/off single error detection. In TC1798 the SED bits are tied to “disabled”. The Register is supervisor and endinit protected.

SEDCON
SED Control **(0804_H)** **Reset Value: 0000 007F_H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0									SEDI2EN	SEDI1EN	SEDO2EN	SEDO1EN	SEDT2EN	SEDT1EN	SEDMEN
r									rw	rw	rw	rw	rw	rw	rw

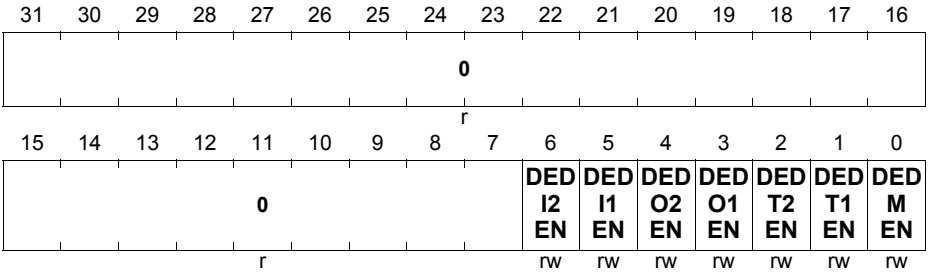
Field	Bits	Type	Description
SEDMEN	0	rw	**Single Bit Error Detection for Message Buffer (MBF) RAM Enable/Test Disable** 0_B OFF 1_B ON
SEDT1EN	1	rw	**Single Bit Error Detection for Transfer Buffer 1 (TBF1) RAMs Enable/Test Disable** 0_B OFF 1_B ON
SEDT2EN	2	rw	**Single Bit Error Detection for Transfer Buffer 2 (TBF2) RAMs Enable/Test Disable** 0_B OFF 1_B ON
SEDO1EN	3	rw	**Single Bit Error Detection for Output Buffer 1 (OBF1) RAM Enable/Test Disable** 0_B OFF 1_B ON

Field	Bits	Type	Description
SEDO2EN	4	rw	**Single Bit Error Detection for Output Buffer 2(OBF2) RAM Enable/Test Disable** 0_B OFF 1_B ON
SEDI1EN	5	rw	**Single Bit Error Detection for Input Buffer 1 (IBF1) RAM Enable/Test Disable** 0_B OFF 1_B ON
SEDI2EN	6	rw	**Single Bit Error Detection for Input Buffer 2 (IBF2) RAM Enable/Test Disable** 0_B OFF 1_B ON
0	[31:7]	r	**Reserved** Returns 0 if read; should be written with 0.

DEDCON

The Double Bit Error Detection Control Register holds the bits required for enabling the double bit error detection for each respective RAM block of the E-Ray module.

DEDCON
DED Control **(0808_H)** **Reset Value: 0000 007F$_H$**



Field	Bits	Type	Description
DEDMEN	0	rw	**Double Bit Error Detection for Message Buffer (MBF) RAM Enable/Test Disable** 0_B OFF 1_B ON
DEDT1EN	1	rw	**Double Bit Error Detection for Transfer Buffer 1 (TBF1) RAMs Enable/Test Disable** 0_B OFF 1_B ON
DEDT2EN	2	rw	**Double Bit Error Detection for Transfer Buffer 2 (TBF2) RAMs Enable/Test Disable** 0_B OFF 1_B ON
DEDO1EN	3	rw	**Double Bit Error Detection for Output Buffer 1 (OBF1) RAM Enable/Test Disable** 0_B OFF 1_B ON
DEDO2EN	4	rw	**Double Bit Error Detection for Output Buffer 2(OBF2) RAM Enable/Test Disable** 0_B OFF 1_B ON

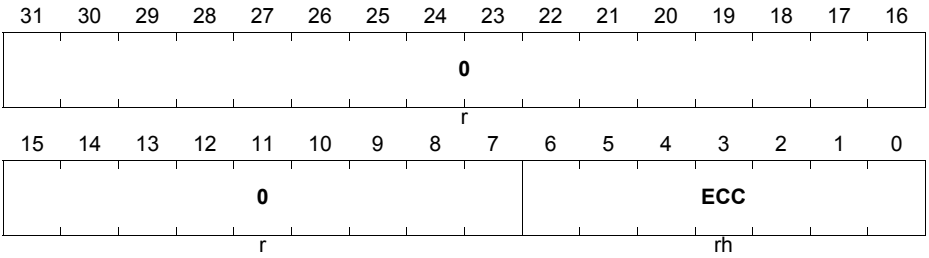
Field	Bits	Type	Description
DEDI1EN	5	rw	**Double Bit Error Detection for Input Buffer 1 (IBF1) RAM Enable/Test Disable** 0_B OFF 1_B ON
DEDI2EN	6	rw	**Double Bit Error Detection for Input Buffer 2 (IBF2) RAM Enable/Test Disable** 0_B OFF 1_B ON
0	[31:7]	r	**Reserved** Returns 0 if read; should be written with 0.

ECCR

The ECC Data Read Register always holds the ECC bits referring to the last accessed RAM address. In normal operation RAM can not be accessed by the CPU. For dedicated RAM access to selected addresses by the CPU, Test mode must be entered. See **“Test Register 2 (TEST2)” on Page 26-28**

ECCR

ECC Data Read Register **(080C$_H$)** **Reset Value: 0000 0000$_H$**



Field	Bits	Type	Description
ECC	[6:0]	rh	**Error Correction Data of the last accessed RAM address**
0	[31:7]	r	**Reserved** Returns 0 if read; should be written with 0.

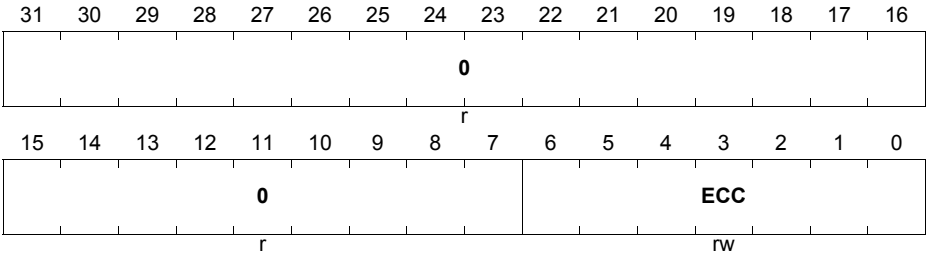
ECCW

The ECC Data Write Register holds the ECC bits to be written together with the next RAM access. These bits are written to the ECC bit field referring to the RAM address accessed next. In normal operation E-Ray RAM can not be accessed by the CPU. The content of ECCW is not transferred to the RAM ECC data field in normal operation. For ECCW to become effective (and for dedicated RAM access to selected addresses by the CPU), Test mode must be entered. See **"Test Register 1 (TEST1)" on Page 26-23**. The referring RAM must be selected. See **"Test Register 2 (TEST2)" on Page 26-28**.

Note: Content of ECCW is transferred to the RAM only if TEST2.WRECC is set!

ECCW

ECC Data Write Register (0810$_H$) Reset Value: 0000 0000$_H$

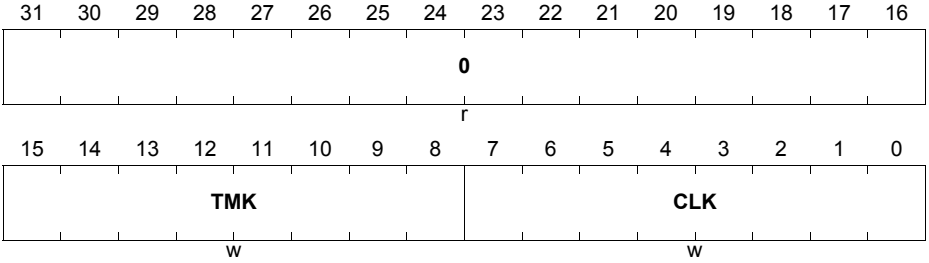


Field	Bits	Type	Description
ECC	[6:0]	rw	**Error Correction Data written with next RAM address written next**
0	[31:7]	r	**Reserved** Returns 0 if read; should be written with 0.

Lock Register (LCK)

The Lock Register is write-only. Reading the register will return 0000 0000_H.

LCK
Lock Register **($001C_H$)** **Reset Value: $0000\ 0000_H$**



Field	Bits	Type	Description
CLK	[7:0]	w	**Configuration Lock Key** To leave “CONFIG” state by writing to SUCC1.CMD commands READY, MONITOR_MODE, ATM, LOOP_BACK) in the SUC Configuration Register 1, the write operation has to be directly preceded by two consecutive write accesses to the Configuration Lock Key (unlock sequence). If the write sequence below is interrupted by other write accesses between the second write to the Configuration Lock Key and the write access to the SUCC1 register, the Communication Controller remains in “CONFIG” state and the sequence has to be repeated. First write: LCK.CLK = CE_H = $1100\ 1110_B$ Second write: LCK.CLK = 31_H = $0011\ 0001_B$ Third write: SUCC1.CMD Returns 0 if read

Field	Bits	Type	Description
TMK	[15:8]	w	**Test Mode Key** To set bit TEST1.WRTEN the write operation has to be directly preceded by two consecutive write accesses to the Test Mode Key. If the write sequence is interrupted by other write accesses between the second write to the Test Mode Key and the write access to the Test1 register, bit TEST1.WRTEN is not set to 1 and the sequence has to be repeated. First write: LCK.TMK = 75_H = 0111 0101_B Second write: LCK.TMK = $8A_H$ = 1000 1010_B Second write: TEST1.WRTEN = 1 Returns 0 if read
0	[31:16]	r	**Reserved** Returns 0 if read; should be written with 0.

Note: In case the Host uses 8/16-bit accesses to write the listed bit fields, the programmer has to ensure that no "dummy accesses" e.g. to the remaining register bytes / words are inserted by the compiler.

To exit "CONFIG" state by writing to SUCC1.CMD in the SUC Configuration Register 1, the write operation has to be directly preceded by two consecutive write accesses to the Configuration Lock Key. If this write sequence is service requested by read accesses or write accesses to other locations, the Communication Controller remains in "CONFIG" state and the sequence has to be repeated.

First write: LCK.CLK = CE_H = 1100 1110_B

Second write: LCK.CLK = 31_H = 0011 0001_B

26.5.2.3 Service Request Registers

The address space from 0020_H to $007F_H$ is reserved for service request registers.

Error Service Request Select (EIR)

The flags are set when the Communication Controller detects one of the listed error conditions. They remain set until the Host clears them. A flag is cleared by writing a 1 to the corresponding bit position. Writing a 0 has no effect on the flag. An application reset will also clear the register.

EIR
Error Service Request Register (0020_H) Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0					TABB	LTVB	EDB	0					TABA	LTVA	EDA
r					rwh	rwh	rwh	r					rwh	rwh	rwh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0				MHF	IOBA	IIBA	EFA	RFO	EERR	CCL	CCF	SFO	SFBM	CNA	PEMC
r				rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh

Field	Bits	Type	Description
PEMC	0	rwh	**POC Error Mode Changed** This flag is set whenever the error mode signalled by CCEV.ERRM in the Communication Controller Error Vector register has changed. 0_B Error mode has not changed 1_B Error mode has changed This flag is cleared by writing a 1.
CNA	1	rwh	**Command Not Accepted** The flag signals that the write access to the CHI command vector SUCC1.CMD in the SUC Configuration Register 1 was not successful because the requested command was not valid in the actual POC state, or because the CHI command was locked (CCL = 1). 0_B CHI command accepted 1_B CHI command not accepted This flag is cleared by writing a 1.

Field	Bits	Type	Description
SFBM	2	rwh	**SYNC Frames Below Minimum** This flag signals that the number of SYNC Frames received during the last communication cycle was below the limit required by the FlexRay™ protocol. May be set during startup and therefore should be cleared by the Host after the Communication Controller entered “NORMAL_ACTIVE” state. 0_B Sync node: 1 or more SYNC Frames received Non-sync node: 2 or more SYNC Frames received 1_B Less than the required minimum of SYNC Frames received This flag is cleared by writing a 1.
SFO	3	rwh	**SYNC Frame Overflow** Set when either the number of SYNC Frames received during the last communication cycle or the total number of SYNC Frames received during the last double cycle exceeds the maximum number of SYNC Frames as defined by GTUC02.SNM in the GTU Configuration Register 2. 0_B Number of received SYNC Frames ≤ GTUC02.SNM 1_B More SYNC Frames received than configured by GTUC02.SNM This flag is cleared by writing a 1.
CCF	4	rwh	**Clock Correction Failure** This flag is set at the end of the cycle whenever one of the following errors occurred: • Missing offset and / or rate correction • Clock Correction limit reached The clock correction status is monitored in registers CCEV and SFS. A failure may occur during startup, therefore bit CCF should be cleared by the Host after the Communication Controller entered “NORMAL_ACTIVE” state. 0_B Clock correction successful so far 1_B Clock correction failed This flag is cleared by writing a 1.

Field	Bits	Type	Description
CCL	5	rwh	**CHI Command Locked** The flag signals that the write access to the CHI command vector SUCC1.CMD was not successful because the execution of the previous CHI command has not yet completed. In this case bit EIR.CNA is also set to 1. 0_B CHI command accepted 1_B CHI command not accepted This flag is cleared by writing a 1.
EERR	6	rh	**ECC Error** The flag signals an ECC error to the Host. It is set whenever one of the flags MHDS.EIBF, MHDS.EOBF, MHDS.EMR, MHDS.ETBF1, MHDS.ETBF2 changes from 0 to 1. See also **“Message Handler Status (MHDS)” on Page 26-145**. 0_B No error detected 1_B Error detected
RFO	7	rh	**Receive FIFO Overrun** The flag is set by the Communication Controller when a receive FIFO overrun is detected. When a receive FIFO overrun occurs, the oldest message is overwritten with the actual received message. The actual state of the FIFO is monitored in register FSR. 0_B No receive FIFO overrun detected 1_B A receive FIFO overrun has been detected
EFA	8	rwh	**Empty FIFO Access** This flag is set by the Communication Controller when the Host requests the transfer of a message from the receive FIFO via Output Buffer while the receive FIFO is empty. 0_B No Host access to empty FIFO occurred 1_B Host access to empty FIFO occurred

Field	Bits	Type	Description
IIBA	9	rwh	**Illegal Input Buffer Access** This flag is set by the Communication Controller when the Host wants to modify a Message Buffer via Input Buffer while the Communication Controller is not in “CONFIG” or “DEFAULT_CONFIG” state and one of the following conditions applies: 1. The Host writes to the Input Buffer Command Request register to modify the: a) Header Section of Message Buffer 0, 1 if configured for transmission in key slot b) Header Section of static Message Buffers with buffer number < MRC.FDB while MRC.SEC = 01_B c) Header Section of any static or dynamic Message Buffer while MRC.SEC = $1x_B$ d) Header and / or Data Section of any message buffer belonging to the receive FIFO 2. The Host writes to any register of the Input Buffer while IBCR.IBSYS is set. 0_B No illegal Host access to Input Buffer occurred 1_B Illegal Host access to Input Buffer occurred
IOBA	10	rwh	**Illegal Output Buffer Access** This flag is set by the Communication Controller when the Host requests the transfer of a Message Buffer from the Message RAM to the Output Buffer while OBCR.OBSYS is set to 1. 0_B No illegal Host access to Output Buffer occurred 1_B Illegal Host access to Output Buffer occurred
MHF	11	rwh	**Message Handler Constraints Flag** The flag signals a Message Handler constraints violation condition. It is set whenever one of the flags MHDF.SNUA, MHDF.SNUB, MHDF.FNFA, MHDF.FNFB, MHDF.TBFA, MHDF.TBFB, MHDF.TNSA, MHDF.TNSB, MHDF.WAHP changes from 0 to 1. 0_B No Message Handler failure detected 1_B Message Handler failure detected

Field	Bits	Type	Description
EDA	16	rwh	**Error Detected on Channel A** This bit is set whenever one of the flags ACS.SEDA, ACS.CEDA, ACS.CIA, ACS.SBVA changes from 0 to 1. 0_B No error detected on channel A 1_B Error detected on channel A This flag is cleared by writing a 1.
LTVA	17	rwh	**Latest Transmit Violation Channel A** The flag signals a latest transmit violation on channel A to the Host. 0_B No latest transmit violation detected on channel A 1_B Latest transmit violation detected on channel A This flag is cleared by writing a 1.
TABA	18	rwh	**Transmission Across Boundary Channel A** The flag signals to the Host that a transmission across a slot boundary occurred for channel A. 0_B No transmission across slot boundary detected on channel A 1_B Transmission across slot boundary detected on channel A This flag is cleared by writing a 1.
EDB	24	rwh	**Error Detected on Channel B** This bit is set whenever one of the flags ACS.SEDB, ACS.CEDB, ACS.CIB, ACS.SBVB changes from 0 to 1. 0_B No error detected on channel B 1_B Error detected on channel B This flag is cleared by writing a 1.
LTVB	25	rwh	**Latest Transmit Violation Channel B** The flag signals a latest transmit violation on channel B to the Host. 0_B No latest transmit violation detected on channel B 1_B Latest transmit violation detected on channel B This flag is cleared by writing a 1.

Field	Bits	Type	Description
TABB	26	rwh	**Transmission Across Boundary Channel B** The flag signals to the Host that a transmission across a slot boundary occurred for channel B. 0_B No transmission across slot boundary detected on channel B 1_B Transmission across slot boundary detected on channel B This flag is cleared by writing a 1.
0	[15:12], [23:19], [31:27]	r	**Reserved** Returns 0 if read; should be written with 0.

Status Service Request Register (SIR)

The flags are set whenever the Communication Controller detects one of the listed events. The flags remain set until the Host clears them. A flag is cleared by writing a 1 to the corresponding bit position. Writing a 0 has no effect on the flag. An application reset will also clear the register.

SIR

Status Service Request Register (0024$_H$) Reset Value: 0000 0000$_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0						MTSB	WUPB	0						MTSA	WUPA
r						rwh	rwh	r						rwh	rwh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SDS	MBSI	SUCS	SWE	TOBC	TIBC	TI1	TI0	NMVC	RFCL	RFNE	RXI	TXI	CYCS	CAS	WST
rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rh	rh	rwh	rwh	rwh	rwh	rwh

Field	Bits	Type	Description
WST	0	rwh	**Wakeup Status** This flag is set when the wakeup status vector CCSV.WSV in the Communication Controller Status Vector register changes to a value other than UNDEFINED. 0_B Wake-up status unmodified 1_B Wake-up status modified (and not UNDEFINED) This flag is cleared by writing a 1.
CAS	1	rwh	**Collision Avoidance Symbol** This flag is set by the Communication Controller during STARTUP state when a CAS or potential CAS was received. 0_B No bit pattern matching the CAS symbol received 1_B Bit pattern matching the CAS symbol received This flag is cleared by writing a 1.
CYCS	2	rwh	**Cycle Start Service Request** This flag is set by the Communication Controller when a communication cycle starts 0_B No communication cycle started 1_B Communication cycle started This flag is cleared by writing a 1.

Field	Bits	Type	Description
TXI	3	rwh	**Transmit Service Request** This flag is set by the Communication Controller at the end of Frame transmission if bit WRHS1.MBI in the respective Message Buffer is set (see **Table 26-24**). 0_B No Frame transmitted from a transmit buffer with WRHS1.MBI = 1 1_B At least one Frame was transmitted from a transmit buffer with WRHS1.MBI = 1 This flag is cleared by writing a 1.
RXI	4	rwh	**Receive Service Request** This flag is set by the Communication Controller whenever the set condition of a Message Buffer ND flag is fulfilled and if bit WRHS1.MBI of that Message Buffer is set to 1(see **Table 26-24**). 0_B No ND flag of a receive buffer with WRHS1.MBI = 1 has been set to 1 1_B At least one ND flag of a receive buffer with WRHS1.MBI = 1 has been set to 1 This flag is cleared by writing a 1.
RFNE	5	rh	**Receive FIFO Not Empty** This flag is set by the Communication Controller when a received valid Frame was stored into the empty receive FIFO.m The actual state of the receive FIFO is monitored in register FSR 0_B Receive FIFO is empty 1_B Receive FIFO is not empty
RFCL	6	rh	**Receive FIFO Critical Level** This flag is set when a valid receive FIFO fill level FSR.RFFL is equal or greater than the critical level as configured by FCL.CL. 0_B Receive FIFO below critical level 1_B Receive FIFO critical level reached
NMVC	7	rwh	**Network Management Vector Changed** This service request flag signals a change in the Network Management Vector visible to the Host. 0_B No change in the Network Management vector 1_B Network Management vector changed This flag is cleared by writing a 1.

Field	Bits	Type	Description
TI0	8	rwh	**Timer Service Request 0** This flag is set whenever timer 0 matches the conditions configured in the Timer Service Request 0 Configuration Register T0C. A Timer Service Request 0 is also signalled by TINT0SRC. 0_B No Timer Service Request 0 1_B Timer Service Request 0 occurred This flag is cleared by writing a 1.
TI1	9	rwh	**Timer Service Request 1** This flag is set whenever the conditions programmed in the Timer Service Request 1 Configuration Register T1C are met. A Timer Service Request 1 is also signalled by TINT1SRC. 0_B No Timer Service Request 1 1_B Timer Service Request 1 occurred This flag is cleared by writing a 1.
TIBC	10	rwh	**Transfer Input Buffer Completed** This flag is set whenever a transfer from Input Buffer to the Message RAM has completed and bit IBCR.IBSYS in the Input Buffer Command Request register has been reset by the Message Handler. 0_B No transfer completed 1_B Transfer between Input Buffer and Message RAM completed This flag is cleared by writing a 1.
TOBC	11	rwh	**Transfer Output Buffer Completed** This flag is set whenever a transfer from Message RAM to the Output Buffer has completed and bit OBCR.OBSYS in the Output Buffer Command Request register has been reset by the Message Handler. 0_B No transfer completed 1_B Transfer between Message RAM and the Output Buffer completed This flag is cleared by writing a 1.
SWE	12	rwh	**Stop Watch Event** This flag is set after a stop watch activation when the current cycle counter and Macrotick value are stored in the Stop Watch Register 1 (STPW1). 0_B No Stop Watch Event 1_B Stop Watch Event occurred This flag is cleared by writing a 1.

Field	Bits	Type	Description
SUCS	13	rwh	**Startup Completed Successfully** This flag is set whenever a startup completed successfully and the Communication Controller entered “NORMAL_ACTIVE” state. 0_B No startup completed successfully 1_B Startup completed successfully This flag is cleared by writing a 1.
MBSI	14	rwh	**Message Buffer Status Service Request** This flag is set by the Communication Controller when the Message Buffer status MBS has changed and if bit RDHS1.MBI of that Message Buffer is set (see **Table 26-24**). 0_B No Message Buffer status change of Message Buffer with RDHS1.MBI= 1 has changed 1_B Message Buffer status of at least one Message Buffer with RDHS1.MBI= 1 has changed This flag is cleared by writing a 1.
SDS	15	rwh	**Start of Dynamic Segment** This flag is set by the Communication Controller when the dynamic segment starts. 0_B Dynamic segment not yet started 1_B Dynamic segment started
WUPA	16	rwh	**Wakeup Pattern Channel A** This flag is set by the Communication Controller when a wakeup pattern was received on channel A. Only set when the Communication Controller is in “WAKEUP”, “READY”, or “STARTUP” state, or when in Monitor mode. 0_B No wake-up pattern received on channel A 1_B Wake-up pattern received on channel A This flag is cleared by writing a 1.
MTSA	17	rwh	**MTS Received on Channel A** (vSS!ValidMTSA) Media Access Test symbol received on channel A during the proceeding symbol window. Updated by the Communication Controller for each channel at the end of the symbol window. 0_B No MTS symbol received on channel A 1_B MTS symbol received on channel A This flag is cleared by writing a 1.

Field	Bits	Type	Description
WUPB	24	rwh	**Wakeup Pattern Channel B** This flag is set by the Communication Controller when a wakeup pattern was received on channel B. Only set when the Communication Controller is in “WAKEUP”, “READY”, or “STARTUP” state, or when in Monitor mode. 0_B No wake-up pattern received on channel B 1_B Wake-up pattern received on channel B This flag is cleared by writing a 1.
MTSB	25	rwh	**MTS Received on Channel B** (vSS!ValidMTSB) Media Access Test symbol received on channel B during the proceeding symbol window. Updated by the Communication Controller for each channel at the end of the symbol window. 0_B No MTS symbol received on channel B 1_B MTS symbol received on channel B This flag is cleared by writing a 1.
0	[23:18], [31:26]	r	**Reserved** Returns 0 if read; should be written with 0.

Error Service Request Line Select (EILS)

The Error Service Request Line Select register assigns a service request generated by a specific error service request flag from register EIR to one of the two module service request lines INT0SRC or INT1SRC:

0 = Interrupt assigned to interrupt line (INT0SRC)

1 = Interrupt assigned to interrupt line (INT1SRC)

EILS

Error Service Request Line Select (0028_H) **Reset Value: $0000\ 0000_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0					TABBL	LTVBL	EDBL	0					TABAL	LTVAL	EDAL
r					rw	rw	rw	r					rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0				MHFL	IOBAL	IIBAL	EFAL	RFOL	EERRL	CCLL	CCFL	SFOL	SFBML	CNAL	PEMCL
r				rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
PEMCL	0	rw	**POC Error Mode Changed Service Request Line** 0_B Service Request assigned to service request line INT0SRC 1_B Service Request assigned to service request line INT1SRC
CNAL	1	rw	**Command Not Accepted Service Request Line** 0_B Service Request assigned to service request line INT0SRC 1_B Service Request assigned to service request line INT1SRC
SFBML	2	rw	**SYNC Frames Below Minimum Service Request Line** 0_B Service Request assigned to service request line INT0SRC 1_B Service Request assigned to service request line INT1SRC

Field	Bits	Type	Description
SFOL	3	rw	**SYNC Frame Overflow Service Request Line** 0_B Service Request assigned to service request line INT0SRC 1_B Service Request assigned to service request line INT1SRC
CCFL	4	rw	**Clock Correction Failure Service Request Line** 0_B Service Request assigned to service request line INT0SRC 1_B Service Request assigned to service request line INT1SRC
CCLL	5	rw	**CHI Command Locked Service Request Line** 0_B Service Request assigned to service request line INT0SRC 1_B Service Request assigned to service request line INT1SRC
EERRL	6	rw	**ECC Error Service Request Line** 0_B Service Request assigned to service request line INT0SRC 1_B Service Request assigned to service request line INT1SRC
RFOL	7	rw	**Receive FIFO Overrun Service Request Line** 0_B Service Request assigned to service request line INT0SRC 1_B Service Request assigned to service request line INT1SRC
EFAL	8	rw	**Empty FIFO Access Service Request Line** 0_B Service Request assigned to service request line INT0SRC 1_B Service Request assigned to service request line INT1SRC
IIBAL	9	rw	**Illegal Input Buffer Access Service Request Line** 0_B Service Request assigned to service request line INT0SRC 1_B Service Request assigned to service request line INT1SRC

Field	Bits	Type	Description
IOBAL	10	rw	**Illegal Output Buffer Access Service Request Line** 0_B Service Request assigned to service request line INT0SRC 1_B Service Request assigned to service request line INT1SRC
MHFL	11	rw	**Message Handler Constrains Flag Service Request Line** 0_B Service Request assigned to service request line INT0SRC 1_B Service Request assigned to service request line INT1SRC
EDAL	16	rw	**Error Detected on Channel A Service Request Line** 0_B Service Request assigned to service request line INT0SRC 1_B Service Request assigned to service request line INT1SRC
LTVAL	17	rw	**Latest Transmit Violation Channel A Service Request Line** 0_B Service Request assigned to service request line INT0SRC 1_B Service Request assigned to service request line INT1SRC
TABAL	18	rw	**Transmission Across Boundary Channel A Service Request Line** 0_B Service Request assigned to service request line INT0SRC 1_B Service Request assigned to service request line INT1SRC
EDBL	24	rw	**Error Detected on Channel B Service Request Line** 0_B Service Request assigned to service request line INT0SRC 1_B Service Request assigned to service request line INT1SRC
LTVBL	25	rw	**Latest Transmit Violation Channel B Service Request Line** 0_B Service Request assigned to service request line INT0SRC 1_B Service Request assigned to service request line INT1SRC

Field	Bits	Type	Description
TABBL	26	rw	**Transmission Across Boundary Channel A Service Request Line** 0_B Service Request assigned to service request line INT0SRC 1_B Service Request assigned to service request line INT1SRC
0	[15:12], [23:19], [31:27]	r	**Reserved** Returns 0 if read; should be written with 0.

Status Service Request Line Select (SILS)

The Status Service Request Line Select register assign an service request generated by a specific status service request flag from register SIR to one of the two module service request lines INT0SRC or INT1SRC:

0 = Interrupt assigned to interrupt line INT0SRC

1 = Interrupt assigned to interrupt line INT1SRC

SILS

Status Service Request Line Select (002C$_H$) **Reset Value: 0303 FFFF$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0						MTSBL	WUPBL	0						MTSAL	WUPAL
r						rw	rw	r						rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SDSL	MBSIL	SUCSL	SWEL	TOBCL	TIBCL	TI1L	TI0L	NMVCL	RFCLL	RFNEL	RXIL	TXIL	CYCSL	CASL	WSTL
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
WSTL	0	rw	**Wakeup Status Service Request Line** 0_B Service Request assigned to service request line INT0SRC 1_B Service Request assigned to service request line INT1SRC
CASL	1	rw	**Collision Avoidance Symbol Service Request Line** 0_B Service Request assigned to service request line INT0SRC 1_B Service Request assigned to service request line INT1SRC
CYCSL	2	rw	**Cycle Start Service Request Line** 0_B Service Request assigned to service request line INT0SRC 1_B Service Request assigned to service request line INT1SRC

Field	Bits	Type	Description
TXIL	3	rw	**Transmit Service Request Line** 0_B Service Request assigned to service request line INT0SRC 1_B Service Request assigned to service request line INT1SRC
RXIL	4	rw	**Receive Service Request Line** 0_B Service Request assigned to service request line INT0SRC 1_B Service Request assigned to service request line INT1SRC
RFNEL	5	rw	**Receive FIFO Not Empty Service Request Line** 0_B Service Request assigned to service request line INT0SRC 1_B Service Request assigned to service request line INT1SRC
RFCLL	6	rw	**Receive FIFO Critical Level Service Request Line** 0_B Service Request assigned to service request line INT0SRC 1_B Service Request assigned to service request line INT1SRC
NMVCL	7	rw	**Network Management Vector Changed Service Request Line** 0_B Service Request assigned to service request line INT0SRC 1_B Service Request assigned to service request line INT1SRC
TI0L	8	rw	**Timer Service Request 0 Line** 0_B Service Request assigned to service request line INT0SRC 1_B Service Request assigned to service request line INT1SRC
TI1L	9	rw	**Timer Service Request 1 Line** 0_B Service Request assigned to service request line INT0SRC 1_B Service Request assigned to service request line INT1SRC

Field	Bits	Type	Description
TIBCL	10	rw	**Transfer Input Buffer Completed Service Request Line** 0_B Service Request assigned to service request line INT0SRC 1_B Service Request assigned to service request line INT1SRC
TOBCL	11	rw	**Transfer Output Buffer Completed Service Request Line** 0_B Service Request assigned to service request line INT0SRC 1_B Service Request assigned to service request line INT1SRC
SWEL	12	rw	**Stop Watch Event Service Request Line** 0_B Service Request assigned to service request line INT0SRC 1_B Service Request assigned to service request line INT1SRC
SUCSL	13	rw	**Startup Completed Successfully Service Request Line** 0_B Service Request assigned to service request line INT0SRC 1_B Service Request assigned to service request line INT1SRC
MBSIL	14	rw	**Message Buffer Status Service Request Line** 0_B Service Request assigned to service request line INT0SRC 1_B Service Request assigned to service request line INT1SRC
SDSL	15	rw	**Start of Dynamic Segment Service Request Line** 0_B Service Request assigned to service request line INT0SRC 1_B Service Request assigned to service request line INT1SRC
WUPAL	16	rw	**Wakeup Pattern Channel A Service Request Line** 0_B Service Request assigned to service request line INT0SRC 1_B Service Request assigned to service request line INT1SRC

Field	Bits	Type	Description
MTSAL	17	rw	**Media Access Test Symbol Channel A Service Request Line** 0_B Service Request assigned to service request line INT0SRC 1_B Service Request assigned to service request line INT1SRC
WUPBL	24	rw	**Wakeup Pattern Channel B Service Request Line** 0_B Service Request assigned to service request line INT0SRC 1_B Service Request assigned to service request line INT1SRC
MTSBL	25	rw	**Media Access Test Symbol Channel B Service Request Line** 0_B Service Request assigned to service request line INT0SRC 1_B Service Request assigned to service request line INT1SRC
0	[23:18], [31:26]	r	**Reserved** Returns 0 if read; should be written with 0.

Error Service Request Enable Set (EIES)

The settings in the Error Service Request Enable register determine which status changes in the Error Service Request Register will result in an service request. The enable bits are set by writing to EIES and reset by writing to EIER. Writing a 1 sets the specific enable bit, a 0 has no effect.

EIES

Error Service Request Enable Set (0030_H) Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0					TABBE	LTVBE	EDBE	0					TABAE	LTVAE	EDAE
r					rwh	rwh	rwh	r					rwh	rwh	rwh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0				MHFE	IOBAE	IIBAE	EFAE	RFOE	EERRE	CCLE	CCFE	SFOE	SFBME	CNAE	PEMCE
r				rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh

Field	Bits	Type	Description
PEMCE	0	rwh	**POC Error Mode Changed Service Request Enable** Read: 0_B Protocol Error Mode Changed Service Request disabled 1_B Protocol Error Mode Changed Service Request enabled Write: 0_B Unchanged 1_B Enable Protocol Error Mode Changed Service Request
CNAE	1	rwh	**Command Not Accepted Service Request Enable** Read: 0_B Command Not Valid Service Request disabled 1_B Command Not Valid Service Request enabled Write: 0_B Unchanged 1_B Enable Command Not Valid Service Request

Field	Bits	Type	Description
SFBME	2	rwh	**SYNC Frames Below Minimum Service Request Enable** Read: 0_B SYNC Frames Below Minimum Service Request disabled 1_B SYNC Frames Below Minimum Service Request enabled Write: 0_B Unchanged 1_B Enable SYNC Frames Below Minimum Service Request
SFOE	3	rwh	**SYNC Frame Overflow Service Request Enable** Read: 0_B SYNC Frame Overflow Service Request disabled 1_B SYNC Frame Overflow Service Request enabled Write: 0_B Unchanged 1_B Enable Protocol Error Mode Changed Service Request
CCFE	4	rwh	**Clock Correction Failure Service Request Enable** Read: 0_B Clock Correction Failure Service Request disabled 1_B Clock Correction Failure Service Request enabled Write: 0_B Unchanged 1_B Enable Clock Correction Failure Service Request
CCLE	5	rwh	**CHI Command Locked Service Request Enable** Read: 0_B CHI Command Locked Service Request disabled 1_B CHI Command Locked Service Request enabled Write: 0_B Unchanged 1_B Enable CHI Command Locked Service Request
EERRE	6	rwh	**ECC Error Service Request Enable** Read: 0_B ECC Error Service Request disabled 1_B ECC Error Service Request enabled Write: 0_B Unchanged 1_B Enable ECC Error Service Request

Field	Bits	Type	Description
RFOE	7	rwh	**Receive FIFO Overrun Service Request Enable** Read: 0_B Receive FIFO Overrun Service Request disabled 1_B Receive FIFO Overrun Service Request enabled Write: 0_B Unchanged 1_B Enable Receive FIFO Overrun Service Request
EFAE	8	rwh	**Empty FIFO Access Service Request Enable** Read: 0_B Empty FIFO Access Service Request disabled 1_B Empty FIFO Access Service Request enabled Write: 0_B Unchanged 1_B Enable Empty FIFO Access Service Request
IIBAE	9	rwh	**Illegal Input Buffer Access Service Request Enable** Read: 0_B Illegal Input Buffer Access Service Request disabled 1_B Illegal Input Buffer Access Service Request enabled Write: 0_B Unchanged 1_B Enable Illegal Input Buffer Access Service Request
IOBAE	10	rwh	**Illegal Output Buffer Access Service Request Enable** Read: 0_B Illegal Output Buffer Access Service Request disabled 1_B Illegal Output Buffer Access Service Request enabled Write: 0_B Unchanged 1_B Enable Illegal Output Buffer Access Service Request
MHFE	11	rwh	**Message Handler Constraints Flag Service Request Enable** Read: 0_B Message Handler Constraints Flag Service Request disabled 1_B Message Handler Constraints Flag Service Request enabled Write: 0_B Unchanged 1_B Enable Message Handler Constraints Flag Service Request

Field	Bits	Type	Description
EDAE	16	rwh	**Error Detected on Channel A Service Request Enable** Read: 0_B Error Detected on Channel A Service Request disabled 1_B Error Detected on Channel A Service Request enabled Write: 0_B Unchanged 1_B Enable Error Detected on Channel A Service Request
LTVAE	17	rwh	**Latest Transmit Violation Channel A Service Request Enable** Read: 0_B Latest Transmit Violation Channel A Service Request disabled 1_B Latest Transmit Violation Channel A Service Request enabled Write: 0_B Unchanged 1_B Enable Latest Transmit Violation Channel A Service Request
TABAE	18	rwh	**Transmission Across Boundary Channel A Service Request Enable** Read: 0_B Transmission Across Boundary Channel A Service Request disabled 1_B Transmission Across Boundary Channel A Service Request enabled Write: 0_B Unchanged 1_B Enable Transmission Across Boundary Channel A Service Request
EDBE	24	rwh	**Error Detected on Channel B Service Request Enable** Read: 0_B Error Detected on Channel B Service Request disabled 1_B Error Detected on Channel B Service Request enabled Write: 0_B Unchanged 1_B Enable Error Detected on Channel B Service Request

Field	Bits	Type	Description
LTVBE	25	rwh	**Latest Transmit Violation Channel B Service Request Enable** Read: 0_B Latest Transmit Violation Channel B Service Request disabled 1_B Latest Transmit Violation Channel B Service Request enabled Write: 0_B Unchanged 1_B Enable Latest Transmit Violation Channel B Service Request
TABBE	26	rwh	**Transmission Across Boundary Channel B Service Request Enable** Read: 0_B Transmission Across Boundary Channel B Service Request disabled 1_B Transmission Across Boundary Channel B Service Request enabled Write: 0_B Unchanged 1_B Enable Transmission Across Boundary Channel B Service Request
0	[15:12], [23:19], [31:27]	r	**Reserved** Returns 0 if read; should be written with 0.

Error Service Request Enable Reset (EIER)

The settings in the Error Service Request Enable register determine which status changes in the Error Service Request Register will result in a service request. The enable bits are set by writing to EIES and reset by writing to EIER. Writing a 1 resets the specific enable bit, a 0 has no effect.

EIER

Error Service Request Enable Reset (0034_H) **Reset Value: $0000\ 0000_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0					TABBE	LTVBE	EDBE	0					TABAE	LTVAE	EDAE
r					rwh	rwh	rwh	r					rwh	rwh	rwh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0				MHFE	IOBAE	IIBAE	EFAE	RFOE	EERRE	CCLE	CCFE	SFOE	SFBME	CNAE	PEMCE
r				rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh

Field	Bits	Type	Description
PEMCE	0	rwh	**POC Error Mode Changed Service Request Enable** Read: 0_B Protocol Error Mode Changed Service Request disabled 1_B Protocol Error Mode Changed Service Request enabled Write: 0_B Unchanged 1_B Disable Protocol Error Mode Changed Service Request
CNAE	1	rwh	**Command Not Accepted Service Request Enable** Read: 0_B Command Not Accepted Service Request disabled 1_B Command Not Accepted Service Request enabled Write: 0_B Unchanged 1_B Disable Command Not Accepted Service Request

Field	Bits	Type	Description
SFBME	2	rwh	**SYNC Frames Below Minimum Service Request Enable** Read: 0_B SYNC Frames Below Minimum Service Request disabled 1_B SYNC Frames Below Minimum Service Request enabled Write: 0_B Unchanged 1_B Disable SYNC Frames Below Minimum Service Request
SFOE	3	rwh	**SYNC Frame Overflow Service Request Enable** Read: 0_B SYNC Frame Overflow Service Request disabled 1_B SYNC Frame Overflow Service Request enabled Write: 0_B Unchanged 1_B Disable Protocol Error Mode Changed Service Request
CCFE	4	rwh	**Clock Correction Failure Service Request Enable** Read: 0_B Clock Correction Failure Service Request disabled 1_B Clock Correction Failure Service Request enabled Write: 0_B Unchanged 1_B Disable Clock Correction Failure Service Request
CCLE	5	rwh	**CHI Command Locked Service Request Enable** Read: 0_B CHI Command Locked Service Request disabled 1_B CHI Command Locked Service Request enabled Write: 0_B Unchanged 1_B Disable CHI Command Locked Service Request
EERRE	6	rwh	**ECC Error Service Request Enable** Read: 0_B ECC Error Service Request disabled 1_B ECC Error Service Request enabled Write: 0_B Unchanged 1_B Disable ECC Error Service Request

Field	Bits	Type	Description
RFOE	7	rwh	**Receive FIFO Overrun Service Request Enable** Read: 0_B Receive FIFO Overrun Service Request disabled 1_B Receive FIFO Overrun Service Request enabled Write: 0_B Unchanged 1_B Disable Receive FIFO Overrun Service Request
EFAE	8	rwh	**Empty FIFO Access Service Request Enable** Read: 0_B Empty FIFO Access Service Request disabled 1_B Empty FIFO Access Service Request enabled Write: 0_B Unchanged 1_B Disable Empty FIFO Access Service Request
IIBAE	9	rwh	**Illegal Input Buffer Access Service Request Enable** Read: 0_B Illegal Input Buffer Access Service Request disabled 1_B Illegal Input Buffer Access Service Request enabled Write: 0_B Unchanged 1_B Disable Illegal Input Buffer Access Service Request
IOBAE	10	rwh	**Illegal Output Buffer Access Service Request Enable** Read: 0_B Illegal Output Buffer Access Service Request disabled 1_B Illegal Output Buffer Access Service Request enabled Write: 0_B Unchanged 1_B Disable Illegal Output Buffer Access Service Request
MHFE	11	rwh	**Message Handler Constraints Flag Service Request Enable** Read: 0_B Message Handler Constraints Flag Service Request disabled 1_B Message Handler Constraints Flag Service Request enabled Write: 0_B Unchanged 1_B Disable Message Handler Constraints Flag Service Request

Field	Bits	Type	Description
EDAE	16	rwh	**Error Detected on Channel A Service Request Enable** Read: 0_B Error Detected on Channel A Service Request disabled 1_B Error Detected on Channel A Service Request enabled Write: 0_B Unchanged 1_B Disable Error Detected on Channel A Service Request
LTVAE	17	rwh	**Latest Transmit Violation Channel A Service Request Enable** Read: 0_B Latest Transmit Violation Channel A Service Request disabled 1_B Latest Transmit Violation Channel A Service Request enabled Write: 0_B Unchanged 1_B Disable Latest Transmit Violation Channel A Service Request
TABAE	18	rwh	**Transmission Across Boundary Channel A Service Request Enable** Read: 0_B Transmission Across Boundary Channel A Service Request disabled 1_B Transmission Across Boundary Channel A Service Request enabled Write: 0_B Unchanged 1_B Enable Transmission Across Boundary Channel A Service Request
EDBE	24	rwh	**Error Detected on Channel B Service Request Enable** Read: 0_B Error Detected on Channel B Service Request disabled 1_B Error Detected on Channel B Service Request enabled Write: 0_B Unchanged 1_B Disable Error Detected on Channel B Service Request

Field	Bits	Type	Description
LTVBE	25	rwh	**Latest Transmit Violation Channel B Service Request Enable** Read: 0_B Latest Transmit Violation Channel B Service Request disabled 1_B Latest Transmit Violation Channel B Service Request enabled Write: 0_B Unchanged 1_B Disable Latest Transmit Violation Channel B Service Request
TABBE	26	rwh	**Transmission Across Boundary Channel B Service Request Enable** Read: 0_B Transmission Across Boundary Channel B Service Request disabled 1_B Transmission Across Boundary Channel B Service Request enabled Write: 0_B Unchanged 1_B Disable Transmission Across Boundary Channel B Service Request
0	[15:12], [23:19], [31:27]	r	**Reserved** Returns 0 if read; should be written with 0.

Status Service Request Enable Set (SIES)

The settings in the Status Service Request Enable Set register determine which status changes in the Status Service Request Register will result in a service request. The enable bits are set by writing to SIES and reset by writing to SIER. Writing a 1 sets the specific enable bit, a 0 has no effect.

SIES

Status Service Request Enable Set (0038_H) **Reset Value: $0000\ 0000_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0						MTSBE	WUPBE	0						MTSAE	WUPAE
r						rwh	rwh	r						rwh	rwh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SDSE	MBSIE	SUCSE	SWEE	TOBCE	TIBCE	TI1E	TI0E	NMVCE	RFCLE	RFNEE	RXIE	TXIE	CYCSE	CASE	WSTE
rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh

Field	Bits	Type	Description
WSTE	0	rwh	**Wakeup Status Service Request Enable** Read: 0_B Wake-up Status Service Request disabled 1_B Wake-up Status Service Request enabled Write: 0_B Unchanged 1_B Enable Wakeup Status Service Request
CASE	1	rwh	**Collision Avoidance Symbol Service Request Enable** Read: 0_B Collision Avoidance Symbol Service Request disabled 1_B Collision Avoidance Symbol Service Request enabled Write: 0_B Unchanged 1_B Enable Collision Avoidance Symbol Service Request
CYCSE	2	rwh	**Cycle Start Service Request Enable** Read: 0_B Cycle Start Service Request disabled 1_B Cycle Start Service Request enabled Write: 0_B Unchanged 1_B Enable Cycle Start Service Request

Field	Bits	Type	Description
TXIE	3	rwh	**Transmit Service Request Enable** Read: 0_B Transmit Service Request disabled 1_B Transmit Service Request enabled Write: 0_B Unchanged 1_B Enable Transmit Service Request
RXIE	4	rwh	**Receive Service Request Enable** Read: 0_B Receive Service Request disabled 1_B Receive Service Request enabled Write: 0_B Unchanged 1_B Enable Receive Service Request
RFNEE	5	rwh	**Receive FIFO Not Empty Service Request Enable** Read: 0_B Receive FIFO Not Empty Service Request disabled 1_B Receive FIFO Not Empty Service Request enabled Write: 0_B Unchanged 1_B Enable Receive FIFO Not Empty Service Request
RFCLE	6	rwh	**Receive FIFO Critical Level Service Request Enable** Read: 0_B Receive FIFO Critical Level Service Request disabled 1_B Receive FIFO Critical Level Service Request enabled Write: 0_B Unchanged 1_B Enable Receive FIFO Critical Level Service Request
NMVCE	7	rwh	**Network Management Vector Changed Service Request Enable** Read: 0_B Network Management Vector Changed Service Request disabled 1_B Network Management Vector Changed Service Request enabled Write: 0_B Unchanged 1_B Enable Network Management Vector Changed Service Request

Field	Bits	Type	Description
TI0E	8	rwh	**Timer Service Request 0 Enable** Read: 0_B Timer Service Request 0disabled 1_B Timer Service Request 0 enabled Write: 0_B Unchanged 1_B Enable Timer Service Request 0
TI1E	9	rwh	**Timer Service Request 1 Enable** Read: 0_B Timer Service Request 1disabled 1_B Timer Service Request 1 enabled Write: 0_B Unchanged 1_B Enable Timer Service Request 1
TIBCE	10	rwh	**Transfer Input Buffer Completed Service Request Enable** Read: 0_B Wakeup Status Service Request disabled 1_B Wakeup Status Service Request enabled Write: 0_B Unchanged 1_B Enable Wakeup Status Service Request
TOBCE	11	rwh	**Transfer Output Buffer Completed Service Request Enable** Read: 0_B Transfer Input Buffer Completed Service Request disabled 1_B Transfer Input Buffer Completed Service Request enabled Write: 0_B Unchanged 1_B Enable Transfer Input Buffer Completed Service Request
SWEE	12	rwh	**Stop Watch Event Service Request Enable** Read: 0_B Stop Watch Event Service Request disabled 1_B Stop Watch Event Service Request enabled Write: 0_B Unchanged 1_B Enable Stop Watch Event Service Request

Field	Bits	Type	Description
SUCSE	13	rwh	**Startup Completed Successfully Service Request Enable** Read: 0_B Startup Completed Successfully Service Request disabled 1_B Startup Completed Successfully Service Request enabled Write: 0_B Unchanged 1_B Enable Startup Completed Successfully Service Request
MBSIE	14	rwh	**Message Buffer Status Service Request Enable** Read: 0_B Message Buffer Status Service Request disabled 1_B Message Buffer Status Service Request enabled Write: 0_B Unchanged 1_B Enable Message Buffer Status Service Request
SDSE	15	rwh	**Start of Dynamic Segment Service Request Enable** Read: 0_B Start of Dynamic Service Request disabled 1_B Start of Dynamic Service Request enabled Write: 0_B Unchanged 1_B Enable Start of Dynamic Service Request
WUPAE	16	rwh	**Wakeup Pattern Channel A Service Request Enable** Read: 0_B Wakeup Pattern Channel A Service Request disabled 1_B Wakeup Pattern Channel A Service Request enabled Write: 0_B Unchanged 1_B Enable Wakeup Pattern Channel A Service Request

Field	Bits	Type	Description
MTSAE	17	rwh	**Media Access Test Symbol Channel A Service Request Enable** Read: 0_B Media Access Test Symbol Channel A Service Request disabled 1_B Media Access Test Symbol Channel A Service Request enabled Write: 0_B Unchanged 1_B Enable Media Access Test Symbol Channel A Service Request
WUPBE	24	rwh	**Wakeup Pattern Channel B Service Request Enable** Read: 0_B Wakeup Pattern Channel B Service Request disabled 1_B Wakeup Pattern Channel B Service Request enabled Write: 0_B Unchanged 1_B Enable Wakeup Pattern Channel A Service Request
MTSBE	25	rwh	**Media Access Test Symbol Channel B Service Request Enable** Read: 0_B Media Access Test Symbol Channel B Service Request disabled 1_B Media Access Test Symbol Channel B Service Request enabled Write: 0_B Unchanged 1_B Enable Media Access Test Symbol Channel B Service Request
0	[23:18], [31:26]	r	**Reserved** Returns 0 if read; should be written with 0.

Status Service Request Enable Reset (SIER)

The settings in the Status Service Request Enable Reset register determine which status changes in the Status Service Request Register will result in a service request. The enable bits are set by writing to SIES and reset by writing to SIER. Writing a 1 resets the specific enable bit, a 0 has no effect.

SIER

Status Service Request Enable Reset(003C$_H$) **Reset Value: 0000 0000$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0						MTSBE	WUPBE	0						MTSAE	WUPAE
r						rwh	rwh	r						rwh	rwh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SDSE	MBSIE	SUCSE	SWEE	TOBCE	TIBCE	TI1E	TI0E	NMVCE	RFCLE	RFNEE	RXIE	TXIE	CYCSE	CASE	WSTE
rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh

Field	Bits	Type	Description
WSTE	0	rwh	**Wakeup Status Service Request Enable** Read: 0_B Wakeup Status Service Request disabled 1_B Wakeup Status Service Request enabled Write: 0_B Unchanged 1_B Disable Wakeup Status Service Request
CASE	1	rwh	**Collision Avoidance Symbol Service Request Enable** Read: 0_B Collision Avoidance Symbol Service Request disabled 1_B Collision Avoidance Symbol Service Request enabled Write: 0_B Unchanged 1_B Disable Collision Avoidance Symbol Service Request
CYCSE	2	rwh	**Cycle Start Service Request Enable** Read: 0_B Cycle Start Service Request disabled 1_B Cycle Start Service Request enabled Write: 0_B Unchanged 1_B Disable Cycle Start Service Request

Field	Bits	Type	Description
TXIE	3	rwh	**Transmit Service Request Enable** Read: 0_B Transmit Service Request disabled 1_B Transmit Service Request enabled Write: 0_B Unchanged 1_B Disable Transmit Service Request
RXIE	4	rwh	**Receive Service Request Enable** Read: 0_B Receive Service Request disabled 1_B Receive Service Request enabled Write: 0_B Unchanged 1_B Disable Receive Service Request
RFNEE	5	rwh	**Receive FIFO Not Empty Service Request Enable** Read: 0_B Receive FIFO Not Empty Service Request disabled 1_B Receive FIFO Not Empty Service Request enabled Write: 0_B Unchanged 1_B Disable Receive FIFO Not Empty Service Request
RFCLE	6	rwh	**Receive FIFO Critical Level Service Request Enable** Read: 0_B Service Request disabled 1_B Receive FIFO Critical Level Service Request enabled Write: 0_B Unchanged 1_B Disable Receive FIFO Critical Level Service Request
NMVCE	7	rwh	**Network Management Vector Changed Service Request Enable** Read: 0_B Network Management Vector Changed Service Request disabled 1_B Network Management Vector Changed Service Request enabled Write: 0_B Unchanged 1_B Disable Network Management Vector Changed Service Request

Field	Bits	Type	Description
TI0E	8	rwh	**Timer Service Request 0 Enable** Read: 0_B Timer Service Request 0 disabled 1_B Timer Service Request 0 enabled Write: 0_B Unchanged 1_B Disable Service Request 0
TI1E	9	rwh	**Timer Service Request 1 Enable** Read: 0_B Timer Service Request 1 disabled 1_B Timer Service Request 1 enabled Write: 0_B Unchanged 1_B Disable Timer Service Request 1
TIBCE	10	rwh	**Transfer Input Buffer Completed Service Request Enable** Read: 0_B Wakeup Status Service Request disabled 1_B Wakeup Status Service Request enabled Write: 0_B Unchanged 1_B Disable Wakeup Status Service Request
TOBCE	11	rwh	**Transfer Output Buffer Completed Service Request Enable** Read: 0_B Transfer Input Buffer Completed Service Request disabled 1_B Transfer Input Buffer Completed Service Request enabled Write: 0_B Unchanged 1_B Disable Transfer Input Buffer Completed Service Request
SWEE	12	rwh	**Stop Watch Event Service Request Enable** Read: 0_B Stop Watch Event Service Request disabled 1_B Stop Watch Event Service Request enabled Write: 0_B Unchanged 1_B Disable Stop Watch Event Service Request

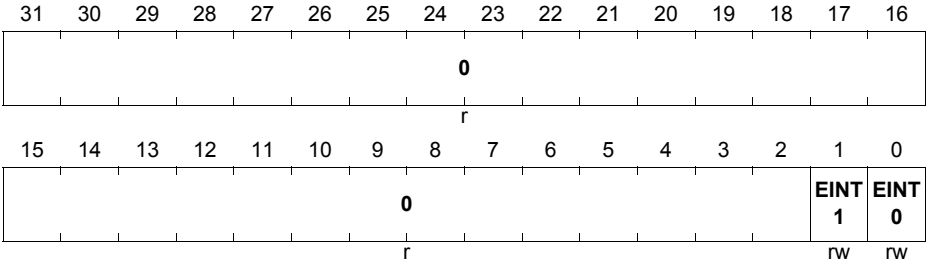
Field	Bits	Type	Description
SUCSE	13	rwh	**Startup Completed Successfully Service Request Enable** Read: 0_B Startup Completed Successfully Service Request disabled 1_B Startup Completed Successfully Service Request enabled Write: 0_B Unchanged 1_B Disable Startup Completed Successfully Service Request
MBSIE	14	rwh	**Message Buffer Status Service Request Enable** Read: 0_B Message Buffer Status Service Request disabled 1_B Message Buffer Status Service Request enabled Write: 0_B Unchanged 1_B Disable Message Buffer Status Service Request
SDSE	15	rwh	**Start of Dynamic Segment Service Request Enable** Read: 0_B Start of Dynamic Service Request disabled 1_B Start of Dynamic Service Request enabled Write: 0_B Unchanged 1_B Disable Start of Dynamic Service Request
WUPAE	16	rwh	**Wakeup Pattern Channel A Service Request Enable** Read: 0_B Wakeup Pattern Channel A Service Request disabled 1_B Wakeup Pattern Channel A Service Request enabled Write: 0_B Unchanged 1_B Disable Wakeup Pattern Channel A Service Request

Field	Bits	Type	Description
MTSAE	17	rwh	**Media Access Test Symbol Channel A Service Request Enable** Read: 0_B Media Access Test Symbol Channel A Service Request disabled 1_B Media Access Test Symbol Channel A Service Request enabled Write: 0_B Unchanged 1_B Disable Media Access Test Symbol Channel A Service Request
WUPBE	24	rwh	**Wakeup Pattern Channel B Service Request Enable** Read: 0_B Wakeup Pattern Channel B Service Request disabled 1_B Wakeup Pattern Channel B Service Request enabled Write: 0_B Unchanged 1_B Disable Wakeup Pattern Channel A Service Request
MTSBE	25	rwh	**Media Access Test Symbol Channel B Service Request Enable** Read: 0_B Media Access Test Symbol Channel B Service Request disabled 1_B Media Access Test Symbol Channel B Service Request enabled Write: 0_B Unchanged 1_B Disable Media Access Test Symbol Channel B Service Request
0	[23:18], [31:26]	r	**Reserved** Returns 0 if read; should be written with 0.

Service Request Line Enable (ILE)

Each of the two service request lines to the Host INT0SRC, INT1SRC can be enabled / disabled separately by programming bit EINT0 and EINT1.

ILE
Service Request Line Enable **(0040_H)** **Reset Value: $0000\ 0000_H$**



Field	Bits	Type	Description
EINT0	0	rw	**Enable Service Request Line 0** (INT0SRC) 0_B Service Request line disabled 1_B Service Request line enabled
EINT1	1	rw	**Enable Service Request Line 1** (INT1SRC) 0_B Service Request line disabled 1_B Service Request line enabled
0	[31:2]	r	**Reserved** Returns 0 if read; should be written with 0.

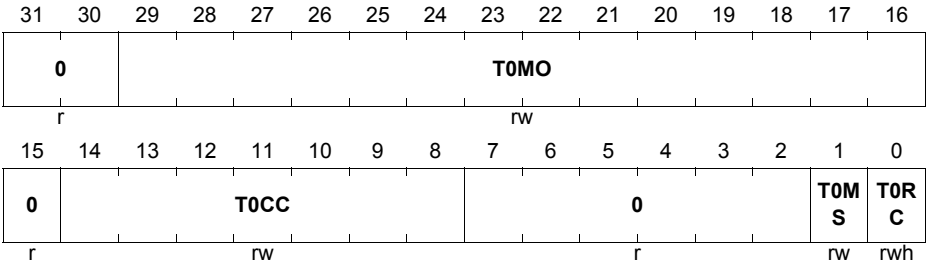
Timer 0 Configuration (T0C)

Absolute timer. Specifies in terms of cycle count and Macrotick the point in time when the timer 0 service request occurs. When the timer 0 service request is asserted, output signal TINT0SR is set to 1 for the duration of one Macrotick and SIR.TI0 is set to 1.

Timer 0 can be activated as long as the POC is either in “NORMAL_ACTIVE” state or in “NORMAL_PASSIVE” state. Timer 0 is deactivated when leaving “NORMAL_ACTIVE” state or “NORMAL_PASSIVE” state except for transitions between the two states.

Before reconfiguration of the timer, the timer has to be halted first by writing 0 to bit T0RC.

T0C
Timer 0 Configuration **(0044_H)** **Reset Value: $0000\ 0000_H$**



Field	Bits	Type	Description
T0RC	0	rwh	**Timer 0 Run Control** 0_B Timer 0 halted 1_B Timer 0 running
T0MS	1	rw	**Timer 0 Mode Select** 0_B Single-shot mode 1_B Continuous mode
T0CC	[14:8]	rw	**Timer 0 Cycle Code** The 7-bit timer 0 cycle code determines the cycle set used for generation of the timer 0 service request. For details about the configuration of the cycle code see **“Cycle Counter Filtering” on Page 26-224**.
T0MO	[29:16]	rw	**Timer 0 Macrotick Offset** Configures the Macrotick offset from the beginning of the cycle where the service request is to occur. The Timer 0 Service Request occurs at this offset for each cycle of the cycle set.

Field	Bits	Type	Description
0	[7:2], 15, [31:30]	r	**Reserved** Returns 0 if read; should be written with 0.

Note: The configuration of timer 0 is compared against the Macrotick counter value, there is no separate counter for timer 0. In case the Communication Controller leaves "NORMAL_ACTIVE" or "NORMAL_PASSIVE" state, or if timer 0 is halted by Host command, output signal TINT0SR *is reset to 0 immediately.*

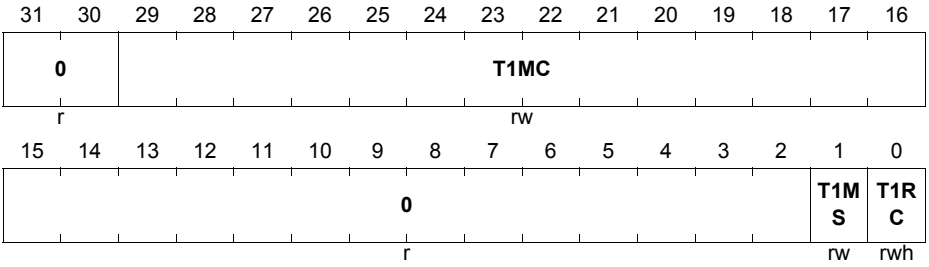
Timer 1 Configuration (T1C)

Relative timer. After the specified number of Macroticks has expired, the timer 1 service request is asserted, output signal TINT1SR is set to 1 for the duration of one Macrotick and SIR.TI1 is set to 1.

Timer 1 can be activated as long as the POC is either in “NORMAL_ACTIVE” state or in “NORMAL_PASSIVE” state. Timer 1 is deactivated when leaving “NORMAL_ACTIVE” state or “NORMAL_PASSIVE” state except for transitions between the two states.

Before reconfiguration of the timer, the timer has to be halted first by resetting bit T1RC to 0.

T1C
Timer 1 Configuration **(0048_H)** **Reset Value: $0002\ 0000_H$**



Field	Bits	Type	Description
T1RC	0	rwh	**Timer 1 Run Control** 0_B Timer 1 halted 1_B Timer 1 running
T1MS	1	rw	**Timer 1 Mode Select** 0_B Single-shot mode 1_B Continuous mode
T1MC	[29:16]	rw	**Timer 1 Macrotick Count** When the configured Macrotick count is reached the timer 1 service request is generated. Valid values are: 2_H …$3FFF_H$ Macroticks in continuous mode 1_H …$3FFF_H$ Macroticks in single-shot mode
0	[15:2], [31:30]	r	**Reserved** Returns 0 if read; should be written with 0.

Note: In case the Communication Controller leaves "NORMAL_ACTIVE" or "NORMAL_PASSIVE" state, or if timer 1 is halted by Host command, output signal TINT1SR *is reset to 0 immediately.*

Stop Watch Register 1 (STPW1)

The stop watch is activated by a rising or falling edge on signal STPW, by a service request 0 or 1 event (rising edge on signal INT0SR or INT1SR) or by the Host by writing bit STPW1.SSWT to 1. With the Macrotick counter increment following next to the stop watch activation the actual cycle counter and Macrotick value are captured in the Stop Watch Register 1 STPW1 while the slot counter values for channel A and B are captured in the Stop Watch Register 2 STPW2.

STPW1
Stop Watch Register 1 **(004C$_H$)** **Reset Value: 0000 0000$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0								SMTV							
r								rh							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0		SCCV						0	EINT1	EINT0	EETP	SSWT	EDGE	SWMS	ESWT
r		rh						r	rw	rw	rw	rwh	rw	rw	rwh

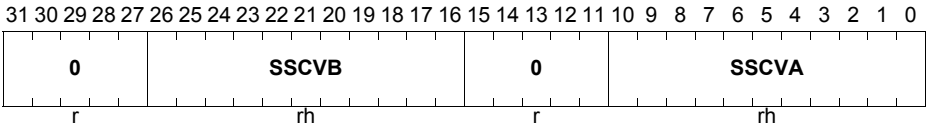
Field	Bits	Type	Description
ESWT	0	rwh	**Enable Stop Watch Trigger** If enabled an edge on input STPW or a service request 0 or 1 event (rising edge on signal INT0SR or INT1SR) activates the stop watch. In single-shot mode this bit is reset to 0 after the actual cycle counter and Macrotick value are stored in the Stop Watch register. 0_B Stop watch trigger disabled 1_B Stop watch trigger enabled
SWMS	1	rw	**Stop Watch Mode Select** It is not possible to change the Stop Watch Mode during enabled stop watch trigger (STPW1.ESWT) 0_B Single-shot mode 1_B Continuous mode
EDGE	2	rw	**Stop Watch Trigger Edge Select** 0_B Falling Edge 1_B Rising Edge

Field	Bits	Type	Description
SSWT	3	rwh	**Software Stop Watch Trigger** When the Host writes this bit to 1 the stop watch is activated. After the actual cycle counter and Macrotick value are stored in the Stop Watch register this bit is reset to 0. The bit is only writeable while ESWT = 0. 0_B Software trigger reset 1_B Stop watch activated by software trigger
EETP	4	rw	**Enable External Trigger Pin** Enables stop watch trigger event via signal STPW if ESWT = 1. 0_B Stop watch trigger via signal STPW disabled 1_B Edge on signal STPW triggers stop watch
EINT0	5	rw	**Enable Service Request 0 Trigger** Enables stop watch trigger by service request 0 event if ESWT = 1. 0_B Stop watch trigger by service request 0 disabled 1_B Service Request 0 event triggers stop watch
EINT1	6	rw	**Enable Service Request 1 Trigger** Enables stop watch trigger by service request 1 event if ESWT = 1. 0_B Stop watch trigger by service request 1 disabled 1_B Service Request 1 event triggers stop watch
SCCV	[13:8]	rh	**Stopped Cycle Counter Value** State of the cycle counter when the stop watch event occurred. Valid values are: $0…3F_H$ Valid Values
SMTV	[29:16]	rh	**Stopped Macrotick Value** State of the Macrotick counter when the stop watch event occurred. Valid values are: $0…3F_H$ Valid Values
0	7, [15:14], [31:30]	r	**Reserved** Returns 0 if read; should be written with 0.

Note: Bits ESWT and SSWT cannot be set to 1 simultaneously. In this case the write access is ignored, and both bits keep their previous values. Therefore either the external stop watch triggers or the software stop watch trigger may be used.

Stop Watch Register 2 (STPW2)

STPW2
Stop Watch Register 2 **(0050_H)** **Reset Value: $0000\ 0000_H$**



Field	Bits	Type	Description
SSCVA	[10:0]	rh	**Stop Watch Captured Slot Counter Value Channel A** State of the slot counter for channel A when the stop watch event occurred. Valid values are 0 to 2047 (0_H to $7FF_H$).
SSCVB	[26:16]	rh	**Stop Watch Captured Slot Counter Value Channel B** State of the slot counter for channel B when the stop watch event occurred. Valid values are 0 to 2047 (0_H to $7FF_H$).
0	[15:11], [31:27]	r	**Reserved** Returns 0 if read; should be written with 0.

26.5.2.4 Communication Controller Control Registers

This section describes the registers provided by the Communication Controller to allow the Host to control the operation of the Communication Controller. The FlexRay™ protocol specification requires the Host to write application configuration data in “CONFIG” state only. Please consider that the configuration registers are not locked for writing in “DEFAULT_CONFIG” state.

The configuration data is reset when “DEFAULT_CONFIG” state is entered from application reset. To change POC state from “DEFAULT_CONFIG” to “CONFIG” state the Host has to apply CHI command “CONFIG”. If the Host wants the Communication Controller to leave “CONFIG” state, the Host has to proceed as described on **“Lock Register (LCK)” on Page 26-39**.

SUC Configuration Register 1 (SUCC1)

SUCC1
SUC Configuration Register 1 (0080_H) Reset Value: $0C40\ 1080_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0				CCHB	CCHA	MTSB	MTSA	HCSE	TSM	WUCS	PTA				
r				rw	rw	rw	rw	rw	rw	rw	rw				

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CSA					0	TXSY	TXST	PBSY	0			CMD			
rw					r	rw	rw	rh	r			rwh			

Field	Bits	Type	Description
CMD	[3:0]	rwh	**CHI Command Vector** The host may write any CHI command at any time, but certain commands are only enabled in specific POC states. A disabled command will not be executed, the CHI command vector CMD will be reset to 0000_B = “COMMAND_NOT_ACCEPTED”, and flag EIR.CNA in the Error Service Request register will be set to 1. In case the previous CHI command has not yet completed, EIR.CCL is set to 1 together with EIR.CNA; the CHI command needs to be repeated. Except for HALT state, POC state change command applied while the Communication Controller is already in the requested POC state will be ignored. 0000_B COMMAND_NOT_ACCEPTED” 0001_B CONFIG 0010_B READY 0011_B WAKEUP 0100_B RUN 0101_B ALL_SLOTS 0110_B HALT 0111_B FREEZE 1000_B SEND_MTS 1001_B ALLOW_COLDSTART 1010_B RESET_STATUS_INDICATORS 1011_B MONITOR_MODE 1100_B CLEAR_RAMS 1101_B Reserved 1110_B Reserved 1111_B Reserved Reading SUCC1.CMD shows whether the last CHI command was accepted. CCSV.POCS monitors the actual POC state. The reserved CHI commands code hardware test functions.
PBSY	7	rh	**POC Busy** Signals that the POC is busy and cannot accept a command from the Host. SUCC1.CMD is locked against write accesses. Set to 1 after hard reset during initialization of internal RAM blocks. 0_B POC not busy, SUCC1.CMD writable 1_B POC is busy, SUCC1.CMD locked

Field	Bits	Type	Description
TXST	8	rw	**Transmit Startup Frame in Key Slot**[1) 2)] (pKeySlotUsedForStartup) Defines whether the key slot is used to transmit startup Frames. The bit can be modified in “DEFAULT_CONFIG” or “CONFIG” state only. 0_B No Startup Frame transmission in key slot, node is non-coldstarter 1_B Key slot used to transmit startup Frame, node is leading or following coldstarter
TXSY	9	rw	**Transmit SYNC Frame in Key Slot**[1) 2)] (pKeySlotUsedForSync) Defines whether the key slot is used to transmit SYNC Frames. The bit can be modified in “DEFAULT_CONFIG” or “CONFIG” state only. 0_B No SYNC Frame transmission in key slot, node is neither sync nor coldstart node 1_B Key slot used to transmit SYNC Frames, node is sync node
CSA	[15:11]	rw	**Cold Start Attempts**[1)](gColdStartAttempts) Configures the maximum number of attempts that a cold starting node is permitted to try to start up the network without receiving any valid response from another node. It can be modified in “DEFAULT_CONFIG” or “CONFIG” state only. Must be identical in all nodes of a cluster. Valid values are 2 to 31.
PTA	[20:16]	rw	**Passive to Active**[1)] (pAllowPassiveToActive) Defines the number of consecutive even / odd cycle pairs that must have valid clock correction terms before the Communication Controller is allowed to transit from “NORMAL_PASSIVE” to “NORMAL_ACTIVE” state. If set to 00000_B the Communication Controller is not allowed to transit from “NORMAL_PASSIVE” to “NORMAL_ACTIVE” state. It can be modified in “DEFAULT_CONFIG” or “CONFIG” state only. Valid values are 0 to 31 even / odd cycle pairs.

Field	Bits	Type	Description
WUCS	21	rw	**Wakeup Channel Select**[1] (pWakeupChannel) With this bit the Host selects the channel on which the Communication Controller sends the Wakeup pattern. The Communication Controller ignores any attempt to change the status of this bit when not in “DEFAULT_CONFIG” or “CONFIG” state. 0_B Send wakeup pattern on channel A 1_B Send wakeup pattern on channel B
TSM	22	rw	**Transmission Slot Mode**[1] (pSingleSlotEnabled) Selects the initial transmission slot mode. In SINGLE slot mode the Communication Controller may only transmit in the preconfigured key slot. The key slot ID is configured in the Header Section of Message Buffer 0 respectively Message Buffers 0 and 1 depending on bit MRC.SPLM. In case SUCC1.TSM = 1, Message Buffer 0 respectively Message Buffers 0,1 can be (re)configured in “DEFAULT_CONFIG” or “CONFIG” state only. In ALL slot mode the Communication Controller may transmit in all slots. The bit can be written in “DEFAULT_CONFIG” or “CONFIG” state only. The communication controller changes to ALL slot mode when the Host successfully applied the ALL_SLOTS command by writing SUCC1.CMD = 0101_B in POC states “NORMAL_ACTIVE” or “NORMAL_PASSIVE”. The actual slot mode is monitored by CCSV.SLM. 0_B ALL Slot Mode 1_B SINGLE Slot Mode (default after application reset)
HCSE	23	rw	**Halt due to Clock Sync Error**[1] (pAllowHaltDueToClock) Controls the transition to “HALT” state due to a clock synchronization error. The bit can be modified in “DEFAULT_CONFIG” or “CONFIG” state only. 0_B Communication Controller will enter / remain in “NORMAL_PASSIVE” 1_B Communication Controller will enter “HALT” state
MTSA	24	rw	**Select Channel A for MTS Transmission**[1] [3] The bit selects channel A for MTS symbol transmission. The flag is reset by default and may be modified only in “DEFAULT_CONFIG” or “CONFIG” state. 0_B Channel A disabled for MTS transmission 1_B Channel A selected for MTS transmission

Field	Bits	Type	Description
MTSB	25	rw	**Select Channel B for MTS Transmission**[1) 3)] The bit selects channel B for MTS symbol transmission. The flag is reset by default and may be modified only in "DEFAULT_CONFIG" or "CONFIG" state. 0_B Channel B disabled for MTS transmission 1_B Channel B selected for MTS transmission
CCHA	26	rw	**Connected to Channel A**[1)] (pChannels) Configures whether the node is connected to channel A. 0_B Not connected to channel A 1_B Node connected to channel A (default after application reset)
CCHB	27	rw	**Connected to Channel B**[1)] (pChannels) Configures whether the node is connected to channel B. 0_B Not connected to channel B 1_B Node connected to channel B (default after application reset)
0	[6:4], 10, [31:28]	r	**Reserved** Returns 0 if read; should be written with 0.

1) This bit can be updated in "DEFAULT_CONFIG" or "CONFIG" state only!

2) The protocol requires that both bits TXST and TXSY are set for coldstart nodes.

3) MTSA and MTSB may also be changed outside "DEFAULT_CONFIG" or "CONFIG" state when the write to SUCC1 register is directly preceded by the unlock sequence as described in Lock Register (LCK). This may be combined with CHI command "SEND_MTS". If both bits MTSA and MTSB are set to 1 an MTS symbol will be transmitted on both channels when requested by writing SUCC1.CMD = 1000_B.

COMMAND_NOT_ACCEPTED

SUCC1.CMD is reset to 0000_B due to one of the following conditions:

- Illegal command applied by the Host
- Host writes command_not_accepted
- Host applied new command while execution of the previous Host command has not completed

When SUCC1.CMD is reset to 0000_B, bit EIR.CNA in the Error Service Request register is set, and - if enabled - an service request is generated. Commands which are not accepted are not executed.

CONFIG

Go to POC state "CONFIG" when called in POC states "DEFAULT_CONFIG", "READY", or in "MONITOR_MODE". When called in "HALT" state transits to POC state

"DEFAULT_CONFIG". When called in any other state, SUCC1.CMD will be reset to 0000_B = "COMMAND_NOT_ACCEPTED".

READY

Go to POC state "READY" when called in POC states "CONFIG", "NORMAL_ACTIVE", "NORMAL_PASSIVE", "STARTUP", or "WAKEUP". When called in any other state, SUCC1.CMD will be reset to 0000_B = "COMMAND_NOT_ACCEPTED".

WAKEUP

Go to POC state WAKEUP when called in POC state "READY". When called in any other state, SUCC1.CMD will be reset to 0000_B = "COMMAND_NOT_ACCEPTED".

RUN

Go to POC state "STARTUP" when called in POC state "READY". When called in any other state, SUCC1.CMD will be reset to 0000_B = "COMMAND_NOT_ACCEPTED".

ALL_SLOTS

Leave SINGLE slot mode after successful startup / integration at the next end of cycle when called in POC states "NORMAL_ACTIVE" or "NORMAL_PASSIVE". When called in any other state, SUCC1.CMD will be reset to
0000_B = "COMMAND_NOT_ACCEPTED".

HALT

Set the halt request CCSV.HRQ bit in the Communication Controller Status Vector register and go to POC state "HALT" at the next end of cycle when called in POC states "NORMAL_ACTIVE" or "NORMAL_PASSIVE". When called in any other state, SUCC1.CMD will be reset to 0000_B = "COMMAND_NOT_ACCEPTED".

FREEZE

Set the freeze status indicator CCSV.FSI and go to POC state "HALT" immediately. Can be called from any state.

SEND_MTS

Send single MTS symbol during the next following symbol window on the channel configured by SUCC1.MTSA, SUCC1.MTSB, when called in POC state "NORMAL_ACTIVE". When called in any other state, SUCC1.CMD will be reset to 0000_B = "COMMAND_NOT_ACCEPTED".

ALLOW_COLDSTART

The command resets bit CCSV.CSI to enable the node to become cold starter. When called in states “DEFAULT_CONFIG“, “CONFIG”, “HALT”, or “MONITOR_MODE“. SUCC1.CMD will be reset to 0000_B = “COMMAND_NOT_ACCEPTED”. To become leading coldstarter it is also required that both TXST and TXSY are set.

RESET_STATUS_INDICATORS

Resets status flags CCSV.CSNI, CCSV.CSAI, CCSV.WSV to their default values. May be called in POC state READY. When called in any other state, SUCC1.CMD will be reset to 0000_B = “COMMAND_NOT_ACCEPTED”.

MONITOR_MODE

Enter MONITOR_MODE when called in POC state CONFIG. In this mode the Communication Controller is able to receive FlexRay™ Frames and wakeup pattern. It is also able to detect coding errors. The temporal integrity of received Frames is not checked. This mode can be used for debugging purposes, e.g. in case that the startup of a FlexRay™ network fails. When called in any other state, SUCC1.CMD will be reset to 0000_B = “COMMAND_NOT_ACCEPTED”. For details see **“MONITOR_MODE” on Page 26-208**.

CLEAR_RAMS

Sets bit MHDS.CRAM in the Message Handler Status register when called in “DEFAULT_CONFIG” or “CONFIG” state. When called in any other state, SUCC1.CMD will be reset to 0000_B = “COMMAND_NOT_ACCEPTED”. MHDS.CRAM is also set when the Communication Controller leaves application reset. By setting MHDS.CRAM all internal RAM blocks are initialized to zero. Note that only the currently active IBF bank is cleared. To clear the 2nd bank as well, CUST1.IBF1PAG and CUST1.IBF2PAG need to be set and command CLEAR_RAMS need to be issued again. This is required in particular after an application reset. If the 2nd bank of IBF is left unused, this procedure is not required. During the initialization of the RAMs, SUCC1.PBSY will show POC busy. Access to the configuration and status registers is possible during execution of CHI command CLEAR_RAMS.

The initialization of the E-Ray internal RAM blocks requires 2048 f_{CLC_ERAY} cycles. There should be no Host access to IBF or OBF during initialization of the internal RAM blocks after application reset or after assertion of CHI command CLEAR_RAMS. Before asserting CHI command CLEAR_RAMS the Host should make sure that no transfer between Message RAM and IBF / OBF or the Transient Buffer RAMs is ongoing. This command also resets the Message Buffer Status registers MHDS, LDTS, FSR, MHDF, TXRQ1, TXRQ2, TXRQ3, TXRQ4, NDAT1, NDAT2, NDAT3, NDAT4, MBSC1, MBSC2, MBSC3, and MBSC4.

Note: All accepted commands with exception of CLEAR_RAMS and SEND_MTS will cause a change of register CCSV after at most 8 cycles of the slower of the two clocks f_{CLC_ERAY} and f_{SCLK}, assumed that POC was not busy when the command was applied and that no POC state change was forced by bus activity in that time Frame. Reading register CCSV will show data that is delayed by synchronization from f_{SCLK} to f_{CLC_ERAY} domain and by the Host-specific CPU interface.

Table 26-4 below references the CHI commands from the FlexRay™ Protocol Specification v2.1 (section 2.2.1.1, Table 2-2) to the E-Ray CHI command vector CMD.]

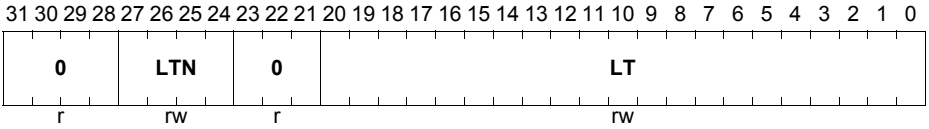
Table 26-4 Reference to CHI Host command summary from FlexRay™ protocol specification

CHI Command	Where processed (POC State)	CHI Command Vector CMD
ALL_SLOT	POC:NORMAL_ACTIVE, POC:NORMAL_PASSIVE	ALL_SLOTS
ALLOW_COLDSTART	All except POC:DEFAULT_CONFIG, POC:CONFIG, POC:HALT	ALLOW_COLDSTART
CONFIG	POC:DEFAULT_CONFIG, POC:READY	CONFIG
CONFIG_COMPLETE	POC:CONFIG	Unlock sequence & READY
DEFAULT_CONFIG	POC:HALT	CONFIG
FREEZE	All	FREEZE
HALT	POC:NORMAL_ACTIVE, POC:NORMAL_PASSIVE	HALT
READY	All except POC:DEFAULT_CONFIG, POC:CONFIG, POC:READY, POC:HALT	READY
RUN	POC:READY	RUN
WAKEUP	POC:READY	WAKEUP

SUC Configuration Register 2 (SUCC2)

The Communication Controller accepts modifications of the register in “DEFAULT_CONFIG” or “CONFIG” state only.

SUCC2
SUC Configuration Register 2 (0084_H) Reset Value: 0100 0504_H



Field	Bits	Type	Description
LT	[20:0]	rw	**Listen Timeout**[1] (pdListenTimeout) Configures wakeup / startup listen timeout in Microticks. The range for wakeup / startup listen timeout (pdListenTimeout) is 1284 to 1283846 (504_H to 139706_H) Microticks
LTN	[27:24]	rw	**Listen Time-out Noise**[1] (gListenNoise - 1) Configures the upper limit for startup and wakeup listen timeout in the presence of noise expressed as a multiple of the cluster constant pdListenTimeout. The range of pdListenTimeout 2 to 16. LTN must be configured identical in all nodes of a cluster. 1_H Listen Time-out Noise is equal 2 2_H Listen Time-out Noise is equal 3 $\cdots_H$ ... F_H Listen Time-out Noise is equal 16
0	[23:21], [31:28]	r	**Reserved** Returns 0 if read; should be written with 0.

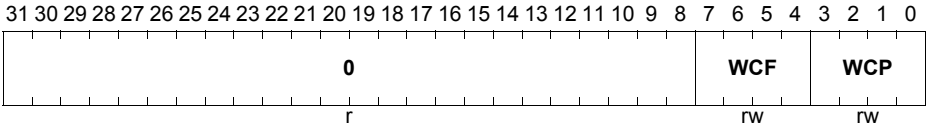
1) This bit can be updated in “DEFAULT_CONFIG” or “CONFIG” state only!

Note: The wakeup / startup noise time-out is calculated as follows:
The wakeup / startup noise time-out = pdListenTimeout • gListenNoise
= LT • (LTN+ 1)

SUC Configuration Register 3 (SUCC3)

The Communication Controller accepts modifications of the register in “DEFAULT_CONFIG” or “CONFIG” state only.

SUCC3
SUC Configuration Register 3 (0088_H) Reset Value: $0000\ 0011_H$



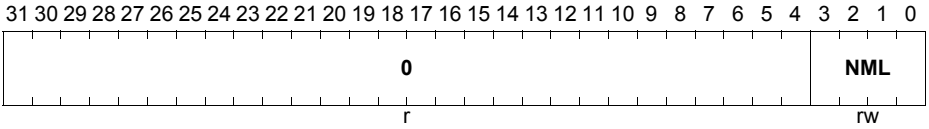
Field	Bits	Type	Description
WCP	[3:0]	rw	**Maximum Without Clock Correction Passive**[1)] (gMaxWithoutClockCorrectionPassive) Defines the number of consecutive even / odd cycle pairs with missing clock correction terms that will cause a transition from “NORMAL_ACTIVE” to “NORMAL_PASSIVE” state. Must be identical in all nodes of a cluster. Valid values are 1 to 15 (1_H to F_H) cycle pairs.
WCF	[7:4]	rw	**Maximum Without Clock Correction Fatal**[1)] (gMaxWithoutClockCorrectionFatal) Defines the number of consecutive even / odd cycle pairs with missing clock correction terms that will cause a transition from “NORMAL_ACTIVE” or “NORMAL_PASSIVE” to “HALT” state. Must be identical in all nodes of a cluster. Valid values are 1 to 15 (1_H to F_H)cycle pairs.
0	[31:8]	r	**Reserved** Returns 0 if read; should be written with 0.

1) This bit can be updated in “DEFAULT_CONFIG” or “CONFIG” state only!

NEM Configuration Register (NEMC)

The Communication Controller accepts modifications of the register in “DEFAULT_CONFIG” or “CONFIG” state only.

NEMC
NEM Configuration Register (008C$_H$) Reset Value: 0000 0000$_H$



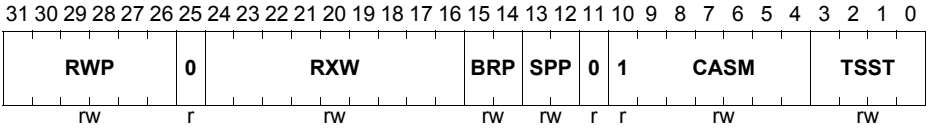
Field	Bits	Type	Description
NML	[3:0]	rw	**Network Management Vector Length**[1)] (gNetworkManagementVectorLength) These bits configure the length of the NM Vector. The configured length must be identical in all nodes of a cluster. Valid values are 0 to 12 (0_H to C_H) bytes.
0	[31:4]	r	**Reserved** Returns 0 if read; should be written with 0.

1) This bit can be updated in “DEFAULT_CONFIG” or “CONFIG” state only!

PRT Configuration Register 1 (PRTC1)

The Communication Controller accepts modifications of the register in “DEFAULT_CONFIG” or “CONFIG” state only.

PRTC1
PRT Configuration Register 1 (0090_H) Reset Value: $084C\ 0633_H$



Field	Bits	Type	Description
TSST	[3:0]	rw	**Transmission Start Sequence Transmitter**[1)] (gdTSSTransmitter) Configures the duration of the Transmission Start Sequence (TSS) in terms of Bit Times (1 bit time = 4 Microticks = 100ns at 10Mbps). Must be identical in all nodes of a cluster. Valid values are 3 to 15 (3_H to F_H) Bit Times.
CASM	[10:4]	rw	**Collision Avoidance Symbol Maximum**[1)] (gdCASRxLowMax) Configures the upper limit of the acceptance window for a collision avoidance symbol (CAS). Valid values are 67 to 99 (43_H to 63_H). Most significant bit of CASM is hard wired to 1 and can not be modified.
SPP	[13:12]	rw	**Strobe Point Position**[1)] Defines the sample count value for strobing. The strobed bit value is set to the voted value when the sample count is incremented to the value configured by SPP. 00_B Sample 5 (default) 01_B Sample 4 10_B Sample 6 11_B Reserved; should not be used. *Note: The current revision 2.1 of the FlexRay™ protocol requires that SPP = 00_B. The alternate strobe point positions could be used to compensate for asymmetries in the physical layer.*

Field	Bits	Type	Description
BRP	[15:14]	rw	**Baud Rate Prescaler**[1] (gdSampleClockPeriod, pSamplePerMicrotick) The baud rate prescaler configures the baud rate on the FlexRay™ bus. The baud rates listed below are valid with a sample clock f_{SCLK}= 80 MHz. One bit time always consists of 8 samples independent of the configured baud rate. 00_B 10 Mbit/s (1 Microtick= 25 ns; twice sampled with f_{SCLK}) gdSampleClockPeriod = 12.5 ns = 1 / f_{SCLK} pSamplesPerMicrotick = 2 01_B 5 Mbit/s (1 Microtick= 25ns; single sampled with f_{SCLK} / 2) gdSampleClockPeriod = 25 ns = 2 / f_{SCLK} pSamplesPerMicrotick = 1 10_B 2.5 Mbit/s (1 Microtick = 50ns; single sampled with f_{SCLK} / 4) gdSampleClockPeriod = 50 ns = 4 / f_{SCLK} pSamplesPerMicrotick = 1 11_B Reserved; should not be used (2.5 Mbit/s (1 Microtick = 50 ns; single sampled with f_{SCLK} / 4) gdSampleClockPeriod = 50 ns = 4 / f_{SCLK} pSamplesPerMicrotick = 1
RXW	[24:16]	rw	**Wakeup Symbol Receive Window Length**[1] (gdWakeupSymbolRxWindow**)** Configures the number of Bit Times used by the node to test the duration of the received wakeup pattern. Must be identical in all nodes of a cluster. Valid values are 76 to 301 ($4C_H$ to $12D_H$) Bit Times.
RWP	[31:26]	rw	**Repetitions of Tx Wakeup Pattern**[1] (pWakeupPattern) Configures the number of repetitions (sequences) of the Tx wakeup symbol. Valid values are 2 to 63 (2_H to $3F_H$).
0	11, 25	r	**Reserved** Returns 0 if read; should be written with 0.

1) This bit can be updated in “DEFAULT_CONFIG” or “CONFIG” state only!

PRT Configuration Register 2 (PRTC2)

The Communication Controller accepts modifications of the register in “DEFAULT_CONFIG” or “CONFIG” state only.

PRTC2
PRT Configuration Register 2 (0094_H) Reset Value: $0F2D\ 0A0E_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0				TXL							TXI					0				RXL						0				RXI		
r				rw							rw					r				rw						r				rw		

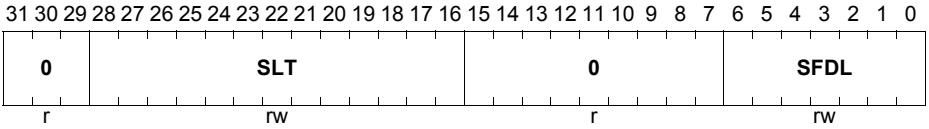
Field	Bits	Type	Description
RXI	[5:0]	rw	**Wakeup Symbol Receive Idle**[1)] (gdWakeupSymbolRxIdle) Configures the number of Bit Times used by the node to test the duration of the idle phase of the received wakeup symbol. Must be identical in all nodes of a cluster. Valid values are 14 to 59 (E_H to $3B_H$) Bit Times.
RXL	[13:8]	rw	**Wakeup Symbol Receive Low**[1)] (gdWakeupSymbolRxLow) Configures the number of Bit Times used by the node to test the duration of the low phase of the received wakeup symbol. Must be identical in all nodes of a cluster. Valid values are 10 to 55 (A_H to 37_H) Bit Times.
TXI	[23:16]	rw	**Wakeup Symbol Transmit Idle**[1)] (gdWakeupSymbolTxIdle) Configures the number of Bit Times used by the node to transmit the idle phase of the wakeup symbol. Must be identical in all nodes of a cluster. Valid values are 45 to 180 ($2D_H$ to $B4_H$)Bit Times.
TXL	[29:24]	rw	**Wakeup Symbol Transmit Low**[1)] (gdWakeupSymbolTxLow) Configures the number of Bit Times used by the node to transmit the low phase of the wakeup symbol. Must be identical in all nodes of a cluster. Valid values are 15 to 60 (F_H to $3C_H$) Bit Times.
0	[7:6], [15:14], [31:30]	r	**Reserved** Returns 0 if read; should be written with 0.

1) This bit can be updated in “DEFAULT_CONFIG” or “CONFIG” state only!

MHD Configuration Register (MHDC)

The Communication Controller accepts modifications of the register in “DEFAULT_CONFIG” or “CONFIG” state only.

MHDC
MHD Configuration Register **(0098_H)** **Reset Value: $0000\ 0000_H$**



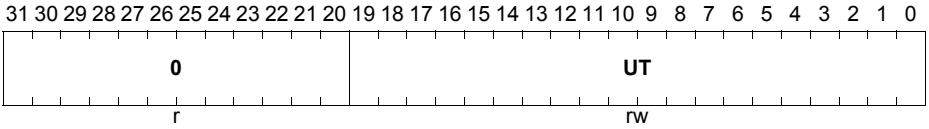
Field	Bits	Type	Description
SFDL	[6:0]	rw	**Static Frame Data Length** (gPayloadLengthStatic)[1)] Configures the cluster-wide payload length for all Frames sent in the static segment in double byte. The payload length must be identical in all nodes of a cluster. Valid values are 0 to 127 (0 to $7F_H$).
SLT	[28:16]	rw	**Start of Latest Transmit** (pLatestTx)[1)] Configures the maximum minislot value allowed before inhibiting Frame transmission in the dynamic segment of the cycle. There is no transmission dynamic segment if SLT is reset to zero. Valid values are 0 to 7981 (0 to $1F2D_H$) minislots.
0	[15:7], [31:29]	r	**Reserved** Returns 0 if read; should be written with 0.

1) This bit can be updated in “DEFAULT_CONFIG” or “CONFIG” state only!

GTU Configuration Register 1 (GTUC01)

The Communication Controller accepts modifications of the register in “DEFAULT_CONFIG” or “CONFIG” state only.

GTUC01
GTU Configuration Register 1 ($00A0_H$) Reset Value: $0000\ 0280_H$



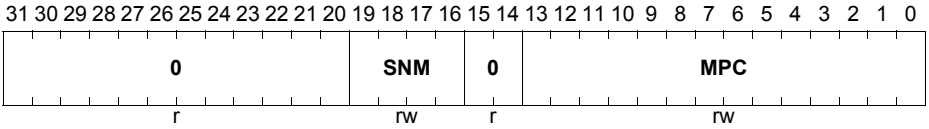
Field	Bits	Type	Description
UT	[19:0]	rw	**Microtick per Cycle** (pMicroPerCycle)[1)] Configures the duration of the communication cycle in Microticks. Valid values are 640 to 640000 (280_H to $9C400_H$) Microticks.
0	[31:20]	r	**Reserved** Returns 0 if read; should be written with 0.

1) This bit can be updated in “DEFAULT_CONFIG” or “CONFIG” state only!

GTU Configuration Register 2 (GTUC02)

The Communication Controller accepts modifications of the register in “DEFAULT_CONFIG” or “CONFIG” state only.

GTUC02
GTU Configuration Register 2 ($00A4_H$) Reset Value: $0002\ 000A_H$



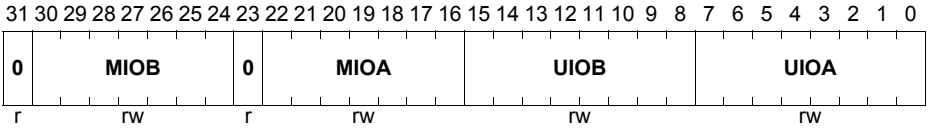
Field	Bits	Type	Description
MPC	[13:0]	rw	**Macrotick Per Cycle** (gMacroPerCycle)[1)] Configures the duration of one communication cycle in Macroticks. The cycle length must be identical in all nodes of a cluster. Valid values are 10 to 16000 (A_H to $3E80_H$) Macroticks.
SNM	[19:16]	rw	**Sync Node Max** (gSyncNodeMax)[1)] Maximum number of Frames within a cluster with SYNC Frame indicator bit SYN set to 1. Must be identical in all nodes of a cluster. Valid values are 2 to 15 (2_H to F_H).
0	[15:14], [31:20]	r	**Reserved** Returns 0 if read; should be written with 0.

1) This bit can be updated in “DEFAULT_CONFIG” or “CONFIG” state only!

GTU Configuration Register 3 (GTUC03)

The Communication Controller accepts modifications of the register in “DEFAULT_CONFIG” or “CONFIG” state only.

GTUC03
GTU Configuration Register 3 (00A8$_H$) Reset Value: 0202 0000$_H$



Field	Bits	Type	Description
UIOA	[7:0]	rw	**Microtick Initial Offset Channel A**[1)] (pMicroInitialOffset[A]) Configures the number of Microticks between the actual time reference point on channel A and the subsequent Macrotick boundary of the secondary time reference point. The parameter depends on pDelayCompensation[A] and therefore has to be set for each channel independently. Valid values are 0 to 240 (0_H to $F0_H$) Microticks.
UIOB	[15:8]	rw	**Microtick Initial Offset Channel B**[1)] (pMicroInitialOffset[B]) Configures the number of Microticks between the actual time reference point on channel B and the subsequent Macrotick boundary of the secondary time reference point. The parameter depends on pDelayCompensation[B] and therefore has to be set for each channel independently. Valid values are 0 to 240 (0_H to $F0_H$) Microticks.
MIOA	[22:16]	rw	**Macrotick Initial Offset Channel A** (gMacroInitialOffset[A])[1)] Configures the number of Macroticks between the static slot boundary and the subsequent Macrotick boundary of the secondary time reference point based on the nominal Macrotick duration. Must be identical in all nodes of a cluster. Valid values are 2 to 72 (2_H to 48_H) Macroticks.
MIOB	[30:24]	rw	**Macrotick Initial Offset Channel B** (gMacroInitialOffset[B])[1)] Configures the number of Macroticks between the static slot boundary and the subsequent Macrotick boundary of the secondary time reference point based on the nominal Macrotick duration. Must be identical in all nodes of a cluster. Valid values are 2 to 72 (2_H to 48_H) Macroticks.

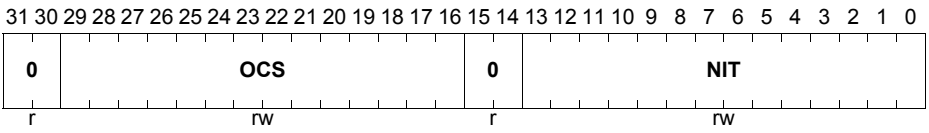
Field	Bits	Type	Description
0	23, 31	r	**Reserved** Returns 0 if read; should be written with 0.

1) This bit can be updated in “DEFAULT_CONFIG” or “CONFIG” state only!

GTU Configuration Register 4 (GTUC04)

The Communication Controller accepts modifications of the register in “DEFAULT_CONFIG” or “CONFIG” state only. For details about configuration of NIT and OCS see **“Configuration of Network Idle Time (NIT) Start and Offset Correction Start” on Page 26-197**.

GTUC04
GTU Configuration Register 4 (00AC$_H$) Reset Value: 0008 0007$_H$



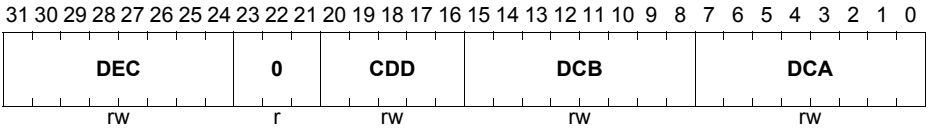
Field	Bits	Type	Description
NIT	[13:0]	rw	**Network Idle Time Start** [1] (gMacroPerCycle - gdNIT - 1) Configures the starting point of the Network Idle Time (NIT) at the end of the communication cycle expressed in terms of Macroticks from the beginning of the cycle. The start of network idle time (NIT) is recognized if Macrotick = gMacroPerCycle - gdNIT -1 and the increment pulse of Macrotick is set. Must be identical in all nodes of a cluster. Valid values are 7 to 15997 (7_H to $3E7D_H$) Macroticks.
OCS	[29:16]	rw	**Offset Correction Start**[1] (gOffsetCorrectionStart - 1) Determines the start of the offset correction within the network idle time (NIT) phase, calculated from start of cycle. Must be identical in all nodes of a cluster. For cluster consisting of E-Ray implementations only, it is sufficient to program OCS = NIT + 1. Valid values are 8 to 15998 (8_H to $3E7E_H$) Macroticks.
0	[15:14], [31:30]	r	**Reserved** Returns 0 if read; should be written with 0.

1) This bit can be updated in “DEFAULT_CONFIG” or “CONFIG” state only!

GTU Configuration Register 5 (GTUC05)

The Communication Controller accepts modifications of the register in “DEFAULT_CONFIG” or “CONFIG” state only.

GTUC05
GTU Configuration Register 5 ($00B0_H$) **Reset Value: $0E00\ 0000_H$**



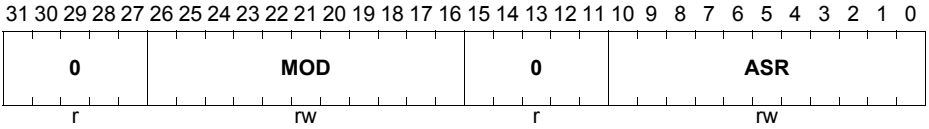
Field	Bits	Type	Description
DCA	[7:0]	rw	**Delay Compensation Channel A**[1] (pDelayCompensation[A]) Used to compensate for reception delays on channel A. This covers assumed propagation delay up to cPropagationDelayMax for Microticks in the range of 0.0125µs to 0.05µs. In practice, the minimum of the propagation delays of all sync nodes should be applied. Valid values are 0 to 200 (0_H to $C8_H$) Microticks.
DCB	[15:8]	rw	**Delay Compensation Channel B**[1] (pDelayCompensation[B]) Used to compensate for reception delays on channel B. This covers assumed propagation delay up to cPropagationDelayMax for Microticks in the range of 0.0125 to 0.05µs. In practice, the minimum of the propagation delays of all sync nodes should be applied. Valid values are 0 to 200 (0_H to $C8_H$) Microticks.
CDD	[20:16]	rw	**Cluster Drift Damping** (pClusterDriftDamping)[1] Configures the cluster drift damping value used in clock synchronization to minimize accumulation of rounding errors. Valid values are 0 to 20 (0_H to 14_H) Microticks.
DEC	[31:24]	rw	**Decoding Correction** (pDecodingCorrection)[1] Configures the decoding correction value used to determine the primary time reference point. Valid values are 14 to 143 (E_H to $8F_H$) Microticks.
0	[23:21]	r	**Reserved** Returns 0 if read; should be written with 0.

1) This bit can be updated in “DEFAULT_CONFIG” or “CONFIG” state only!

GTU Configuration Register 6 (GTUC06)

The Communication Controller accepts modifications of the register in “DEFAULT_CONFIG” or “CONFIG” state only.

GTUC06
GTU Configuration Register 6 (00B4$_H$) Reset Value: 0002 0000$_H$



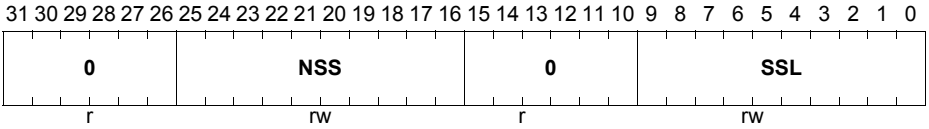
Field	Bits	Type	Description
ASR	[10:0]	rw	**Accepted Startup Range**[1] (pdAcceptedStartupRange) Number of Microticks constituting the expanded range of measured deviation for startup Frames during integration. Valid values are 0 to 1875 (0_H to 753_H) Microticks.
MOD	[26:16]	rw	**Maximum Oscillator Drift** (pdMaxDrift)[1] Maximum drift offset between two nodes that operate with unsynchronized clocks over one communication cycle in Microticks. Valid values are 2 to 1923 (2_H to 783_H) Microticks.
0	[15:11], [31:27]	r	**Reserved** Returns 0 if read; should be written with 0.

1) This bit can be updated in “DEFAULT_CONFIG” or “CONFIG” state only!

GTU Configuration Register 7 (GTUC07)

The Communication Controller accepts modifications of the register in “DEFAULT_CONFIG” or “CONFIG” state only.

GTUC07
GTU Configuration Register 7 (00B8$_H$) Reset Value: 0002 0004$_H$



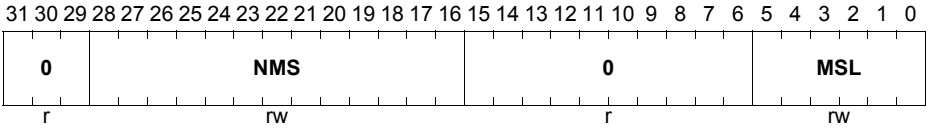
Field	Bits	Type	Description
SSL	[9:0]	rw	**Static Slot Length** (gdStaticSlot)[1)] Configures the duration of a static slot in Macroticks. The static slot length must be identical in all nodes of a cluster. Valid values are 4 to 659 (4_H to 293_H) Macroticks.
NSS	[25:16]	rw	**Number of Static Slots** (gNumberOfStaticSlots)[1)] Configures the number of static slots in a cycle. At least 2 coldstart nodes must be configured to startup a FlexRay™ network. The number of static slots must be identical in all nodes of a cluster. Valid values are 2 to 1023 (2_H to $3FF_H$).
0	[15:10], [31:26]	r	**Reserved** Returns 0 if read; should be written with 0.

1) This bit can be updated in “DEFAULT_CONFIG” or “CONFIG” state only!

GTU Configuration Register 8 (GTUC08)

The Communication Controller accepts modifications of the register in “DEFAULT_CONFIG” or “CONFIG” state only.

GTUC08
GTU Configuration Register 8 (00BC$_H$) Reset Value: 0000 0002$_H$



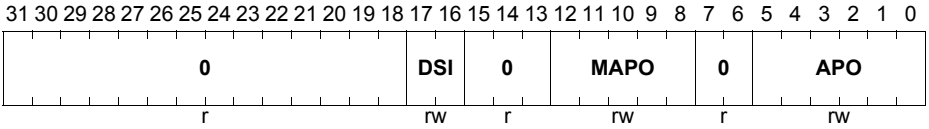
Field	Bits	Type	Description
MSL	[5:0]	rw	**Minislot Length** (gdMinislot)[1)] Configures the duration of a minislot in Macroticks. The minislot length must be identical in all nodes of a cluster. Valid values are 2 to 63 (2_H to $3F_H$) Macroticks.
NMS	[28:16]	rw	**Number of Minislots** (gNumberOfMinislots)[1)] Configures the number of minislots within the dynamic segment of a cycle. The number of minislots must be identical in all nodes of a cluster. Valid values are 0 to 7986 (0_H to $1F32_H$).
0	[15:6], [31:29]	r	**Reserved** Returns 0 if read; should be written with 0.

1) This bit can be updated in “DEFAULT_CONFIG” or “CONFIG” state only!

GTU Configuration Register 9 (GTUC09)

The Communication Controller accepts modifications of the register in “DEFAULT_CONFIG” or “CONFIG” state only.

GTUC09
GTU Configuration Register 9 ($00C0_H$) Reset Value: $0000\ 0101_H$



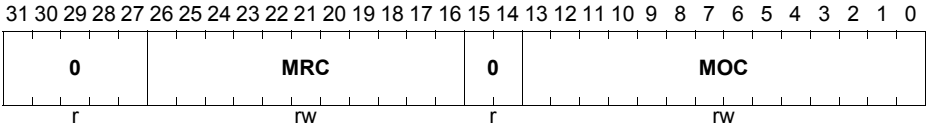
Field	Bits	Type	Description
APO	[5:0]	rw	**Action Point Offset** (gdActionPointOffset)[1)] Configures the action point offset in Macroticks within static slots and symbol window. Must be identical in all nodes of a cluster. Valid values are 1 to 63 (1_H to $3F_H$) Macroticks.
MAPO	[12:8]	rw	**Minislot Action Point Offset**[1)] (gdMinislotActionPointOffset) Configures the action point offset in Macroticks within the minislots of the dynamic segment. Must be identical in all nodes of a cluster. Valid values are 1 to 31 (1_H to $1F_H$) Macroticks.
DSI	[17:16]	rw	**Dynamic Slot Idle Phase**[1)] (gdDynamicSlotIdlePhase) The duration of the dynamic slot idle phase has to be greater or equal than the idle detection time. Must be identical in all nodes of a cluster. Valid values are 0 to 2 Minislot.
0	[7:6], [15:13], [31:18]	r	**Reserved** Returns 0 if read; should be written with 0.

1) This bit can be updated in “DEFAULT_CONFIG” or “CONFIG” state only!

GTU Configuration Register 10 (GTUC10)

The Communication Controller accepts modifications of the register in “DEFAULT_CONFIG” or “CONFIG” state only.

GTUC10
GTU Configuration Register 10 (00C4$_H$) Reset Value: 0002 0005$_H$

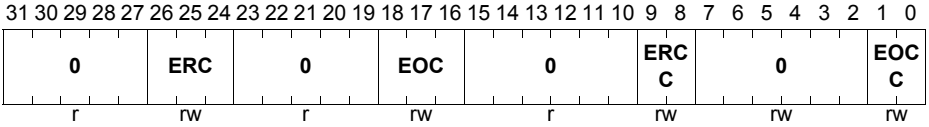


Field	Bits	Type	Description
MOC	[13:0]	rw	**Maximum Offset Correction**[1)] (pOffsetCorrectionOut) Holds the maximum permitted offset correction value to be applied by the internal clock synchronization algorithm (absolute value). The Communication Controller checks only the internal offset correction value against the maximum offset correction value. Valid values are 5 to 15266 (5_H to $3BA2_H$) Microticks.
MRC	[26:16]	rw	**Maximum Rate Correction**[1)] (pRateCorrectionOut) Holds the maximum permitted rate correction value to be applied by the internal clock synchronization algorithm. The communication controller checks only the internal rate correction value against the maximum rate correction value (absolute value). Valid values are 2 to 1923 (2_H to 783_H) Microticks.
0	[15:14], [31:27]	r	**Reserved** Returns 0 if read; should be written with 0.

1) This bit can be updated in “DEFAULT_CONFIG” or “CONFIG” state only!

GTU Configuration Register 11 (GTUC11)

GTUC11
GTU Configuration Register 11 ($00C8_H$) **Reset Value: $0000\ 0000_H$**



Field	Bits	Type	Description
EOCC	[1:0]	rw	**External Offset Correction Control** (pExternOffsetControl) By writing to EOCC the external offset correction is enabled as specified below. Should be modified only outside network idle time (NIT). 00_B No external clock correction 01_B No external clock correction 10_B External offset correction value subtracted from calculated offset correction value 11_B External offset correction value added to calculated offset correction value
ERCC	[9:8]	rw	**External Rate Correction Control** (pExternRateControl) By writing to ERCC the external rate correction is enabled as specified below. Should be modified only outside network idle time (NIT). 00_B No external rate correction 01_B No external rate correction 10_B External rate correction value subtracted from calculated rate correction value 11_B External rate correction value added to calculated rate correction value
EOC	[18:16]	rw	**External Offset Correction**[1)] (pExternOffsetCorrection) Holds the external clock offset correction value in Microticks to be applied by the internal synchronization algorithm. The value is subtracted / added from / to the calculated offset correction value. The value is applied during network idle time (NIT). May be modified in “DEFAULT_CONFIG” or “CONFIG” state only. Valid values are 0 to 7 Microticks.

Field	Bits	Type	Description
ERC	[26:24]	rw	**External Rate Correction**[1] (pExternRateCorrection) Holds the external rate correction value in Microticks to be applied by the internal clock synchronization algorithm. The value is subtracted / added from / to the calculated rate correction value. The value is applied during network idle time (NIT). May be modified in “DEFAULT_CONFIG” or “CONFIG” state only. Valid values are 0 to 7 Microticks.
0	[7:2], [15:10], [23:19], [31:27]	r	**Reserved** Returns 0 if read; should be written with 0.

1) This bit can be updated in “DEFAULT_CONFIG” or “CONFIG” state only!

26.5.2.5 Communication Controller Status Registers

During 8/16-bit accesses to status variables coded with more than 8/16-bit, the variable might be updated by the Communication Controller between two accesses (non-atomic read accesses). The status vector may change faster than the Host can poll the status vector, depending on f_{CLC_ERAY} frequency.

Communication Controller Status Vector (CCSV)

CCSV

Communication Controller Status Vector(0100_H) **Reset Value: $0010\ 4000_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0		PSL						RCA					WSV		
r		rh						rh					rh		

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	CSI	CSAI	CSNI	0		SLM		HRQ	FSI	POCS					
r	rh	rh	rh	r		rh		rh	rh	rh					

Field	Bits	Type	Description
POCS	[5:0]	rh	**Protocol Operation Control Status** Indicates the actual state of operation of the Communication Controller Protocol Operation Control 000000_B “DEFAULT_CONFIG” state 000001_B “READY” state 000010_B “NORMAL_ACTIVE” state 000011_B “NORMAL_PASSIVE” state 000100_B “HALT” state 000101_B “MONITOR_MODE” state 000110_B … 001110_B are reserved. 001111_B “CONFIG” state Indicates the actual state of operation of the POC in the wakeup path 010000_B WAKEUP_STANDBY state 010001_B “WAKEUP_LISTEN” state 010010_B “WAKEUP_SEND” state 010011_B “WAKEUP_DETECT” state 010100_B … 011111_B are reserved. Indicates the actual state of operation of the POC in the startup path 100000_B “STARTUP_PREPARE” state 100001_B “COLDSTART_LISTEN” state 100010_B “COLDSTART_COLLISION_RESOLUTION state 100011_B “COLDSTART_CONSISTENCY_CHECK” state 100100_B “COLDSTART_GAP state 100101_B “COLDSTART_JOIN” State 100110_B “INTEGRATION_COLDSTART_CHECK” state 100111_B “INTEGRATION_LISTEN” state 101000_B “INTEGRATION_CONSISTENCY_CHECK” state 101001_B “INITIALIZE_SCHEDULE” state 101010_B “ABORT_STARTUP” state 101011_B “STARTUP_SUCCESS” state 101100_B … 111111_B are reserved.

Field	Bits	Type	Description
FSI	6	rh	**Freeze Status Indicator** (vPOC!Freeze**)** Indicates that the POC has entered the “HALT” state due to CHI command “FREEZE” or due to an error condition requiring an immediate POC halt. Reset by transition from “HALT” to “DEFAULT_CONFIG” state.
HRQ	7	rh	**Halt Request** (vPOC!CHIHaltRequest) Indicates that a request from the Host has been received to halt the POC at the end of the communication cycle. Reset by transition from “HALT” to “DEFAULT_CONFIG” state or when entering “READY” state.
SLM	[9:8]	rh	**Slot Mode** (vPOC!SlotMode) Indicates the actual slot mode of the POC in states READY, WAKEUP, STARTUP, NORMAL_ACTIVE, and NORMAL_PASSIVE. Default is “SINGLE”. Changes to “ALL”, depending on configuration bit SUCC1.TSM. In “NORMAL_ACTIVE” or “NORMAL_PASSIVE” state the CHI command “ALL_SLOTS” will change the slot mode from “SINGLE” over “ALL_PENDING” to “ALL”. Set to SINGLE in all other states. 00_B SINGLE 01_B Reserved 10_B ALL_PENDING 11_B ALL
CSNI	12	rh	**Coldstart Noise Indicator** (vPOC!ColdstartNoise) Indicates that the cold start procedure occurred under noisy conditions. Reset by CHI command “RESET_STATUS_INDICATORS” or by transition from “HALT” to “DEFAULT_CONFIG” state or from “READY” to “STARTUP” state.
CSAI	13	rh	**Coldstart Abort Indicator** Coldstart aborted. Reset by CHI command “RESET_STATUS_INDICATORS” or by transition from “HALT” to “DEFAULT_CONFIG” state or from “READY” to “STARTUP” state.

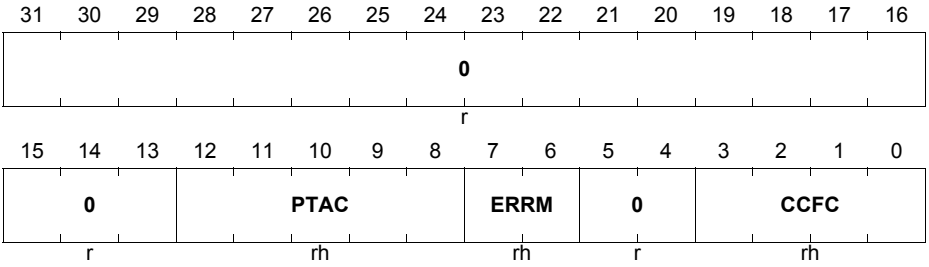
Field	Bits	Type	Description
CSI	14	rh	**Cold Start Inhibit** (vColdStartInhibit) Indicates that the node is disabled from cold starting. The flag is set whenever the POC enters “READY” state due to CHI command “READY”. The flag has to be reset under control of the Host by CHI command “ALLOW_COLDSTART” (SUCC1.CMD = 1001_B). 0_B Cold starting of node enabled 1_B Cold starting of node disabled
WSV	[18:16]	rh	**Wakeup Status** (vPOC!WakeupStatus) Indicates the status of the current wakeup attempt. Reset by CHI command “RESET_STATUS_INDICATORS” or by transition from “HALT” to “DEFAULT_CONFIG” state. 000_B UNDEFINED. Wakeup not yet executed by the Communication Controller. 001_B RECEIVED_HEADER. Set when the Communication Controller finishes wakeup due to the reception of a Frame Header without coding violation on either channel in “WAKEUP_LISTEN” state. 010_B RECEIVED_WUP. Set when the Communication Controller finishes wakeup due to the reception of a valid wakeup pattern on the configured wakeup channel in “WAKEUP_LISTEN” state. 011_B COLLISION_HEADER. Set when the Communication Controller stops wakeup due to a detected collision during wakeup pattern transmission by receiving a valid Header on either channel. 100_B COLLISION_WUP. Set when the Communication Controller stops wakeup due to a detected collision during wakeup pattern transmission by receiving a valid wakeup pattern on the configured wakeup channel. 101_B COLLISION_UNKNOWN. Set when the Communication Controller stops wakeup by leaving “WAKEUP_DETECT” state after expiration of the wakeup timer without receiving a valid wakeup pattern or a valid Frame Header. 110_B TRANSMITTED. Set when the Communication Controller has successfully completed the transmission of the wakeup pattern. 111_B Reserved

Field	Bits	Type	Description
RCA	[23:19]	rh	**Remaining Coldstart Attempts** (vRemainingColdstartAttempts) Indicates the number of remaining coldstart attempts. The RUN command resets this counter to the maximum number of coldstart attempts as configured by SUCC1.CSA.
PSL	[29:24]	rh	**POC Status Log** Status of CCSV.POCS immediately before entering “HALT” state. Set when entering “HALT” state. Set to “HALT” when FREEZE command is applied during “HALT” state. Reset to 000000_B when leaving “HALT” state.
0	[11:10], 15, [31:30]	rh	**Reserved** Returns 0 if read; should be written with 0.

Communication Controller Error Vector (CCEV)

Reset by transition from “HALT” to “DEFAULT_CONFIG” state or when entering “READY” state.

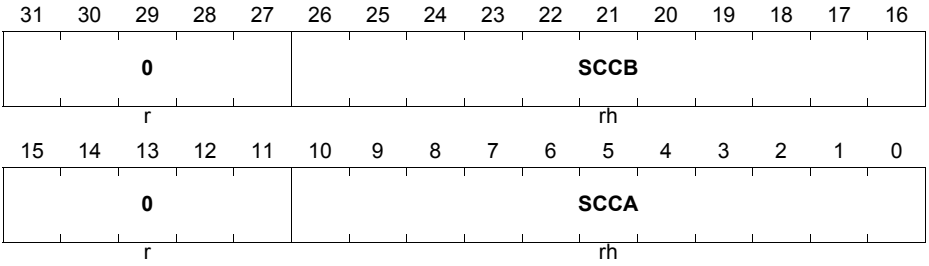
CCEV
Communication Controller Error Vector (0104_H) **Reset Value: $0000\ 0000_H$**



Field	Bits	Type	Description
CCFC	[3:0]	rh	**Clock Correction Failed Counter** (vClockCorrectionFailed) The Clock Correction Failed Counter is incremented by one at the end of any odd communication cycle where either the missing offset correction error or missing rate correction error are active. The Clock Correction Failed Counter is reset to 0 at the end of an odd communication cycle if neither the offset correction failed nor the rate correction failed errors are active. The Clock Correction Failed Counter stops at 15.
ERRM	[7:6]	rh	**Error Mode** (vPOC!ErrorMode) Indicates the actual error mode of the POC. 00_B “ACTIVE” (green) 01_B “PASSIVE” (yellow) 10_B “COMM_HALT” (red) 11_B Reserved
PTAC	[12:8]	rh	**Passive to Active Count** (vAllowPassiveToActive) Indicates the number of consecutive even / odd cycle pairs that have passed with valid rate and offset correction terms, while the node is waiting to transit from “NORMAL_PASSIVE” state to “NORMAL_ACTIVE” state. The transition takes place when PTAC equals SUCC1.PTA.
0	[5:4], [31:13]	r	**Reserved** Returns 0 if read; should be written with 0.

Slot Counter Value (SCV)

SCV
Slot Counter Value **(0110_H)** **Reset Value: $0000\ 0000_H$**

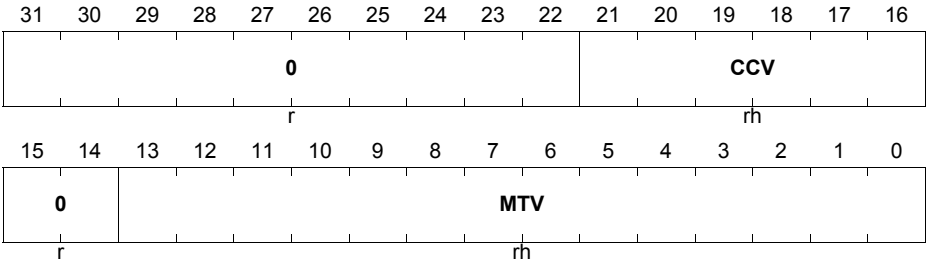


Field	Bits	Type	Description
SCCA	[10:0]	rh	**Slot Counter Channel A** (vSlotCounter[A]**)** Current slot counter value on channel A. The value is incremented by the Communication Controller and reset at the start of a communication cycle. Valid values are 0 to 2047 (0_H to $7FD_H$).
SCCB	[26:16]	rh	**Slot Counter Channel B** (vSlotCounter[B]**)** Current slot counter value on channel B. The value is incremented by the Communication Controller and reset at the start of a communication cycle. Valid values are 0 to 2047 (0_H to $7FD_H$).
0	[15:11], [31:27]	r	**Reserved** Returns 0 if read; should be written with 0.

Macrotick and Cycle Counter Value (MTCCV)

MTCCV

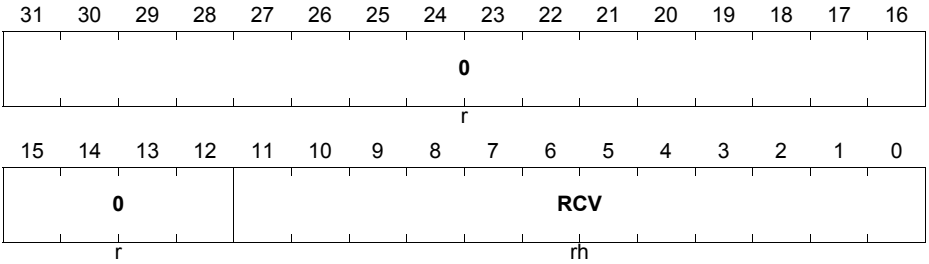
Macrotick and Cycle Counter Value (0114_H) **Reset Value: $0000\ 0000_H$**



Field	Bits	Type	Description
MTV	[13:0]	rh	**Macrotick Value** (vMacrotick) Current Macrotick value. The value is incremented by the Communication Controller and reset at the start of a communication cycle. Valid values are 0 to 16000 (0_H to $3E80_H$).
CCV	[21:16]	rh	**Cycle Counter Value** (vCycleCounter) Current cycle counter value. The value is incremented by the Communication Controller at the start of a communication cycle. Valid values are 0 to 63 (0_H to $3F_H$).
0	[15:14], [31:22]	r	**Reserved** Returns 0 if read; should be written with 0.

Rate Correction Value (RCV)

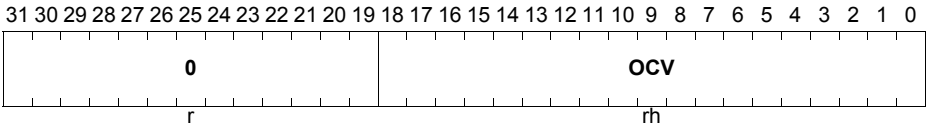
RCV
Rate Correction Value **(0118_H)** **Reset Value: $0000\ 0000_H$**



Field	Bits	Type	Description
RCV	[11:0]	rh	**Rate Correction Value** (vRateCorrection) Rate correction value (two's complement). Calculated internal rate correction value before limitation. If the RCV value exceeds the limits defined by GTUC10.MRC, flag SFS.RCLR is set to 1.
0	[31:12]	r	**Reserved** Returns 0 if read; should be written with 0.

Offset Correction Value (OCV)

OCV
Offset Correction Value **(011C$_H$)** **Reset Value: 0000 0000$_H$**



Field	Bits	Type	Description
OCV	[18:0]	rh	**Offset Correction Value** (vOffsetCorrection) Offset correction value (two's complement). Calculated internal offset correction value before limitation. If the OCV value exceeds the limits defined by GTUC10.MOC flag SFS.OCLR is set to 1.
0	[31:19]	r	**Reserved** Returns 0 if read; should be written with 0.

Note: The external rate / offset correction value is added to the limited rate / offset correction value.

SYNC Frame Status (SFS)

The maximum number of valid SYNC Frames in a communication cycle is 15.

SFS

SYNC Frame Status **(0120_H)** **Reset Value: $0000\ 0000_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0												RCLR	MRCS	OCLR	MOCS
r												rh	rh	rh	rh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VSBO				VSBE				VSAO				VSAE			
rh				rh				rh				rh			

Field	Bits	Type	Description
VSAE	[3:0]	rh	**Valid SYNC Frames Channel A, even communication cycle** Holds the number of valid SYNC Frames received on channel A in the even communication cycle. If transmission of SYNC Frames is enabled by SUCC1.TXSY the value is incremented by one. The value is updated during the network idle time (NIT) of each even communication cycle. This bit field is only valid if the channel A is assigned to the Communication Controller by SUCC1.CCHA.
VSAO	[7:4]	rh	**Valid SYNC Frames Channel A, odd communication cycle** Holds the number of valid SYNC Frames received on channel A in the odd communication cycle. If transmission of SYNC Frames is enabled by SUCC1.TXSY the value is incremented by one. The value is updated during the network idle time (NIT) of each odd communication cycle. This bit field is only valid if the channel A is assigned to the Communication Controller by SUCC1.CCHA.
VSBE	[11:8]	rh	**Valid SYNC Frames Channel B, even communication cycle** Holds the number of valid SYNC Frames received on channel B in the even communication cycle. If transmission of SYNC Frames is enabled by SUCC1.TXSY the value is incremented by one. The value is updated during the network idle time (NIT) of each even communication cycle. This bit field is only valid if the channel B is assigned to the Communication Controller by SUCC1.CCHB.

Field	Bits	Type	Description
VSBO	[15:12]	rh	**Valid SYNC Frames Channel B, odd communication cycle** Holds the number of valid SYNC Frames received on channel B in the odd communication cycle. If transmission of SYNC Frames is enabled by SUCC1.TXSY the value is incremented by one. The value is updated during the network idle time (NIT) of each odd communication cycle. This bit field is only valid if the channel B is assigned to the Communication Controller by SUCC1.CCHB.
MOCS	16	rh	**Missing Offset Correction Signal** The Missing Offset Correction flag signals to the Host, that no offset correction calculation can be performed because no SYNC Frames were received. The flag is updated by the Communication Controller at start of offset correction phase. 0_B Offset correction signal valid 1_B Missing offset correction signal
OCLR	17	rh	**Offset Correction Limit Reached** The Offset Correction Limit Reached flag signals to the Host, that the offset correction value has exceeded its limit as defined by GTUC10.MOC. The flag is updated by the Communication Controller at start of offset correction phase. 0_B Offset correction below limit 1_B Offset correction limit reached
MRCS	18	rh	**Missing Rate Correction Signal** The Missing Rate Correction Flag signals to the Host, that no rate correction calculation can be performed because no pairs of even / odd SYNC Frames were received. The flag is updated by the Communication Controller at start of offset correction phase. 0_B Rate correction signal valid 1_B Missing rate correction signal
RCLR	19	rh	**Rate Correction Limit Reached** The Rate Correction Limit Reached flag signals to the Host, that the rate correction value has exceeded its limit.as defined by GTUC10.MRC. The flag is updated by the Communication Controller at start of offset correction phase. 0_B Rate correction below limit 1_B Rate correction limit reached
0	[31:20]	r	**Reserved** Returns 0 if read; should be written with 0.

Symbol Window and network idle time (NIT) Status (SWNIT)

Symbol window related status information. Updated by the Communication Controller at the end of the symbol window for each channel. During startup the status data is not updated.

Note: MTSA and MTSB may be changed outside "DEFAULT_CONFIG" or "CONFIG" state when the write to SUC Configuration Register 1 (SUCC1) register is directly preceded by the unlock sequence as described in ***"Lock Register (LCK)" on Page 26-39****. This may be combined with CHI command SEND_MTS. If both bits MTSA and MTSB are set to 1 an MTS symbol will be transmitted on both channels when requested by writing SUCC1.CMD = 1000$_B$*

SWNIT
Symbol Window and Network Idle Time Status
(0124$_H$) **Reset Value: 0000 0000$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0				SBNB	SENB	SBNA	SENA	MTSB	MTSA	TCSB	SBSB	SESB	TCSA	SBSA	SESA
r				rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh

Field	Bits	Type	Description
SESA	0	rh	**Syntax Error in Symbol Window Channel A** (vSS!SyntaxErrorA) 0_B No syntax error detected 1_B Syntax error during symbol window detected on channel A
SBSA	1	rh	**Slot Boundary Violation in Symbol Window Channel A** (vSS!BViolationA) 0_B No slot boundary violation detected 1_B Slot boundary violation during symbol window detected on channel A

Field	Bits	Type	Description
TCSA	2	rh	**Transmission Conflict in Symbol Window Channel A** (vSS!TxConflictA) 0_B No transmission conflict detected 1_B Transmission conflict in symbol window detected on channel A
SESB	3	rh	**Syntax Error in Symbol Window Channel B** (vSS!SyntaxErrorB) 0_B No syntax error detected 1_B Syntax error during symbol window detected on channel B
SBSB	4	rh	**Slot Boundary Violation in Symbol Window Channel B** (vSS!BViolationB) 0_B No slot boundary violation detected 1_B Slot boundary violation during symbol window detected on channel B
TCSB	5	rh	**Transmission Conflict in Symbol Window Channel B** (vSS!TxConflictB) 0_B No transmission conflict detected 1_B Transmission conflict in symbol window detected on channel B
MTSA	6	rh	**MTS Received on Channel A** (vSS!ValidMTSA)[1)] Media Access Test symbol received on channel A during the proceeding symbol window. Updated by the Communication Controller for each channel at the end of the symbol window. When this bit is set to 1, also interrupt flag SIR.MTSA is set to 1. 0_B No MTS symbol received on channel A 1_B MTS symbol received on channel A
MTSB	7	rh	**MTS Received on Channel B** (vSS!ValidMTSB)[1)] Media Access Test symbol received on channel B during the proceeding symbol window. Updated by the Communication Controller for each channel at the end of the symbol window. When this bit is set to 1, also interrupt flag SIR.MTSB is set to 1. 0_B No MTS symbol received on channel B 1_B MTS symbol received on channel B

Field	Bits	Type	Description
SENA	8	rh	**Syntax Error during network idle time (NIT) Channel A** (vSS!SyntaxErrorA) Updated by the Communication Controller channel A at the end of the NIT. 0_B No syntax error detected 1_B Syntax error during network idle time (NIT) detected on channel A
SBNA	9	rh	**Slot Boundary Violation during network idle time (NIT) Channel A** (vSS!BViolationA) Updated by the Communication Controller channel A at the end of the NIT. 0_B No slot boundary violation detected 1_B Slot boundary violation during network idle time (NIT) detected on channel A
SENB	10	rh	**Syntax Error during network idle time (NIT) Channel B** (vSS!SyntaxErrorB) Updated by the Communication Controller channel B at the end of the NIT. 0_B No syntax error detected 1_B Syntax error during network idle time (NIT) detected on channel B
SBNB	11	rh	**Slot Boundary Violation during network idle time (NIT) Channel B** (vSS!BViolationB) Updated by the Communication Controller channel B at the end of the NIT. 0_B No slot boundary violation detected 1_B Slot boundary violation during network idle time (NIT) detected on channel B
0	[31:12]	r	**Reserved** Returns 0 if read; should be written with 0.

1) MTSA and MTSB may also be changed outside “DEFAULT_CONFIG” or “CONFIG” state when the write to SUCC1 register is directly preceded by the unlock sequence as described in “Lock Register (LCK)”. This may be combined with CHI command SEND_MTS. If both bits MTSA and MTSB are set to 1 an MTS symbol will be transmitted on both channels when requested by writing SUCC1.CMD = 1000_B.

Aggregated Channel Status (ACS)

The aggregated channel status provides the Host with an accrued status of channel activity for all communication slots regardless of whether they are assigned for transmission or subscribed for reception. The aggregated channel status also includes status data from the symbol window and the network idle time. The status data is updated (set) after each slot and aggregated until it is reset by the Host. During startup the status data is not updated. A flag is cleared by writing a 1 to the corresponding bit position. Writing a 0 has no effect on the flag. An application reset will also clear the register.

ACS
Aggregated Channel Status **(0128_H)** **Reset Value: $0000\ 0000_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0			SBVB	CIB	CEDB	SEDB	VFRB	0			SBVA	CIA	CEDA	SEDA	VFRA
r			rwh	rwh	rwh	rwh	rwh	r			rwh	rwh	rwh	rwh	rwh

Field	Bits	Type	Description
VFRA	0	rwh	**Valid Frame Received on Channel A** (vSS!ValidFrameA) One or more valid Frames were received on channel A in any static or dynamic slot during the observation period. 0_B No valid Frame received 1_B Valid Frame(s) received on channel A
SEDA	1	rwh	**Syntax Error Detected on Channel A** (vSS!SyntaxErrorA) One or more syntax errors in static or dynamic slots, symbol window, and network idle time (NIT) were observed on channel A. 0_B No syntax error observed 1_B Syntax error(s) observed on channel A
CEDA	2	rwh	**Content Error Detected on Channel A** (vSS!ContentErrorA) One or more Frames with a content error were received on channel A in any static or dynamic slot during the observation period. 0_B No Frame with content error received 1_B Frame(s) with content error received on channel A

Field	Bits	Type	Description
CIA	3	rwh	**Communication Indicator Channel A** One or more valid Frames were received on channel A in slots that also contained any additional communication during the observation period, i.e. one or more slots received a valid Frame AND had any combination of either syntax error OR content error OR slot boundary violation. 0_B No valid Frame(s) received in slots containing any additional communication 1_B Valid Frame(s) received on channel A in slots containing any additional communication
SBVA	4	rwh	**Slot Boundary Violation on Channel A** (vSS!BViolationA) One or more slot boundary violations were observed on channel A at any time during the observation period (static or dynamic slots, symbol window, and network idle time NIT). 0_B No slot boundary violation observed 1_B Slot boundary violation(s) observed on channel A
VFRB	8	rwh	**Valid Frame Received on Channel B** (vSS!ValidFrameB) One or more valid Frames were received on channel B in any static or dynamic slot during the observation period. 0_B No valid Frame received 1_B Valid Frame(s) received on channel B
SEDB	9	rwh	**Syntax Error Detected on Channel B** (vSS!SyntaxErrorB) One or more syntax errors in static or dynamic slots, symbol window, and network idle time (NIT) were observed on channel B. 0_B No syntax error observed 1_B Syntax error(s) observed on channel B
CEDB	10	rwh	**Content Error Detected on Channel B** (vSS!ContentErrorB) One or more Frames with a content error were received on channel B in any static or dynamic slot during the observation period. 0_B No Frame with content error received 1_B Frame(s) with content error received on channel B

Field	Bits	Type	Description
CIB	11	rwh	**Communication Indicator Channel B** One or more valid Frames were received on channel B in slots that also contained any additional communication during the observation period, i.e. one or more slots received a valid Frame AND had any combination of either syntax error OR content error OR slot boundary violation. 0_B No valid Frame(s) received in slots containing any additional communication 1_B Valid Frame(s) received on channel B in slots containing any additional communication
SBVB	12	rwh	**Slot Boundary Violation on Channel B** (vSS!BViolationB) One or more slot boundary violations were observed on channel B at any time during the observation period (static or dynamic slots, symbol window, and network idle time NIT). 0_B No slot boundary violation observed 1_B Slot boundary violation(s) observed on channel B
0	[7:5], [31:13]	r	**Reserved** Returns 0 if read; should be written with 0.

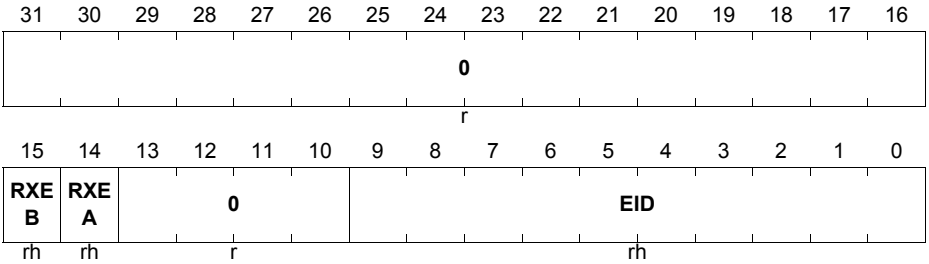
Note: The set condition of flags CIA and CIB is also fulfilled if there is only one single Frame in the slot and the slot boundary at the end of the slot is reached during the Frames channel idle recognition phase. When one of the flags SEDB, CEDB, CIB, SBVB changes from 0 to 1, service request flag EIR.EDB is set to 1.When one of the flags SEDA, CEDA, CIA, SBVA changes from 0 to 1, service request flag EIR.EDA is set to 1.

Even Sync ID [01…15] (ESIDnn)

Registers Even Sync ID nn (ESIDnn, nn=01-15) hold the Frame IDs of the SYNC Frames received in **even** communication cycles, sorted in ascending order, with register ESID01 holding the lowest received SYNC Frame ID. If the node itself transmits a SYNC Frame in an even communication cycle, register ESID01 holds the respective SYNC Frame ID as configured in Message Buffer 0 and the flags RXEA, RXEB are set. The value is updated during the network idle time (NIT) of each even communication cycle.

ESIDnn (nn = 01-15)
Even Sync ID Symbol Window nn

(012C$_H$ + nn * 4) **Reset Value: 0000 0000$_H$**



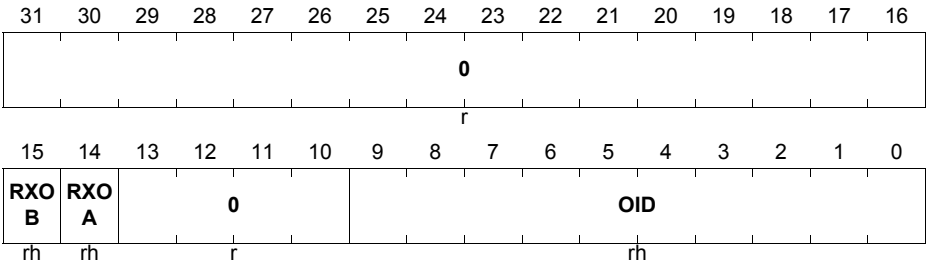
Field	Bits	Type	Description
EID	[9:0]	rh	**Even Sync ID** (vsSyncIDListA,B even) SYNC Frame ID even communication cycle.
RXEA	14	rh	**Received/Configured Even Sync ID on Channel A** Signals that a SYNC Frame corresponding to the stored even sync ID was received on channel A or that the node is configured to be a sync node with key slot = EID (ESID1 only). 0_B SYNC Frame not received on channel A / node configured to transmit SYNC Frames 1_B SYNC Frame received on channel A/ node not configured to transmit SYNC Frames
RXEB	15	rh	**Received/Configured Even Sync ID on Channel B** Signals that a SYNC Frame corresponding to the stored even sync ID was received on channel B or that the node is configured to be a sync node with key slot = EID (ESID1 only). 0_B SYNC Frame not received on channel B / node configured to transmit SYNC Frames 1_B SYNC Frame received on channel B / node not configured to transmit SYNC Frames

Field	Bits	Type	Description
0	[13:10], [31:16]	r	**Reserved** Returns 0 if read; should be written with 0.

Odd Sync ID [01…15] (OSIDnn)

he Odd Sync ID nn (OSIDnn, nn=01-15) hold the Frame IDs of the SYNC Frames received in **odd** communication cycles, sorted in ascending order, with register OSID01 holding the lowest received SYNC Frame ID. If the node itself transmits a SYNC Frame in an odd communication cycle, register OSID01 holds the respective SYNC Frame ID as configured in Message Buffer 0 and flags RXOA, RXOB are set. The value is updated during the network idle time (NIT) of each odd communication cycle.

OSIDnn (nn = 01-15)
Odd Sync ID Symbol Window nn ($016C_H$ + nn * 4) **Reset Value: $0000\ 0000_H$**



Field	Bits	Type	Description
OID	[9:0]	rh	**Odd Sync ID** (vsSyncIDListA,B odd) SYNC Frame ID even communication cycle.
RXOA	14	rh	**Received Odd Sync ID on Channel A** Signals that a SYNC Frame corresponding to the stored odd sync ID was received on channel A or that the node is configured to be a sync node with key slot = OID (OSID1 only). 0_B SYNC Frame not received on channel A/ node configured to transmit SYNC Frames 1_B SYNC Frame received on channel A/ node not configured to transmit SYNC Frames
RXOB	15	rh	**Received Odd Sync ID on Channel B** Signals that a SYNC Frame corresponding to the stored odd sync ID was received on channel B or that the node is configured to be a sync node with key slot = OID (OSID1 only) 0_B SYNC Frame not received on channel B/ node configured to transmit SYNC Frames 1_B SYNC Frame received on channel B/ node not configured to transmit SYNC Frames

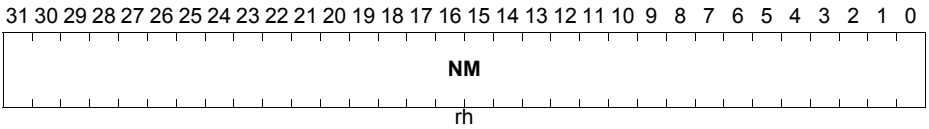
Field	Bits	Type	Description
0	[13:10], [31:16]	r	**Reserved** Returns 0 if read; should be written with 0.

Network Management Vector [1…3] (NMVx)

The three Network Management Vectors n (NMVx, x=1-3) registers hold the accrued Network Management (NM) vector (configurable 0 to 12 byte). The accrued Network Management (NM) vector is generated by the Communication Controller by bit-wise ORing each Network Management (NM) vector received (valid static Frames with PPI = 1) on each channel (see **"Network Management" on Page 26-222**). The Communication Controller updates the Network Management (NM) vector at the end of each communication cycle as long as the Communication Controller is either in "NORMAL_ACTIVE" or "NORMAL_PASSIVE" state. NMVx-bytes exceeding the configured Network Management (NM) vector length are not valid.

NMVx (x = 1-3)
Network Management Vector x

($01AC_H$ + x * 4) **Reset Value: $0000\ 0000_H$**



Field	Bits	Type	Description
NM	[31:0]	rh	**Network Management Vector**

Table 26-5 below shows the assignment of the received payload's data byte to the Network Management vector.

Table 26-5 Assignment of Data Byte to Network Management Vector

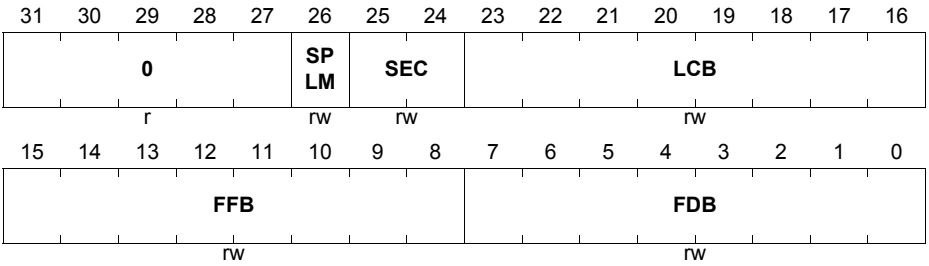
Bit / Word	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NM1	Data3								Data2								Data1								Data0							
NM2	Data7								Data6								Data5								Data4							
NM3	Data11								Data10								Data9								Data8							

26.5.2.6 Message Buffer Control Registers

Message RAM Configuration (MRC)

The Message RAM Configuration register defines the number of Message Buffers assigned to the static segment, dynamic segment, and FIFO. The register can be written during “DEFAULT_CONFIG” or “CONFIG” state only.

MRC
Message RAM Configuration (0300_H) Reset Value: $0180\ 0000_H$



Field	Bits	Type	Description
FDB	[7:0]	rw	**First Dynamic Buffer** May be modified in “DEFAULT_CONFIG” or “CONFIG” state only. 00_H No group of Message Buffers exclusively for the static segment configured 01_H …$7F_H$ Message Buffers 0 to FDB-1 reserved for static segment 80_H …FF_H No dynamic Message Buffers configured
FFB	[15:8]	rw	**First Buffer of FIFO** May be modified in “DEFAULT_CONFIG” or “CONFIG” state only. 00_H …$7E_H$ Message Buffers from FFB to LCB assigned to the FIFO $7F_H$ All Message Buffers assigned to the FIFO 80_H …FF_H No Message Buffers assigned to the FIFO

Field	Bits	Type	Description
LCB	[23:16]	rw	**Last Configured Buffer** May be only modified in “DEFAULT_CONFIG” or “CONFIG” state. 01_H …$7F_H$ Number of Message Buffers is LCB + 1 80_H …FF_H No Message Buffer configured
SEC	[25:24]	rw	**Secure Buffers** Not evaluated when the Communication Controller is in “DEFAULT_CONFIG” or “CONFIG” state. For temporary unlocking see **“Host Handling of Errors” on Page 26-257**. 00_B Reconfiguration of Message Buffers enabled with numbers < FFB enabled. *Note: In nodes configured for SYNC Frame transmission or for single slot mode operation Message Buffer 0 (and if SPLM = 1, also Message Buffer 1) Reconfiguration of all Message Buffers is always locked* 01_B Reconfiguration of Message Buffers with numbers < FDB and with numbers ≥ FFB locked and transmission of Message Buffers for static segment with numbers ≥ FDB disabled 10_B Reconfiguration of all Message Buffers locked 11_B Reconfiguration of all Message Buffers locked and transmission of Message Buffers for static segment with numbers ≥ FDB disabled
SPLM	26	rw	**SYNC Frame Payload Multiplex** This bit is only evaluated if the node is configured as sync node (SUCC1.TXSY = 1) or for single slot mode operation (SUCC1.TSM = 1). When this bit is set to 1 Message Buffers 0 and 1 are dedicated for SYNC Frame transmission with different payload data on channel A and B. When this bit is reset to 0, SYNC Frames are transmitted from Message Buffer 0 with the same payload data on both channels. Note that the channel filter configuration for Message Buffer 0 resp. Message Buffer 1 has to be chosen accordingly. 0_B Only Message Buffer 0 locked against reconfiguration 1_B Both Message Buffers 0 and 1 are locked against reconfiguration

Field	Bits	Type	Description
0	[31:27]	r	**Reserved** Returns 0 if read; should be written with 0.

*Note: In case the node is configured as sync node (*SUCC1.*TXSY = 1) or for single slot mode operation (*SUCC1.*TSM = 1), Message Buffer 0 resp. 1 is reserved for SYNC Frames or single slot Frames and have to be configured with the node-specific key slot ID. In case the node is neither configured as sync node nor for single slot operation Message Buffer 0 resp. 1 is treated like all other Message Buffers.*

Table 26-6 Usage of the three Message Buffer Pointer

Message Buffer 0	⇓ Static Buffers		
Message Buffer 1			
	⇓ Static + Dynamic Buffers	⇐ **FDB**	
…			FIFO configured: **FFB** > **FDB**
	⇓ FIFO	⇐ **FFB**	No FIFO configured: **FFB** ≥ 128
Message Buffer N-1			**LCB** ≥ **FDB**, **LCB** ≥ **FFB**
Message Buffer N		⇐ **LCB**	

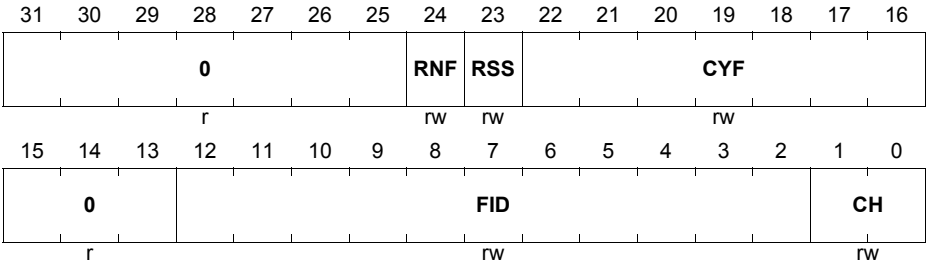
The programmer has to ensure that the configuration defined by FDB, FFB, and LCB is valid. **The Communication Controller does not check for erroneous configurations!**

Note: The maximum number of Header Sections is 128. This means a maximum of 128 Message Buffer can be configured. The maximum length of a Data Section is 254 byte. The length of the Data Section may be configured differently for each Message Buffer. For details see ***"Message RAM" on Page 26-248****.*
In case two or more Message Buffers are assigned to slot 1 by use of cycle filtering, all of them must be located either in the "Static Buffers" or at the beginning of the "Static + Dynamic Buffers" section.
The payload length configured and the length of the Data Section need to be configured identically for all Message Buffers belonging to the FIFO via WRHS2.PLC and WRHS3.DP. When the Communication Controller is not in "DEFAULT_CONFIG" or "CONFIG" state reconfiguration of Message Buffers belonging to the FIFO is locked.

FIFO Rejection Filter (FRF)

The FIFO Rejection Filter defines a user specified sequence of bits to which channel, Frame ID, and cycle count of the incoming Frames are compared. Together with the FIFO Rejection Filter Mask this register determines whether a message is rejected by the FIFO. The FRF register can be written during “DEFAULT_CONFIG” or “CONFIG” state only.

FRF
FIFO Rejection Filter **(0304_H)** **Reset Value: $0180\ 0000_H$**



Field	Bits	Type	Description
CH	[1:0]	rw	**Channel Filter** May be modified in “DEFAULT_CONFIG” or “CONFIG” state only. 00_B receive on both channels[1)] 01_B receive only on channel B 10_B receive only on channel A 11_B no reception
FID	[12:2]	rw	**Frame ID Filter** Determines the Frame ID to be rejected by the FIFO. With the additional configuration of register FRFM, the corresponding Frame ID filter bits are ignored, which results in further rejected Frame IDs. When FRFM.MFID is zero, a Frame ID filter value of zero means that no Frame ID is rejected. 000_H …$7FF_H$ Frame ID filter values

Field	Bits	Type	Description
CYF	[22:16]	rw	**Cycle Counter Filter** The 7-bit cycle counter filter determines the cycle set to which Frame ID and channel rejection filter are applied. In cycles **not** belonging to the cycle set specified by CYF, all Frames are rejected. For details about the configuration of the cycle counter filter see **“Cycle Counter Filtering” on Page 26-224**. May be modified in “DEFAULT_CONFIG” or “CONFIG” state only.
RSS	23	rw	**Reject in Static Segment** If this bit is set, the FIFO is used only be used in dynamic segment. May be modified in “DEFAULT_CONFIG” or “CONFIG” state only. 0_B FIFO also used in static segment 1_B Reject messages for static segment
RNF	24	rw	**Reject NULL Frames** If this bit is set, received NULL Frames are not stored in the FIFO. May be modified in “DEFAULT_CONFIG” or “CONFIG” state only. 0_B NULL Frames are stored in the FIFO 1_B Reject all NULL Frames
0	[15:13], [31:25]	r	**Reserved** Returns 0 if read; should be written with 0.

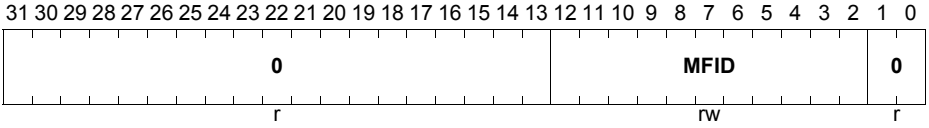
1) If reception on both channels is configured, also in static segment always both Frames (from channel A and B) are stored in the FIFO, even if they are identical.

FIFO Rejection Filter Mask (FRFM)

The FIFO Rejection Filter Mask specifies which of the corresponding Frame ID filter bits are relevant for rejection filtering. If a bit is set, it indicates that the corresponding bit in the FRF register will not be considered for rejection filtering. The FRFM register can be written during “DEFAULT_CONFIG” or “CONFIG” state only.

FRFM

FIFO Rejection Filter Mask **(0308_H)** **Reset Value: $0000\ 0000_H$**

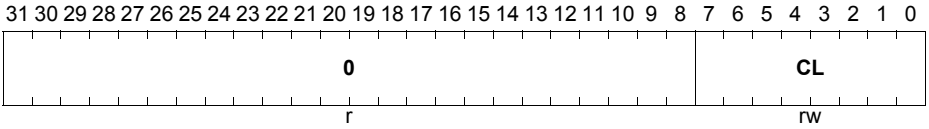


Field	Bits	Type	Description
MFID	[12:2]	rw	**Mask Frame ID Filter** May be modified in “DEFAULT_CONFIG” or “CONFIG” state only. 0_B Corresponding Frame ID filter bit is used for rejection filtering. 1_B Ignore corresponding Frame ID filter bit.
0	[1:0], [31:13]	r	**Reserved** Returns 0 if read; should be written with 0.

FIFO Critical Level (FCL)

The Communication Controller accepts modifications of the register in “DEFAULT_CONFIG” or “CONFIG” state only.

FCL
FIFO Critical Level **($030C_H$)** **Reset Value: $0000\ 0080_H$**



Field	Bits	Type	Description
CL	[7:0]	rw	**Critical Level** When the receive FIFO fill level FSR.RFFL is equal or greater than the critical level configured by CL, the receive FIFO critical level flag FSR.RFCL is set. If CL is programmed to values > 128, bit FSR.RFCL is never set. When FSR.RFCL changes from 0 to 1 bit **SIR.RFCL** is set to 1, and if enabled, a service request is generated.
0	[31:8]	r	**Reserved** Returns 0 if read; should be written with 0.

26.5.2.7 Message Buffer Status Registers

Message Handler Status (MHDS)

The Message Handler Status register gives the Host access to the current state of the Message Handler. A flag is cleared by writing a 1 to the corresponding bit position. Writing a 0 has no effect on the flag. An application reset will also clear the register. If one of the flags MHDS.EIBF, MHDS.EOBF, MHDS.EMR, MHDS.ETBF1, MHDS.ETBF2 changes from 0 to 1 EIR.EERR is set.

MHDS
Message Handler Status **(0310_H)** **Reset Value: $0000\ 0080_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	MBU							0	MBT						
r	rh							r	rh						

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	FMB							CRAM	MFMB	FMBD	ETBF2	ETBF1	EMR	EOBF	EIBF
r	rh							rh	rwh	rwh	rwh	rwh	rwh	rwh	rwh

Field	Bits	Type	Description
EIBF	0	rwh	**ECC Error Input Buffer RAM 1,2** 0_B No error 1_B Error occurred when reading Input Buffer RAM 1 or Input Buffer RAM 2
EOBF	1	rwh	**ECC Error Output Buffer RAM 1,2** 0_B No error 1_B Error occurred when reading Output Buffer RAM 1 or Output Buffer RAM 2
EMR	2	rwh	**ECC Error Message RAM** 0_B No error 1_B Error occurred when reading the Message RAM
ETBF1	3	rwh	**ECC Error Transient Buffer RAM A** 0_B No error 1_B Error occurred when reading Transient Buffer RAM A
ETBF2	4	rwh	**ECC Error Transient Buffer RAM B** 0_B No error 1_B Error occurred when reading Transient Buffer RAM B

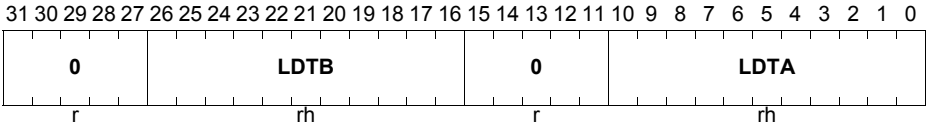
Field	Bits	Type	Description
FMBD	5	rwh	**Faulty Message Buffer Detected** 0_B No faulty Message Buffer 1_B Message Buffer referenced by MHDS.FMB holds faulty data due to a ECC error
MFMB	6	rwh	**Multiple Faulty Message Buffers detected** 0_B No additional faulty Message Buffer 1_B Another faulty Message Buffer was detected while flag MHDS.FMBD is set
CRAM	7	rh	**Clear all internal RAM's** Signals that execution of the CHI command CLEAR_RAMS is ongoing (all bits of all internal RAM blocks are written to 0). The bit is set by application reset or by CHI command CLEAR_RAMS. 0_B No execution of the CHI command CLEAR_RAMS 1_B Execution of the CHI command CLEAR_RAMS ongoing
FMB	[14:8]	rh	**Faulty Message Buffer** ECC error occurred when reading from the Message Buffer or when transferring data from Input Buffer or Transient Buffer A or Transient Buffer B to the Message Buffer referenced by MHDS.FMB. Value only valid when one of the flags MHDS.EIBF, MHDS.EMR, MHDS.ETBF1, MHDS.ETBF2, and flag MHDS.FMBD is set. Updated only after the Host has reset flag MHDS.FMBD.
MBT	[22:16]	rh	**Message Buffer Transmitted** Number of last successfully transmitted Message Buffer. If the Message Buffer is configured for single-shot mode, the respective TXR flag in the Transmission Request Registers TXRQ1 to TXRQ4 was reset. MBT is reset when the Communication Controller leaves "CONFIG" state or enters "STARTUP" state.
MBU	[30:24]	rh	**Message Buffer Updated** Number of Message Buffer that was updated last. For this Message Buffer the respective NDn (n = 0-31) to NDn (n = 96-127)and / or MBCn (n = 0-31) to MBCn (n = 96-127) flag in the New Data Registers NDAT1 to NDAT4 and the Message Buffer Status Changed MBSC1 to MBSC4 registers are also set. MBU is reset when the Communication Controller leaves "CONFIG" state or enters "STARTUP" state.

Field	Bits	Type	Description
0	15, 23, 31	r	**Reserved** Returns 0 if read; should be written with 0.

Last Dynamic Transmit Slot (LDTS)

The Last Dynamic Transmit Slot Register stores the Slot Counter value at the time of the last Frame transmission in the dynamic segment. This register is reset when the Communication Controller leaves “CONFIG” state or enters “STARTUP” state.

LDTS
Last Dynamic Transmit Slot **(0314_H)** **Reset Value: $0000\ 0000_H$**

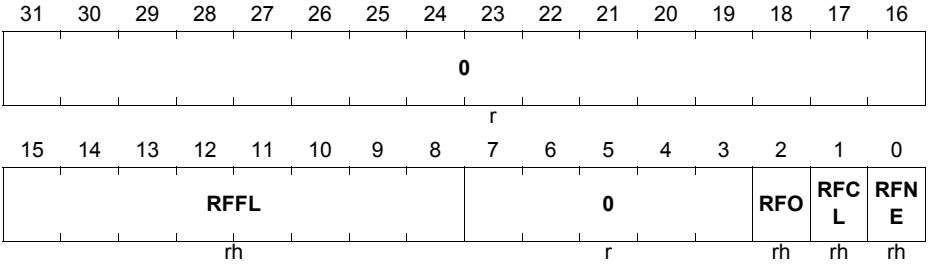


Field	Bits	Type	Description
LDTA	[10:0]	rh	**Last Dynamic Transmission Channel A** Value of (vSlotCounter[A]) at the time of the last Frame transmission on channel A in the dynamic segment of this node. It is updated at the end of the dynamic segment and is reset to zero if no Frame was transmitted during the dynamic segment.
LDTB	[26:16]	rh	**Last Dynamic Transmission Channel B** Value of (vSlotCounter[B]) at the time of the last Frame transmission on channel B in the dynamic segment of this node. It is updated at the end of the dynamic segment and is reset to zero if no Frame was transmitted during the dynamic segment.
0	[15:11], [31:27]	r	**Reserved** Returns 0 if read; should be written with 0.

FIFO Status Register (FSR)

The register is reset when the Communication Controller leaves “CONFIG” state or enters “STARTUP” state.

FSR
FIFO Status Register **(0318_H)** **Reset Value: $0000\ 0000_H$**



Field	Bits	Type	Description
RFNE	0	rh	**Receive FIFO Not Empty** This flag is set by the Communication Controller when a received valid Frame (data or NULL Frame depending on rejection mask) was stored in the FIFO. In addition, service request flag SIR.RFNE is set. The bit is reset after the Host has read all message from the FIFO. 0_B Receive FIFO is empty 1_B Receive FIFO is not empty
RFCL	1	rh	**Receive FIFO Critical Level** This flag is set when the receive FIFO fill level RFFL is equal or greater than the critical level as configured by FCL.CL. The flag is cleared by the Communication Controller as soon as RFFL drops below FCL.CL. When RFCL changes from 0 to 1 bit SIR.RFCL is set to 1, and if enabled, an service request is generated. 0_B Receive FIFO below critical level 1_B Receive FIFO critical level reached

Field	Bits	Type	Description
RFO	2	rh	**Receive FIFO Overrun** The flag is set by the Communication Controller when a receive FIFO overrun is detected. When a receive FIFO overrun occurs, the oldest message is overwritten with the actual received message. In addition, service request flag EIR.RFO is set.The flag is cleared by the next FIFO read access issued by the Host. 0_B No receive FIFO overrun detected 1_B A receive FIFO overrun has been detected
RFFL	[15:8]	rh	**Receive FIFO Fill Level** Number of FIFO buffers filled up with new data not yet read by the Host. Maximum value is 128.
0	[7:3], [31:16]	r	**Reserved** Returns 0 if read; should be written with 0.

Message Handler Constraints Flags (MHDF)

Some constraints exist for the Message Handler regarding f_{CLC_ERAY} frequency, Message RAM configuration, and FlexRay™ bus traffic. To simplify software development, constraints violations are reported by setting flags in the MHDF. The register is reset when the Communication Controller leaves “CONFIG” state or enters “STARTUP” state. A flag is cleared by setting the corresponding bit position. Clearing has no effect on the flag. If any flag in MHDFL is set, interrupt flag EIR.MHF is set.

MHDF

Message Handler Constraints Flags (031C$_H$) **Reset Value: 0000 0000$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0							WAHP	TNSB	TNSA	TBFB	TBFA	FNFB	FNFA	SNUB	SNUA
r							rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh

Field	Bits	Type	Description
SNUA	0	rwh	**Status Not Updated Channel A** This flag is set by the Communication Controller when the Message Handler, due to overload condition, was not able to update a Message Buffer’s status MBS with respect to channel A. 0_B No overload condition occurred when updating MBS for channel A 1_B MBS for channel A not updated
SNUB	1	rwh	**Status Not Updated Channel B** This flag is set by the Communication Controller when the Message Handler, due to overload condition, was not able to update a Message Buffer’s status MBS with respect to channel B. 0_B No overload condition occurred when updating MBS for channel B 1_B MBS for channel B not updated

Field	Bits	Type	Description
FNFA	2	rwh	**Find Sequence Not Finished Channel A** This flag is set by the Communication Controller when the Message Handler, due to overload condition, was not able to finish a find sequence (scan of Message RAM for matching Message Buffer) with respect to channel A. 0_B No find sequence not finished for channel A 1_B Find sequence not finished for channel A
FNFB	3	rwh	**Find Sequence Not Finished Channel B** This flag is set by the Communication Controller when the Message Handler, due to overload condition, was not able to finish a find sequence (scan of Message RAM for matching Message Buffer) with respect to channel B. 0_B No find sequence not finished for channel B 1_B Find sequence not finished for channel B
TBFA	4	rwh	**Transient Buffer Access Failure A** This flag is set by the Communication Controller when a read or write access to Transient Buffer A requested by PRT A could not complete within the available time. 0_B No TBF A access failure 1_B TBF A access failure
TBFB	5	rwh	**Transient Buffer Access Failure B** This flag is set by the Communication Controller when a read or write access to Transient Buffer B requested by PRT B could not complete within the available time. 0_B No Transient Buffer B access failure 1_B Transient Buffer B access failure
TNSA	6	rwh	**Transmission Not Started Channel A** This flag is set by the CC when the Message Handler was not ready to start a scheduled transmission on channel A at the action point of the configured slot. 0_B No transmission not started on channel A 1_B Transmission not started on channel A
TNSB	7	rwh	**Transmission Not Started Channel B** This flag is set by the CC when the Message Handler was not ready to start a scheduled transmission on channel B at the action point of the configured slot. 0_B No transmission not started on channel B 1_B Transmission not started on channel B

Field	Bits	Type	Description
WAHP	8	rwh	**Write Attempt to Header Partition** Outside “DEFAULT_CONFIG” and “CONFIG” state this flag is set by the Communication Controller when the message handler tries to write message data into the Header Partition of the Message RAM due to faulty configuration of a Message Buffer. The write attempt is not executed, to protect the Header Partition from unintended write accesses. 0_B No write attempt to Header Partition 1_B Write attempt to Header Partition
0	[31:9]	r	**Reserved** Returns 0 if read; should be written with 0.

Transmission Request 1 (TXRQ1)

This register reflect the state of the TXR flags of the configured Message Buffers 0 to 31. The flags are evaluated for transmit buffers only. If the number of configured Message Buffers is less than 31, the remaining TXRn flags have no meaning and are read as 0.

TXRQ1
Transmission Request Register 1 (0320_H) **Reset Value: $0000\ 0000_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TXR 31	**TXR 30**	**TXR 29**	**TXR 28**	**TXR 27**	**TXR 26**	**TXR 25**	**TXR 24**	**TXR 23**	**TXR 22**	**TXR 21**	**TXR 20**	**TXR 19**	**TXR 18**	**TXR 17**	**TXR 16**
rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TXR 15	**TXR 14**	**TXR 13**	**TXR 12**	**TXR 11**	**TXR 10**	**TXR 9**	**TXR 8**	**TXR 7**	**TXR 6**	**TXR 5**	**TXR 4**	**TXR 3**	**TXR 2**	**TXR 1**	**TXR 0**
rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh

Field	Bits	Type	Description
TXRn (n = 0-31)	n	rh	**Transmission Request n (n = 0-31)** If the flag is set, the respective Message Buffer 0 to 31 is ready for transmission respectively transmission of this Message Buffer is in progress. In single-shot mode the flags are reset after transmission has completed.

Transmission Request Register 2 (TXRQ2)

This register reflect the state of the TXR flags of the configured Message Buffers 31 to 63. The flags are evaluated for transmit buffers only. If the number of configured Message Buffers is less than 63, the remaining TXRn flags have no meaning and are read as 0.

TXRQ2

Transmission Request Register 2 (0324_H) Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TXR 63	**TXR 62**	**TXR 61**	**TXR 60**	**TXR 59**	**TXR 58**	**TXR 57**	**TXR 56**	**TXR 55**	**TXR 54**	**TXR 53**	**TXR 52**	**TXR 51**	**TXR 50**	**TXR 49**	**TXR 48**
rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TXR 47	**TXR 46**	**TXR 45**	**TXR 44**	**TXR 43**	**TXR 42**	**TXR 41**	**TXR 40**	**TXR 39**	**TXR 38**	**TXR 37**	**TXR 36**	**TXR 35**	**TXR 34**	**TXR 33**	**TXR 32**
rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh

Field	Bits	Type	Description
TXRn (n = 32-63)	n - 32	rh	**Transmission Request n (n = 32-63)** If the flag is set, the respective Message Buffer 32 to 63 is ready for transmission respectively transmission of this Message Buffer is in progress. In single-shot mode the flags are reset after transmission has completed.

Transmission Request Register 3 (TXRQ3)

This register reflect the state of the TXR flags of the configured Message Buffers 64 to 95. The flags are evaluated for transmit buffers only. If the number of configured Message Buffers is less than 95, the remaining TXRn flags have no meaning and are read as 0.

TXRQ3

Transmission Request Register 3 (0328_H) **Reset Value: $0000\ 0000_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TXR 95	**TXR 94**	**TXR 93**	**TXR 92**	**TXR 91**	**TXR 90**	**TXR 89**	**TXR 88**	**TXR 87**	**TXR 86**	**TXR 85**	**TXR 84**	**TXR 83**	**TXR 82**	**TXR 81**	**TXR 80**
rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TXR 79	**TXR 78**	**TXR 77**	**TXR 76**	**TXR 75**	**TXR 74**	**TXR 73**	**TXR 72**	**TXR 71**	**TXR 70**	**TXR 69**	**TXR 68**	**TXR 67**	**TXR 66**	**TXR 65**	**TXR 64**
rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh

Field	Bits	Type	Description
TXRn (n = 64-95)	n - 64	rh	**Transmission Request n (n = 64-95)** If the flag is set, the respective Message Buffer 64 to 95 is ready for transmission respectively transmission of this Message Buffer is in progress. In single-shot mode the flags are reset after transmission has completed.

Transmission Request Register 4 (TXRQ4)

This register reflect the state of the TXR flags of the configured Message Buffers 96 to 127. The flags are evaluated for transmit buffers only. If the number of configured Message Buffers is less than 127, the remaining TXRn flags have no meaning and are read as 0.

TXRQ4

Transmission Request Register 4 ($032C_H$) Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TXR 127	**TXR 126**	**TXR 125**	**TXR 124**	**TXR 123**	**TXR 122**	**TXR 121**	**TXR 120**	**TXR 119**	**TXR 118**	**TXR 117**	**TXR 116**	**TXR 115**	**TXR 114**	**TXR 113**	**TXR 112**
rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TXR 111	**TXR 110**	**TXR 109**	**TXR 108**	**TXR 107**	**TXR 106**	**TXR 105**	**TXR 104**	**TXR 103**	**TXR 102**	**TXR 101**	**TXR 100**	**TXR 99**	**TXR 98**	**TXR 97**	**TXR 96**
rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh

Field	Bits	Type	Description
TXRn (n = 96-127)	n - 96	rh	**Transmission Request n (n = 96-127)** If the flag is set, the respective Message Buffer 96 to 127 is ready for transmission respectively transmission of this Message Buffer is in progress. In single-shot mode the flags are reset after transmission has completed.

New Data Register 1 (NDAT1)

This register reflect the state of the ND flags of all configured Message Buffers 0 to 31. ND flags assigned to transmit buffers are meaningless. If the number of configured Message Buffers is less than 31, the remaining NDn flags have no meaning. The registers are reset when the Communication Controller leaves “CONFIG” state or enters “STARTUP” state.

NDAT1
New Data Register 1 **(0330_H)** **Reset Value: 0000 0000$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ND 31	**ND 30**	**ND 29**	**ND 28**	**ND 27**	**ND 26**	**ND 25**	**ND 24**	**ND 23**	**ND 22**	**ND 21**	**ND 20**	**ND 19**	**ND 18**	**ND 17**	**ND 16**
rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ND 15	**ND 14**	**ND 13**	**ND 12**	**ND 11**	**ND 10**	**ND9**	**ND8**	**ND7**	**ND6**	**ND5**	**ND4**	**ND3**	**ND2**	**ND1**	**ND0**
rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh

Field	Bits	Type	Description
NDn (n = 0-31)	n	rh	**New Data n (n = 0-31)** The flags are set when a valid received Data Frame matches the Message Buffer’s filter configuration, independent of the payload length received or the payload length configured for that Message Buffer. The flags are not set after reception of NULL Frames except for Message Buffers belonging to the receive FIFO. An ND flag is reset when the Header Section of the corresponding Message Buffer is reconfigured or when the Data Section has been transferred to the Output Buffer.

New Data Register 2 (NDAT2)

This register reflect the state of the ND flags of all configured Message Buffers 32 to 63. ND flags assigned to transmit buffers are meaningless. If the number of configured Message Buffers is less than 63, the remaining NDn flags have no meaning. The registers are reset when the Communication Controller leaves “CONFIG” state or enters “STARTUP” state.

NDAT2
New Data Register 2 **(0334_H)** **Reset Value: 0000 0000$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ND 63	**ND 62**	**ND 61**	**ND 60**	**ND 59**	**ND 58**	**ND 57**	**ND 56**	**ND 55**	**ND 54**	**ND 53**	**ND 52**	**ND 51**	**ND 50**	**ND 49**	**ND 48**
rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ND 47	**ND 46**	**ND 45**	**ND 44**	**ND 43**	**ND 42**	**ND 41**	**ND 40**	**ND 39**	**ND 38**	**ND 37**	**ND 36**	**ND 35**	**ND 34**	**ND 33**	**ND 32**
rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh

Field	Bits	Type	Description
NDn (n = 32-63)	n - 32	rh	**New Data n (n = 32-63)** The flags are set when a valid received Data Frame matches the Message Buffer’s filter configuration, independent of the payload length received or the payload length configured for that Message Buffer. The flags are not set after reception of NULL Frames except for Message Buffers belonging to the receive FIFO. An ND flag is reset when the Header Section of the corresponding Message Buffer is reconfigured or when the Data Section has been transferred to the Output Buffer.

New Data Register 3 (NDAT3)

This register reflect the state of the ND flags of all configured Message Buffers 64 to 95. ND flags assigned to transmit buffers are meaningless. If the number of configured Message Buffers is less than 95, the remaining NDn flags have no meaning. The registers are reset when the Communication Controller leaves “CONFIG” state or enters “STARTUP” state.

NDAT3
New Data Register 3 **(0338_H)** **Reset Value: 0000 0000$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ND 95	**ND 94**	**ND 93**	**ND 92**	**ND 91**	**ND 90**	**ND 89**	**ND 88**	**ND 87**	**ND 86**	**ND 85**	**ND 84**	**ND 83**	**ND 82**	**ND 81**	**ND 80**
rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ND 79	**ND 78**	**ND 77**	**ND 76**	**ND 75**	**ND 74**	**ND 73**	**ND 72**	**ND 71**	**ND 70**	**ND 69**	**ND 68**	**ND 67**	**ND 66**	**ND 65**	**ND 64**
rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh

Field	Bits	Type	Description
NDn (n = 64-95)	n - 64	rh	**New Data n (n = 64-95)** The flags are set when a valid received Data Frame matches the Message Buffer’s filter configuration, independent of the payload length received or the payload length configured for that Message Buffer. The flags are not set after reception of NULL Frames except for Message Buffers belonging to the receive FIFO. An ND flag is reset when the Header Section of the corresponding Message Buffer is reconfigured or when the Data Section has been transferred to the Output Buffer.

New Data Register 4 (NDAT4)

This register reflect the state of the ND flags of all configured Message Buffers 96 to 127. ND flags assigned to transmit buffers are meaningless. If the number of configured Message Buffers is less than 127, the remaining NDn flags have no meaning. The registers are reset when the Communication Controller leaves “CONFIG” state or enters “STARTUP” state.

NDAT4
New Data Register 4 **($033C_H$)** **Reset Value: 0000 0000$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ND 127	**ND 126**	**ND 125**	**ND 124**	**ND 123**	**ND 122**	**ND 121**	**ND 120**	**ND 119**	**ND 118**	**ND 117**	**ND 116**	**ND 115**	**ND 114**	**ND 113**	**ND 112**
rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ND 111	**ND 110**	**ND 109**	**ND 108**	**ND 107**	**ND 106**	**ND 105**	**ND 104**	**ND 103**	**ND 102**	**ND 101**	**ND 100**	**ND 99**	**ND 98**	**ND 97**	**ND 96**
rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh

Field	Bits	Type	Description
NDn (n = 96-127)	n - 96	rh	**New Data n (n = 96-127)** The flags are set when a valid received Data Frame matches the Message Buffer’s filter configuration, independent of the payload length received or the payload length configured for that Message Buffer. The flags are not set after reception of NULL Frames except for Message Buffers belonging to the receive FIFO. An ND flag is reset when the Header Section of the corresponding Message Buffer is reconfigured or when the Data Section has been transferred to the Output Buffer.

Message Buffer Status Changed 1 (MBSC1)

This register reflect the state of the MBC flags of all configured Message Buffers. If the number of configured Message Buffers is less than 31, the remaining MBCn flags have no meaning. The register is reset when the communication controller leaves “CONFIG” state or enters “STARTUP” state.

MBSC1

Message Buffer Status Changed 1 (0340_H) **Reset Value: $0000\ 0000_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MBC 31	**MBC 30**	**MBC 29**	**MBC 28**	**MBC 27**	**MBC 26**	**MBC 25**	**MBC 24**	**MBC 23**	**MBC 22**	**MBC 21**	**MBC 20**	**MBC 19**	**MBC 18**	**MBC 17**	**MBC 16**
rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MBC 15	**MBC 14**	**MBC 13**	**MBC 12**	**MBC 11**	**MBC 10**	**MBC 9**	**MBC 8**	**MBC 7**	**MBC 6**	**MBC 5**	**MBC 4**	**MBC 3**	**MBC 2**	**MBC 1**	**MBC 0**
rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh

Field	Bits	Type	Description
MBCn (n = 0-31)	n	rh	**Message Buffer Status Changed n (n = 0-31)** An MBC flags is set whenever the Message Handler changes on of the status flags VFRA, VFRB, SEOA, SEOB, CEOA, CEOB, SVOA, SVOB, TCIA, TCIB, ESA, ESB, MLST, FTA, FTB in the Header Section (see **“Message Buffer Status (MBS)” on Page 26-186**) of the respective Message Buffer 0 to Message Buffer 31. The flags are reset when the Header Section of the Message Buffer is reconfigured or when it has been transferred to the Output Buffer.

Message Buffer Status Changed 2 (MBSC2)

This register reflect the state of the MBC flags of all configured Message Buffers. If the number of configured Message Buffers is less than 63, the remaining MBCn flags have no meaning. The register is reset when the communication controller leaves “CONFIG” state or enters “STARTUP” state.

MBSC2

Message Buffer Status Changed 2 (0344_H) **Reset Value: $0000\ 0000_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MBC 63	**MBC 62**	**MBC 61**	**MBC 60**	**MBC 59**	**MBC 58**	**MBC 57**	**MBC 56**	**MBC 55**	**MBC 54**	**MBC 53**	**MBC 52**	**MBC 51**	**MBC 50**	**MBC 49**	**MBC 48**
rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MBC 47	**MBC 46**	**MBC 45**	**MBC 44**	**MBC 43**	**MBC 42**	**MBC 41**	**MBC 40**	**MBC 39**	**MBC 38**	**MBC 37**	**MBC 36**	**MBC 35**	**MBC 34**	**MBC 33**	**MBC 32**
rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh

Field	Bits	Type	Description
MBCn (n = 32-63)	n - 32	rh	**Message Buffer Status Changed n (n = 32-63)** An MBC flags is set whenever the Message Handler changes on of the status flags VFRA, VFRB, SEOA, SEOB, CEOA, CEOB, SVOA, SVOB, TCIA, TCIB, ESA, ESB, MLST, FTA, FTB in the Header Section (see **“Message Buffer Status (MBS)” on Page 26-186**) of the respective Message Buffer 32 to Message Buffer 63. The flags are reset when the Header Section of the Message Buffer is reconfigured or when it has been transferred to the Output Buffer.

Message Buffer Status Changed 3 (MBSC3)

This register reflect the state of the MBC flags of all configured Message Buffers. If the number of configured Message Buffers is less than 95, the remaining MBCn flags have no meaning. The register is reset when the communication controller leaves “CONFIG” state or enters “STARTUP” state.

MBSC3

Message Buffer Status Changed 3 (0348_H) **Reset Value: $0000\ 0000_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MBC 95	**MBC 94**	**MBC 93**	**MBC 92**	**MBC 91**	**MBC 90**	**MBC 89**	**MBC 88**	**MBC 87**	**MBC 86**	**MBC 85**	**MBC 84**	**MBC 83**	**MBC 82**	**MBC 81**	**MBC 80**
rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MBC 79	**MBC 78**	**MBC 77**	**MBC 76**	**MBC 75**	**MBC 74**	**MBC 73**	**MBC 72**	**MBC 71**	**MBC 70**	**MBC 69**	**MBC 68**	**MBC 67**	**MBC 66**	**MBC 65**	**MBC 64**
rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh

Field	Bits	Type	Description
MBCn (n = 64-95)	n - 64	rh	**Message Buffer Status Changed n (n = 64-95)** An MBC flags is set whenever the Message Handler changes on of the status flags VFRA, VFRB, SEOA, SEOB, CEOA, CEOB, SVOA, SVOB, TCIA, TCIB, ESA, ESB, MLST, FTA, FTB in the Header Section (see **“Message Buffer Status (MBS)” on Page 26-186**) of the respective Message Buffer 64 to Message Buffer 95. The flags are reset when the Header Section of the Message Buffer is reconfigured or when it has been transferred to the Output Buffer.

Message Buffer Status Changed 4 (MBSC4)

This register reflect the state of the MBC flags of all configured Message Buffers. If the number of configured Message Buffers is less than 127, the remaining MBCn flags have no meaning. The register is reset when the communication controller leaves “CONFIG” state or enters “STARTUP” state.

MBSC4

Message Buffer Status Changed 4 ($034C_H$) Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MBC 127	**MBC 126**	**MBC 125**	**MBC 124**	**MBC 123**	**MBC 122**	**MBC 121**	**MBC 120**	**MBC 119**	**MBC 118**	**MBC 117**	**MBC 116**	**MBC 115**	**MBC 114**	**MBC 113**	**MBC 112**
rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MBC 111	**MBC 110**	**MBC 109**	**MBC 108**	**MBC 107**	**MBC 106**	**MBC 105**	**MBC 104**	**MBC 103**	**MBC 102**	**MBC 101**	**MBC 100**	**MBC 99**	**MBC 98**	**MBC 97**	**MBC 96**
rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh

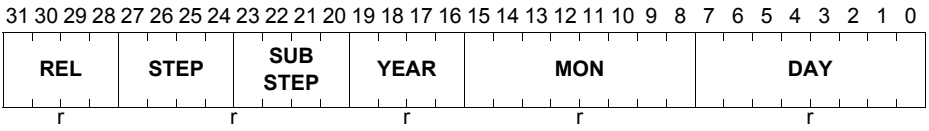
Field	Bits	Type	Description
MBCn (n = 96-127)	n - 96	rh	**Message Buffer Status Changed n (n = 96-127)** An MBC flags is set whenever the Message Handler changes on of the status flags VFRA, VFRB, SEOA, SEOB, CEOA, CEOB, SVOA, SVOB, TCIA, TCIB, ESA, ESB, MLST, FTA, FTB in the Header Section (see **“Message Buffer Status (MBS)” on Page 26-186**) of the respective Message Buffer 96 to Message Buffer 127. The flags are reset when the Header Section of the Message Buffer is reconfigured or when it has been transferred to the Output Buffer.

26.5.2.8 Identification Registers

Core Release Register (CREL)

This register contains bit fields about the ERAY module identification. It is read only.

CREL
Core Release Register **(03F0$_H$)** **Reset Value: XXXX XXXX$_H$**



Field	Bits	Type	Description
DAY	[7:0]	r	**Design Time Stamp, Day** Two digits, BCD-coded.
MON	[15:8]	r	**Design Time Stamp, Month** Two digits, BCD-coded.
YEAR	[19:16]	r	**Design Time Stamp, Year** One digit, BCD-coded.
SUBSTEP	[23:20]	r	**Sub-Step of Core Release** One digits, BCD-coded. 0_H Alpha, pre-Beta, pre-Beta-update, pre-Beta2, pre-Beta2-update, Beta, Beta2, Revision 1.0.0 1_H Beta_ct, Beta-ct-fix1, Revision 1.0.1 2_H Revision1.0RC1,Beta-ct-fix2, REVISION 1.0RC1
STEP	[27:24]	r	**Step of Core Release** One digits, BCD-coded. 0_H Revision 1.0.0 1_H Alpha 2_H pre-Beta 3_H pre-Beta-update 4_H pre-Beta2 5_H pre-Beta2-update 6_H Beta 7_H Beta2

Field	Bits	Type	Description
REL	[31:28]	r	**Core Release** One digit, BCD-coded. 0_B alpha…beta2ct 1_B Revision 1.0

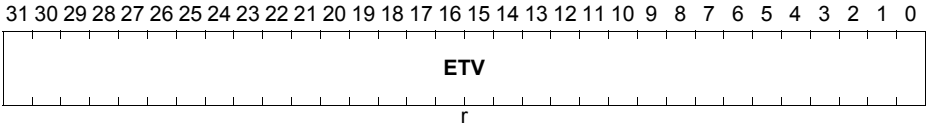
Table 26-7 Coding of releases

Release	Step	Sub-Step	Name	Release Date
0	1	0	Alpha	
0	2	0	pre-Beta	
0	3	0	pre-Beta-update	
0	4	0	pre-Beta2	
0	5	0	pre-Beta2-update	
0	6	0	Beta	
0	6	1	Beta-ct-fix1	14.10.2005
0	6	2	Beta-ct-fix2	14.12.2005
0	7	0	Beta2	03.02.2006
0	7	1	Beta2ct	24.03.2006
0	7	2	Revision 1.0RC1	07.04.2006
1	0	0	Release 1.0.0	19.05.2006
1	0	1	Release 1.0.1	2006
1	0	2	Release 1.0.2	31.10.2007

Endian Register (ENDN)

This register may be used to check, if the data of the E-Ray is handled by a host with the correct endian format. It is read only.

ENDN
Endian Register **(003F4$_H$)** **Reset Value: 8765 4321$_H$**



Field	Bits	Type	Description
ETV	[31:0]	r	**Endianness Test Value** The endianness test value.

26.5.2.9 Input Buffer

Double buffer structure consisting of Input Buffer Host and Input Buffer Shadow. While the Host can write to Input Buffer Host, the transfer to the Message RAM is done from Input Buffer Shadow. The Input Buffer holds the Header and Data Sections to be transferred to the selected Message Buffer in the Message RAM. It is used to configure the Message Buffers in the Message RAM and to update the Data Sections of transmit buffers.

When updating the Header Section of a Message Buffer in the Message RAM from the Input Buffer, the Message Buffer Status as described in **“Message Buffer Status (MBS)” on Page 26-186** is automatically reset to zero.

The Header Sections of Message Buffers belonging to the receive FIFO can only be (re)configured when the Communication Controller is in “DEFAULT_CONFIG” or “CONFIG” state. For those Message Buffers only the payload length configured and the data pointer need to be configured via WRHS2.PLC and WRHS2.DP. All information required for acceptance filtering is taken from the FIFO rejection filter and the FIFO rejection filter mask.

The data transfer between Input Buffer (IBF) and Message RAM is described in detail in **“Data Transfer from Input Buffer to Message RAM” on Page 26-233**.

Write Data Section [01 - 64] (WRDSnn (nn = 01-64))

The Write Data Section (WRDSnn, nn = 01-64) holds the data words to be transferred to the Data Section of the addressed Message Buffer. The data words (DW_n) are written to the Message RAM in transmission order from DW1 (byte0, byte1) to DW_{PL} (PL = number of data words as defined by the payload length configured by WRHS2.PLC).

WRDSnn (nn = 01-64)
Write Data Section nn **($03FC_H$ + nn * 4)** **Reset Value: $0000\ 0000_H$**

31 30 29 28 27 26 25 24	23 22 21 20 19 18 17 16	15 14 13 12 11 10 9 8	7 6 5 4 3 2 1 0
MDWBnn3	MDWBnn2	MDWBnn1	MDWBnn0
rw	rw	rw	rw

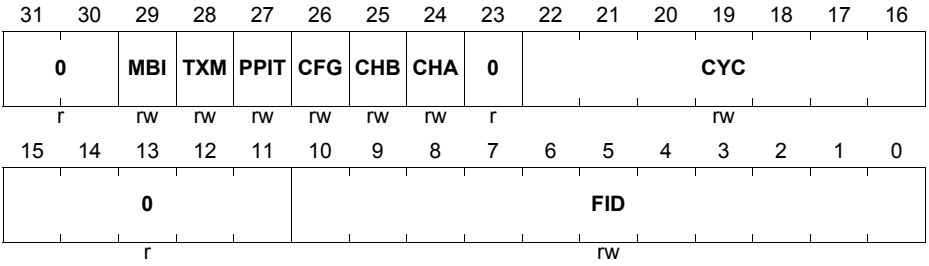
Field	Bits	Type	Description
MDWB0	[7:0]	rw	**32-Bit Word nn, Byte 0**
MDWB1	[15:8]	rw	**32-Bit Word nn, Byte 1**
MDWB2	[23:16]	rw	**32-Bit Word nn, Byte 2**
MDWB3	[31:24]	rw	**32-Bit Word nn, Byte 3**

Note: 16-bit Word 127 is located on WRDS64.MDW. In this case WRDS64.MDW is unused (no valid data). The Input Buffer RAMs are initialized to zero when leaving application reset or by CHI command CLEAR_RAMS.

Note: When writing to the WRDSnn (nn = 01-64), each 32-bit word has to be filled up by one 32-bit access OR two consecutive 16-bit accesses OR four consecutive 8-bit accesses before the transfer from the Input Buffer to the Message RAM is started by writing the number of the target Message Buffer in the Message RAM to the Input Buffer Command Request register. If a 32-bit word of the Input Buffer has been filled with less then two consecutive 16-bit accesses OR four consecutive 8-bit accesses (less then 32-bit), random data is transferred into the Input buffer for every not written 16-bit or 8-bit of a 32-bit word.

Write Header Section 1 (WRHS1)

WRHS1
Write Header Section 1 **(0500_H)** **Reset Value: $0000\ 0000_H$**



Field	Bits	Type	Description
FID	[10:0]	rw	**Frame ID** Frame ID of the selected Message Buffer. The Frame ID defines the slot number for transmission / reception of the respective message. Message Buffers with Frame ID = 0 are considered as not valid.
CYC	[22:16]	rw	**Cycle Code** The 7-bit cycle code determines the cycle set used for cycle counter filtering. For details about the configuration of the cycle code see **Section 26.6.7.3**.
CHA	24	rw	**Channel Filter Control A** The channel filtering field A associated with the buffer serves of channel A as a filter for receive buffers, and as a control field for transmit buffers
CHB	25	rw	**Channel Filter Control B** The channel filtering field B associated with the buffer serves of channel B as a filter for receive buffers, and as a control field for transmit buffers
CFG	26	rw	**Message Buffer Direction Configuration Bit** This bit is used to configure the corresponding buffer as a transmit buffer or as a receive buffer. For Message Buffers belonging to the receive FIFO the bit is not evaluated. 0_B The corresponding buffer is configured as Receive Buffer 1_B The corresponding buffer is configured as Transmit Buffer

Field	Bits	Type	Description
PPIT	27	rw	**Payload Preamble Indicator Transmit** This bit is used to control the state of the Payload Preamble Indicator in transmit Frames. If the bit is set in a static Message Buffer, the respective Message Buffer holds Network Management information. If the bit is set in a dynamic Message Buffer the first two byte of the Payload Segment may be used for message ID filtering by the receiver. Message ID filtering of received FlexRay™ Frames is not supported by the E-Ray module, but can be done by the Host. 0_B Payload Preamble Indicator not set 1_B Payload Preamble Indicator set
TXM	28	rw	**Transmission Mode** This bit is used to select the transmission mode (see **"Transmit Buffers" on Page 26-226**). 0_B Continuous mode 1_B Single-shot mode
MBI	29	rw	**Message Buffer Service Request** This bit enables the receive / transmit service request for the corresponding Message Buffer. After a dedicated receive buffer has been updated by the Message Handler, flag SIR.RXI and /or SIR.MBSI in the Status Service Request register are set. After a transmission has completed flag SIR.TXI is set. 0_B The corresponding Message Buffer service request is disabled 1_B The corresponding Message Buffer service request is enabled
0	[15:11], 23, [31:30]	r	**Reserved** Returns 0 if read; should be written with 0.

Note: The Input Buffer RAMs are initialized to zero when leaving application reset or by CHI command CLEAR_RAMS. Note that only the currently active IBF bank is cleared. To clear the 2nd bank as well, CUST1.IBF1PAG and CUST1.IBF2PAG need to be set and command CLEAR_RAMS need to be issued again. This is required in particular after an application reset. If the 2nd bank of IBF is left unused, this procedure is not required.

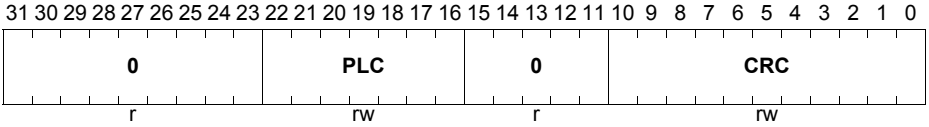
Table 26-8 Channel Filter Control Bits

CHA	CHB	Transmit Buffer transmit Frame on	Receive Buffer store Frame received from
1[1)]	1[1)]	Both Channels (static segment only)	Channel A or B (store first semantically valid Frame, static segment only)
1	0	Channel A	Channel A
0	1	Channel B	Channel B
0	0	No Transmission	Ignore Frame

1) If a Message Buffer is configured for the dynamic segment and both bits of the channel filtering field are set to 1, no Frames are transmitted resp. received Frames are ignored (same function as CHA = CHB = 0)

Write Header Section 2 (WRHS2)

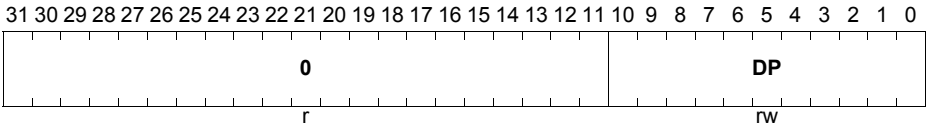
WRHS2
Write Header Section 2 **(0504_H)** **Reset Value: $0000\ 0000_H$**



Field	Bits	Type	Description
CRC	[10:0]	rw	**Header CRC** (vRF!Header!HeaderCRC) Receive Buffer: Configuration not required Transmit Buffer: Header CRC calculated and configured by the Host. For calculation of the Header CRC the payload length of the Frame send on the bus has to be considered. In static segment the payload length of all Frames is configured by MHDC.SFDL.
PLC	[22:16]	rw	**Payload Length Configured** Length of Data Section (number of 2-byte words) as configured by the Host. During static segment the static Frame payload length as configured by MHDC.SFDL in the MHD Configuration Register defines the payload length for all static Frames. If the payload length configured by PLC is shorter than this value padding byte are inserted to ensure that Frames have proper physical length. The padding pattern is logical zero.
0	[15:11], [31:23]	r	**Reserved** Returns 0 if read; should be written with 0.

Write Header Section 3 (WRHS3)

WRHS3
Write Header Section 3 **(0508_H)** **Reset Value: $0000\ 0000_H$**



Field	Bits	Type	Description
DP	[10:0]	rw	**Data Pointer** Pointer to the first 32-bit word of the Data Section of the addressed Message Buffer in the Message RAM.
0	[31:11]	r	**Reserved** Returns 0 if read; should be written with 0.

Input Buffer Command Mask (IBCM)

Configures how the Message Buffer in the Message RAM selected by the Input Buffer Command Request register IBCR is updated. If IBF Host and IBF Shadow are swapped, also masked bits IBCM.LHSH, IBCM.LDSH, and IBCM.STXRH are swapped with bits IBCM.LHSS, IBCM.LDSS, and IBCM.STXRS to keep them attached to the respective Input Buffer transfer.

IBCM
Input Buffer Command Mask **(0510_H)** **Reset Value: 0000 0000$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0													STXRS	LDSS	LHSS
r													rh	rh	rh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0													STXRH	LDSH	LHSH
r													rwh	rwh	rwh

Field	Bits	Type	Description
LHSH	0	rwh	**Load Header Section Host** 0_B Header Section is not updated 1_B Header Section selected for transfer from Input Buffer to the Message RAM
LDSH	1	rwh	**Load Data Section Host** 0_B Data Section is not updated 1_B Data Section selected for transfer from Input Buffer to the Message RAM
STXRH	2	rwh	**Set Transmission Request Host** If this bit is set to 1, the Transmission Request flag TXRQ1.TXRn (n = 0-31) to TXRQ4.TXRn (n = 0-31) for the selected Message Buffer is set in the Transmission Request Registers to release the Message Buffer for transmission. In single-shot mode the flag is cleared by the Communication Controller after transmission has completed. TXRQ1.TXRn (n = 0-31) to TXRQ4.TXRn (n = 0-31) are evaluated for transmit buffer only. 0_B Reset Transmission Request flag 1_B Set Transmission Request flag, transmit buffer released for transmission

Field	Bits	Type	Description
LHSS	16	rh	**Load Header Section Shadow** 0_B Header Section is not updated 1_B Header Section selected for transfer from Input Buffer to the Message RAM (transfer is ongoing of finalized)
LDSS	17	rh	**Load Data Section Shadow** 0_B Data Section is not updated 1_B Data Section selected for transfer from Input Buffer to the Message RAM (transfer is ongoing of finalized)
STXRS	18	rh	**Transmission Request Shadow** If this bit is set to 1, the Transmission Request flag TXRQ1.TXRn (n = 0-31) to TXRQ4.TXRn (n = 0-31) for the selected Message Buffer is set in the Transmission Request Registers to release the Message Buffer for transmission. In single-shot mode the flag is cleared by the Communication Controller after transmission has completed. TXRQ1.TXRn (n = 0-31) to TXRQ4.TXRn (n = 0-31) are evaluated for transmit buffer only. 0_B Reset Transmission Request flag 1_B Set Transmission Request flag, transmit buffer released for transmission (operation is ongoing of finalized)
0	[15:3], [31:19]	r	**Reserved** Returns 0 if read; should be written with 0.

Input Buffer Command Request (IBCR)

When the Host writes the number of the target Message Buffer in the Message RAM to IBRH in the Input Buffer Command Request register, IBF Host and IBF Shadow are swapped. In addition the Message Buffer numbers stored under IBRH and IBRS are also swapped (see also **"Data Transfer from Input Buffer to Message RAM" on Page 26-233**).

With this write operation the IBSYS bit in the Input Buffer Command Request register is set to 1. The Message Handler then starts to transfer the contents of IBF Shadow to the Message Buffer in the Message RAM selected by IBRS.

While the Message Handler transfers the data from IBF Shadow to the target Message Buffer in the Message RAM, the Host may write the next message into the IBF Host. After the transfer between IBF Shadow and the Message RAM has completed, the IBSYS bit is set back to 0 and the next transfer to the Message RAM may be started by the Host by writing the respective target Message Buffer number to IBRH.

If a write access to IBRH occurs while IBSYS is 1, IBSYH is set to 1. After completion of the ongoing data transfer from IBF Shadow to the Message RAM, IBF Host and IBF Shadow are swapped, IBSYH is reset to 0. IBSYS remains set to 1, and the next transfer to the Message RAM is started. In addition the Message Buffer numbers stored under IBRH and IBRS are also swapped. Any write access to an Input Buffer register while both IBSYS and IBSYH are set will cause the error flag EIR.IIBA to be set. In this case the Input Buffer will not be changed.

IBCR
Input Buffer Command Request (0514_H) Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
IBSYS	0								IBRS						
rh	r								rh						

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IBSYH	0								IBRH						
rh	r								rwh						

Field	Bits	Type	Description
IBRH	[6:0]	rwh	**Input Buffer Request Host** Selects the target Message Buffer in the Message RAM for data transfer from Input Buffer. Valid values are 00_H to $7F_H$ (0…127).

Field	Bits	Type	Description
IBSYH	15	rh	**Input Buffer Busy Host** Set to 1 by writing IBRH while IBSYS is still 1. After the ongoing transfer between IBF Shadow and the Message RAM has completed, the IBSYH is set back to 0. 0_B No request pending 1_B Request while transfer between IBF Shadow and Message RAM in progress
IBRS	[22:16]	rh	**Input Buffer Request Shadow** Number of the target Message Buffer actually updated/lately updated. Valid values are 00_H to $7F_H$ (0…127).
IBSYS	31	rh	**Input Buffer Busy Shadow** Set to 1 after writing IBRH. When the transfer between IBF Shadow and the Message RAM has completed, IBSYS is set back to 0. 0_B Transfer between IBF Shadow and Message RAM completed 1_B Transfer between IBF Shadow and Message RAM in progress
0	[14:7], [30:23]	r	**Reserved** Returns 0 if read; should be written with 0.

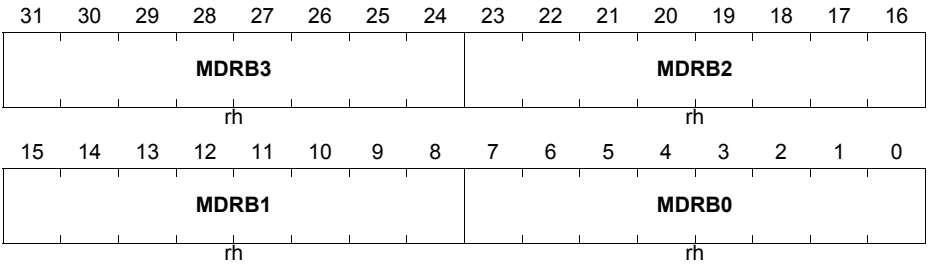
26.5.2.10 Output Buffer

Double buffer structure consisting of Output Buffer Host and Output Buffer Shadow. Used to read out Message Buffers from the Message RAM. While the Host can read from Output Buffer Host, the Message Handler transfers the selected Message Buffer from Message RAM to the respective Output Buffer Shadow. The data transfer between Message RAM and Output Buffer (OBF) is described in **"Data Transfer from Message RAM to Output Buffer" on Page 26-235**.

Read Data Section [1…64] (RDDSn)

The Read Data Section nn (RDDSnn, nn = 01-64) holds the data words read from the Data Section of the addressed Message Buffer. The data words are read from the Message RAM in reception order from DW1 (byte0, byte1) to DW_{PL} (PL = number of data words as defined by the Payload Length).

RDDSnn (nn = 01-64)
Read Data Section nn **($05FC_H$ + nn * 4)** **Reset Value: $0000\ 0000_H$**



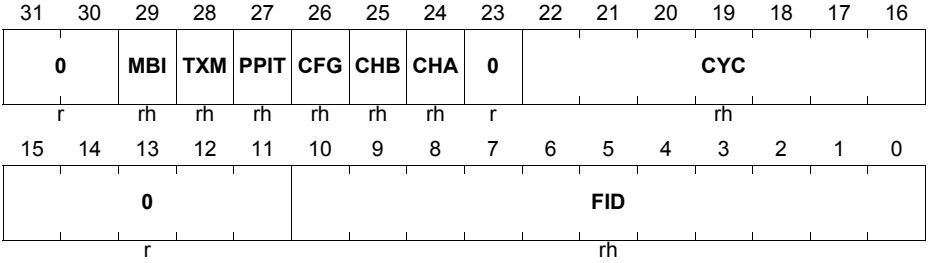
Field	Bits	Type	Description
MDRB0	[7:0]	rh	**32-Bit Word nn, Byte 0**
MDRB1	[15:8]	rh	**32-Bit Word nn, Byte 1**
MDRB2	[23:16]	rh	**32-Bit Word nn, Byte 2**
MDRB3	[31:24]	rh	**32-Bit Word nn, Byte 3**

Note: DW127 is located on RDDS64.MDW. In this case RDDS64.MDW is unused (no valid data). The Output Buffer RAMs are initialized to zero when leaving application reset or by CHI command CLEAR_RAMS.

Read Header Section 1 (RDHS1)

Values as configured by the Host via WRHS1 Register:

RDHS1
Read Header Section 1 **(0700_H)** **Reset Value: $0000\ 0000_H$**



Field	Bits	Type	Description
FID	[10:0]	rh	**Frame ID**
CYC	[22:16]	rh	**Cycle Code**
CHA	24	rh	**Channel Filter Control A**
CHB	25	rh	**Channel Filter Control B**
CFG	26	rh	**Message Buffer Direction Configuration Bit**
PPIT	27	rh	**Payload Preamble Indicator Transmit**
TXM	28	rh	**Transmission Mode**
MBI	29	rh	**Message Buffer Service Request**
0	[15:11], 23, [31:30]	r	**Reserved** Returns 0 if read; should be written with 0.

Note: In case that the Message Buffer read from the Message RAM belongs to the receive FIFO, FID holds the received Frame ID, while CYC, CHA, CHB, CFG, PPIT, TXM, and MBI are reset to zero.

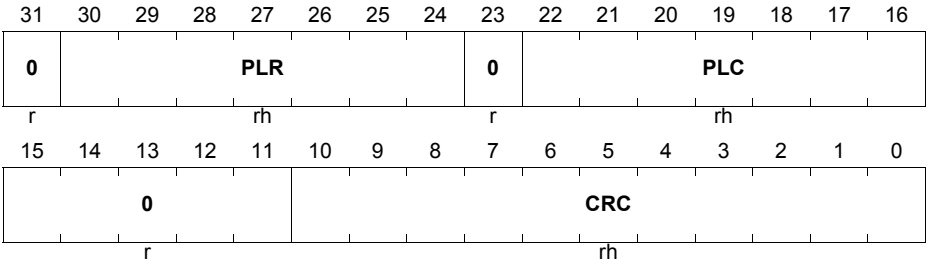
Table 26-9 Channel Filter Control Bits

CHA	CHB	Transmit Buffer transmit Frame on	Receive Buffer store Frame received from
1[1)]	1[1)]	Both Channels (static segment only)	Channel A or B (store first semantically valid Frame, static segment only)
1	0	Channel A	Channel A
0	1	Channel B	Channel B
0	0	No Transmission	Ignore Frame

1) If a Message Buffer is configured for the dynamic segment and both bits of the channel filtering field are set to 1, no Frames are transmitted resp. received Frames are ignored (same function as CHA = CHB = 0)

Read Header Section 2 (RDHS2)

RDHS2
Read Header Section 2 **(0704_H)** **Reset Value: $0000\ 0000_H$**



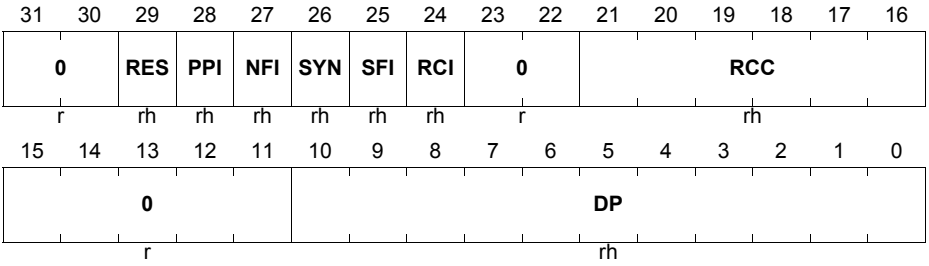
Field	Bits	Type	Description
CRC	[10:0]	rh	**Header CRC** (vRF!Header!HeaderCRC) Receive Buffer: Configuration not required. Header CRC updated from receive Data Frames. Transmit Buffer: Header CRC calculated and configured by the Host
PLC	[22:16]	rh	**Payload Length Configured** Length of Data Section (number of 2-byte words) as configured by the Host.

Field	Bits	Type	Description
PLR	[30:24]	rh	**Payload Length Received** (vRF!Header!Length) Payload length value updated from received Data Frame (exception: if Message Buffer belongs to the receive FIFO PLR is also updated from received NULL Frames). When a message is stored into a Message Buffer the following behavior with respect to payload length received and payload length configured is implemented: • **PLR > PLC:** The payload data stored in the Message Buffer is truncated to the payload length configured for even PLC or else truncated to PLC + 1. • **PLR ≤ PLC:** The received payload data is stored into the Message Buffers Data Section. The remaining data bytes of the Data Section as configured by PLC are filled with undefined data. • **PLR = 0:** The Message Buffer's Data Section is filled with undefined data. • **PLC = 0:** Message Buffer has no Data Section configured. No data is stored into the Message Buffer's Data Section.
0	[15:11], 23, 31	r	**Reserved** Returns 0 if read; should be written with 0.

Note: The Message RAM is organized in 4-byte words. When received data is stored into a Message Buffer's Data Section, the number of 2-byte data words written into the Message Buffer is PLC rounded to the next even value. PLC should be configured identical for all Message Buffers belonging to the receive FIFO. Header 2 is updated from Data Frames only.

Read Header Section 3 (RDHS3)

RDHS3
Read Header Section 3 **(0708_H)** **Reset Value: $0000\ 0000_H$**



Field	Bits	Type	Description
DP	[10:0]	rh	**Data Pointer** Pointer to the first 32-bit word of the Data Section of the addressed Message Buffer in the Message RAM.
RCC	[21:16]	rh	**Receive Cycle Count** (vRF!Header!CycleCount) Cycle counter value updated from received Data Frame.
RCI	24	rh	**Received on Channel Indicator** (vSS!Channel) Indicates the channel from which the received Data Frame was taken to update the respective receive buffer. 0_B Frame received on channel B 1_B Frame received on channel A
SFI	25	rh	**Startup Frame Indicator** (vRF!Header!SuFIndicator) A Startup Frame is marked by the Startup Frame indicator. 0_B The received Frame is not a startup Frame 1_B The received Frame is a startup Frame
SYN	26	rh	**SYNC Frame Indicator** (vRF!Header!SyFIndicator) A SYNC Frame is marked by the SYNC Frame indicator. 0_B The received Frame is not a SYNC Frame 1_B The received Frame is a SYNC Frame
NFI	27	rh	**NULL Frame Indicator** (vRF!Header!NFIndicator) Is set to 1 after storage of the first received Data Frame. 0_B Up to now no Data Frame has been stored into the respective Message Buffer 1_B At least one Data Frame has been stored into the respective Message Buffer

Field	Bits	Type	Description
PPI	28	rh	**Payload Preamble Indicator** (vRF!Header!PPIndicator) The payload preamble indicator defines whether a Network Management vector or message ID is contained within the Payload Segment of the received Frame. 0_B The Payload Segment of the received Frame does not contain a Network Management vector nor a message ID 1_B Static segment: Network Management vector in the first part of the payload Dynamic segment: Message ID in the first part of the payload
RES	29	rh	**Reserved Bit** (vRF!Header!Reserved) Reflects the state of the received reserved bit. The reserved bit is transmitted as 0.
0	[15:11], [23:22], [31:30]	r	**Reserved** Returns 0 if read; should be written with 0.

Note: Header 3 is updated from Data Frames only.

Message Buffer Status (MBS)

The Message Buffer status is updated by the Communication Controller with respect to the assigned channel(s) latest at the end of the slot following the slot assigned to the Message Buffer. The flags are updated only when the Communication Controller is in “NORMAL_ACTIVE” or “NORMAL_PASSIVE” state. If only one channel (A or B) is assigned to a Message Buffer, the channel-specific status flags of the other channel are written to zero. If both channels are assigned to a Message Buffer, the channel-specific status flags of both channels are updated. The Message Buffer status is updated only when the slot counter reached the configured Frame ID and when the cycle counter filter matched. When the Host updates a Message Buffer via Input Buffer, all MBS flags are reset to zero independent of which IBCM bits are set or not. For details about receive / transmit filtering see **“Filtering and Masking” on Page 26-222**, **“Transmit Process” on Page 26-226**, and **“Receive Process” on Page 26-229**.

Whenever the Message Handler changes one of the flags VFRA, VFRB, SEOA, SEOB, CEOA, CEOB, SVOA, SVOB, TCIA, TCIB, ESA, ESB, MLST, FTA, FTB the respective Message Buffer’s MBC flag in registers MBSC1 to MBSC4 is set

MBS

Message Buffer Status **($070C_H$)** **Reset Value: $0000\ 0000_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0		RES	PPIS	NFIS	SYNS	SFIS	RCIS	0		CCS					
r		rh	rh	rh	rh	rh	rh	r		rh					

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FTB	FTA	0	MLST	ESB	ESA	TCIB	TCIA	SVOB	SVOA	CEOB	CEOA	SEOB	SEOA	VRFB	VRFA
rh	rh	r	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh

Field	Bits	Type	Description
VFRA	0	rh	**Valid Frame Received on Channel A** (vSS!ValidFrameA) A valid Frame indication is set if a valid Frame was received on channel A. 0_B No valid Frame received on channel A 1_B Valid Frame received on channel A
VFRB	1	rh	**Valid Frame Received on Channel B** (vSS!ValidFrameB) A valid Frame indication is set if a valid Frame was received on channel B. 0_B No valid Frame received on channel B 1_B Valid Frame received on channel B

Field	Bits	Type	Description
SEOA	2	rh	**Syntax Error Observed on Channel A** (vSS!SyntaxErrorA) A syntax error was observed in the assigned slot on channel A. 0_B No syntax error observed on channel A 1_B Syntax error observed on channel A
SEOB	3	rh	**Syntax Error Observed on Channel B** (vSS!SyntaxErrorB) A syntax error was observed in the assigned slot on channel B. 0_B No syntax error observed on channel B 1_B Syntax error observed on channel B
CEOA	4	rh	**Content Error Observed on Channel A** (vSS!ContentErrorA) A content error was observed in the assigned slot on channel A. 0_B No content error observed on channel A 1_B Content error observed on channel A
CEOB	5	rh	**Content Error Observed on Channel B** (vSS!ContentErrorB) A content error was observed in the assigned slot on channel B. 0_B No content error observed on channel B 1_B Content error observed on channel B
SVOA	6	rh	**Slot Boundary Violation Observed on Channel A** (vSS!BViolationA) A slot boundary violation (channel active at the start or at the end of the assigned slot) was observed on channel A. 0_B No slot boundary violation observed on channel A 1_B Slot boundary violation observed on channel A
SVOB	7	rh	**Slot Boundary Violation Observed on Channel B** (vSS!BViolationB) A slot boundary violation (channel active at the start or at the end of the assigned slot) was observed on channel B. 0_B No slot boundary violation observed on channel B 1_B Slot boundary violation observed on channel B
TCIA	8	rh	**Transmission Conflict Indication Channel A** (vSS!TxConflictA) A transmission conflict indication is set if a transmission conflict has occurred on channel A. 0_B No transmission conflict occurred on channel A 1_B Transmission conflict occurred on channel A

Field	Bits	Type	Description
TCIB	9	rh	**Transmission Conflict Indication Channel B** (vSS!TxConflictB) A transmission conflict indication is set if a transmission conflict has occurred on channel B. 0_B No transmission conflict occurred on channel B 1_B Transmission conflict occurred on channel B
ESA	10	rh	**Empty Slot Channel A** In an empty slot there is no activity detected on the bus. The condition is checked in static and dynamic slots. 0_B Bus activity detected in the assigned slot on channel A 1_B No bus activity detected in the assigned slot on channel A
ESB	11	rh	**Empty Slot Channel B** In an empty slot there is no activity detected on the bus. The condition is checked in static and dynamic slots. 0_B Bus activity detected in the assigned slot on channel B 1_B No bus activity detected in the assigned slot on channel B
MLST	12	rh	**Message Lost** The flag is set in case the Host did not read the message before the Message Buffer was updated from a received Data Frame. Not affected by reception of NULL Frames except for Message Buffers belonging to the receive FIFO. The flag is reset by a Host write to the Message Buffer via IBF or when a new message is stored into the Message Buffer after the Message Buffers ND flag was reset by reading out the Message Buffer via OBF. 0_B No message lost 1_B Unprocessed message was overwritten
FTA	14	rh	**Frame Transmitted on Channel A** Indicates that this node has transmitted a Data Frame in the assigned slot on channel A. 0_B No transmission transmitted on channel A 1_B Data Frame transmitted on channel A in cycle defined by CCS bit field *Note: The FlexRay™ protocol specification requires that FTA can only be reset by the Host. Therefore the Cycle Count Status CCS for these bits is only valid for the cycle where the bits are set to 1*

Field	Bits	Type	Description
FTB	15	rh	**Frame Transmitted on Channel B** Indicates that this node has transmitted a Data Frame in the assigned slot on channel B. 0_B No transmission transmitted on channel B 1_B Data Frame transmitted on channel B in cycle defined by CCS bit field *Note: The FlexRay™ protocol specification requires that FTB can only be reset by the Host. Therefore the Cycle Count Status CCS for these bits is only valid for the cycle where the bits are set to 1*
CCS	[21:16]	rh	**Cycle Count Status** Cycle Count when status (MBS register) has been updated.
RCIS	24	rh	**Received on Channel Indicator Status** (vSS!Channel) Indicates the channel on which the Frame was received. 0_B Frame received on channel B 1_B Frame received on channel A *Note: For receive buffers (CFG = 0) the RCIS is updated from both valid data and NULL Frames. If no valid Frame was received, the previous value is maintained. For transmit buffers the flags have no meaning and should be ignored.*
SFIS	25	rh	**Startup Frame Indicator Status** (vRF!Header!SuFIndicator) A Startup Frame is marked by the Startup Frame indicator. 0_B No Startup Frame received 1_B The received Frame is a startup Frame *Note: For receive buffers (CFG = 0) the SFIS is updated from both valid data and NULL Frames. If no valid Frame was received, the previous value is maintained. For transmit buffers the flags have no meaning and should be ignored.*
SYNS	26	rh	**SYNC Frame Indicator Status** (vRF!Header!SyFIndicator) A Startup Frame is marked by the Startup Frame indicator. 0_B No SYNC Frame received 1_B The received Frame is a SYNC Frame *Note: For receive buffers (CFG = 0) the SYNS is updated from both valid data and NULL Frames. If no valid Frame was received, the previous value is maintained. For transmit buffers the flags have no meaning and should be ignored.*

Field	Bits	Type	Description
NFIS	27	rh	**NULL Frame Indicator Status** (vRF!Header!NFIndicator) If reset to 0 the Payload Segment of the received Frame contains no usable data. 0_B Received Frame is a NULL Frame 1_B Received Frame is not a NULL Frame *Note: For receive buffers (CFG = 0) the NFIS is updated from both valid data and NULL Frames. If no valid Frame was received, the previous value is maintained. For transmit buffers the flags have no meaning and should be ignored.*
PPIS	28	rh	**Payload Preamble Indictor Status** (vRF!Header!PPIndicator) The payload preamble indicator defines whether a Network Management vector or message ID is contained within the Payload Segment of the received Frame. Static Segment: 0_B The Payload Segment of the received Frame does not contain a Network Management vector or a message ID 1_B Network Management vector at the beginning of the payload Dynamic Segment: 0_B The Payload Segment of the received Frame does not contain a Network Management vector or a message ID 1_B Message ID at the beginning of the payload *Note: For receive buffers (CFG = 0) the PPIS is updated from both valid data and NULL Frames. If no valid Frame was received, the previous value is maintained. For transmit buffers the flags have no meaning and should be ignored.*
RESS	29	rh	**Reserved Bit Status** (vRF!Header!Reserved) Reflects the state of the received reserved bit. The reserved bit is transmitted as 0. *Note: For receive buffers (CFG = 0) the RESS is updated from both valid data and NULL Frames. If no valid Frame was received, the previous value is maintained. For transmit buffers the flags have no meaning and should be ignored.*
0	13, [23:22], [31:30]	r	**Reserved** Returns 0 if read; should be written with 0.

Output Buffer Command Mask (OBCM)

Configures how the Output Buffer is updated from the Message Buffer in the Message RAM selected by the Output Buffer Command Request register. If OBF Host and OBF Shadow are swapped, also mask bits OBCM.RDSH and OBCM.RHSH are swapped with bits OBCM.RDSS and OBCM.RHSS to keep them attached to the respective Output Buffer transfer.

OBCM
Output Buffer Command Mask **(0710_H)** **Reset Value: $0000\ 0000_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0														RDSH	RHSH
r														rh	rh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0														RDSS	RHSS
r														rwh	rwh

Field	Bits	Type	Description
RHSS	0	rwh	**Read Header Section Shadow** 0_B Header Section is not read 1_B Header Section selected for transfer from Message RAM to Output Buffer
RDSS	1	rwh	**Read Data Section Shadow** 0_B Data Section is not read 1_B Data Section selected for transfer from Message RAM to Output Buffer
RHSH	16	rh	**Read Header Section Host** 0_B Header Section is not read 1_B Header Section selected for transfer from Message RAM to Output Buffer
RDSH	17	rh	**Read Data Section Host** 0_B Data Section is not read 1_B Data Section selected for transfer from Message RAM to Output Buffer
0	[15:2], [31:18]	r	**Reserved** Returns 0 if read; should be written with 0.

Note: After the transfer of the Header Section from the Message RAM to OBF Shadow has completed, the Message Buffer status changed flag MBCn (n = 0-31) to MBCn (n = 96-127) of the selected Message Buffer in the Message Buffer Changed MBSC1 to MBSC4 registers is cleared. After the transfer of the Data Section from the Message RAM to OBF Shadow has completed, the New Data flag NDn (n = 0-31) to NDn (n = 96-127) of the selected Message Buffer in the New Data NDAT1 to NDAT4 registers is cleared.

Output Buffer Command Request (OBCR)

The Message Buffer selected by OBCR.OBRS is transferred from the Message RAM to the Output Buffer as soon as the Host has set OBCR.REQ. Bit OBCR.REQ can only be set while OBCR.OBSYS is 0 (see also **"Data Transfer from Message RAM to Output Buffer" on Page 26-235**).

After setting OBCR.REQ, OBCR.OBSYS is automatically set, and the transfer of the Message Buffer selected by OBCR.OBRS from the Message RAM to Output Buffer Shadow is started. When the transfer between the Message RAM and OBF Shadow has completed, this is signalled by clearing OBCR.OBSYS. By setting OBCR.VIEW while OBCR.OBSYS is 0, OBF Host and OBF Shadow are swapped. When Output Buffer Host and Output Buffer Shadow are swapped, also mask bits OBCM.RDSH and OBCM.RHSH are swapped with bits OBCM.RDSS and OBCM.RHSS to keep them attached to the respective Output Buffer transfer. Now the Host can read the transferred Message Buffer from OBF Host. In parallel the Message Handler may transfer the next message from the Message RAM to OBF Shadow if OBCR.VIEW and OBCR.REQ are set at the same time.

Any write access to an Output Buffer register while OBCR.OBSYS is set will cause the error flag EIR.IOBA to be set. In this case the Output Buffer will not be changed.

OBCR

Output Buffer Command Request (0714$_H$) **Reset Value: 0000 0000$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0									OBRH						
r									rh						

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OBSYS	0					REQ	VIEW	0	OBRS						
rh	r					rw	rw	r	rwh						

Field	Bits	Type	Description
OBRS	[6:0]	rw	**Output Buffer Request Shadow** Number of source Message Buffer to be transferred from the Message RAM to OBF Shadow. Valid values are 00_H to $7F_H$ (0 to 127). If the number of the first Message Buffer of the receive FIFO is written to this register the Message Handler transfers the Message Buffer addressed by the GET Index Register (GIDX, **"FIFO Function" on Page 26-230**) to OBF Shadow.
VIEW	8	rw	**View Shadow Buffer** Toggles between OBF Shadow and OBF Host. Only writeable while OBCR.OBSYS = 0. 0_B No action 1_B Swap OBF Shadow and OBF Host
REQ	9	rw	**Request Message RAM Transfer** Requests transfer of Message Buffer addressed by OBCR.OBRS from Message RAM to OBF Shadow. Only writeable while OBCR.OBSYS = 0. 0_B No request 1_B Transfer to OBF Shadow requested
OBSYS	15	rh	**Output Buffer Busy Shadow** Set to 1 after setting bit OBCR.REQ. When the transfer between the Message RAM and OBF Shadow has completed, OBCR.OBSYS is cleared again. 0_B No transfer in progress 1_B Transfer between Message RAM and OBF Shadow in progress

Field	Bits	Type	Description
OBRH	[22:16]	rh	**Output Buffer Request Host** Number of Message Buffer currently accessible by the Host via RDHS1 to RDHS3, MBS, and RDDSnn (nn = 01-64). By setting OBCR.VIEW OBF Shadow and OBF Host are swapped and the transferred Message Buffer is accessible by the Host. Valid values are 00_H to $7F_H$ (01 to 27).
0	7, [14:10], [31:23]	r	**Reserved** Returns 0 if read; should be written with 0.

26.6 Functional Description

This chapter describes the E-Ray implementation together with the related FlexRay™ protocol features. More information about the FlexRay™ protocol itself can be found in the FlexRay™ protocol specification v2.1.

Communication on FlexRay™ networks is based on Frames and symbols. The wakeup symbol (WUS) and the collision avoidance symbol (CAS) are transmitted outside the communication cycle to setup the time schedule. Frames and media access test symbols (MTS) are transmitted inside the communication cycle.

26.6.1 Communication Cycle

A communication cycle in FlexRay™ consists of the following elements:

- Static Segment
- Dynamic Segment
- Symbol Window
- Network Idle Time (NIT)

Static segment, dynamic segment, and symbol window form the Network Communication Time (NCT). For each communication channel the slot counter starts at 1 and counts up until the end of the dynamic segment is reached. Both channels share the same arbitration grid which means that they use the same synchronized Macrotick.

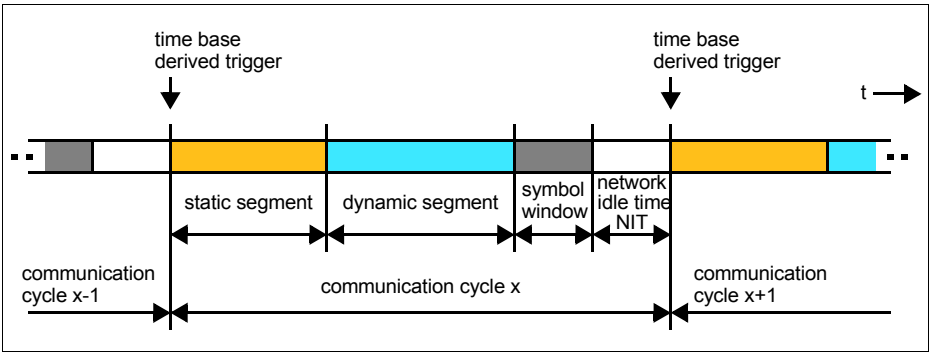


Figure 26-4 Structure of Communication Cycle

26.6.1.1 Static Segment

The Static Segment is characterized by the following features:

- Time slots of fixed length (optionally protected by bus guardian)
- Start of Frame transmission at action point of the respective static slot
- Payload length same for all Frames on both channel

Parameters: Number of Static Slots **GTUC07.NSS**, Static Slot Length **GTUC07.SSL**, Payload Length Static **MHDC.SFDL**, Action Point Offset **GTUC09.APO**.

26.6.1.2 Dynamic Segment

The Dynamic Segment is characterized by the following features:

- All controllers have bus access (no bus guardian protection possible)
- Variable payload length and duration of slots, different for both channels
- Start of transmission at minislot action point

Parameters: Number of Minislots **GTUC08.NMS**, Minislot Length **GTUC08.MSL** Minislot Action Point Offset **GTUC09.MAPO**, Start of Latest Transmit (last minislot) **MHDC.SLT**.

26.6.1.3 Symbol Window

During the symbol window only one media access test symbol (MTS) may be transmitted per channel. MTS symbols are send in “NORMAL_ACTIVE” state to test the bus guardian.

The symbol window is characterized by the following features:

- Send single symbol
- Transmission of the MTS symbol starts at the symbol windows action point

Parameters: Symbol Window Action Point Offset **GTUC09.APO** (same as for static slots), Network Idle Time Start **GTUC04.NIT**.

26.6.1.4 Network Idle Time (NIT)

During network idle time the Communication Controller has to perform the following tasks:

- Calculate clock correction terms (offset and rate)
- Distribute offset correction over multiple Macroticks
- Perform cluster cycle related tasks

Parameters: Network Idle Time Start **GTUC04.NIT**, Offset Correction Start **GTUC04.OCS**.

26.6.1.5 Configuration of Network Idle Time (NIT) Start and Offset Correction Start

The number of Macroticks per cycle (gMacroPerCycle) is assumed to be m. It is configured by programming **GTUC02.MPC** = m.

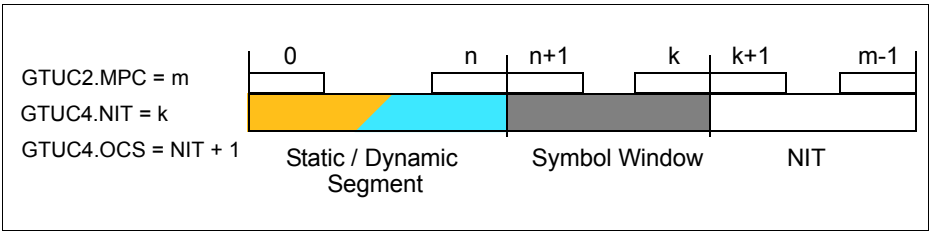


Figure 26-5 Configuration of network idle time (NIT) start and offset correction start

The static / dynamic segment starts with Macrotick 0 and ends with Macrotick n:
n = static segment length + dynamic segment offset + dynamic segment length - 1 Macrotick

n = gNumberOfStaticSlots • gdStaticSlot + dynamic segment offset
+ gNumberOfMinislots • gdMinislot - 1 Macroticks

The static segment length is configured by **GTUC07.SSL** and **GTUC07.NSS**.
The dynamic segment length is configured by **GTUC08.MSL** and **GTUC08.NMS**.

The dynamic segment offset is:

If gdActionPointOffset ≤ gdMinislotActionPointOffset:

dynamic segment offset = 0 MT

Else if gdActionPointOffset > gdMinislotActionPointOffset:

dynamic segment offset = gdActionPointOffset - gdMinislotActionPointOffset

The network idle time (NIT) starts with Macrotick k+1 and ends with the last Macrotick of cycle m-1. It has to be configured by setting **GTUC04.NIT** = k.

For the E-Ray the offset correction start is required to be

GTUC04.OCS ≥ **GTUC04.NIT** + 1 = k+1.

The length of symbol window results from the number of Macroticks between the end of the static / dynamic segment and the beginning of the NIT. It can be calculated by k - n.

26.6.2 Communication Modes

The FlexRay™ Protocol Specification v2.1 defines the Time-Triggered Distributed (TT-D) mode.

Time-triggered Distributed (TT-D)

In TT-D mode the following configurations are possible:

- **Pure static**: minimum 2 static slots + symbol window (optional)
- **Mixed static/dynamic**: minimum 2 static slots + dynamic segment + symbol window (optional)

A minimum of two coldstart nodes need to be configured for distributed time-triggered operation. Two fault-free coldstart nodes are necessary for the cluster startup. Each Startup Frame must be a SYNC Frame, therefore all coldstart nodes are sync nodes.

26.6.3 Clock Synchronization

In TT-D mode a distributed clock synchronization is used. Each node individually synchronizes itself to the cluster by observing the timing of received SYNC Frames from other nodes.

26.6.3.1 Global Time

Activities in a FlexRay™ node, including communication, are based on the concept of a global time, even though each individual node maintains its own view of it. It is the clock synchronization mechanism that differentiates the FlexRay™ cluster from other node collections with independent clock mechanisms. The global time is a vector of two values; the cycle (cycle counter) and the cycle time (Macrotick counter).

Cluster specific:

- Macrotick = basic unit of time measurement in a FlexRay™ network, a Macrotick consists of an integer number of Microticks
- Cycle length = duration of a communication cycle in units of Macroticks

26.6.3.2 Local Time

Internally, nodes time their behavior with Microtick resolution. Microticks are time units derived from the oscillator clock tick of the specific node. Therefore Microticks are controller-specific units. They may have different duration in different controllers. The precision of a node's local time difference measurements is a Microtick.

Node specific:

- Oscillator clock → prescaler → Microtick
- Microtick = basic unit of time measurement in a Communication Controller, clock correction is done in units of Microticks
- Cycle counter + Macrotick counter = nodes local view of the global time

26.6.3.3 Synchronization Process

Clock synchronization is performed by means of SYNC Frames. Only preconfigured nodes (sync nodes) are allowed to send SYNC Frames. In a two-channel cluster a sync node has to send its SYNC Frame on both channels.

For synchronization in FlexRay™ the following constraints have to be considered:

- Max. one SYNC Frame per node in one communication cycle
- Max. 15 SYNC Frames per cluster in one communication cycle
- Every node has to use all available SYNC Frames for clock synchronization
- Minimum of two sync nodes required for clock synchronization and startup

For clock synchronization the time difference between expected and observed arrival time of SYNC Frames received during the static segment, valid on both channels (two-channel cluster), is measured. The calculation of correction terms is done during network idle time (NIT) (offset: every cycle, rate: odd cycle) by using a FTA / FTM algorithm. For details see FlexRay™ protocol specification v2.1, chapter 8.

Offset (phase) Correction

- Only deviation values measured and stored in the current cycle used
- For a two channel node the smaller value will be taken
- Calculation during network idle time (NIT) of **every** communication cycle, value may be negative
- Offset correction value calculated in even cycles used for error checking only
- Checked against limit values (violation: “NORMAL_ACTIVE” → “NORMAL_PASSIVE” → “HALT”)
- Correction value is an integer number of Microticks
- Correction done in **odd** numbered cycles, distributed over the Macroticks beginning at offset correction start up to cycle end (end of network idle time (NIT)) to shift nodes next start of cycle (Macroticks lengthened / shortened)

Rate (frequency) Correction

- Pairs of deviation values measured and stored in even / odd cycle pair used
- For a two channel node the average of the differences from the two channels is used
- Calculated during network idle time (NIT) of **odd** numbered cycles, value may be negative
- Cluster drift damping is performed using global damping value

- Checked against limit values
- Correction value is a signed integer number of Microticks
- Distributed over Macroticks comprising the next **even / odd** cycle pair (Macroticks lengthened / shortened)

Synchronization Process

Clock synchronization is performed by means of SYNC Frames. Only preconfigured nodes (sync nodes) are allowed to send SYNC Frames. In a two-channel cluster a sync node has to send its SYNC Frame on both channels.

For synchronization in FlexRay™ the following constraints have to be considered:

- Max. one SYNC Frame per node in one communication cycle
- Max. 15 SYNC Frames per cluster in one communication cycle
- Every node has to use all available SYNC Frames for clock synchronization
- Minimum of two sync nodes required for clock synchronization and startup

For clock synchronization the time difference between expected and observed arrival time of SYNC Frames received during the static segment, valid on both channels (two-channel cluster), is measured. The calculation of correction terms is done during network idle time (NIT) (offset: every cycle, rate: odd cycle) by using a FTA / FTM algorithm. For details see FlexRay™ protocol specification v2.1, chapter 8.

SYNC Frame Transmission

SYNC Frame transmission is only possible from buffer 0 and 1. Message Buffer 1 may be used for SYNC Frame transmission in case that SYNC Frames should have different payloads on the two channels. In this case bit **MRC.SPLM** has to be programmed to 1.

Message Buffers used for SYNC Frame transmission have to be configured with the key slot ID and can be (re)configured in “DEFAULT_CONFIG” or “CONFIG” state only. For nodes transmitting SYNC Frames **SUCC1.TXSY** must be set to 1.

26.6.3.4 External Clock Synchronization

During normal operation, independent clusters can drift significantly. If synchronous operation across independent clusters is desired, external synchronization is necessary; even though the nodes within each cluster are synchronized. This can be accomplished with synchronous application of host-deduced rate and offset correction terms to the clusters.

- External offset / rate correction value is a signed integer
- External offset / rate correction value is added to calculated offset / rate correction value
- Aggregated offset / rate correction term (external + internal) is not checked against configured limits

26.6.4 Error Handling

The implemented error handling concept is intended to ensure that in case of a lower layer protocol error in a single node communication between non-affected nodes can be maintained. In some cases, higher layer program command activity is required for the Communication Controller to resume normal operation. A change of the error handling state will set bit **EIR.PEMC** in the Error Service Request Register and may trigger an service request to the Host if enabled. The actual error mode is signalled by **CCEV.ERRM** in the Communication Controller Error Vector register.

Table 26-10 Error Modes of the POC (Degradation Model)

Error Mode	Activity
ACTIVE (green)	**Full operation**, State: “NORMAL_ACTIVE” The Communication Controller is fully synchronized and supports the cluster wide clock synchronization. The host is informed of any error condition(s) or status change by interrupt (if enabled) or by reading the error and status interrupt flags from registers **EIR** and **SIR**.
PASSIVE (yellow)	**Reduced operation**, State: “NORMAL_PASSIVE”, Communication Controller self rescue allowed The Communication Controller stops transmitting Frames and symbols, but received Frames are still processed. Clock synchronization mechanisms are continued based on received Frames. No active contribution to the cluster wide clock synchronization. The host is informed of any error condition(s) or status change by interrupt (if enabled) or by reading the error and status interrupt flags from registers **EIR** and **SIR**.
COMM_HALT (red)	**Operation halted**, State: “HALT”, Communication Controller self rescue not allowed The Communication Controller stops Frame and symbol processing, clock synchronization processing, and the Macrotick generation. The host has still access to error and status information by reading the error and status interrupt flags from registers **EIR** and **SIR**. The bus drivers are disabled.

26.6.4.1 Clock Correction Failed Counter

When the Clock Correction Failed Counter reaches the maximum “without clock correction passive” limit defined by **SUCC3.WCP**, the POC transits from “NORMAL_ACTIVE” to “NORMAL_PASSIVE” state. When it reaches the “maximum without clock correction fatal” limit defined by **SUCC3.WCF**, it transits “NORMAL_ACTIVE” or “NORMAL_PASSIVE” to the “HALT” state. Both limits are defined in the SUC Configuration Register 3.

The Clock Correction Failed Counter **CCEV.CCFC** allows the Host to monitor the duration of the inability of a node to compute clock correction terms after the Communication Controller passed protocol startup phase. It will be incremented by one at the end of any **odd** numbered communication cycle where either the Missing Offset Correction signal **SFS.MOCS** nor the Missing Rate Correction signal **SFS.MRCS** flag is set. The two flags are located in the SYNC Frame Status register, while the Clock Correction Failed Counter is located in the Communication Controller Error Vector register.

The Clock Correction Failed Counter is reset to zero at the end of an **odd** communication cycle if neither the Missing Offset Correction signal **SFS.MOCS** nor the Missing Rate Correction signal **SFS.MRCS** flag is set.

The Clock Correction Failed Counter stops incrementing when the “maximum without clock correction fatal” value **SUCC3.WCF** as defined in the SUC Configuration Register 3 is reached (i.e. incrementing the counter at its maximum value will not cause it to “wraparound” back to zero). The Clock Correction Failed Counter is initialized to zero when the Communication Controller enters “READY” state or when “NORMAL_ACTIVE” state is entered.

26.6.4.2 Passive to Active Counter

The passive to active counter controls the transition of the POC from “NORMAL_PASSIVE” to “NORMAL_ACTIVE” state. **SUCC1.PTA** in the SUC Configuration Register 1 defines the number of consecutive even / odd cycle pairs that must have valid clock correction terms before the Communication Controller is allowed to transit from “NORMAL_PASSIVE” to “NORMAL_ACTIVE” state. If **SUCC1.PTA** is reset to zero the Communication Controller is not allowed to transit from “NORMAL_PASSIVE” to “NORMAL_ACTIVE” state.

26.6.4.3 HALT Command

In case the Host wants to stop FlexRay™ communication of the local node it can bring the Communication Controller into “HALT” state by asserting the HALT command. This can be done by writing **SUCC1.CMD** = 0110_B in the SUC Configuration Register 1. When called in “NORMAL_ACTIVE” or “NORMAL_PASSIVE” state the POC transits to “HALT” state at the end of the current cycle. When called in any other state **SUCC1.CMD** will be reset to 0000_B = “COMMAND_NOT_ACCEPTED” and bit **EIR.CNA** in the Error Service Request Register is set to 1. If enabled an service request to the Host is generated.

26.6.4.4 FREEZE Command

In case the Host detects a severe error condition it can bring the Communication Controller into “HALT” state by asserting the FREEZE command. This can be done by writing **SUCC1.CMD** = 0111_B in the SUC Configuration Register 1. The FREEZE

command triggers the entry of the “HALT” state immediately regardless of the actual POC state.

The POC state from which the transition to HALT state took place can be read from **CCSV.PSL**.

26.6.5 Communication Controller States

This chapter introduces the states of the Communication Controller.

26.6.5.1 Communication Controller State Diagram

State transitions are controlled by externals the application reset or RXDA/B, by the POC state machine, and by the CHI Command Vector **SUCC1.CMD** located in the SUC Configuration Register 1.

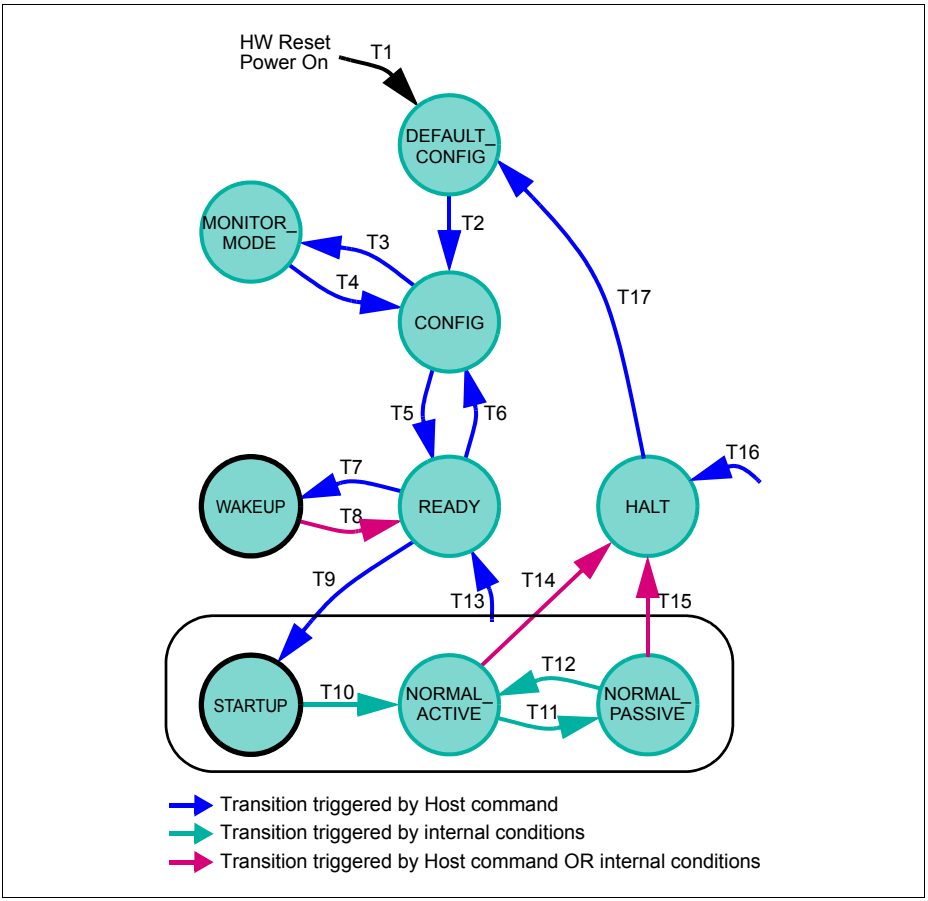


Figure 26-6 Overall State Diagram of E-Ray Communication Controller

The Communication Controller exits from all states to “HALT” state after application of the FREEZE command (SUCC1.CMD = 0111_B).

Table 26-11 State Transitions of E-Ray Overall State Machine

T#	Condition	From	To
1	application reset	HW Reset	DEFAULT_CONFIG
2	Command CONFIG, SUCC1.CMD = 0001_B	DEFAULT_CONFIG	CONFIG
3	Unlock sequence followed by command MONITOR_MODE, SUCC1.CMD = 1011_B	CONFIG	MONITOR_MODE
4	Command CONFIG, SUCC1.CMD = 0001_B	MONITOR_MODE	CONFIG
5	Unlock sequence followed by command READY, SUCC1.CMD = 0010_B	CONFIG	READY
6	Command CONFIG, SUCC1.CMD = 0001_B	READY	CONFIG
7	Command WAKEUP, SUCC1.CMD = 0011_B	READY	WAKEUP
8	Complete, non-aborted transmission of wakeup pattern OR received WUP OR received Frame Header OR command READY, SUCC1.CMD = 0010_B	WAKEUP	READY
9	Command RUN, SUCC1.CMD = 0100_B	READY	STARTUP
10	Successful startup	STARTUP	NORMAL_ACTIVE
11	Clock Correction Failed counter reached Maximum Without Clock Correction Passive limit configured by WCP in SUC Configuration Register 3	NORMAL_ACTIVE	NORMAL_PASSIVE
12	Number of valid correction terms reached the Passive to Active limit configured by PTA in SUC Configuration Register 1	NORMAL_PASSIVE	NORMAL_ACTIVE
13	Command READY, SUCC1.CMD = 0010_B	STARTUP, NORMAL_ACTIVE, NORMAL_PASSIVE	READY

Table 26-11 State Transitions of E-Ray Overall State Machine (cont'd)

T#	Condition	From	To
14	Clock Correction Failed counter reached Maximum Without Clock Correction Fatal limit configured by WCF in SUC Configuration Register 3 AND bit HCSE in the SUC Configuration Register 1 set to 1 OR command HALT, SUCC1.CMD = 0110_B	NORMAL_ACTIVE	HALT
15	Clock Correction Failed counter reached Maximum Without Clock Correction Fatal limit configured by WCF in SUC Configuration Register 3 AND bit HCSE in the SUC Configuration Register 1 set to 1 OR command HALT, SUCC1.CMD = 0110_B	NORMAL_PASSIVE	HALT
16	Command FREEZE, SUCC1.CMD = 0111_B	All States	HALT
17	Command CONFIG, SUCC1.CMD = 0001_B	HALT	DEFAULT_CONFIG

26.6.5.2 DEFAULT_CONFIG State

In "DEFAULT_CONFIG" state, the Communication Controller is stopped. All configuration registers are accessible and the pins to the physical layer are in their inactive state.

The Communication Controller enters this state

- When leaving application reset
- When exiting from "HALT" state

To leave "DEFAULT_CONFIG" state the Host has to write SUCC1.CMD = 0001_B in the SUC Configuration Register 1. The Communication Controller transits to "CONFIG" state.

CONFIG State

In "CONFIG" state, the Communication Controller is stopped. All configuration registers are accessible and the pins to the physical layer are in their inactive state. This state is used to initialize the Communication Controller configuration.

The Communication Controller enters this state

- When exiting from “DEFAULT_CONFIG” state
- When exiting from “MONITOR_MODE” or “READY” state

When the state has been entered via “HALT” and “DEFAULT_CONFIG” state, the Host can analyze status information and configuration. Before leaving “CONFIG” state the Host has to assure that the configuration is fault-free.

To leave “CONFIG” state, the Host has to perform the unlock sequence as described on **“LCK” on Page 26-39**. Directly after unlocking the “CONFIG” state the Host has to write **SUCC1.CMD** in the SUC Configuration Register 1 to enter the next state.

Internal counters and the Communication Controller status flags are reset when the Communication Controller leaves “CONFIG”.

*Note: The Message Buffer Status Registers (**MHDS**, **TXRQ1** to **TXRQ4**, **NDAT1** to **NDAT4**, **MBSC1** to **MBSC4**) and status data stored in the Message RAM and are not affected by the transition of the POC from “CONFIG” to “READY” state.*

When the Communication Controller is in “CONFIG” state it is also possible to bring the Communication Controller into a power saving mode by halting the module clocks (f_{SCLK}, f_{CLC_ERAY}). To do this the Host has to assure that all Message RAM transfers have finished before turning off the clocks.

26.6.5.3 MONITOR_MODE

After unlocking “CONFIG” state and writing **SUCC1.CMD** = 0011_B the Communication Controller enters “MONITOR_MODE”. In this mode the Communication Controller is able to receive FlexRay™ Frames and to detect wakeup pattern. The temporal integrity of received Frames is not checked, and therefore cycle counter filtering is not supported. It is not possible to distinguish between static and dynamic frames, because limited functions in Monitor Mode (FRF.RSS will be ignored, filtering not functional).This mode can be used for debugging purposes in case e.g. that startup of a FlexRay™ network fails. After writing **SUCC1.CMD** = 0001_B the Communication Controller transits back to “CONFIG” state.

In MONITOR_MODE the pick first valid mechanism is disabled. This means that a receive Message Buffer may only be configured to receive on one channel. Received Frames are stored into Message Buffers according to Frame ID and receive channel. NULL Frames are handled like Data Frames. After Frame reception only status bits **MBS.VFRA**, **MBS**, **MBS.MLST**, **MBS.RCIS**, **MBS.SFIS**, **MBS.SYNS**, **MBS.NFIS**, **MBS.PPIS**, **MBS.RESS** have valid value.

In “MONITOR_MODE” the Communication Controller is not able to distinguish between CAS and MTS symbols. In case one of these symbols is received on one or both of the two channels, the flags **SIR.MTSA** resp. **SIR.MTSB** are set. **SIR.CAS** has no function in “MONITOR_MODE”.

26.6.5.4 READY State

After unlocking “CONFIG” state and writing **SUCC1.CMD** = 0010_B the Communication Controller enters “READY” state. From this state the Communication Controller can transit to WAKEUP state and perform a cluster wakeup or to “STARTUP” state to perform a coldstart or to integrate into a running communication.

The Communication Controller enters this state

- When exiting from “CONFIG”, “WAKEUP”, “STARTUP”, “NORMAL_ACTIVE”, or “NORMAL_PASSIVE” state by writing **SUCC1.CMD** = 0010_B (READY command).

The Communication Controller exits from this state

- To “CONFIG” state by writing **SUCC1.CMD** = 0001_B (CONFIG command)
- To “WAKEUP” state by writing **SUCC1.CMD** = 0011_B (WAKEUP command)
- To “STARTUP” state by writing **SUCC1.CMD** = 0100_B (RUN command)

Internal counters and the Communication Controller status flags are reset when the Communication Controller enters “STARTUP” state.

*Note: Status bits **MHDS**, registers **TXRQ1** to **TXRQ4**, and status data stored in the Message RAM are not affected by the transition of the POC from “READY” to “STARTUP” state.*

26.6.5.5 WAKEUP State

The description below is intended to help configuring wakeup for the E-Ray IP-module. A detailed description of the wakeup procedure together with the respective SDL diagrams can be found in the FlexRay™ protocol specification v2.1, section 7.1.

The Communication Controller enters this state

- When exiting from “READY” state by writing **SUCC1.CMD** = 0011_B (WAKEUP command).

The Communication Controller exits from this state to “READY” state

- After complete non-aborted transmission of wakeup pattern
- After WUP reception
- After detecting a WUP collision
- After reception of a Frame Header
- By writing **SUCC1.CMD** = 0010_B (READY command)

The cluster wakeup must precede the communication startup in order to ensure that all mechanisms defined for the startup work properly. The minimum requirement for a cluster wakeup is that all bus drivers are supplied with power. A bus driver has the ability to wake up the other components of its node when it receives a wakeup pattern on its channel. At least one node in the cluster needs an **external** wakeup source.

The Host completely controls the wakeup procedure. It is informed about the state of the cluster by the bus driver and the Communication Controller and configures bus guardian

(if available) and Communication Controller to perform the cluster wakeup. The Communication Controller provides to the Host the ability to transmit a special wakeup pattern on each of its available channels separately. The Communication Controller needs to recognize the wakeup pattern only during “WAKEUP” state.

Wakeup may be performed on only one channel at a time. The Host has to configure the wakeup channel while the Communication Controller is in “CONFIG” state by writing bit **SUCC1.WUCS** in the SUC Configuration Register 1. The Communication Controller ensures that ongoing communication on this channel is not disturbed. The Communication Controller cannot guarantee that all nodes connected to the configured channel awake upon the transmission of the wakeup pattern, since these nodes cannot give feedback until the startup phase. The wakeup procedure enables single-channel devices in a two-channel system to trigger the wakeup, by only transmitting the wakeup pattern on the single channel to which they are connected. Any coldstart node that deems a system startup necessary will then wake the remaining channel before initiating communication startup.

The wakeup procedure tolerates any number of nodes simultaneously trying to wakeup a single channel and resolves this situation such that only one node transmits the pattern. Additionally the wakeup pattern is collision resilient, so even in the presence of a fault causing two nodes to simultaneously transmit a wakeup pattern, the resulting collided signal can still wake the other nodes.

After wakeup the Communication Controller returns to “READY” state and signals the change of the wakeup status to the Host by setting bit **SIR.WST** in the Status Service Request Register. The wakeup status vector can be read from the Communication Controller Status Vector register **CCSV.WSV**. If a valid wakeup pattern was received also either flag **SIR.WUPA** or flag **SIR.WUPB** in the Status Service Request Register is set.

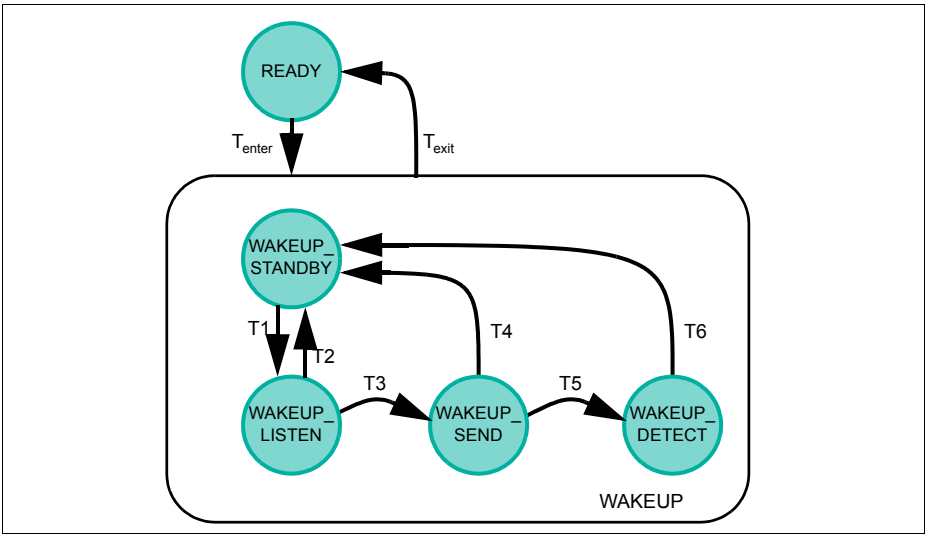


Figure 26-7 Structure of POC State WAKEUP

Table 26-12 State Transitions WAKEUP

T#	Condition	From	To
enter	Host commands change to “WAKEUP” state by writing **SUCC1.CMD** = 0011_B (WAKEUP command)	READY	WAKEUP
1	CHI command WAKEUP triggers wakeup FSM to transit to “WAKEUP_LISTEN” state	WAKEUP_ STANDBY	WAKEUP_ LISTEN
2	Received WUP on wakeup channel selected by flag **SUCC1.WUCS** in the SUC Configuration Register 1 OR Frame Header on either available channel	WAKEUP_ LISTEN	WAKEUP_ STANDBY
3	Timer event	WAKEUP_ LISTEN	WAKEUP_ SEND
4	Complete, non-aborted transmission of wakeup pattern	WAKEUP_ SEND	WAKEUP_ STANDBY

Table 26-12 State Transitions WAKEUP (cont'd)

T#	Condition	From	To
5	Collision detected	WAKEUP_ SEND	WAKEUP_ DETECT
6	Wakeup timer expired OR WUP detected on wakeup channel selected by flag **SUCC1.WUCS** in the SUC Configuration Register 1 OR Frame Header received on either available channel	WAKEUP_ DETECT	WAKEUP_ STANDBY
exit	Wakeup completed (after T2 or T4 or T6) OR Host commands change to "READY" state by writing **SUCC1.CMD** = 0010_B (READY command). This command also resets the wakeup FSM to "WAKEUP_STANDBY" state	WAKEUP	READY

The "WAKEUP_LISTEN" state is controlled by the wakeup timer and the wakeup noise timer. The two timers are controlled by the parameters listen time-out **SUCC2.LT** and listen time-out noise **SUCC2.LTN**. Both values can be configured in the SUC Configuration Register 2. listen time-out enables a fast cluster wakeup in case of a noise free environment, while listen time-out noise enables wakeup under more difficult conditions regarding noise interference.

In "WAKEUP_SEND" state the Communication Controller transmits the wakeup pattern on the configured channel and checks for collisions. After return from wakeup the Host has to bring the Communication Controller into "STARTUP" state by CHI command RUN.

In "WAKEUP_DETECT" state the Communication Controller attempts to identify the reason for the wakeup collision detected in "WAKEUP_SEND" state. The monitoring is bounded by the expiration of listen time-out as configured by **SUCC2.LT** in the SUC Configuration Register 2. Either the detection of a wakeup pattern indicating a wakeup attempt by another node or the reception of a Frame Header indication existing communication, causes the direct transition to "READY" state. Otherwise WAKEUP_DETECT is left after expiration of listen time-out; in this case the reason for wakeup collision is unknown.

The Host has to be aware of possible failures of the wakeup and act accordingly. It is advisable to delay any potential startup attempt of the node having instigated the wakeup by the minimal time it takes another coldstart node to become awake and to be configured.

The FlexRay™ Protocol Specification v2.1 recommends that two different Communication Controllers shall awake the two channels.

Host activities

The host must coordinate the wakeup of the two channels and must decide whether, or not, to wake a specific channel. The sending of the wakeup pattern is initiated by the Host and generated by the Communication Controller. The wakeup pattern is detected by the remote BDs and signalled to their local Hosts.

Wakeup procedure controlled by Host (single-channel wakeup):

- Configure the Communication Controller in “CONFIG” state
  - Select wakeup channel by programming bit **SUCC1.WUCS**
- Check local BDs whether a WUP was received
- Activate BD of selected wakeup channel
- Command Communication Controller to start wakeup on the configured channel by writing **SUCC1.CMD** = 0011_B
  - Communication Controller enters “WAKEUP
  - Communication Controller returns to “READY” state and signals status of wakeup attempt to Host
- Wait predefined time to allow the other nodes to wakeup and configure themselves
- Coldstart node: wait for WUP on the other channel
  - In a dual channel cluster wait for WUP on the other channel
  - Reset coldstart inhibit flag **CCSV.CSI** by writing **SUCC1.CMD** = 1001_B (ALLOW_COLDSTART command))
- Reset Coldstart Inhibit flag **CCSV.CSI** in the CCSV register by writing **SUCC1.CMD** = 1001_B (ALLOW_COLDSTART command), coldstart node only
- Command Communication Controller to enter startup by writing **SUCC1.CMD** = 0100_B (RUN command)

Wakeup procedure triggered by BD:

- Wakeup recognized by BD
- BD triggers power-up of Host (if required)
- BD signals wakeup event to Host
- Host configures its local Communication Controller
- If necessary Host commands wakeup of second channel and waits predefined time to allow the other nodes to wakeup and configure themselves
- Host commands Communication Controller to enter “STARTUP” state by writing **SUCC1.CMD** = 0100_B (RUN command)

Wakeup pattern (WUP)

The wakeup pattern is composed of at least two wakeup symbols (WUS). Wakeup symbol and wakeup pattern are configured by the PRT Configuration Registers **PRTC1** and **PRTC2**.

- Single channel wakeup, wakeup symbol may not be sent on both channels at the same time

- Wakeup symbol collision resilient for up to two sending nodes (two overlapping wakeup symbols still recognizable)
- Wakeup symbol must be configured identical in all nodes of a cluster
- Wakeup symbol transmit low time configured by **PRTC2.TXL**
- Wakeup symbol idle time used to listen for activity on the bus, configured by **PRTC2.TXI**
- A wakeup pattern composed of at least two Tx-wakeup symbols needed for wakeup
- Number of repetitions configurable by **PRTC1.RWP** (2 to 63 repetitions)
- Wakeup symbol receive window length configured by **PRTC1.RXW**
- Wakeup symbol receive low time configured by **PRTC2.RXL**
- Wakeup symbol receive idle time configured by **PRTC2.RXI**

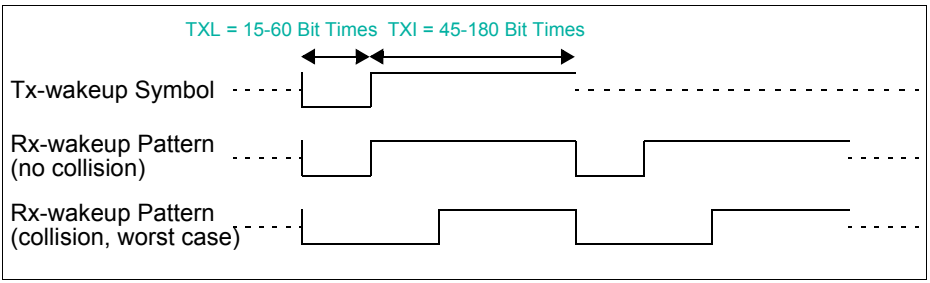


Figure 26-8 Timing of Wakeup Pattern

26.6.5.6 STARTUP State

The description below is intended to help configuring startup for the E-Ray IP-module. A detailed description of the startup procedure together with the respective SDL diagrams can be found in the FlexRay™ protocol specification v2.1, section 7.2.

Any node entering “STARTUP” state that has coldstart capability should assure that both channels attached have been awakened before initiating coldstart.

It cannot be assumed that all nodes and stars need the same amount of time to become completely awake and to be configured. Since at least two nodes are necessary to start up the cluster communication, it is advisable to delay any potential startup attempt of the node having instigated the wakeup by the minimal amount of time it takes another coldstart node to become awake, to be configured and to enter startup. It may require several hundred milliseconds (depending on the hardware used) before all nodes and stars are completely awakened and configured.

Startup is performed on all channels synchronously. During startup, a node only transmits startup Frames.

A fault-tolerant, distributed startup strategy is specified for initial synchronization of all nodes. In general, a node may enter “NORMAL_ACTIVE” state via (see **Figure 26-9**):

- Coldstart path initiating the schedule synchronization (leading coldstart node)
- Coldstart path joining other coldstart nodes (following coldstart node)
- Integration path integrating into an existing communication schedule (all other nodes)

A coldstart attempt begins with the transmission of a collision avoidance symbol (CAS). Only a coldstart node that had transmitted the CAS transmits Frames in the first four cycles after the CAS, it is then joined firstly by the other coldstart nodes and afterwards by all other nodes.

A coldstart node has the Transmit SYNC Frame in Key Slot bits **SUCC1.TXST** and **SUCC1.TXSY** in the SUC Configuration Register 1 set to 1. The Message Buffer 0 holds the key slot ID which defines the slot number where the Startup Frame is send. In the Frame Header of the Startup Frame the Startup Frame indicator bit is set.

In clusters consisting of three or more nodes, at least three nodes shall be configured to be coldstart nodes. In clusters consisting of two nodes, both nodes must be coldstart nodes. At least two fault-free coldstart nodes are necessary for the cluster to startup.

Each Startup Frame must also be a SYNC Frame; therefore each coldstart node will also be a sync node. The number of coldstart attempts is configured by **SUCC1.CSA** in the SUC Configuration Register 1.

A non-coldstart node requires at least two startup Frames from distinct nodes for integration. It may start integration before the coldstart nodes have finished their startup. It will not finish its startup until at least two coldstart nodes have finished their startup.

Both non-coldstart nodes and coldstart nodes start passive integration via the integration path as soon as they receive SYNC Frames from which to derive the TDMA schedule information. During integration the node has to adapt its own clock to the global clock (rate and offset) and has to make its cycle time consistent with the global schedule observable at the network. Afterwards, these settings are checked for consistency with all available network nodes. The node can only leave the integration phase and actively participate in communication when these checks are passed.

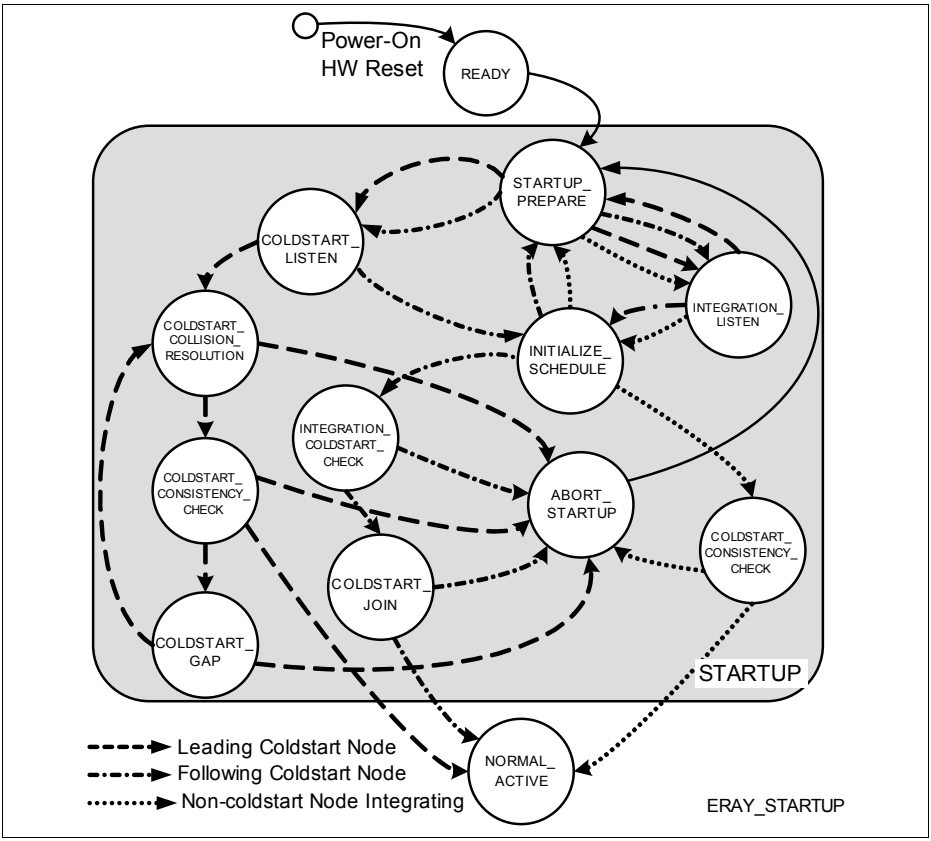


Figure 26-9 State Diagram Time-Triggered Startup

Coldstart Inhibit Mode

In coldstart inhibit mode the node is prevented from initializing the TDMA communication schedule. If bit **CCSV.CSI** in the Communication Controller Status Vector register is set, the node is not allowed to initialize the cluster communication, i.e. entering the coldstart path is prohibited. The node is allowed to integrate to a running cluster or to transmit startup Frames after another coldstart node started the initialization of the cluster communication.

The coldstart inhibit bit **CCSV.CSI** is set whenever the POC enters “READY” state. The bit has to be cleared under control of the Host by CHI command ALLOW_COLDSTART (**SUCC1.CMD** = 1001_B)

26.6.5.7 Startup Time-outs

The Communication Controller supplies two different Microtick timers supporting two time-out values, startup time-out and startup noise time-out. The two timers are reset when the Communication Controller enters the “COLDSTART_LISTEN” state. The expiration of either of these timers causes the node to leave the initial sensing phase (“COLDSTART_LISTEN” state) with the intention of starting up communication.

*Note: The startup and startup noise timers are identical with the wakeup and wakeup noise timers and use the same configuration values **SUCC2.LT** and **SUCC2.LTN** from the SUC Configuration Register 2.*

Startup Time-out

The startup time-out limits the listen time used by a node to determine if there is already communication between other nodes or at least one coldstart node actively requesting the integration of others.

The startup timer is configured by programming **SUCC2.LT** (pdListenTimeout) in the SUC Configuration Register 2.

The startup timer is restarted upon:

- Entering the “COLDSTART_LISTEN” state
- Both channels reaching idle state while in “COLDSTART_LISTEN” state

The startup timer is stopped:

- If communication channel activity is detected on one of the configured channels while the node is in the “COLDSTART_LISTEN” state
- When the “COLDSTART_LISTEN” state is left

Once the startup time-out expires, neither an overflow nor a cyclic restart of the timer is performed. The timer status is kept for further processing by the startup state machine.

Startup Noise Time-out

At the same time the startup timer is started for the first time (transition from “STARTUP_PREPARE” state to “COLDSTART_LISTEN” state), the startup noise timer is started. This additional time-out is used to improve reliability of the startup procedure in the presence of noise.

The startup noise timer is configured by programming **SUCC2.LTN** (gListenNoise - 1) in the SUC Configuration Register 2 (see **“SUC Configuration Register 2 (SUCC2)” on Page 26-96**).

The startup noise time-out is:
pdListenTimeout • ´gListenNoise = **SUCC2.LT** • (**SUCC2.LTN** + 1)

The startup noise timer is restarted upon:

- Entering the “COLDSTART_LISTEN” state
- Reception of correctly decoded Headers or CAS symbols while the node is in “COLDSTART_LISTEN” state

The startup noise timer is stopped when the “COLDSTART_LISTEN” state is left.

Once the startup noise time-out expires, neither an overflow nor a cyclic restart of the timer is performed. The status is kept for further processing by the startup state machine. Since the startup noise timer won’t be restarted when random channel activity is sensed, this time-out defines the fall-back solution that guarantees that a node will try to start up the communication cluster even in the presence of noise.

26.6.5.8 Path of leading Coldstart Node (initiating coldstart)

When a coldstart node enters “COLDSTART_LISTEN”, it listens to its attached channels.

If no communication is detected, the node enters the “COLDSTART_COLLISION_RESOLUTION” state and commences a coldstart attempt. The initial transmission of a CAS symbol is succeeded by the first regular cycle. This cycle has the number zero.

From cycle zero on, the node transmits its startup Frame. Since each coldstart node is allowed to perform a coldstart attempt, it may occur that several nodes simultaneously transmit the CAS symbol and enter the coldstart path. This situation is resolved during the first four cycles after CAS transmission.

As soon as a node that initiates a coldstart attempt receives a CAS symbol or a Frame Header during these four cycles, it re-enters the “COLDSTART_LISTEN” state. Thereby, only one node remains in this path. In cycle four, other coldstart nodes begin to transmit their startup Frames.

After four cycles in “COLDSTART_COLLISION_RESOLUTION” state, the node that initiated the coldstart enters the “COLDSTART_CONSISTENCY_CHECK” state. It collects all startup Frames from cycle four and five and performs the clock correction. If the clock correction does not deliver any errors and it has received at least one valid Startup Frame pair, the node leaves “COLDSTART_CONSISTENCY_CHECK” and enters “NORMAL_ACTIVE” state.

The number of coldstart attempts that a node is allowed to perform is configured by **SUCC1.CSA** in the SUC Configuration Register 1. The number of remaining coldstarts attempts **CCSV.RCA** can be read from Communication Controller Status Vector register. The number of remaining attempts is reduced by one for each attempted coldstart. A node may enter the “COLDSTART_LISTEN” state only if this value is larger than one and it may enter the “COLDSTART_COLLISION_RESOLUTION” state only if this value is larger than zero. If the number of coldstart attempts is one, coldstart is inhibited but integration is still possible.

Path of following Coldstart Node (responding to leading Coldstart Node)

When a coldstart node enters the “COLDSTART_LISTEN” state, it tries to receive a valid pair of startup Frames to derive its schedule and clock correction from the leading coldstart node.

As soon as a valid Startup Frame has been received the “INITIALIZE_SCHEDULE” state is entered. If the clock synchronization can successfully receive a matching second valid Startup Frame and can derive a schedule from this startup Frames, the “INTEGRATION_COLDSTART_CHECK” state is entered.

In “INTEGRATION_COLDSTART_CHECK” state it is assured that the clock correction can be performed correctly and that the coldstart node from which this node has initialized its schedule is still available. The node collects all SYNC Frames and performs clock correction in the following double-cycle. If clock correction does not signal any errors and if the node continues to receive sufficient Frames from the same node it has integrated on, the “COLDSTART_JOIN” state is entered.

In “COLDSTART_JOIN” state integrating coldstart nodes begin to transmit their own startup Frames. Thereby the node that initiated the coldstart and the nodes joining it can check if their schedules agree to each other. If for the following three cycles the clock correction does not signal errors and at least one other coldstart node is visible, the node leaves “COLDSTART_JOIN” state and enters “NORMAL_ACTIVE” state. Thereby it leaves “STARTUP” at least one cycle after the node that initiated the coldstart.

Path of Non-coldstart Node

When a non-coldstart node enters the INTEGRATION_LISTEN state, it listens to its attached channels and tries to receive FlexRay™ Frames.

As soon as a valid Startup Frame has been received the “INITIALIZE_SCHEDULE” state is entered. If the clock synchronization can successfully receive a matching second valid Startup Frame and derive a schedule from this, the INTEGRATION_CONSISTENCY_CHECK state is entered.

In “INTEGRATION_CONSISTENCY_CHECK” state it is verified that the clock correction can be performed correctly and that enough coldstart nodes (at least 2) send startup Frames that agree to the nodes own schedule. Clock correction is activated, and if any errors are signalled, the integration attempt is aborted.

During the first even cycle in this state, either two valid startup Frames or the Startup Frame of the node that this node has integrated on must be received; otherwise the node aborts the integration attempt.

During the first double-cycle in this state, either two valid Startup Frame pairs or the Startup Frame pair of the node that this node has integrated on must be received; otherwise the node aborts the integration attempt.

If after the first double-cycle less than two valid startup Frames are received within an even cycle, or less than two valid Startup Frame pairs are received within a double-cycle, the startup attempt is aborted.

Nodes in this state need to see two valid Startup Frame pairs for two consecutive double-cycles each to be allowed to leave STARTUP and enter NORMAL_OPERATION. Consequently, they leave startup at least one double-cycle after the node that initiated the coldstart and only at the end of a cycle with an odd cycle number.

26.6.5.9 NORMAL_ACTIVE State

As soon as the node that transmitted the first CAS symbol (resolving the potential access conflict and entering “STARTUP” via coldstart path) and one additional node have entered the “NORMAL_ACTIVE” state, the startup phase for the cluster has finished. In the “NORMAL_ACTIVE” state, all configured messages are scheduled for transmission. This includes all Data Frames as well as the SYNC Frames. Rate and offset measurement is started in all even cycles (even/odd cycle pairs required).

In “NORMAL_ACTIVE” state the Communication Controller supports regular communication functions

- The Communication Controller performs transmissions and reception on the FlexRay™ bus as configured
- Clock synchronization is running
- The Host interface is operational

The Communication Controller exits from that state to

- “HALT” state by writing **SUCC1.CMD** = 0110_B (HALT command, at the end of the current cycle)
- “HALT” state by writing **SUCC1.CMD** = 0111_B (FREEZE command, immediately)
- “HALT” state due to change of the error state from “ACTIVE” to “COMM_HALT”
- “NORMAL_PASSIVE” state due to change of the error state from “ACTIVE” to “PASSIVE”
- “READY” state by writing **SUCC1.CMD** = 0010_B (READY command)

26.6.5.10 NORMAL_PASSIVE State

“NORMAL_PASSIVE” state is entered from “NORMAL_ACTIVE” state when the error state changes from ACTIVE (green) to PASSIVE (yellow).

In “NORMAL_PASSIVE” state, the node is able to receive all Frames (node is fully synchronized and performs clock synchronization). In comparison to the “NORMAL_ACTIVE” state the node does not actively participate in communication, i.e. neither symbols nor Frames are transmitted.

In “NORMAL_PASSIVE” state

- The Communication Controller performs reception on the FlexRay™ bus
- The Communication Controller does not transmit any Frames or symbols on the FlexRay™ bus
- Clock synchronization is running
- The Host interface is operational

The Communication Controller exits from this state to

- “HALT” state by writing **SUCC1.CMD** = 0110_B (HALT command, at the end of the current cycle)
- “HALT” state by writing **SUCC1.CMD** = 0111_B (FREEZE command, immediately)
- “HALT” state due to change of the error state from “PASSIVE” to “COMM_HALT”
- “NORMAL_ACTIVE” state due to change of the error state from “PASSIVE” to “ACTIVE”. The transition takes place when **CCEV.PTAC** from the Communication Controller Error Vector register equals **SUCC1.PTA** - 1.
- “READY” state by writing **SUCC1.CMD** = 0010_B (READY command)

26.6.5.11 HALT State

In this state all communication (reception and transmission) is stopped.

The Communication Controller enters this state

- By writing **SUCC1.CMD** = 0110_B (HALT command) while the Communication Controller is in “NORMAL_ACTIVE” or “NORMAL_PASSIVE” state
- By writing **SUCC1.CMD** = 0111_B (FREEZE command) from all states
- When exiting from “NORMAL_ACTIVE” state because the clock correction failed counter reached the “maximum without clock correction fatal” limit
- When exiting from “NORMAL_PASSIVE” state because the clock correction failed counter reached the “maximum without clock correction fatal” limit

The Communication Controller exits from this state to “CONFIG” state

- By writing **SUCC1.CMD** = 0001_B (DEFAULT_CONFIG command)

When the Communication Controller enters “HALT” state, all configuration and status data is maintained for analyzing purposes.

When the Host writes **SUCC1.CMD** = 0110_B (HALT command) in the SUC Configuration Register 1 to 1, the Communication Controller sets bit **CCSV.HRQ** in the Communication Controller Status Vector register and enters “HALT” state after the current communication cycle has finished.

When the Host writes **SUCC1.CMD** = 0111_B (FREEZE command) in the SUC Configuration Register to 1, the Communication Controller enters “HALT” state immediately and sets the **CCSV.FSI** bit in the Communication Controller Status Vector register.

The POC state from which the transition to HALT state took place can be read from **CCSV.PSL**.

26.6.6 Network Management

The accrued Network Management (NM) vector is located in the Network Management Register 1 to Network Management Register 3 (**NMVx (x = 1-3)**). The Communication Controller performs a logical OR operation over all Network Management (NM) vectors out of all received valid Network Management (NM) Frames with the Payload Preamble Indicator (PPI) bit set. Only a static Frame may be configured to hold Network Management (NM) information. The Communication Controller updates the Network Management (NM) vector at the end of each cycle.

The length of the Network Management (NM) vector can be configured from 0 to 12 byte by NML in the NEM Configuration Register. The Network Management (NM) vector length must be configured identically in all nodes of a cluster.

To configure a transmit buffer to send FlexRay™ Frames with the PPI bit set, the PPIT bit in the Header Section of the respective transmit buffer has to be set via **WRHS1.PPIT**. In addition the Host has to write the Network Management (NM) information to the Data Section of the respective transmit buffer.

The evaluation of the Network Management (NM) vector has to be done by the application running on the Host.

*Note: In case a Message Buffer is configured for transmission / reception of Network Management Frames, the payload length configured in Header 2 of that Message Buffer should be equal or greater than the length of the NM Vector configured by **NEMC.NML**.*
When the Communication Controller transits to "HALT" state, the cycle count is not incremented and therefore the NM Vector is not updated. In this case NMV1 to NMV3 holds the value from the cycle before.

26.6.7 Filtering and Masking

Filtering is done by checking specific fields in a received Frame against the corresponding configuration constants of the valid Message Buffers and the actual slot and cycle counter values (acceptance filtering), or by comparing the configuration constants of the valid Message Buffers against the actual slot and cycle counter values (transmit filtering). A Message Buffer is only updated / transmitted if the required matches occur.

Filtering is done on the following fields:

- Channel ID
- Frame ID
- Cycle Counter

The following filter combinations for acceptance / transmit filtering are allowed:

- Frame ID + Channel ID
- Frame ID + Channel ID + Cycle Counter

In order to store a received message in a Message Buffer all configured filters must match.

Note: For the FIFO the acceptance filter is configured by the FIFO Rejection Filter and the FIFO Rejection Filter Mask.

A message will be transmitted in the time slot corresponding to the configured Frame ID on the configured channel(s). If cycle counter filtering is enabled the configured cycle filter value must also match.

26.6.7.1 Frame ID Filtering

Every transmit and receive buffer contains a Frame ID stored in the Header Section. This Frame ID is used differently for receive and transmit buffers.

Receive Buffers

A received message is stored in the first receive buffer where the received Frame ID matches the configured Frame ID, provided channel ID and cycle counter criteria are also met.

Transmit Buffers

For transmit buffers the configured Frame ID is used to determine the appropriate slot for message transmission. The Frame will be transmitted in the time slot corresponding to the configured Frame ID, provided channel ID and cycle counter criteria are also met.

26.6.7.2 Channel ID Filtering

There is a 2-bit channel filtering field (CHA, CHB) located in the Header Section of each Message Buffer in the Message RAM. It serves as a filter for receive buffers, and as a control field for transmit buffers (see **Table 26-13**).

Table 26-13 Channel Filtering Configuration

CHA	CHB	**Transmit Buffer** transmit Frame	**Receive Buffer** store valid receive Frame
1	1	on both channels (static segment only)	received on channel A or B (store first semantically valid Frame, static segment only)
1	0	on channel A	received on channel A
0	1	on channel B	received on channel B
0	0	no transmission	ignore Frame

Note: If a Message Buffer is configured for the dynamic segment and both bits of the channel filtering field are set to 1, no Frames are transmitted resp. received Frames are ignored (same function as CHA = CHB = 0)

Receive Buffers

Valid received Frames are stored if they are received on the channels specified in the channel filtering field. Only in static segment a receive buffer may be setup for reception on both channels (CHA and CHB set). Other filtering criteria must also be met.

If a valid Header Segment was stored, the respective MBC flag in the Message Buffer Status Changed register is set. If a valid Payload Segment was stored, the respective **NDn (n = 0-31)** to **NDn (n = 96-127)** flag in the New Data **NDAT1** to **NDAT4** register is set. In both cases, if bit **RDHS1.MBI** in the Header Section of the respective Message Buffer is set, the RXI flag in the Status Service Request Register is set to 1. If enabled an service request is generated.

Transmit Buffers

The content of the buffer is transmitted only on the channels specified in the channel filtering field when the Frame ID filtering and cycle counter filtering criteria are also met. Only in static segment a transmit buffer may be setup for transmission on both channels (CHA and CHB set). After transmission has completed, and if bit **WRHS1.MBI** in the Header Section of the respective Message Buffer is set, the TXI flag in the Status Service Request Register is set to 1. If enabled an service request is generated.

26.6.7.3 Cycle Counter Filtering

Cycle counter filtering is based on the notion of a cycle set. For filtering purposes, a match is detected if any one of the elements of the cycle set is matched. The cycle set is defined by the cycle code field in the Header Section of each Message Buffer.

If Message Buffer 0 is configured to hold the startup / SYNC Frame or the single slot Frame by bits TXST, TXSY, and TSM in the SUC Configuration Register 1, cycle counter filtering for Message Buffer 0 should be disabled.

*Note: Sharing of a static time slot via cycle counter filtering between different nodes of a FlexRay™ network is **not** allowed.*

The set of cycle numbers belonging to a cycle set is determined as described in **Table 26-14**.

Table 26-14 Definition of Cycle Set

Cycle Code	Matching Cycle Counter Values		
$000000x_B$	all Cycles		
$000001c_B$	every second Cycle	at (Cycle Count)mod2	= c
$00001cc_B$	every fourth Cycle	at (Cycle Count)mod4	= cc
$0001ccc_B$	every eighth Cycle	at (Cycle Count)mod8	= ccc
$001cccc_B$	every sixteenth Cycle	at (Cycle Count)mod16	= cccc
$01ccccc_B$	every thirty-second Cycle	at (Cycle Count)mod32	= ccccc
$1cccccc_B$	every sixty-fourth Cycle	at (Cycle Count)mod64	= cccccc

Table 26-15 below gives some examples for valid cycle sets to be used for cycle counter filtering:

Table 26-15 Examples for Valid Cycle Sets

Cycle Code	Matching Cycle Counter Values
0000011_B	1-3-5-7- ….-63 ↵
0000100_B	0-4-8-12- ….-60 ↵
0001110_B	6-14-22-30- ….-62 ↵
0011000_B	8-24-40-56 ↵
0100011_B	3-35 ↵
1001001_B	9 ↵

Receive Buffers

The received message is stored only if the received cycle counter matches an element of the receive buffer's cycle set. Channel ID and Frame ID criteria must also be met.

Transmit Buffers

The content of the buffer is transmitted on the configured channels when an element of the cycle set matches the current cycle counter value and the Frame ID matches the slot counter value.

26.6.7.4 FIFO Filtering

For FIFO filtering there is one rejection filter and one rejection filter mask available. The FIFO rejection filter consists of 20 bits for **Channel** (2 bits), **Frame ID** (11 bits), and **Cycle Code** (7 bits). Rejection filter and rejection filter mask can be configured in

DEFAIULT_CONGIF or “CONFIG” state only. The filter configuration in the Header Sections of Message Buffers belonging to the FIFO is ignored.

A valid received Frame is stored in the FIFO if channel ID, Frame ID, and cycle counter are not rejected by the configured rejection filter and rejection filter mask, and if there is no matching dedicated receive buffer.

26.6.8 Transmit Process

The transmit process is described in the following sections.

26.6.8.1 Static Segment

For the static segment, if there are several messages pending for transmission, the message with the Frame ID corresponding to the next sending slot is selected for transmission.

The Data Section of transmit buffers assigned to the static segment can be updated until the end of the preceding time slot. This means that a transfer from the Input Buffer has to be started by writing to the Input Buffer Command Request register latest at this time.

26.6.8.2 Dynamic Segment

In the dynamic segment, if several messages are pending, the message with the highest priority (lowest Frame ID) is selected next. Only Frame ID’s which are higher than the largest static Frame ID are allowed for the dynamic segment.

In the dynamic segment different slot counter sequences are possible (concurrent sending of different Frame ID’s on both channels). Therefore pending messages are selected according to their Frame ID and their channel configuration bit.

The Data Section of transmit buffers assigned to the dynamic segment can be updated until the end of the preceding slot. This means that a transfer from the Input Buffer has to be started by writing to the Input Buffer Command Request register latest at this time.

The start of latest transmit configured by SLT in the MHD Configuration Register 1 defines the maximum minislot value allowed before inhibiting new Frame transmission in the dynamic segment of the current cycle.

26.6.8.3 Transmit Buffers

A portion of the E-Ray Message Buffers can be configured as transmit buffers by programming bit CFG in the Header Section of the respective Message Buffer to 1. This can be done via the Write Header Section 1 register.

There exist the following possibilities to assign a transmit buffer to the Communication Controller channels:

- Static segment: channel A **or** channel B, channel A **and** channel B

- Dynamic segment: channel A **or** channel B

Message Buffer 0 is dedicated to hold the startup Frame, the SYNC Frame, or the designated single slot Frame as configured by TXST, TXSY, and TSM in the SUC Configuration Register 1. In this case it can be reconfigured in “DEFAULT_CONFIG” or “CONFIG” state only. This ensures that any node transmits at most one startup / SYNC Frame per communication cycle. Transmission of startup / SYNC Frames from other Message Buffers is not possible.

All other Message Buffers configured for transmission in static or dynamic segment are reconfigurable during runtime. Due to the organization of the Data Partition in the Message RAM (reference by data pointer), reconfiguration of the configured payload length and the data pointer in the Header Section of a Message Buffer may lead to erroneous configurations. If a Message Buffer is reconfigured during runtime it may happen that this Message Buffer is not send out in the respective communication cycle.

The Communication Controller does not have the capability to calculate the Header CRC. The Host is supposed to provide the Header CRCs for all transmit buffers. If Network Management is required the Host has to set the PPIT bit in the Header Section of the respective Message Buffer to 1 and write the Network Management information to the Data Section of the Message Buffer (see **Section 26.6.6**).

The payload length field configures the data payload length in 2-byte words. If the configured payload length of a static transmit buffer is shorter than the payload length configured for the static segment by SFDL in the Message Handler Configuration Register 1, the Communication Controller generates padding byte to ensure that Frames have proper physical length. The padding pattern is logical zero.

Each transmit buffer provides a transmission mode flag TXM that allows the Host to configure the transmission mode for the transmit buffer in the static segment. If this bit is set, the transmitter operates in the single-shot mode. If this bit is cleared, the transmitter operates in the continuous mode. In dynamic segment the transmitter always works in single-shot mode.

If a Message Buffer is configured in the continuous mode, the Communication Controller does not reset the transmission request flag TXR after successful transmission. In this case a Frame is sent out each time the Frame ID and cycle counter filter match. The TXR flag can be reset by the Host by writing the respective Message Buffer number to the Input Buffer Command Request register while bit **STXRH** in the Input Buffer Command Mask register is reset to 0.

If two or more transmit buffers are configured with the same Frame ID **and** cycle counter filter value, the transmit buffer with the lowest Message Buffer number will be transmitted in the respective slot.

26.6.8.4 Frame Transmission

To prepare a transmit buffer for transmission the following steps are required:

- Configure the Message Buffer as transmit buffer by writing bit CFG = 1 in the Write Header Section 1 register
- Write transmit message (Header and Data Section) to the Input Buffer.
- To transfer a transmit message from Input Buffer to the Message RAM proceed as described on **“Data Transfer from Input Buffer to Message RAM” on Page 26-233**.
- If configured in the Input Buffer Command Mask register the Transmission Request flag for the respective Message Buffer will be set as soon as the transfer has completed, and the Message Buffer is ready for transmission.
- Check whether the Message Buffer has been transmitted by checking the TXR bits (TXR = 0) in the Transmission Request 1,2 registers (single-shot mode only).

In single-shot mode the Communication Controller resets the TXR flag after transmission has been completed. Now the Host may update the transmit buffer with the next message. The Communication Controller does not transmit the message before the Host has indicated that the update is completed by setting the Transmission Request flag TXR again. The Host can check the actual state of the TXR flags of all Message Buffers by reading the Transmission Request registers. After successful transmission, if bit **WRHS1.MBI** in the Header Section of the respective Message Buffer is set, the transmit service request flag in the Status Service Request Register is set (TXI = 1). If enabled an service request is generated.

26.6.8.5 NULL Frame Transmission

If in static segment the Host does not set the transmission request flag before transmit time, and if there is no other transmit buffer with matching filter criteria (matching Frame ID and cycle counter filter), the Communication Controller transmits a NULL Frame with the NULL Frame indication bit reset to 0 and the payload data reset to zero.

In the following cases the Communication Controller transmits a NULL Frame with the NULL Frame indication bit reset to 0, and the rest of the Frame Header and the Frame length unchanged (payload data is reset to zero):

- All transmit buffers configured for the slot have cycle counter filters that do not match the current cycle
- There are matching Frame ID’s and cycle counter filters, but none of these transmit buffers has the transmission request flag TXR set

NULL Frames are not transmitted in the dynamic segment.

26.6.9 Receive Process

The receive process is described in the following sections.

26.6.9.1 Frame Reception

To prepare or change a Message Buffer for reception the following steps are required:

- Configure the Message Buffer as receive buffer by writing bit CFG = 0 in the Write Header Section 1 register
- Configure the receive buffer by writing the configuration data (Header Section) to the Input Buffer
- Transfer the configuration from Input Buffer to the Message RAM by writing the number of the target Message Buffer to the Input Buffer Command Request register.

Once these steps are performed, the Message Buffer functions as an active receive buffer and participates in the internal acceptance filtering process, which takes place every time the Communication Controller receives a message. The first matching receive buffer is updated from the received message. If the Message Buffer holds an unprocessed Data Section (ND = 1) it is overwritten with the new message and the MLST bit in the respective Message Buffer Status register is set.

If the payload length of a received Frame PLC is longer than the value programmed by PLC in the Header Section of the respective Message Buffer, the data field stored in the Message Buffer is truncated to that length.

If no Frame, a NULL Frame, or a corrupted Frame is received in a slot, the Data Section of the Message Buffer configured for this slot is not updated. In this case only the flags in the Message Buffer Status register are updated to signal the cause of the problem. In addition the respective MBC flag in the Message Buffer Status Changed 1,2,3,4 registers is set.

When the Data Section of a receive buffer has been updated from a received Frame, the respective New Data **NDn (n = 0-31)** to **NDn (n = 96-127)** flag in the New Data **NDAT1** to **NDAT4** registers is set. When the Message Handler has updated the Message Buffer status, the respective MBC flag in the Message Buffer Status Changed 1,2,3,4 registers is set. If bit **RDHS1.MBI** in the Header Section of the respective Message Buffer is set, the receive service request flag in the Status Service Request Register is set (RXI = 1). If enabled an service request is generated.

To read a receive buffer from the Message RAM via the Output Buffer proceed as described on **“Data Transfer from Message RAM to Output Buffer” on Page 26-235**.

Note: The ND and MBC flags are automatically cleared by the Message Handler when the received message has been transferred to the Output Buffer.

26.6.9.2 NULL Frame reception

The Payload Segment of a received NULL Frame is **not** copied into the matching receive buffer. If a NULL Frame has been received, the Header Section of the matching Message Buffer is updated from the received NULL Frame. The NULL Frame indication bit in the Header Section 3 of the respective Message Buffer is reset (NFI = 0) and the respective MBC flag in the Message Buffer Status Changed 1,2,3,4 registers is set.

In case that bit ND and / or MBC were already set before this event because the Host did not read the last received message, bit MLST in the Message Buffer Status register of the respective Message Buffer is also set.

26.6.10 FIFO Function

A group of the Message Buffers can be configured as a cyclic First-In-First-Out (FIFO). The group of Message Buffers belonging to the FIFO is contiguous in the register map starting with the Message Buffer referenced by FFB and ending with the Message Buffer referenced by LCB in the Message RAM Configuration register. Up to 128 Message Buffers can be assigned to the FIFO.

26.6.10.1 Description

Every valid incoming message not matching with any dedicated receive buffer but passing the programmable FIFO filter is stored into the FIFO. In this case Frame ID, payload length, receive cycle count, and the status bits of the addressed FIFO Message Buffer are overwritten with Frame ID, payload length, receive cycle count, and the status from the received message and can be read by the Host for message identification. Bit RFNE in the Status Service Request Register shows that the FIFO is not empty, bit RFF in the Status Service Request Register is set when the last available Message Buffer belonging to the FIFO is written, bit RFO in the Error Service Request Register shows that a FIFO overrun has been detected. If enabled, service requests are generated.

There are two index registers associated with the FIFO. The PUT Index Register (PIDX) is an index to the next available location in the FIFO. When a new message has been received it is written into the Message Buffer addressed by the PIDX register. The PIDX register is then incremented and addresses the next available Message Buffer. If the PIDX register is incremented past the highest numbered Message Buffer of the FIFO, the PIDX register is loaded with the number of the first (lowest numbered) Message Buffer in the FIFO chain. The GET Index Register (GIDX) is used to address the next Message Buffer of the FIFO to be read. The GIDX register is incremented after transfer of the contents of a Message Buffer belonging to the FIFO to the Output Buffer. The PUT Index Register and the GET Index Register are not accessible by the Host.

The FIFO is completely filled when the PUT index (PIDX) reaches the value of the GET index (GIDX). When the next message is written to the FIFO before the oldest message has been read, both PUT index and GET index are incremented and the new message

overwrites the oldest message in the FIFO. This will set FIFO overrun flag RFO in the Error Service Request Register.

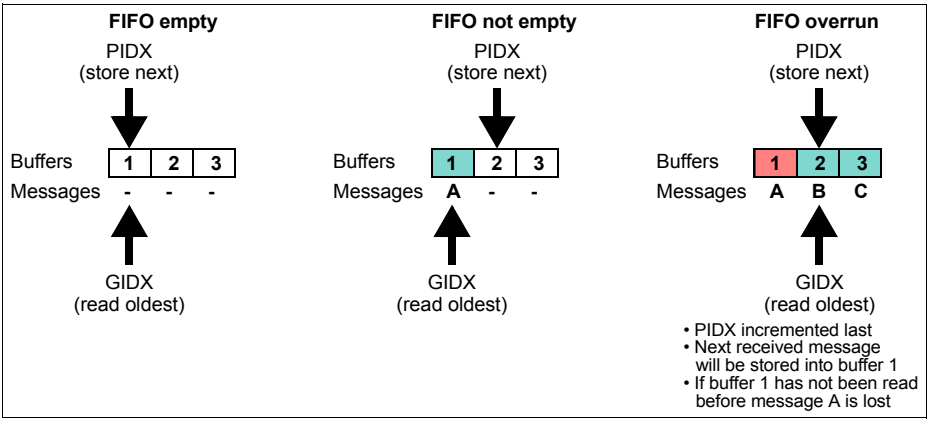


Figure 26-10 FIFO Status: Empty, Not Empty, Overrun

A FIFO non empty status is detected when the PUT index (PIDX) differs from the GET index (GIDX). In this case flag RFNE is set. This indicates that there is at least one received message in the FIFO. The FIFO empty, FIFO not empty, and the FIFO overrun states are explained in **Figure 26-10** for a three Message Buffer FIFO.

There is a programmable FIFO rejection filter for the FIFO. The FIFO Rejection Filter register (FRF) defines a filter pattern for messages to be rejected. The FIFO rejection filter consists of channel filter, Frame ID filter, and cycle counter filter. If bit RSS is set to 1 (default), all messages received in the static segment are rejected by the FIFO. If bit RNF is set to 1 (default), received NULL Frames are not stored in the FIFO.

The FIFO Rejection Filter Mask register (FRFM) specifies which bits of the Frame ID filter in the FIFO Rejection Filter register are marked “don’t care” for rejection filtering.

26.6.10.2 Configuration of the FIFO

For all Message Buffers belonging to the FIFO the data pointer to the first 32-bit word of the Data Section of the respective Message Buffer in the Message RAM has to be configured via the Write Header Section 3 register. All information required for acceptance filtering is taken from the FIFO rejection filter and the FIFO rejection filter mask and needs not be configured in the Header Sections of the Message Buffers belonging to the FIFO.

When programming the data pointers for the Message Buffers belonging to the FIFO, the payload length of all Message Buffers should be programmed to the same value.

*Note: It is recommended to program the MBI bits of the Message Buffers belonging to the FIFO to 0 via **WRHS1.MBI** to avoid generation of RX interrupts.*
*If the payload length of a received Frame is longer than the value programmed by **WRHS2.PLC** in the Header Section of the respective Message Buffer, the data field stored in a Message Buffer of the FIFO is truncated to that length.*

26.6.10.3 Access to the FIFO

To read from the FIFO the Host has to trigger a transfer from the Message RAM to the Output Buffer by writing the number of the first Message Buffer of the FIFO (referenced by FFB) to the Output Buffer Command Request register. The Message Handler then transfers the Message Buffer addressed by the GET Index Register (GIDX) to the Output Buffer. After this transfer the GET Index Register (GIDX) is incremented.

26.6.11 Message Handling

The Message Handler controls data transfers between the Input / Output Buffer and the Message RAM and between the Message RAM and the two Transient Buffer RAMs. All accesses to the internal RAM's are 32 bit accesses.

Access to the Message Buffers stored in the Message RAM is done under control of the Message Handler state machine. This avoids conflicts between accesses of the two protocol controllers and the Host to the Message RAM.

Frame IDs of Message Buffers assigned to the static segment have to be in the range from 1 to NSS as configured in the GTU Configuration Register 7. Frame IDs of Message Buffers assigned to the dynamic segment have to be in the range from NSS + 1 to 2047.

Received messages with no matching dedicated receive buffer (static or dynamic segment) are stored in the receive FIFO (if configured) if they pass the FIFO rejection filter.

26.6.11.1 Host access to Message RAM

The message transfer between Input Buffer and Message RAM as well as between Message RAM and Output Buffer is triggered by the Host by writing the number of the target / source Message Buffer to be accessed to the Input or Output Buffer Command Request register.

The Input / Output Buffer Command Mask registers can be used to write / read Header and Data Section of the selected Message Buffer separately. If bit **STXRS** in the Input Buffer Command Mask register is set (**STXRS** = 1), the transmission request flag TXR of the selected Message Buffer is automatically set after the Message Buffer has been updated.

If bit **STXRS** in the Input Buffer Command Mask register is reset (**STXRS** = 0), the transmission request flag TXR of the selected Message Buffer is reset. This can be used to stop transmission from Message Buffers operated in continuous mode.

Input Buffer (IBF) and the Output Buffer (OBF) are build up as a double buffer structure. One half of this double buffer structure is accessible by the Host (IBF Host / OBF Host), while the other half (IBF Shadow / OBF Shadow) is accessed by the Message Handler for data transfers between IBF / OBF and Message RAM.

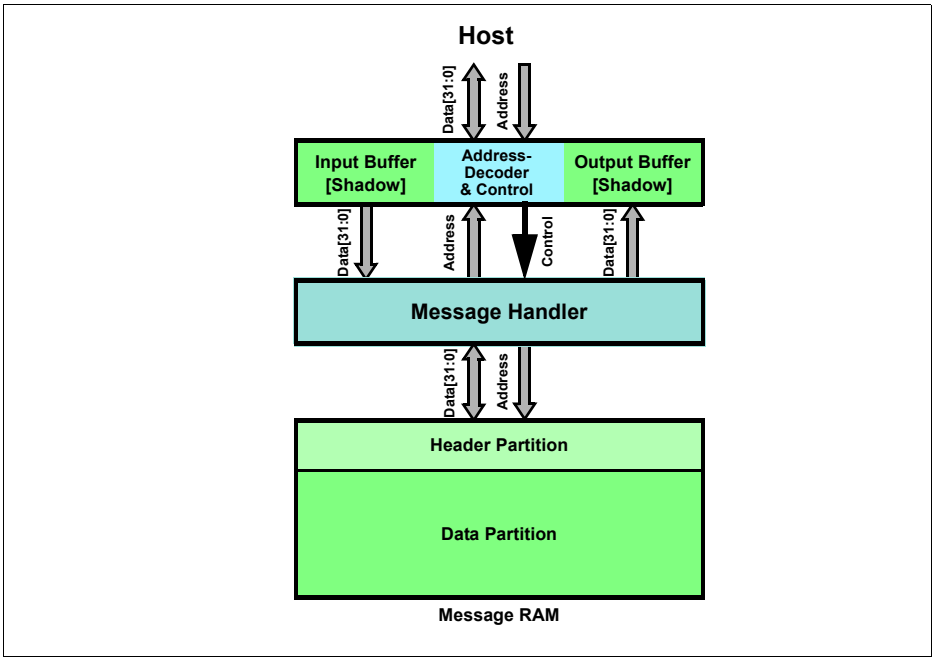


Figure 26-11 Host Access to Message RAM

Data Transfer from Input Buffer to Message RAM

To configure / update a Message Buffer in the Message RAM, the Host has to write the data to **WRDSnn (nn = 01-64)** and the Header to **WRHS1**, **WRHS2**, **WRHS3**. Two sets of **WRDSnn (nn = 01-64)** are available in parallel and selected by **CUST1.IBF1PAG**and **CUST1.IBF2PAG**. **CUST1.IBFS** shows which Input Buffer is currently used as Input Shadow Buffer and which as Input Host Buffer. **WRHS1**, **WRHS2**, and **WRHS2** does only exist once. The specific action is selected by configuring the Input Buffer Command Mask **IBCM**.

When the Host writes the number of the target Message Buffer in the Message RAM to IBRH in the Input Buffer Command Request register **IBCR**, IBF Host and IBF Shadow are swapped (see **Figure 26-12**).

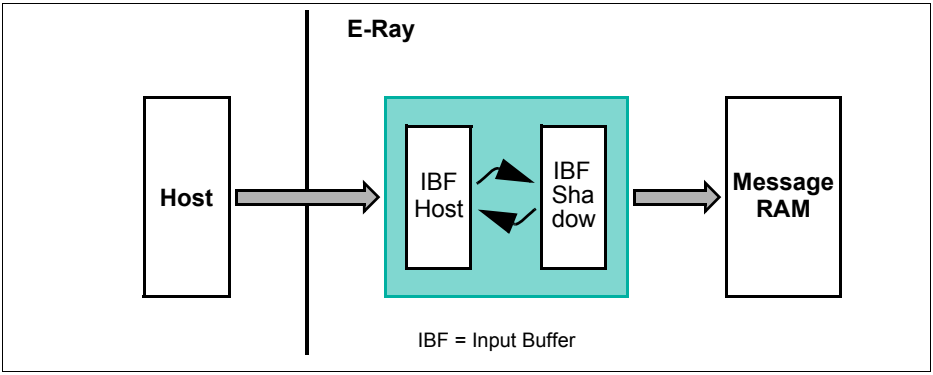


Figure 26-12 Double Buffer Structure Input Buffer

In addition the bits in the Input Buffer Command Mask and Input Buffer Command Request registers are also swapped to keep them attached to the respective IBF section (see **Figure 26-13**).

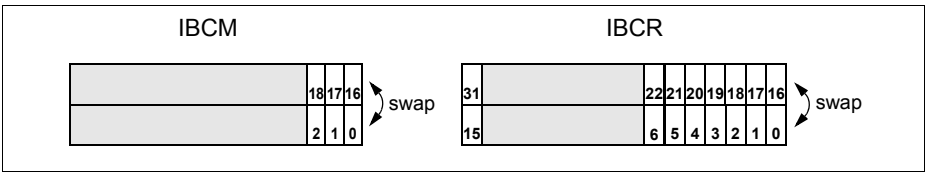


Figure 26-13 Swapping of IBCM and IBCR Bit

With this write operation the IBSYS bit in the Input Buffer Command Request register is set to 1. The Message Handler then starts to transfer the contents of IBF Shadow to the Message Buffer in the Message RAM selected by IBRS.

While the Message Handler transfers the data from IBF Shadow to the target Message Buffer in the Message RAM, the Host may write the next message to IBF Host. After the transfer between IBF Shadow and the Message RAM has completed, the IBSYS bit is set back to 0 and the next transfer to the Message RAM may be started by the Host by writing the respective target Message Buffer number to IBRH in the Input Buffer Command Request register.

If a write access to IBRH occurs while IBSYS is 1, IBSYH is set to 1. After completion of the ongoing data transfer from IBF Shadow to the Message RAM, IBF Host and IBF Shadow are swapped, IBSYH is reset to 0, IBSYS remains set to 1, and the next transfer

to the Message RAM is started. In addition the Message Buffer numbers stored under IBRH and IBRS and the Command Mask flags are also swapped.

Table 26-16 Assignment of Input Buffer Command Mask Bit

Pos.	Access	Bit	Function
18	rh	**STXRS**	Set Transmission Request Shadow
17	rh	**LDSS**	Load Data Section Shadow
16	rh	**LHSS**	Load Header Section Shadow
2	rw	**STXRH**	Set Transmission Request Host
1	rw	**LDSH**	Load Data Section Host
0	rw	**LHSH**	Load Header Section Host

Table 26-17 Assignment of Input Buffer Command Request Bit

Pos.	Access	Bit	Function
31	rh	IBSYS	**IBF Busy Shadow,** signals ongoing transfer from IBF Shadow to Message RAM
21–16	rh	IBRS	**IBF Request Shadow,** number of Message Buffer currently / last updated
15	rh	IBSYH	**IBF Busy Host,** transfer request pending for Message Buffer referenced by IBRH
5-0	rwh	IBRH	**IBF Request Host,** number of Message Buffer to be updated next

Data Transfer from Message RAM to Output Buffer

To read a Message Buffer from the Message RAM, the Host has to write to Command Request register **OBCR** to trigger the data transfer as configured in Output Buffer Command Mask **OBCM** register. After the transfer has completed, the Host can read the transferred data from **RDDSnn (nn = 01-64)**, **RDHS1**, **RDHS2**, **RDHS2**, and **MBS**.

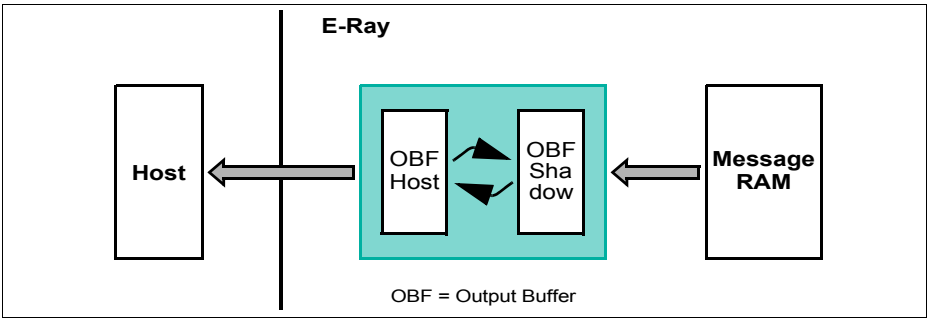


Figure 26-14 Double Buffer Structure Output Buffer

OBF Host and OBF Shadow as well as bits **OBCM.RHSS**, **OBCM.RDSS**, **OBCM.RHSH**, **OBCM.RDSH** and bits **OBCR.OBRS**, **OBCR.OBRH** are swapped under control of bits **OBCR.VIEW** and **OBCR.REQ**.

Writing bit **OBCR.REQ** to 1 copies bits **OBCM.RHSS**, **OBCM.RDSS** and bits **OBCR.OBRS** to an internal storage (see **Figure 26-15**).

After setting **OBCR.REQ** to 1, **OBCR.OBSYS** is set to 1, and the transfer of the Message Buffer selected by **OBCR.OBRS** from the Message RAM to OBF Shadow is started. After the transfer between the Message RAM and OBF Shadow has completed, the **OBCR.OBSYS** bit is set back to 0. Bits **OBCR.REQ** and **OBCR.VIEW** can only be set to 1 while **OBCR.OBSYS** is 0.

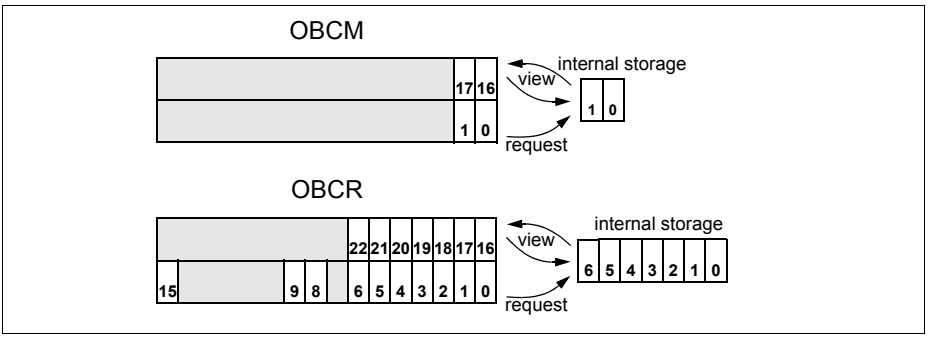


Figure 26-15 Swapping of OBCM and OBCR Bit

OBF Host and OBF Shadow are swapped by setting bit **OBCR.VIEW** to 1 while bit **OBCR.OBSYS** is 0 (see **Figure 26-14**).

In addition bits **OBCR.OBRH** and bits **OBCM.RHSH**, **OBCM.RDSH** are swapped with the registers internal storage thus assuring that the Message Buffer number stored in

OBCR.OBRH and the mask configuration stored in **OBCM.RHSH**, **OBCM.RDSH** matches the transferred data stored in OBF Host (see **Figure 26-15**).

Now the Host can read the transferred Message Buffer from OBF Host while the Message Handler may transfer the next message from the Message RAM to OBF Shadow.

Table 26-18 Assignment of Output Buffer Command Mask Bit

Pos.	Access	Bit	Function
17	rh	RDSH	Data Section available for Host access
16	rh	RHSH	Header Section available for Host access
1	rw	RDSS	Read Data Section Shadow
0	rw	RHSS	Read Header Section Shadow

Table 26-19 Assignment of Output Buffer Command Request Bit

Pos.	Access	Bit	Function
22–16	rh	OBRH	**OBF Request Host,** number of Message Buffer available for Host access
15	rh	OBSYS	**OBF Busy Shadow,** signals ongoing transfer from Message RAM to OBF Shadow
9	rw	REQ	**Request Transfer from Message RAM to OBF Shadow**
8	rwh	VIEW	**View OBF Shadow, swap OBF Shadow, and OBF Host**
6–0	rwh	OBRS	**OBF Request Shadow,** number of Message Buffer for next request

26.6.11.2 Data Transfers between IBF / OBF and Message RAM

This document uses the following terms and abbreviations:

Table 26-20 Terms and Abbreviations

Term	Meaning
MHD	Message Handler
IBF	Input Buffer 1 or 2 RAM
OBF	Output Buffer 1 or 2 RAM
MBF	Message Buffer RAM
TBF	Transient Buffer RAM Channel A (TBF1) or Channel B (TBF2)

Table 26-20 Terms and Abbreviations (cont'd)

IBF ⇒ MBF	Transfer from IBF to MBF
MBF ⇒ OBF	Transfer from MBF to OBF
MBF ⇒ TBF	Transfer from MBF to TBF
TBF ⇒ MBF	Transfer from TBF to MBF
SS	Slot Status
SS ⇒ MBF	Transfer SS to MBF

Message Handler functionality

The MHD controls the access to the MBF. It manages data-transfer between MBF and IBF, OBF, TBF1, TBF2. The data-path are shown in Figure 26-16.

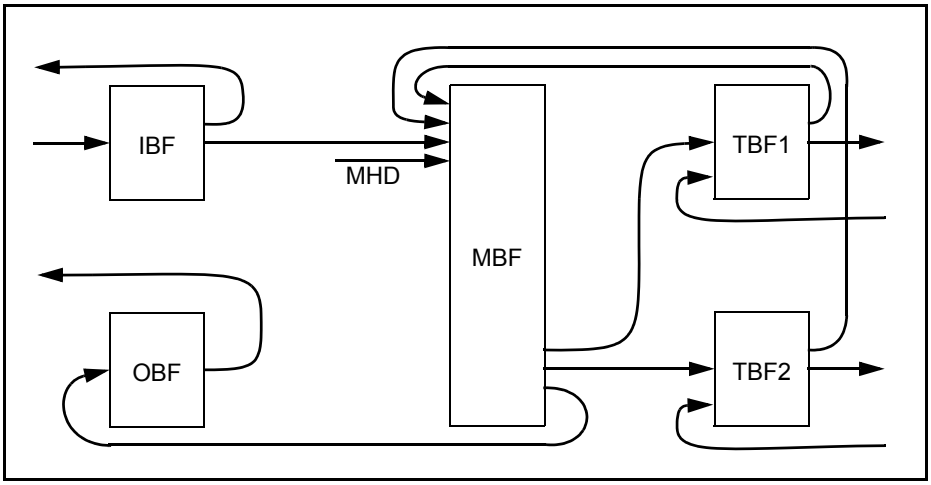


Figure 26-16 Interconnection of RAMs

Furthermore a search-algorithm allows to find the next valid message object in the MBF for transmission or reception.

Each transfer consists of a setup-time, four time steps to transfer the Header-section and a payload-length-dependent number of time steps to transfer the data-section. The internal data-busses have a width of 32 bits. Thereby it is possible to transfer two 2-byte words in one time step. If the payload consists of an odd number of 2-byte words the last time step of the data-section contains only 16 bit of valid data. If the Payload-Length (PL) is e.g. 7, the data-section consists of 4 time steps.

The maximum length for the data-section is 64 time steps, the minimum length is zero time steps.

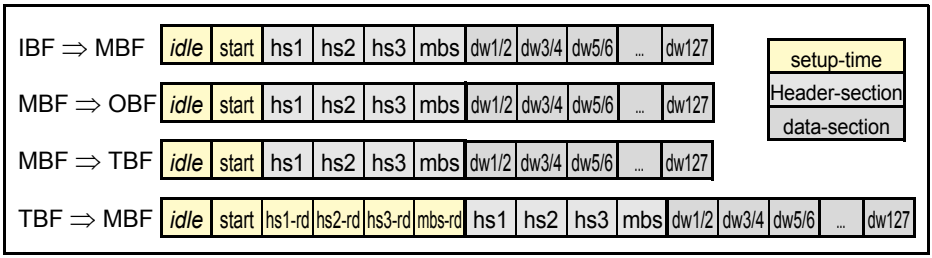


Figure 26-17 Different Possible Buffer Transfers

The update of the Slot-Status consists of a setup-time and one time-step to write the new Slot-Status.

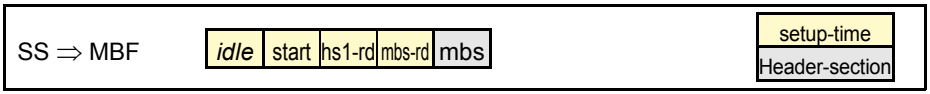


Figure 26-18 Update of Slot Status

The length of a time step depends on the number of concurrent tasks.

The following concurrent tasks are executed under control of the Message Handler:

- Data transfer between IBF or OBF and MBF
- Data transfer between TBF1 and MBF, search next TX / RX Message Buffer CHA
- Data transfer between TBF2 and MBF, search next TX / RX Message Buffer CHB

Thereby the time step length can vary between one and three f_{CLC_ERAY} periods.

Under certain conditions it is possible that a transfer is stopped or interrupted for a number of time steps until it is continued.

When a IB F⇒ MBF is started short after a TBF ⇒ MBF or SS ⇒ MBF the transfer from IBF has to wait until the setup-time of the internal transfer has finished (see Figure 26-19)

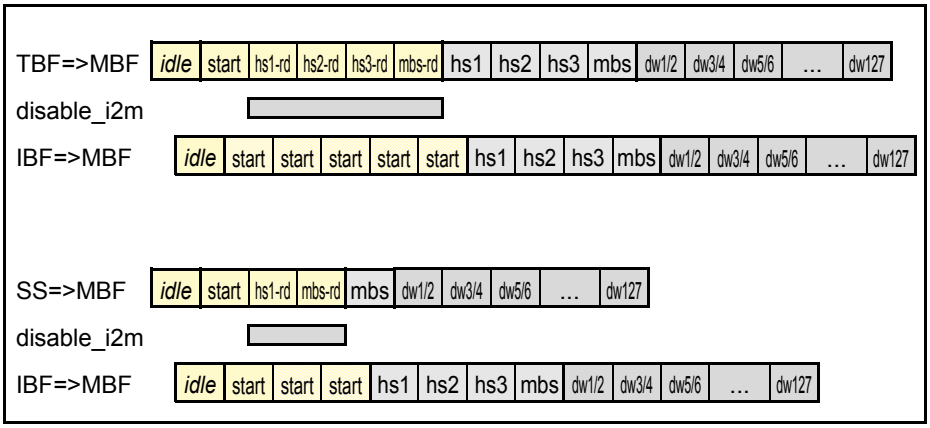


Figure 26-19 Delay start of IBF⇒MBF

The internal signal “disable_i2m” is always active when the TBF ⇒ MBF is in state “hs1-rd”, “hs2-rd”, “hs3-rd” or “mbs-rd” and when the SS ⇒ MBF is in state “hs1-rd” or “mbs-rd”.

The IBF ⇒ MBF is hold in state “start” until the internal signal “disable_i2m” gets inactive.

These additional time-steps are independent of any address-counter-values. This means, the IBF ⇒ MBF has to wait even if it writes to another buffer than the internal transfer.

Multiple requests of transfers between IBF/OBF and Message RAM

The time required to transfer the contents of a Message Buffer between IBF / OBF and Message RAM depends on the number of 4-byte words to be transferred, the number of concurrent tasks to be managed by the Message Handler, and in special cases the type and address range of the internal transfer. The number of 4-byte words varies from 4 (Header Section only) to 68 (Header + maximum Data Section) plus a short setup time to start the first transfer, while the number of concurrent task varies from one to three. The 4 Header words have to be included in calculation even if only the Data Section is requested for transfer.

The following concurrent tasks are executed under control of the Message Handler:

- Data transfer between IBF or OBF and MBF
- Data transfer between TBF1 and MBF, search next TX / RX Message Buffer CHA
- Data transfer between TBF2 and MBF, search next TX / RX Message Buffer CHB

Transfers between IBF and MBF respectively MBF and OBF can only be handled one after another. In case that e.g. a IBF ⇒ MBF has been started shortly before a

MBF ⇒ OBF is requested, the MBF ⇒ OBF has to wait until the IBF ⇒ MBF has completed.

In case that e.g. a second IBF⇒MBF is requested, a MBF⇒OBF is requested and a IBF⇒MBF is ongoing, the MBF⇒OBF has to wait until the first IBF⇒IBF has completed. The second IBF=MBF has to wait until the MBF⇒OBF has completed (see figure 26-20) independent whether MBF⇒OBF or second IBF⇒MBF is requested first.

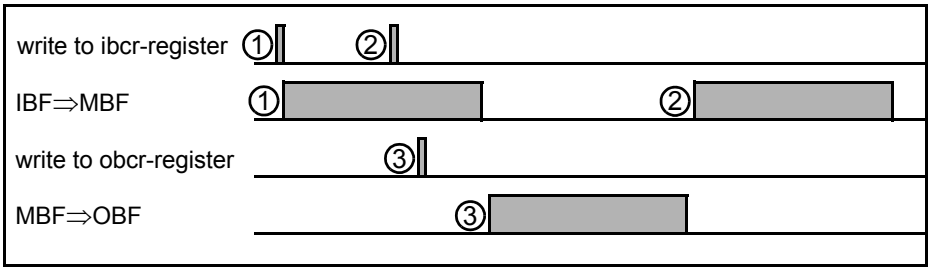


Figure 26-20 Multiple IBF/OBF Request

Worst case for single request

When a message with a large payload length is received the TBF⇒MBF is started at the begin of the next slot (n+1). If the next slot is a dynamic slot without transmission/reception (minislot), it may happen that the TBF⇒MBF has not finished until begin of the next but one slot (n+2). In this case the TBF⇒MBF will be service requested (break) to start a transmission in the next but one slot (MBF⇒TBF) and/or to update the slot status (SS⇒MBF) for the RX-buffer corresponding with next slot (n+1). After this interruption the TBF⇒MBF is continued.

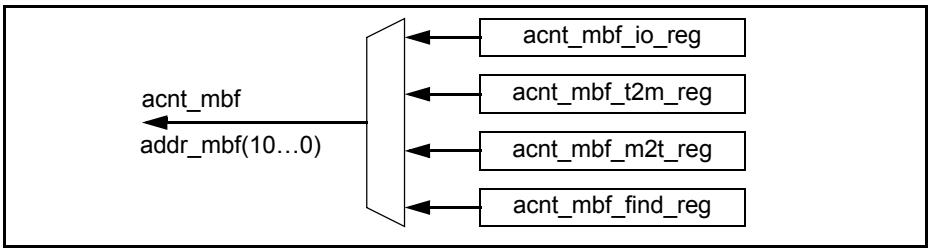


Figure 26-21 Address Counter Scheme of Message RAM (simplified)

For the transfers IBF⇒MBF / MBF⇒OBF, TBF⇒MBF and MBF⇒TBF separate address-counter are implemented (see Figure 26-21).

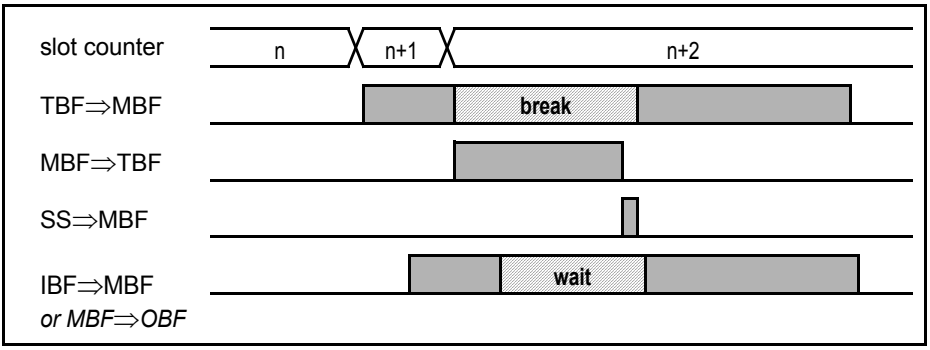


Figure 26-22 interruption of TBF⇒MBF

If the address-counter for IBF⇒MBF / MBF⇒OBF (acnt_mbf_io_reg) reaches the address of the interrupted TBF=>MBF (acnt_mbf_t2m_reg) the IBF⇒MBF / MBF⇒OBF has to wait until the TBF⇒MBF is continued (see Figure 26-22).

The relative time is measured in f_{CLC_ERAY} cycles. Absolute time depends on the actual f_{CLC_ERAY} cycle period.

tbf_to_mbf_break time$_{max}$ = (setup time + mbf_to_tbf time$_{max}$) + (setup time + ss_to_mbf)

cycles$_{req}$ = (number of concurrent tasks) × ((setup time+ (number of 4-byte words)$_{req}$) + tbf_to_mbf_break time)

setup time = 2 f_{CLC_ERAY} cycles

Worst case for one IBF⇒MBF or MBF⇒OBF:

Max. break time: tbf_to_mbf_break time$_{max}$ = (2+68) + (4+1) = 75

Max. number of f_{CLC_ERAY} cycles: cycles$_{req}$ = 3 × (6 + 68 + 75) = 435

Worst case for multiple transfers

If a second IBF⇒MBF and a MBF⇒OBF (see Figure 26-20) is requested directly after the first IBF⇒MBF has started following worst case timing could appear:

cycles$_{trans}$ = (remaining cycles of transfer running)
+ (cycles of second requested transfer)
+ (cycles of third requested transfer)

cycles$_{trans}$ = cycles$_{rem}$ + cycles$_{req_2}$+ cycles$_{req_3}$

Max. number of f_{CLC_ERAY} cycles: cycles$_{trans}$ = 447 + 435 + 447 = 1329

26.6.11.3 Minimum f_{CLC_ERAY}

To calculate the minimum f_{CLC_ERAY} the worst case scenario has to be considered.

The worst case scenario depends on the following parameters

- maximum payload length
- minimum minislot length
- number of configured Message Buffers (excluding FIFO)
- used channels (single/dual channel)

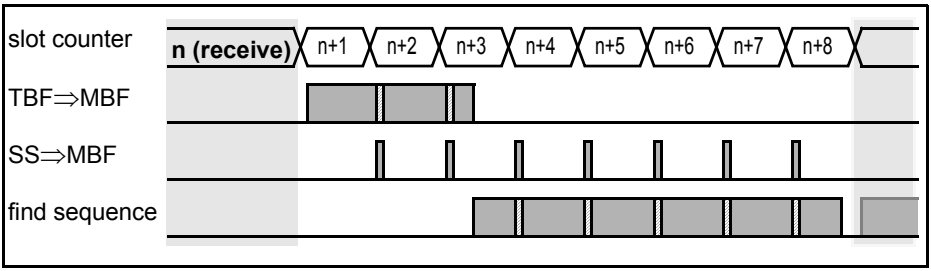


Figure 26-23 worst case scenario

Worst case scenario:

- reception of message with a maximum payload length in Slot n (n is 7,15,23,31,39,…)
- slot n+1 to n+7 are empty dynamic slots (minislot) and configured as receive buffer
- the find-sequence (usually started in slot 8,16,24,32,40,…) has to scan the maximum number of configured buffers
- the number of concurrent tasks has its maximum value of three

The find-sequence is executed each 8 Slots (slot 8,16,24,32,40,…). It has to be finished until the next find-sequence is requested.

The length of a TBF⇒MBF varies from 4 (Header Section only) to 68 (Header + maximum Data Section) time step plus a setup time of 6 time steps.

$$cycles_{t2m} = \frac{f_{CLC\_ERAY}}{\text{number of concurrent tasks}) \times (\text{setup time}_{t2m} + (\text{number of 4-byte words})_{t2m})}$$

A SS⇒MBF has a fixed length of 1 time steps plus a setup time of 4 time steps.

$$cycles_{ss2m} = \frac{f_{CLC\_ERAY}}{(\text{number of concurrent tasks}) \times 5}$$

The find sequence has a maximum length of 128 (maximum number of buffers) time steps plus a setup time of 2 time steps.

$$cycles_{find} = \frac{f_{CLC\_ERAY}}{(\text{number of concurrent tasks}) \times (\text{setup time}_{find} + (\text{number of configured buffers}))}$$

A minislot has a length of 2 to 63 Macrotick (gdMinislot). The minimum nominal Macrotick period (cdMinMTNom) is 1 µs. A sequence of 8 minislots has a length of

$$time_{8minislots} = 8 \times gdMinislot \times cdMinMTNom$$

The maximum period $T_{CLC\_ERAY} = 1/f_{CLC\_ERAY}$ can be calculated as followed:

$$time_{8minislots} \geq (f_{CLC\_ERAY}\ \text{period in}\ \mu s) \times (\ (f_{CLC\_ERAY}\ cycles_{t2m}) + 7 \times (f_{CLC\_ERAY}\ cycles_{ss2m}) + (f_{CLC\_ERAY}\ cycles_{find}))$$

$$f_{CLC\_ERAY}\ \text{period in ms} \leq \frac{time_{8mnislots}}{(\ cycles_{t2m}) + 7 \times (cycles_{ss2m}) + (cycles_{find})}$$

minimum $time_{8minislots}$ = $8 \times 2 \times 1\ \mu s = 16\ \mu s$

maximum $f_{CLC\_ERAY}\ cycles_{t2m}$ = $3 \times (6 + 68) = 222$

maximum $f_{CLC\_ERAY}\ cycles_{ss2m}$ = $3 * 5 = 15$

maximum $f_{CLC\_ERAY}\ cycles_{find}$ = $3 * (2 + 128) = 390$

$$f_{CLC\_ERAY}\ \text{period in ms} \leq \frac{16\mu s}{222 + 7 \times 15 + 390} = 22.315\ldots ns$$

The minimum f_{CLC_ERAY} frequency for this worst case scenario is 44.8125 MHz.

A too low f_{CLC_ERAY} frequency can cause a malfunction of the E-Ray.

The E-Ray can detect several malfunctions and reports this by setting the corresponding flag in the Message Handler Constraints Flags (**MHDF**) register.

Minimum f_{CLC_ERAY} for various maximum payload length

Table 26-21 summarizes the minimum required f_{CLC_ERAY} frequency for various maximum payload length assuming:

- a minimum minislot length of 2µs.
- a maximum of 128 configured Message Buffers.
- dual channels in use.

Table 26-21 Minimum f_{CLC_ERAY} for different maximum payload length

Maximum payload length of 32 bit words	4	8	16	32	64
minimum f_{CLC_ERAY}	32,82 MHz	33,57 MHz	35,07 MHz	38,07 MHz	44,82 MHz

Minimum f_{CLC_ERAY} for various minimum minislot length

Table 26-22 summarizes the minimum required f_{CLC_ERAY} frequency for various minimum minislot length assuming:

- a maximum payload length of 254 bytes / 64 four-byte-words.
- a maximum 128 configured Message Buffers.
- dual channels in use.

Table 26-22 Minimum f_{CLC_ERAY} for different minimum minislot length

gdMinislot at dMinMTNom = 1 µs	2 µs	3 µs	4 µs	7 µs	8 µs
minimum f_{CLC_ERAY}	44,82 MHz	29,88 MHz	22,412 MHz	12,8 MHz	9,96 MHz

Minimum f_{CLC_ERAY} for various amount of configured Message Buffers

Table 26-23 summarizes the minimum required f_{CLC_ERAY} frequency for various amount of configured Message Buffers assuming:

- a maximum payload length of 254 bytes / 64 four-byte-words.
- a minimum minislot length of 2 µs.
- dual channels in use.

Table 26-23 Minimum f_{CLC_ERAY} for different amount of configured Message Buffers

Configured maximum amount of Message Buffers	128	64	32
minimum f_{CLC_ERAY}	44,82 MHz	32,82 MHz	26,82 MHz

Minimum f_{CLC_ERAY} for a typical configuration

´The minimum required f_{CLC_ERAY} frequency for various assuming the following typical E-Ray configuration:

- a maximum payload length of 32 bytes / 8 four-byte-words.
- a minimum minislot length of 7 µs.
- a maximum 128 configured Message Buffers.
- dual channels in use

The minimum f_{CLC_ERAY} frequency for this typical example would be 10 MHz.

26.6.11.4 FlexRay™ Protocol Controller access to Message RAM

The two Transient Buffer RAMs (TBF 1, TBF 2) are used to buffer the data for transfer between the two FlexRay™ Protocol Controllers and the Message RAM.

Each Transient Buffer RAM is build up as a double buffer, able to store two complete FlexRay™ messages. There is always one buffer assigned to the corresponding Protocol Controller while the other one is accessible by the Message Handler.

If e.g. the Message Handler writes the next message to be send to Transient Buffer Tx, the FlexRay™ Channel Protocol Controller can access Transient Buffer Rx to store the message it is actually receiving. During transmission of the message stored in Transient Buffer Tx, the Message Handler transfers the last received message stored in Transient Buffer Rx to the Message RAM (if it passes acceptance filtering) and updates the respective Message Buffer.

Data transfers between the Transient Buffer RAMs and the shift registers of the FlexRay™ Channel Protocol Controllers are done in words of 32 bit. This enables the use of a 32 bit shift register independent of the length of the FlexRay™ messages.

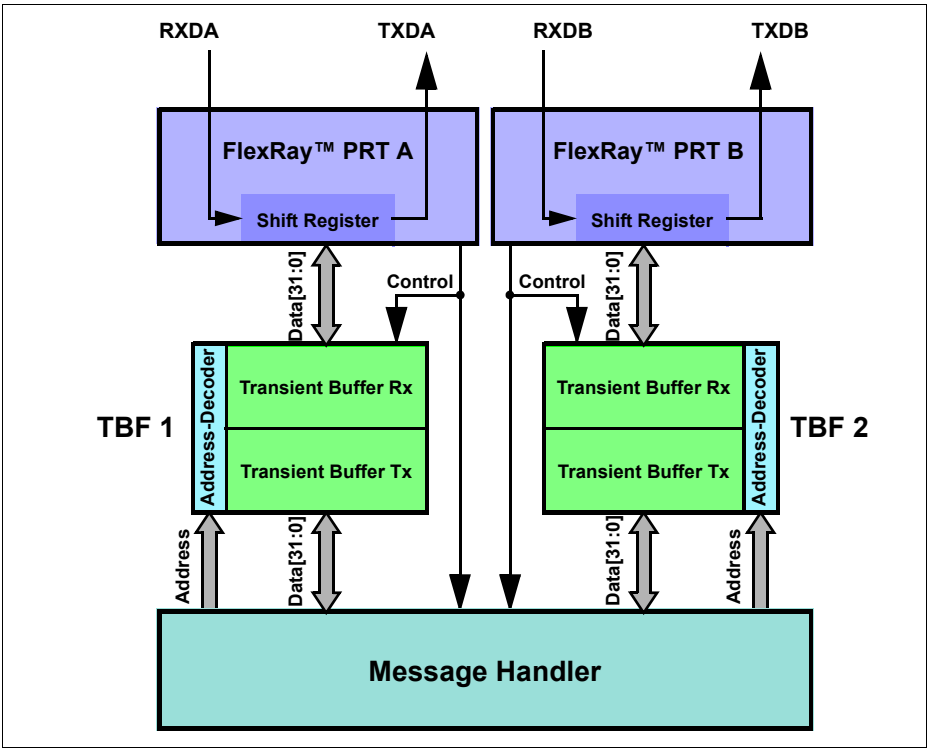


Figure 26-24 Access to Transient Buffer RAMs

26.6.12 Message RAM

To avoid conflicts between Host access to the Message RAM and FlexRay™ message reception / transmission, the Host cannot directly access the Message Buffers in the Message RAM. These accesses are handled via the Input and Output Buffers. The Message RAM is able to store up to 128 Message Buffers depending on the configured payload length.

The Message RAM is organized 2048 x 32. To achieve the required flexibility with respect to different numbers of data byte per FlexRay™ Frame (0 to 254), the Message RAM has a structure as shown in **Figure 26-25**.

The Data Partition is allowed to start at Message RAM word number: (MRC.LCB + 1) • 4

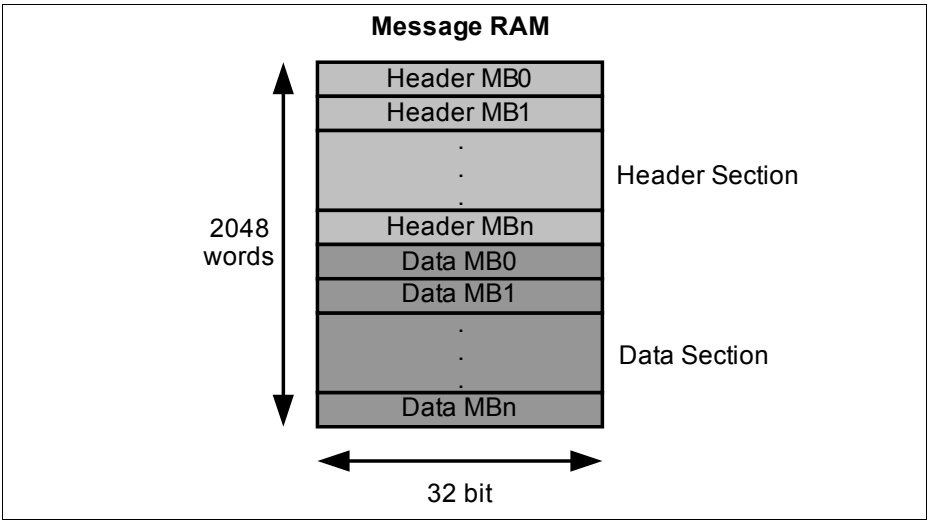


Figure 26-25 Structure of Message RAM

Header Partition

Stores Header Segments of FlexRay™ Frames:

- Supports a maximum of 128 Message Buffers
- Each Message Buffer has a Header of four 32 bit words
- Header 3 of each Message Buffer holds the11 bit pointer to the respective Data Section in the Data Partition

Data Partition

Flexible storage of Data Sections with different length. Some maximum values are:

- 30 Message Buffers with 254 byte Data Section each
- Or 56 Message Buffers with 128 byte Data Section each
- Or 128 Message Buffers with 48 byte Data Section each

Restriction: Header Partition + Data Partition may not occupy more than 2048 32-bit words.

26.6.12.1 Header Partition

The Header of each Message Buffer occupies four 32-bit words in the Header Partition of the Message RAM. The Header of Message Buffer 0 starts with the first word in the Message RAM.

For transmit buffers the Header CRC has to be calculated by the Host.

Payload Length Received **PLR**, Receive Cycle Count **RCC**, Received on Channel Indication **RCI**, Startup Frame Indication bit **SFI**, Sync bit **SYN**, NULL Frame Indication bit **NFI**, Payload Preamble Indication bit **PPI**, and Reserved bit **RES** are only updated from received valid Frames (including valid NULL Frames).

Header word 4 of each configured Message Buffer holds the respective Message Buffer Status **MBS** information.

Table 26-24 Header Section of a Message Buffer in the Message RAM

Bit Word	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1			MBI	TXM	NME	CFG	CHB	CHA		Cycle Code												Frame ID										
2		Payload Length Received								Payload Length Configured												Tx Buffer: Header CRC Configured Rx Buffer: Header CRC Received										
3			RES	PPI	NFI	SYN	SFI	RCI		Receive Cycle Count												Data Pointer										
4			RESS	PPIS	NFIS	SYNS	SFIS	RCIS		Cycle Count Status							TFB	FTY		MLST	ESB	ESA	TCIB	TCIA	SVOB	SVOA	CEOB	CEOA	SEOB	SEOA	VFRB	VFRA

- Frame Configuration
- Filter Configuration
- Message Buffer Control
- Message RAM Configuration
- Updated from received Frame
- Message Buffer Status
- unused

Header 1 (word 0)

Write access via **WRHS1**, read access via **RDHS1**:

- Frame ID: Slot counter filtering configuration
- Cycle Code: Cycle counter filtering configuration
- CHA, CHB: Channel filtering configuration
- CFG: Message Buffer configuration: receive / transmit
- PPIT: Payload Preamble Indicator Transmit
- XMI: Transmit mode configuration: single-shot / continuous
- MBI: Message Buffer receive / transmit service request enable

Header 2 (word 1)

Write access via **WRHS2**, read access via **RDHS2**:

- Header CRC
  - Transmit Buffer: Configured by the Host (calculated from Frame Header Segment)
  - Receive Buffer: Updated from received Frame
- Payload Length Configured
  - Length of Data Section (2-byte words) as configured by the Host
- Payload Length Received
  - Length of Payload Segment (2-byte words) stored from received Frame

Header 3

Write access via **WRHS3**, read access via **RDHS3**:

- Data Pointer
  - Pointer to the beginning of the corresponding Data Section in the Data Partition

Read access via **RDHS3**, valid for receive buffers only, updated from received Frames:

- Receive Cycle Count: Cycle count from received Frame
- RCI: Received on Channel Indicator
- SFI: Startup Frame Indicator
- SYN: SYNC Frame Indicator
- NFI: NULL Frame Indicator
- PPI: Payload Preamble Indicator
- RES: Reserved bit

Message Buffer Status MBS (word 3)

Read access via MBS, updated by the Communication Controller at the end of the configured slot.

- VFRA: Valid Frame Received on channel A
- VFRB: Valid Frame Received on channel B
- SEOA: Syntax Error Observed on channel A
- SEOB: Syntax Error Observed on channel B
- CEOA: Content Error Observed on channel A
- CEOB: Content Error Observed on channel B
- SVOA: Slot boundary Violation Observed on channel A
- SVOB: Slot boundary Violation Observed on channel B
- TCIA: Transmission Conflict Indication channel A
- TCIB: Transmission Conflict Indication channel B
- ESA: Empty Slot Channel A
- ESB: Empty Slot Channel B
- MLST: Message LoST
- FTA: Frame Transmitted on Channel A
- FTA: Frame Transmitted on Channel B
- Cycle Count Status: Actual cycle count when status was updated
- RCIS: Received on CHannel Indicator Status
- SFIS: Startup Frame Indicator Status
- SYNS: SYNC Frame Indicator Status
- NFIS: NULL Frame Indicator Status
- PPIS: Payload Preamble Indicator Status
- RESS: Reserved Bit Status

26.6.12.2 Data Partition

The Data Partition of the Message RAM stores the Data Sections of the Message Buffers configured for reception / transmission as defined in the Header Partition. The number of data bytes for each Message Buffer can vary from 0 to 254. To optimize the data transfer between the shift registers of the two FlexRay™ Protocol Controllers and the Message RAM as well as between the Host interface and the Message RAM, the physical width of the Message RAM is set to 4 bytes.

The Data Partition starts after the last word of the Header Partition. When configuring the Message Buffers in the Message RAM the programmer has to assure that the data pointers point to addresses within the Data Partition. **Table 26-25** below shows an example how the Data Sections of the configured Message Buffers can be stored in the Data Partition of the Message RAM.

The beginning and the end of a Message Buffer's Data Section is determined by the data pointer and the payload length configured in the Message Buffer's Header Section,

respectively. This enables a flexible usage of the available RAM space for storage of Message Buffers with different data length.

If the size of the Data Section is an odd number of 2-byte words, the remaining 16 bits in the last 32-bit word are unused (see **Table 26-25** below)

Table 26-25 Example for Structure of the Data Section in the Message RAM

Bit Word	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
…	unused								unused								unused								unused							
…	unused								unused								unused								unused							
…	**MB1** Data3								**MB1** Data2								**MB1** Data1								**MB1** Data0							
…	…								…								…								…							
…	…								…								…								…							
…	**MB1** Data(n)								**MB1** Data(n-1)								**MB1** Data(n-2)								**MB1** Data(n-3)							
…	…								…								…								…							
…	…								…								…								…							
…	…								…								…								…							
…	**MB1** Data3								**MB1** Data2								**MB1** Data1								**MB1** Data0							
…	…								…								…								…							
…	**MB1** Data(k)0								**MB1** Data(k-1)0								**MB1** Data(k-2)0								**MB1** Data(k-3)0							
2046	**MB80** Data3								**MB80** Data2								**MB80** Data2								**MB80** Data0							
2047	unused								unused								**MB80** Data5								**MB80** Data4							

26.6.12.3 ECC Check

There is an ECC checking mechanism implemented in the E-Ray module to assure the integrity of the data stored in the seven RAM blocks of the module. The RAM blocks have an ECC generator / checker attached as shown in **Figure 26-26**. When data is written to a RAM block, the local ECC generator generates the ECC data. The ECC data is stored together with the respective data word. The ECC data is checked each time a data word is read from any of the RAM blocks.

If an ECC error is detected, the respective error flag is set. The ECC error flags **MHDS.EIBF**, **MHDS.EOBF**, **MHDS.EMR**, **MHDS.ETBF1**, **MHDS.ETBF2**, and the faulty Message Buffer indicators **MHDS.FMBD**, **MHDS.MFMB**, **MHDS.FMB** are located in the Message Handler Status register. These error flags control the error interrupt flag **EIR.EERR**.

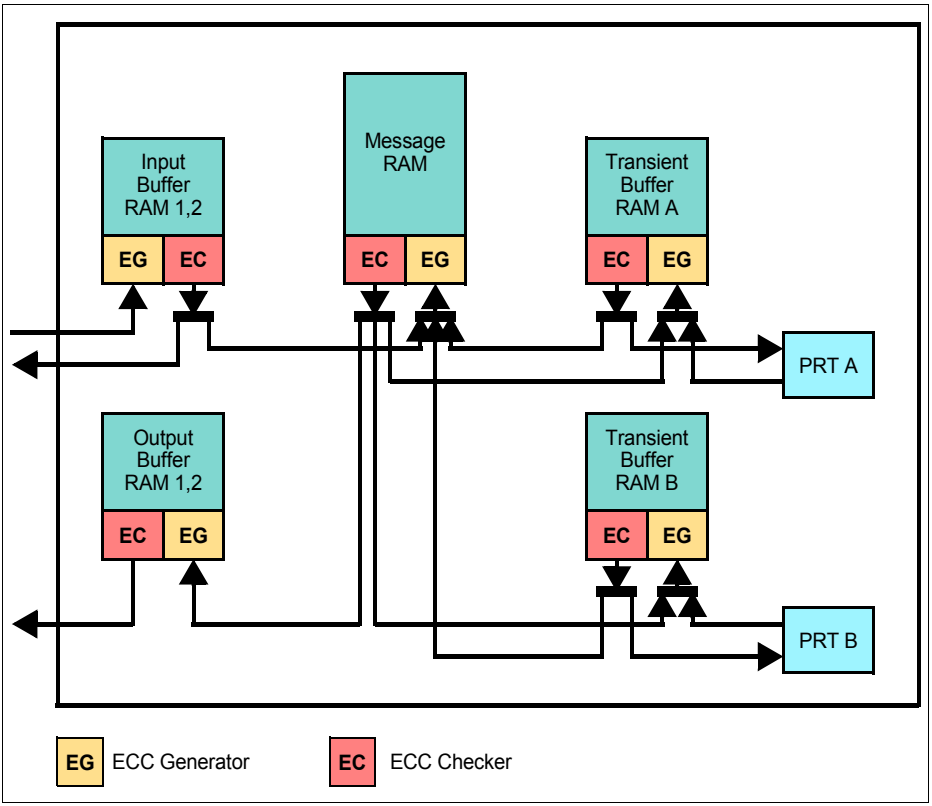


Figure 26-26 ECC Generation and Check

When an ECC error has been detected the following actions will be performed:

In all cases

- The respective ECC error flag in the Message Handler Status **MHDS** register is set
- The ECC error flag **EIR.EERR** in the Error Service Request Register is set, and if enabled, a module service request to the Host will be generated.

Additionally in specific cases

1. ECC error in data transfer from Input Buffer RAM 1,2 ⇒ Message RAM (Transfer of Header and Data Section)
   a) **MHDS.EIBF** bit is set
   b) **MHDS.FMBD** bit is set to indicate that **MHDS.FMB** has been updated
   c) **MHDS.FMB** indicates the number of the faulty Message Buffer
   d) Transmit buffer: Transmission request for the respective Message Buffer is not set
2. ECC error in data transfer from Input Buffer RAM 1,2 ⇒ Message RAM (Transfer of Data Section only)
   a) **MHDS.EMR** bit is set
   b) **MHDS.FMBD** bit is set to indicate that **MHDS.FMB** points to a faulty Message Buffer
   c) **MHDS.FMB** indicates the number of the faulty Message Buffer
   d) The Data Section of the respective Message Buffer is not updated
   e) Transmit buffer: Transmission request for the respective Message Buffer is not set
3. ECC error during host reading Input Buffer RAM
   a) • **MHDS.EIBF** bit is set
4. ECC error during scan of Header Sections in Message RAM
   a) **MHDS.EMR** bit is set
   b) **MHDS.FMBD** bit is set to indicate that **MHDS.FMB** points to a faulty Message Buffer
   c) **MHDS.FMB** indicates the number of the faulty Message Buffer
   d) Ignore Message Buffer (Message Buffer is skipped)
5. ECC error during data transfer from Message RAM ⇒ Transient Buffer RAM A, B
   a) **MHDS.EMR** bit is set
   b) **MHDS.FMBD** bit is set to indicate that **MHDS.FMB** points to a faulty Message Buffer
   c) **MHDS.FMB** indicates the number of the faulty Message Buffer
   d) Frame not transmitted, Frames already in transmission are invalidated by setting the Frame CRC to zero
6. ECC error during data transfer from Transient Buffer RAM A, B ⇒ Protocol Controller 1, 2
   a) **MHDS.ETBF1**, **MHDS.ETBF2** bit is set
7. ECC error in data transfer from Transient Buffer RAM A, B ⇒ Message RAM (ECC error when reading Header Section of respective Message Buffer from Message RAM)
   a) **MHDS.EMR** bit is set
   b) **MHDS.FMBD** bit is set to indicate that **MHDS.FMB** points to a faulty Message Buffer
   c) **MHDS.FMB** indicates the number of the faulty Message Buffer
   d) The Data Section of the respective Message Buffer is not updated

8. ECC error in data transfer from Transient Buffer RAM A, B ⇒ Message RAM (ECC error when reading Transient Buffer RAM A, B)
   a) **MHDS.ETBF1**, **MHDS.ETBF2** bit is set
   b) **MHDS.FMBD** bit is set to indicate that **MHDS.FMB** points to a faulty Message Buffer
   c) **MHDS.FMB** indicates the number of the faulty Message Buffer
9. ECC error during data transfer from Message RAM ⇒ Output Buffer RAM
   a) **MHDS.EMR** bit is set
   b) **MHDS.FMBD** bit is set to indicate that **MHDS.FMB** points to a faulty Message Buffer
   c) **MHDS.FMB** indicates the number of the faulty Message Buffer
10. ECC error during Host reading Output Buffer RAM
   a) • **MHDS.EOBF** bit is set
11. ECC error during data read of Transient Buffer RAM A, B

If an ECC error occurs while the Message Handler reads a Frame with Network Management information (PPI = 1) from the Transient Buffer RAM A, B the corresponding Network Management vector registers NMV1 to NMV3 are not updated from that Frame.

26.6.13 Host Handling of Errors

An ECC error caused by transient bit flips can be fixed by:

26.6.13.1 Self-Healing

ECC errors located in

- Input Buffer RAM 1,2
- Output Buffer RAM 1,2
- Data Section of Message RAM
- Transient Buffer RAM A
- Transient Buffer RAM B

are overwritten with the next write access to the disturbed bit(s) caused by Host access or by FlexRay communication.

26.6.13.2 CLEAR_RAMS Command

When called in DEFAULT_CONFIG or CONFIG state POC command CLEAR_RAMS initializes all module-internal RAMs to zero.

26.6.13.3 Temporary Unlocking of Header Section

An ECC error in the header section of a locked message buffer can be fixed by a transfer from the Input Buffer to the locked buffer Header Section. For this transfer, the write-

access to the IBCR (specifying the message buffer number) must be immediately preceded by the unlock sequence normally used to leave CONFIG state (see **“Lock Register (LCK)” on Page 26-39**).

For that single transfer the respective message buffer header is unlocked, regardless whether it belongs to the FIFO or whether its locking is controlled by MRC.SEC[1:0], and will be updated with new data.

26.7 Module Service Request

In general, service requests provide a close link to the protocol timing as they are triggered almost immediately when an error or status change is detected by the controller, a Frame is received or transmitted, a configured timer service request is activated, or a stop watch event occurred. This enables the Host to react very quickly on specific error conditions, status changes, or timer events. On the other hand too many service requests can cause the Host to miss deadlines required for the application. Therefore the Communication Controller supports disable / enable controls for each individual service request source separately.

An service request may be triggered when

- An error was detected
- A status flag is set
- A timer reaches a preconfigured value
- A message transfer from Input Buffer to Message RAM or from Message RAM to Output Buffer has completed
- A stop watch event occurred

Tracking status and generating service requests when a status change or an error occurs are two independent tasks. Regardless of whether an service request is enabled or not, the corresponding status is tracked and indicated by the Communication Controller. The Host has access to the actual status and error information by reading the Error Service Request Register **EIR** and the Status Service Request **SIR** Register.

Table 26-26 Module Service Request Flags and Service Request Line Enable

Register	Bit	Function
SIR	WST	Wakeup Status
	CAS	Collision Avoidance Symbol
	CYCS	Cycle Start Service Request
	TXI	Transmit Service Request
	RXI	Receive Service Request
	RFNE	Receive FIFO not Empty
	RFF	Receive FIFO Full
	NMVC	Network Management Vector Changed
	TI0	Timer Service Request 0
	TI1	Timer Service Request 1
	TIBC	Transfer Input Buffer Completed
	TOBC	Transfer Output Buffer Completed
	SWE	Stop Watch Event
	SUCS	Startup Completed Successfully
	MBSI	Message Buffer Status Interrupt
	SDS	Start of Dynamic Segment
	WUPA	Wakeup Pattern Channel A
	MTSA	MTS Received on Channel A
	WUPB	Wakeup Pattern Channel B
	MTSB	MTS Received on Channel B
ILE	EINT0	Enable Service Request Line 0
	EINT1	Enable Service Request Line 1
EIR	PEMC	Protocol Error Mode Changed
	CNA	Command Not Valid
	SFBM	SYNC Frames Below Minimum
	SFO	SYNC Frame Overflow
	CCF	Clock Correction Failure
	CCL	CHI Command Locked
	EERR	ECC Error
	RFO	Receive FIFO Overrun

Table 26-26 Module Service Request Flags and Service Request Line Enable

Register	Bit	Function
EIR	EFA	Empty FIFO Access
	IIBA	Illegal Input Buffer Access
	IOBA	Illegal Output Buffer Access
	MHF	Message Handler Constraints Flag
	EDA	Error Detected on Channel A
	LTVA	Latest Transmit Violation Channel A
	TABA	Transmission Across Boundary Channel A
	EDB	Error Detected on Channel B
	LTVB	Latest Transmit Violation Channel B
	TABB	Transmission Across Boundary Channel B

The interrupt lines to the Host TINT0SR and TINT1SR are controlled by the enabled interrupts. In addition each of the two interrupt lines can be enabled / disabled separately by programming bit ILE.EINT0/INT0SRC.SRE and ILE.EINT1/ INT1SRC.SRE.

The interrupt lines to the Host NDAT0SR and NDAT1SR are controlled by the enabled new data interrupts (**NDIC1** to **NDIC4**). In addition each of the two interrupt lines can be enabled / disabled separately by programming bit NDAT0SRC.SRE and NDAT1SRC.SRE.

The interrupt lines to the Host MBSC0SR and MBSC1SR are controlled by the enabled new data interrupts (**MSIC1** to **MSIC4**). In addition each of the two interrupt lines can be enabled / disabled separately by programming bit MBSC0SRC.SRE and MBSC1SRC.SRE.

The two timer service requests generated by service request timer 0 and 1 are available on pins TINT0SR and TINT1SR. They can be configured via the Timer 0 and Timer 1 Configuration register. In addition each of the two interrupt lines can be enabled / disabled separately by programming bit TINT0SRC.SRE and TINT1SRC.SRE.

A stop watch event may be triggered via input pin STPWn.

The status of the data transfer between IBF / OBF and the Message RAM is signalled on signals IBUSY and OBUSY. When a transfer has completed bit **SIR.TIBC** or **SIR.TOBC** is set.

26.8 Restrictions

The following restrictions have to be considered when programming the E-Ray IP-module. A violation of these restrictions may lead to an erroneous behavior of the E-Ray IP-module.

26.8.1 Message Buffers with the same Frame ID

If two or more Message Buffers are configured with the same Frame ID, and if they have a matching cycle counter filter value for the same slot, then the Message Buffer with the lowest Message Buffer number is used.

Sharing of a static time slot via cycle counter filtering between different nodes of a FlexRay™ network is **not** allowed.

26.8.2 Data Transfers between IBF / OBF and Message RAM

The time required to transfer the contents of a Message Buffer between IBF / OBF and Message RAM depends on the setup time to start the first transfer, the number of 4-byte words to be transferred, and the number of concurrent tasks to be managed by the Message Handler. The number of 4-byte words varies from 4 (Header Section only) to 68 (Header + maximum Data Section) while the number of concurrent task varies from one to three.

The following concurrent tasks are executed under control of the Message Handler:

- Data transfer between IBF or OBF and Message RAM
- Data transfer between TBF1 and Message RAM, search next TX / RX Message Buffer CHA
- Data transfer between TBF2 and Message RAM, search next TX / RX Message Buffer CHB

Transfers between IBF and Message RAM respectively Message RAM and OBF can only be handled one after another. In case that e.g. a transfer between IBF and Message RAM has been started shortly before a transfer between Message RAM and OBF is requested, the OBF transfer has to wait until the IBF transfer has completed.

The relative time is measured in f_{CLC_ERAY} cycles. Absolute time depends on the actual f_{CLC_ERAY} cycle period.

cyclestrans = (remaining cycles of transfer running) + (cycles of requested transfer)

cyclestrans = cyclesrem + cyclesreq

cyclesrem = (number of concurrent tasks) * (setup time + (number of 4-byte words)rem)

cyclesreq = (number of concurrent tasks) * (setup time + (number of 4-byte words)req)

setup time = 2 f_{CLC_ERAY} cycles

Under worst case conditions a transfer is requested directly after the previous transfer started:

Max. number of f_{CLC_ERAY} cycles: cyclestrans = (3 * (2 + 68)) + (3 * (2 + 68)) = 420

Worst case timing: timetrans(40MHz) = 420 * 25ns = 10.5 ms

26.9 E-Ray Module Implementation

This section describes the E-Ray interfaces as implemented in TC1798 with the clock control, port and DMA connections, interrupt control, and address decoding.

Figure 26-27 shows a detailed view of the E-Ray interface.

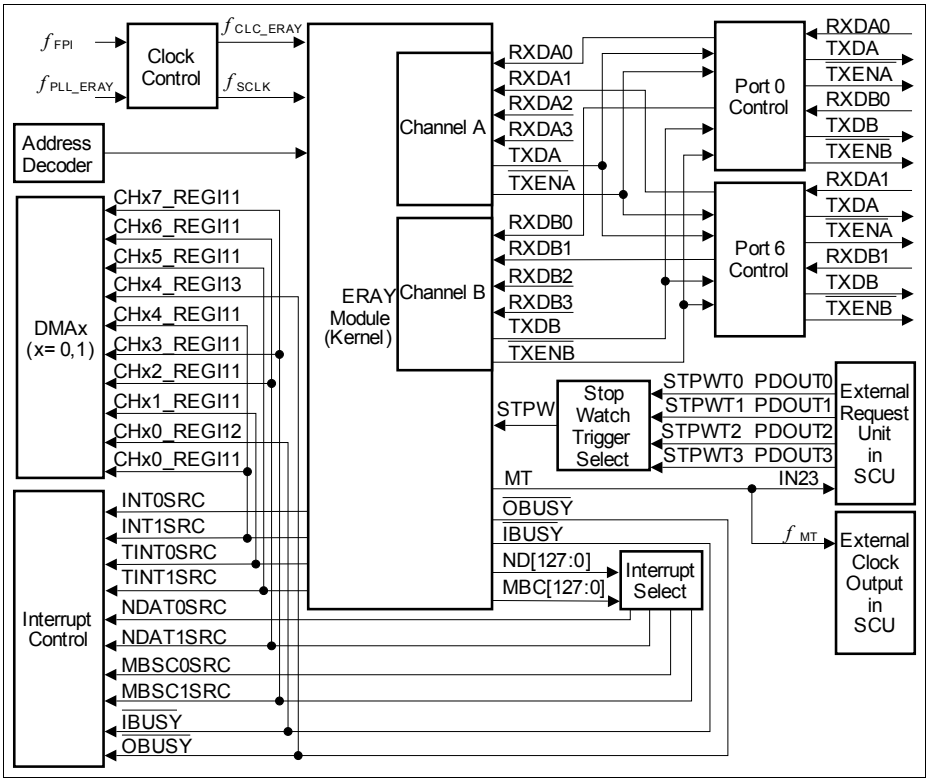


Figure 26-27 Detailed Block Diagram of the E-Ray Interface

26.9.1 Interconnections of the E-Ray Module

The E-Ray module has 2 FlexRay™ communication channels, channel A and channel B. Each channel provides a set of signals to drive a bus driver. The E-Ray module requires two different clocks, a sampling clock of the FlexRay™ bus f_{SCLK}. f_{SCLK} has to be 8 times the baud rate of the FlexRay™ communication. A second clock f_{CLC_ERAY} is

used for the main protocol controller state machine and the customer interface logic. To enable deactivation of the E-Ray Module, f_{CLC_ERAY} and f_{SCLK} may be disabled (clock gated) by the **CLC.DISR** Enable E-Ray (Clock Gating) bit.The following items are described in this section:

- E-Ray module (kernel) external registers
- Port control and connections
  - I/O port line assignment
  - I/O function selection
  - Pad driver characteristics selection
- On-chip connections
  - SCU Connections
  - DMA connections
- Module clock generation
- Interrupt registers
- E-Ray address map

26.9.2 Port Control and Connections

This section describes the I/O connections of the E-Ray module.

26.9.2.1 Input/Output Function Selection

Table 26-27 shows how bits and bit fields must be programmed for the required I/O functionality of the E-Ray I/O lines. This table also shows the values of the peripheral input select registers.

Table 26-27 E-Ray I/O Control Selection and Setup

FlexRay™ Channel	Port Lines	Input Select Register	Input/Output Control Register Bits	I/O
A	RXDA0/ P0.9	ERAY_**CUST1.RISA** = 00_B	P0_IOCR8.PC9 = $0XXX_B$	Input
	RXDA1/ P6.12	ERAY_**CUST1.RISA** = 01_B	P6_IOCR12.PC12 = $0XXX_B$	Input
	RXDA2	ERAY_**CUST1.RISA** = 10_B		Input
	RXDA3	ERAY_**CUST1.RISA** = 11_B		Input
	TXDA/ P0.14	not applicable	P0_IOCR12.PC14 = $1X01_B$	Output
	TXDA/ P6.13	not applicable	P6_IOCR12.PC13 = $1X10_B$	Output
	$\overline{\text{TXENA}}$/ P0.10	not applicable	P0_IOCR8.PC10 = $1X01_B$	Output
	$\overline{\text{TXENA}}$/ P6.10	not applicable	P6_IOCR8.PC10 = $1X11_B$	Output
B	RXDB0/ P0.13	ERAY_**CUST1.RISB** = 00_B	P0_IOCR12.PC13 = $0XXX_B$	Input
	RXDB1/ P6.14	ERAY_**CUST1.RISB** = 01_B	P6_IOCR12.PC14 = $0XXX_B$	Input
	RXDB2	ERAY_**CUST1.RISB** = 10_B		Input
	RXDB3	ERAY_**CUST1.RISB** = 11_B		Input
	TXDB/ P0.12	not applicable	P0_IOCR12.PC12 = $1X01_B$	Output
	TXDB/ P6.15	not applicable	P6_IOCR12.PC15 = $1X10_B$	Output
	$\overline{\text{TXENB}}$/ P0.11	not applicable	P0_IOCR8.PC11 = $1X01_B$	Output
	$\overline{\text{TXENB}}$/ P6.11	not applicable	P6_IOCR8.PC11 = $1X11_B$	Output

26.9.3 On-Chip Connections

This section describes all on-chip interconnections of the E-Ray modules except the connections to I/O ports (see **Section 26.9.2**).

26.9.3.1 E-Ray Connections with DMA

The E-Ray module of the TC1798 has several on-chip interconnections to the DMA modules. **Table 26-28** shows these interconnections. These enable the DMA to handle different service request of E-Ray module via the DMA.

Table 26-28 DMA Request Assignment for DMA Sub-Block 0 and DMA Sub-Block 1

DMA Channel	ERAY Output Signal	DMA Request Input Line	Selected by
00	INT1SRC	CH00_REGI11	CHCR00.PRSEL = 1011_B
00	IBUSY	CH00_REGI12	CHCR00.PRSEL = 1100_B
01	TINT0SRC	CH01_REGI11	CHCR01.PRSEL = 1011_B
02	NDAT1SRC	CH02_REGI11	CHCR02.PRSEL = 1011_B
03	MBSC1SRC	CH03_REGI11	CHCR03.PRSEL = 1011_B
04	INT1SRC	CH04_REGI11	CHCR04.PRSEL = 1011_B
04	OBUSY	CH04_REGI13	CHCR04.PRSEL = 1101_B
05	TINT1SRC	CH05_REGI11	CHCR05.PRSEL = 1011_B
06	NDAT1SRC	CH06_REGI11	CHCR06.PRSEL = 1011_B
07	MBSC1SRC	CH07_REGI11	CHCR07.PRSEL = 1011_B
10	INT1SRC	CH10_REGI11	CHCR10.PRSEL = 1011_B
10	IBUSY	CH10_REGI12	CHCR10.PRSEL = 1100_B
11	TINT0SRC	CH11_REGI11	CHCR11.PRSEL = 1011_B
12	NDAT1SRC	CH12_REGI11	CHCR12.PRSEL = 1011_B
13	MBSC1SRC	CH13_REGI11	CHCR13.PRSEL = 1011_B
14	INT1SRC	CH14_REGI11	CHCR14.PRSEL = 1011_B
14	OBUSY	CH14_REGI13	CHCR14.PRSEL = 1101_B
15	TINT1SRC	CH15_REGI11	CHCR15.PRSEL = 1011_B
16	NDAT1SRC	CH16_REGI11	CHCR16.PRSEL = 1011_B
17	MBSC1SRC	CH17_REGI11	CHCR17.PRSEL = 1011_B

26.9.3.2 E-Ray Connections with the External Request Unit of SCU

The E-Ray module of the TC1798 has several on-chip interconnections to the External Request Unit (ERU) in the SCU to externally trigger stop watch events and to provide a global time e.g. to the on chip timers. **Table 26-29** and **Table 26-30** show these interconnections.

Table 26-29 External Stop Watch Request Assignment

ERAY Input Signal	ERU Request Output Line	Selected by
STPWT0	ERU_PDOUT0	**CUST1.STPWTS** = 00_B
STPWT1	ERU_PDOUT1	**CUST1.STPWTS** = 01_B
STPWT2	ERU_PDOUT2	**CUST1.STPWTS** = 10_B
STPWT3	ERU_PDOUT3	**CUST1.STPWTS** = 11_B

Table 26-30 Global Macrotick Connection to ERU

ERAY Output Signal	ERU Request Input Line	Selected by
MT	ERU_IN23	ERU_EICR1.EXIS2 = 11_B

26.9.3.3 E-Ray Connections with the ECC Error Handling Unit of SCU

The E-Ray module of the TC1798 has one on-chip interconnection to the ECC Error Handling Unit in the SCU to trigger an ECC Error Trap. **Table 26-31** shows this interconnection.

Table 26-31 ECC Error Signalling to SCU

ERAY Output Signal	SCU Line	Selected by
EERR	ECCT	TRAPDIS.ECCT = 0_B

26.9.3.4 E-Ray Connections with the External Clock Output of SCU

The E-Ray module of the TC1798 has one on-chip interconnections to the External Clock Output Unit in the SCU to distribute externally as also internally the Macro Tick as time base for distributed system control e.g. to the GPTA® as global system timer or external devices. **Table 26-32** shows this interconnection.

Table 26-32 Global Macrotick Connection to External Clock Output

ERAY Output Signal	External Clock Output	Selected by
MT	f_{MT}	SCU_EXCTCON.SEL0 = 1111_B

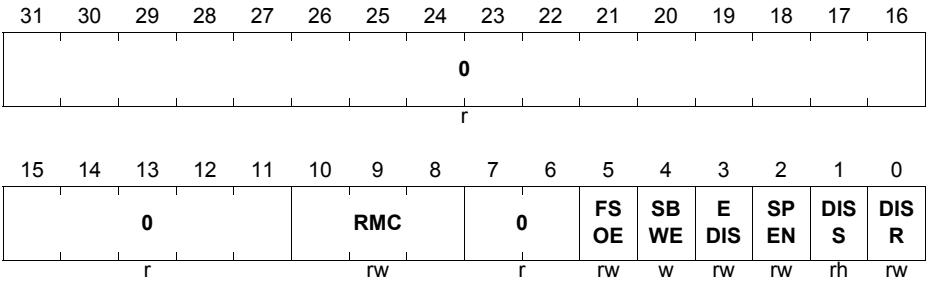
26.9.4 Clock Control Register

The clock control register makes it possible to control (enable/disable) the E-Ray module control clock f_{CLC_ERAY}. The clock signal f_{CLC_ERAY} is used by the E-Ray as a clock for internal control operations but not for FlexRay™ Bus Signal Sampling.

After an application reset, by default, the startup software (SSW) will disable the module by setting CLC.DISR and thereby requesting the HW to set bit CLC.DISS. In consequence, the initial value readable by the application is $0x0000\ 0003_H$

Note: The application SW must make sure that the Transceiver Enable ($\overline{TXENA}$, $\overline{TXENB}$) pins are forced to their inactive state first, before the module clock is switched off.

ERAY_CLC
ERAY Clock Control Register (0000_H) Reset Value: $0000\ 0100_H$



Field	Bits	Type	Description
DISR	0	rw	**E-Ray Module Disable Request Bit** Used for enable/disable control of the E-Ray module. *Note: This bit disables the kernel clocks f_{CLC_ERAY} and the sampling clock f_{SCLK}.*
DISS	1	rh	**E-Ray Module Disable Status Bit** Bit indicates the current status of the E-Ray module.
SPEN	2	rw	**E-Ray Module Suspend Enable for OCDS** Used to enable the suspend mode.
EDIS	3	rw	**External Request Disable** Used to control the external clock disable request.
SBWE	4	w	**E-Ray Module Suspend Bit Write Enable for OCDS** Determines whether SPEN and FSOE are write-protected.

Field	Bits	Type	Description
FSOE	5	rw	**Fast Switch Off Enable** Used for fast clock switch off in suspend mode.
RMC	[10:8]	rw	**Clock Divider in Run Mode** 000_B No clock signal f_{CLC_ERAY} generated (default after reset) 001_B Clock $f_{CLC\_ERAY} = f_{FPI}$ selected 010_B Clock $f_{CLC\_ERAY} = f_{FPI}$ /2 selected 011_B Clock $f_{CLC\_ERAY} = f_{FPI}$ /3 selected 100_B Clock $f_{CLC\_ERAY} = f_{FPI}$ /4 selected 101_B Clock $f_{CLC\_ERAY} = f_{FPI}$ /5 selected 110_B Clock $f_{CLC\_ERAY} = f_{FPI}$ /6 selected 111_B Clock $f_{CLC\_ERAY} = f_{FPI}$ /7 selected *Note: This bit field is not affected by an application reset.* *Note: This bit field only controls the kernel clock f_{CLC_ERAY} and not the sampling clock f_{SCLK}.*
0	[7:6], [31:11]	r	**Reserved** Read as 0; should be written with 0.

Note: After an application reset, the f_{CLC_ERAY} clock is disabled (DISS set). Therefore, the E-Ray modules clock generation is completely disabled.

26.9.5 Interrupt Registers

Two different type of Interrupt Registers are described within this chapter.
The Interrupt Control register enable the selection of the Service Request used to signal an event. The Interrupt Control registers **NDIC1** to **NDIC4** select the service request node used for New Data Events.The Interrupt Control registers **MSIC1** to **MSIC4** select the service request node used for Message Buffer Status Changed Events.
The Interrupt Service Request Control Registers control the eight service request nodes.

New Data Interrupt Control 1 (NDIC1)

This New Data Interrupt Control register controls the interrupt that becomes active (NDAT0SRC or NDAT1SRC) on a ND flag turning active of all configured Message Buffers 0 to Message Buffers 31.

NDIC1
New Data Interrupt Control 1 **($03A8_H$)** **Reset Value: $0000\ 0000_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NDIP 31	**NDIP 30**	**NDIP 29**	**NDIP 28**	**NDIP 27**	**NDIP 26**	**NDIP 25**	**NDIP 24**	**NDIP 23**	**NDIP 22**	**NDIP 21**	**NDIP 20**	**NDIP 19**	**NDIP 18**	**NDIP 17**	**NDIP 16**
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NDIP 15	**NDIP 14**	**NDIP 13**	**NDIP 12**	**NDIP 11**	**NDIP 10**	**NDIP 9**	**NDIP 8**	**NDIP 7**	**NDIP 6**	**NDIP 5**	**NDIP 4**	**NDIP 3**	**NDIP 2**	**NDIP 1**	**NDIP 0**
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
NDIPn (n = 0-31)	n	rw	**New Data Interrupt Pointer n (n = 0-31)** NDIPn determines the interrupt (NDAT0SRC or NDAT1SRC) of the service request output that becomes active on a New Data Flag becoming active. 0_B NDAT0SRC selected for New Data Service Request 1_B NDAT1SRC selected for New Data Service Request

New Data Interrupt Control 2 (NDIC2)

This New Data Interrupt Control register controls the interrupt that becomes active (NDAT0SRC or NDAT1SRC) on a ND flag turning active of all configured Message Buffers 32 to Message Buffers 63.

NDIC2
New Data Interrupt Control 2 **($03AC_H$)** **Reset Value: $0000\ 0000_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NDIP 63	**NDIP 62**	**NDIP 61**	**NDIP 60**	**NDIP 59**	**NDIP 58**	**NDIP 57**	**NDIP 56**	**NDIP 55**	**NDIP 54**	**NDIP 53**	**NDIP 52**	**NDIP 51**	**NDIP 50**	**NDIP 49**	**NDIP 48**
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NDIP 47	**NDIP 46**	**NDIP 45**	**NDIP 44**	**NDIP 43**	**NDIP 42**	**NDIP 41**	**NDIP 40**	**NDIP 39**	**NDIP 38**	**NDIP 37**	**NDIP 36**	**NDIP 35**	**NDIP 34**	**NDIP 33**	**NDIP 32**
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
NDIPn (n = 32-63)	n - 32	rw	**New Data Interrupt Pointer n (n = 32-63)** NDIPn determines the interrupt (NDAT0SRC or NDAT1SRC) of the service request output that becomes active on a New Data Flag becoming active. 0_B NDAT0SRC selected for New Data Service Request 1_B NDAT1SRC selected for New Data Service Request

New Data Interrupt Control 3 (NDIC3)

This New Data Interrupt Control register controls the interrupt that becomes active (NDAT0SRC or NDAT1SRC) on a ND flag turning active of all configured Message Buffers 64 to Message Buffers 95.

NDIC3
New Data Interrupt Control 3 ($03B0_H$) Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NDIP 95	**NDIP 94**	**NDIP 93**	**NDIP 92**	**NDIP 91**	**NDIP 90**	**NDIP 89**	**NDIP 88**	**NDIP 87**	**NDIP 86**	**NDIP 85**	**NDIP 84**	**NDIP 83**	**NDIP 82**	**NDIP 81**	**NDIP 80**
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NDIP 79	**NDIP 78**	**NDIP 77**	**NDIP 76**	**NDIP 75**	**NDIP 74**	**NDIP 73**	**NDIP 72**	**NDIP 71**	**NDIP 70**	**NDIP 69**	**NDIP 68**	**NDIP 67**	**NDIP 66**	**NDIP 65**	**NDIP 64**
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
NDIPn (n = 64-95)	n - 64	rw	**New Data Interrupt Pointer n (n = 64-95)** NDIPn determines the interrupt (NDAT0SRC or NDAT1SRC) of the service request output that becomes active on a New Data Flag becoming active. 0_B NDAT0SRC selected for New Data Service Request 1_B NDAT1SRC selected for New Data Service Request

New Data Interrupt Control 4 (NDIC4)

This New Data Interrupt Control register controls the interrupt that becomes active (NDAT0SRC or NDAT1SRC) on a ND flag turning active of all configured Message Buffers 96 to Message Buffers 127.

NDIC4
New Data Interrupt Control 4 **($03B4_H$)** **Reset Value: $0000\ 0000_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NDIP 127	**NDIP 126**	**NDIP 125**	**NDIP 124**	**NDIP 123**	**NDIP 122**	**NDIP 121**	**NDIP 120**	**NDIP 119**	**NDIP 118**	**NDIP 117**	**NDIP 116**	**NDIP 115**	**NDIP 114**	**NDIP 113**	**NDIP 112**
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NDIP 111	**NDIP 110**	**NDIP 109**	**NDIP 108**	**NDIP 107**	**NDIP 106**	**NDIP 105**	**NDIP 104**	**NDIP 103**	**NDIP 102**	**NDIP 101**	**NDIP 100**	**NDIP 99**	**NDIP 98**	**NDIP 97**	**NDIP 96**
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
NDIPn (n = 96-127)	n - 96	rw	**New Data Interrupt Pointer n (n = 96-127)** NDIPn determines the interrupt (NDAT0SRC or NDAT1SRC) of the service request output that becomes active on a New Data Flag becoming active. 0_B NDAT0SRC selected for New Data Service Request 1_B NDAT1SRC selected for New Data Service Request

Message Buffer Status Changed Interrupt Control 1 (MSIC1)

This Message Buffer Status Change Interrupt Control register controls the interrupt that becomes active (MBSC0SRC or MBSC1SRC) on a MBC flag of all configured Message Buffer 0 to Message Buffer 31 turning active.

MSIC1
Message Buffer Status Changed Interrupt Control 1
($03B8_H$) **Reset Value: 0000 0000$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSIP 31	**MSIP 30**	**MSIP 29**	**MSIP 28**	**MSIP 27**	**MSIP 26**	**MSIP 25**	**MSIP 24**	**MSIP 23**	**MSIP 22**	**MSIP 21**	**MSIP 20**	**MSIP 19**	**MSIP 18**	**MSIP 17**	**MSIP 16**
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSIP 15	**MSIP 14**	**MSIP 13**	**MSIP 12**	**MSIP 11**	**MSIP 10**	**MSIP 9**	**MSIP 8**	**MSIP 7**	**MSIP 6**	**MSIP 5**	**MSIP 4**	**MSIP 3**	**MSIP 2**	**MSIP 1**	**MSIP 0**
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
MSIPn (n = 0-31)	n	rw	**Message Buffer Status Changed Interrupt Pointer n (n = 0-31)** MSIPn determines the interrupt (MBSC0SRC or MBSC1SRC) of the service request output that becomes active on a Message Buffer Status Changed Flag becoming active. 0_B MBSC0SRC selected for Message Buffer Status Changed Service Request 1_B MBSC1SRC selected for Message Buffer Status Changed Service Request

Message Buffer Status Changed Interrupt Control 2 (MSIC2)

This Message Buffer Status Change Interrupt Control register controls the interrupt that becomes active (MBSC0SRC or MBSC1SRC) on a MBC flag of all configured Message Buffer 32 to Message Buffer 63 turning active.

MSIC2
Message Buffer Status Changed Interrupt Control 2
($03BC_H$) **Reset Value: 0000 0000$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSIP 63	**MSIP 62**	**MSIP 61**	**MSIP 60**	**MSIP 59**	**MSIP 58**	**MSIP 57**	**MSIP 56**	**MSIP 55**	**MSIP 54**	**MSIP 53**	**MSIP 52**	**MSIP 51**	**MSIP 50**	**MSIP 49**	**MSIP 48**
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSIP 47	**MSIP 46**	**MSIP 45**	**MSIP 44**	**MSIP 43**	**MSIP 42**	**MSIP 41**	**MSIP 40**	**MSIP 39**	**MSIP 38**	**MSIP 37**	**MSIP 36**	**MSIP 35**	**MSIP 34**	**MSIP 33**	**MSIP 32**
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
MSIPn (n = 32-63)	n - 32	rh	**Message Buffer Status Changed Interrupt Pointer n (n = 32-63)** MSIPn determines the interrupt (MBSC0SRC or MBSC1SRC) of the service request output that becomes active on a Message Buffer Status Changed Flag becoming active. 0_B MBSC0SRC selected for Message Buffer Status Changed Service Request 1_B MBSC1SRC selected for Message Buffer Status Changed Service Request

Message Buffer Status Changed Interrupt Control 3 (MSIC3)

This Message Buffer Status Change Interrupt Control register controls the interrupt that becomes active (MBSC0SRC or MBSC1SRC) on a MBC flag of all configured Message Buffer 64 to Message Buffer 95 turning active.

MSIC3
Message Buffer Status Changed Interrupt Control 3
($03C0_H$) **Reset Value: 0000 0000$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSIP 95	**MSIP 94**	**MSIP 93**	**MSIP 92**	**MSIP 91**	**MSIP 90**	**MSIP 89**	**MSIP 88**	**MSIP 87**	**MSIP 86**	**MSIP 85**	**MSIP 84**	**MSIP 83**	**MSIP 82**	**MSIP 81**	**MSIP 80**
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSIP 79	**MSIP 78**	**MSIP 77**	**MSIP 76**	**MSIP 75**	**MSIP 74**	**MSIP 73**	**MSIP 72**	**MSIP 71**	**MSIP 70**	**MSIP 69**	**MSIP 68**	**MSIP 67**	**MSIP 66**	**MSIP 65**	**MSIP 64**
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
MSIPn (n = 64-95)	n - 64	rw	**Message Buffer Status Changed Interrupt Pointer n (n = 64-95)** MSIPn determines the interrupt (MBSC0SRC or MBSC1SRC) of the service request output that becomes active on a Message Buffer Status Changed Flag becoming active. 0_B MBSC0SRC selected for Message Buffer Status Changed Service Request 1_B MBSC1SRC selected for Message Buffer Status Changed Service Request

Message Buffer Status Changed Interrupt Control 4 (MSIC4)

This Message Buffer Status Change Interrupt Control register controls the interrupt that becomes active (MBSC0SRC or MBSC1SRC) on a MBC flag of all configured Message Buffer 96 to Message Buffer 127 turning active.

MSIC4
Message Buffer Status Changed Interrupt Control 4
($03C4_H$) **Reset Value: 0000 0000$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MSIP 127	**MSIP 126**	**MSIP 125**	**MSIP 124**	**MSIP 123**	**MSIP 122**	**MSIP 121**	**MSIP 120**	**MSIP 119**	**MSIP 118**	**MSIP 117**	**MSIP 116**	**MSIP 115**	**MSIP 114**	**MSIP 113**	**MSIP 112**
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MSIP 111	**MSIP 110**	**MSIP 109**	**MSIP 108**	**MSIP 107**	**MSIP 106**	**MSIP 105**	**MSIP 104**	**MSIP 103**	**MSIP 102**	**MSIP 101**	**MSIP 100**	**MSIP 99**	**MSIP 98**	**MSIP 97**	**MSIP 96**
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
MSIPn (n = 96-127)	n - 96	rw	**Message Buffer Status Changed Interrupt Pointer n (n = 96-127)** MSIPn determines the interrupt (MBSC0SRC or MBSC1SRC) of the service request output that becomes active on a Message Buffer Status Changed Flag becoming active. 0_B MBSC0SRC selected for Message Buffer Status Changed Service Request 1_B MBSC1SRC selected for Message Buffer Status Changed Service Request

Service Request Control Registers

Each of the service request outputs of the E-Ray module kernels is able to generate an interrupt and is controlled by an interrupt service request control register INT0SRC, INT1SRC, TINT0SRC, TINT1SRC, NDAT0SRC, NDAT1SRC, MBSC0SRC, MBSC1SRC, OBUSYSRC, and IBUSYSRC.The service request OBUSYSRC, and IBUSYSRC is generated, when the Output Buffer or Input Buffer switches from busy state to the state being accessible by the host.

INT0SRC
Interrupt 0 Service Request Control Register
($3EC_H$) **Reset Value: $0000\ 0000_H$**

INT1SRC
Interrupt 1 Service Request Control Register
($3E8_H$) **Reset Value: $0000\ 0000_H$**

TINT0SRC
Timer Interrupt 0 Service Request Control Register
($3E4_H$) **Reset Value: $0000\ 0000_H$**

TINT1SRC
Timer Interrupt 1 Service Request Control Register
($3E0_H$) **Reset Value: $0000\ 0000_H$**

NDAT0SRC
New Data 0 Service Request Control Register
($3DC_H$) **Reset Value: $0000\ 0000_H$**

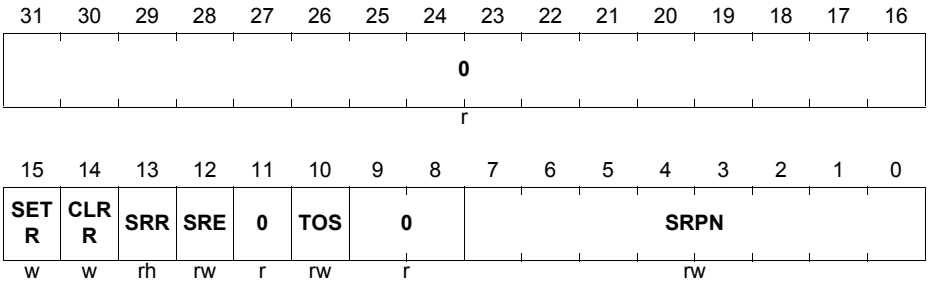
NDAT1SRC
New Data 1 Service Request Control Register
($3D8_H$) **Reset Value: $0000\ 0000_H$**

MBSC0SRC
Message Buffer Status Changed 0 Service Request Control Register
($3D4_H$) **Reset Value: $0000\ 0000_H$**

MBSC1SRC
Message Buffer Status Changed 1 Service Request Control Register
($3D0_H$) **Reset Value: $0000\ 0000_H$**

OBUSYSRC
Output Buffer Busy Service Request Control Register
($3CC_H$) **Reset Value: $0000\ 0000_H$**

IBUSYSRC
Input Buffer Busy Service Request Control Register
($3C8_H$) **Reset Value: $0000\ 0000_H$**



Field	Bits	Type	Description
SRPN	[7:0]	rw	**Service Request Priority Number**
TOS	10	rw	**Type of Service Control**
SRE	12	rw	**Service Request Enable**
SRR	13	rh	**Service Request Flag**
CLRR	14	w	**Request Clear Bit**
SETR	15	w	**Request Set Bit**
0	[9:8], 11, [31:16]	r	**Reserved** Read as 0; should be written with 0.

Note: Additional details on service request nodes and the service request control registers are described in Chapter “Interrupt System” of the TC1798 User´s Manual System Units part (Volume 1).

27 Micro Link Interface (MLI)

This chapter describes the Micro Link Interface module and the MLI protocol. It contains the following sections:

- Functional description of the MLI (see **Page 27-2**)
- Module kernel description (see **Page 27-27**)
- Operation the MLI module (see **Page 27-69**)
- MLI kernel register descriptions (see **Page 27-77**)
- Device implementation-specific descriptions and details (see **Page 27-127**)

*Note: The MLI kernel register names described in **Section 27.3** are referenced in the TC1798 User´s Manual by the module name prefix “MLI0_” for the MLI0 interface and “MLI1_” for the MLI1 interface.*

27.1 Functional Description

This chapter describes the functionality of the MLI interface.

- A general introduction to the interface (see **Page 27-2**)
- The MLI frame structure for data exchange (see **Page 27-10**)

27.1.1 General Introduction

The introduction comprises:

- An overview about the MLI (see **Page 27-2**)
- Naming conventions (see **Page 27-4**)
- A description of the MLI communication principles (see **Page 27-6**)

27.1.1.1 MLI Overview

The Micro Link Interface (MLI) is a fast synchronous serial interface to exchange data between microcontrollers or other devices, such as stand-alone peripheral components. **Figure 27-1** shows how two microcontrollers are typically connected together via their MLI interfaces.

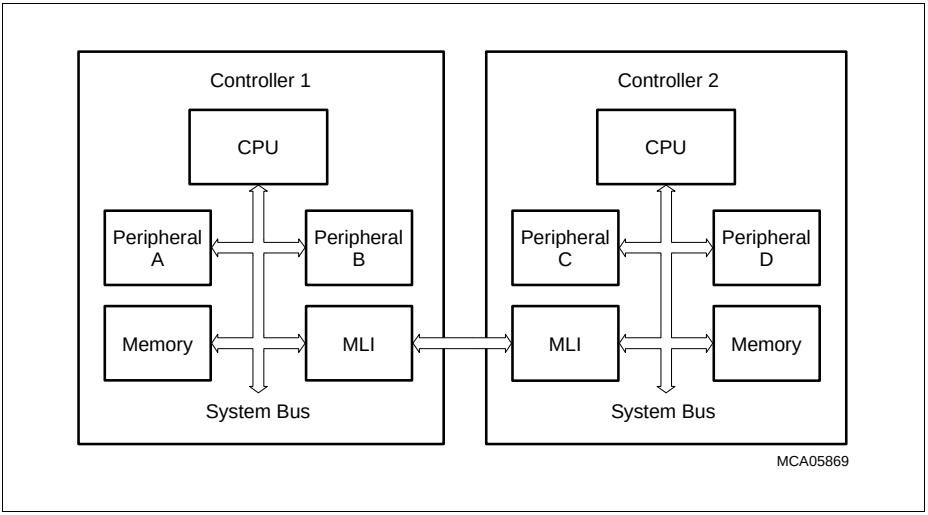


Figure 27-1 Typical Micro Link Interface Connection

Features

- Synchronous serial communication between an MLI transmitter and an MLI receiver
- Different system clock speeds supported in MLI transmitter and MLI receiver due to full handshake protocol (4 lines between a transmitter and a receiver)
- Fully transparent read/write access supported (= remote programming)
- Complete address range of target device available
- Specific frame protocol to transfer commands, addresses and data
- Error detection by parity bit
- 32-bit, 16-bit, or 8-bit data transfers supported
- Programmable baud rates
  - MLI transmitter baud rate: max. $f_{MLI}/2$
  - MLI receiver baud rate: max. f_{MLI}
- Address range protection scheme to block unauthorized accesses
- Multiple receiving devices supported

27.1.1.2 Naming Conventions

Local and Remote Controller

The terms “Local” and “Remote” Controller are assigned to the two partners (microcontrollers or other devices with MLI modules) of a serial MLI connection. The controller with an MLI module initiating a data exchange or a control task is defined as Local Controller. Each data exchange and control task starts with a frame transmission of the Local Controller. The controller with an MLI module reacting on received data exchange requests or executing control tasks is defined as Remote Controller. The terms “Local” and “Remote” are independent of the direction of the information flow (transmission or reception), except for Read Frames (always transmitted by the Local Controller) and Answer Frames (always transmitted by the Remote Controller). A Triggered Command Frame is transferred from the Local to the Remote Controller.

Due to the full duplex operation capability of an MLI module (independent transmitter and receiver), each microcontroller with an MLI module is able to operate as a Local Controller (e.g. for data transmission) as well as a Remote Controller (e.g. for data reception) at the same time.

Transmitting and Receiving Controller

The terms “transmitting” and “receiving” controller are referring to the direction of the information flow. These terms are independent from the terms “Local” and “Remote”. For example, the initialization of a bidirectional MLI connection between two controllers (or between a controller and a stand-alone device) is always controlled and initiated by one controller (named Local), although during this phase, both MLI participants can transmit and receive frames.

Due to the full duplex operation capability of the MLI module (independent transmitter and receiver), each microcontroller with an MLI module is able to operate as a transmitting controller as well as a receiving controller at the same time.

Transfer Window

A Transfer Window is an address space in the address map of the transmitting controller. Transfer Windows are typically assigned to a fixed address space (base address and size). The Transfer Windows are the logical data inputs for the MLI transmitter. Data write actions via MLI are initiated by a write access to a Transfer Window, whereas data read actions are started by a read access from a Transfer Window.

Each MLI module supports up to four independent Transfer Windows, one for each pipe. In the implementation of a specific device, a Transfer Window can appear at several locations in the address map. Here, each Transfer Window can be accessed at two different address ranges with two different window sizes (one 64 Kbyte and one 8 Kbyte area for each Transfer Window), leading to:

- Four Small Transfer Windows STW with 8 Kbyte address range each and

- Four Large Transfer Windows LTW with 64 Kbyte address range each

Remote Window

A Remote Window is an area in the address space of the receiving controller. Remote Window parameters (base address and size) of the receiving controller are programmable by the transmitting microcontroller by MLI transfers, independently for each pipe. Each Remote Window of a receiving controller is related to specific Transfer Window of the transmitting controller.

The Remote Windows are the logical data outputs of the MLI receiver. If enabled, the MLI module can automatically execute the requested data transfer to/from the defined address location in the Remote Window. If the automatic data handling is disabled, the offset and the data are available in the MLI receiver registers and have to be handled by software. Remote windows can not be accessed by read or write accesses by software of the Remote Controller (either the data is automatically transferred or it is located in receiver registers).

Pipe

A pipe defines the logical connection between a Transfer Window in the transmitting controller and the associated Remote Window in the receiving controller. The MLI protocol supports four independent pipes.

Frame

A frame is a contiguous set of bits forming a message sent by an MLI transmitter to an MLI receiver.

A **Normal Frame** is a frame used for data exchange between a transmitting and a receiving controller (read request and write data from a Local Controller to a Remote Controller, as well as the answer to a read request back to the Local Controller). Base address copy frames are also considered as Normal Frames.

A **Command Frame** contains information about the receiver setting or triggers actions in the MLI receiver.

A **Triggered Command Frame** is generated under hardware control and can be used to transfer interrupt or service requests between the MLI participants.

Offset

The offset is an address distance relative to the base address of the Transfer Window in the transmitting controller and the base address of the Remote Window in the receiving controller. For example, a write access to the 10th byte of the Transfer Window is transferred to a write to the 10th byte of the Remote Window.

The offset of a write access to a Transfer Window is also called write offset, whereas a read offset is related to a read access from a Transfer Window.

27.1.1.3 MLI Communication Principles

The communication principle of the MLI modules allows data to be transferred between a Local and a Remote Controller without intervention of a CPU in the Remote Controller. Data transfers are always triggered in the Local Controller by read or write operations to an address location in a Transfer Window. All control tasks, address and data transmissions that are required for the data transfer/request between Local and Remote Controller can be handled autonomously by the two connected MLI modules.

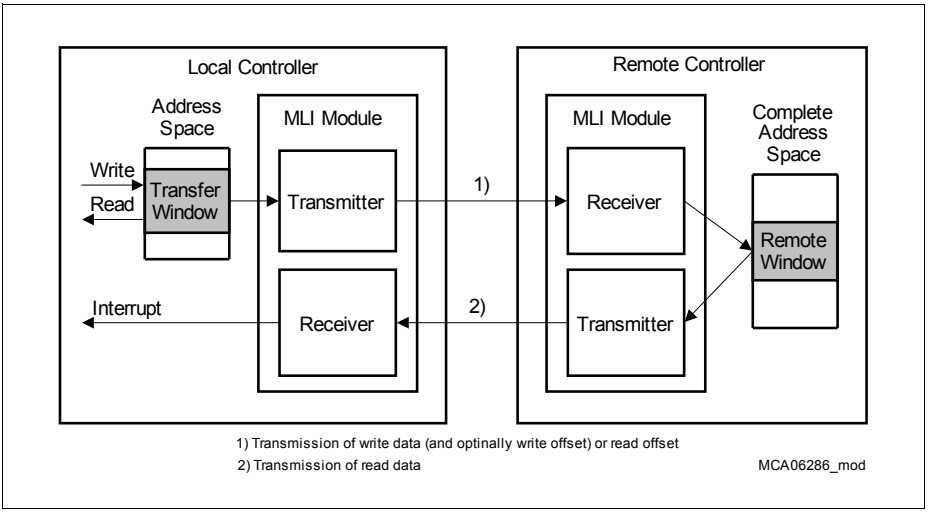


Figure 27-2 MLI Communication Principles

Write Access to a Transfer Window

A write access to a location within a Transfer Window of the transmitting (Local) controller is detected by the MLI transmitter. This detection initiates a transfer of the data that has been written to the Transfer Window together with the write offset to the MLI of the receiving controller. The receiving controller stores the data internally and can also automatically place the data in the Remote Window of the receiving controller (at the address location defined by the write offset plus the base address).

Read Access from a Transfer Window

A read access from a location of a Transfer Window in the Local Controller is detected by the MLI transmitter and delivers dummy data. This detection initiates a transfer of the read offset from the Local microcontroller to the MLI receiver to request data from the Remote Controller. This data can be automatically read or prepared by a CPU in the Remote Controller. When the requested data is available in the Remote Controller, it is

introduced into the data stream back to the Local Controller (Answer Frame). Then, the CPU in the Local Controller is informed by an MLI event that the requested data is now available and can be read.

Transfer Window Organization

Figure 27-3 shows an example of the organization of Transfer Windows and Remote Windows with a possible assignment in Local and Remote Controller. Each of the four pipes assigns one Transfer Window to one Remote Window with its base address and window size. For reasons of simplicity, a pipe to a Remote Window is only shown either from a LTW or from a STW, although each Transfer Window can be accessed at both address locations, its LTW and its STW.

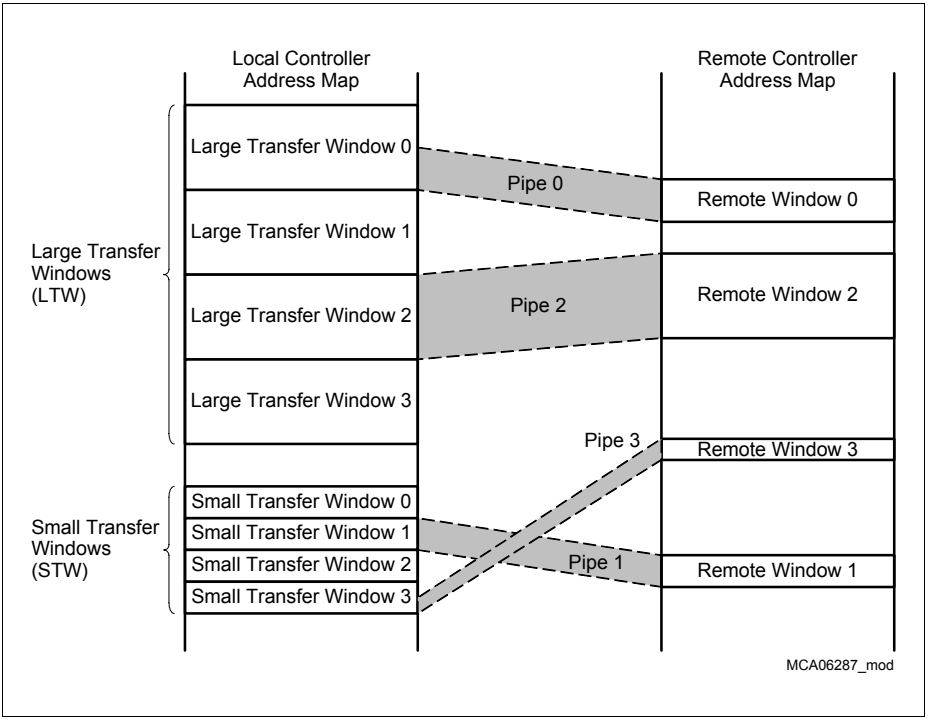


Figure 27-3 Transfer/Remote Window Assignment Example

During initialization of the pipes, base addresses and sizes of the Remote Windows are transmitted from the Local Controller to the Remote Controller. In the example of **Figure 27-3**, pipe 1 and pipe 2 cover the full range of their Transfer and Remote

Windows. The ranges of the Remote Windows of pipe 0 and pipe 3 are sub-ranges of the related Transfer Windows.

The location of a Transfer Window (base address and size) in the Local Controller is always fixed in a specific product device. Remote windows can be freely moved and located within the address space of the receiving controller. They are used to overlay address ranges of peripheral modules or internal memories.

Remote Window Address Generation

Figure 27-4 shows the generation of the Remote Window address ranges, with fixed base address part and additional variable address part. The variable address part is determined by the available address area for each Remote Window (also named buffer size, value of BSx = buffer size for Remote Window x indicates how many address bits are variable, defining the available address range).

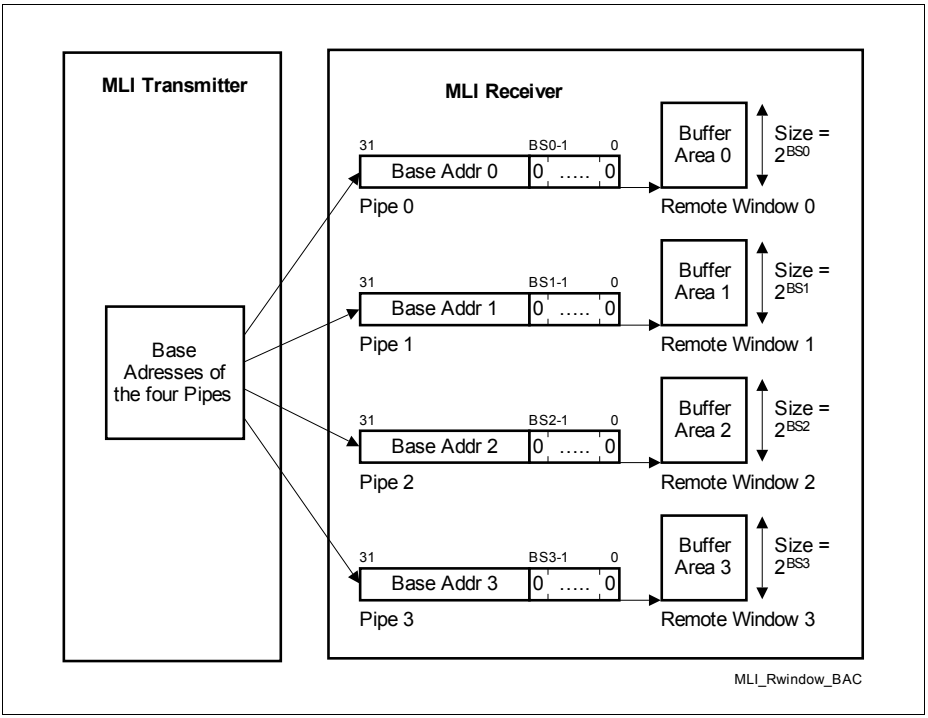


Figure 27-4 Base Address Definition of Remote Windows

Figure 27-5 shows the generation of the complete Remote Window address without address prediction. The variable address part can be transferred as offset by a write or a Read Frame, or it can be predicted in case of regular address modifications, whereas the fixed part of the address is defined by the upper bits of the base address.
In case of address prediction, the variable address part is internally calculated and taken as lower address bits of the target address (the upper address bits are given by the Remote Window's base address).

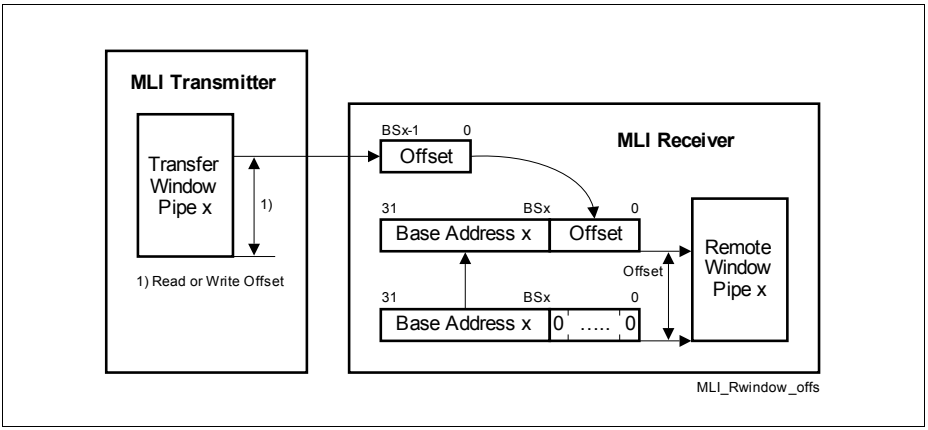


Figure 27-5 Remote Window Address Generation without Address Prediction

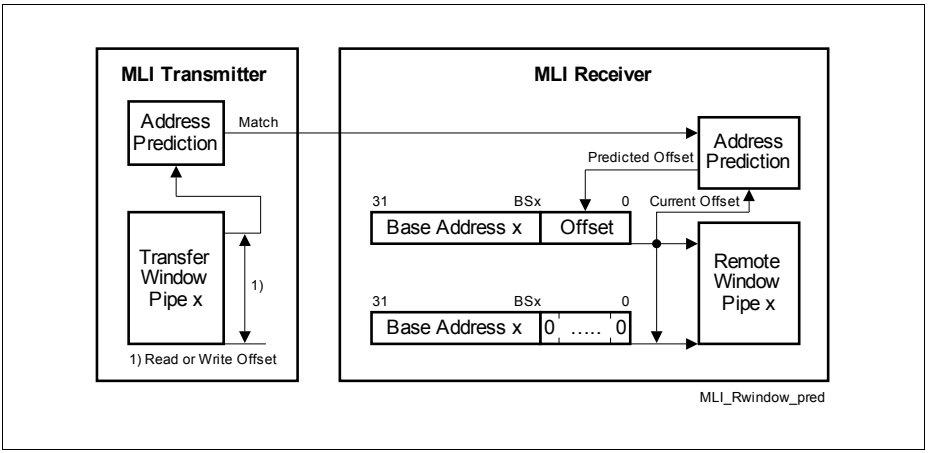


Figure 27-6 Remote Window Address Generation with Address Prediction

27.1.2 MLI Frame Structure

A frame is a message sent by an MLI transmitter to an MLI receiver. Depending on the desired behavior, different frame types exist:

- Copy Base Address Frame to define location and size of a Remote Window (see **Page 27-12**)
- Write Offset and Data Frame to transmit the write offset and the write data (see **Page 27-13**)
- Optimized Write Frame to transmit write data without write offset in case of an address prediction match (see **Page 27-14**)
- Discrete Read Frame to transmit read request with the read offset (see **Page 27-15**)
- Optimized Read Frame to transmit the read request without read offset in case of an address prediction match (see **Page 27-16**)
- Command Frame to transmit a command, e.g. setup information or MLI service request generation (see **Page 27-17**)
- Answer Frame to transmit the data previously requested by a Read Frame (see **Page 27-18**)

The local/remote structure of an MLI connection between two microcontrollers requires a transmitter unit and a receiver unit in both MLI modules (local and remote) for communication.

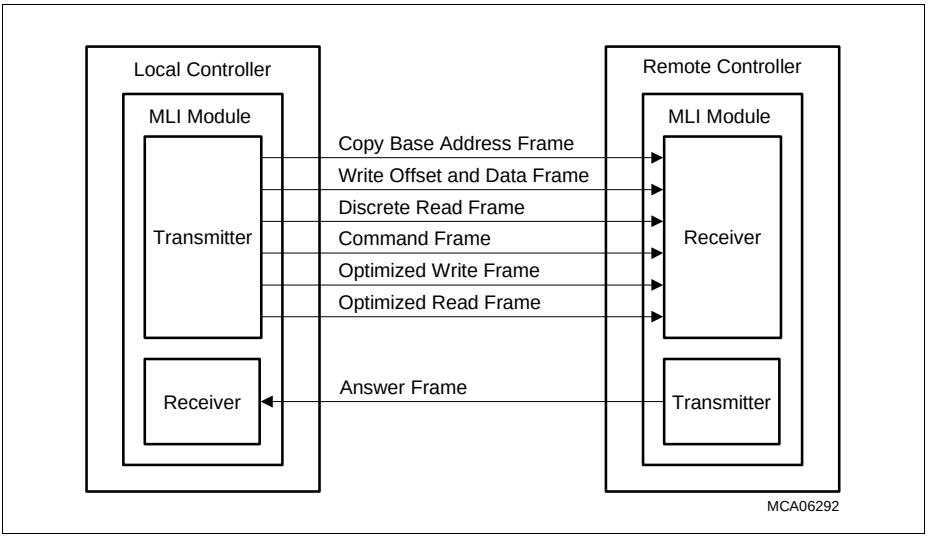


Figure 27-7 Logic Frame Assignment to Local/Remote Controller

27.1.2.1 General Frame Layout

The general layout of a frame is shown in **Figure 27-8**. It contains the following parts:

- A frame starts with a 4-bit header field that contains a 2-bit frame code (FC) and a 2-bit pipe number (PN).
- The data field can contain address, data, or control information. The width of the data field depends on the frame type.
- The frame is terminated by a parity bit (P) with even parity (see **Page 27-26**), calculated over header and data field bits.

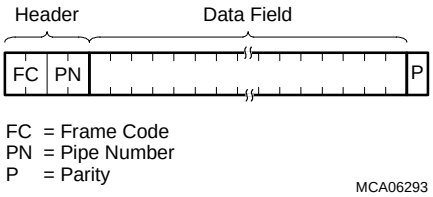


Figure 27-8 General Frame Layout

The frame code (FC) determines the frame type of the transmitted frame. The pipe number (PN) indicates the pipe that is related to the frame content (the value of PN is defined as 00_B for pipe 0, 01_B for pipe 1, 10_B for pipe 2, and 11_B for pipe 3).

The FC parameter is coded according to **Table 27-1**. If more than one frame type is defined with the same frame code value (see FC = 01_H, 10_H or 11_H), the width of the received frame defines the type. The value given by m in the table below represents the number of address bits transferred as offset (defined by the buffer size BSx of the Remote Window x).

Table 27-1 Frame Code Definition

Frame Code FC	Frame Type	Data Field Width [bits]	Description see
00_B	Copy Base Address Frame	32	**Page 27-12**
01_B	Write Offset and Data Frame	8+m, 16+m, or 32+m	**Page 27-13**
	Discrete Read Frame	2+m	**Page 27-15**
10_B	Command Frame	4	**Page 27-17**
	Answer Frame	8, 16, or 32	**Page 27-18**
11_B	Optimized Write Frame	8, 16, or 32	**Page 27-14**
	Optimized Read Frame	2	**Page 27-16**

27.1.2.2 Copy Base Address Frame

With a Copy Base Address Frame, the two parameters of a Remote Window are transferred from the transmitting controller to the receiving controller to initialize or to redirect the Remote Window.

The Copy Base Address Frame contains the following parts:

- Header:
  The header starts with frame code FC = 00_B followed by the pipe number PN of the pipe targeted by the transmitted base address bits and the size code.
- Remote Window address location:
  The 28 most significant bits of the 32-bit base address bits can be programmed by the transmitting controller (the 4 LSBs are considered as 0). The base address of a Remote Window has to be aligned to its size, e.g. a window of 1 Kbyte has to start at 1Kbyte address boundaries.
- Remote Window size:
  The size is defined by the 4-bit coded buffer size BS. The maximum size is 64 Kbytes.
- Parity bit P

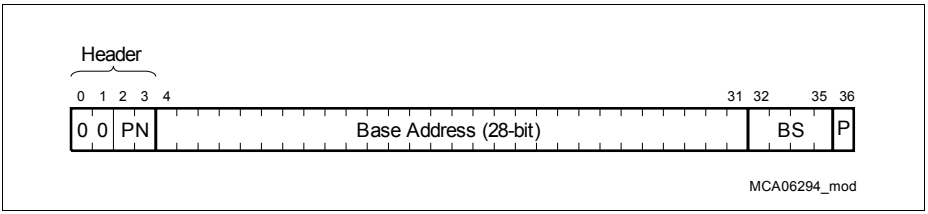


Figure 27-9 Copy Base Address Frame

Table 27-2 BS Coding

Buffer Size Code BS	Remote Window Size (also named Buffer Size)	Number m of Offset Bits
0000_B	2 bytes	m = 1
0001_B	4 bytes	m = 2
...	...	...
1110_B	32 Kbytes	m = 15
1111_B	64 Kbytes	m = 16

More details about the Copy Base Address Frame handling of the MLI module are described on **Page 27-28**.

27.1.2.3 Write Offset and Data Frame

A Write Offset and Data Frame is used by the transmitting controller to send an address offset and data to the receiving controller. This frame is initiated by a write operation to one of the Transfer Windows in the transmitting controller.

The Write Offset and Data Frame contains the following parts:

- Header:
  The header starts with frame code FC = 01_B followed by the pipe number PN of the Transfer Window that has been the target of the write operation.
- m-Bits of write offset:
  These bits define the write offset. The value of m depends on the size of the Remote Window, defined by the Copy Base Address Frame (m = 1-16).
- Write data field:
  The write data field can be 8-bit, 16-bit, or 32-bit wide, depending on the data width of the write access to the Transfer Window.
- Parity bit P

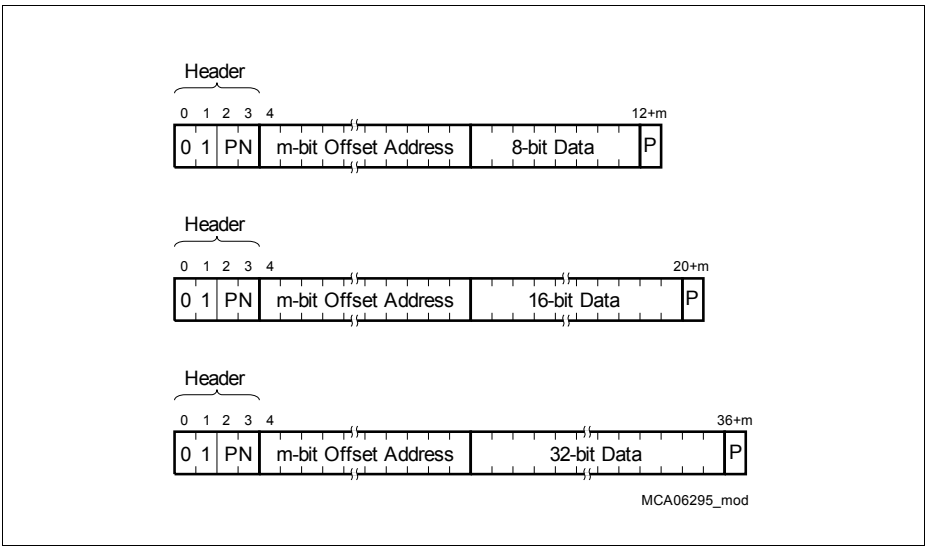


Figure 27-10 Write Offset and Data Frame

More details about the Write Offset and Data Frame handling of the MLI module are provided on **Page 27-30**.

27.1.2.4 Optimized Write Frame

An Optimized Write Frame is used by the transmitting controller to send 8-bit, 16-bit, or 32-bit wide data to the receiving controller. This frame is initiated by a write operation to one of the Transfer Windows in the transmitting controller. In contrast to a Write Offset and Data Frame, no write offset is transmitted because the offset address for the write data can be predicted and calculated by the receiving controller. An Optimized Write Frame allows a higher data bandwidth than Write Offset and Data Frames, because they are shorter. An optimized frame is only possible if the predicted address matches with the actually written one.

The Optimized Write Frame contains the following parts:

- Header:
  The header starts with frame code FC = 11_B followed by the pipe number PN of the Transfer Window that has been the target of the write operation.
- Write data field:
  The write data field can be 8-bit, 16-bit, or 32-bit wide, depending on the data width of the write access to the Transfer Window.
- Parity bit P

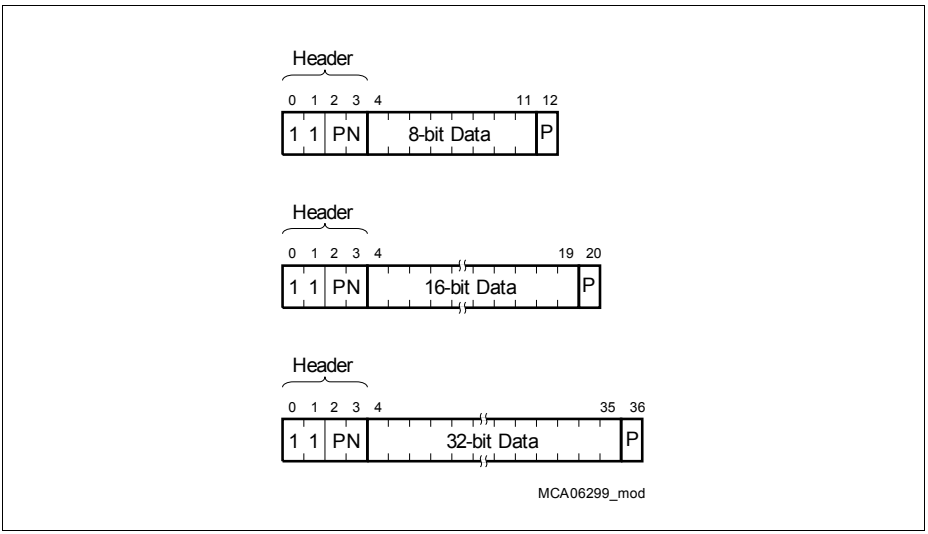


Figure 27-11 Optimized Write Frame

More details about the Optimized Write Frame handling of the MLI module are provided on **Page 27-30**.

27.1.2.5 Discrete Read Frame

A Discrete Read Frame is used by the Local Controller to request data to be read from the Remote Window in the Remote Controller. If the data is available, the Remote Controller typically responds to this request by sending an Answer Frame with the requested read data back to the Local Controller.

The Discrete Read Frame contains the following parts:

- Header:
  The header starts with frame code FC = 01_B followed by the pipe number PN of the Transfer Window that has been the target of the read operation.
- m-Bits of write offset:
  These bits define the read offset. The value of m depends on the size of the Remote Window, defined by the Copy Base Address Frame (m = 1-16).
- Data Width DW:
  The data width DW indicates if the read from the Transfer Window was a 8-bit, 16-bit, or 32-bit read action. It defines how many bytes have to be delivered to the Local Controller by the Answer Frame.
- Parity bit P

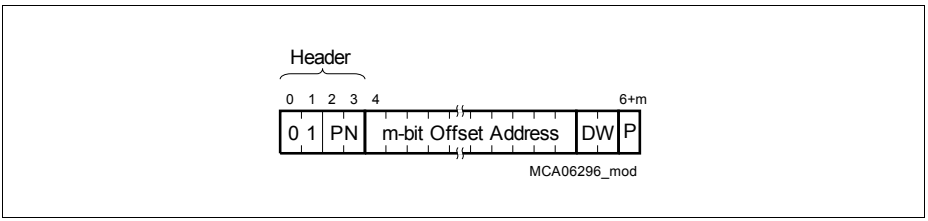


Figure 27-12 Discrete Read Frame

Table 27-3 Data Width DW Coding

Data Width DW	Number of Data Bits to be transferred
00_B	8-bit read access
01_B	16-bit read access
10_B	32-bit read access
11_B	reserved for future use

More details about the Discrete Read Frame handling of the MLI module are provided on **Page 27-34**.

27.1.2.6 Optimized Read Frame

An Optimized Read Frame is used by the Local Controller to request 8-bit, 16-bit, or 32-bit wide data from the Remote Controller without sending any offset address. The address for the requested data can be predicted and calculated by the MLI receiver of the Remote Controller.

The Optimized Read Frame contains the following parts:

- Header:
  The header starts with frame code FC = 11_B followed by the pipe number PN of the Transfer Window that has been the target of the read operation.
- Data Width DW:
  The data width DW indicates if the read from the Transfer Window was a 8-bit, 16-bit, or 32-bit read action. It defines how many bytes have to be delivered to the Local Controller by the Answer Frame. Same coding as for the Discrete Read Frame.
- Parity bit P

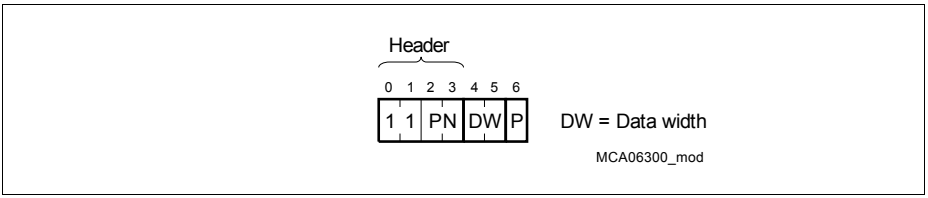


Figure 27-13 Optimized Read Frame

More details about the Optimized Read Frame handling of the MLI module are provided on **Page 27-30**.

27.1.2.7 Command Frame

The transmitting controller is able to initiate control actions to be executed by the receiving controller by sending a Command Frame.

The Command Frame contains the following parts:

- Header:
  The header starts with frame code FC = 10_B followed by the pipe number PN. The pipe number defines the type of command to be executed.
- Command Code CMD:
  Pipe number PN and a 4-bit CMD field are used for command coding. The command coding of some control actions is fixed, but free programmable software commands can also be defined (with PN = 11_B). The coding of the command bit field is pipe-specific and depends on the transmitted pipe number x.
- Parity bit P

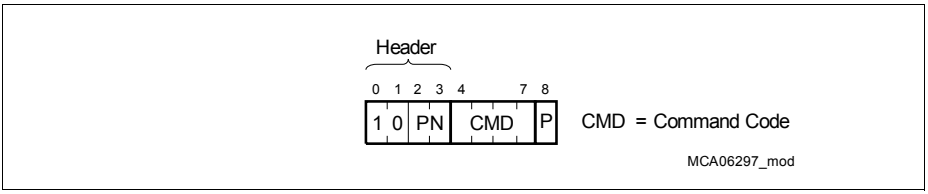


Figure 27-14 Command Frame

Table 27-4 PN for Command Coding

Pipe Number PN	Command Type
00_B	Activate MLI service request or other control signal(s) of the receiving controller. The definition which signal becomes activated is defined by CMD. The usage of these lines depends on the implementation.
01_B	Define delay for parity error indication in the receiving controller. The delay in RCLK cycles is defined by the value of CMD.
10_B	Control of internal functions of the receiving controller. The value of CMD indicates which function is controlled. The coding of CMD and the control mechanisms depend on the implementation.
11_B	Freely programmable software command.

More details about the Command Frame handling of the MLI module are provided on **Page 27-41**.

27.1.2.8 Answer Frame

An Answer Frame is used by the Remote Controller to send 8-bit, 16-bit, or 32-bit wide data to the Local Controller. The Answer Frame is the only frame that is transmitted within a logic Local/Remote Controller assignment from the Remote Controller to the Local Controller. It is the answer to a Discrete Read Frame or an Optimized Read Frame that has been sent by the Local Controller to request data from the Remote Controller.

The Answer Frame contains the following parts:

- Header:
  The header starts with frame code FC = 10_B followed by the pipe number PN. The value of PN is taken from the Read Frame that has triggered the Answer Frame.
- Read data field:
  The read data field can be 8-bit, 16-bit, or 32-bit wide, depending on the data width requested by the Read Frame that triggered the Answer Frame.
- Parity bit P

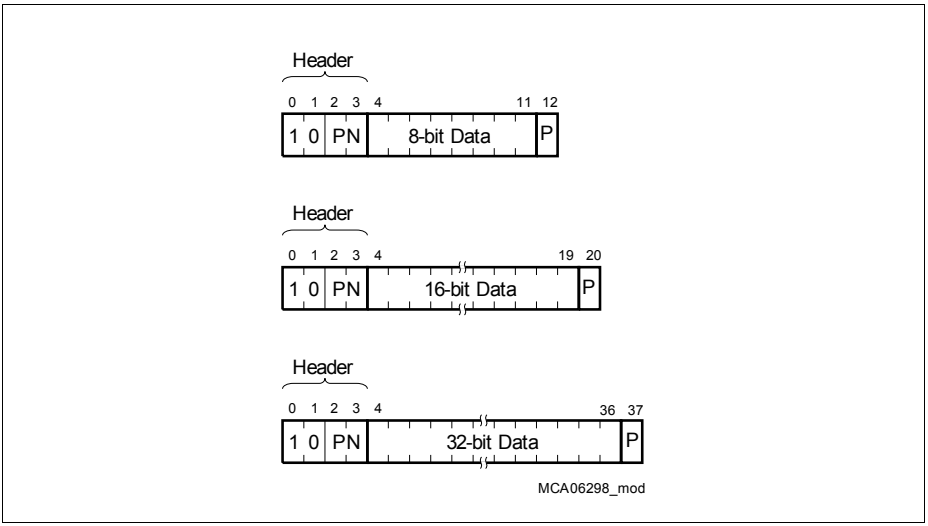


Figure 27-15 Answer Frame

More details about the Answer Frame handling of the MLI module are provided on **Page 27-39**.

27.1.3 Handshake Description

The description of the transmitter/receiver signal handshaking refers to an MLI connection between an MLI transmitter and an MLI receiver. MLI module transmitter I/O signals are indicated with prefix “T” and MLI receiver I/O signals are indicated with the prefix “R”. The 4-line MLI bus between a transmitter and a receiver outside the controllers uses signal names without any prefix.
In order to lay emphasis where a signal is generated or sampled, actions taken by the transmitter are described referring to signals with the prefix “T”, whereas receiver actions are referring to signals with the prefix “R”.

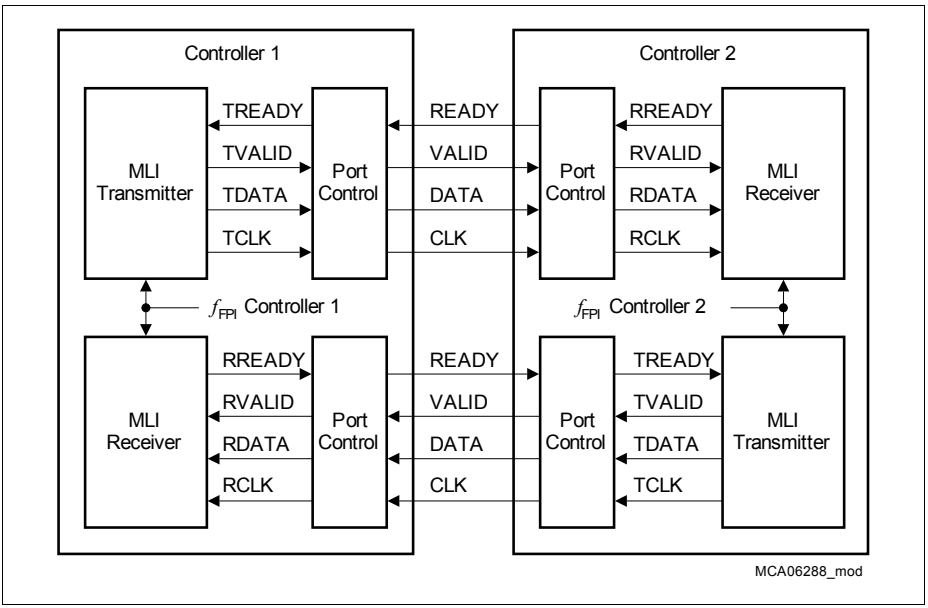


Figure 27-16 Transmitter/Receiver Signal Definitions

The MLI connection allows high data rates and, at the same time, supports significant signal propagation delays between the transmitter and the receiver. As shown in **Figure 27-16**, each output signal passes through the port stage, reaches the physical interface line between the MLI modules, enters via an input stage and can be finally evaluated. All these steps introduce an accumulating propagation delay. In standard synchronous serial connections (such as SPI), this delay limits the reachable baud rate to a few Mbit/s (closed-loop delay problem). In order to support higher baud rates than a standard SPI, the MLI protocol is based on a full handshake (READY-VALID) to deal with propagation delays in the range of some shift clock cycles and to avoid the closed-loop delay limitations of an SPI connection.

In a full handshake, each edge of the handshake signals has a defined meaning and the sequence of edges is clearly specified.
As a result, the propagation delays do not directly limit the MLI baud rate. Therefore, the points in time when a signal is generated, when it is visible on the physical interface line, or when it is evaluated have to be considered independently. This is done by defining 3 different names for a signal, referring to the 3 significant locations:

- The place where it is generated, also in relation to the generation clock edge
- The physical interface line where it can be observed
- The place where it is evaluated, also in relation to the evaluation clock edge

If a Local Controller should be connected to more than one Remote Controller, the transmitter signals CLK and DATA can be used as broadcast signals (parallel connection to the Remote Controllers), whereas the handshake signals VALID and READY have to be established as independent signal pairs for each device. As a result, a Local Controller only needs one CLK and one DATA output, but an individual set of READY and VALID handshake signals for each Remote Controller. Please note that Read Frames and Answer Frames are based on an established connection between a Local and a Remote Controller (because the Answer Frame is the only frame sent back to the Local Controller). Therefore, switching between several Remote Controllers can only be done while no read request is pending in the Local Controller. If no Read Frames are used by the Local Controller, frames can be sent out in parallel to all Remote Controllers if their READY signals are all respected.
If a Remote Controller should be connected to several Local Controllers, it may have several DATA and CLK inputs in addition to the READY-VALID signal sets. Please note that an active switching of a Remote Controller between several Local Controllers requires that all Local Controllers have the information which connection is active.
In any case, switching between Local and Remote Controllers is not allowed while frame transmission is in progress.

27.1.3.1 Handshake Signals

The synchronous serial frame transfer from an MLI transmitter to an MLI receiver is based on the following 4 signals (the MLI protocol only defines the signal transitions, but neither the signaling level nor the driver characteristics):

- Shift clock CLK:
  This signal is used as serial shift clock that is generated by the transmitter during the complete frame transfer (TVALID is active) and until the end of ready delay time. Signal TCLK can also be generated while no frame is transferred. In this case, the receiving controller can use the incoming RCLK receiver signal as base for its internal clock generation.
  The transmitter signals are always referring to the rising edge of TCLK, so TREADY is sampled and the output signals TDATA and TVALID are changing with the rising edge of TCLK.
  The MLI receiver actions refer to the falling edges of its RCLK input. The receiver samples the RVALID and RDATA signals and outputs its RREADY line with the falling edges of RCLK.
- Shift data DATA:
  This signal represents the transmit data TDATA transferred from the MLI transmitter to the MLI receiver input RDATA. Changes on transmitter side take place with rising edges of TCLK, whereas sampling on the receiver side takes place with falling edges of RCLK.
- Transmitter valid handshake VALID:
  This signal indicates the start and the end of each frame. It is active (1-level) during a frame transmission and passive (0-level) while no frame is transferred. Changes of TVALID on transmitter side take place with rising edges of TCLK, whereas sampling of RVALID on the receiver side takes place with falling edges of RCLK.
  An activation of TVALID to start a new frame can only take place if TREADY is 1.
- Receiver ready handshake READY:
  This signal indicates that the receiver is ready for a data transfer. Additionally, this line is used to indicate reception errors (parity error indication). Changes of RREADY on receiver side take place with falling edges of RCLK, whereas sampling of TREADY on the transmitter side takes place with rising edges of TCLK.

27.1.3.2 Error-free Handshake

A transmission can be started by an MLI transmitter when the MLI receiver is ready to receive data indicated by RREADY = 1 by the receiver. When the MLI transmitter detects TREADY = 1 and starts its transmission, TVALID is asserted to 1 level while a frame transfer is in progress. When the MLI receiver has detected the 0-to-1 transition of the RVALID signal it will de-assert RREADY back to 0 (transmission start acknowledged by receiver). At the end of the frame transmission, the MLI transmitter also de-asserts signal TVALID back to 0 and checks if the TREADY signal is at 0 level,

too. This check is used as life-sign of the receiver and the MLI transmitter can detect whether the receiver is able to react in-time to the transmitter actions (see also Page 27-23).

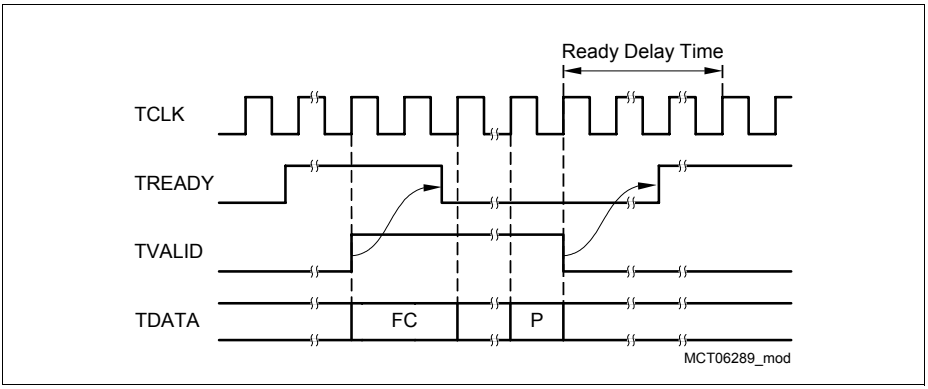


Figure 27-17 MLI Handshake without Error Indication

27.1.3.3 Ready Delay Time

In order to support significant propagation delays, the handshake signal TREADY is evaluated with respect to TVALID and TCLK in an time interval called Ready Delay Time after the end of the frame (see **Figure 27-17**). The length of the Ready Delay Time is programmable, defining the size of the time interval.

When a transmission is finished (RVALID becomes 0), the MLI receiver checks the received frame for correct reception (parity error). If no parity error has been detected, the MLI receiver asserts its RREADY signal again to 1 to indicate the correct reception with the next falling edge of RCLK. The MLI transmitter checks its TREADY input with each rising edge of TCLK after TVALID has become 0 and increments a counter. This counter is started from 0 at the end of a frame transmission (TVALID becomes 0) and counts TCLK periods (Ready Delay Time Counter). If the condition TREADY = 1 is detected before the programmed Ready Delay Time has elapsed, the MLI receiver has indicated a frame reception without parity error to the MLI transmitter. In this case, a new frame transmission can be started. The transfer handshake signalling without a parity error indication is shown in **Figure 27-17**.

Figure 27-18 shows the transfer handshake if a parity error condition has been detected by the MLI receiver and indicated to the MLI transmitter. In this case, the receiver waits a programmable number of RCLK clock cycles before setting RREADY to 1. If the TREADY = 1 condition is detected by the transmitter after the ready delay has elapsed, a parity error has been indicated by the MLI receiver. In this case, it is assumed that the MLI receiver has detected a frame with a parity error and has discarded the frame. The

transmitter automatically sends the last frame again after a parity error indication. Optionally, this MLI event can activate a service request output.

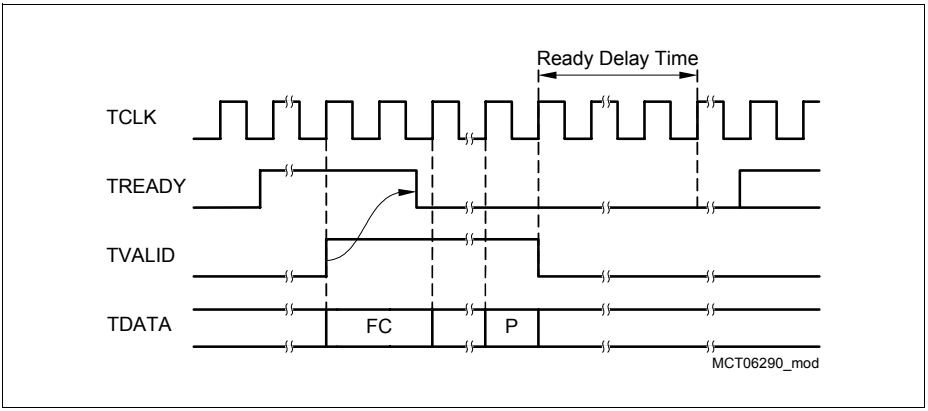


Figure 27-18 MLI Handshake with Parity Error Indication

27.1.3.4 Non-Acknowledge Error

A transmitter of an MLI module is able to detect an inoperable receiver by analyzing the handshake signal TREADY. After TVALID has been asserted to 1, the transmitter checks the receiver's acknowledge (TREADY becoming 0). A Non-Acknowledge error condition is detected by the transmitter when at the end of a frame transmission the TREADY signal is still at high level (TREADY = 1 when TVALID becomes 0). **Figure 27-19** shows the Non-Acknowledge error case. In this case, the transmitter automatically sends the last frame again. Optionally, this MLI event can activate a service request output.

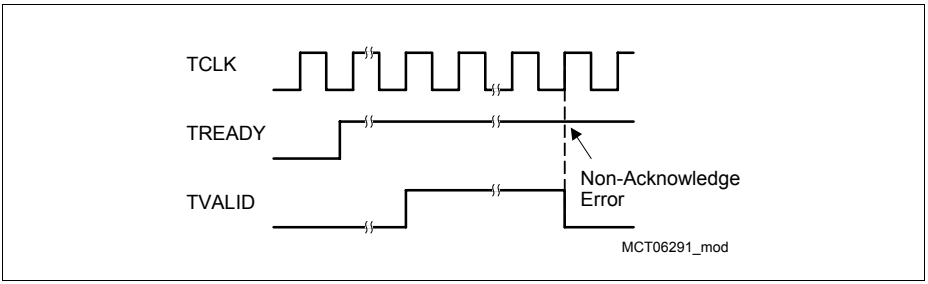


Figure 27-19 Non-Acknowledge Error

27.1.3.5 Signal Timing

Figure 27-20 shows the MLI timing requirements.

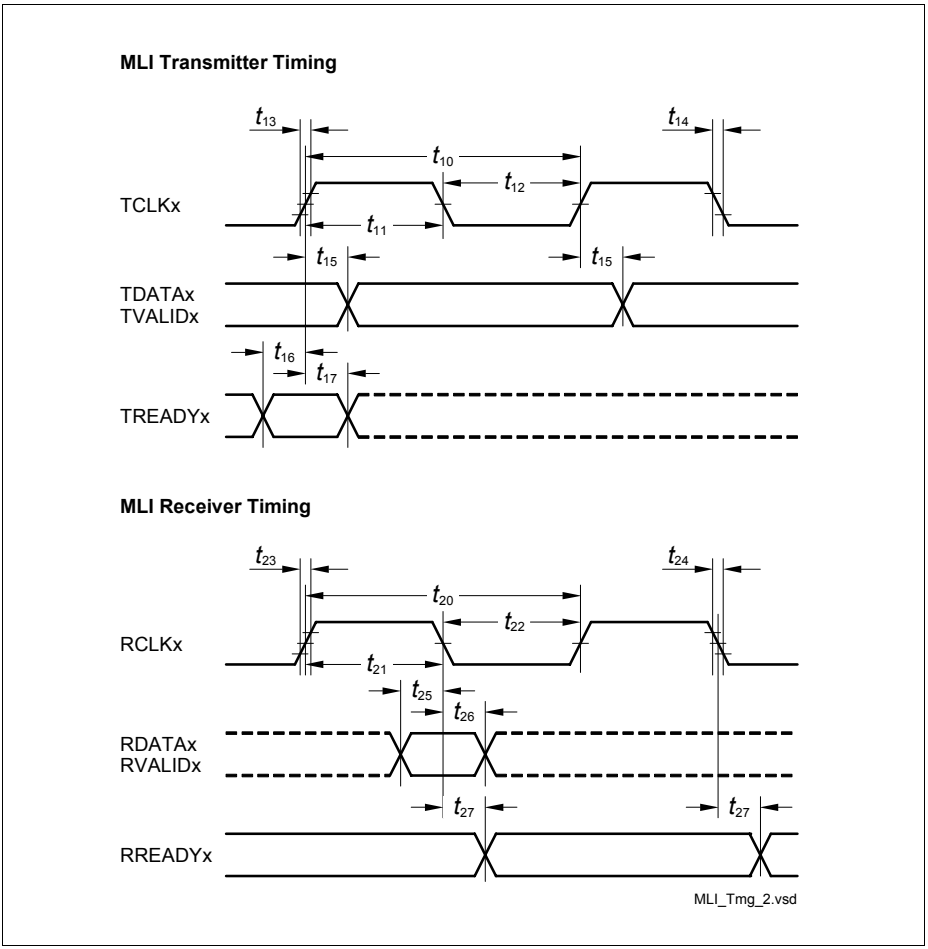


Figure 27-20 Signal Timing

The transmitter output signals TDATA and TVALIDx might have a certain delay to the transmitter clock output TCLK due to on-chip variation of the driver stages and differences in the propagation delays. The transmitter TREADY input can change at any point in time compared to TCLK. In order to ensure stability, it is internally synchronized to f_{MLI} of the transmitter before being evaluated with the rising TCLK edge when TVALID becomes 0. For the calculation of the signal propagation time, these 2 clock cycles have to be taken into account.

The transmitter input TREADYx has to be stable a certain time before TVALID becomes low, referring to the rising edge of TCLK when TVALID becomes low. If at this point in time, TREADYx is detected at a high level, a Non-Acknowledge error is signaled. The same timing relation has to be considered at the end of the ready delay time for the parity error detection.

The receiver input signals are handled asynchronously based on the RCLK signal. The synchronization to the receiver's system clock f_{FPI} is done in the receiver logic. The input signals RDATA and RVALID have to respect a certain setup and hold time at the falling edge of RCLK.

27.1.4 Parity Generation

For parity generation, the number of transmitted bits with the value of 1 is counted over the header and the complete data field of a frame. For even parity, the parity bit is set if the result of a modulo-2 division of the elaborated number is 1. For error-free MLI traffic, even parity generation and checking is defined.

More details about the parity handling of the MLI module are provided on **Page 27-44**.

27.1.5 Address Prediction

An address prediction method can be enabled to support communication between MLI transmitter and MLI receiver without sending address offset information in the frames. This feature reduces the required bandwidth for MLI communication. Both of the communication partners, MLI transmitter and receiver are able to detect regular offset differences of consecutive window accesses to the same window. The address prediction mechanism working independently for each pipe, different prediction values can be handled in parallel for the different pipes.

The MLI transmitter can compare the offset of each Transfer Window read or write access with the offset of the previous access to the same Transfer Window. Between the accesses to a specific window, other windows can be accessed without disturbing the prediction. Bigger offset differences than 512 bytes are not supported by the address prediction.

If the offset differences are identical in at least two accesses to the same Transfer Window, an address prediction is possible and Optimized Write Frames or Optimized Read Frames can be sent to the receiving controller for this pipe. If the offset difference of a next access to this Transfer Window does not match the former ones (predicted offset), address prediction is not possible. In this case, a Normal Frame for writing or reading (Write Offset and Data Frame or Discrete Read Frame) is started.
The identical address prediction mechanism is built in the receiver. As a result, the receiver can elaborate the original offset value in the transmitter when receiving an optimized frame for any pipe.

More details about the address prediction mechanism of the MLI module are provided on **Page 27-47**.

27.2 Module Kernel Description

This chapter describes how the MLI protocol is implemented in the MLI module and how frame handling can be done by software, comprising:

- The frame handling (see **Page 27-27**)
- The general MLI features (see **Page 27-44**)
- The interface signals (see **Page 27-51**)
- The general MLI service request structure (see **Page 27-57**)
- The MLI transmitter events (see **Page 27-59**)
- The MLI receiver events (see **Page 27-62**)
- The baud rate generation (see **Page 27-67**)

27.2.1 Frame Handling

The frame handling is based on receiver and transmitter registers and the Transfer Windows. Depending on the type of access to the Transfer Windows, different actions take place inside the MLI module. Please refer to the following pages for the handling of:

- Copy Base Address Frame (see **Page 27-28**)
- Data Frames (see **Page 27-30**)
- Read Frames (see **Page 27-34**)
- Answer Frame (see **Page 27-39**)
- Command Frame (see **Page 27-41**)

27.2.1.1 Copy Base Address Frame

A Copy Base Address Frame defines the location and the size of a Remote Window.

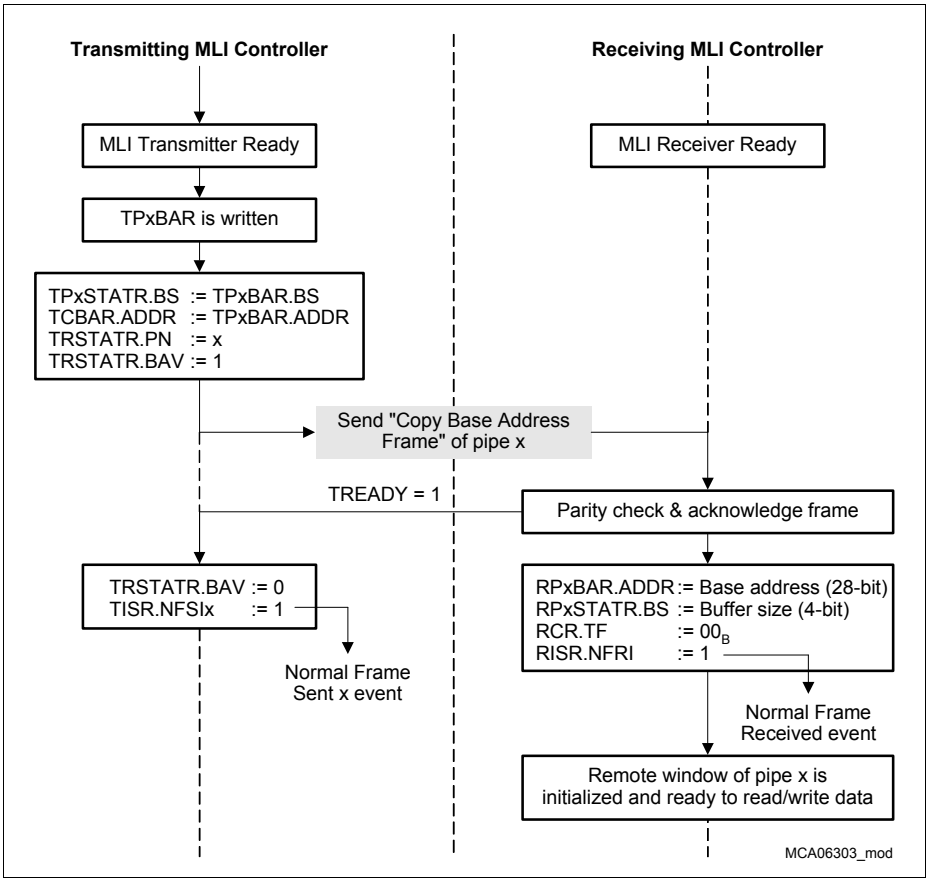


Figure 27-21 Copy Base Address Frame Flow

Transmitting Controller

The transmission of a Copy Base Address Frame is started after a transmitter pipe x base address registers TPxBAR has been written, triggering the following actions for pipe x.

- Bit field TPxBAR.BS (4-bit coded buffer size) is loaded into bit field TPxSTATR.BS
- Bit field TPxBAR.ADDR (28 most significant base address bits) is loaded into bit field TCBAR.ADDR.

- Status bit field TRSTATR.PN is updated with the pipe number x (for example x = 2 when TP2BAR has been written).
- Status flag TRSTATR.BAV (base address valid) becomes set.
- The transmission of a Copy Base Address Frame with the two buffered parameters TCBAR.ADDR and TPxSTATR.BS is started for pipe x (if the corresponding pipe is idle and TREADY = 1).
- Status flag TRSTATR.BAV (in the transmitting controller) is cleared after the Copy Base Address Frame has been finished and correctly acknowledged by the MLI receiver of the receiving controller.
- MLI event status flag TISR.NFSIx (Normal Frame Sent event in pipe x) is set and a service request output is activated if enabled by TIER.NFSIEx = 1.

Note: After the transfer of a Copy Base Address Frame the optimized mode will be suppressed automatically by hardware for the next two data frames. This ensures a correct offset prediction afterwards.

Receiving Controller

When a Copy Base Address Frame for pipe x has been received correctly and acknowledged, the following actions are executed in the MLI receiver.

- The received 28 most significant address bits are written into the receiver pipe x base address register bit field RPxBAR.ADDR. This bit field determines the base address of the pipe x Remote Window.
- The received 4-bit coded buffer size is stored in the receiver pipe x status register bit field RPxSTATR.BS. This bit field determines the number of variable address bits for the offset (determining the size) of the pipe x Remote Window.
- The information about the received frame type (= 00_B for Copy Base Address Frame) is written into the receiver control register bit field RCR.TF.
- MLI event status flag RISR.NFRI (Normal Frame Received event) is set and a service request output is activated if enabled by RIER.NFRIE = 01_B or 10_B.

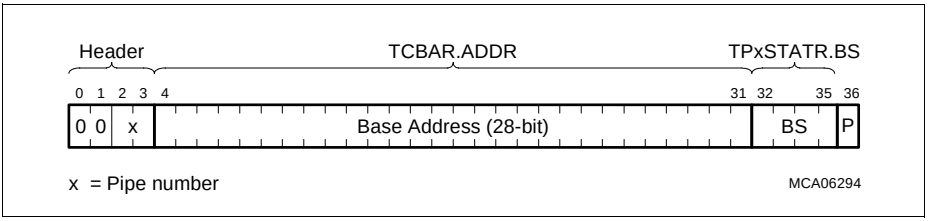


Figure 27-22 Copy Base Address Frame

27.2.1.2 Write/Data Frames

Write Frames (also named Data Frames) transmit the write data and optionally the write offset.

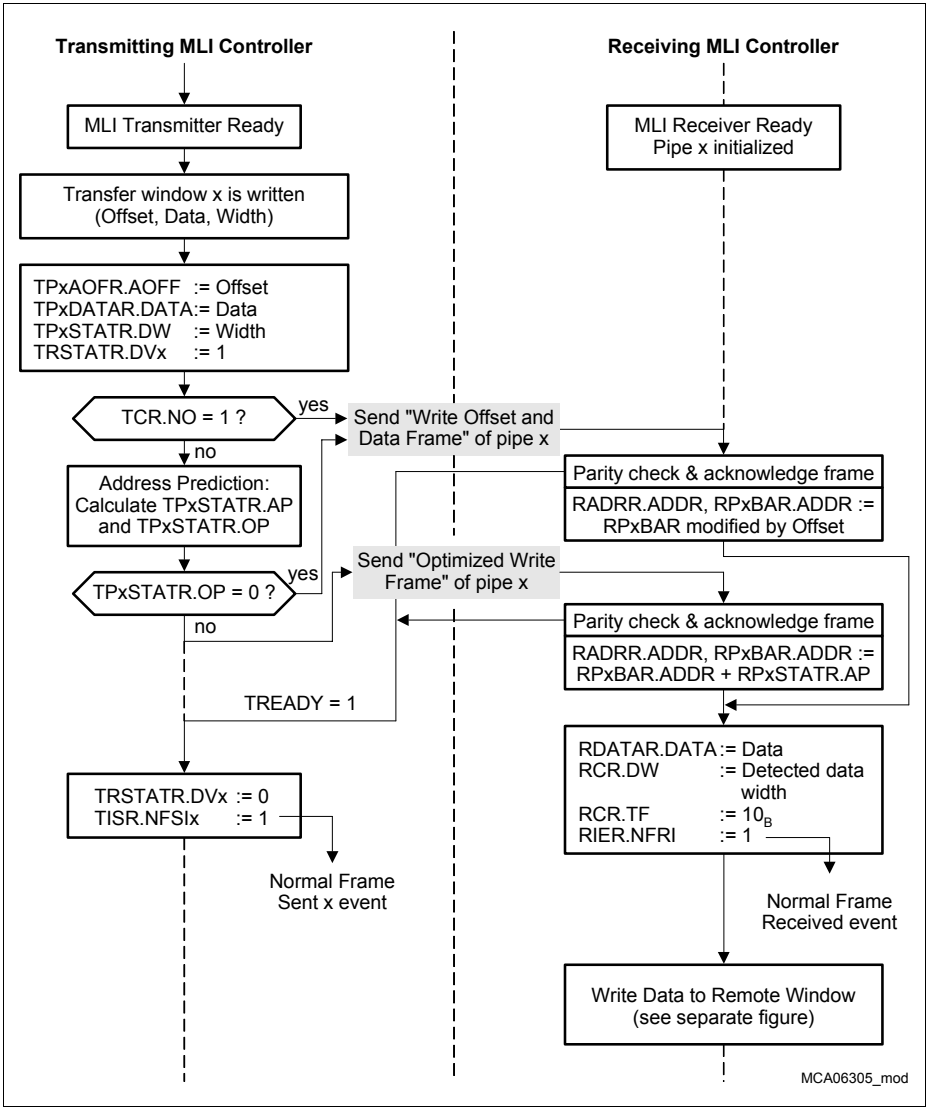


Figure 27-23 Write Frame Flow

Transmitting Controller

In the transmitting controller, a write operation to a location within a Transfer Window delivers the address, the data, and the data size to the transmitter and triggers the following actions in the MLI transmitter.

- The 16 least significant address bits of the Transfer Window write access are stored in TPxAOFR.AOFF as write offset address. In case of a an access to a Small Transfer Window, also 16 bits are stored, but the higher bits are not taken into account assuming the buffer size is configured correctly (see **Page 27-105**).
- The data of the write access to the Transfer Window is stored in TPxDATAR.DATA.
- The data width of the write access to the Transfer Window (8-bit, 16-bit, or 32-bit) is stored in bit field TPxSTATR.DW.
- Status flag TRSTATR.DVx (data valid) is set, indicating that the pipe contains valid data for transmission.
- If the address prediction method is disabled (TCR.NO = 1), the transmission of a Write Offset and Data Frame is started as soon as the MLI transmitter is idle, no higher priority frames are pending, and TREADY = 1.
  If the address prediction method is enabled (TCR.NO = 0), a Write Offset and Data Frame is started only if an address prediction is not possible (indicated by TPxSTATR.OP = 0). If TPxSTATR.OP = 1, an address prediction is possible in the MLI transmitter (and the MLI receiver) and an Optimized Write Frame can be started. The address prediction method used is described on **Page 27-47**.
- Status flag TRSTATR.DVx is cleared by hardware and MLI event status flag TISR.NFSIx (Normal Frame Sent event in pipe x) is set (and a service request output is activated if enabled by TIER.NFSIEx = 1) after the Write Frame has been finished and correctly acknowledged by the MLI receiver.

The number m of offset address bits that are transmitted at a Write Offset and Data Frame is determined by the size of the Remote Window in the receiving controller that has been previously initialized by the transmission of a Copy Base Address Frame. Parameter m is referring to bit field TPxSTATR.BS (and RPxSTATR.BS) and can be in the range of 1 to 16 bits.

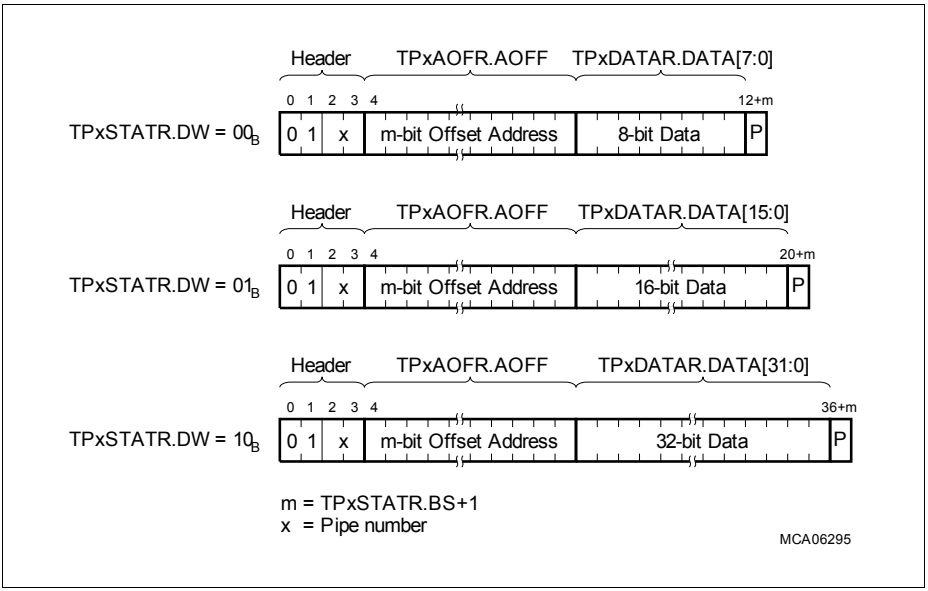


Figure 27-24 Write Offset and Data Frame

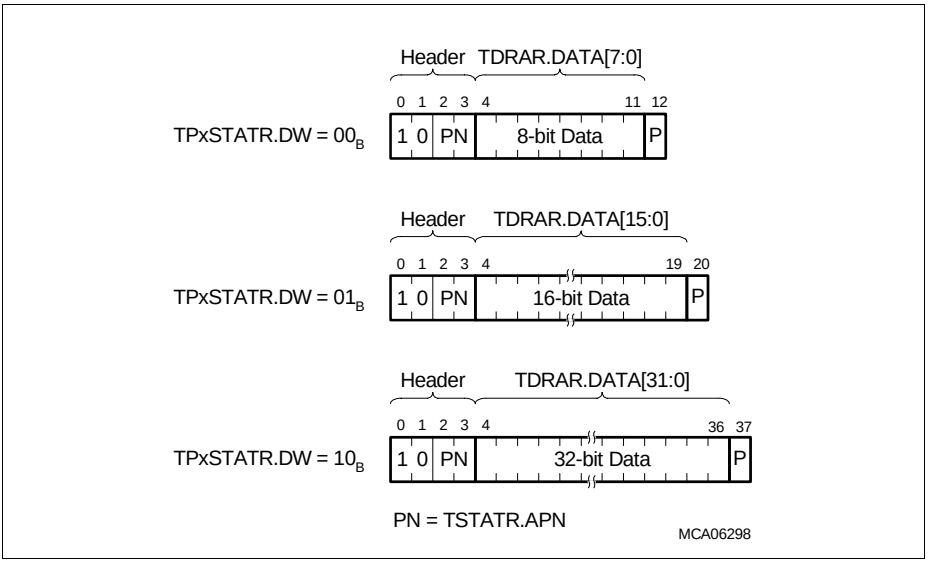


Figure 27-25 Optimized Write Frame

Receiving Controller

After a Write Frame has been received correctly and acknowledged, the following actions are automatically executed in the MLI receiver:

- In the case of a Write Offset and Data Frame:
  The result of the internal address prediction is not taken into account. The received offset address is added to the base address of the pipe x Remote Window and the result is stored in RPxBAR.ADDR. It is also stored in RADDR.ADDR and represents the destination address in the receiving controller where data should be written to.
  In the case of an Optimized Write Frame:
  The result of the internal address prediction is taken into account. The next address in the receiving controller where data should be written to is calculated by adding the detected receiver address prediction value RPxSTATR.AP to the actual address stored in RPxBAR.ADDR and the result is stored in RPxBAR.ADDR and in RADDR.ADDR.
- The received data is written into the receiver data register RDATAR (right aligned, unused bits are 0).
- The detected data width of the received data is written into bit field RCR.DW.
- The information about the received frame type (= 10_B for a Write Frame) is written into bit field RCR.TF.
- MLI event status flag RISR.NFRI (Normal Frame Received event) is set and an SR output line is activated if enabled by RIER.NFRIE = 01_B or 10_B.

After these actions related to the reception of a Write Frame by the receiving controller, the data that has been received from the transmitting controller is ready to be written into the Remote Window related to the receiving pipe.
This write operation can be executed in two ways:

- RCR.MOD = 0: Automatic Data Mode is disabled.
  In this mode, a bus master of the receiving controller, typically a CPU, is informed by a Normal Frame received event RISR.NFRI (a service request output is activated if RIER.NFRIE = 10_B) to transfer the received write data from the MLI receiver to the Remote Window. Therefore, it must read the data from RDATAR, together with width RCR.DW and the address stored in RADRR and write it to the indicated address location.
- RCR.MOD = 1: Automatic Data Mode is enabled.
  In this mode, the MLI module automatically writes the received write data to the Remote Window. This automatic action is controlled by a move engine block in the MLI receiver. It also sets event status flag RISR.MEI (move engine event when the access is terminated). A service request output is activated if enabled by RIER.MEIE = 1.
  The write operation to the Remote Window is executed only if the write address is within an enabled access protection range. If the address range is disabled for the write address, the automatic write action does not take place and event status flag RISR.MPEI (memory protection error) is set and a service request output is activated

if enabled by RIER.MPEIE = 1. In this case, the receiving controller software can analyze the values in RDATAR, together with width RCR.DW and the address stored in RADRR.

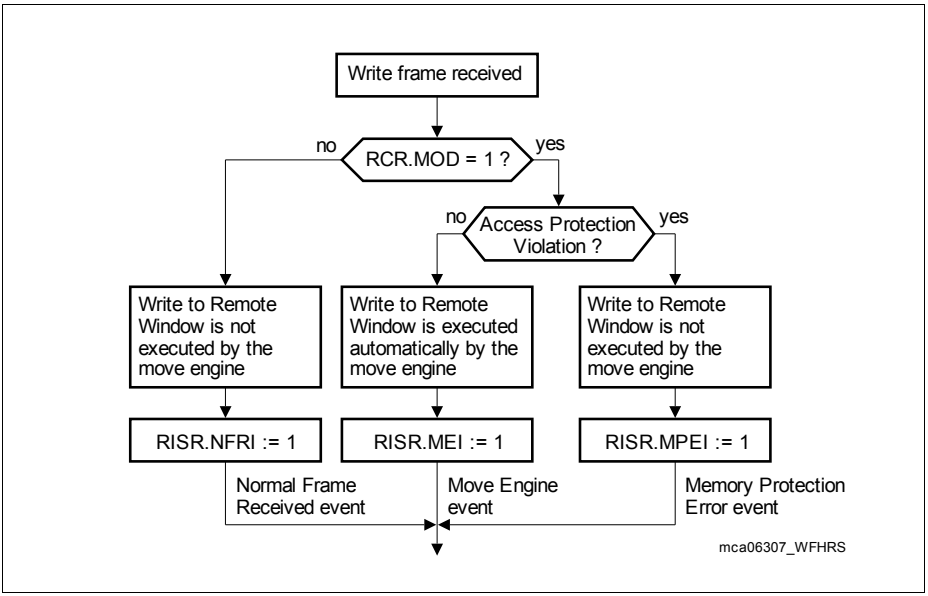


Figure 27-26 Write Frame Handling on Receiving Side

Note: In Automatic Data Mode, Write Frames are leading to a write action executed by the MLI move engine. During the move engine operation, only one more MLI frame can be received (stored in a waiting position to be executed). Then the reception of more frames is blocked by Non-Acknowledge handshake. If the move engine operation is finished, frame execution and reception continue normally.
If Automatic Data Mode is disabled, no blocking mechanism has been implemented. The receiving controller software has to take care to deal with the received data before it is overwritten by new incoming frames.

27.2.1.3 Read Frames

Read Frames transmit read request and optionally the read offset from the Local Controller to the Remote Controller.

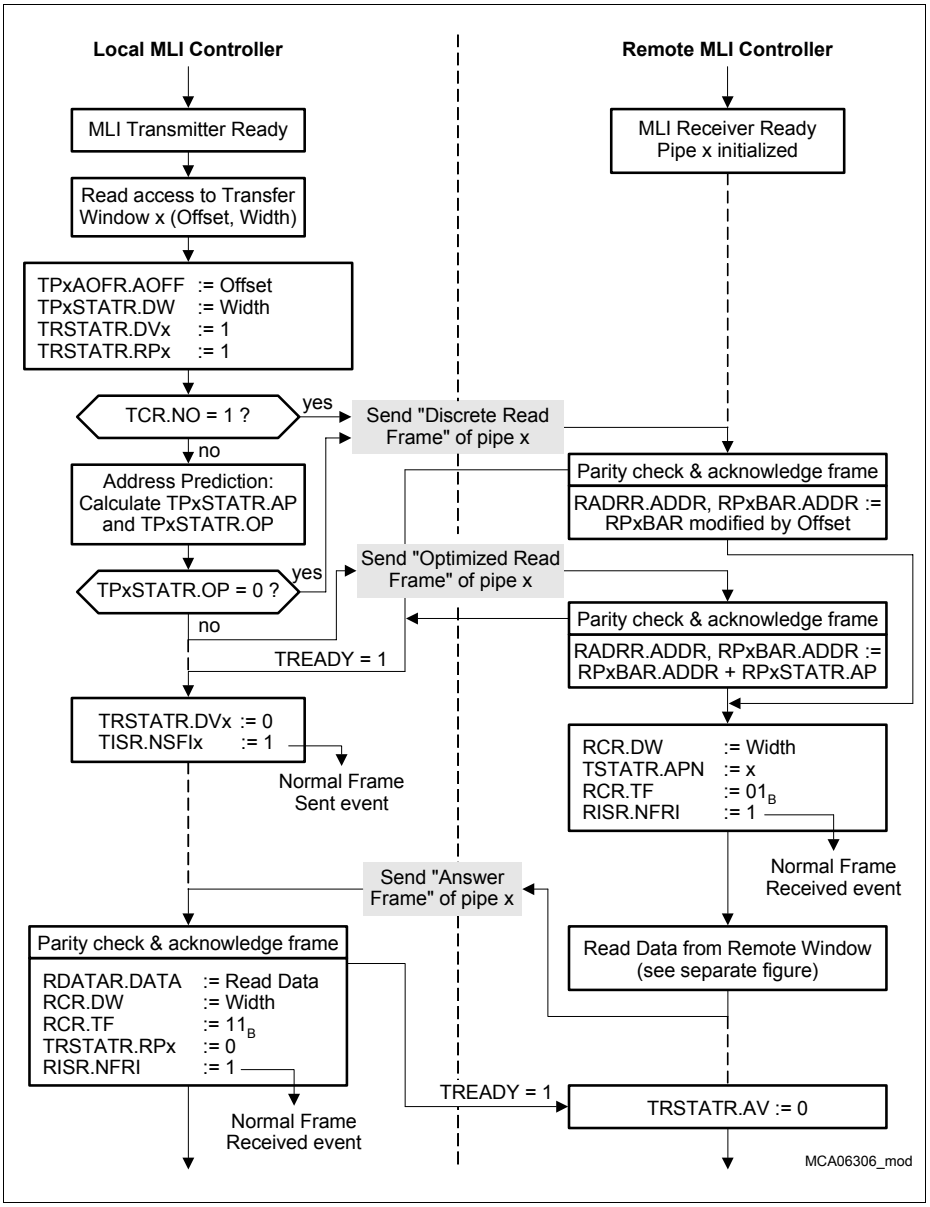


Figure 27-27 Read Frame and Answer Frame Flow

Local Controller

A read operation from a location within a Transfer Window x of the Local Controller delivers a dummy value as result of the read action and triggers the transmission of a Read Frame. The dummy value of the initial read action should be ignored and the software has to wait for the reception of the Answer Frame to get the desired data.

- The 16 least significant address bits of the Transfer Window read access are stored in TPxAOFR.AOFF as read offset address. In case of a an access to a Small Transfer Window, also 16 bits are stored, but the higher bits are not taken into account assuming the buffer size is configured correctly (see **Page 27-105**).
- The data width of the Transfer Window read access (8-bit, 16-bit, or 32-bit) is stored in bit field TPxSTATR.DW.
- Status flag TRSTATR.DVx (data valid) is set.
- Status flag TRSTATR.RPx (read pending) is set. This bit is cleared by hardware when an Answer Frame has been received correctly.
- If the address prediction method is not enabled (TCR.NO = 1), transmission of a Discrete Read Frame is started. If the address prediction method is enabled (TCR.NO = 0), a Discrete Read Frame is started only if an address prediction is not possible (indicated by TPxSTATR.OP = 0). If TPxSTATR.OP = 1, an address prediction is possible and an Optimized Read Frame is started.
- Status flag TRSTATR.DVx is cleared by hardware and MLI event status flag TISR.NFSIx (Normal Frame Sent event in pipe x) is set (and a service request output is activated if enabled by TIER.NFSIEx = 1) after the Read Frame has been finished and correctly acknowledged by the MLI receiver of the Remote Controller.

The number m of offset address bits that are transmitted at a Discrete Read Frame is determined by the (coded) size of the Remote Window in the Remote Controller that has been previously initialized by the transmission of a Copy Base Address Frame. Parameter m is stored in bit field TPxSTATR.BS (and RPxSTATR.BS) and can be in the range of 1 to 16 bits.

After a completed transmission of a Read Frame, the Local Controller expects the reception of an Answer Frame. The Answer Frame is introduced with the highest priority into the data flow of the transmitter of the Remote Controller.

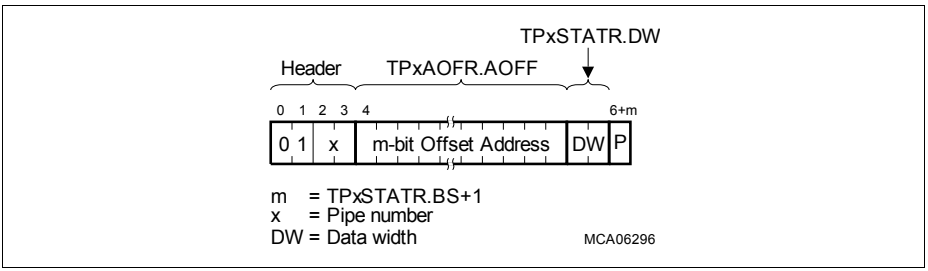


Figure 27-28 Discrete Read Frame

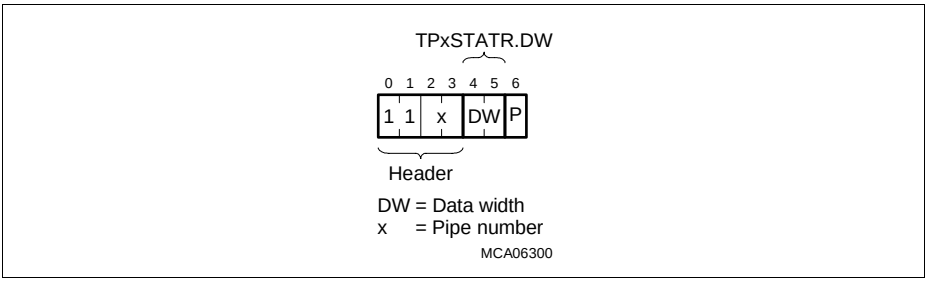


Figure 27-29 Optimized Read Frame

Remote Controller

After a Read Frame has been correctly received and acknowledged, the following actions are executed in the MLI receiver of the Remote Controller:

- In the case of a Discrete Read Frame:
  The result of the address prediction is not taken into account. The received offset address is added to the base address of the pipe x Transfer Window (stored in RPxBAR.ADDR). The result of this addition is stored in RADRR.ADDR and also in RPxBAR.ADDR and represents the destination address in the Remote Controller from where data should be read.
  In the case of an Optimized Read Frame:
  The result of the address prediction is taken into account. The next address in the Remote Controller where data should be read is calculated by adding the detected receiver address prediction value RPxSTATR.AP to the actual address stored in RPxBAR.ADDR. The result of this addition is stored in RADRR.ADDR and also in RPxBAR.ADDR and represents the destination address in the Remote Controller from where data should be read.
- The transmitted data width DW is written into bit field RCR.DW.
- The information about the received frame type (= 01_B for a Read Frame) is written into bit field RCR.TF.
- MLI event status flag RISR.NFRI (Normal Frame Received event) is set and a service request output is activated if enabled by RIER.NFRIE = 01_B or 10_B.

After correct reception of a Read Frame by the Remote Controller, the data requested by the Local Controller can be read by the Remote Controller and sent back to the Local Controller in form of an Answer Frame.

This read operation can be executed in two ways:

- RCR.MOD = 0:
  Automatic Data Mode is disabled. In this mode, a bus master of the Remote Controller, typically a CPU, is informed by a Normal Frame received event to read the requested read data and transfer it to the MLI receiver. Therefore, it must read data

with width RCR.DW from the address stored in RADRR and write the data into TDRAR.DATA.

- RCR.MOD = 1:
  Automatic Data Mode is enabled. In this mode, the move engine of the MLI automatically reads data from the Remote Window and sets event status flag RISR.MEI (move engine access terminated). A service request output is activated if enabled by RIER.MEIE = 1.
  The read operation from the Remote Window is executed only if the read address is within an enabled access protection range. If no address range is enabled for the actual read address, the automatic read action is not executed by the move engine, event status flag RISR.MPEI (memory protection error) is set and a service request output is activated if enabled by RIER.MPEIE = 1. In the interrupt handler routine, a bus master (e.g. CPU or PCP) must then take care of the remote window read operation and the data transfer to TDRAR.
- After TDRAR.DATA has been updated, status flag TRSTATR.AV of the Remote Controller is set and the transmission of an Answer Frame is started.

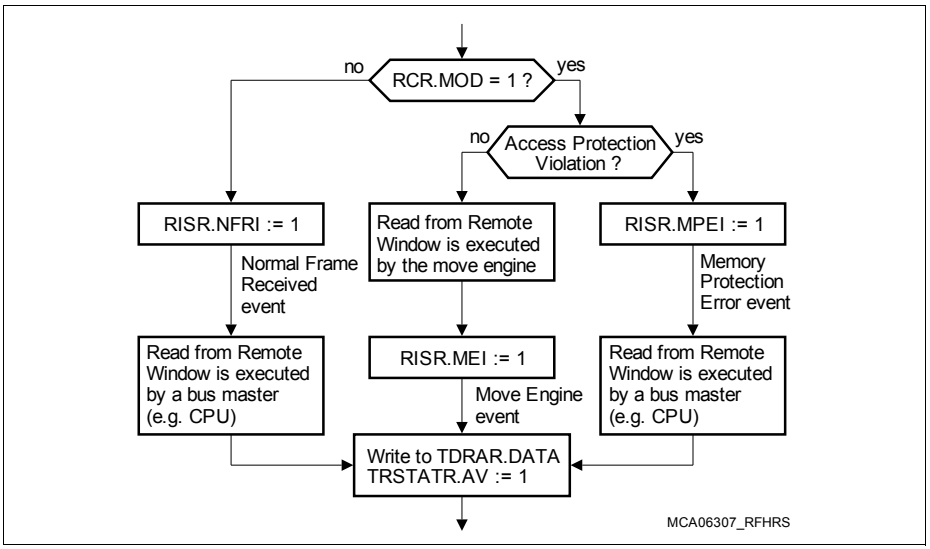


Figure 27-30 Read Frame Handling on Remote Side

Note: In Automatic Data Mode, Read Frames are leading to a read action executed by the MLI move engine. During the move engine operation, only one more MLI frame can be received (stored in a waiting position to be executed). Then the reception of more frames is blocked by a Non-Acknowledge handshake. If the move engine operation is finished, frame execution and reception can continue normally. If Automatic Data Mode is disabled, no blocking mechanism has been

implemented. The Remote Controller software has to take care to read the received data.

27.2.1.4 Answer Frame

Please note that only one Answer Frame can be handled by the system at a time (no Read Frame request while any TRSTATR.RPx is set). Make sure that not more than one Read Frame is pending at a time. If a Read Frame is not answered by an Answer Frame during a certain time interval, a time-out criterion should be handled in software. The Remote Controller has to take care that no Answer Frame is delivered after the time-out criterion has been detected (e.g. by a software-triggered Command Frame). Do not start a new Read Frame while waiting for an Answer Frame if the time-out criterion has not yet been detected and the Answer Frame has not yet been received. The length of the time-out interval depends on the application and has to be defined accordingly on a case by case base (e.g. the transfer rates between MLI modules, bus architecture, etc. have to be considered). In the case a time-out has been detected, the Local Controller software has to clear the TRSTATR.RPx bit by writing 1 to SCR.CDVx and can start a new Read Frame.

Remote Controller (Receiving the read request)

The Answer Frame is the only frame sent from the Remote Controller back to the Local Controller. The transmitter registers of the Remote Controller are used to generate the Answer Frame.

Every time the transmitter data read answer register TDRAR is written in the Remote Controller, the transmission of an Answer Frame is started and the following actions are triggered.

- Status flag TRSTATR.AV is set to trigger the transmission of an Answer Frame.

The following parameter is transmitted in the data field of the Answer Frame:

- Read data: stored in TDRAR.DATA; data width is determined by TRSTATR.DW.
- Status flag TRSTATR.AV is cleared after the Answer Frame has been finished and correctly acknowledged by the MLI receiver of the Local Controller.

An Answer Frame should be sent through the pipe that has received a read request but there must be only one MLI Transfer Window read access pending on any side of a MLI connection at any time, because the answer mechanism does not contain buffers for multiple Answer Frames.

Local Controller (Transmitting the read request)

If an Answer Frame has been received correctly and acknowledged, the following actions are executed in the MLI receiver of the Local Controller:

- The TRSTATR.RPx flags are cleared.

- The received data is written into the receiver data register RDATAR.
  If 8 data bits are received, they are duplicated to all 4 bytes in RDATAR.
  If 16 data bits are received, they are duplicated to both half-words in RDATAR.
- The detected data width of the received data is written into bit field RCR.DW.
- The received Pipe Number x represents the answer Pipe Number and is written into bit field TSTATR.APN.
- The information about the received frame type (= 11_B for an Answer Frame) is written into bit field RCR.TF.
- MLI event status flag RISR.NFRI (Normal Frame Received event) is set and a service request output is activated if enabled by RIER.NFRIE = 01_B or 10_B.
- The content of RADRR becomes invalid.
- The data that has been previously requested from the Remote Controller by a Read Frame is now available in RDATAR and can be read by a bus master (e.g. the CPU) of the Local Controller.
- If an Answer Frame is received while the corresponding TRSTATR.RPx bit is 0, the reception is declared as unintended and a Discarded Read Answer event is generated (see **Page 27-62**).

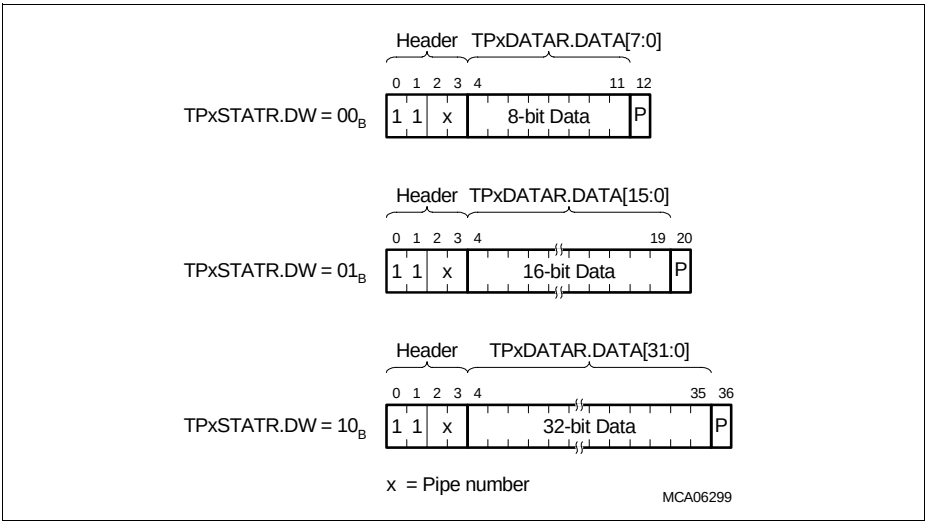


Figure 27-31 Answer Frame

Note: If an Answer Frame has been correctly received in the Local Controller, the Local Controller's software has to read it. As long as at least one byte of this data has not yet been read out, only one more MLI frame can be received (stored in a waiting position to be executed). Then the reception of more frames is blocked by Non-Acknowledge handshake. If the received data has been read out, frame execution and reception continue normally.

27.2.1.5 Command Frame

Command Frames transmit a command (e.g. setup information or service request) from a transmitting controller to a receiving controller.

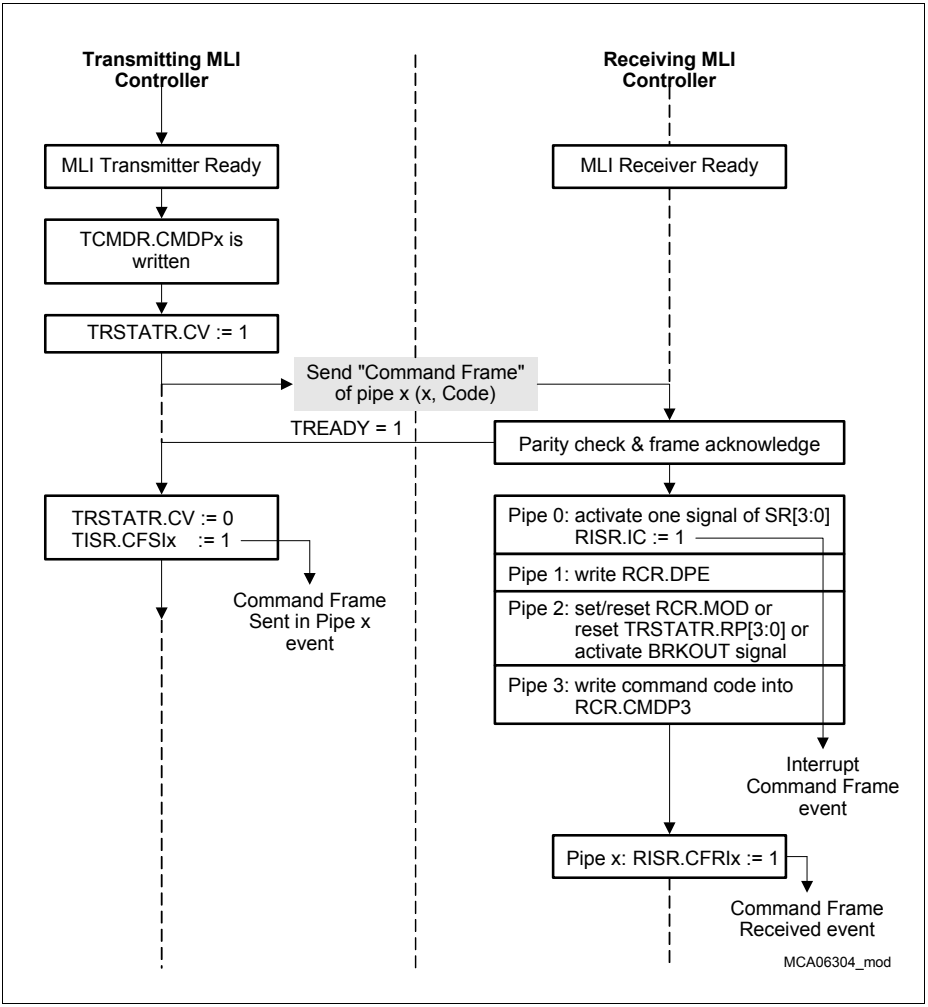


Figure 27-32 Command Frame Transaction Flow

Transmitting Controller

The transmission of a Command Frame is initiated by writing one of the four pipe x related command code bit fields in register TCMDR.CMDPx, triggering the following actions:

- Status flag TPxSTATR.CVx (command valid) is set and the Command Frame transmission is started using x as pipe number PN and the command code stored in TCMDR.CMDPx as parameters.
- TRSTATR.CVx is cleared after the Command Frame has been finished and correctly acknowledged by the MLI receiver of the Remote Controller.
- MLI event status flag TISR.CFSIx (Command Frame Sent event in pipe x) is set and a service request output is activated if enabled by TIER.CFSIEx = 1.

Receiving Controller

Depending on the pipe x related command code that is transmitted by a Command Frame, different actions are triggered in the receiving controller. **Table 27-5** describes the actions that are transmitted by a Command Frame and that cause a specific control task in the MLI receiver.

- The received PN value is checked and the corresponding control actions are executed according to **Table 27-5**.
- Independent of the received Pipe Number, event status flag RISR.CFRIx (Command Frame Received event in pipe x) is set and a service request output is activated if enabled by RIER.CFRIEx = 1.

If a Command Frame is received for pipe 2 with command code 1111_B, the $\overline{\text{BRKOUT}}$ output signal of the MLI module becomes activated if it is enabled by bit RCR.BEN = 1. If disabled by RCR.BEN = 0, signal $\overline{\text{BRKOUT}}$ will not be activated. The usage of $\overline{\text{BRKOUT}}$ is implementation-specific and can be used, for example, to generate a break condition in the on-chip debug support logic or trigger other functions.

Table 27-5 Command Frame Encoding

PN	CMD	Command Description
00_B	0001_B	Activate service request output SR0 of receiving MLI module
	0010_B	Activate service request output SR1 of receiving MLI module
	0011_B	Activate service request output SR2 of receiving MLI module
	0100_B	Activate service request output SR3 of receiving MLI module
	Others	no effect, reserved for future use

Table 27-5 Command Frame Encoding (cont'd)

PN	CMD	Command Description
01_B	0000_B	Set RCR.DPE (delay for parity error indication) in receiving MLI to 0000_B
	0001_B	Set RCR.DPE in receiving MLI to 0001_B
	0010_B	Set RCR.DPE in receiving MLI to 0010_B
	...	...
	1111_B	Set RCR.DPE in receiving MLI to 1111_B
10_B	0001_B	Enable Automatic Data Mode in receiving MLI (set RCR.MOD = 1)
	0010_B	Disable Automatic Data Mode in receiving MLI (set RCR.MOD = 0)
	0100_B	Clear bit TRSTATR.RP0 in receiving MLI
	0101_B	Clear bit TRSTATR.RP1 in receiving MLI
	0110_B	Clear bit TRSTATR.RP2 in receiving MLI
	0111_B	Clear bit TRSTATR.RP3 in receiving MLI
	1111_B	Generate break output signal $\overline{\text{BRKOUT}}$ in receiving MLI (if enabled by RCR.BEN = 1)
	others	no effect, reserved for future use
11_B	Any	Free programmable software command, written into bit field RCR.CMDP3 of receiving MLI

27.2.2 General MLI Features

The general MLI features comprise the:

- Parity generation and checking (see **Page 27-44**)
- Non-Acknowledge error (see **Page 27-47**)
- Address prediction (see **Page 27-47**)
- Automatic data transfers (see **Page 27-48**)
- Access protection (see **Page 27-49**)
- Triggered Command Frames (see **Page 27-49**)
- Transmit priority (see **Page 27-50**)
- Transmission delay (see **Page 27-50**)

27.2.2.1 Parity Check and Parity Error Indication

For parity generation, the number of transmitted bits with the value of 1 is counted over the header and the complete data field of a frame. For even parity, the parity bit is set if the result of a modulo-2 division of the elaborated number is 1. For odd parity, the parity bit is set if the result of a modulo-2 division of the elaborated number is 0.

For a parity error-free MLI connection, even parity must be selected in the transmitter because the receiver operates only with even parity detection. The capability to select odd parity can be used by the transmitter to force a parity error reply from the receiver during the startup procedure of the MLI connection. This can be used to measure the propagation delay and to optimize the ready delay time (see **Page 27-73**).

Note: There is no protection against frames where more than one bit is corrupted (e.g. shortened frames). In such a case, an unpredictable behavior of the MLI module may occur.

Transmitting Controller

The MLI transmitter counts the detected parity error conditions and generates a parity error event if a programmable number (max. 16) of parity error conditions has occurred. A parity error condition is indicated to the transmitter by the receiver after the transmission of a frame (see **Page 27-23**). The transmitter parity error condition is detected when the TREADY signal is sampled at low level within a programmable number (TCR.MDP = maximum delay for parity errors) of TCLK clock cycles after TVALID has been de-asserted to low.

If a transmitter parity error condition is detected, the MLI transmitter sets the parity error flag TSTATR.PE and also decreases the maximum parity error counter TCR.MPE by 1. The maximum parity error counter of the transmitter TCR.MPE determines the number of transmit parity error conditions that can be still detected until a transmitter parity error event is generated. If a transmitter parity error condition is detected and TCR.MPE is becoming 0 or while it is 0, a transmitter parity error event is generated by setting bit TISR.PEI (see **Figure 27-40** on **Page 27-60**) and an SRx output line is activated if

enabled by TIER.PEIE = 1. After a transmitter parity error event occurred, TCR.MPE can be set again by software to a value greater 0001_B. Otherwise, each additional transmitter parity error condition will generate a parity error event.

The transmitter parity error flag TSTATR.PE is cleared by hardware when a correct frame transmission and TREADY has been sampled with 1 within the ready delay time. It can be cleared by software by writing a 1 to bit SCR.CTPE. If for example, each transmitter parity error condition should generate a transmitter parity error event, TCR.MPE should be set to 0000_B. The software can check for accumulated parity error conditions by reading TCR.MPE or TISR.PEI, for the status of the latest received frame, it can check TSTATR.PE.

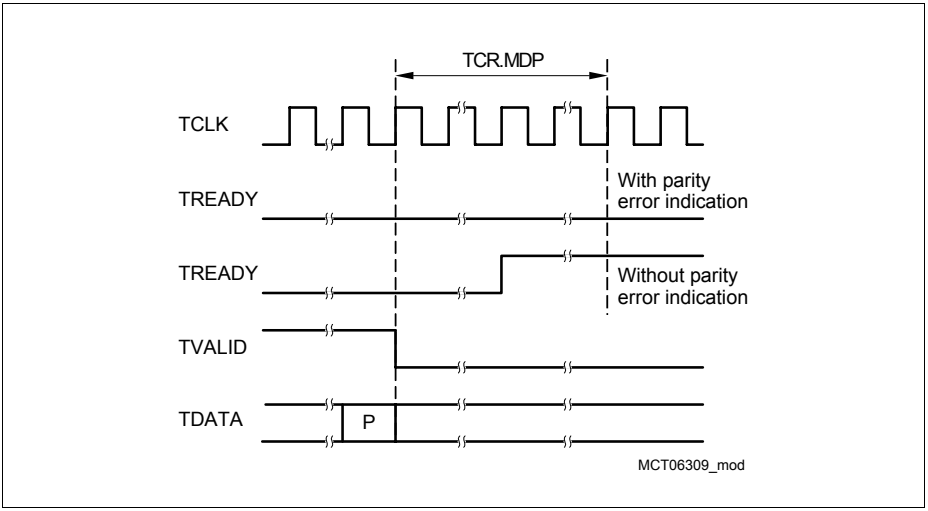


Figure 27-33 Parity Error Indication for the Transmitter

Receiving Controller

The receiver always checks the parity bit of a received frame for even parity. A receiver parity error condition is detected if the received parity bit does not match with the internally calculated one. If no receiver parity error condition is found after the reception of a frame, RREADY is immediately set to 1, otherwise RREADY is kept at 0 until a defined number of RCLK cycles (determined by bit field RCR.DPE = delay for parity error) has been elapsed. Then, RREADY is asserted high.

If a receiver parity error condition is found, the MLI receiver sets the parity error flag RCR.PE and additionally decreases the maximum parity error counter of the receiver RCR.MPE by 1. The maximum parity error counter RCR.MPE determines the number of receiver parity error conditions that can be still detected until a receiver parity error event is generated. If a receiver parity error condition is detected and RCR.MPE is becoming

0 or while it is already 0, a receiver parity error event is generated by setting bit RISR.PEI (see **Figure 27-44** on **Page 27-63**) and a service request output is activated if enabled by RIER.PEIE = 1. After a receiver parity error event has occurred, RCR.MPE can set again by software to a value greater 0001_B. If, for example, each receiver parity error condition should generate a receiver parity error event, RCR.MPE can be programmed to 0000_B or 0001_B.

The receiver parity error flag RCR.PE is cleared by hardware if a correct frame transmission has occurred. RCR.PE can be cleared by software by writing a 1 to bit SCR.CRPE.

The receiver parity error flag RCR.PE is cleared by hardware after a correct frame reception. It can be cleared by software by writing a 1 to bit SCR.CRPE. The software can check for accumulated parity error conditions by reading RCR.MPE or RISR.PEI, for the status of the latest received frame, it can check RCR.PE.

The delay for parity error bit field RCR.DPE is a read-only bit field in the receiver that updated by hardware if a Command Frame for pipe 1 is received. With this frame type, the transmitting controller transfers a value for RCR.DPE to the receiving controller during the setup phase of the MLI connection.

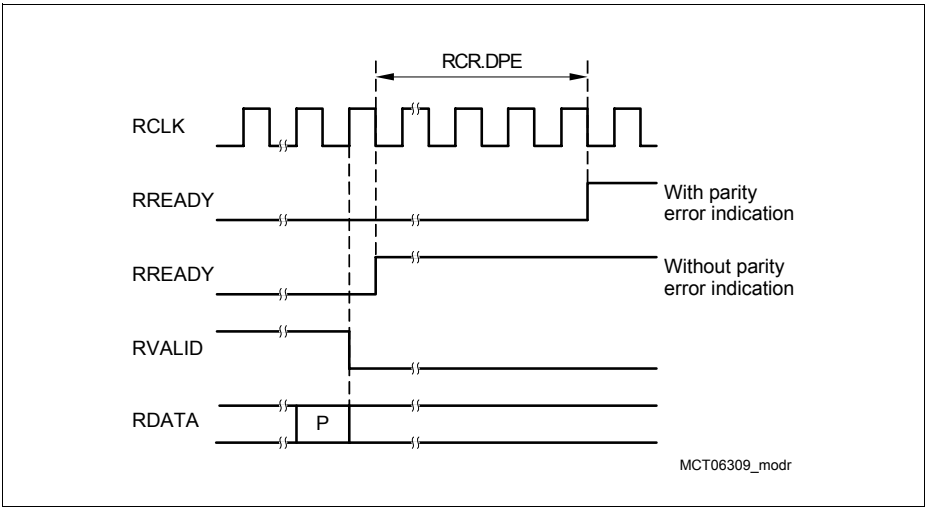


Figure 27-34 Parity Error Indication by the Receiver

27.2.2.2 Non-Acknowledge Error

A Non-Acknowledge error condition is detected by the transmitter when at the end of a frame transmission, the TREADY signal is still at high level (TREADY = 1 when TVALID becomes 0). In this case, the error flag TSTATR.NAE is set and the maximum Non-Acknowledge error counter TCR.MNAE is decremented by 1. If a Non-Acknowledge error condition is detected and TCR.MNAE is becoming 0 or while it is already 0, a time-out event is generated by setting bit TISR.TEI (see **Figure 27-40** on **Page 27-60**) and an MLI service request is generated if enabled by TIER.TEIE = 1. The Non-Acknowledge error flag TSTATR.NAE is cleared by hardware when a frame transmission has been acknowledged correctly. It can also be cleared by software when writing a 1 to bit SCR.CNAE.

The Non-Acknowledge error counter TCR.MNAE is automatically set to 11_B when a frame has been acknowledged correctly. It can be read and written by software, allowing a limited number of consecutive Non-Acknowledge errors to be defined that can be detected until a time-out error event is generated. If, for example, the first occurrence of a Non-Acknowledge error should lead to a time-out event, bit TCR.MNAE has to be written by software with 00_B or 01_B after each correctly received frame.

27.2.2.3 Address Prediction

An address prediction method can be enabled to support communication between MLI transmitter and MLI receiver without sending address offset information in the frames to optimize the required MLI bandwidth. This feature reduces the required bandwidth for MLI communication. Both communication partners, MLI transmitter and the MLI receiver are able to detect regular offset differences of consecutive window accesses to the same window. The address prediction mechanism working independently for each pipe, different prediction values can be handled in parallel for the different pipes.

Transmitting Controller

If the address prediction method is enabled (TCR.NO = 0), the MLI transmitter compares the offset of each Transfer Window read or write access with the offset of the previous access to the same Transfer Window (stored in TPxAOFR.AOFF). The result of this comparison is stored in two's complement representation in TPxSTATR.AP (limited to 9 bits, otherwise prediction is not possible). Between the accesses to a specific window, other windows can be accessed without disturbing the prediction.

If the offset differences are identical in at least two consecutive accesses to the same Transfer Window, an address prediction is possible (flag TPxSTATR.OP becomes set) and optimized frames can be sent to the receiving controller for this pipe. If the offset difference of a next access to the same Transfer Window does not match the calculated value in TPxSTATR.AP, flag TPxSTATR.OP is cleared and address prediction is not possible. In this case, a Normal Frame for writing or reading (Write Offset and Data Frame or Discrete Read Frame) is started.

Receiving Controller

The MLI receiver operates with an address prediction method equivalent to the MLI transmitter. This means that after receiving at least two consecutive Write Offset and Data Frames and/or Discrete Read Frames that include address information, the MLI receiver is able to follow the address prediction method used by the MLI transmitter.
Each received offset is compared in the MLI receiver with the offset of the previously received frame of the same pipe. The result of this comparison is stored in two's complement representation in RPxSTATR.AP (limited 9 bits).

If an optimized frame is received by the MLI receiver, it calculates the next address by adding the value stored in RPxSTATR.AP to the contents of the receiver address register RADRR.

In case of a Write Offset and Data Frame or a Discrete Read Frame (m offset bits), the receiver address registers RADRR and RPxBAR are always loaded with an updated address. This address is calculated by replacing the lowest m bit positions in RPxBAR with the received offset value. In this case, the address delta value stored in RPxSTATR.AP is not taken into account. The programmed size of the Remote Window and the number m of offset bits are given by RPxSTATR.BS. The bit positions RPxBAR[31:m] are kept constant, whereas the bit positions RPxBAR[m-1:0] are replaced.

27.2.2.4 Automatic Data Mode

The MLI module supports automatic data transfers for read or Write Frames without any CPU load in the receiving controller. This features is based on a move engine block providing the data, the complete address and the data width to an associated bus master on the system bus (see **Figure 27-1**). Depending on the implementation, this bus master can be capable of executing the requested data move operations autonomously. The Automatic Data Mode in the receiving controller can be enabled (RCR.MOD = 1) or disabled (RCR.MOD = 0) by software on receiving side or a Command Frame sent by the transmitting controller.
If the Automatic Data Mode is disabled, the receiving controller software has to execute the requested data transfers.
Additionally to the global enable/disable of the automatic mode by **RCR**.MOD, it is possible to individually exclude address ranges from automatic data transfer by an access protection scheme. The definition of the address ranges depend on the product and has been introduced to support the protection of critical data or modules.

Note: If a device contains the MLI move engine block as the only bus master, automatic mode has to be selected to allow transfers. This could be the case for external peripheral devices without own CPU.

27.2.2.5 Memory Access Protection

The MLI receiver provides a memory access protection logic allowing to exclude read and write accesses of the MLI move engine to specific parts of the memory map from automatic mode. Each address of a data move (read or write) is always checked if it targets an address range that is enabled for read/write access. If a requested data move is targeting an excluded address range, a memory access protection error event is generated and the receiving controller's software can take care of the service request.

The memory access protection logic handles two levels of address range definitions:

- Fixed address ranges (for complete modules or memory areas)
- Programmable address sub-ranges (to limit accesses to specific parts of bigger memory areas)

There is a maximum of 2 x 32 fixed address ranges available that can be individually enabled/disabled by the address range enable bits AER0.AENx and AER1.AENx (x = 0-31). If bit AERy.AENx is set, read/write accesses to the associated address range x are supported in automatic mode. If bit AENx is cleared, read/write accesses to the associated address range x are not automatically executed, a memory protection error event is generated, and SRx output line is activated if enabled by RISR.MPEI.

The MLI module supports a definition of up to two times four programmable address sub-ranges (with index n) within fixed address ranges. The parameters for the sub-ranges are stored in the access range registers ARR0 and ARR1, comprising:

- The size of an address slice defined as sub-range (ARRy.SIZEn)
- The location of an address slice defined as sub-range (ARRy.SLICEn)

Note: The definition of the fixed address ranges and the sub-ranges is product-specific. Detailed values are given in the module implementation chapter.

27.2.2.6 Triggered Command Transfers

The MLI module supports the transmission of Command Frames triggered by hardware signals (up to 4 trigger inputs TR[3:0]). If a rising edge at a TRx input is detected, a corresponding bit TRSTATR.CIVx is set. The MLI transmitter sends out a Command Frame with PN = 00_B and CMD = x + 1 if bit CIVx = 1. This Command Frame can then trigger the activation of the corresponding SRx service request output of the Remote Controller. A Triggered Command Frame can be used monitor service request signals in the Local Controller and to transfer the requests to the Remote Controller, without intervention of any CPU.

Bit CIVx is automatically cleared after successful transmission of the related Command Frame or by writing 1 to SCR.CCIVx.

Note: The connection of the TR[3:0] input lines is product-specific. Detailed information is given in the module implementation chapter (see ***Page 27-137****).*

27.2.2.7 Transmit Priority

In the case that several requests for frame transmission are pending at the same time in a MLI transmitter, the following priority scheme is applied, starting with the highest priority.

For the Answer Frame, only one frame can be pending at a time in the transmitter. So the user has to take care that an older Answer Frame is completely handled before requesting a new one. The same applies for the base address copy frame.

For the Triggered Command Frames, the software driven Command Frames and the read or Write Frames, one frame of each type can be pending per pipe at a time.

Note: The MLI has 4 inputs for Triggered Command Frames. They are not necessarily connected in all devices. Please refer to the device specific implementation chapter for details (see ***Page 27-137****).*

- Answer Frame (only one frame pending allowed at a time)
- Triggered Command Transfer (CIV0 before CIV1 before CIV2 before CIV3)
- Software driven Command Frames (CV0 before CV1 before CV2 before CV3)
- Read or Write Frames (DV0 before DV1 before DV2 before DV3)
- Base Address Copy Frame (only one frame pending allowed at a time)

27.2.2.8 Transmission Delay

A transmission delay can be introduced in the transmitter between the detection of the rising edge of the RREADY input signal and the next possible frame start. This delay represents the minimum time between the acknowledge of a former frame by RREADY and a new frame (if a request is pending). The delay is defined by bit field TCR.TDEL in cycles of the transmitter system clock f_{FPI}.

The purpose of the transmission delay is to compensate for the time required for data to be transferred from the receiver frequency domain into the microcontroller frequency domain.

27.2.3 Interface Description

The MLI transmitter and MLI receiver communicate with other MLI receivers and MLI transmitters via a four-line serial connection each. Several I/O lines of these connections are available outside the MLI module kernel as a four-line output or input vector with index numbering A, B, C and D. The MLI module internal I/O control blocks define which signal of a vector is actually taken into account and also allow polarity inversions (to adapt to different physical interconnection means).

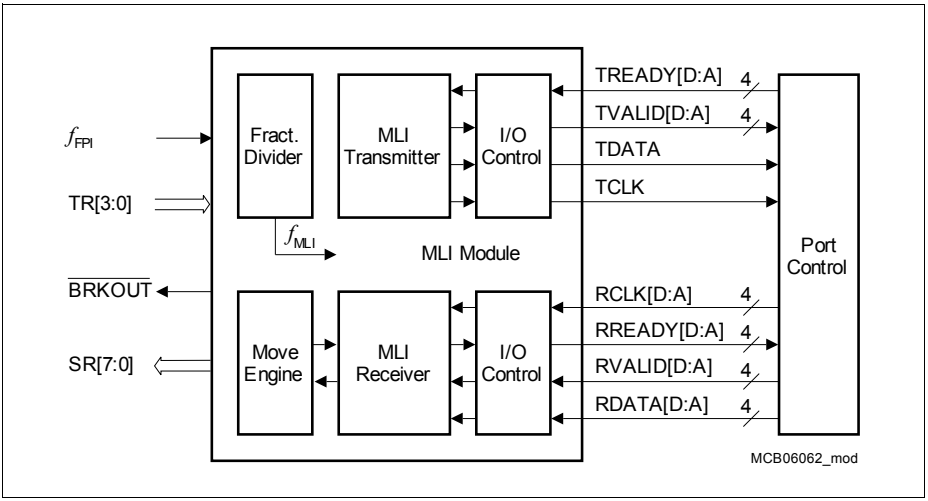


Figure 27-35 General Block Diagram of the MLI Module

Each input/output signal used for MLI communication between a transmitter and a receiver can be disabled and inverted in its polarity. Please note that all waveform diagrams in the MLI chapter refer to non-inverted signals. If polarity inversions are programmed, the waveform diagrams have to be interpreted accordingly. In order to avoid naming mismatches, the signals keep their names, although a polarity inversion might have been programmed. If desired, polarity inversions for the same signal have to be programmed in the transmitter and in the receiver to guaranty signal consistency (there has always to be an even number of inversions between an MLI transmitter and receiver). After reset, the following setting is applied, allowing MLI communication without modification of register OICR[1)]:

- The signal with the index A is selected from each input/output vector.
- TCLK generation is enabled and RCLK reception is enabled.

1) Other services (e.g. an automatic boot sequence or a boot routine) can change the OICR setting. Differing values are then indicated in the corresponding implementation chapter.

- Polarity inversion is disabled for all signals (no inversion).
- Not selected output signals are at low level.

The usage of signal BRKOUT is implementation-specific and can be used, for example, to generate a break condition in the on-chip debug support logic or trigger other functions. This signal is activated (as a pulse) by a Command Frame.

The service request outputs SR[7:0] of the MLI module can be activated (as a pulse) by transmitter or receiver events (for all SRx), as well as by Command Frames (only for SR[3:0]).

The MLI module also supports 4 trigger inputs TR[3:0]. A rising edge at input TRx sets bit TRSTATR.CIVx and requests the transfer of a Triggered Command Frame in pipe 0, with a CMD = x + 1.

27.2.3.1 Transmitter I/O Line Control

Figure 27-36 shows the MLI transmitter I/O control logic.

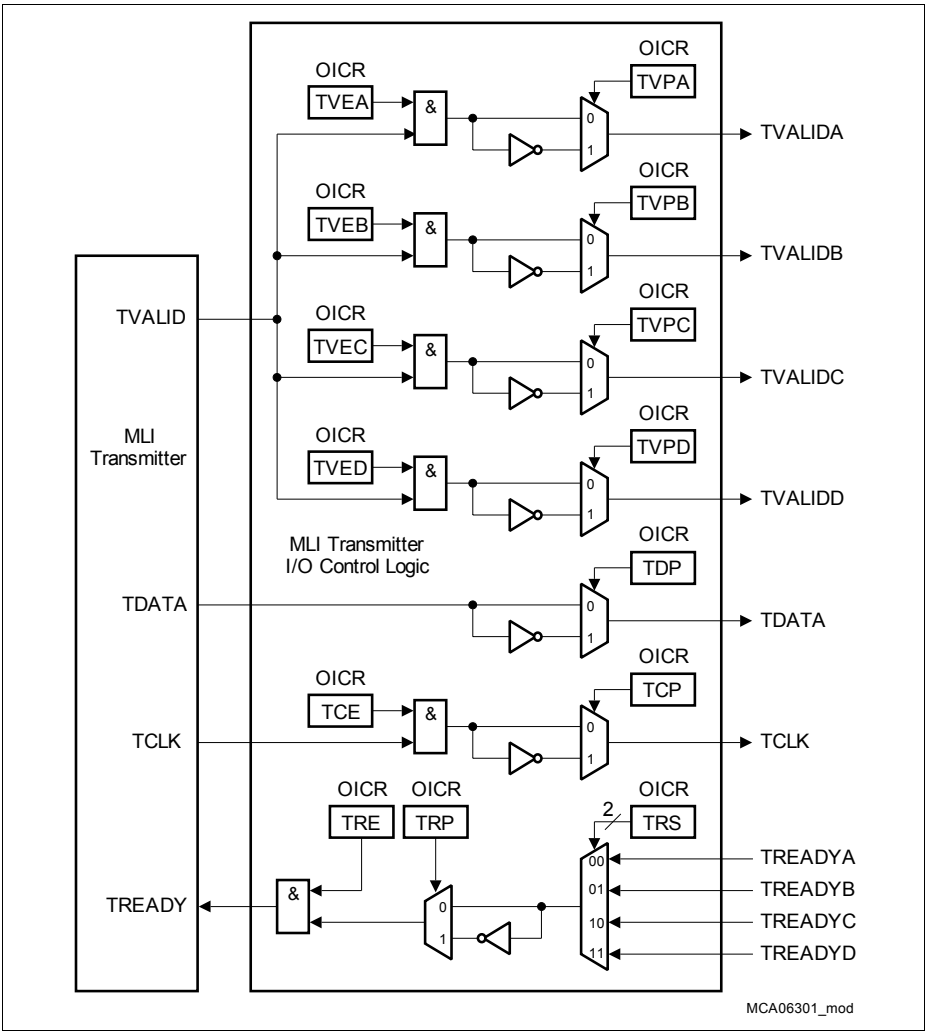


Figure 27-36 Transmitter Input/Output Control Logic

27.2.3.2 Receiver I/O Line Control

Figure 27-37 shows the MLI receiver I/O control logic.

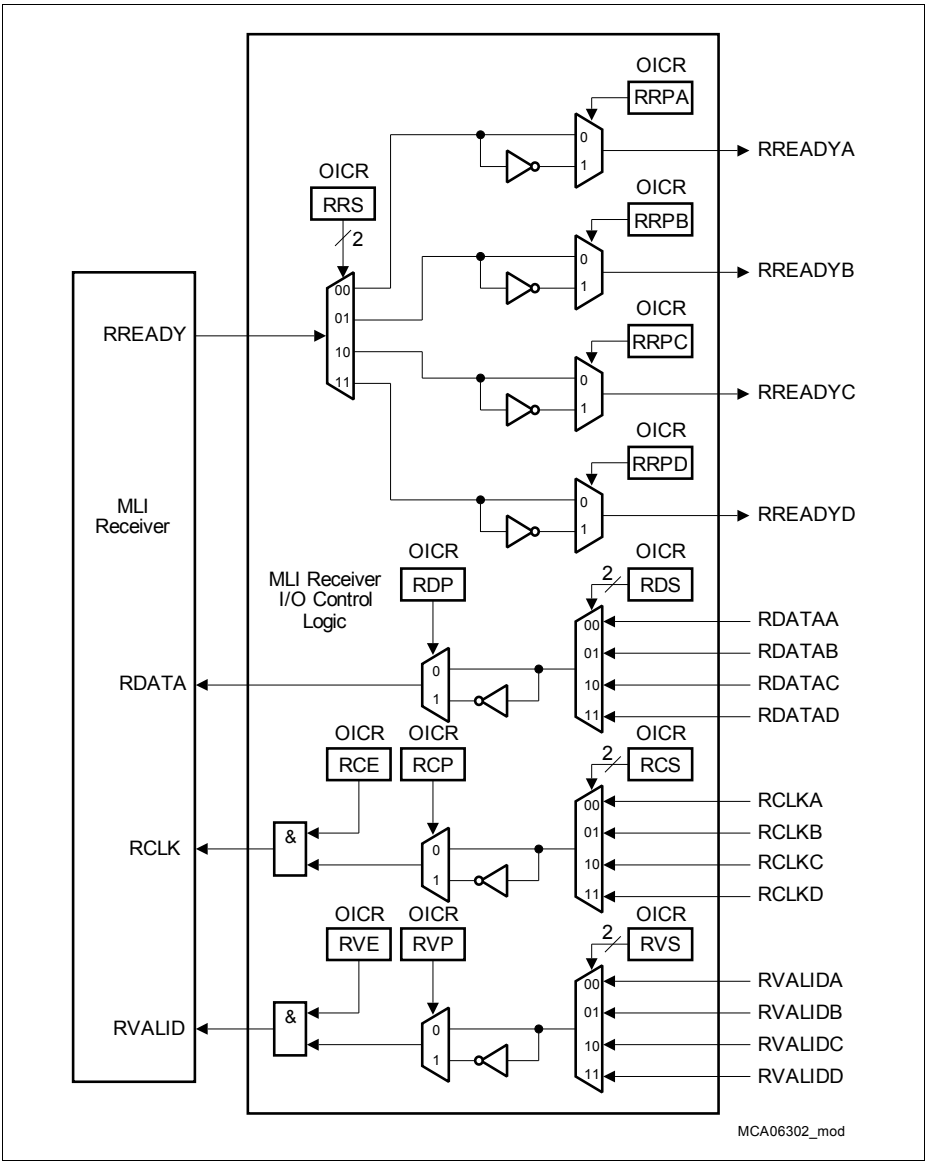


Figure 27-37 Receiver Input/Output Control Logic

27.2.3.3 Connecting Several MLI Modules

The MLI structure also allows to connect several MLI modules together, e.g. two Remote Controllers (X and Y) to one Local Controller. In this case, the Local Controller can send data to either one or the other or to both Remote Controllers in parallel. Each Remote Controller is connected via an own set of READY/VALID signals to the Local Controller, whereas the transmitter DATA and CLK are broadcast signals. The status of the VALID lines defines, which Remote Controller is accessed.

Only one receiver being available in the Local Controller, the reception of data can be handled only either from one or the other Remote Controller. The software has to ensure that only one Remote Controller sends data back to the Local Controller, e.g. by using Read Frames or by enabling/disabling the generation of Write Frames in the Remote Controllers.

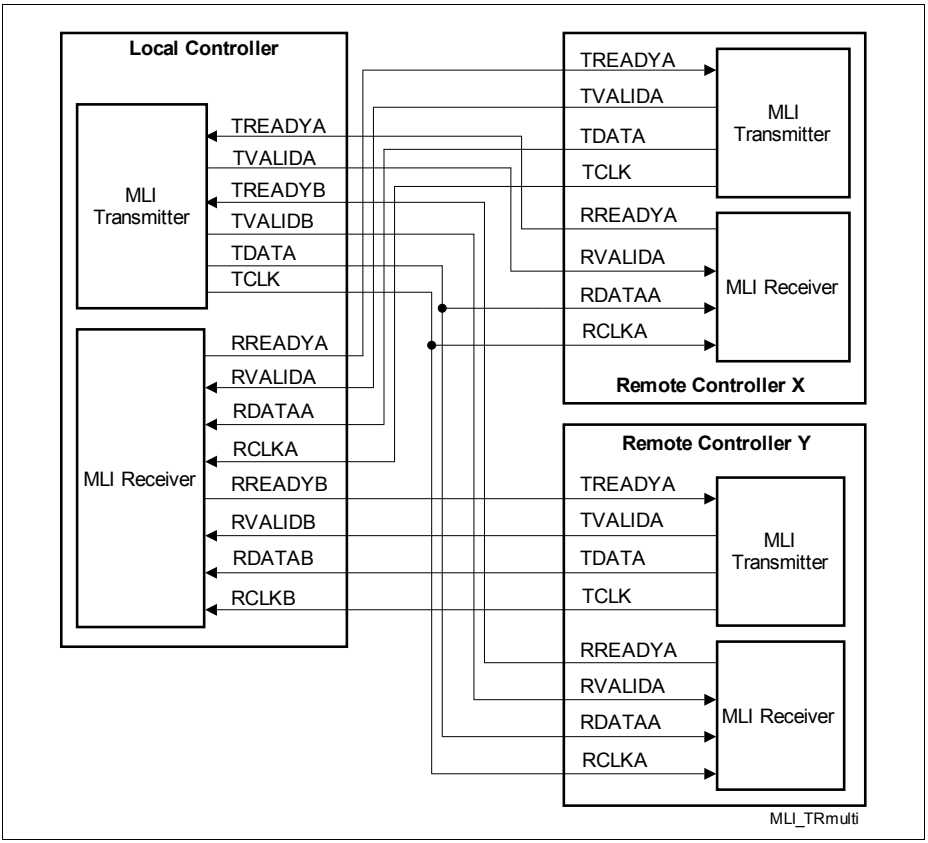


Figure 27-38 Connecting Two Remote Controllers

Another possibility to connect several MLI modules is a ring structure, with (at least) one dedicated pipe per device. This leads to a structure where the Local Controller's transmitter is connected to the receiver of Remote Controller X, the transmitter of Remote Controller X to the receiver of Remote Controller Y, and the transmitter of Remote Controller Y to the Local Controller's receiver.

This structure supports autonomous data generation and transfer in both Remote Controllers, for example to transfer data generated in a Remote Controller to the Local Controller without using Read Frames. In a ring structure, the Read Frame handling should be avoided. It is possible for the Local Controller to access both Remote Controllers independently. For example, the Remote Window of pipe x covers the address range of Remote Controller X, whereas pipe y targets the Transfer Window y of Remote Controller X. In Remote Controller Y, the pipe y targets the available address range. If the Local Controller issues a Write Frame on pipe x, the Remote Controller X is addressed. In case of a Write Frame on pipe y, the Remote Controller Y is targeted, passing through a Transfer Window of Remote Controller X. The two remaining pipes could be used for Write Frames issued by Remote Controller X (passing through a Transfer Window of Remote Controller Y) and by Remote Controller Y.

27.2.4 MLI Service Request Generation

The MLI module's service request outputs SRx are used to indicate module internal MLI events to other modules or devices outside the MLI module, depending on the device implementation. They can trigger interrupts of a CPU (if available), can be used as DMA request lines (if available), or for other trigger purposes. The MLI events being able to trigger interrupts or other service requests, names of some flags and control registers refer to interrupt generation.

MLI module events are generated by event sources in the transmitter and in the receiver. Each event source provides a status flag and an enable bit with software clear capability. In some cases, several event sources are combined to a common event. An MLI event, internally generated by an event source, is stored in a status flag that is located in the interrupt status registers TISR (for transmitter events) or RISR (for receiver events). All event flags can be cleared individually by software write actions to bits located in the interrupt enable registers TIER (for transmitter events) or RIER (for receiver events). These two registers also contain the enable control bits that allow each event source to be enabled/disabled individually for service request activation. Each event can be connected to exactly one of the eight service request outputs SR[7:0] by a 3-bit interrupt node pointer.

One additional register, the Global Interrupt Set Register GINTR, allows each service request output to be activated separately without setting the status flags of the event sources (see **Page 27-58**). This feature is sometimes helpful for software test purposes or to trigger MLI external actions.

Interrupt Registers

The MLI event sources are controlled by several registers (see **Table 27-6** and **Page 27-107**). The register name prefixes "T" and "R" indicate if a register is assigned to the MLI transmitter or to the MLI receiver.

Table 27-6 Interrupt Registers

Unit	Registers with		
	Request Flags	**Enable Bits/ Req. Flag Clear Bits**	**Node Pointer**
MLI Transmitter	TISR	TIER	TINPR
MLI Receiver	RISR	RIER	RINPR

Service Request Compressor

The MLI event logic uses a compressing scheme for flexible service request processing. Eleven MLI events (six transmitter events and four of the five receiver events) are directed via a 3-bit interrupt node pointer to one of the eight service request outputs

SR[7:0]. Each demultiplexer output selected by its Node Pointer = x (x = 0-7) is connected to one input of the SRx OR-Gate. This wiring scheme also supports the connection of more than one event source to an service request output SRx. One receiver event, the interrupt Command Frame event, has a special characteristic: its node pointer is controlled by the received CMD value directly and only SR[3:0] OR-Gates are selectable.

Figure 27-39 shows the service request compressing logic. For reasons of simplicity, not all MLI events, connections, and OR-Gates are explicitly shown. The OR-Gate inputs are connected to the demultiplexers of the MLI event specific lines. Furthermore, a service request output SRx can be triggered by software if the corresponding interrupt set bit in register GINTR is written with a 1.

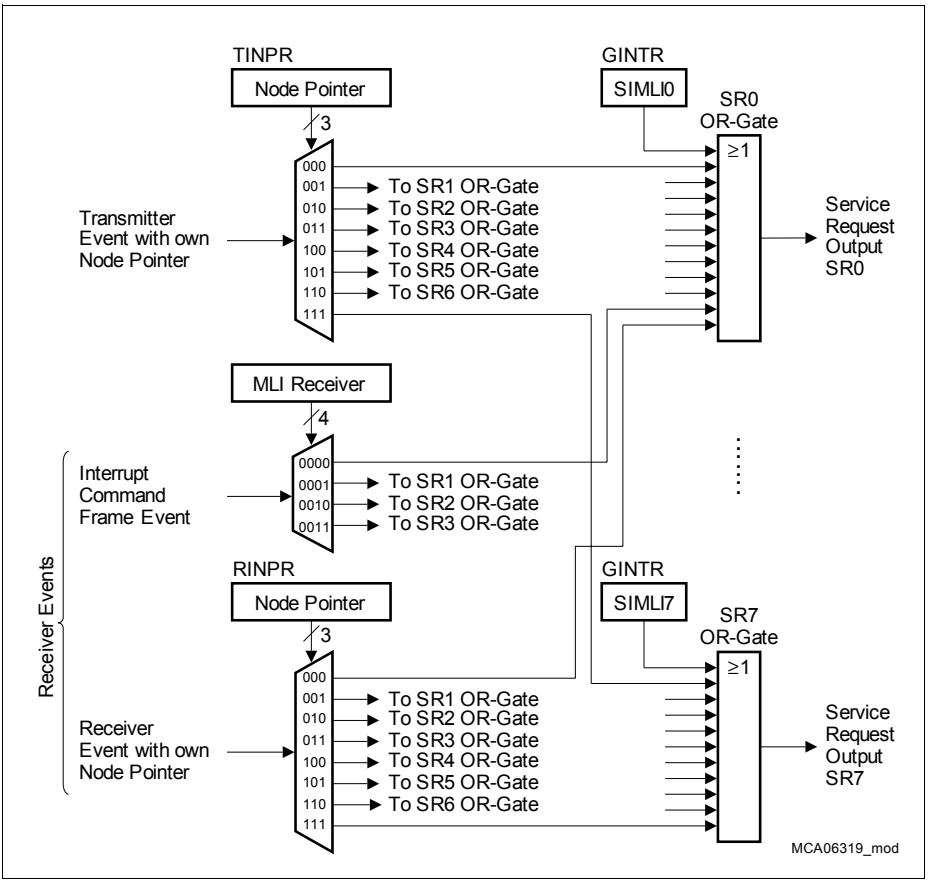


Figure 27-39 Service Request Compressor

Note: The number of SRx outputs of an MLI module and their connection to other modules depends on the implementation of the MLI module in the specific product.

27.2.5 Transmitter Events

The MLI transmitter can generate the following MLI events:

Table 27-7 MLI Transmitter Events

Events	Events combined to	See
Parity Error	Parity/Time-out Error	Page 27-60
Time-out Error		
Normal Frame Sent in Pipe 0	Normal Frame Sent in Pipe 0	Page 27-60
Normal Frame Sent in Pipe 1	Normal Frame Sent in Pipe 1	
Normal Frame Sent in Pipe 2	Normal Frame Sent in Pipe 2	
Normal Frame Sent in Pipe 3	Normal Frame Sent in Pipe 3	
Command Frame Sent in Pipe 0	Command Frame Sent	Page 27-61
Command Frame Sent in Pipe 1		
Command Frame Sent in Pipe 2		
Command Frame Sent in Pipe 3		

27.2.5.1 Parity/Time-out Error Event

A parity/time-out error event is generated when a programmable maximum number of parity errors or a programmable maximum number of Non-Acknowledge errors have been reached. Both events have separate status/control bits but are concatenated to one common error event.

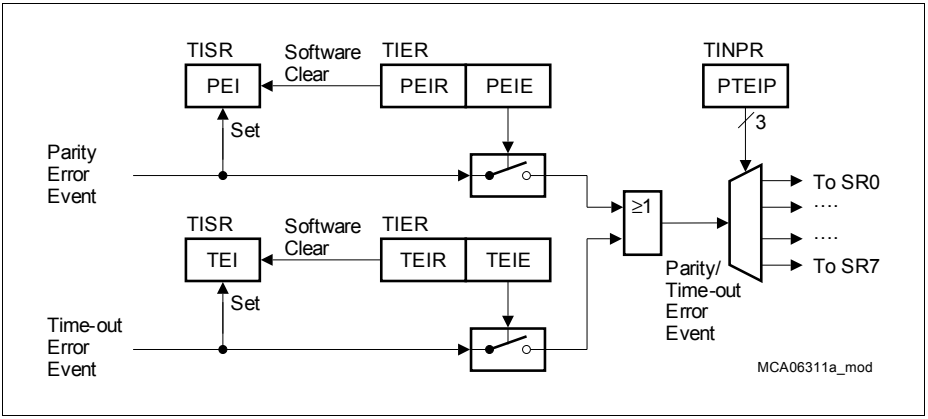


Figure 27-40 Parity/Time-out Error Event Logic

27.2.5.2 Normal Frame Sent x Event

A Normal Frame sent x (x = 0-3) event is generated when a Normal Frame has been sent and correctly received in pipe x.

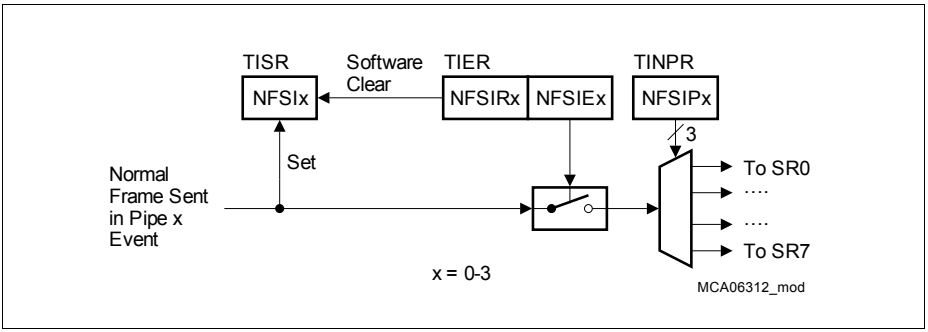


Figure 27-41 Normal Frame Sent x Event Logic

27.2.5.3 Command Frame Sent Events

A Command Frame sent event is generated when the MLI transmitter has sent a Command Frame through pipe x (x = 0-3) that has been correctly received. Separate status/control bits are assigned to each pipe. All four pipe related Command Frame sent events are concatenated to one common Command Frame sent event.

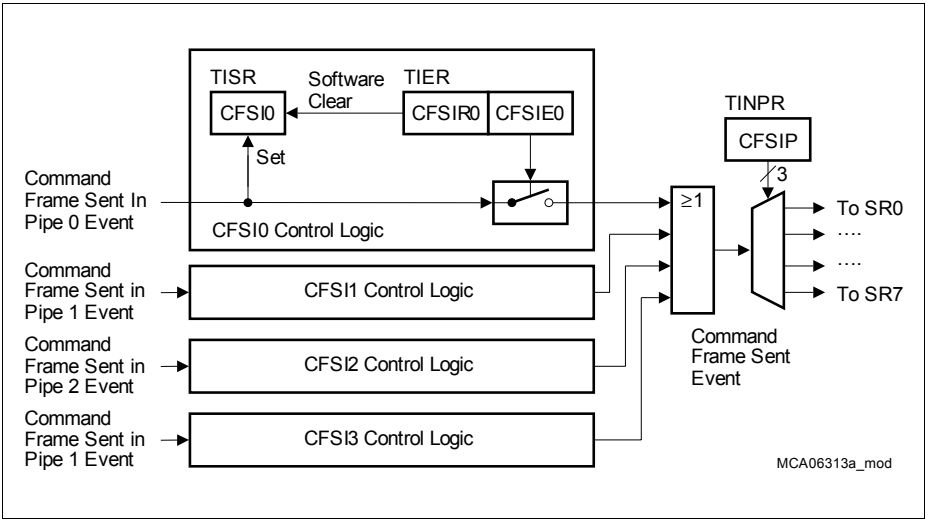


Figure 27-42 Command Frame Sent Event Logic

27.2.6 Receiver Events

The MLI receiver can generate the following MLI events:

Table 27-8 MLI Receiver Interrupts

Events	Events combined to	See
Discarded Read Answer	Discarded Read Answer	Page 27-62
Memory Access Protection Error	Memory Access Protection/ Parity Error	Page 27-63
Parity Error		
Normal Frame Correctly Received	Normal Frame Received	Page 27-64
Move Engine Access Terminated		
Interrupt Command Frame	Interrupt Command Frame	Page 27-65
Command Frame Received on Pipe 0	Command Frame Received	Page 27-66
Command Frame Received on Pipe 1		
Command Frame Received on Pipe 2		
Command Frame Received on Pipe 3		

27.2.6.1 Discarded Read Answer Event

A discarded read answer received event is generated if an Answer Frame has been received and the read pending flag TRSTATR.RPx of its correspondent pipe is 0. Although named “discarded”, the received data is available in the receiver data register until it is overwritten by the next incoming data.

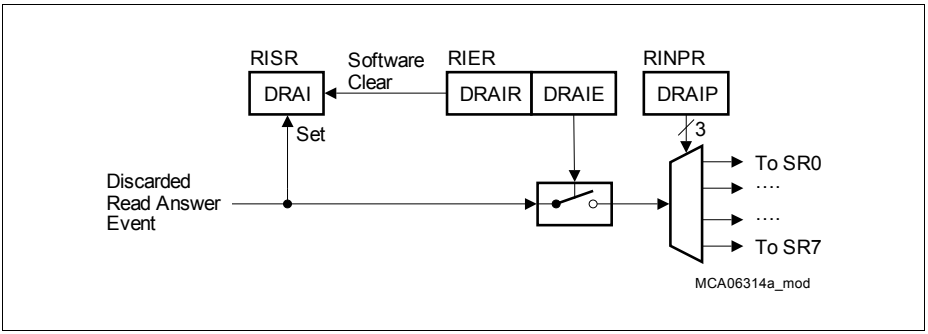


Figure 27-43 Discarded Read Answer Event Logic

27.2.6.2 Memory Access Protection/Parity Error Event

A memory access protection/parity error event is detected if a non allowed read or write access has been detected or if a programmable maximum number of receiver parity errors is reached. Both MLI events have separate status/control bits but are concatenated to one common error event.

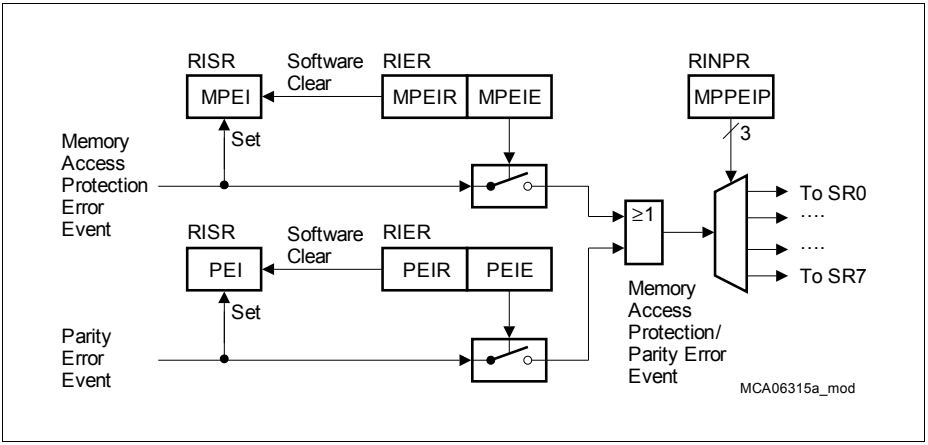


Figure 27-44 Memory Access Protection/Parity Error Event Logic

27.2.6.3 Normal Frame Received/Move Engine Terminated Event

A Normal Frame received event is generated if the MLI receiver has correctly received a Normal Frame (a Copy Base Address Frame, a Read or a Write Frame, an Answer Frame, but not a Command Frame) or if the move engine has terminated its read or write access. Both event sources have separate status/control bits but are concatenated to one common Normal Frame received event.

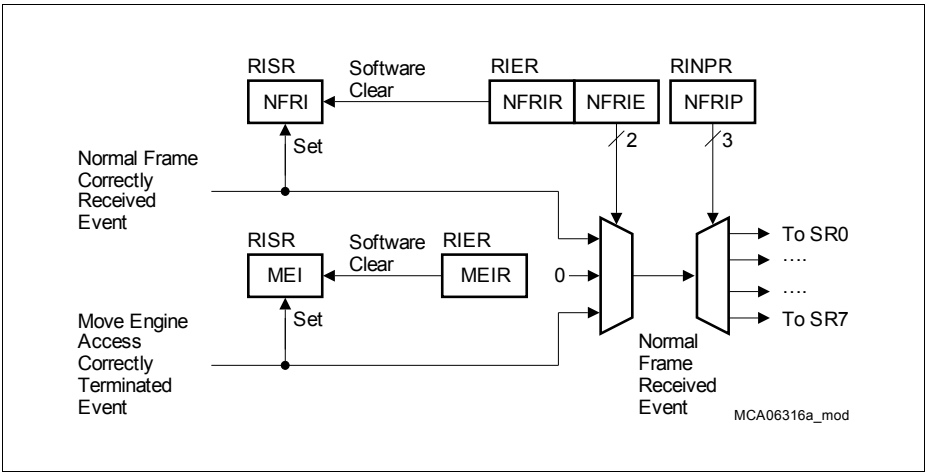


Figure 27-45 Normal Frame Received Event Logic

27.2.6.4 Interrupt Command Frame Event

An interrupt Command Frame event is generated if a Command Frame is received correctly on pipe 0 with a valid command code for service request output activation (CMD = 0000_B to 0011_B). The received command code determines which of the service request outputs SR[3:0] should be activated.

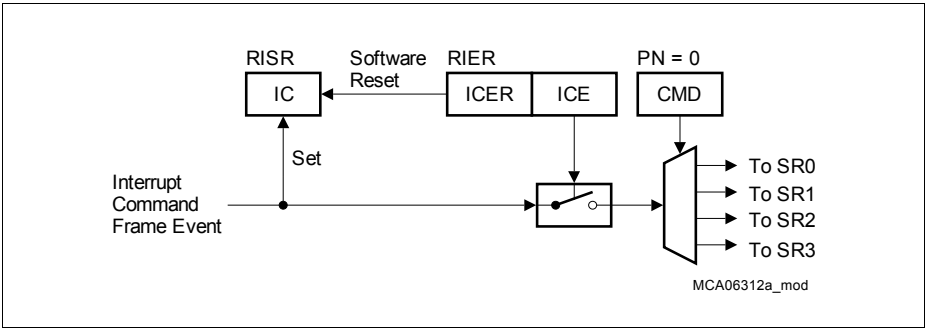


Figure 27-46 Interrupt Command Frame Event Logic

27.2.6.5 Command Frame Received Event

A Command Frame received event is generated if the MLI receiver has correctly received a Command Frame through Pipe Number x (x = 0-3). Separate status/control bits are assigned to each pipe. All four pipe related Command Frame received in pipe x events are concatenated to one common Command Frame received event.

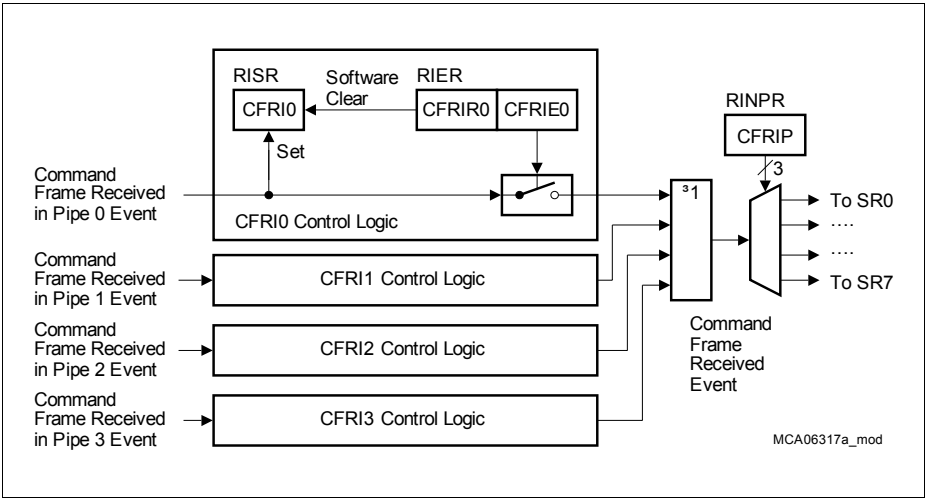


Figure 27-47 Command Frame Received Event Logic

27.2.7 Baud Rate Generation

The MLI transmitter baud rate is given by $f_{MLI}/2$. The MLI shift clock output signal TCLK of the transmitter toggles with each clock cycle of f_{MLI} in order to obtain a 50% duty cycle (the 50% duty cycle can vary up to one clock cycle of f_{FPI} in fractional divider mode). The MLI receiver automatically adapts to the incoming receive shift clock signal RCLK. The received baud rate is determined by the connected transmitter and has no direct relation to f_{FPI} except that it should not exceed f_{FPI}.
The frequency f_{MLI} is generated by the fractional divider FDIV.

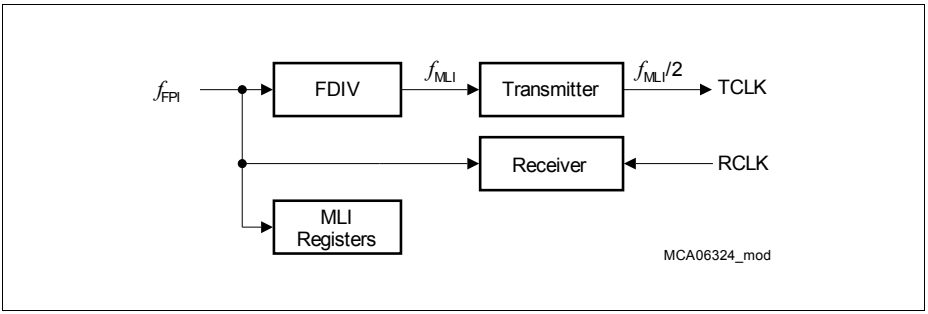


Figure 27-48 MLI Baud Rate Generation

Normal Divider Mode

In normal divider mode (FDR.DM = 01_B) the fractional divider behaves like a reload counter (addition of +1) that generates a clock f_{MLI} on the transition from $3FF_H$ to 000_H. FDR.RESULT represents the counter value and FDR.STEP defines the reload value. In order to achieve $f_{MLI} = f_{FPI}$, FDR.STEP must be programmed with $3FF_H$. The output frequency in normal divider mode is defined according the following equation:

$$f_{MLI} = f_{FPI} \times \frac{1}{1024 - FDR.STEP} \quad (27.1)$$

Fractional Divider Mode

If the fractional divider mode is selected (FDR.DM = 10_B), the clock f_{MLI} is derived from the input clock f_{FPI} by division of a fraction of STEP/1024 for any value of STEP from 0 to 1023. In general, the fractional divider mode allows to program the average clock frequency with a higher accuracy than in normal divider mode. In fractional divider mode a clock pulse f_{MLI} is generated depending on the result of the addition FDR.RESULT + FDR.STEP. The frequency f_{MLI} corresponds to the overflows over $3FF_H$. Note that in fractional divider mode the clock f_{MLI} can have a maximum period jitter of one f_{FPI} clock period. This jitter is not accumulated over several cycles and does not

exceed one cycle of f_{FPI}.
The frequency in fractional divider mode is defined according the following equation:

$$f_{MLI} = f_{FPI} \times \frac{STEP}{1024} \quad (27.2)$$

The baud rate of MLI transmissions equals f_{TCLK}, that is defined by the frequency of clock signal f_{MLI} divided by 2 to create the 50% duty cycle of the shift clock signal TCLK. The signal TCLK toggling with each period of f_{MLI}, a jitter due to fractional dividing is propagated to TCLK.

$$f_{TCLK} = \frac{f_{MLI}}{2} \quad (27.3)$$

27.2.8 Automatic Register Overwrite

The value of register OICR and bit RCR.RCVRST is overwritten by hardware in the next two clock cycles after a reset (first OICR, followed by RCR). The value applied during reset is given in the register description. This automatic overwrite allows adapting the module to different application requirements without changing the module itself. For example, during reset the receiver is set to a defined state and can be used afterwards for reception without the need to modify it by a write action (if the bit RCVRST is modified to 0).

The values applied after the overwrite can be identical to the indicated reset values. Please refer to the implementation chapter for the modified values (see).

27.3 Operating the MLI

Data transfer via MLI between a Local Controller and a Remote Controller is only possible if both are initialized correctly by following sequence of 4 steps. Steps 3 and 4 are necessary if the initialization sequence is exclusively controlled by the Local Controller. If both communication partners are able to run initialization software, steps 1 and 2 can be executed separately by both controllers to initialize both transmitters and both receivers.

1. The transmitter of the Local Controller has to be initialized by write actions to the transmitter registers.
2. The pipes from the Local Controller's transmitter to the Remote Controller's receiver and the Remote Controller's receiver have to be initialized.
3. The Remote Controller's transmitter has to be initialized by data write actions from the Local Controller via the Remote Controller's receiver to the Remote Controller's transmitter registers.
4. The pipes from the Remote Controller's transmitter back to the Local Controller's receiver and the Local Controller's receiver have to be initialized. This is done by frames from the Remote Controller's transmitter. These frames are the result of data write actions of the Local Controller to the Remote Controller's transmitter registers.

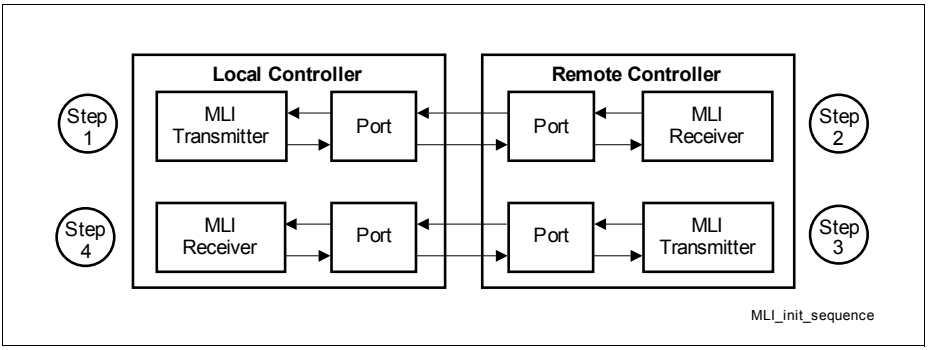


Figure 27-49 Initialization Sequence for an MLI Connection

To initialize and to operate the MLI, the following items should be taken into account:

- Connection setup (see **Page 27-70**)
- Local Controller transmitter and pipe setup (see **Page 27-71**)
- Remote Controller receiver setup (see **Page 27-71**)
- Remote Controller transmitter and Local Controller receiver setup (see **Page 27-72**)
- Delay adjustment (see **Page 27-73**)
- Connection to DMA mechanism (see **Page 27-75**)
- Connection of MLI to SPI (see **Page 27-75**)

27.3.1 Connection Setup

For the general setup of an MLI connection, several steps have to be respected.

- There is the possibility to change the signal routing to adapt to different applications. If another connection than the default one from an input/output vector of the MLI signals is desired, register OICR has to be programmed (see also **Section 27.2.8**).
- In some devices (mainly stand-alone peripheral devices without CPU, where the MLI module is a possible communication channel), the setting “A” can be modified by hardware to another setting (e.g. to setting “B”) during the boot phase. In this case, the initial setting “A” can correspond to an inactive setting (MLI not used for communication), whereas the setting “B” is used for MLI communication.
- In the case a memory access protection is implemented in the receiver and automatic handling of data is desired, the user has to enable the corresponding address range in registers AER and ARR. After a reset, in most microcontrollers, the access protection is generally disabled to avoid access to safety-critical data. Depending on the device, some specific address ranges can already be enabled for automatic access by default.
- In devices with explicit port control (such as microcontrollers), the port pins are generally set to input after a reset. In order to allow MLI communication, the MLI-related port pins have to be configured to make the MLI signals externally available and to adapt the driver setting (refer to port chapter).
  The MLI module should not be enabled for reception (RCR.RCVRST = 1) before programming the desired port setting, because changing the port setting can lead to unintended edges at the module inputs due to setting changes. If the MLI module is already enabled for reception, unintended edges are interpreted as communication signals, so the receiver might deliver wrong results. If this has happened unintentionally, the receiver can be reset by RCR.RCVRST=1.

27.3.2 Local Transmitter and Pipe Setup

The initialization of the transmitter of the Local Controller is done by writing to the transmitter registers. The Remote Controller's MLI receiver can then be initialized by the Local Controller's transmitter.

- After a hardware reset operation, the MLI transmitter is disabled (TCR.MOD = 0). In disabled mode, no frame transmission can take place. After writing TCR.MOD = 1, the transmitter is enabled to send frames.
- The desired transmitter baud rate can be adjusted by the fractional divider FDIV. It has to be ensured that the fractional divider is set to a value that is supported by the port structures of the Local and the Remote Controllers (rise/fall times) and the physical layer. For example, if a division by 1,5 is selected, the fractional divider will deliver count pulses for f_{MLI} with a sequence of 1-2-1-2-1-2- clock cycles of f_{FPI}. The shortest interval between two count pulses in a sequence (given by the truncated divider factor, so 1 cycle of in this example) has to be handled by the communicating devices.f_{FPI}
- Depending on the application requirements, a desired service request output SRx can be activated if a transmitter event is detected.
- The maximum delay for parity error detection in the transmitter has to be programmed. There are two possibilities to get the MLI communication started.
  First (easier) possibility is to write TCR.MDP to 14 and to set RCR.DPE to 15.
  The second possibility could be used to optimize the bandwidth of the MLI connection. It is described in **Section 27.3.5** on **Page 27-73**.

27.3.3 Remote Receiver Setup

The initialization of the Remote Controller's receiver is done by frames sent by the Local transmitter. Therefore, the Remote Controller's receiver has to be able to receive frames.

- In order to allow communication, the Remote Controller's MLI signals have to be connected to the Local Controller's transmitter signals (see register OICR and port settings).
- The Remote Controller's bit RCR.RCVRST has to be 0 to enable frame reception.
- The buffer area size and the base address of the Remote Window for pipe x are defined by the data written to registers TPxBAR. Bit TRSTATR.BAV has to be 0 before each write action to one of these registers. With this information, the buffer area sizes (defining the number of address bits in data frames or Read Frames) are known in the transmitter and in the receiver for each pipe.
  The base addresses for the Remote Windows have to be selected to cover the target address ranges in the Remote Controller. It is recommended to use the minimum buffer size required by the application in order to minimize the bandwidth taken by the transfer of the address bits. The base address of a Remote Window has to be set to a value aligned to its size, e.g. a Remote Window of 8 Kbytes must start at an 8 Kbyte address boundary.

- In devices with access protection mechanism against unauthorized accesses via MLI, the Remote Controller has to enable the desired address range(s) to support automatic mode. If automatic mode is not desired, the Remote Controller has to handle the complete data traffic by software.
- A possibility to test the setup in devices with the capability to run own test software is the local loop back (the transmitter is connected locally to the receiver of the same MLI module). In devices without this capability, the module loop back can be hardly used (or it is even not implemented, refer the connection table in the implementation chapter).
  If implemented, for local loop back, the signal connections have to be programmed to setting “D”, leading to the local receiver being connected directly to the local transmitter (without using a port structure). In this case, the local receiver seems to be the remote receiver. Data written to a local Transfer Window are received and handled by the local receiver. Test software in the Local Controller can check for correct setup, data consistency, MLI event handling, and correct address handling in the Local Controller.
- If automatic data handling is desired (necessary for devices without the capability to handle data traffic by its CPU), the Automatic Data Mode has to be enabled by sending a Command Frame in pipe 2 with CM = 0001_B to set RCR.MOD = 1 in the Remote Controller.

27.3.4 Remote Transmitter and Local Receiver Setup

The initialization of the Remote Controller’s transmitter and the Local Controller’s receiver can be done by data frames sent by the local transmitter. Therefore, the Remote Controller’s receiver has to be able to receive frames (the port structure has to be set up accordingly).

- The Remote Window of pipe x (x can be freely chosen) has to be set to the MLI register address range in the Remote Controller. The initialization by data frames is then done via pipe x.
- The automatic mode has to be enabled in the Remote Controller (Command Frame in pipe 2 with CM = 0001_B).
- The connections between the remote transmitter and the local receiver have to be established (if not already done by the default setting), similar to **Section 27.3.2**.
- The remote transmitter has to be enabled, similar procedure as for the local transmitter. The data word to be written to the Remote Controller’s MLI registers have to be written to the corresponding address in the local Transfer Window of pipe x.
- The local receiver can then be configured by writing the appropriate data (similar scenario as for the remote receiver) to the local Transfer Window of pipe x.
- A possibility to test the complete setup is the remote loop back. In this case another Remote Window is overlaid directly to a Transfer Window in the Remote Controller. Writing data to the corresponding Transfer Window in the Local Controller leads to a data frame sent to the Remote Controller. There, the received data is written to the

Transfer Window and a new data frame is sent back to the Local Controller. The MLI move engine in the Local Controller's receiver can be used to write the received data to a defined location, e.g. to a memory location. Test software in the Local Controller can check for correct setup, data consistency, MLI event handling, and correct address handling in the Local and the Remote Controllers.

27.3.5 Delay Adjustment

The local MLI transmitter is measuring the number of TCLK clock cycles between TVALID becoming 0 after a transmission and TREADY becoming 1 again. This time represents the overall loop delay of the MLI connection. The loop delay is the time used for signal propagation, input/output driver delay and remote receiver reaction. For example, with slow drivers and a high load (due to long wires, etc.), the signals take a longer time to propagate from the local transmitter to the remote receiver and back again (READY-VALID control handshake). This delay (also visible when TVALID becomes 1 at the beginning of a frame) limits the maximum baud rate of an MLI connection, because the answer of the receiver has to be detected by the transmitter with TREADY = 0 at the end of the frame. The value measured after the end of the frame is indicated in bit field TSTATR.RDC.

The receiver participates in the control handshake by changing its RREADY output as a reaction to an incoming RVALID signal. For the transmitter, the TREADY input delivers the information that a receiver is connected and that it is ready for reception (transfer only starts if TREADY = 1). If a receiver is not able to handle the data or is not connected, the TREADY line will not become low after TVALID becomes 1 (Non-Acknowledge).

In addition to this information, the MLI protocol offers the possibility to use the control handshake also to indicate that the receiver has detected a parity error in the received frame. If a correct frame has been received, the receiver immediately asserts RREADY = 1 after the reception of a frame when detecting RVALID = 0. If the receiver has detected a parity error, it waits for a programmable number of RCLK cycles before setting RREADY = 1 again. This additional delay is defined by bit field RCR.DPE.

The transmitter measuring the delay and comparing it to a programmed value, it can detect that the receiver has signaled a parity error by introducing the additional delay. The compare value for the transmitter is programmed by bit field TCR.MDP. A measured value of TSTATR.RDC above TCR.MDP is interpreted as parity error by the transmitter (for parity error handling refer to **Page 27-44**).

In the receiver, frames with parity error are ignored for data transfers and don't lead to internal move actions.

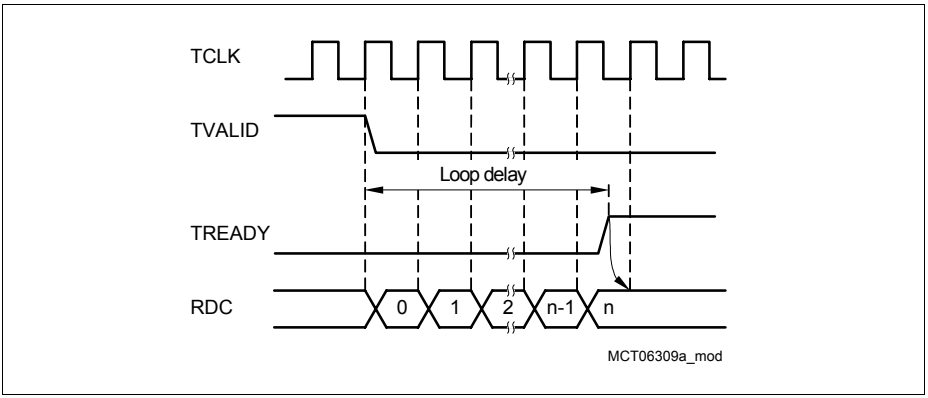


Figure 27-50 Loop Delay Measurement

To adjust the generated parity delay in the local transmitter and in the remote receiver, the following steps are necessary:

- Send a dummy frame to the receiver for measuring the loop delay. This frame should not lead to internal data move actions in the receiver, so a parity error can be simulated in the transmitter. The receiver has a fixed even parity scheme, whereas the transmitter can be programmed either for even or for odd parity. Programming odd parity before sending a frame will generate a (dummy) frame that will be discarded by the receiver (assuming a correct transfer). For a dummy frame, it is recommended to use a data frame with disabled Automatic Data Mode in the receiver (RCR.MOD = 0).
- The receiver delay RCR.DPE being 0 after a module reset, the transmitter can measure the loop delay and the receiver discards the frame (without modification of DPE, there is no difference in time between a frame with or without a parity error having been detected). The value given by TSTATR.RDC indicates how many TCLK cycles are necessary for a control handshake. This value should be incremented by a value DELTA (value see below) and written to TCR.MDP.
- The transmitter parity has to be programmed to even parity to be able to generate frames that are not discarded by the receiver.
- Programming the receiver delay for parity error (RCR.DPE) to a value bigger than DELTA will lead to a value of TSTATR.RDC bigger than TCR.MDP if the receiver detects a parity error. The value of DPE in the remote receiver is modified by the local transmitter by sending a Command Frame in pipe 1 with the desired value. The difference between TSTATR.RDC and TCR.MDP allows a certain timing tolerance between local transmitter and remote receiver.
- The value of DELTA depends on the possible variations of the propagation characteristics of the MLI connection. If the environment does not significantly change, DELTA can be 1. For systems with variations, DELTA could be bigger. The

user can check about changing propagation characteristics by reading TSTATR.RDC from time to time and to check if it is constant for correct transfers. If it changes, either a bigger DELTA value can be applied, or the delay adjustment can be repeated, adapting to the new circumstances.

27.3.6 Connection to DMA Mechanism

The MLI module supports the connection to a DMA (direct memory access) mechanism. This mechanism allows the transfer of blocks of data of programmable size via an MLI connection without CPU intervention. Therefore, a DMA mechanism can be used in the Local Controller to write the desired number of data words one after the other to the corresponding MLI Transfer Window. The address ranges of the data blocks and their length has to be handled by the DMA module.

An MLI pipe supporting only one pending Write Frame request at a time, the DMA has to wait until the pipe is capable to handle new data before writing another data word to the Transfer Window. Therefore, the Normal Frame sent events of the pipes can trigger DMA data transfers. Depending on the connection of the MLI module's service request outputs SRx to the DMA trigger inputs, the Normal Frame sent events have to be enabled for service request activation and directed to the desired SRx outputs. It is recommended to use only one type of MLI event per SRx output to trigger a data transfer by DMA. If the DMA mechanism needs a start trigger for the first data word transfer, register GINTR can be written with the appropriate pattern to activate an SRx output.

27.3.7 Connection of MLI to SPI

The handshake signals between a transmitter and a receiver are based on a synchronous transfer protocol. In the SPI protocol, the shift clock and the data signal are equivalent to CLK and DATA. In case of an 4-wire SPI, the slave select signal represents the VALID signal (the leading and the trailing delay have to be set up accordingly).

Contrary to the MLI, in the SPI protocol, a complete control handshake is not defined, so the READY signal does not exist in SPI modules. As a result, the SPI communication does not check by hardware for correct data transfer, but has to handle this on an upper software layer. If using an SPI module for communication with an MLI transmitter or an MLI receiver, the READY signal has to be handled by software or the handshake has to be given up. This can be done by connecting the TVALID signal of an MLI transmitter to one of its own TREADY inputs with polarity inversion. Like this, the TREADY input directly following the inverted TVALID signal, the parity error indication and the Non-Acknowledge error detection are not possible.

Furthermore, in the MLI protocol, the frames may have a different width, depending on their type and selected buffer size. The different numbers of data bits per frame have also to be handled by the SPI module. In order to minimize the number of different frames, it is recommended to restrict the possibility to program different buffer sizes, the use of Read Frames or Command Frames. In order to simplify the data handling by an

SPI module, the parity generation could be skipped for frames received by the SPI module and an error detection mechanism on an upper software layer could be implemented. For frames sent by an SPI module, the parity bit has to be calculated and sent correctly. Otherwise, the MLI receiver will discard the received frame.

27.4 MLI Kernel Registers

This section describes the kernel registers of the MLI module. All registers can be accessed with 8-bit, 16-bit or 32-bit write or read operations. Accesses to address locations inside the MLI address range not targeting the indicated registers are not allowed. The complete and detailed address map of the of the MLI module and its registers is described in **Table 27-14** on **Page 27-139**.

All registers in the MLI address spaces are reset with the application reset.

MLI Kernel Register Overview

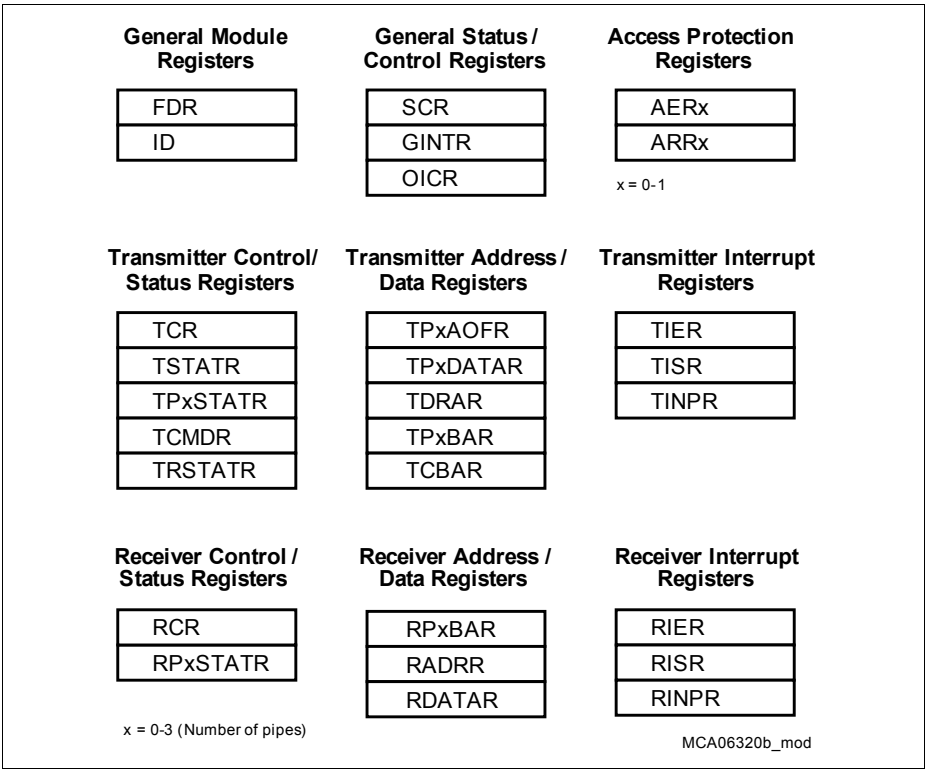


Figure 27-51 MLI Kernel Registers

Table 27-9 Registers Address Space - MLI Kernel Registers

Module	Base Address	End Address	Note
MLI0	$F010\ C000_H$	$F010\ C0FF_H$	–
MLI1	$F010\ C100_H$	$F010\ C1FF_H$	–

Table 27-10 Registers Overview - MLI Kernel Registers

Register Short Name	Register Long Name	Offset Address[1)]	Description see
ID	Module Identification Register	08_H	Page 27-82
FDR	Fractional Divider Register	$0C_H$	Page 27-79
TCR	Transmitter Control Register	10_H	Page 27-92
TSTATR	Transmitter Status Register	14_H	Page 27-95
TPxSTATR	Transmitter Pipe x Status Register	18_H + (x * 4)	Page 27-97
TCMDR	Transmitter Command Register	28_H	Page 27-99
TRSTATR	Transmitter Receiver Status Register	$2C_H$	Page 27-101
TPxAOFR	Transmitter Pipe x Address Offset Register	30_H + (x * 4)	Page 27-103
TPxDATAR	Transmitter Pipe x Data Register	40_H + (x * 4)	Page 27-104
TDRAR	Transmitter Data Read Answer Register	50_H	Page 27-104
TPxBAR	Transmitter Pipe x Base Address Register	54_H + (x * 4)	Page 27-105
TCBAR	Transmitter Copy Base Address Register	64_H	Page 27-106
RCR	Receiver Control Register	68_H	Page 27-113
RPxBAR	Receiver Pipe x Base Address Register	$6C_H$ + (x * 4)	Page 27-117
RPxSTATR	Receiver Pipe x Status Register	$7C_H$ + (x * 4)	Page 27-116
RADDR	Receiver Address Register	$8C_H$	Page 27-118
RDATAR	Receiver Data Register	90_H	Page 27-119
SCR	Set Clear Register	94_H	Page 27-84
TIER	Transmitter Interrupt Enable Register	98_H	Page 27-107
TISR	Transmitter Interrupt Status Register	$9C_H$	Page 27-109
TINPR	Transmitter Interrupt Node Pointer Register	$0A0_H$	Page 27-111
RIER	Receiver Interrupt Enable Register	$A4_H$	Page 27-120
RISR	Receiver Interrupt Status Register	$A8_H$	Page 27-123

Table 27-10 Registers Overview - MLI Kernel Registers (cont'd)

Register Short Name	Register Long Name	Offset Address[1)]	Description see
RINPR	Receiver Interrupt Node Pointer Register	AC_H	Page 27-125
GINTR	Global Interrupt Set Register	$B0_H$	Page 27-83
OICR	Output Input Control Register	$B4_H$	Page 27-86
AER0	Access Enable Register 0	$B8_H$	Page 27-90
ARR0	Access Range Register 0	BC_H	Page 27-91
AER1	Access Enable Register 1	$C0_H$	Page 27-90
ARR1	Access Range Register 1	$C4_H$	Page 27-91

1) The absolute register address is calculated as follows:
Module Base Address (Table 27-9) + Offset Address (shown in this column)

27.4.1 General Module Registers

Fractional Divider Register

The fractional divider register allows to program the frequency f_{MLI} to generate the baud rate of the of the 50% duty cycle transmitter shift clock TCLK.

FDR
Fractional Divider Register **($0C_H$)** **Reset Value: $03FF\ 43FF_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DISCLK	ENHW	SUSREQ	SUSACK	0		RESULT									
rwh	rw	rh	rh	r		rh									

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DM		SC		SM	0	STEP									
rw		rw		rw	r	rw									

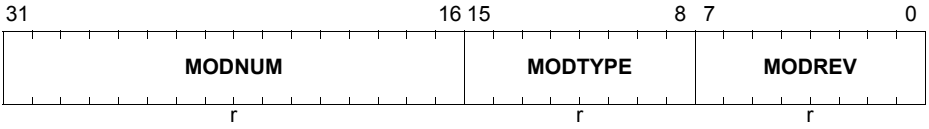
Field	Bits	Type	Description
STEP	[9:0]	rw	**Step Value** In normal divider mode STEP contains the reload value for RESULT. In fractional divider mode this bit field defines the 10-bit value that is added to the RESULT with each input clock cycle.
SM	11	rw	**Suspend Mode** SM selects between granted or immediate suspend mode. This bit is only taken into account in devices supporting suspend mode. 0_B Granted suspend mode selected 1_B Immediate suspend mode selected
SC	[13:12]	rw	**Suspend Control** This bit field defines the behavior of the fractional divider in suspend mode (bit SUSREQ and SUSACK set). This bit field is only taken into account in devices supporting suspend mode. 01_B Clock generation is stopped and the clock output signals are not generated. RESULT is not changed except when writing bit field DM with 01_B or 10_B. 00_B Clock generation continues. 10_B Clock generation is stopped and the clock output signals are not generated. RESULT is loaded with $3FF_H$. 11_B Same as SC = 10_B but RST_EXT_DIV is 1 (independently of bit field DM).
DM	[15:14]	rw	**Divider Mode** This bit fields defines the functionality of the fractional divider block. 00_B Fractional divider is switched off; no output clock is generated. RST_EXT_DIV is 1. RESULT is not updated (default after reset). 01_B Normal divider mode selected. 10_B Fractional divider mode selected. 11_B Fractional divider is switched off; no output clock is generated. RESULT is not updated.

Field	Bits	Type	Description
RESULT	[25:16]	rh	**Result Value** In normal divider mode RESULT acts as reload counter (addition +1). In fractional divider mode this bit field contains the result of the addition RESULT+STEP. If DM is written with 01_B or 10_B, RESULT is loaded with $3FF_H$.
SUSACK	28	rh	**Suspend Mode Acknowledge** 0_B Suspend mode is not acknowledged. 1_B Suspend mode is acknowledged. Suspend mode is entered when SUSACK and SUSREQ are set.
SUSREQ	29	rh	**Suspend Mode Request** 0_B Suspend mode is not requested. 1_B Suspend mode is requested. Suspend mode is entered when SUSACK and SUSREQ are set.
ENHW	30	rw	**Enable Hardware Clock Control** 0_B Bit DISCLK cannot be cleared by hardware by a high level at input signal ECEN. 1_B Bit DISCLK is cleared by hardware while input signal ECEN is at high level.
DISCLK	31	rwh	**Disable Clock** 0_B Clock generation of $f_{OUT} = f_{MLI}$ is enabled according to the setting of bit field DM. 1_B Fractional divider is stopped. Signal $f_{OUT} = f_{MLI}$ becomes inactive. No change except when writing bit field DM. In case of a conflict between hardware reset and software set of DISCLK, the software set wins. Any write or read-modify-write action leads to the described behavior. As a result read-modify-write operations should be avoided.
0	10, [27:26]	r	**Reserved** Read as 0; should be written with 0.

Module Identification Register

The MLI Module Identification Register ID contains read-only information about the module version.

ID
Module Identification Register **(08_H)** **Reset Value: 0025 C0XX$_H$**



Field	Bits	Type	Description
MODREV	[7:0]	r	**Module Revision Number** This bit field defines the module revision number. The value of a module revision starts with 01_H (first revision).
MODTYPE	[15:8]	r	**Module Type** This bit field defines the module as a 32-bit module: $C0_H$
MODNUM	[31:16]	r	**Module Number Value** This bit field defines the module identification number for the MLI: 0025_H

27.4.2 General Status/Control Registers

Global Interrupt Set Register

The Global Interrupt Set Register GINTR is a write only register (always reads 0) that allows each of the service request outputs SRx to be activated under software control (see **Page 27-58**).

GINTR
Global Interrupt Set Register **($B0_H$)** **Reset Value: 0000 0000$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0								SI MLI7	SI MLI6	SI MLI5	SI MLI4	SI MLI3	SI MLI2	SI MLI1	SI MLI0
r								w	w	w	w	w	w	w	w

Field	Bits	Type	Description
SIMLIx (x = 0-7)	x	w	**Set MLI Service Request Output Line x** 0_B No action 1_B Service request output SRx is activated (pulse).
0	[31:8]	r	**Reserved** Read as 0; should be written with 0.

Set Clear Register

The Set Clear Register SCR is a write only register that makes it possible to set or clear by software several status flags located in registers TSTATR, TRSTATR and RCR. Reading register SCR always returns zeros at all bit locations. Bits that are not written with a 1 have no effect.

SCR
Set Clear Register **(94_H)** **Reset Value: $0000\ 0000_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
C CIV3	C CIV2	C CIV1	C CIV0	C NAE	C TPE	C RPE	C AV	0						C BAV	C MOD
w	w	w	w	w	w	w	w	w						w	w

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C CV3	C CV2	C CV1	C CV0	C DV3	C DV2	C DV1	C DV0	0			S MOD	S CV3	S CV2	S CV1	S CV0
w	w	w	w	w	w	w	w	w			w	w	w	w	w

Field	Bits	Type	Description
SCV0, **SCV1,** **SCV2,** **SCV3**	0, 1, 2, 3	w	**Set Command Valid** 0_B No effect 1_B Bit TRSTATR.CVx is set.
SMOD	4	w	**Set MOD Flag** 0_B No effect 1_B If CMOD = 0, RCR is set. If CMOD = 1, RCR.MOD is cleared.
CDV0, **CDV1,** **CDV2,** **CDV3**	8, 9, 10, 11	w	**Clear Data Valid x Flag** 0_B No effect 1_B Bits TRSTATR.DVx and TRSTATR.RPx are cleared.
CCV0, **CCV1,** **CCV2,** **CCV3**	12, 13, 14, 15	w	**Clear Command Valid x Flag** 0_B No effect. 1_B If SCVx = 0, bit TRSTATR.CVx is cleared. If SCVx = 1, bit TRSTATR.CVx is set.
CMOD	16	w	**Clear MOD Flag** 0_B No effect. 1_B Bit RCR.MOD is cleared.

Field	Bits	Type	Description
CBAV	17	w	**Clear BAV Flag** 0_B No effect. 1_B Bit TRSTATR.BAV is cleared.
CAV	24	w	**Clear AV Flag** 0_B No effect. 1_B Bit TRSTATR.AV is cleared.
CRPE	25	w	**Clear Receiver PE Flag** 0_B No effect. 1_B Bit RCR.PE is cleared.
CTPE	26	w	**Clear Transmitter PE Flag** 0_B No effect. 1_B Bit TSTATR.PE is cleared.
CNAE	27	w	**Clear NAE Flag** 0_B No effect. 1_B Bit TSTATR.NAE is cleared.
CCIV0, **CCIV1,** **CCIV2,** **CCIV3**	28, 29, 30, 31	w	**Clear Command Interrupt Valid x Flag** 0_B No effect. 1_B Bit TSTATR.CIVx is cleared.
0	[7:5], [23:18]	w	**Reserved** Read as 0; should be written with 0.

Output Input Control Register

The Output Input Control Register OICR determines the functionality of the MLI transmitter and MLI receiver I/O control logic. The bits in this register are automatically overwritten after a reset with a value given in the implementation chapter (see). Furthermore, the connection table of the MLI module signals is given there.

Note: The value of register OICR should not be modified while a data transfer (reception or transmission) is ongoing (bits in OICR directly control the I/O signal paths).

OICR
Output Input Control Register ($B4_H$) Reset Value: 1000 8000$_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RDP	RDS		RCE	RCP	RCS		RVP	RVS		RRP D	RRP C	RRP B	RRP A	RRS	
rw	rw		rw	rw	rw		rw	rw		rw	rw	rw	rw	rw	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RVE	TDP	TCP	TCE	TRE	TRP	TRS		TVP D	TVP C	TVP B	TVP A	TVE D	TVE C	TVE B	TVE A
rw	rw	rw	rw	rw	rw	rw		rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
TVEA, TVEB, TVEC, TVED	0, 1, 2, 3	rw	**Transmitter Valid Enable** These bits enable the module kernel output signals TVALIDx (x = A, B, C, D) to be driven by MLI transmitter output signal TVALID. 0_B TVALIDx is disabled and remains at passive level (as selected by TVPx). 1_B Transmitter output signal TVALIDx is enabled and driven by TVALID.
TVPA, TVPB, TVPC, TVPD	4, 5, 6, 7	rw	**Transmitter Valid Polarity** These bits determine the polarity of the module kernel transmitter output signals TVALIDx (x = A, B, C, D). 0_B Non-inverted polarity for TVALIDx selected: TVALIDx is passive when driving a 0. TVALIDx is active when driving a 1. 1_B Inverted polarity for TVALIDx selected: TVALIDx is passive when driving a 1. TVALIDx is active when driving a 0.

Field	Bits	Type	Description
TRS	[9:8]	rw	**Transmitter Ready Selection** This bit field determines the module kernel input signal TREADYx (x = A, B, C, D) that is used as MLI transmitter input signal TREADY. 00_B TREADYA is selected. 01_B TREADYB is selected. 10_B TREADYC is selected. 11_B TREADYD is selected.
TRP	10	rw	**Transmitter Ready Polarity** This bit determines the polarity of TREADYx. 0_B Non-inverted polarity for TREADYx selected: TREADYx is passive if 0. TREADYx is active if 1. 1_B Inverted polarity for TREADYx selected: TREADYx is passive if 1. TREADY is active if 0.
TRE	11	rw	**Transmitter Ready Enable** This bit enables the MLI transmitter input signal TREADY. 0_B TREADY signal is disabled (always at 0 level). 1_B TREADY signal is enabled and driven by TREADYx according to the settings of TRS and TRP.
TCE	12	rw	**Transmitter Clock Enable** This bit enables the module kernel output signal TCLK. 0_B TCLK is disabled and remains at passive level (as selected by TCP). 1_B TCLK is enabled and driven according to the setting of TCP.
TCP	13	rw	**Transmitter Clock Polarity** This bit determines the polarity of the module kernel output clock signal TCLK. 0_B Non-inverted polarity for TCLK selected: TCLK is driving a 0 when it is passive. 1_B Inverted polarity for TCLK selected: TCLK is driving a 1 when it is passive.

Field	Bits	Type	Description
TDP	14	rw	**Transmitter Data Polarity** This bit determines the polarity of the module kernel output clock signal TDATA. 0_B TDATA is directly driven by MLI transmitter output signal TDATA (non-inverted). 1_B TDATA is directly driven by the inverted MLI transmitter output signal TDATA.
RVE	15	rw	**Receiver Valid Enable** This bit enables the MLI receiver input signal RVALID. 0_B RVALID signal is disabled (always at 0 level). 1_B RVALID signal is enabled and driven by RVALIDx according to the settings of RVS and RVP (default after reset).
RRS	[17:16]	rw	**Receiver Ready Selector** This bit field determines the module kernel output signal RREADYx (x = A, B, C, D) that is driven by the MLI receiver output signal RREADY. The RREADYx output signals that are not selected drives a passive level according to the setting of RRPx. 00_B RREADYA is selected. 01_B RREADYB is selected. 10_B RREADYC is selected. 11_B RREADYD is selected.
RRPA, RRPB, RRPC, RRPD	18, 19, 20, 21	rw	**Receiver Ready Polarity** These bits determine the polarity of the module kernel receiver output signals RREADYx (x = A, B, C, D). 0_B Non-inverted polarity for RREADYx selected: RREADYx is passive if 0. RREADYx is active if 1. 1_B Inverted polarity for RREADYx selected: RREADYx is passive if 1. RREADYx is active if 0.
RVS	[23:22]	rw	**Receiver Valid Selector** This bit field determines the module kernel input signal RVALIDx (x = A, B, C, D) that is used as MLI receiver input signal RVALID. 00_B RVALIDA is selected. 01_B RVALIDB is selected. 10_B RVALIDC is selected. 11_B RVALIDD is selected.

Field	Bits	Type	Description
RVP	24	rw	**Receiver Valid Polarity** This bit determines the polarity of RVALIDx. 0_B Non-inverted polarity for RVALIDx selected: RVALIDx is passive if 0. RVALIDx is active if 1. 1_B Inverted polarity for RVALIDx selected: RVALIDx is passive if 1. RVALIDx is active if 0.
RCS	[26:25]	rw	**Receiver Clock Selector** This bit field determines the module kernel input signal RCLKx (x = A, B, C, D) that is used as MLI receiver input clock CLK. 00_B RCLKA is selected. 01_B RCLKB is selected. 10_B RCLKC is selected. 11_B RCLKD is selected.
RCP	27	rw	**Receiver Clock Polarity** This bit determines the polarity of RCLKx. 0_B Non-inverted polarity for RCLKx selected: RCLKx is at 0 level in passive state. 1_B Inverted polarity for TCLK selected: RCLKx is at 1 level in passive state.
RCE	28	rw	**Receiver Clock Enable** This bit enables the MLI receiver input clock RCLK. 0_B RCLK signal is disabled (always at 0 level). 1_B RCLK signal is enabled and driven by RCLKx according to the settings of RCS and RCP.
RDS	[30:29]	rw	**Receiver Data Selector** This bit field determines the module kernel input signal RDATAx (x = A, B, C, D) that is used as MLI receiver data input line RDATA. 00_B RDATAA is selected. 01_B RDATAB is selected. 10_B RDATAC is selected. 11_B RDATAD is selected.
RDP	31	rw	**Receiver Data Polarity** This bit determines the polarity of RDATAx. 0_B Non-inverted polarity for RDATAx selected: RDATAx is passive if 0. RDATAx is active if 1. 1_B Inverted polarity for RDATAx selected: RDATAx is passive if 1. RDATAx is active if 0.

27.4.3 Access Protection Registers

Access Enable Register

The Access Enable Register AER enables write and read operations in the corresponding address ranges (x = 0 to 31) in addition to the global move engine enable RCR.MOD. Each address range can be individually enabled or excluded from automatic mode.

Note: Please refer to the implementation chapter for the device specific access protection (see ***Page 27-137****).*

AER0
Access Enable Register 0 **($B8_H$)** **Reset Value: 0000 0000$_H$**
AER1
Access Enable Register 1 **($C0_H$)** **Reset Value: 0000 0000$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
AEN 31	**AEN 30**	**AEN 29**	**AEN 28**	**AEN 27**	**AEN 26**	**AEN 25**	**AEN 24**	**AEN 23**	**AEN 22**	**AEN 21**	**AEN 20**	**AEN 19**	**AEN 18**	**AEN 17**	**AEN 16**
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

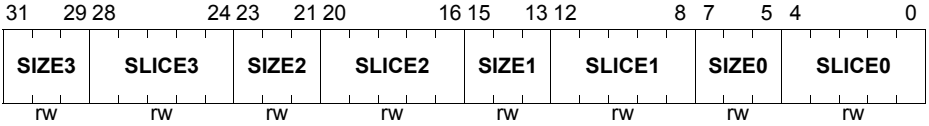
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AEN 15	**AEN 14**	**AEN 13**	**AEN 12**	**AEN 11**	**AEN 10**	**AEN 9**	**AEN 8**	**AEN 7**	**AEN 6**	**AEN 5**	**AEN 4**	**AEN 3**	**AEN 2**	**AEN 1**	**AEN 0**
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
AENx (x = 0-31)	x	rw	**Address Range x Enable** This bit enables the read and write capability of the MLI move engine for address range x (x = 0-31). 0_B Automatic MLI read and write moves to address range x are disabled. Read/write moves to address range x are not executed automatically and an MLI service request can be generated. The receiving controller's software has to take care about the move. 1_B Automatic MLI read and write moves to address range x are enabled if RCR.MOD = 1.

Access Range Register

The Access Range Register ARR determines size and number of the address sub-range n (n = 0-3).

ARR0
Access Range Register 0 **(BC_H)** **Reset Value: 0000 0000$_H$**
ARR1
Access Range Register 1 **($C4_H$)** **Reset Value: 0000 0000$_H$**



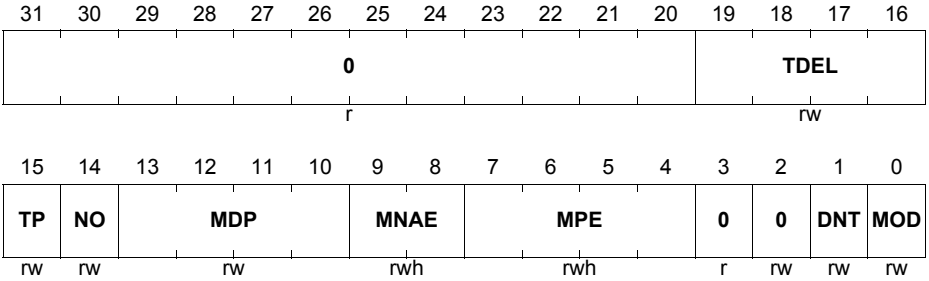
Field	Bits	Type	Description
SLICE0	[4:0]	rw	**Address Slice 0** SLICE0 selects a specific sub-range within address sub-range 0.
SIZE0	[7:5]	rw	**Address Size 0** SIZE0 determines the sub-range size within address sub-range 0.
SLICE1	[12:8]	rw	**Address Slice 1** SLICE1 selects a specific sub-range within address sub-range 1.
SIZE1	[15:13]	rw	**Address Size 1** SIZE1 determines the sub-range size within address sub-range 1.
SLICE2	[20:16]	rw	**Address Slice 2** SLICE2 selects a specific sub-range within address sub-range 2.
SIZE2	[23:21]	rw	**Address Size 2** SIZE2 determines the sub-range size within address sub-range 2.
SLICE3	[28:24]	rw	**Address Slice 3** SLICE3 selects a specific sub-range within address sub-range 3.
SIZE3	[31:29]	rw	**Address Size 3** SIZE3 determines the sub-range size within address sub-range 3.

27.4.4 Transmitter Control/Status Registers

Transmitter Control Register

The Transmitter Control Register TCR includes transmitter related control bits and bit fields that are used for parity/acknowledge, address optimization, TDATA idle polarity, retry, and transmitter enable/disable control.

TCR
Transmitter Control Register (10$_H$) Reset Value: 0000 0110$_H$



Field	Bits	Type	Description
MOD	0	rw	**Mode of Operation** This bit enables the MLI transmitter. 0_B The MLI transmitter is disabled. 1_B The MLI transmitter is enabled.
DNT	1	rw	**Data in Not Transmission** This bit determines the level of the transmitter data line TDATA when no transmission is in progress. 0_B TDATA is at low level if no transmission is running. 1_B TDATA is at high level if no transmission is running.
0	2	rw	**Reserved** Read as 0; should be written with 0.

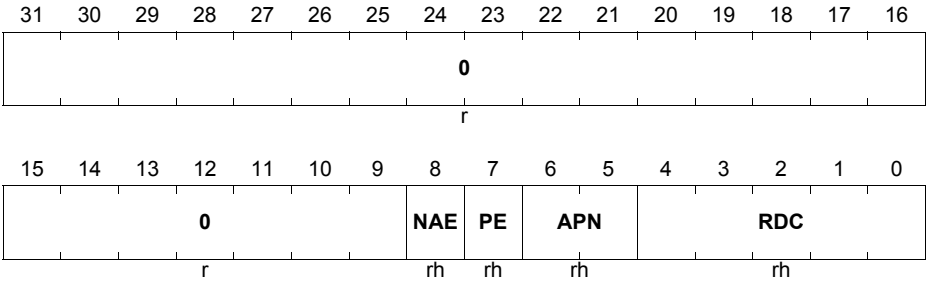
Field	Bits	Type	Description
MPE	[7:4]	rwh	**Maximum Parity Errors** This bit field determines the maximum number of transmitter parity error conditions that can be still detected until a transmitter parity error event is generated (see **Page 27-44**). With each condition detected, MPE is decremented down to 0. 0000_B A parity error event is generated if a transmitter parity error condition is detected. 0001_B A parity error event is generated if a transmitter parity error condition is detected. 0010_B A parity error event is generated if 2 transmitter parity error conditions are detected. 0011_B A parity error event is generated if 3 transmitter parity error conditions are detected. $\ldots_B$ … 1110_B A parity error event is generated if 14 transmitter parity error conditions are detected. 1111_B A parity error event is generated if 15 transmitter parity error conditions are detected.
MNAE	[9:8]	rwh	**Maximum Non Acknowledge Errors** This bit field determines the maximum number of consecutive Non-Acknowledge error conditions that can be still detected in the transmitter until a time-out event is generated. MNAE is decremented down to 0 at each Non-Acknowledge error condition. When MNAE = 0 or becoming 0, a time-out event is generated. MNAE is automatically set to 11_B after a successful frame transmission (see **Page 27-47**). 00_B A time-out event is generated if a non-ack condition is detected. 01_B A time-out event is generated if a non-ack condition is detected. 10_B A time-out event is generated if 2 consecutive non-ack conditions are detected. 11_B A time-out event is generated if 3 consecutive non-ack conditions are detected.

Field	Bits	Type	Description
MDP	[13:10]	rw	**Maximum Delay for Parity Error** This bit field determines a window for the transmitter in number of TCLK clock periods where a TREADY low-to-high signal transition signal is considered as “correctly received” condition (see **Page 27-22**). 0000_B Zero clock periods selected (not useful) 0001_B 1 clock period selected $\cdots_B$ … 1110_B 14 clock periods selected 1111_B 15 clock periods selected
NO	14	rw	**No Optimized Method** This bit field enables/disables the address prediction for read or Write Frames (see **Page 27-47**). 0_B Optimized method (address prediction) enabled. 1_B Optimized method (address prediction) disabled.
TP	15	rw	**Type of Parity** This bit will determines the type of parity used in frame transmissions. For correct data transfers, TP = 0 has to be programmed. The value TP = 1 can be selected to force parity errors to analyze the propagation delay (see **Page 27-26**). 0_B Even parity is selected. 1_B Odd parity selected.
TDEL	[19:16]	rw	**Transmission Delay** This bit field defines a delay in cycles of f_{FPI} of the transmitter between the reception of the rising edge of RREADY and the next possible frame start (see **Page 27-50**). 0000_B No transmission delay selected 0001_B One f_{FPI} cycle delay selected $\cdots_B$ ... 1110_B Fourteen f_{FPI} cycles delay selected 1111_B Fifteen f_{FPI} cycles delay selected
0	3, [31:20]	r	**Reserved** Read as 0; should be written with 0.

Transmitter Status Register

The Transmitter Status Register TSTATR contains transmitter specific status information.

TSTATR
Transmitter Status Register **(14_H)** **Reset Value: 0000 0000_H**



Field	Bits	Type	Description
RDC	[4:0]	rh	**Ready Delay Counter** This bit field counts TCLK periods after the end of a frame transmission. When the TVALID signal goes to low level, RDC is cleared to zero and starts counting up the TCLK clock periods until a TREADY high level is detected (see **Page 27-22**).
APN	[6:5]	rh	**Answer Pipe Number** This bit field is written by the MLI receiver with the Pipe Number of a received Read Frame. APN is used by an Answer Frame that is transmitted as response to the Read Frame. 00_B Pipe 0 is used in Answer Frame. 01_B Pipe 1 is used in Answer Frame. 10_B Pipe 2 is used in Answer Frame. 11_B Pipe 3 is used in Answer Frame.
PE	7	rh	**Parity Error Flag** This bit is set if a transmitter parity error condition is detected by the transmitter after a frame transmission. PE is cleared by hardware when a frame has been transmitted without a parity error (see **Page 27-44**). Bit PE can be cleared by software via bit SCR.CTPE.

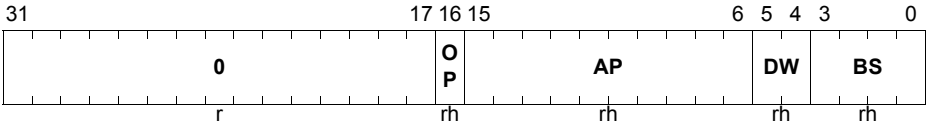
Field	Bits	Type	Description
NAE	8	rh	**Non Acknowledge Error Flag** This bit is set when a Non-Acknowledge error condition is detected by the MLI transmitter after a frame transmission (see **Page 27-47**). NAE is cleared by hardware if a transmitted frame has been acknowledged correctly. Bit NAE can be cleared by software via bit SCR.CNAE.
0	[31:9]	r	**Reserved** Read as 0; should be written with 0.

Transmitter Pipe x Status Registers

The Transmitter Pipe x Status Registers TPxSTATR contain pipe-specific status information related to address optimization and prediction, data width for transmit data, and Remote Window size.

TPxSTATR (x = 0-3)
Transmitter Pipe x Status Register

(18_H+4_H*x) **Reset Value: 0000 0000_H**



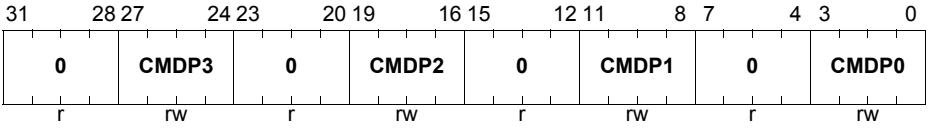
Field	Bits	Type	Description
BS	[3:0]	rh	**Buffer Size** This bit field indicates the coded buffer size of the pipe x Remote Window in the receiving controller. BS further determines how many address offset bits are transmitted in a Write Offset and Data Frame or in a Discrete Read Frame. When register TPxBAR is written for generation of a Copy Base Address Frame, BS is updated by the Copy Base Address Frame (see Page 27-28). 0000_B 1-bit offset address of Remote Window 0001_B 2-bit offset address of Remote Window 0010_B 3-bit offset address of Remote Window $\cdots_B$ ... 1110_B 15-bit offset address of Remote Window 1111_B 16-bit offset address of Remote Window
DW	[5:4]	rh	**Data Width** This bit field indicates the data width that has been detected for a read or write access of a bus master to a Transfer Window of pipe x (see Page 27-30 and Page 27-34). 00_B 8-bit data width detected 01_B 16-bit data width detected 10_B 32-bit data width detected 11_B Reserved

Field	Bits	Type	Description
AP	[15:6]	rh	**Address Prediction Factor** This bit field indicates the delta value (positive or negative number) of offset address used by the MLI transmitter for the next address prediction. AP is a signed 9-bit number (10th bit is the sign bit) that is written with each transmitter address prediction calculation (see **Page 27-26** and **Page 27-47**).
OP	16	rh	**Use Optimized Frame** When address optimization is enabled with TCR.NO = 0, this bit indicates if address prediction is possible in the transmitter. OP is written with each transmitter address prediction calculation (see **Page 27-26** and **Page 27-47**). 0_B No address prediction is possible. A Write Offset and Data Frame or a Discrete Read Frame are used for transmission. 1_B Address prediction is possible. An Optimized Write Frame or an Optimized Read Frame are used for transmission.
0	[31:17]	r	**Reserved** Read as 0; should be written with 0.

Transmitter Command Register

The Transmitter Command Register TCMDR contains the command codes that are used during Command Frame transmission (see **Page 27-41**). Each time one of the CMDPx bit fields is written, a Command Frame transmission is triggered. Independent of the transferred command code value, a Command Frame transmitted event can be generated in the transmitter for each pipe and a Command Frame received event for each pipe in the receiver, respectively.

TCMDR
Transmitter Command Register (28$_H$) Reset Value: 0000 0000$_H$



Field	Bits	Type	Description
CMDP0	[3:0]	rw	**Command Code for Pipe 0** This bit field contains the command code related to pipe 0. The pipe 0 command codes allow an activation (pulse) of one of the service request outputs SR[3:0] in the receiving controller. 0001_B Activate SR0 0010_B Activate SR1 0011_B Activate SR2 0100_B Activate SR3 Other bit combinations are reserved for future use; no further action in the receiver.
CMDP1	[11:8]	rw	**Command Code for Pipe 1** This bit field contains the command code related to pipe 1. The pipe 1 command codes allow to adjust the receiver delay for the parity error condition (see RCR.DPE) in the MLI receiver of the receiving controller. 0000_B Set RCR.DPE = 0000_B 0001_B Set RCR.DPE = 0001_B $\cdots_B$ ... 1110_B Set RCR.DPE = 1110_B 1111_B Set RCR.DPE = 1111_B

Field	Bits	Type	Description
CMDP2	[19:16]	rw	**Command Code for Pipe 2** This bit field contains the command code related to pipe 2. The pipe 2 command codes allow to control the MLI receiver in the receiving controller. 0001_B Enable Automatic Data Mode (RCR.MOD = 1) 0010_B Disable Automatic Data Mode (RCR.MOD = 0) 0100_B Clear bit TRSTATR.RP0 0101_B Clear bit TRSTATR.RP1 0110_B Clear bit TRSTATR.RP2 0111_B Clear bit TRSTATR.RP3 1111_B Activate a pulse at $\overline{\text{BRKOUT}}$ Other bit combinations are reserved for future use; no further action in the receiver.
CMDP3	[27:24]	rw	**Command Code for Pipe 3** This bit field contains the command code related to pipe 3. The command codes for pipe 3 are free programmable by software.
0	[7:4], [15:12], [23:20], [31:28]	r	**Reserved** Read as 0; should be written with 0.

Transmitter-Receiver Status Register

The Transmitter Receiver Status Register TRSTATR contains read-only flags that indicate the status of MLI operations.

TRSTATR
Transmitter Receiver Status Register

($2C_H$) **Reset Value: 0000 0000$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0						PN		RP3	RP2	RP1	RP0	DV3	DV2	DV1	DV0
r						rh		rh	rh	rh	rh	rh	rh	rh	rh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0						BAV	AV	CV3	CV2	CV1	CV0	CIV3	CIV2	CIV1	CIV0
r						rh	rh	rh	rh	rh	rh	rh	rh	rh	rh

Field	Bits	Type	Description
CIV0, **CIV1,** **CIV2,** **CIV3**	0, 1, 2, 3	rh	**Command Interrupt Valid** Bit is set to 1 by the MLI transmitter whenever it detects a rising edge at the corresponding TRx input line (for Triggered Command Frames in pipe 0). It is cleared by hardware when the Command Frame has been correctly transmitted. CIVx can be cleared by software via bit SCR.CCIVx.
CV0, **CV1,** **CV2,** **CV3**	4, 5, 6, 7	rh	**Command Valid** Bit is set by hardware when a TCMDR.CMDPx bit field is written. It is cleared by hardware when the Command Frame has been correctly transmitted. CVx can be set or cleared by software via bits SCR.SCVx or SCR.CCVx.
AV	8	rh	**Answer Valid** Bit is set by hardware when the TDRAR register in the the MLI transmitter (in the Remote Controller) is written. AV is cleared by hardware when the Answer Frame has been correctly sent. AV can be cleared by software via bit SCR.CAV.

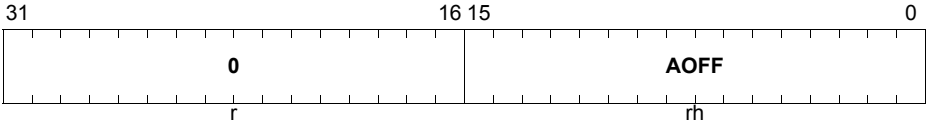
Field	Bits	Type	Description
BAV	9	rh	**Base Address Valid** Bit is set by hardware when the TCBAR register in the MLI transmitter is written. BAV is cleared by hardware when the Copy Base Address Frame has been correctly sent. BAV can be cleared by software via bit SCR.CBAV.
DV0, **DV1,** **DV2,** **DV3**	16, 17, 18, 19	rh	**Data Valid** Bit is set by hardware when the TPxDATAR and/or the TPxAOFR registers of the MLI transmitter are updated after a read or write access to a Transfer Window of pipe x. DVx is cleared again by hardware when the read or Write Frame has been correctly sent. DVx can be cleared by software via bit SCR.CDVx.
RP0, **RP1,** **RP2,** **RP3**	20, 21, 22, 23	rh	**Read Pending** Bit is set by hardware when the TPxAOFR register of the MLI transmitter is updated after a read access to a Transfer Window of pipe x. RPx is cleared by hardware when the MLI receiver in the Local Controller receives an Answer Frame for pipe x from the Remote Controller. RPx can be cleared by software via bit SCR.CDVx.
PN	[25:24]	rh	**Pipe Number** This bit field indicates the Pipe Number x of the base address that has been written into register TPxBAR. 00_B TP0BAR has been last written. 01_B TP1BAR has been last written. 10_B TP2BAR has been last written. 11_B TP3BAR has been last written.
0	[15:10], [31:26]	r	**Reserved** Read as 0; should be written with 0.

27.4.5 Transmitter Pipe x Address Offset Register

Transmitter Pipe x Address Offset Register

The Transmitter Pipe x Address Offset Register TPxAOFR is a read-only register that stores the offset address that has been used by the last read or write access to a Transfer Window of pipe x.

TPxAOFR (x = 0-3)
Transmitter Pipe x Address Offset Register
(30_H+4_H*x) **Reset Value: 0000 0000_H**

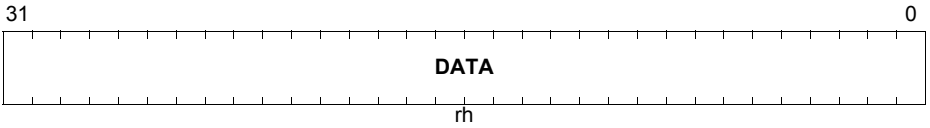


Field	Bits	Type	Description
AOFF	[15:0]	rh	**Address Offset** Whenever a location within a Transfer Window is accessed (read or written) AOFF is loaded with the lowest 16 address bits of the access. Also in the case of a small Transfer Window access, all AOFF bits are loaded, but AOFF[15:13] are not taken into account for further actions assuming the buffer size is configured correctly (see **Page 27-105**).
0	[31:16]	r	**Reserved** Read as 0; should be written with 0.

Transmitter Pipe x Data Register

The Transmitter Pipe x Data Register TPxDATAR is a read-only register that stores the data that has been written during the last write access to a Transfer Window of pipe x.

TPxDATAR (x = 0-3)
Transmitter Pipe x Data Register (40_H+4_H*x) Reset Value: 0000 0000$_H$

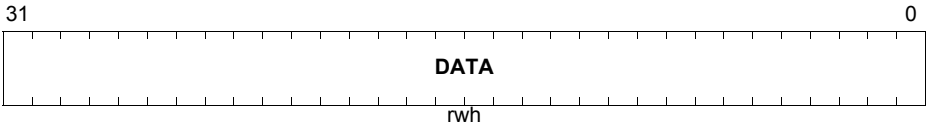


Field	Bits	Type	Description
DATA	[31:0]	rh	**Data** Whenever a location within a Transfer Window is written, the data is loaded in this bit field.

Transmitter Data Read Answer Register

The Transmitter Data Read Answer Register TDRAR contains the read data for the transmission of an Answer Frame.

TDRAR
Transmitter Data Read Answer Register
(50_H) Reset Value: 0000 0000$_H$

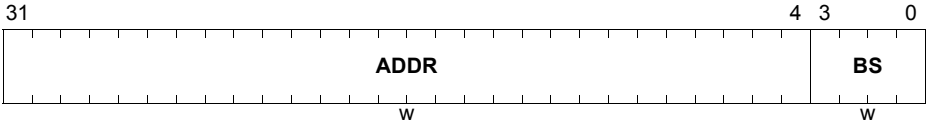


Field	Bits	Type	Description
DATA	[31:0]	rwh	**Data** This bit field is loaded with data that is read from the address requested by a Read Frame. An update of this bit field triggers the start of an Answer Frame with DATA used as content of the Answer Frame. This bit field can be updated either automatically by the move engine (if Automatic Data Mode is enabled) or by the CPU (if Automatic Data Mode is disabled).

Transmitter Pipe x Base Address Register

The write-only Transmitter Pipe x Base Address Register TPxBAR represents the 28-bit pipe x Remote Window base address and the Remote Window size that is transmitted to the receiving controller via a Copy Base Address Frame.

TPxBAR (x = 0-3)
Transmitter Pipe x Base Address Register
(54_H+4_H*x) **Reset Value: 0000 0000_H**

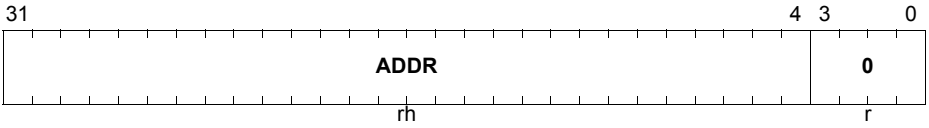


Field	Bits	Type	Description
BS	[3:0]	w	**Buffer Size** This bit field determines the coded buffer size of the pipe x Remote Window in the receiving controller. When writing TPxBAR, BS is copied into bit field TPxSTATR.BS. 0000_B 1-bit offset address of Remote Window 0001_B 2-bit offset address of Remote Window 0010_B 3-bit offset address of Remote Window $...{}_B$ ... 1101_B 14-bit offset address of Remote Window 1110_B 15-bit offset address of Remote Window 1111_B 16-bit offset address of Remote Window Do not use the coding values 1101_B, 1110_B, and 1111_B as buffer size for Small Transfer Windows.
ADDR	[31:4]	w	**Address** This bit field determines the most significant 28 bits of the pipe x Remote Window base address. When writing TPxBAR, ADDR is copied into bit field TCBAR.ADDR[31:4].

Transmitter Copy Base Address Register

The Transmitter Copy Base Address Register TCBAR contains the 28-bit pipe x Remote Window base address of the latest write access to TPxBAR.ADDR.

TCBAR
Transmitter Copy Base Address Register
(64_H) **Reset Value: 0000 0000$_H$**



Field	Bits	Type	Description
ADDR	[31:4]	rh	**Address** This bit field contains the 28 address bits written to TPxBAR.ADDR. This value will be transferred to the receiving controller to define the base address of the Remote Window for pipe x.
0	[3:0]	r	**Reserved** Read as 0; should be written with 0.

27.4.6 Transmitter Interrupt Registers

Transmitter Interrupt Enable Register

The Transmitter Interrupt Enable Register TIER contains the interrupt enable bits and the clear bits for all transmitter events. The bits marked w always read as 0.

TIER
Transmitter Interrupt Enable Register (98_H) **Reset Value: $0000\ 0000_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0						TEIR	PEIR	CFSIR3	CFSIR2	CFSIR1	CFSIR0	NFSIR3	NFSIR2	NFSIR1	NFSIR0
r						w	w	w	w	w	w	w	w	w	w

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0						TEIE	PEIE	CFSIE3	CFSIE2	CFSIE1	CFSIE0	NFSIE3	NFSIE2	NFSIE1	NFSIE0
r						rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
NFSIE0, **NFSIE1,** **NFSIE2,** **NFSIE3**	0, 1, 2, 3	rw	**Normal Frame Sent in Pipe x Interrupt Enable** 0_B Normal frame sent in pipe x event is disabled for activation of an SRx line. 1_B Normal frame sent in pipe x event is enabled for activation of an SRx line.
CFSIE0, **CFSIE1,** **CFSIE2,** **CFSIE3**	4, 5, 6, 7	rw	**Command Frame Sent in Pipe x Interrupt Enable** 0_B Command frame sent in pipe x event is disabled for activation of an SRx line. 1_B Command frame sent in pipe x event is enabled for activation of an SRx line.
PEIE	8	rw	**Parity Error Interrupt Enable** 0_B Parity error event is disabled for activation of an SRx line. 1_B Parity error event is enabled for activation of an SRx line.

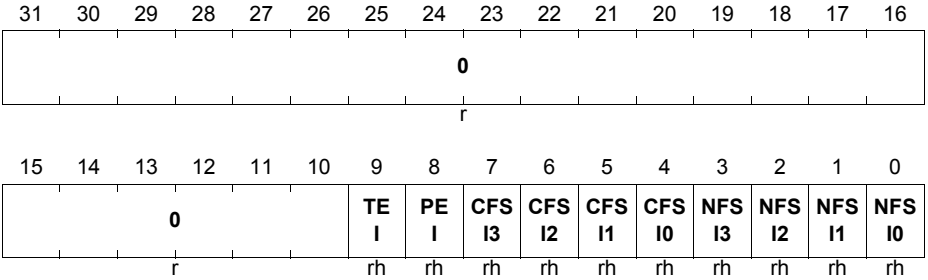
Field	Bits	Type	Description
TEIE	9	rw	**Time-Out Error Interrupt Enable** 0_B Time-out error event is disabled for activation of an SRx line. 1_B Time-out error event is enabled for activation of an SRx line.
NFSIR0, NFSIR1, NFSIR2, NFSIR3	16, 17, 18, 19	w	**Normal Frame Sent in Pipe x Flag Clear** 0_B No action. 1_B Clear TISR.NFSIx.
CFSIR0, CFSIR1, CFSIR2, CFSIR3	20, 21, 22, 23	w	**Command Frame Sent in Pipe x Flag Clear** 0_B No action. 1_B Clear TISR.CFSIx.
PEIR	24	w	**Parity Error Flag Clear** 0_B No action. 1_B Clear TISR.PEIx.
TEIR	25	w	**Time Out Error Flag Clear** 0_B No action. 1_B Clear TISR.TEIx.
0	[15:10], [31:26]	r	**Reserved** Read as 0; should be written with 0.

Transmitter Interrupt Register

The Transmitter Interrupt Status Register TISR contains all MLI event (or interrupt) flags of the MLI transmitter. These flags can be cleared by software when writing the appropriate bits in the TIER register; they are not cleared by hardware.

TISR

Transmitter Interrupt Status Register ($9C_H$) **Reset Value: $0000\ 0000_H$**



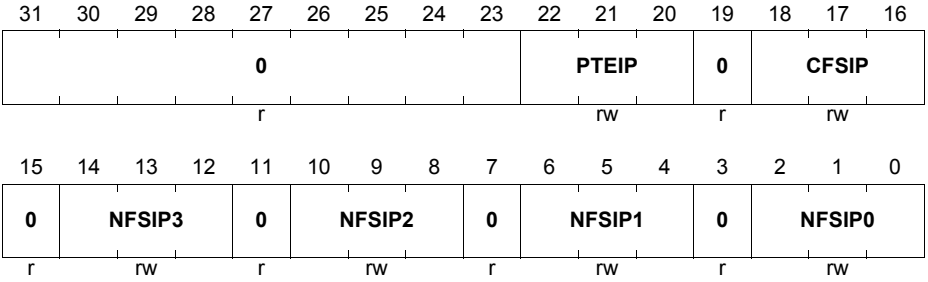
Field	Bits	Type	Description
NFSI0, **NFSI1,** **NFSI2,** **NFSI3**	0, 1, 2, 3	rh	**Normal Frame Sent in Pipe x Flag** The service request output that can be activated is defined by TINPR.NFSIPx. 0_B A Normal Frame has not yet been sent. 1_B A Write or Read Frame has been correctly sent and acknowledged for pipe x.
CFSI0, **CFSI1,** **CFSI2,** **CFSI3**	4, 5, 6, 7	rh	**Command Frame Sent in Pipe x Flag** The service request output that can be activated is defined by TINPR.CFSIP. 0_B A Command Frame has not yet been sent. 1_B A Command Frame has been correctly sent and acknowledged for pipe x.
PEI	8	rh	**Parity Error Flag** The service request output that can be activated is defined by TINPR.PTEIPx. 0_B A parity error event has not yet been detected. 1_B A parity error event has been detected.

Field	Bits	Type	Description
TEI	9	rh	**Time-Out Error Flag** The service request output that can be activated is defined by TINPR.PTEIPx. 0_B A time-out error event has not yet been detected. 1_B A time-out error event has been detected.
0	[31:10]	r	**Reserved** Read as 0; should be written with 0.

Transmitter Interrupt Node Pointer Register

The Transmitter Interrupt Node Pointer Register TINPR contains the node pointers for the MLI transmitter events.

TINPR
Transmitter Interrupt Node Pointer Register
($A0_H$) **Reset Value: $0000\ 0000_H$**



Field	Bits	Type	Description
NFSIP0	[2:0]	rw	**Normal Frame Sent in Pipe 0 Interrupt Pointer** This bit field determines which service request output SRx becomes active when a Normal Frame sent in pipe 0 event occurs (if enabled). 000_B The service request output SR0 is selected. 001_B The service request output SR1 is selected. $\cdots_B$ … 110_B The service request output SR6 is selected. 111_B The service request output SR7 is selected.
NFSIP1	[6:4]	rw	**Normal Frame Sent in Pipe 1 Interrupt Pointer** This bit field determines which service request output SRx becomes active when a Normal Frame sent in pipe 1 event occurs (if enabled). Coding see NFSIP0.
NFSIP2	[10:8]	rw	**Normal Frame Sent in Pipe 2 Interrupt Pointer** This bit field determines which service request output SRx becomes active when a Normal Frame sent in pipe 2 event occurs (if enabled). Coding see NFSIP0.
NFSIP3	[14:12]	rw	**Normal Frame Sent in Pipe 3 Interrupt Pointer** This bit field determines which service request output SRx becomes active when a Normal Frame sent in pipe 3 event occurs (if enabled). Coding see NFSIP0.

Field	Bits	Type	Description
CFSIP	[18:16]	rw	**Command Frame Sent Interrupt Pointer** This bit field determines which service request output SRx becomes active when a Command Frame sent event occurs (if enabled). Coding see NFSIP0.
PTEIP	[22:20]	rw	**Parity or Time Out Interrupt Pointer** This bit field determines which service request output SRx becomes active when a parity/time-out event occurs (if enabled). Coding see NFSIP0.
0	3, 7, 11, 15, 19, [31:23]	r	**Reserved** Read as 0; should be written with 0.

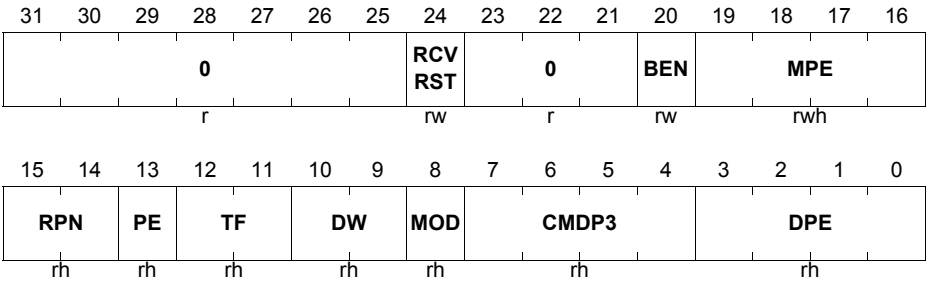
27.4.7 Receiver Control/Status Registers

Receiver Control Register

The Receiver Control Register RCR contains control and status bits/bit fields that are related to the MLI receiver operation.

Bit RCVRST is automatically overwritten after a reset (see **Page 27-68**) with a value given in the implementation chapter (see **Page 27-130**).

RCR
Receiver Control Register **(68_H)** **Reset Value: $0100\ 0000_H$**



Field	Bits	Type	Description
DPE	[3:0]	rh	**Delay for Parity Error** DPE determines the number of RCLK clock periods that the MLI receiver waits before the RREADY signal is raised again when it has detected a parity error (see **Page 27-22**). When a pipe 1 Command Frame is received by the MLI receiver, the command code is stored in this bit field (see **Page 27-41**). 0000_B Zero RCLK clock period delay is selected. 0001_B One RCLK clock period delay is selected. 0010_B Two RCLK clock periods delay is selected. $...B$ ... 1110_B Fourteen RCLK clock periods delay is selected. 1111_B Fifteen RCLK clock periods delay is selected.
CMDP3	[7:4]	rh	**Command From Pipe 3** When a pipe 3 Command Frame is received by the MLI receiver, the command code is stored in this bit field. Pipe 3 commands are free for software use.

Field	Bits	Type	Description
MOD	8	rh	**Mode of Operation** This bit determines the data transfer operation mode of the MLI receiver. Bit MOD can be set by hardware with the reception of a pipe 2 Command Frame (see Page 27-100). It can be set or cleared by software via bits SCR.SMOD or SCR.CMOD. 0_B Automatic Data Mode is disabled. Data read/write operations from/to a Remote Window must be executed by a bus master (e.g. the CPU). 1_B Automatic Data Mode is enabled. Data read/write operations from/to a Remote Window are executed by the MLI's move engine.
DW	[10:9]	rh	**Data Width** This bit field is updated by the MLI receiver whenever new data is received in the RDATAR register. It indicates the relevant data width. 00_B 8-bit relevant data width in RDATAR 01_B 16-bit relevant data width in RDATAR 10_B 32-bit relevant data width in RDATAR 11_B Reserved
TF	[12:11]	rh	**Type of Frame** This bit field determines the frame type that has most recently been received by the MLI receiver. It is updated whenever the MLI receiver updates RDATAR, RADDR, or RPxBAR. The most recently received frame was a: 00_B Copy Base Address Frame 01_B Discrete Read Frame or Optimized Read Frame 10_B Write Offset and Data Frame or Optimized Write Frame 11_B Answer frame Note that the coding of TF is different from the frame coding as defined in Table 27-1 on Page 27-11.
PE	13	rh	**Parity Error** PE is set when a parity error is detected in a received frame (see Page 27-44). PE is cleared by hardware when a frame has been received without parity error. PE can be cleared by software via bit SCR.CRPE.

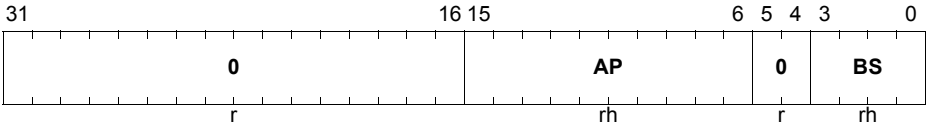
Field	Bits	Type	Description
RPN	[15:14]	rh	**Received Pipe Number** This bit field contains the Pipe Number that was indicated by the Pipe Number bit field of the latest received frame. It is updated by any received frame.
MPE	[19:16]	rwh	**Maximum Parity Errors** This bit field indicates the number of receive parity error conditions after which a receiver parity error event will be generated. It is set to a desired value by software and it is decremented down to 0 automatically by the MLI each time it detects a receiver parity error condition. If a receiver parity error condition is detected and MPE becomes 0 or is already 0, a receiver parity error event is generated (see **Page 27-44**). 0000_B A receiver parity event is generated if a receiver error condition is detected. 0001_B A receiver parity event is generated if a receiver error condition is detected. 0010_B A receiver parity event is generated if 2 receiver error conditions are detected. $\ldots_B$ … 1110_B A receiver parity event is generated if 14 receiver error conditions are detected. 1111_B A receiver parity event is generated if 15 receiver error conditions are detected.
BEN	20	rw	**Break Out Enable** When setting BEN = 1, the MLI receiver generates a pulse on its break output signal BRKOUT when a pipe 2 Command Frame with command code CMD = 1111_B is received. 0_B Break output signal generation is disabled. 1_B Break output signal is enabled.
RCVRST	24	rw	**Receiver Reset** This bit forces the receiver to be reset in order to be able to change OICR settings without affecting the receiver registers. 0_B The MLI receiver is in operating mode. 1_B The MLI receiver is held in reset state and OICR can be modified without unintentional actions in the receiver.

Field	Bits	Type	Description
0	[23:21], [31:25]	r	**Reserved** Read as 0; should be written with 0.

Receiver Pipe x Status Register

The Receiver Pipe x Status Register RPxSTATR indicates the coded buffer size which represents the Remote Window Size of 2 Bytes to 64 Kbytes and the address prediction factor that has been calculated for pipe x in the receiving controller.

RPxSTATR (x = 0-3)
Receiver Pipe x Status Register **($7C_H$+4_H*x)** **Reset Value: 0000 0000_H**



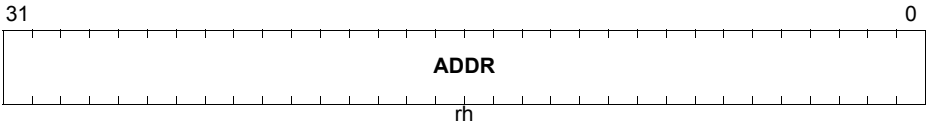
Field	Bits	Type	Description
BS	[3:0]	rh	**Buffer Size** This bit field indicates the size of pipe x Remote Window in the receiving controller. It is updated by hardware when a Copy Base Address Frame has been received (see **Page 27-28**). 0000_B 1-bit offset address of Remote Window 0001_B 2-bit offset address of Remote Window 0010_B 3-bit offset address of Remote Window $...{}_B$ ... 1110_B 15-bit offset address of Remote Window 1111_B 16-bit offset address of Remote Window
AP	[15:6]	rh	**Address Prediction Factor** AP contains the address prediction factor that has been calculated for pipe x in the receiving controller. It is a signed 9-bit number with the sign in its most significant bit (see **Page 27-47**).
0	[5:4], [31:16]	r	**Reserved** Read as 0; should be written with 0.

27.4.8 Receiver Address/Data Registers

Receiver Pipe x Base Address Register

The Receiver Pipe x Base Address Register RPxBAR is a read-only register that contains the complete target address in the Remote Window of pipe x.

RPxBAR (x = 0-3)
Receiver Pipe x Base Address Register
($6C_H$+4_H*x) **Reset Value: 0000 0000_H**

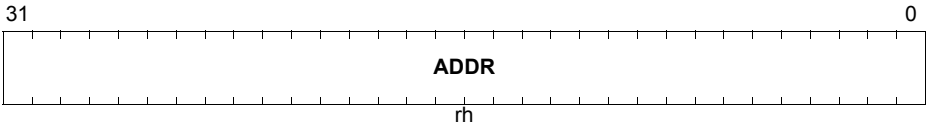


Field	Bits	Type	Description
ADDR	[31:0]	rh	**Address** ADDR indicates the complete target address for the pipe x Remote Window. If a pipe x Copy Base Address Frame is received, ADDR[31:4] becomes loaded with the transmitted 28-bit address and bits [3:0] are cleared. If a write or Read Frame with m bits of address offset is received, bits ADDR[31:m] are held constant and bits ADDR[m-1:0] are replaced by the received offset. If an optimized read or data frame is received, the address prediction mechanism adds the predicted address offset RPxSTATR.AP to ADDR and stores the result in ADDR. If an Answer Frame is received, ADDR is not changed.

Receiver Address Register

The Receiver Address Register RADRR is a read-only register storing the complete address of the most recently (or currently) targeted Remote Window.

RADRR
Receiver Address Register **($8C_H$)** **Reset Value: $0000\ 0000_H$**

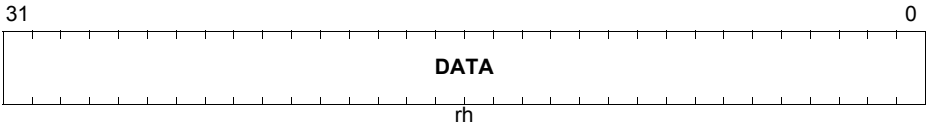


Field	Bits	Type	Description
ADDR	[31:0]	rh	**Address** ADDR indicates the complete target address for the most recently (or currently) targeted Remote Window (pipe x). If a Copy Base Address Frame is received, ADDR is unchanged. If a write or Read Frame with m bits of address offset is received, bits ADDR[31:m] replaced by the bits RPxBAR.ADDR[31:m] and bits ADDR[m-1:0] are replaced by the received offset. If an optimized read or data frame is received, the address prediction mechanism adds the predicted address offset RPxSTATR.AP to RPxBAR.ADDR and stores the result in ADDR. If an Answer Frame is received, ADDR becomes invalid.

Receiver Data Register

The Receiver Data Register RDATAR is a read-only register that stores data received by a Write Frame or an Answer Frame.

RDATAR
Receiver Data Register **(90_H)** **Reset Value: $0000\ 0000_H$**



Field	Bits	Type	Description
DATA	[31:0]	rh	**Data** In the receiving controller, DATA contains the data received by a Write Frame or an Answer Frame. Bit field RCR.DW determines the width of the relevant data that is stored in RDATAR. RCR.DW = 00_B: RDATAR[7:0] are relevant (8-bit) RCR.DW = 01_B: RDATAR[15:0] are relevant (16-bit) RCR.DW = 10_B: RDATAR[31:0] are relevant (32-bit)

27.4.9 Receiver Interrupt Registers

Receiver Interrupt Enable Register

The Receiver Interrupt Enable Register RIER contains the interrupt enable bits and the clear bits for all receiver events. The bits marked w are always read as 0.

RIER
Receiver Interrupt Enable Register ($A4_H$) **Reset Value: $0000\ 0000_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0						DRAIR	MPEIR	PEIR	ICER	CFRIR3	CFRIR2	CFRIR1	CFRIR0	MEIR	NFRIR
r						w	w	w	w	w	w	w	w	w	w

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0						DRAIE	MPEIE	PEIE	ICE	CFRIE3	CFRIE2	CFRIE1	CFRIE0	NFRIE	
r						rw	rw	rw	rw	rw	rw	rw	rw	rw	

Field	Bits	Type	Description
NFRIE	[1:0]	rw	**Normal Frame Received Interrupt Enable** This bit field defines if an SRx output is activated if a Normal Frame is correctly received. 00_B The SRx activation is disabled. 01_B The selected SRx line is activated each time a Normal Frame is correctly received. 10_B The selected SRx line is activated each time a Normal Frame is correctly received that is not handled automatically by the MLI move engine (e.g. an Answer Frame). 11_B Reserved
CFRIE0, CFRIE1, CFRIE2, CFRIE3	2, 3, 4, 5	rw	**Command Received in Pipe x Interrupt Enable** This bit determines if an SRx output is activated if a Command Frame for pipe x has been received correctly. 0_B Command received in pipe x event is disabled for activation of an SRx line. 1_B Command received in pipe x event is enabled for activation of an SRx line.

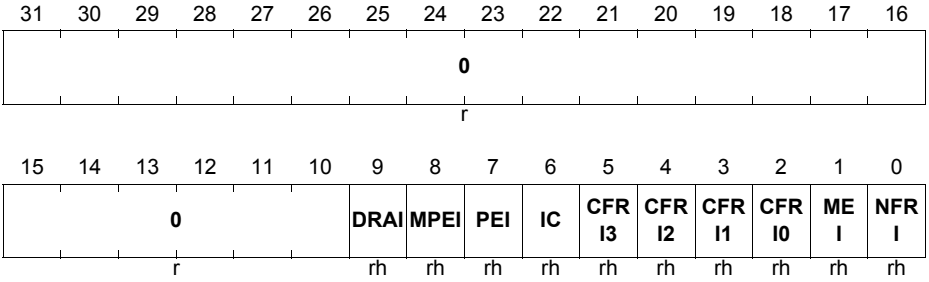
Field	Bits	Type	Description
ICE	6	rw	**Interrupt Command Enable** This bit determines if an SRx output line is activated if a Command Frame is received in pipe 0. 0_B Command frame received in pipe 0 event is disabled for activation of an SRx line. 1_B Command frame received in pipe 0 event is enabled for activation of an SRx line.
PEIE	7	rw	**Parity Error Interrupt Enable** This bit determines if an SRx output line is activated if receiver a parity error event is detected. 0_B Parity error event is disabled for activation of an SRx line. 1_B Parity error event is enabled for activation of an SRx line.
MPEIE	8	rw	**Memory Access Protection Interrupt Enable** This bit determines if an SRx output line is activated if a memory access protection error is detected. 0_B Memory access protection error event is disabled for activation of an SRx line. 1_B Memory access protection error event is enabled for activation of an SRx line.
DRAIE	9	rw	**Discarded Read Answer Interrupt Enable** This bit determines if an SRx output line is activated if a discarded read Answer Frame condition is detected. 0_B Discarded read answer event is disabled for activation of an SRx line. 1_B Discarded read answer event is enabled for activation of an SRx line.
NFRIR	16	w	**Normal Frame Received Interrupt Flag Clear** 0_B No action. 1_B Clear RISR.NFRI.
MEIR	17	w	**MLI Move Engine Interrupt Flag Clear** 0_B No action. 1_B Clear RISR.MEI.
CFRIR0, CFRIR1, CFRIR2, CFRIR3	18, 19, 20, 21	w	**Command Frame Received in Pipe x Interrupt Flag Clear** 0_B No action. 1_B Clear RISR.CFRIx.

Field	Bits	Type	Description
ICER	22	w	**Interrupt Command Flag Clear** 0_B No action. 1_B Clear RISR.ICE.
PEIR	23	w	**Parity Error Interrupt Flag Clear** 0_B No action. 1_B Clear RISR.PEI.
MPEIR	24	w	**Memory Protection Error Interrupt Flag Clear** 0_B No action. 1_B Clear RISR.MPEI.
DRAIR	25	w	**Discarded Read Answer Interrupt Flag Clear** 0_B No action. 1_B Clear RISR.DRAI.
0	[15:10], [31:26]	r	**Reserved** Read as 0; should be written with 0.

Receiver Interrupt Status Register

The Receiver Interrupt Status Register RISR contains all event (interrupt) flags of the MLI receiver. These flags can be cleared by software when writing the appropriate bits in the RIER register; they are not cleared by hardware.

RISR
Receiver Interrupt Status Register (A8$_H$) Reset Value: 0000 0000$_H$



Field	Bits	Type	Description
NFRI	0	rh	**Normal Frame Received Interrupt Flag** This flag is set when a write or a Read Frame has been received. The service request output that is activated is defined by RINPR.NFRIP.
MEI	1	rh	**MLI Move Engine Interrupt Flag** This flag is set when the move engine has finished an operation (read or write, depending on received frame). The service request output that is activated is defined by RINPR.MPPEIP.
CFRI0, CFRI1, CFRI2, CFRI3	2, 3, 4, 5	rh	**Command Frame Received in Pipe x Interrupt Flag** This flag is set when a Command Frame has been received in pipe x. The service request output that is activated is defined by RINPR.CFRIP.
IC	6	rh	**Interrupt Command Flag** This flag is set when a Command Frame has been received in pipe 0 leading to an activation of one of the service request outputs SR[3:0]. The service request output that is activated is defined by the received command CMD.

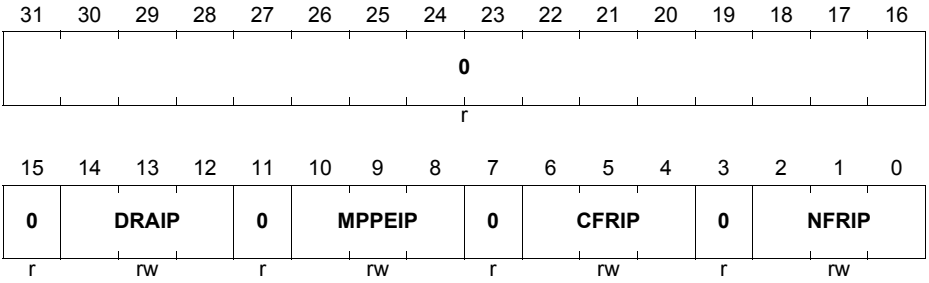
Field	Bits	Type	Description
PEI	7	rh	**Parity Error Interrupt Flag** This flag is set when a parity error event has occurred. The service request output that is activated is defined by RINPR.MPPEIP.
MPEI	8	rh	**Memory Protection Error Interrupt Flag** This flag is set when a memory protection event has occurred. The service request output that is activated is defined by RINPR.MPPEIP.
DRAI	9	rh	**Discarded Read Answer Interrupt Flag** This flag is set when the discarded read answer event has occurred. This condition occurs if an Answer Frame is received while none of the TRSTATR.RPx bits is set (the Answer Frame was not expected). The service request output that is activated is defined by RINPR.DRAIP.
0	[31:10]	r	**Reserved** Read as 0; should be written with 0.

Receiver Interrupt Node Pointer Register

The Receiver Interrupt Node Pointer Register RINPR contains the node pointers for the MLI receiver events.

RINPR
Receiver Interrupt Node Pointer Register

(AC_H) **Reset Value: 0000 0000$_H$**



Field	Bits	Type	Description
NFRIP	[2:0]	rw	**Normal Frame Received Interrupt Pointer** This bit field determines which service request output SRx becomes active when a Normal Frame received event occurs. 000_B The service request output SR0 is selected. 001_B The service request output SR1 is selected. $\ldots_B$ … 110_B The service request output SR6 is selected. 111_B The service request output SR7 is selected.
CFRIP	[6:4]	rw	**Command Frame Received Interrupt Pointer** This bit field determines which service request output SRx becomes active when a Command Frame received event occurs. Coding see NFRIP.
MPPEIP	[10:8]	rw	**Memory Protection or Parity Error Interrupt Pointer** This bit field determines which service request output SRx becomes active when a memory protection/parity error event occurs. Coding see NFRIP.
DRAIP	[14:12]	rw	**Discarded Read Answer Interrupt Pointer** This bit field determines which service request output SRx becomes active when a discarded read answer event occurs. Coding see NFRIP.

Field	Bits	Type	Description
0	3, 7, 11, [31:15]	r	**Reserved** Read as 0; should be written with 0.

27.5 Implementation of the MLI0/MLI1 in TC1798

This section describes the MLI0/MLI1 module related external functions such as port connections, interrupt and service request control, connections to other on-chip modules, clock control, and the address map.

27.5.1 Interfaces of the MLI Modules

Each MLI module is supplied with separate clock control, address decoding, and interrupt control logic. Four (for MLI0) and two (for MLI1) of the eight module service request outputs are connected to service request nodes. Four service request outputs of each MLI module are connected as DMA request to with the DMA controller.

The data, clock, and control lines of each MLI receiver and transmitter are connected to GPIO lines. Alternate functions of Port 1 and Port 5 lines are assigned to the MLI0 module I/O lines while alternate functions of Port 8 lines are assigned to the MLI0 module I/O lines. Additionally, within one MLI module transmitter and receiver signals can be dynamically connected among each other without using pins; this is useful for test purposes.

Figure 27-52 and **Figure 27-53** show how the MLI0 and MLI1 modules are interconnected to port lines and other on-chip functional blocks.

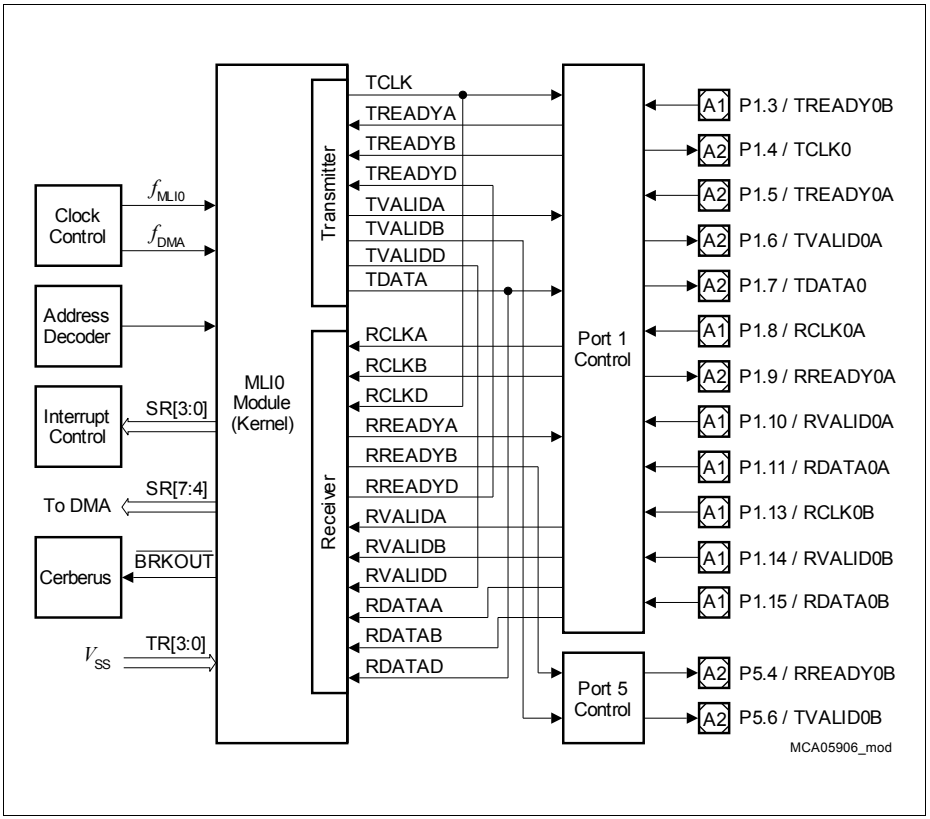


Figure 27-52 MLI0 Module Implementation and Interconnections

When programming the MLI0_OICR register, the following additional items must be considered:

- Unused transmitter/receiver output lines with index “C” (TVALIDC and RREADYC) are not connected.
- Unused transmitter/receiver input lines with index “C” (TREADYC, RCLKC, RVALIDC, and RDATAC) are connected to low level.

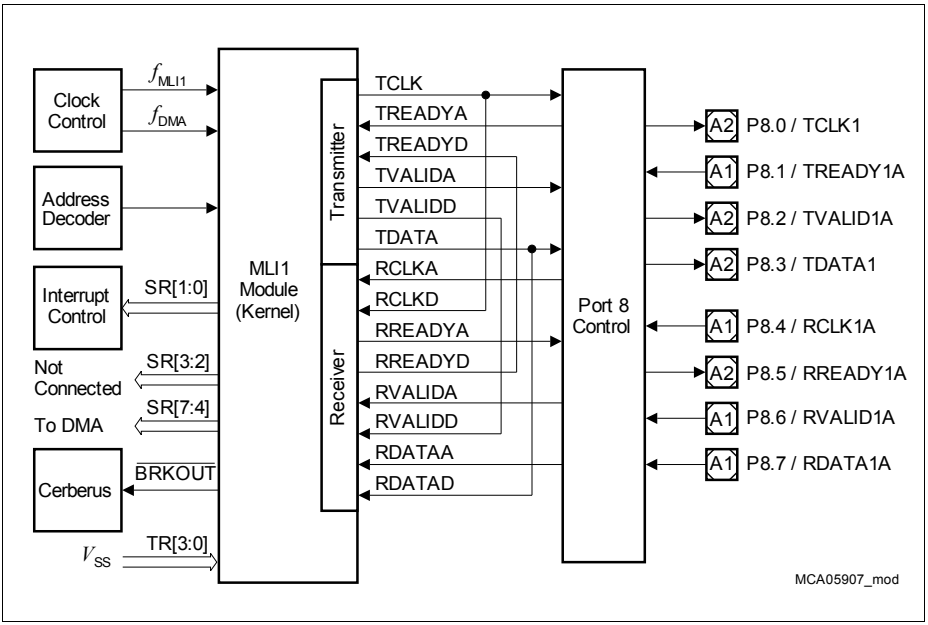


Figure 27-53 MLI1 Module Implementation and Interconnections

When programming the MLI1_OICR register, the following additional items must be considered:

- Lines with index “B” (not shown in the figure above)
  - Unused transmitter/receiver output lines TVALIDB and RREADYB are not connected.
  - Unused transmitter/receiver input lines TREADYB, RCLKB, RVALIDB, and RDATAB are connected to low level.
- Lines with index “C” (not shown in the figure above)
  - Unused transmitter/receiver output lines TVALIDC and RREADYC are reserved for emulation purposes.
  - Unused transmitter/receiver input lines TREADYC, RCLKC, RVALIDC, and RDATAC are reserved for emulation purposes and should not be selected during normal operation of the TC1798.

See also **Page 27-133** for additional details on I/O line control and function.

27.5.2 MLI Module External Registers

Figure 27-54 summarizes the module related external registers that are required for MLI0/MLI1 programming. Details on MLI0/MLI1 related register settings are shown in the following sections.

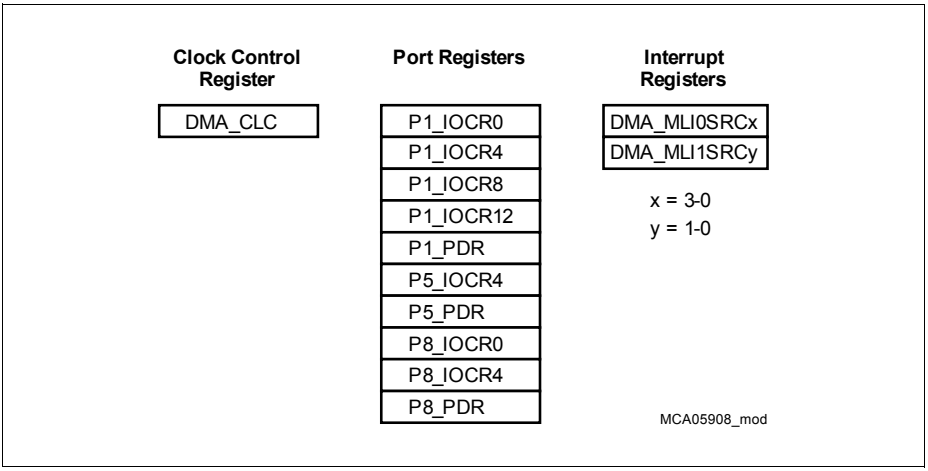


Figure 27-54 MLI0/MLI1 Implementation-Specific Special Function Registers

27.5.2.1 Automatic Register Overwrite

The following values are applied after reset (see **Page 27-68**).

- OICR = 1000 8000_H; Setting “A” is selected
- RCR.RCVRST = 0: the receiver is enabled for reception.

27.5.3 Module Clock Generation

The module clock generation configuration for the two MLI modules is shown in **Figure 27-55**.

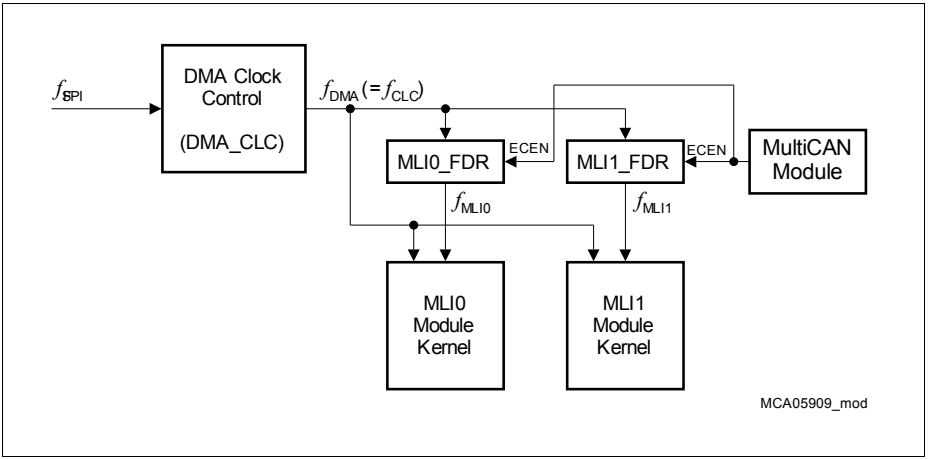


Figure 27-55 Clock Configuration of the MLI Modules

The DMA controller and the two MLI modules (MLI0 and MLI1) are supplied from a common module clock f_{DMA}, that has the frequency of the system clock f_{FPI}) and is controlled via the DMA_CLC clock control register. The MLI modules do not have its own clock control registers. Its module clocks f_{MLI0} and f_{MLI1} are derived from f_{DMA} by two separate fractional divider registers, MLI0_FDR and MLI1_FDR (description see **Page 27-79**).

Output signal CAN_INT_O15 of the MultiCAN module can be used for external clock enable control of the fractional divider.

- f_{DMA}
  This is the module clock used inside the MLI kernels for control purposes such as for clocking of control logic and register operations. The clock control register DMA_CLC makes it possible to enable/disable f_{DMA} under certain conditions. DMA_CLC is described in the DMA chapter of this document.
- f_{MLI0} and f_{MLI1}
  This clock is the module clock used in the MLI kernels as base for the shift clock and therefore determines the baud rate of the synchronous serial data transmission. The fractional divider registers MLI0_FDR and MLI1_FDR control the frequencies of f_{MLI0} and f_{MLI1}. This configuration makes it possible to enable/disable the module clocks f_{MLI0} and f_{MLI1} independently of f_{DMA}.

Combined with the baud rate as derived in the MLI module (see **Equation (27.1)** on **Page 27-67**) and the MLIx_FDR fractional divider setup, the resulting MLI baud rate is defined by:

$$\text{Baud rate}_{MLIx} = \frac{f_{DMA}}{2} \times \frac{1}{n} \quad \text{with n = 1024 - FDR.STEP} \tag{27.4}$$

$$\text{Baud rate}_{MLIx} = \frac{f_{DMA}}{2} \times \frac{n}{1024} \quad \text{with n = 0-1023} \tag{27.5}$$

Equation (27.4) applies to normal divider mode of the fractional divider (FDR.DM = 01_B). **Equation (27.5)** applies to fractional divider mode (FDR.DM = 10_B).

After a reset operation, both MLI modules are enabled in normal divider mode. According the MLIx_FDR register's reset value of 03FF $43FF_H$, the selected baud rate is $f_{DMA}/2$. Note that the DMA controller is also enabled after a reset operation with clock $f_{DMA} = f_{FPI}$.

27.5.4 Port Control and Connections

MLI0 and MLI1 clock and data output lines are connected to GPIO ports and are, therefore, controlled in the port logics (see also **Page 27-128** and **Page 27-129**). The following port control operations selections must be executed for these I/O lines:

- Input/output function selection (IOCR registers)
- Pad driver characteristics selection for the outputs (PDR registers)

27.5.4.1 Input/Output Function Selection

The port input/output control registers contain the bit fields that select the digital output and input driver characteristics such as port direction (input/output) with alternate output selection, pull-up/down devices, and open-drain selections. The I/O lines for the MLI modules are controlled by the Port 1, Port 5 and Port 8 input/output control registers. When the MLI modules are connected to the GPIO port lines, the correct settings of the enable/polarity control bits and bit fields in the output input control registers MLI0_IOCR and MLI1_IOCR must also be regarded (transmitter I/O line control see **Page 27-53**, receiver I/O line control see **Page 27-54**). Note that after a reset operation the MLI0 and MLI1 modules (although enabled) have no direct connections to the GPIO lines.

Table 27-11 shows how OICR register bits and bit fields must be programmed for the required GPIO functionality of the MLI I/O lines.

Table 27-11 MLI0 and MLI1 I/O Line Selection and Setup

Module	Port Lines	Input/Output Control Register Bits	I/O
MLI0	P1.3 / TREADY0B	P1_IOCR0.PC3 = $0XXX_B$ MLI0_OICR.TRE = 1 MLI0_OICR.TRP = X MLI0_OICR.TRS = 01_B	Input
	P1.4 / TCLK0	P1_IOCR4.PC4 = $1X01_B$ MLI0_OICR.TCE = 1 MLI0_OICR.TCP = X	Output
	P1.5 / TREADY0A	P1_IOCR4.PC5 = $0XXX_B$ MLI0_OICR.TRE = 1 MLI0_OICR.TRP = X MLI0_OICR.TRS = 00_B	Input
	P1.6 / TVALID0A	P1_IOCR4.PC6 = $1X01_B$ MLI0_OICR.TVEA = 1 MLI0_OICR.TVPA = X	Output
	P1.7 / TDATA0	P1_IOCR4.PC7 = $1X01_B$ MLI0_OICR.TDP = X	Output

Table 27-11 MLI0 and MLI1 I/O Line Selection and Setup (cont'd)

Module	Port Lines	Input/Output Control Register Bits	I/O
MLI0	P1.8 / RCLK0A	P1_IOCR8.PC8 = $0XXX_B$ MLI0_OICR.RCE = 1 MLI0_OICR.RCP = X MLI0_OICR.RCS = 00_B	Input
	P1.9 / RREADY0A	P1_IOCR8.PC9 = $1X01_B$ MLI0_OICR.RRS = 00_B MLI0_OICR.RRPA = X	Output
	P1.10 / RVALID0A	P1_IOCR8.PC10 = $0XXX_B$ MLI0_OICR.RVE = 1 MLI0_OICR.RVP = X MLI0_OICR.RVS = 00_B	Input
	P1.11 / RDATA0A	P1_IOCR8.PC11 = $0XXX_B$ MLI0_OICR.RDP = X MLI0_OICR.RDS = 00_B	Input
	P1.13 / RCLK0B	P1_IOCR12.PC13 = $0XXX_B$ MLI0_OICR.RCE = 1 MLI0_OICR.RCP = X MLI0_OICR.RCS = 01_B	Input
	P1.14 / RVALID0B	P1_IOCR12.PC14 = $0XXX_B$ MLI0_OICR.RVE = 1 MLI0_OICR.RVP = X MLI0_OICR.RVS = 01_B	Input
	P1.15 / RDATA0B	P1_IOCR12.PC15 = $0XXX_B$ MLI0_OICR.RDP = X MLI0_OICR.RDS = 01_B	Input
	P5.4 / RREADY0B	P5_IOCR4.PC4 = $1X10_B$ MLI0_OICR.RRS = 01_B MLI0_OICR.RRPB = X	Output
	P5.6 / TVALID0B	P5_IOCR4.PC6 = $1X10_B$ MLI0_OICR.TVEB = 1 MLI0_OICR.TVPB = X	Output

Table 27-11 MLI0 and MLI1 I/O Line Selection and Setup (cont'd)

Module	Port Lines	Input/Output Control Register Bits	I/O
MLI1	P8.0 / TCLK1	P8_IOCR0.PC0 = $1X11_B$ MLI1_OICR.TCE = 1 MLI1_OICR.TCP = X	Output
	P8.1 / TREADY1A	P8_IOCR0.PC1 = $0XXX_B$ MLI1_OICR.TRE = 1 MLI1_OICR.TRP = X MLI1_OICR.TRS = 00_B	Input
	P8.2 / TVALID1A	P8_IOCR0.PC2 = $1X11_B$ MLI1_OICR.TVEA = 1 MLI1_OICR.TVPA = X	Output
	P8.3 / TDATA1	P8_IOCR0.PC3 = $1X11_B$ MLI1_OICR.TDP = X	Output
	P8.4 / RCLK1A	P8_IOCR4.PC4 = $0XXX_B$ MLI1_OICR.RCE = 1 MLI1_OICR.RCP = X MLI1_OICR.RCS = 00_B	Input
	P8.5 / RREADY1A	P8_IOCR4.PC5 = $1X11_B$ MLI1_OICR.RRS = 00_B MLI1_OICR.RRPA = X	Output
	P8.6 / RVALID1A	P8_IOCR4.PC6 = $0XXX_B$ MLI1_OICR.RVE = 1 MLI1_OICR.RVP = X MLI1_OICR.RVS = 00_B	Input
	P8.7 / RDATA1A	P8_IOCR4.PC7 = $0XXX_B$ MLI1_OICR.RDP = X MLI1_OICR.RDS = 00_B	Input

27.5.5 On-Chip Connections

27.5.5.1 Service Request Output Connections

Each MLI module provides eight service request outputs SR[7:0] that can be used to generate interrupts or DMA requests. In the TC1798, four service request outputs SR[3:0] of the MLI0 module and two service request outputs SR[1:0] of the MLI1 module are connected to an interrupt node. Service request outputs SR[3:2] of the MLI1 module are not connected. Four service request outputs (SR[7:4]) of each MLI module are connected to DMA request inputs of the TC1798 DMA controller.

Each of the service request outputs used as interrupt requests are controlled by a service request control register. The service request control registers of the MLI modules are located inside the DMA address area. Therefore, all MLI0/MLI1 service request control registers are named as DMA_MLIxSRCy and described in the DMA chapter implementation part of the TC1798 User´s Manual.

All MLI service request output connections are listed in **Table 27-12**.

Table 27-12 Service Request Lines and Interconnections of MLI0/MLI1

Module	Service Req. Output Line	Connected to Node or DMA Request Input	Description
MLI0	SR0	DMA_MLI0SRC0	MLI0 Service Request Node 0 (in DMA)
	SR1	DMA_MLI0SRC1	MLI0 Service Request Node 1 (in DMA)
	SR2	DMA_MLI0SRC2	MLI0 Service Request Node 2 (in DMA)
	SR3	DMA_MLI0SRC3	MLI0 Service Request Node 3 (in DMA)
	SR4	CH00_REQI7	DMA Channel 00 Request Input 7
		CH04_REQI7	DMA Channel 04 Request Input 7
	SR5	CH01_REQI7	DMA Channel 01 Request Input 7
		CH05_REQI7	DMA Channel 05 Request Input 7
	SR6	CH02_REQI7	DMA Channel 02 Request Input 7
		CH06_REQI7	DMA Channel 06 Request Input 7
	SR7	CH03_REQI7	DMA Channel 03 Request Input 7
		CH07_REQI7	DMA Channel 07 Request Input 7

Table 27-12 Service Request Lines and Interconnections of MLI0/MLI1 (cont'd)

Module	Service Req. Output Line	Connected to Node or DMA Request Input	Description
MLI1	SR0	DMA_MLI1SRC0	MLI1 Service Request Node 0 (in DMA)
	SR1	DMA_MLI1SRC1	MLI1 Service Request Node 1 (in DMA)
	SR2	–	Not connected
	SR3	–	Not connected
	SR4	CH10_REQI15	DMA Channel 10 Request Input 15
		CH14_REQI15	DMA Channel 14 Request Input 15
	SR5	CH11_REQI15	DMA Channel 11 Request Input 15
		CH15_REQI15	DMA Channel 15 Request Input 15
	SR6	CH12_REQI15	DMA Channel 12 Request Input 15
		CH16_REQI15	DMA Channel 16 Request Input 15
	SR7	CH13_REQI15	DMA Channel 13 Request Input 15
		CH17_REQI15	DMA Channel 17 Request Input 15

27.5.5.2 Break Signals

The $\overline{\text{BRKOUT}}$ output signals of MLI0 and MLI1 are connected as break input signals to the Multi Core Break Switch (MCBS) that is a part of the Cerberus on-chip debug control module. These connections allow MLI0/MLI1 initiated break conditions to be generated in the Cerberus.

27.5.5.3 Trigger Input Signals

The five Trigger Input Signals TR[4:0] are connected to V_{SS}.

27.5.6 Access Protection

The access protection parameters for the MLI module in the TC1798 are identical with access protection parameters of the DMA Controller. Details of the access protection parameters are defined in the DMA chapter at "DMA Module Implementation" - "Access Protection Assignment".

The Table "DMA Access Protection Address Ranges" in the DMA chapter is also valid for MLI register bits AER0.AENRx and AER1.AENRx (x = 0-31).

The Tables "... Address Protection Sub-Range Definition" for PMI, OVRAM, DMI, and PCP PRAM in the DMA chapter are also valid for MLI register bits ARR0,1.SLICEn and ARR0,1.SIZEn (n = 0-3).

27.5.7 MLI0/MLI1 Transfer Window Address Maps

In the TC1798, the transfer windows for the MLI0 and MLI1 modules are located in the address ranges as identified in **Table 27-13**.

Table 27-13 MLI0/MLI1 Transfer Windows

Module	Window Type	Pipe	Address Range
MLI0	Small Transfer Window (STW)	Pipe 0	F01E 0000$_H$ to F01E 1FFF$_H$
		Pipe 1	F01E 2000$_H$ to F01E 3FFF$_H$
		Pipe 2	F01E 4000$_H$ to F01E 5FFF$_H$
		Pipe 3	F01E 6000$_H$ to F01E 7FFF$_H$
	Large Transfer Window (LTW)	Pipe 0	F020 0000$_H$ to F020 FFFF$_H$
		Pipe 1	F021 0000$_H$ to F021 FFFF$_H$
		Pipe 2	F022 0000$_H$ to F022 FFFF$_H$
		Pipe 3	F023 0000$_H$ to F023 FFFF$_H$
MLI1	Small Transfer Window (STW)	Pipe 0	F01E 8000$_H$ to F01E 9FFF$_H$
		Pipe 1	F01E A000$_H$ to F01E BFFF$_H$
		Pipe 2	F01E C000$_H$ to F01E DFFF$_H$
		Pipe 3	F01E E000$_H$ to F01E FFFF$_H$
	Large Transfer Window (LTW)	Pipe 0	F024 0000$_H$ to F024 FFFF$_H$
		Pipe 1	F025 0000$_H$ to F025 FFFF$_H$
		Pipe 2	F026 0000$_H$ to F026 FFFF$_H$
		Pipe 3	F027 0000$_H$ to F027 FFFF$_H$

27.5.8 MLI0/MLI1 Address Map

An absolute register address is given by the offset address of the register (given in Table 27-10) plus the module base address (given in Table 27-9).

Table 27-14 Address Map of MLI0/MLI1

Short Name	Description	Address	Access Mode		Reset Value
			Read	Write	
Multi Link Interface 0 (MLI0)					
–	Reserved	$F010\ C000_H$	nBE	SV, E	–
–	Reserved	$F010\ C004_H$	nBE	nBE	–
MLI0_ ID	MLI0 Module Identification Register	$F010\ C008_H$	U, SV	BE	$0025\ C0XX_H$
MLI0_ FDR	MLI0 Fractional Divider Register	$F010\ C00C_H$	U, SV	SV, E	$03FF\ 43FF_H$
MLI0_ TCR	MLI0 Transmitter Control Register	$F010\ C010_H$	U, SV	U, SV	$0000\ 0110_H$
MLI0_ TSTATR	MLI0 Transmitter Status Register	$F010\ C014_H$	U, SV	BE	$0000\ 0000_H$
MLI0_ TP0STATR	MLI0 Transmitter Pipe 0 Status Register	$F010\ C018_H$	U, SV	BE	$0000\ 0000_H$
MLI0_ TP1STATR	MLI0 Transmitter Pipe 1 Status Register	$F010\ C01C_H$	U, SV	BE	$0000\ 0000_H$
MLI0_ TP2STATR	MLI0 Transmitter Pipe 2 Status Register	$F010\ C020_H$	U, SV	BE	$0000\ 0000_H$
MLI0_ TP3STATR	MLI0 Transmitter Pipe 3 Status Register	$F010\ C024_H$	U, SV	BE	$0000\ 0000_H$
MLI0_ TCMDR	MLI0 Transmitter Command Register	$F010\ C028_H$	U, SV	U, SV	$0000\ 0000_H$
MLI0_ TRSTATR	MLI0 Transmitter Registers Status Register	$F010\ C02C_H$	U, SV	BE	$0000\ 0000_H$
MLI0_ TP0AOFR	MLI0 Transmitter Pipe 0 Address Offset Register	$F010\ C030_H$	U, SV	BE	$0000\ 0000_H$
MLI0_ TP1AOFR	MLI0 Transmitter Pipe 1 Address Offset Register	$F010\ C034_H$	U, SV	BE	$0000\ 0000_H$
MLI0_ TP2AOFR	MLI0 Transmitter Pipe 2 Address Offset Register	$F010\ C038_H$	U, SV	BE	$0000\ 0000_H$

Table 27-14 Address Map of MLI0/MLI1 (cont'd)

Short Name	Description	Address	Access Mode		Reset Value
			Read	Write	
MLI0_ TP3AOFR	MLI0 Transmitter Pipe 3 Address Offset Register	F010 C03C$_H$	U, SV	BE	0000 0000$_H$
MLI0_ TP0DATAR	MLI0 Transmitter Pipe 0 Data Register	F010 C040$_H$	U, SV	BE	0000 0000$_H$
MLI0_ TP1DATAR	MLI0 Transmitter Pipe 1 Data Register	F010 C044$_H$	U, SV	BE	0000 0000$_H$
MLI0_ TP2DATAR	MLI0 Transmitter Pipe 2 Data Register	F010 C048$_H$	U, SV	BE	0000 0000$_H$
MLI0_ TP3DATAR	MLI0 Transmitter Pipe 3 Data Register	F010 C04C$_H$	U, SV	BE	0000 0000$_H$
MLI0_ TDRAR	MLI0 Transmitter Data Read Answer Register	F010 C050$_H$	U, SV	U, SV	0000 0000$_H$
MLI0_ TP0BAR	MLI0 Transmitter Pipe 0 Base Address Register	F010 C054$_H$	U, SV	U, SV	0000 0000$_H$
MLI0_ TP1BAR	MLI0 Transmitter Pipe 1 Base Address Register	F010 C058$_H$	U, SV	U, SV	0000 0000$_H$
MLI0_ TP2BAR	MLI0 Transmitter Pipe 2 Base Address Register	F010 C05C$_H$	U, SV	U, SV	0000 0000$_H$
MLI0_ TP3BAR	MLI0 Transmitter Pipe 3 Base Address Register	F010 C060$_H$	U, SV	U, SV	0000 0000$_H$
MLI0_ TCBAR	MLI0 Transmitter Copy Base Address Register	F010 C064$_H$	U, SV	BE	0000 0000$_H$
MLI0_ RCR	MLI0 Receiver Control Register	F010 C068$_H$	U, SV	U, SV	0100 0000$_H$
MLI0_ RP0BAR	MLI0 Receiver Pipe 0 Base Address Register	F010 C06C$_H$	U, SV	BE	0000 0000$_H$
MLI0_ RP1BAR	MLI0 Receiver Pipe 1 Base Address Register	F010 C070$_H$	U, SV	BE	0000 0000$_H$
MLI0_ RP2BAR	MLI0 Receiver Pipe 2 Base Address Register	F010 C074$_H$	U, SV	BE	0000 0000$_H$
MLI0_ RP3BAR	MLI0 Receiver Pipe 3 Base Address Register	F010 C078$_H$	U, SV	BE	0000 0000$_H$

Table 27-14 Address Map of MLI0/MLI1 (cont'd)

Short Name	Description	Address	Access Mode		Reset Value
			Read	Write	
MLI0_ RP0STATR	MLI0 Receiver Pipe 0 Status Register	F010 C07C$_H$	U, SV	BE	0000 0000$_H$
MLI0_ RP1STATR	MLI0 Receiver Pipe 1 Status Register	F010 C080$_H$	U, SV	BE	0000 0000$_H$
MLI0_ RP2STATR	MLI0 Receiver Pipe 2 Status Register	F010 C084$_H$	U, SV	BE	0000 0000$_H$
MLI0_ RP3STATR	MLI0 Receiver Pipe 3 Status Register	F010 C088$_H$	U, SV	BE	0000 0000$_H$
MLI0_ RADRR	MLI0 Receiver Address Register	F010 C08C$_H$	U, SV	BE	0000 0000$_H$
MLI0_ RDATAR	MLI0 Receiver Data Register	F010 C090$_H$	U, SV	BE	0000 0000$_H$
MLI0_ SCR	MLI0 Set Clear Register	F010 C094$_H$	U, SV	U, SV	0000 0000$_H$
MLI0_ TIER	MLI0 Transmitter Interrupt Enable Register	F010 C098$_H$	U, SV	U, SV	0000 0000$_H$
MLI0_ TISR	MLI0 Transmitter Interrupt Status Register	F010 C09C$_H$	U, SV	BE	0000 0000$_H$
MLI0_ TINPR	MLI0 Transmitter Interrupt Node Pointer Register	F010 C0A0$_H$	U, SV	U, SV	0000 0000$_H$
MLI0_ RIER	MLI0 Receiver Interrupt Enable Register	F010 C0A4$_H$	U, SV	U, SV	0000 0000$_H$
MLI0_ RISR	MLI0 Receiver Interrupt Status Register	F010 C0A8$_H$	U, SV	BE	0000 0000$_H$
MLI0_ RINPR	MLI0 Receiver Interrupt Node Pointer Register	F010 C0AC$_H$	U, SV	U, SV	0000 0000$_H$
MLI0_ GINTR	MLI0 Global Interrupt Set Register	F010 C0B0$_H$	U, SV	U, SV	0000 0000$_H$
MLI0_ OICR	MLI0 Output Input Control Register	F010 C0B4$_H$	U, SV	U, SV	1000 8000$_H$
MLI0_ AER0	MLI0 Access Enable Register 0	F010 C0B8$_H$	U, SV	SV, E	0000 0000$_H$

Table 27-14 Address Map of MLI0/MLI1 (cont'd)

Short Name	Description	Address	Access Mode		Reset Value
			Read	Write	
MLI0_ ARR0	MLI0 Access Range Register 0	F010 C0BC$_H$	U, SV	SV, E	0000 0000$_H$
MLI0_ AER1	MLI0 Access Enable Register 1	F010 C0C0$_H$	U, SV	SV, E	0000 0000$_H$
MLI0 ARR1	MLI0 Access Range Register 1	F010 C0C4$_H$	U, SV	SV, E	0000 0000$_H$
–	Reserved	F010 C0C0$_H$ - F010 C0FC$_H$	BE	BE	–
Micro Link Interface 1 (MLI1)					
–	Reserved	F010 C100$_H$	nBE	SV, E	–
–	Reserved	F010 C104$_H$	nBE	nBE	–
MLI1_ ID	MLI1 Module Identification Register	F010 C108$_H$	U, SV	BE	0025 C0XX$_H$
MLI1_ FDR	MLI1 Fractional Divider Register	F010 C10C$_H$	U, SV	SV, E	03FF 43FF$_H$
MLI1_ TCR	MLI1 Transmitter Control Register	F010 C110$_H$	U, SV	U, SV	0000 0110$_H$
MLI1_ TSTATR	MLI1 Transmitter Status Register	F010 C114$_H$	U, SV	BE	0000 0000$_H$
MLI1_ TP0STATR	MLI1 Transmitter Pipe 0 Status Register	F010 C118$_H$	U, SV	BE	0000 0000$_H$
MLI1_ TP1STATR	MLI1 Transmitter Pipe 1 Status Register	F010 C11C$_H$	U, SV	BE	0000 0000$_H$
MLI1_ TP2STATR	MLI1 Transmitter Pipe 2 Status Register	F010 C120$_H$	U, SV	BE	0000 0000$_H$
MLI1_ TP3STATR	MLI1 Transmitter Pipe 3 Status Register	F010 C124$_H$	U, SV	BE	0000 0000$_H$
MLI1_ TCMDR	MLI1 Transmitter Command Register	F010 C128$_H$	U, SV	U, SV	0000 0000$_H$
MLI1_ TRSTATR	MLI1 Transmitter Registers Status Register	F010 C12C$_H$	U, SV	BE	0000 0000$_H$
MLI1_ TP0AOFR	MLI1 Transmitter Pipe 0 Address Offset Register	F010 C130$_H$	U, SV	BE	0000 0000$_H$

Table 27-14 Address Map of MLI0/MLI1 (cont'd)

Short Name	Description	Address	Access Mode		Reset Value
			Read	Write	
MLI1_ TP1AOFR	MLI1 Transmitter Pipe 1 Address Offset Register	F010 C134$_H$	U, SV	BE	0000 0000$_H$
MLI1_ TP2AOFR	MLI1 Transmitter Pipe 2 Address Offset Register	F010 C138$_H$	U, SV	BE	0000 0000$_H$
MLI1_ TP3AOFR	MLI1 Transmitter Pipe 3 Address Offset Register	F010 C13C$_H$	U, SV	BE	0000 0000$_H$
MLI1_ TP0DATAR	MLI1 Transmitter Pipe 0 Data Register	F010 C140$_H$	U, SV	BE	0000 0000$_H$
MLI1_ TP1DATAR	MLI1 Transmitter Pipe 1 Data Register	F010 C144$_H$	U, SV	BE	0000 0000$_H$
MLI1_ TP2DATAR	MLI1 Transmitter Pipe 2 Data Register	F010 C148$_H$	U, SV	BE	0000 0000$_H$
MLI1_ TP3DATAR	MLI1 Transmitter Pipe 3 Data Register	F010 C14C$_H$	U, SV	BE	0000 0000$_H$
MLI1_ TDRAR	MLI1 Transmitter Data Read Answer Register	F010 C150$_H$	U, SV	U, SV	0000 0000$_H$
MLI1_ TP0BAR	MLI1 Transmitter Pipe 0 Base Address Register	F010 C154$_H$	U, SV	U, SV	0000 0000$_H$
MLI1_ TP1BAR	MLI1 Transmitter Pipe 1 Base Address Register	F010 C158$_H$	U, SV	U, SV	0000 0000$_H$
MLI1_ TP2BAR	MLI1 Transmitter Pipe 2 Base Address Register	F010 C15C$_H$	U, SV	U, SV	0000 0000$_H$
MLI1_ TP3BAR	MLI1 Transmitter Pipe 3 Base Address Register	F010 C160$_H$	U, SV	U, SV	0000 0000$_H$
MLI1_ TCBAR	MLI1 Transmitter Copy Base Address Register	F010 C164$_H$	U, SV	BE	0000 0000$_H$
MLI1_ RCR	MLI1 Receiver Control Register	F010 C168$_H$	U, SV	U, SV	0100 0000$_H$
MLI1_ RP0BAR	MLI1 Receiver Pipe 0 Base Address Register	F010 C16C$_H$	U, SV	BE	0000 0000$_H$
MLI1_ RP1BAR	MLI1 Receiver Pipe 1 Base Address Register	F010 C170$_H$	U, SV	BE	0000 0000$_H$

Table 27-14 Address Map of MLI0/MLI1 (cont'd)

Short Name	Description	Address	Access Mode		Reset Value
			Read	Write	
MLI1_ RP2BAR	MLI1 Receiver Pipe 2 Base Address Register	F010 C174$_H$	U, SV	BE	0000 0000$_H$
MLI1_ RP3BAR	MLI1 Receiver Pipe 3 Base Address Register	F010 C178$_H$	U, SV	BE	0000 0000$_H$
MLI1_ RP0STATR	MLI1 Receiver Pipe 0 Status Register	F010 C17C$_H$	U, SV	BE	0000 0000$_H$
MLI1_ RP1STATR	MLI1 Receiver Pipe 1 Status Register	F010 C180$_H$	U, SV	BE	0000 0000$_H$
MLI1_ RP2STATR	MLI1 Receiver Pipe 2 Status Register	F010 C184$_H$	U, SV	BE	0000 0000$_H$
MLI1_ RP3STATR	MLI1 Receiver Pipe 3 Status Register	F010 C188$_H$	U, SV	BE	0000 0000$_H$
MLI1_ RADRR	MLI1 Receiver Address Register	F010 C18C$_H$	U, SV	BE	0000 0000$_H$
MLI1_ RDATAR	MLI1 Receiver Data Register	F010 C190$_H$	U, SV	BE	0000 0000$_H$
MLI1_ SCR	MLI1 Set Clear Register	F010 C194$_H$	U, SV	U, SV	0000 0000$_H$
MLI1_ TIER	MLI1 Transmitter Interrupt Enable Register	F010 C198$_H$	U, SV	SV	0000 0000$_H$
MLI1_ TISR	MLI1 Transmitter Interrupt Status Register	F010 C19C$_H$	U, SV	BE	0000 0000$_H$
MLI1_ TINPR	MLI1 Transmitter Interrupt Node Pointer Register	F010 C1A0$_H$	U, SV	U, SV	0000 0000$_H$
MLI1_ RIER	MLI1 Receiver Interrupt Enable Register	F010 C1A4$_H$	U, SV	U, SV	0000 0000$_H$
MLI1_ RISR	MLI1 Receiver Interrupt Status Register	F010 C1A8$_H$	U, SV	BE	0000 0000$_H$
MLI1_ RINPR	MLI1 Receiver Interrupt Node Pointer Register	F010 C1AC$_H$	U, SV	U, SV	0000 0000$_H$
MLI1_ GINTR	MLI1 Global Interrupt Set Register	F010 C1B0$_H$	U, SV	U, SV	0000 0000$_H$

Table 27-14 Address Map of MLI0/MLI1 (cont'd)

Short Name	Description	Address	Access Mode		Reset Value
			Read	Write	
MLI1_ OICR	MLI1 Output Input Control Register	F010 C1B4$_H$	U, SV	U, SV	1000 8000$_H$
MLI1_ AER0	MLI1 Access Enable Register 0	F010 C1B8$_H$	U, SV	SV, E	0000 0000$_H$
MLI1_ ARR0	MLI1 Access Range Register 0	F010 C1BC$_H$	U, SV	SV, E	0000 0000$_H$
MLI1_ AER1	MLI1 Access Enable Register 1	F010 C1C0$_H$	U, SV	SV, E	0000 0000$_H$
MLI1_ ARR1	MLI1 Access Range Register 1	F010 C1C4$_H$	U, SV	SV, E	0000 0000$_H$
–	Reserved	F010 C1C0$_H$ - F010 C1CC$_H$	BE	BE	–

28 General Purpose Timer Array (GPTA®v5)

This chapter describes the General Purpose Timer Array of the TC1798. The GPTA[1] consists of the following units: GPTA0 and GPTA1 with identical functionality; LTCA2 with reduced GPTA0 functionality.

This chapter contains the following sections:

- A summary on the structure and basic functionalities (see **Page 28-4**)
- Functional description of the GPTA®v5 kernel, applicable for GPTA0 and GPTA1 (see **Page 28-8**)
- Register descriptions of all GPTA®v5 kernel specific registers, applicable for GPTA0 and GPTA1 (see **Page 28-160**)
- Functional description of the LTCA2 kernel (see **Page 28-234**)
- Register descriptions of all LTCA2 kernel specific registers (see **Page 28-250**)
- TC1798 implementation-specific details and registers of the GPTA®v5 module, including port connections and control, interrupt control, address decoding, and clock control (see **Page 28-274**).

*Note: The GPTA®v5 kernel register names described in **Section 28.4**, **Section 28.6**, and **Section 28.7.2** will be referenced in the TC1798 User´s Manual by the unit name prefix "GPTA0_" for the GPTA0 unit, by "GPTA1_" for the GPTA1 unit, and by "LTCA2_" for the LTCA2 unit.*

28.1 What is new?

The major updates from GPTAv4 to GPTAv5 are:

- The flexibility to generate on-chip trigger and gating signals have been increased. The GPTAv5 provides 16 such signals. Each of the signals may be mapped to any output signal of a Local or Global Timer Cell. Therefore it is not limited as before to a single group of Global or Local Timer Cells (25% of the GTC or LTC). Limitation now is, that no more than 4 different on-chip trigger and gating signals may be mapped to one group of LTC or GTC. Details concerning this new on-chip trigger and gating signal multiplexer are described in **Section 28.3.4.3** (see **Page 28-108**). This new features is not fully upwards compatible to the GPTAv4. Additional output multiplexer registers have to be configured to achieve the same functionality (see **"Multiplexer Register Array Programming" on Page 28-121**). Some very minor issue may occur due to a minor reduction of on-chip signal and trigger signals compared to GPTAv4, but on the other hand the increased flexibility should nearly always compensated this. The following list summarizes the principle of mapping former GPTAv4 signals to the new GPTAv5 signals:
  - GPTAv4 Signal GPTA0_OUT0 is replaced by GPTAv5 Signal GPTA0_TRIG01
  - GPTAv4 Signal GPTA0_OUT1 is replaced by GPTAv5 Signal GPTA0_TRIG11

1) *TriCore®, C166®, Infineon®, Infineon Technologies®, and GPTA® are trademarks of Infineon Technologies AG.*

- GPTAv4 Signal GPTA0_OUT2 is replaced by GPTAv5 Signal GPTA0_TRIG00
- GPTAv4 Signal GPTA0_OUT3 is replaced by GPTAv5 Signal GPTA0_TRIG10
- GPTAv4 Signal GPTA0_OUT8 is replaced by GPTAv5 Signal GPTA0_TRIG03
- GPTAv4 Signal GPTA0_OUT9 is replaced by GPTAv5 Signal GPTA0_TRIG13
- GPTAv4 Signal GPTA0_OUT10 is replaced by GPTAv5 Signal GPTA0_TRIG02
- GPTAv4 Signal GPTA0_OUT11 is replaced by GPTAv5 Signal GPTA0_TRIG12
- GPTAv4 Signal GPTA0_OUT16 is replaced by GPTAv5 Signal GPTA0_TRIG05
- GPTAv4 Signal GPTA0_OUT18 is replaced by GPTAv5 Signal GPTA0_TRIG15
- GPTAv4 Signal GPTA0_OUT19 is replaced by GPTAv5 Signal GPTA0_TRIG04
- GPTAv4 Signal GPTA0_OUT24 is replaced by GPTAv5 Signal GPTA0_TRIG07
- GPTAv4 Signal GPTA0_OUT26 is replaced by GPTAv5 Signal GPTA0_TRIG17
- GPTAv4 Signal GPTA0_OUT27 is replaced by GPTAv5 Signal GPTA0_TRIG06
- GPTAv4 Signal GPTA0_OUT28 is replaced by GPTAv5 Signal GPTA0_TRIG07
- GPTAv4 Signal GPTA0_OUT4 is no longer available in GPTAv5. This signal was routed to the ERU (TC1766 only) to cover 75% of the GTC and LTC cells as input to Input channel 1. But Signal GPTA0_TRIG12 may be routed to all (100%) GTC and LTC cells due to the on-chip trigger and gating multiplexer and therefore fulfills this requirement already.
- GPTAv4 Signal GPTA0_OUT7 is no longer available in GPTAv5. This signal was routed to the ERU (TC1766 only) to cover 75% of the GTC and LTC cells as input to Input channel 2. But Signal GPTA0_TRIG14 may be routed to all (100%) GTC and LTC cells due to the on-chip trigger and gating multiplexer and therefore fulfills this requirement already.
- To be consistent to TC1797, the double connected input group of IOG3 is renamed to IOG6 and the Output Group OG1-7 are renamed to OG0-OG6 and the OG0 is renamed to IOG7.
- GPTAv4 Signal GPTA0_OUT17 is no longer available in GPTAv5. This signal was routed to the ERU to cover 50% of the GTC and LTC cells as input to Input channel 2. But Signal GPTA0_TRIG14 may be routed to all (100%) GTC and LTC cells due to the on-chip trigger and gating multiplexer and therefore fulfills this requirement already.
- GPTAv4 Signal GPTA0_OUT22 is no longer available in GPTAv5. This signal was routed to the ERU (TC1766 only) to cover 75% of the GTC and LTC cells as input to Input channel 3. But Signal GPTA0_TRIG16 may be routed to all (100%) GTC and LTC cells due to the on-chip trigger and gating multiplexer and therefore fulfills this requirement already.
- GPTAv4 Signal GPTA0_OUT25 is no longer available in GPTAv5. This signal was routed to the ERU to cover 50% of the GTC and LTC cells as input to Input channel 3. But Signal GPTA0_TRIG16 may be routed to all (100%) GTC and LTC cells due to the on-chip trigger and gating multiplexer and therefore fulfills this requirement already.
- GPTAv4 Signal GPTA0_OUT5 is no longer required (Time Trigger CAN) but GPTAv5 Signal GPTA0_TRIG05 is reserved for it.

- To improve effective usage of the Local Timer Cells, a new cell bypassing, so called global bypass, is introduced. This bypassing enables more flexible cell allocation and also reduces the number of LTC required for coherent update. Details on the two different Local Timer Cell Bypass mechanism may be found in the section **"Data Output Line Control" on Page 28-73**. Two different application examples using the global and local bypass may be found in **Section 28.3.3.5**(see **Page 28-85**). This new features is upwards compatible to the GPTAv4.
- Due to the new bypassing mechanism, a new coherent update mechanism has been introduced, the Local Coherent update described within **Section 28.3.3.5** (see **Page 28-85**). This new local coherent update or double action principle, is very useful to update single Local Timer Cells or a couple of Local Timer Cells within a Group sequentially (not simultaneously) without signal distortion (no other signal output beside the previously configured and the new configured). The new update principle allows to update a local timer cell within a group of local timer cells independent of other local timer cells and therefore also not synchronous/coherent to other local timer cells. This new mechanism upgrades the older mechanism of global coherent update. This older principle of global coherent is very useful to update a number of Local Timer Cells simultaneously. This new features is upwards compatible to the GPTAv4.
- The GPTA0/GPTA1, and LTCA2 OUTs are additionally assigned to new ports. Eight new outputs on Port 0, eight new outputs on Port 1, one new output on Port 2, two new outputs on Port 3, fourteen new outputs on Port 5, four new outputs on Port 14, sixteen new outputs on Port 13, and twelve new outputs on Port 14.
- To enable a family concept between TC1797 and TC1767, the GPTA to MSC Interconnection Assignment of MSC0 and MSC1 has been changed. Details can be found in **Section 28.7.4.2** (see **Page 28-287**).
- To fix a design bug for TC1797 and TC1767, the input line IN1 of the GPTA1 now switches the common input of GPTA0/GPTA1/LTCA2 units for connecting to the output of a 4-to-1 multiplexer. This multiplexer is controlled by bit field SCU_SYSCON.GPTAIS and allows the GPTA0/GPTA1/LTCA2 input IN1 to be connected to one out of four port input lines.
- GPTA1 provided the clock base for LTCA2 within the GPTAv4 version. This disables a family concept of products only having a GPTA0 and an LTCA2 (e.g. TC1767). Therefore GPTA0 is now used as clock source for the LTCA2 and GPTA1 is used as clock source for LTCA3.
- The common IN0 of GPTA0/GPTA1/LTCA2 is multiplexed within the SCU to connect either to a port pin or the EXTCLK0 (see **Page 28-296**).

28.2 GPTA®v5 Overview

The TC1798 contains the two General Purpose Timer Arrays (GPTA0 and GPTA1) with identical functionality, plus the additional Local Timer Cell Array (LTCA2). **Figure 28-1** shows a global view of the GPTA®v5 units.

The GPTA®v5 provides a set of timer, compare, and capture functionalities that can be flexibly combined to form signal measurement and signal generation cells. They are optimized for tasks typical of engine, gearbox, and electrical motor control applications, but can also be used to generate simple and complex signal waveforms required for other industrial applications.

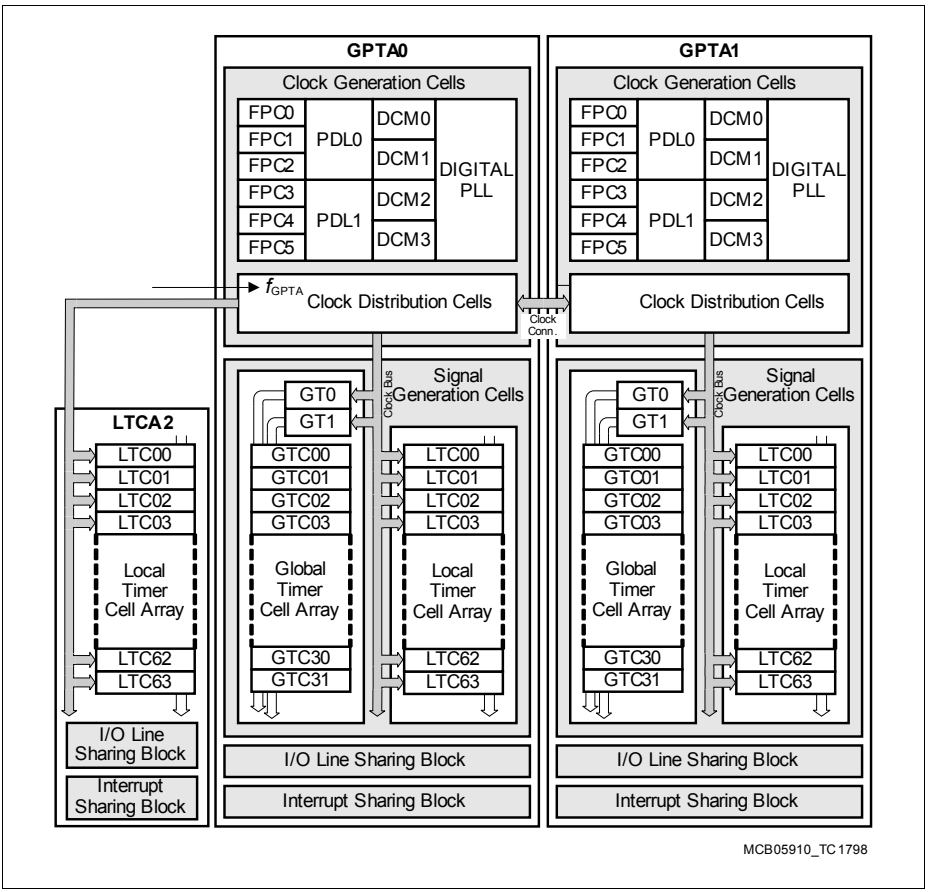


Figure 28-1 General Block Diagram of the GPTA®v5 units in the TC1798

28.2.1 Functionality of GPTA0 and GPTA1

The General Purpose Timer Arrays (GPTA0 and GPTA1) each provides a set of hardware cells required for high-speed digital signal processing:

- Filter and Prescaler Cells (FPC) support input noise filtering and prescaler operation.
- Phase Discrimination Logic cells (PDL) decode the direction information output by a rotation tracking system.
- Duty Cycle Measurement Cells (DCM) provide pulse-width measurement capabilities.
- A Digital Phase Locked Loop cell (PLL) generates a programmable number of GPTA®v5 unit ticks during an input signal's period.
- Global Timer cells (GT) driven by various clock sources are implemented to operate as a time base for the associated Global Timer Cells.
- Global Timer Cells (GTC) can be programmed to capture the contents of a Global Timer on an external or internal event. A GTC may also be used to control an external port pin depending on the result of an internal compare operation. GTCs can be logically concatenated to provide a common external port pin with a complex signal waveform.
- Local Timer Cells (LTC) operating in Timer, Capture, or Compare Mode may also be logically tied together to drive a common external port pin with a complex signal waveform. LTCs – enabled in Timer Mode or Capture Mode – can be clocked or triggered by various external or internal events.
- On-chip Trigger and Gating Signals (OTGS) can be configured to provide trigger or gating signals to integrated peripherals (GPTA0 only).

Input lines can be shared by an LTC and a GTC to trigger their programmed operation simultaneously.

The following list summarizes the specific features of the GPTA®v5 cells.

Clock Generation Cells

- Filter and Prescaler Cell (FPC)
  - Six independent cells
  - Three basic operating modes:
    Prescaler, Delayed Debounce Filter, Immediate Debounce Filter
  - Selectable input sources:
    Port lines, GPTA®v5 unit clock, FPC output of preceding FPC cell
  - Selectable input clocks:
    GPTA®v5 unit clock, prescaled GPTA®v5 unit clock, DCM clock, compensated or uncompensated PLL clock.
  - $f_{GPTA}/2$ maximum input signal frequency in Filter Modes
- Phase Discriminator Logic (PDL)
  - Two independent cells
  - Two operating modes (2- and 3- sensor signals)

  - f_{GPTA}/4 maximum input signal frequency in 2-sensor Mode, f_{GPTA}/6 maximum input signal frequency in 3-sensor Mode
- Duty Cycle Measurement (DCM)
  - Four independent cells
  - 0 - 100% margin and time-out handling
  - f_{GPTA} maximum resolution
  - f_{GPTA}/2 maximum input signal frequency
- Digital Phase Locked Loop (PLL)
  - One cell
  - Arbitrary multiplication factor between 1 and 65535
  - f_{GPTA} maximum resolution
  - f_{GPTA}/2 maximum input signal frequency
- Clock Distribution Cells (CDC)
  - One unit
  - Provides nine clock output signals:
    f_{GPTA}, divided f_{GPTA} clocks, FPC1/FPC4 outputs, DCM clock, LTC prescaler clock

Signal Generation Cells

- Global Timers (GT)
  - Two independent cells
  - Two operating modes (Free-Running Timer and Reload Timer)
  - 24-bit data width
  - f_{GPTA} maximum resolution
  - f_{GPTA}/2 maximum input signal frequency
- Global Timer Cell (GTC)
  - 32 cells related to the Global Timers
  - Two operating modes (Capture, Compare and Capture after Compare)
  - 24-bit data width
  - f_{GPTA} maximum resolution
  - f_{GPTA}/2 maximum input signal frequency
- Local Timer Cell (LTC)
  - 64 independent cells
  - Three basic operating modes (Timer, Capture and Compare) for 63 cells
  - Special compare modes for one cell
  - 16-bit data width
  - f_{GPTA} maximum resolution
  - f_{GPTA}/2 maximum input signal frequency

Interrupt Sharing Block

- 318 interrupt sources, generating up to 108 service requests

On-chip Trigger Block

- 16 on-chip trigger signals

I/O Sharing Block

- Interconnecting inputs and outputs from internal clocks, FPC, GTC, LTC, ports, and MSC interface

28.2.2 Functionality of LTCA2

The Local Timer Cell Array (LTCA2) provide a set of hardware cells required for high-speed digital signal processing:

- Local Timer Cells (LTC) operating in Timer, Capture, or Compare Mode may also be logically tied together to drive a common external port pin with a complex signal waveform. LTCs – enabled in Timer Mode or Capture Mode – can be clocked or triggered by various external or internal events.

The following list summarizes the specific features of the LTCA cells.

Signal Generation Cells

- Local Timer Cell (LTC)
  - 64 independent cells
  - Three basic operating modes (Timer, Capture and Compare) for 63 cells
  - Special compare modes for one cell
  - 16-bit data width
  - f_{GPTA} maximum resolution
  - f_{GPTA}/2 maximum input signal frequency

I/O Sharing Block

- Interconnecting inputs and outputs from internal clocks, LTC, ports, and MSC interface

28.3 GPTA0/GPTA1 Kernel Description

The functionality of the General Purpose Timer Arrays GPTA0/GPTA1 kernel is described in this section. Clock control, address decoding, and service (interrupt) request control are managed outside the GPTA0/GPTA1 unit kernel.

Figure 28-2 shows a global unit diagram of the GPTA®v5 unit kernel.

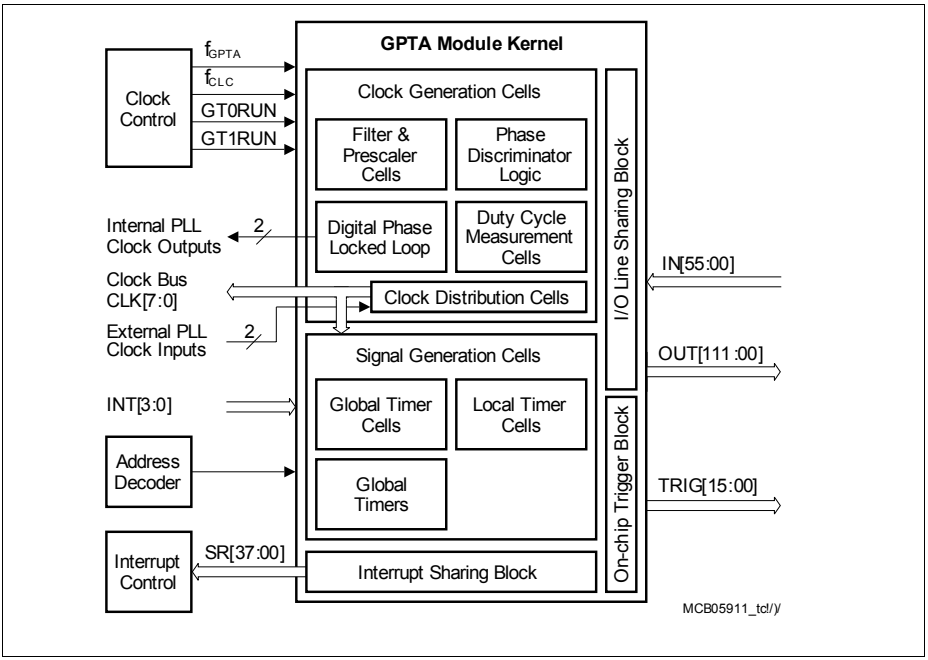


Figure 28-2 Block Diagram of GPTA®v5 Kernel

Each GPTA0/1 kernel has 56 input signals, 112 output signals, and four input signals, that can be connected to port pins or other on-chip logic modules (see **"GPTA®v5 Module Implementation" on Page 28-274** for the TC1798 specific interconnections). Further, several clock input and output signals are provided.

28.3.1 GTPA Units

Each of the General Purpose Timer Arrays GPTA0 and GPTA1 (**Figure 28-2**) is split into Clock Generation Cells (CGC) and a Signal Generation Cells (SGC):

- The **Clock Generation Cells** (see **Page 28-10**) allow a preprocessing of the input signals using filter, timer, capture, compare and enhanced digital PLL cells:
  - The **Filter and Prescaler Cells** (FPC) provide input noise filtering (Immediate Debounce and Delayed Debounce) and may also work as prescalers for the GPTA®v5 module clock and external signals.
  - The **Phase Discrimination Logic** (PDL) may take the outputs of the FPCs to decode phase encoded signals from a position and rotation direction sensor system.
  - The **Duty Cycle Measurement Cells** (DCM) provide signal measurement capabilities (timer plus capture register, single and double capture on rising and falling edges or both) as well as missing pulse detection/reconstruction functions.
  - The **Digital Phase Locked Loop** (Digital PLL) generates a clock with higher clock resolution (harmonic) out of the signal measured by DCM cells. Any arbitrary multiplication factor between 1 and 65535 is supported and may be changed each PLL clock period.
  - The **Clock Distribution Cells** (CDC) provide all LTCs and GTs with a variety of different clock signals. It is equipped with GPTA®v5 module clock prescalers and multiplexers supporting alternate clock sources.

The original signals and all outputs of the preprocessing cells are distributed to the Global Timers and LTCs via the clock bus.

- The **Signal Generation Cells** (see **Page 28-38**) provide a set of timers, capture and compare cells:
  - The two 24-bit **Global Timers** (GT) can be individually configured as free-running counters or as reload counters starting at a programmable value from 0_H to $FFFFFF_H$. Each GT is equipped with a scalable greater-or-equal comparator; the number of bits to be compared is selectable.
  - The **Global Timer Cell** registers (GTC) are 24-bit wide. GTCs may be used as comparators (modifying the logical state of a related output port pin), or as capture cells, storing the current GT0 or GT1 value on rising, falling or both signal edges detected on a related input port pin. Several adjacent GTCs may be connected to logical cells operating on the same pin, allowing complex functions to be implemented.
  - The **Local Timer Cell** registers (LTC) are 16-bit wide. 63 LTCs can be configured to operate in one of four different modes: free-running or resetable counter, capture or compare cell. Adjacent cells can be combined to operate on the same pin, thus generating complex waveforms. One LTC (LTC63) can be used for special compare modes.

28.3.2 Clock Generation Cells

As described in detail in the following sections, the Clock Generation Cells (CGC) provides the following signal pre-processing cells:

- Filter and Prescaler Cell (FPC)
- Phase Discrimination Logic (PDL)
- Duty Cycle Measurement cell (DCM)
- Digital Phase Locked Loop Cell (PLL)
- Clock Distribution Cells (CDC)

The **Filter and Prescaler Cells** (FPC) provide input noise filtering using a debounce filter. FPCs are also able to operate as a prescaler for the GPTA®v5 module clock and external signals. Each FPC can select among different data and clock input signals.

The **Phase Discrimination Logic** (PDL) is able to decode FPC debounce filtered and phase encoded signals coming from a position and rotation direction sensor system. In the PDL, phase encoding can be bypassed.

The **Duty Cycle Measurement Cells** (DCM) provide signal measurement capabilities (timer plus capture register, single and double capture on rising and falling edges or both) as well as missing pulse detection/reconstruction functions.

The **Digital Phase Locked Loop** (PLL) is intended to generate a higher resolution clock out of the values measured by DCM cells. Any arbitrary multiplication factor between 1 and 65535 is supported and may be changed from input clock period to input clock period.

The **Clock Distribution Cells** (CDC) provide all Local and Global Timer Cells with a variety of different clock signals. It is equipped with GPTA®v5 module clock prescalers and multiplexers supporting alternate clock sources.

Figure 28-3 shows how the cells of the CGC are interconnected. The external interface signals of the CGC are:

- GPTA®v5 module clock f_{GPTA}
- GPTA®v5 module input signals (connected to the FPCs)
- Clock bus outputs (generated by the CDC)
- PDL bus outputs
- External PLL clock inputs (fed into CDC)

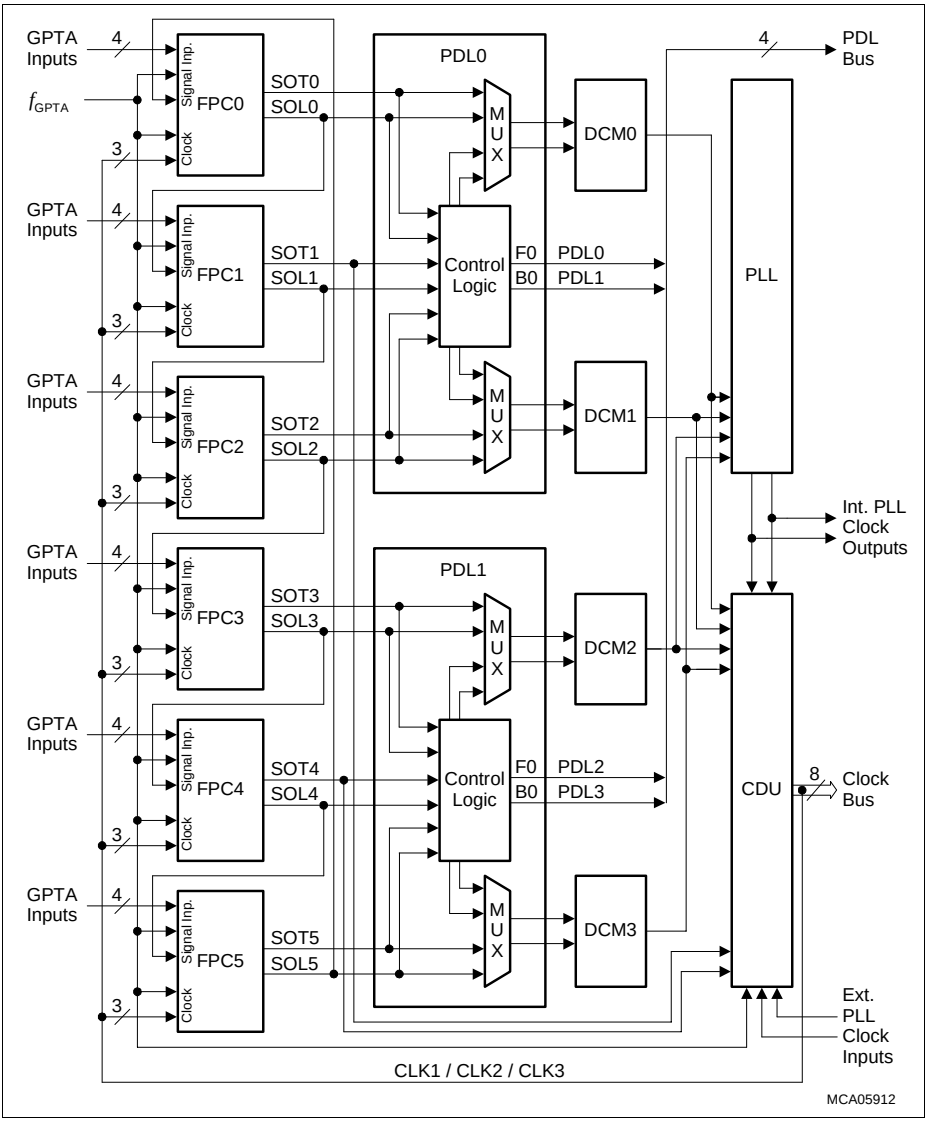


Figure 28-3 Interconnections in the Clock Generation Cells

28.3.2.1 Filter and Prescaler Cell (FPC)

Each GPTA®v5 contains six filter and prescaler cells, FPC0 to FPC5. As shown in **Figure 28-4**, each FPC is equipped with an signal input multiplexer, a clock multiplexer, an edge detection circuitry, a 16-bit timer, a 16-bit compare register, a 16-bit comparator, and a FPC control circuitry (see also **Page 28-126** for the FPC functional algorithm description). The edge detection circuitry detects respective edges for the prescaler modes and detects glitches in all other modes.

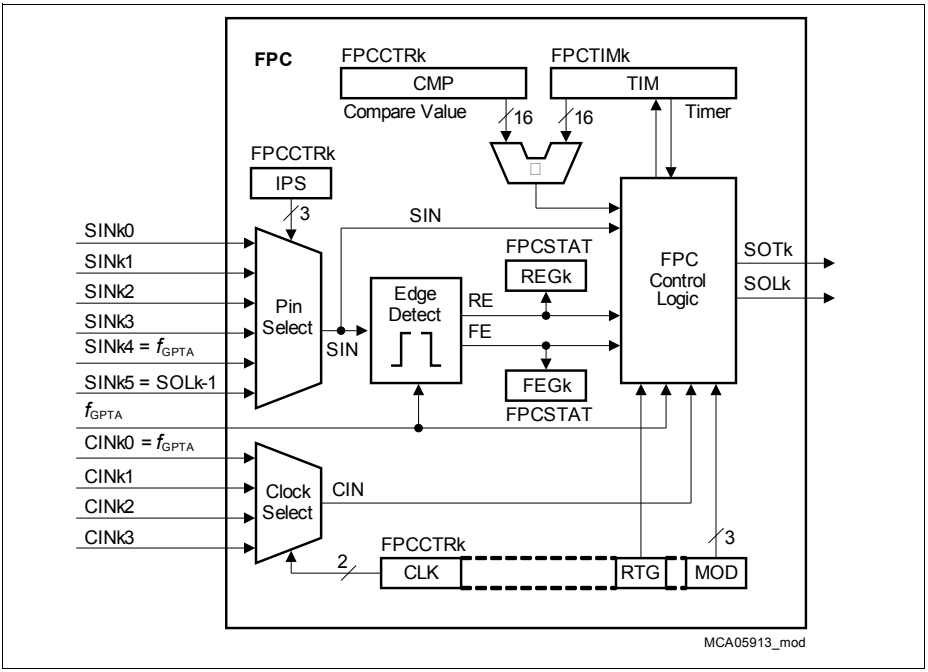


Figure 28-4 Filter and Prescaler Cell Architecture

FPC Registers

The following registers are assigned to the filter and prescaler cells FPCk (k = 0-5):

- FPCSTAT = Filter and Prescaler Cell Status Register (see **Page 28-167**)
- FPCCTRk = Filter and Prescaler Cell Control Register k (see **Page 28-168**)
- FPCTIMk = Filter and Prescaler Cell Timer Register k (see **Page 28-170**)

FPC Operating Modes

Each filter and prescaler cell can be individually configured to operate in one of the following operating modes:

- Delayed Debounce Filter Mode on both edges
- Immediate Debounce Filter Mode on both edges
- Rising edge: Immediate Debounce Filter Mode, falling edge: No filtering
- Rising edge: No filtering, falling edge: Immediate Debounce Filter Mode
- Rising edge: Delayed Debounce Filter Mode, falling edge: Immediate Debounce Filter Mode
- Rising edge: Immediate Debounce Filter Mode, falling edge: Delayed Debounce Filter Mode
- Prescaler Mode (triggered by edge detection circuitry on rising edge)
- Prescaler Mode (triggered by edge detection circuitry on falling edge)

The operation mode is selected by bit field FPCCTRk.MOD (**Page 28-168**).

FPC Input Signals

Bit field FPCCTRk.IPS (see **Page 28-168**) selects one of the following inputs for FPCk:

- Signal input 0 (SINk0)
- Signal input 1(SINk1)
- Signal input 2 (SINk2)
- Signal input 3 (SINk3)
- GPTA®v5 module clock f_{GPTA} (SINk4)
- Preceding FPC level output signal SOLk-1 (SIN05 is connected to SOL5)

When the preceding FPC level output signal is selected as input, two or more FPCs may be concatenated; for example, to combine a delayed debounce filter and an immediate debounce filter.

The maximum FPC input signal frequency must be less than or equal to the sampling rate ($f_{GPTA}/2$). The assignment of GPTA®v5 I/O line and FPC signal inputs SINk is defined in **“FPC Input Line Selection” on Page 28-102**.

FPC Filter Clocks

Bit field FPCCTRk.CLK (see **Page 28-169**) selects one of four filter clocks for FPCk:

- Clock input line 0 (CINk0) = GPTA®v5 module clock f_{GPTA}
- Clock input line 1 (CINk1) = local PLL clock,
- Clock input line 2 (CINk2) = (prescaled) GPTA®v5 module clock f_{GPTA} or PLL clock from other unit or DCM 3 clock
- Clock input line 3 (CINk3) = DCM 2 clock or PLL clock of other unit or uncompensated PLL clock or uncompensated PLL clock of other unit

When using a PLL clock for the FPC, no software is needed to adapt the FPC filter to changing speed for angle-based input signals. The standard PLL clock can be either the

compensated or uncompensated PLL clock or can be the PLL clock of the other GPTA®v5 units. The uncompensated PLL clock is useful in applications in which bursts (due to acceleration) might disturb the filter function.

With a prescaled GPTA®v5 module clock, very long time filter time periods can be achieved.

Note: All filter operation are always synchronously to f_{GPTA}. Therefore the further signal analysis (e.g. glitch detection) is not processed on the rising edge of the selected filter clock CIN, but on the next rising edge of f_{GPTA} following the rising edge of selected CIN (gated clock principle). Therefore CIN clock rates above f_{GPTA} will lead to non deterministic behavior.

Output Signal Splitting

Two output lines are provided by each FPC cell as follows:

- An trigger output signal SOTk, reporting a falling or rising signal edge on the FPC input by a single f_{GPTA} clock pulse,
- A level output signal SOLk, indicating the direction of the detected signal transition.

This signal-splitting scheme (pair of trigger and level output) provides subsequent PDL and DCM cells with the information about an input signal transition in the same f_{GPTA} clock cycle. This feature avoids cascading a one clock delay per edge detection circuitry implemented at the input of each subsequent cell. **Figure 28-5** shows the FPC output signal splitting scheme.

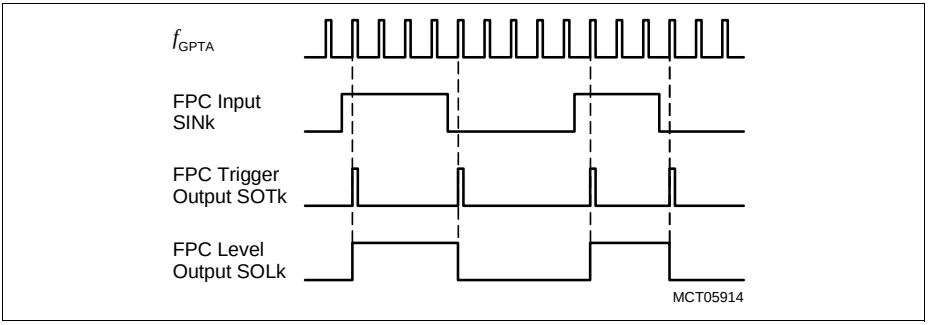


Figure 28-5 FPC Output Splitting into Trigger and Level Information

Delayed Debounce Filter Mode

In Delayed Debounce Filter Mode, the signal input SIN is filtered from all signal transitions and glitches with a width smaller than the selected clock period length multiplied by the compare register value.

The input signal SIN (sampled with f_{GPTA}) is analyzed at the selected filter clock rate of CIN. If the state of the input sample differs from the current output signal value, the 16-bit timer is incremented by one. When the timer register FPCTIMk is not in its idle state (0000_H) **and** the state of the input sample matches the current output signal value, the 16-bit timer is decremented by one (see **Figure 28-6**); if bit FPCCTRk.RTG is set, the timer will be set to idle state again (see **Figure 28-7**). A rising or falling edge, occurring on the signal input line SIN when the timer is greater than zero but less than the compare value, sets the corresponding glitch flag FPCSTAT.REG (on rising edge glitch) or FPCSTAT.FEG (on falling edge glitch). When the timer matches the 16-bit compare value stored in FPCCTRk.CMP (timer threshold), the level output signal line SOLk is inverted, a GPTA®v5 module clock pulse is generated at the trigger output signal SOTk, and the timer is reset to 0000_H. The rising/falling edge glitch flags must be reset by software.

The filter is by-passed if the compare value FPCCTRk.CMP is programmed to zero (0000_H). In this case, the input signal is directly copied to the output signal.

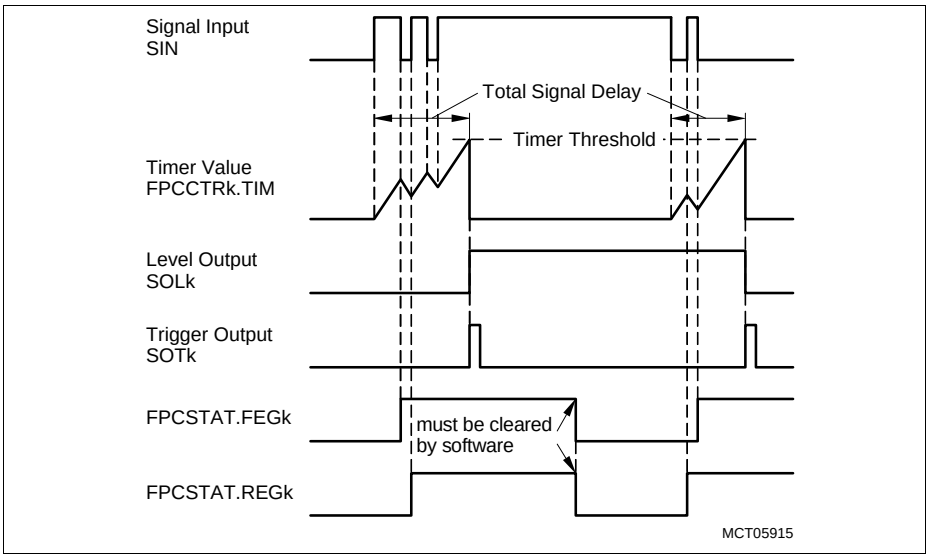


Figure 28-6 FPC Delayed Debounce Filter Algorithm with Timer Decrement

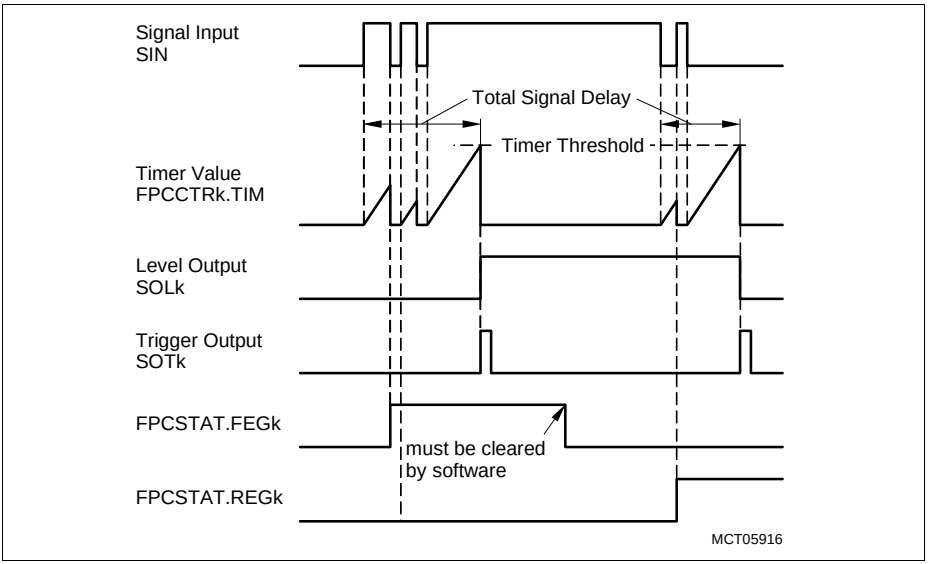


Figure 28-7 FPC Delayed Debounce Filter Algorithm with Timer Reset

The total signal delay from input to output depends on the programmed compare register value, the number of high-frequency pulses (glitches) during the filter operating time, and the timer behavior in case of a glitch (decrement or reset).

The FPC Delayed Debounce Filter Mode is selected by:

- FPCCTRk.MOD = 000_B

Immediate Debounce Filter Mode

In Immediate Debounce Filter Mode, the input signal is filtered from signal transitions and glitches arriving a programmable time after an input signal edge detection (see **Figure 28-8**).

The input signal SIN is sampled with f_{GPTA} and the input signal SIN edge detection is also performed with f_{GPTA}. The further analysis (e.g. filter timer increment, glitch detection) is done at the selected filter clock rate of CIN.

As long as the timer is reset, the FPC control circuitry copies the sampled input value directly to the level output signal line SOLk. When a rising or falling edge occurs on the signal input line SIN and the 16-bit compare value FPCCTRk.CMP is not zero, the timer is enabled to be incremented by the selected clock and the copy mechanism is disabled. When the timer value FPCTIMk.TIM matches the compare value FPCCTRk.CMP, the timer is reset and the copy mechanism is enabled again. A rising or falling edge, occurring on SIN while the timer is greater than zero but less than the compare value, sets the corresponding glitch flag FPCSTAT.REG (on rising edge glitch) or FPCSTAT.FEG (on falling edge glitch). The rising/falling edge glitch flags must be reset by software.

The filter is by-passed if the compare value FPCCTRk.CMP is programmed to zero (0000_H). In this case, the input signal is directly copied to the output signal without any disable periods.

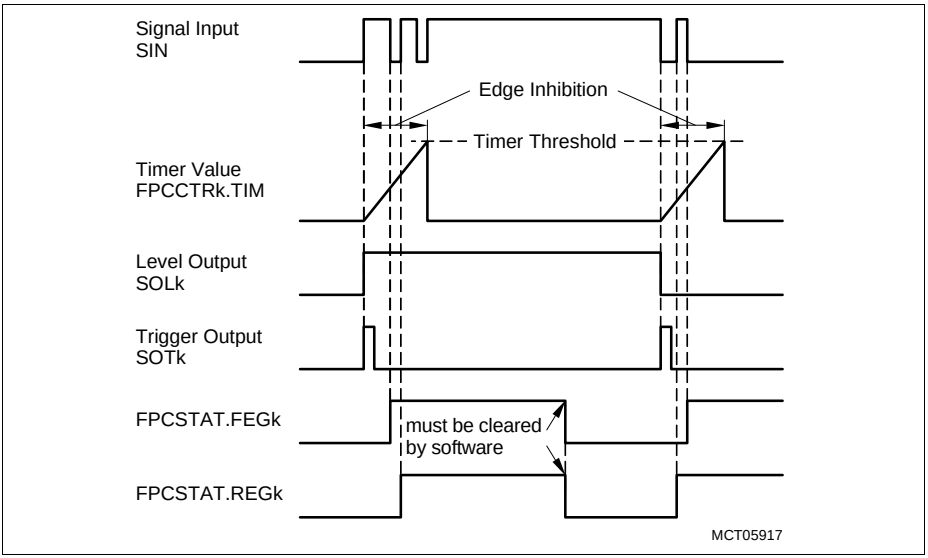


Figure 28-8 FPC Immediate Debounce Filter Algorithm on Both Edges

Note: During the last clock cycle of edge inhibition time (where timer value is equal to the compare value) an input signal glitch will be filtered but the corresponding glitch status flag in register FPCSTAT is not set.

The Immediate Debounce Filter can be enabled only for one edge, either rising or falling. In this case, the signal output follows the signal input value immediately after the timer threshold of the filtered edge is reached, without re-starting the timer (see **Figure 28-9**).

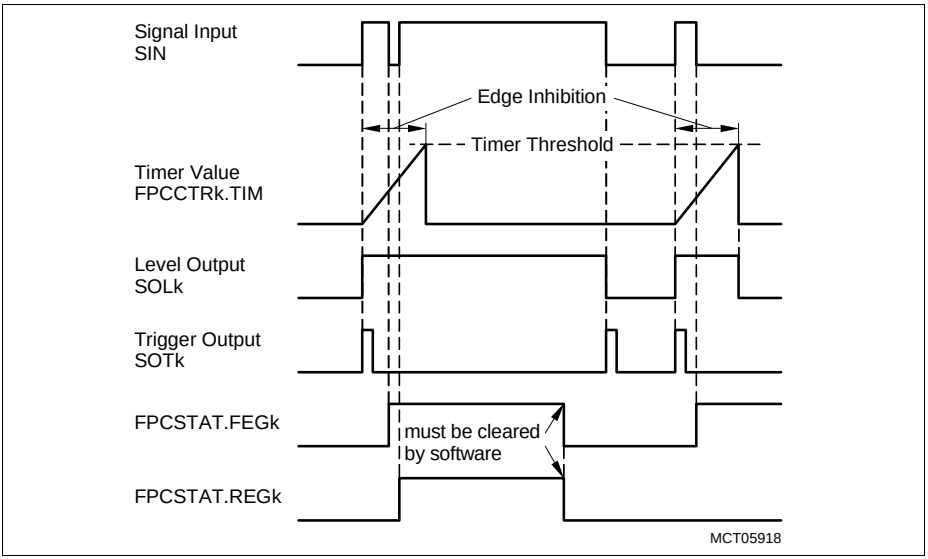


Figure 28-9 FPC Immediate Debounce Filter Algorithm on Rising Edge only

The FPC Immediate Debounce Filter Modes are selected by:

- FPCCTRk.MOD = 001_B: Immediate Debounce Filter Mode on both edges
- FPCCTRk.MOD = 010_B: Immediate Debounce Filter Mode on rising edge only, no filtering on falling edge.
- FPCCTRk.MOD = 011_B: Immediate Debounce Filter Mode on falling edge only, no filtering on rising edge.

Mixed Filter Modes

In the Mixed Filter Modes, one edge of a signal is filtered in the Delayed Debounce Mode, and the other edge is filtered in the Immediate Debounce Mode. The Debounce Mode is switched when the timer threshold is reached. Note that both filter modes use the same timer threshold in this case (see **Figure 28-10**, demonstrating Delayed Debounce Mode with Timer Decrement on Rising Edge and Immediate Debounce of on Falling Edge).

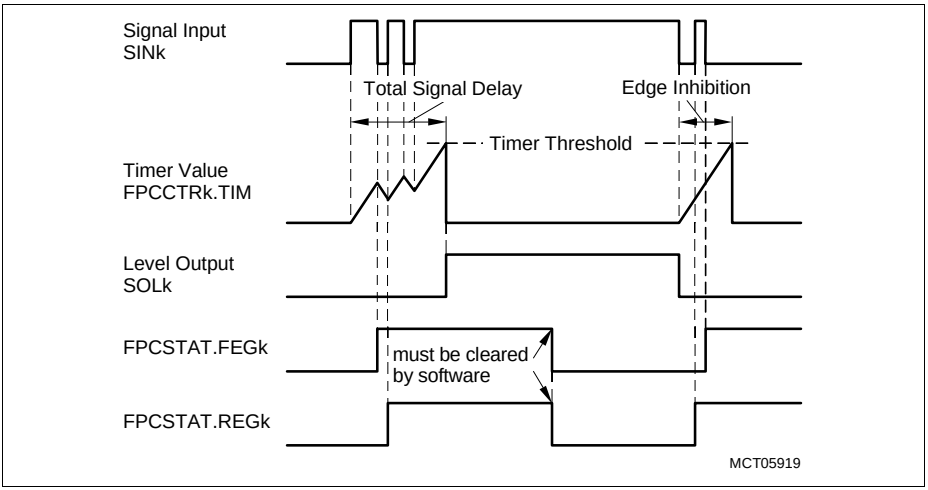


Figure 28-10 FPC Mixed Filter Algorithm

The FPC Mixed Filter Modes are selected by:

- FPCCTRk.MOD = 100_B: Delayed Debounce Filter Mode on rising edge
  Immediate Debounce Filter Mode on falling edge
- FPCCTRk.MOD = 101_B: Immediate Debounce Filter Mode on rising edge
  Delayed Debounce Filter Mode on falling edge

Prescaler Mode

In Prescaler Mode, the input signal is sampled and analyzed with f_{GPTA}. The FPC control circuitry counts each rising (or falling) edge of the input signal. When the timer value matches the compare value:

- one GPTA®v5 module clock pulse is generated at the trigger output signal SOTk and level output signal SOLk
- the timer FPCTIMk.TIM is reset to 0000_H

Figure 28-11 shows a divide-by-6 operation using the FPC in Prescaler Mode with trigger on rising edge selected.

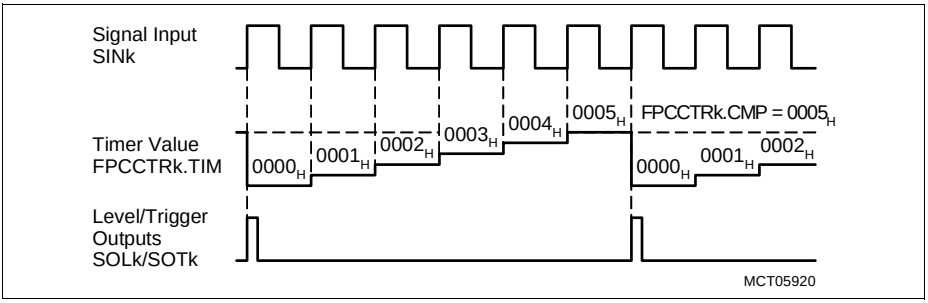


Figure 28-11 FPC Prescaler Mode

For a divide-by-n operation, the compare value FPCCTRk.CMP must be set to n - 1.

The FPC Prescaler Modes are selected by:

- FPCCTRk.MOD = 110_B: Prescaler Mode triggered by edge detection circuitry on rising edge
- FPCCTRk.MOD = 111_B: Prescaler Mode triggered by edge detection circuitry on falling edge

28.3.2.2 Phase Discrimination Logic (PDL)

The GPTA®v5 provides two Phase Discrimination Logic cells (PDL0, PDL1) driven by two signal lines coming from an FPC cell (for description, see Page 28-14):

- An event input signal
- A level input signal

Both Phase Discrimination Logic cells are controlled by the Phase Discrimination Logic Control Register PDLCTR (see Page 28-171).

Each PDL is equipped with an edge detection circuitry, a phase detection circuitry, a PDL control circuitry, and an output multiplexer. Six output lines are provided by each PDL Cell:

- A forward output signal (F0, F1) is driven by one f_{GPTA} clock pulse if an input signal edge is recognized as forward rotation. These signals can be connected to any Local Timer Cell via the PDL bus.
- A backward output signal (B0, B1) is driven by one f_{GPTA} clock pulse if an input signal edge is recognized as backward rotation. This signal can be connected to any Local Timer Cell via the PDL bus.
- Two pairs of output signals, carrying the bypassed input level and event information from the driving FPC cells or the angular velocity and error information provided by the PDL function. These output lines are directly connected to the adjacent Duty Cycle Measurement Cells, DCM0/DCM1(for PDL0) and DCM2/DCM3 (for PDL1).

The PDL processes the output signal of a 2-sensor or 3-sensor positioning system. With bit PDLCTR.TSEx = 1, a 3-sensor system execution is selected providing the DCM1 and/or DCM3 cell with information concerning erroneous states in the signal input. When PDLCTR.TSEx = 0, a 2-sensor system is selected and DCM1 and/or DCM3 are supplied with the input event and level information from the driving FPC2 and/or FPC5.

The rotation direction, monitored by the connected sensors, is automatically derived from the sequence in which the input signals change. Each edge detected on an input signal line generates a pulse on the F0, F1 forward output lines or on the B0, B1 backward output lines. Input jitter, which might occur if a sensor rests near to one of its switching points, is compensated.

If bit PDLCTR.MUXx = 1, the trigger output signal to DCM0/DCM2 (angular velocity information) is driven by a boolean ‘OR’ operation of the corresponding forward trigger and backward trigger signal while the level output signal at DCM0/DCM2 is at fixed high level. In this case, every pulse at F0/B0 and F1/B1 generates a rising edge at the DCM0/DCM trigger signal.

If bit PDLCTR.MUXx = 0, the associated DCM0/DCM2 signals are directly connected with the input event and level signals from the driving FPC0/FPC3.

To calculate the sensor’s current position, the associated LTCs should be clocked with the PDL forward and backward output pulses. A software operation, subtracting the backward counter contents from the forward counter contents, provides the absolute

position. Dynamic information (speed, acceleration, deceleration) may be obtained by analyzing the angular velocity signal periods with the associated DCM cell.

The maximum input frequency is $f_{GPTA}/4$ for a 2-sensor positioning system and $f_{GPTA}/6$ for a 3-sensor positioning system. To ensure that a transition of any input signal is correctly recognized, its level should be held high or low for at least two f_{GPTA} cycles before it changes (three f_{GPTA} cycles for a 3-sensor positioning system).

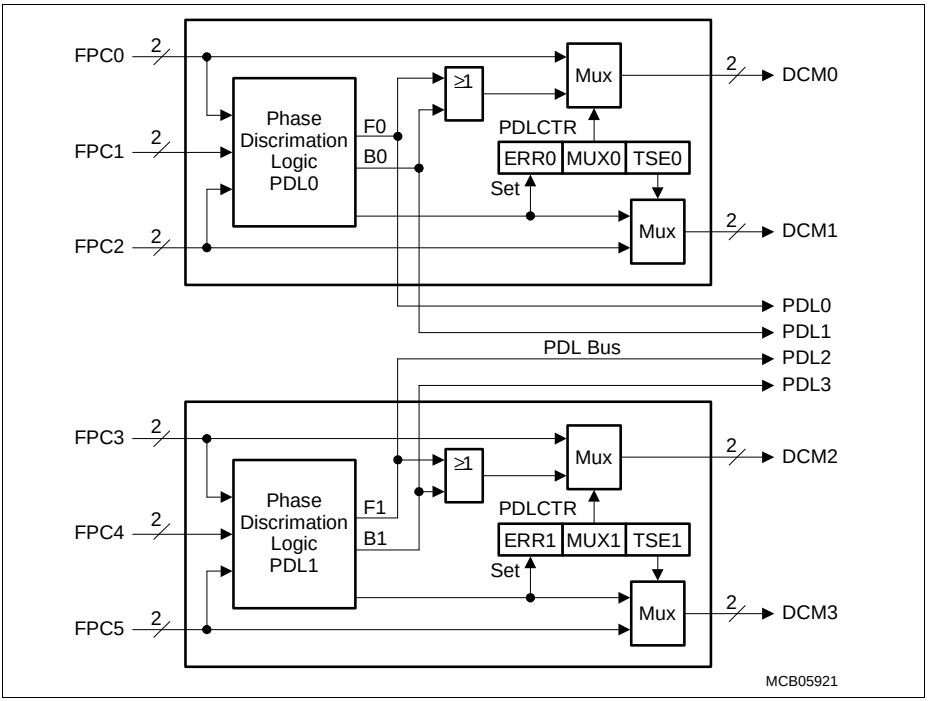


Figure 28-12 Block Diagram of Phase Discrimination Logic Cells

Positioning System With Two Sensors

The 2-sensor Mode is enabled when bit PDLCTR.TSEx is reset. The sensors are mounted at a 90° angle to each other (see **Figure 28-13**). The third sensor input of the PDL cell is internally disabled and DCM1/DCM3 cell inputs are driven by fed-through FPC2/FPC5 output lines.

This configuration can measure an absolute position with a resolution of 90°. No error conditions can be detected.

!	Means not
Re	Means rising edge
Fe	Means falling edge
Forward	ReS1*!S2 + S1*ReS2 + FeS1*S2 + !S1*FeS2
Backward	ReS1*S2 + !S1*ReS2 + FeS1*!S2 + S1*FeS2
Position	Forward_Counter - Backward_Counter

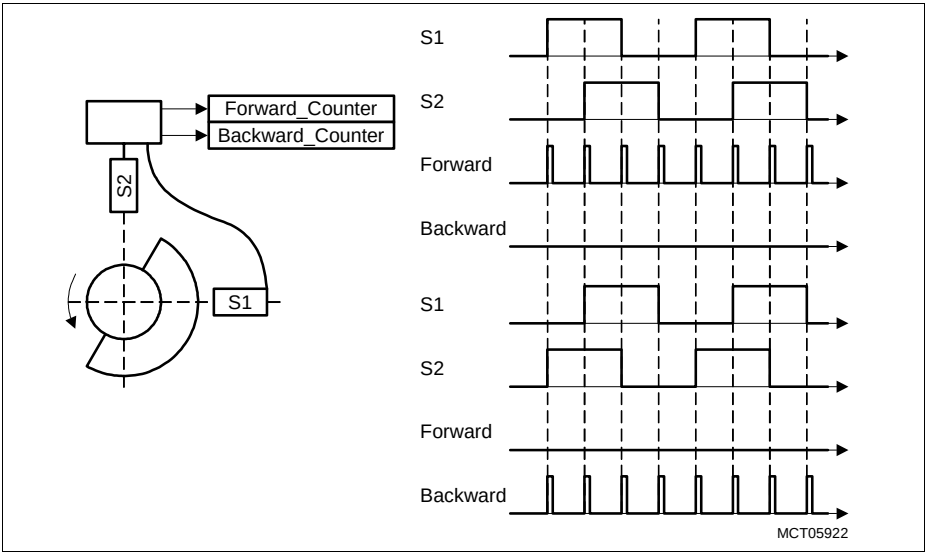


Figure 28-13 Interface Signals of a PDL in a 2-Sensor Positioning System

Figure 28-14 illustrates how the output signals of a 2-sensor system superimposed with noise are processed by the PDL cell. Jitter pulses are completely compensated if they do not occur on both signal lines simultaneously.

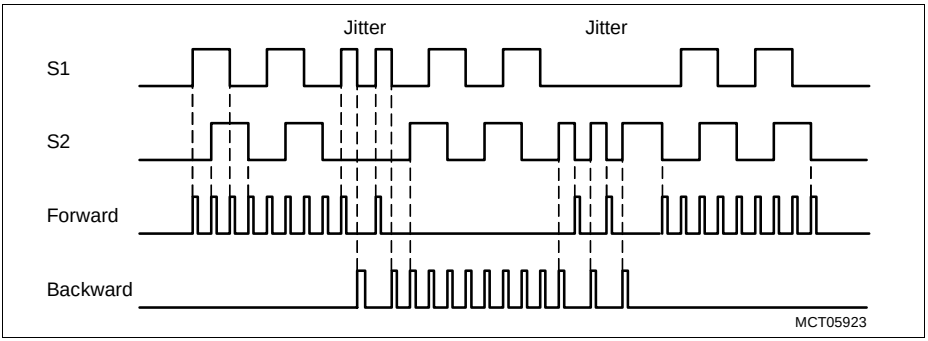


Figure 28-14 Compensation of Input Jitter

Positioning System with Three Sensors

The 3-sensor Mode is enabled when bit PDLCTR.TSEx is set to 1. The sensors are mounted at an 120° angle to each other (see **Figure 28-15**). This configuration can measure an absolute position with a resolution of 60°.

Input signal combinations that are not allowed in a properly-working positioning system (all inputs low or all inputs high) cause the following to occur:

- An error signal is generated, driving the Duty Cycle Measurement cells DCM1 and/or DCM3,
- The error flag PDLCTR.ERRx is set,
- No forward or backward pulses are generated.

When the error disappears, the error signal will be cleared. The error flag PDLCTR.ERRx must be reset by software.

!	Means not
Re	Means rising edge
Fe	Means falling edge
Forward	ReS1*!S2*S3 + FeS3*S1*!S2 + ReS2*S1*!S3 + FeS1*S2*!S3 + ReS3*!S1*S2 + FeS2*!S1*S3
Backward	ReS1*S2*!S3 + FeS3*!S1*S2 + ReS2*!S1*S3 + FeS1*!S2*S3 + ReS3*S1*!S2 + FeS2*S1*!S3
Error	The input signal states S1*S2*S3 and !S1*!S2*!S3 are not allowed
Position	Forward_Counter - Backward_Counter

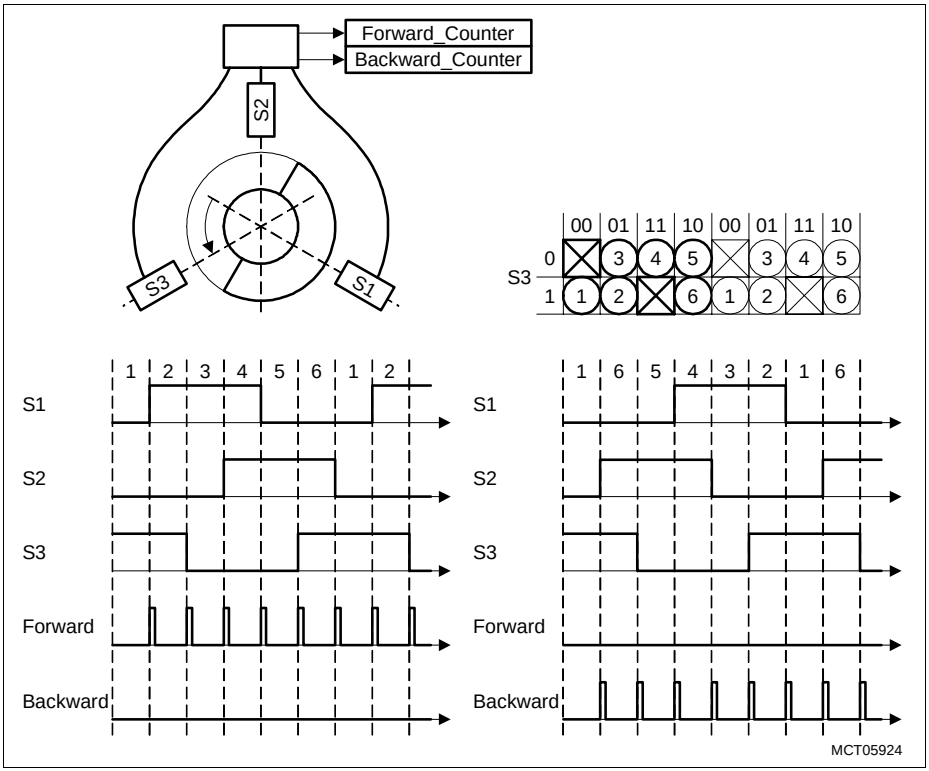


Figure 28-15 Interface Signals of a PDL in a 3-Sensor Positioning System

Jitter pulses are completely compensated as illustrated in **Figure 28-14**.

28.3.2.3 Duty Cycle Measurement Cell (DCM)

The GPTA®v5 contains four DCM cells (DCM0 to DCM3). The input signal to be analyzed is delivered as a 2-line signal input (see **Figure 28-5** for the event/level input signal splitting scheme). It is build by:

- An event input, and
- A signal level input.

Each DCM cell has four outputs:

- An event output line,
- An interrupt output that can become active at a signal input rising edge,
- An interrupt output that can become active at a signal input falling edge,
- An interrupt output that can become active at a compare event.

Each DCM cell is equipped with a 24-bit timer, a 24-bit capture register, a 24-bit capture/compare register, a 24-bit comparator and a DCM control circuitry (**Figure 28-16**).

The following registers are assigned to the DCM cells:

- DCMCTRk = Duty Cycle Measurement Control Register k (see **Page 28-173**)
- DCMTIMk = Duty Cycle Measurement Timer Register k (see **Page 28-175**)
- DCMCAVk = Duty Cycle Measurement Capture Register k (see **Page 28-175**)
- DCMCOVk = Duty Cycle Measurement Capture/Compare Register k (also referred as “CAPCOM”, see **Page 28-176**)
- SRSC0 = Service Request State Clear Register 0 (see **Page 28-223**)
- SRSS0 = Service Request State Set Register 0 (see **Page 28-225**)

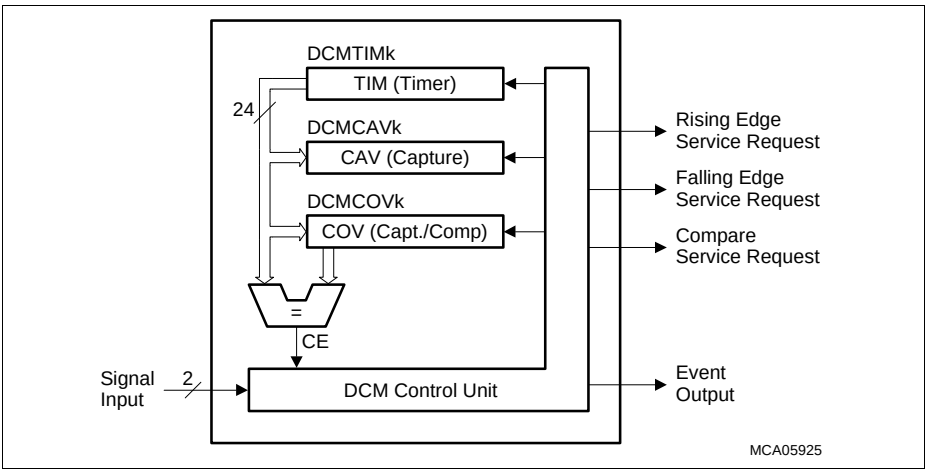


Figure 28-16 Block Diagram of a Duty Cycle Measurement Cell

The DCM cell inputs are connected to the PDL outputs. Depending on the configuration of the associated PDL cell, the DCM cells can also be driven by a FPC directly (as shown in **Figure 28-12**):

- DCM0 is driven by FPC0 or PDL0 angular velocity signal,
- DCM1 is driven by FPC2 or PDL0 error signal,
- DCM2 is driven by FPC3 or PDL1 angular velocity signal,
- DCM3 is driven by FPC5 or PDL1 error signal.

When the driving FPCs and PDL cells are programmed in feed-through mode, an external port pin signal as selected by the FPC input multiplexer can be directly processed by a DCM cell.

The duty cycle of the DCM cell signal input can be determined by measuring its period length and the width of its low or high state. For this purpose, several operations can be started on an signal input edge:

- **Reset Timer**
  The local timer can be reset on rising, falling, or both edges of the signal input line as selected via control bits DCMCTRk.RZE (for rising edge) and DCMCTRk.FZE (for falling edge). After a reset timer event, the timer is continuously incremented by the GPTA®v5 module clock f_{GPTA} until the next reset condition occurs. If no reset timer event is enabled, the timer operates in Free-Running Timer Mode, repeatedly counting from its lower limit (000000_H) to its upper limit ($FFFFFF_H$).
- **Capture**
  The current timer value is stored in the capture register DCMCAV on the rising edge (DCMCTR.RCA = 1) or falling edge (DCMCTRk.RCA = 0) of the signal input line.
  The current timer value is stored in the capture/compare register DCMCOV on the opposite signal edge as selected by DCMCTRk.RCA and if enabled by bit DCMCTRk.OCA = 1. With DCMCTRk.OCA = 0 the capture/compare register DCMCOV is not affected.
- **Edge Service Request and Interrupt Request**
  On a rising input signal edge of the DCMk cell (k = 0-3) the service request flag SRS0.DCM0kR is set. Additionally, a service request signal is triggered if bit DCMCTRk.RRE = 1. A falling input signal edge sets the service request flag SRS0.DCM0kF. An interrupt request generation on this edge is triggered if bit DCMCTRk.FRE = 1. Both edges of the signal input line initiate an interrupt request when both bits, DCMCTRk.FRE and DCMCTRk.RRE, are set. The interrupt on signal input edges is disabled if both bits are cleared.
- **Hardware Generated Output Pulse**
  A single f_{GPTA} clock pulse is generated on the DCM output line if enabled by control register bit DCMCTRk.RCK (rising edge at signal line) and/or DCMCTRk.FCK (falling edge at signal line) and an appropriate edge is detected at the input.
  The 0% or 100% duty cycle exception (no edge or only one edge detected) can be handled by a **limit checking** option. The expected input signal's maximum period length (measured in f_{GPTA} clock ticks) can be loaded into the capture/compare

register DCMCOV that is continuously compared with the timer value. When the timer is incremented up to the limit stored in capture/compare register, the service request flag SRS0.DCM0xC is set. If the compare service request is enabled (control register bit DCMCTRk.CRE = 1), an interrupt request is generated.

- **Software Generated Output Pulse**
  If the **software** intends to compensate an input pulse backlog, bit DCMCTRk.QCK should be set to 1. This immediately triggers a single **clock pulse generation** on the DCM output signal line.

DCM Interrupt Control

Each DCM cell is able to generate three service request output signals. The service request outputs of a DCMk cell are controlled as shown in **Figure 28-17**. When a service request condition occurs, the corresponding service request flag is always set. The service request output is activated only if it is enabled by the corresponding enable bit. Further details on service request and interrupt handling are provided in section **"Interrupt Sharing Block (IS)" on Page 28-123**.

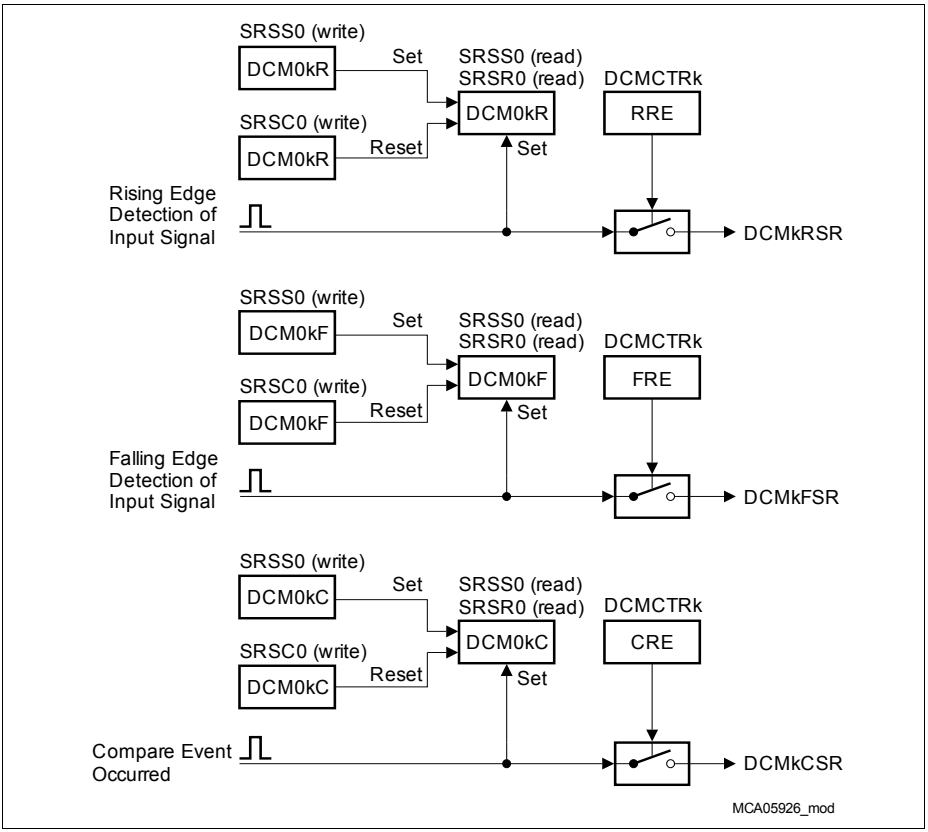


Figure 28-17 DCMk Service Request Generation

28.3.2.4 Digital Phase Locked Loop Cell (PLL)

The GPTA®v5 provides a digital Phase Locked Loop cell (PLL) with a frequency multiplier function. An input signal edge is used as a trigger to generate a programmable number of GPTA®v5 module clocks f_{GPTA} on the output signal line. The four signal output lines of the DCM cells can be used as PLL trigger input. The PLL control circuitry distributes the desired number of GPTA®v5 clocks in regular time intervals over the input signal period length. The PLL can automatically follow an acceleration or deceleration of the input signal. Alternatively, an external software routine may handle the input signal's period length variation.

The PLL includes a 4-channel input multiplexer, a 16-bit timer, a 16-bit step register, a 24-bit reload register, a 24-bit adder, a 24-bit multiplexer, a 25-bit delta register extended by one sign bit and a PLL control circuitry (see **Figure 28-18**).

The following registers are assigned to the Phase Locked Loop cell:

- PLLCTR = Phase Locked Loop Control Register (see **Page 28-177**)
- PLLMTI = Phase Locked Loop Microtick Register (see **Page 28-178**)
- PLLCNT = Phase Locked Loop Counter Register (see **Page 28-179**)
- PLLSTP = Phase Locked Loop Step Register (see **Page 28-179**)
- PLLREV = Phase Locked Loop Reload Register (see **Page 28-180**)
- PLLDTR = Phase Locked Loop Delta Register (see **Page 28-181**)
- SRSC0 = Service Request State Clear Register 0 (see **Page 28-223**)
- SRSS0 = Service Request State Set Register 0 (see **Page 28-225**)

Three output signals are available on the PLL cell:

- PLL signal output line
- Uncompensated PLL signal output line
- Service request line

The desired input signal is selected by programming bit field PLLCTR.MUX. The number of output pulses to be generated within one input signal period must be stored in the microtick register PLLMTI and (coded in 2-complement data format) in the step register PLLSTP. The PLLREV reload register must be programmed with a reload value. This reload value is calculated by subtracting the number of output pulses to be generated within one input signal period from the input signal's period length (measured in number of f_{GPTA} clocks). An automatic compensation of an input signal acceleration or deceleration is enabled by setting bit PLLCTR.AEN to 1 (Automatic End Mode). After disabling the Automatic End Mode, the PLL continuously generates output pulses without synchronization to an input signal edge.

When the counter for the number of remaining output signal pulses PLLCNT decrements to zero, the PLL service request flag is set. Additionally, a service request signal PLLSR will be generated if the control register bit PLLCTR.REN is set.

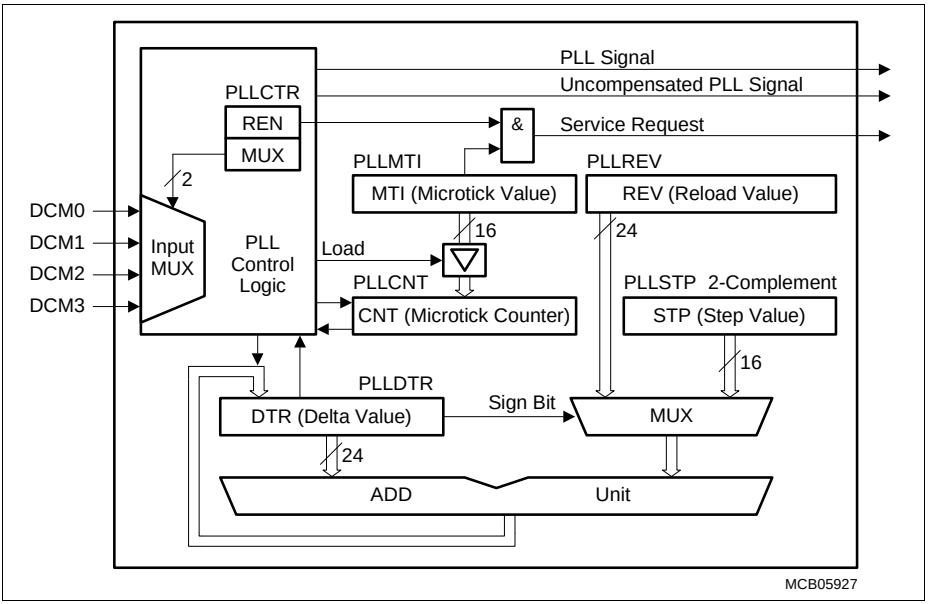


Figure 28-18 Block Diagram of Digital PLL Cell

PLL Interrupt Control

The PLL cell is able to generate a service request output signal PLLSR. This signal is controlled as shown in **Figure 28-19**. When the service request condition PLLCNT = 0 occurs, the service request flag is always set. The service request output PLLSR is activated only if it is enabled by the enable bit PLLCTR.REN. Additional information about service request and interrupt handling are given in section **“Interrupt Sharing Block (IS)” on Page 28-123**.

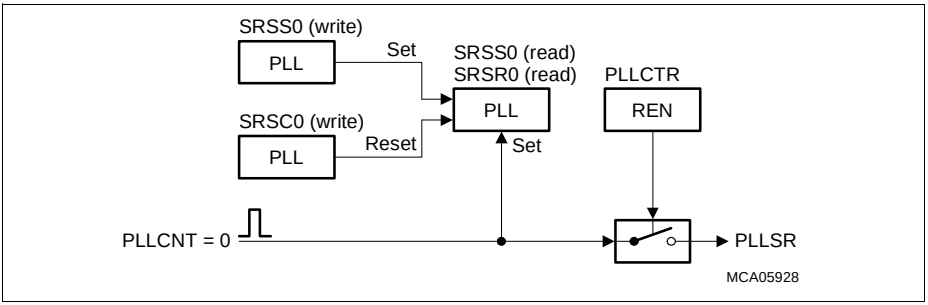


Figure 28-19 PLL Service Request Generation

Steady Input Signal Example

In the following example, the input signal's period length is 13 f_{GPTA} clock periods, which should be subdivided into three equally spaced sections. The reload value to be stored in PLLREV.REV register is calculated to $0A_H$ (10 = 13 - 3). PLLMTI.MTI is loaded with 03_H (number of output pulses) and its 2-complement representation ($FFFD_H$) is written into PLLSTP.STP.

After a reset, a state machine driven by the GPTA®v5 module clock, updates the delta register PLLDTR with the reload value. Afterwards, the PLLSTP register's contents are continuously added to the delta register value (**Figure 28-20**). In fact, the difference between both values is computed and stored in the PLLDTR register again, because the PLLSTP register has been loaded with a negative value (2-complement data format). When the PLLDTR register has been decremented to a negative value, the reload register contents are added to Delta register's current contents.

A rising edge detected on the selected input signal triggers the counter register PLLCNT to load the number of requested output pulses from PLLMTI. When a negative content of the PLLDTR register is detected, the microtick counter is decremented by one. In Automatic Mode (AEN = 1), the output pulse generation is stopped when the microtick counter reaches zero.

The period length of a single output pulse varies between four and five f_{GPTA} clocks; the maximum period length variation of output pulses is restricted to one f_{GPTA} clock. The total period length of all three output pulses, generated by one PLL loop corresponds to the input signal period width (5 + 4 + 4 = 13 f_{GPTA} clocks).

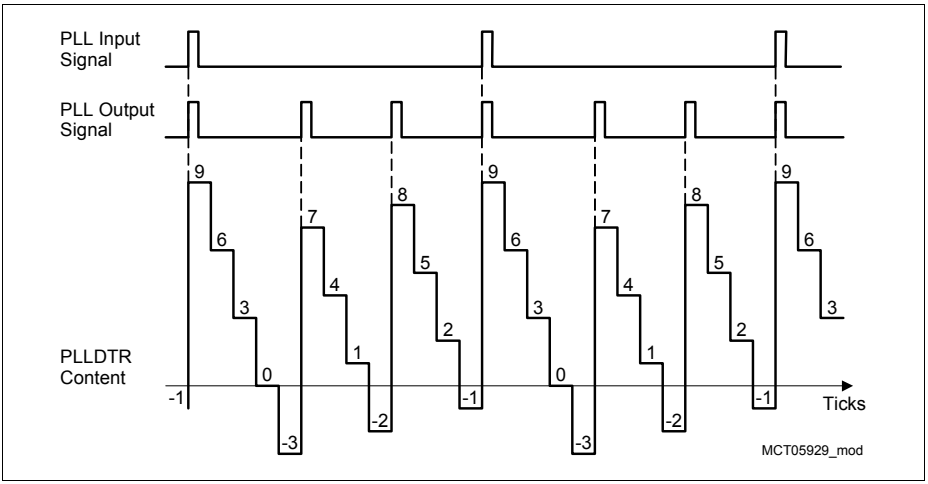


Figure 28-20 Digital PLL Steady State Simulation

This type of PLL implementation presents a valuable advantage compared to classic PLL implementation. Indeed, the generated microticks are equally distributed. The division reminder is distributed to several clocks instead of adding this reminder to the last pulse clock of the period.

Figure 28-21 illustrates this advantage. Considering a period of 15 clock pulses to be divided by a factor of 4, it gives a result of 3 with a reminder equal to 3. The reload value is calculated to $0B_H$ (11 = 15 - 4). The number of output pulses is equal to 4 and its 2-complement representation ($FFFC_H$) is written into the step register.

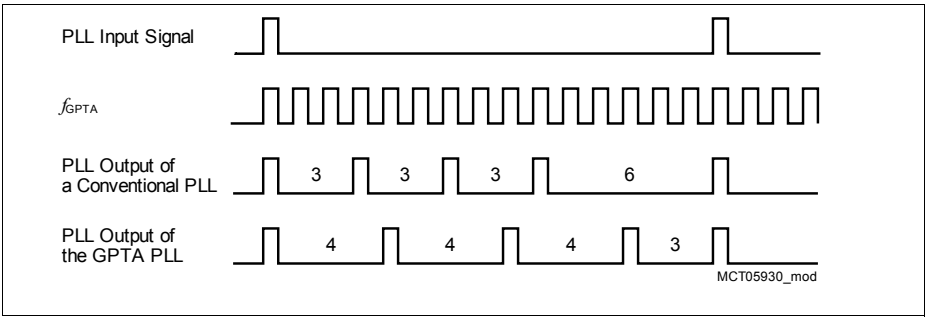


Figure 28-21 Advantage of the GPTA®v5 PLL

Input Signal Acceleration and Deceleration

The consequence of an input signal acceleration or deceleration can be compensated either automatically or by an external software routine. It detects an input signal's period length variation by comparing the current period length (measured in the associated DCM cell) with the expected period length used as calculation base for the PLLREV register contents.

- Compensation of input signal deceleration
  - Compensation by PLL Automatic End Mode
    If Automatic End Mode is enabled (PLLCTR.AEN = 1), the PLL stops at the calculated end of the current input signal period. Due to the deceleration, the rising edge of the following input signal period is delayed, starting the next PLL operation later than expected. A gap occurs between the last output pulse of the current input signal period and the first pulse of the following one (see **Figure 28-22**).
  - Compensation by Software
    After disabling the Automatic End Mode (PLLCTR.AEN = 0), the PLL generates output pulses without synchronization to an input signal edge. In case of a deceleration, more output pulses than calculated are generated during one input signal period. Several algorithms can be implemented to compensate the surplus of generated output pulses:
    The length of the current input signal period has been underestimated by a certain

number of f_{GPTA} clock periods. This deficit could be added to the calculated length of the next input signal period.
The PLL can continue to operate with the old input signal period length estimation, but the number of output pulses to be generated during the next input clock period may be decreased by the surplus of output pulses initiated during the last signal period.

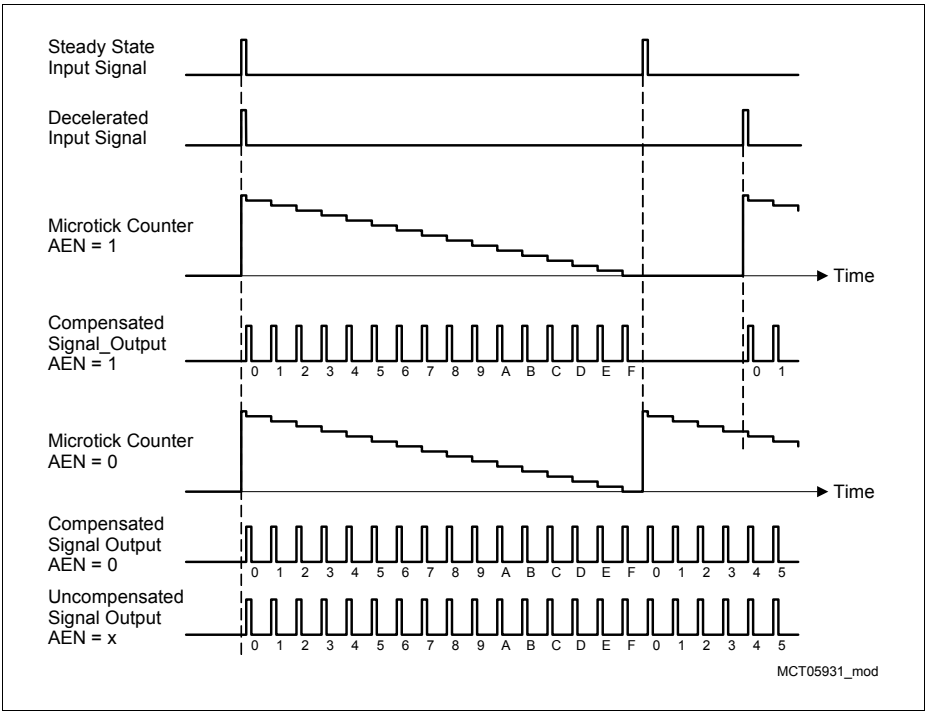


Figure 28-22 Compensation of Input Signal Deceleration

- Compensation of input signal acceleration
  - Compensation by PLL Automatic End Mode
    The next rising edge of the input signal arrives while the counter has not been decremented to zero. The PLL performs all remaining output signal pulses at full speed (f_{GPTA}), when control register bit AEN is set to 1. Afterwards, counter and Delta register are reloaded with their calculated values and the PLL operates at normal speed (see **Figure 28-23**).
  - Compensation by Software
    After disabling the Automatic End Mode, the PLL generates fewer output pulses than calculated during one input signal period. Several algorithm can be

implemented to compensate for the lack of generated output pulses:
The length of the current input signal period has been overestimated by a certain number of f_{GPTA} clock periods. This deficit should be subtracted from the calculated length of the next input signal period.
The PLL can continue to operate with the old input signal period length estimation, but the number of output pulses to be generated during the next input clock period may be increased by the lack of output pulses initiated during the last signal period.

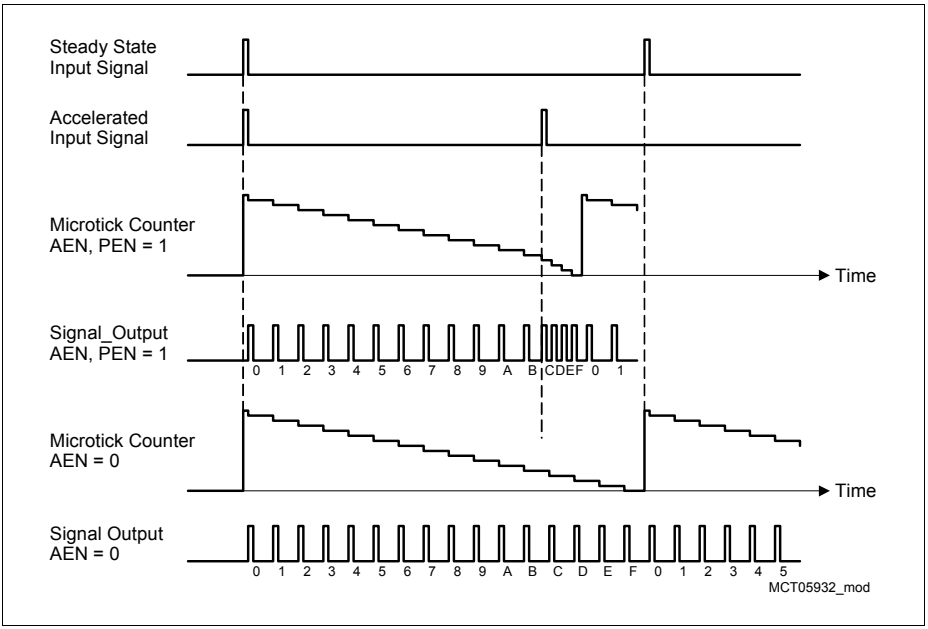


Figure 28-23 Compensation of Input Signal Acceleration

Additionally to the normal output signal, the PLL provides an uncompensated output signal. This signal has no gaps or acceleration bursts. However, the number of microticks during one signal period may be incorrect.

28.3.2.5 Clock Distribution Cell (CDC)

The Clock Distribution Cells (CDC) provides all Local and Global Timer Cells with a clock bus containing eight different clock output signals CLK[7:0] and a special LTC prescaler clock LTCPRE. These nine clock signals are generated out of eleven clock input signals coming from different clock sources (see **Figure 28-24**).

The prescalers divide the GPTA®v5 module clock f_{GPTA} by a programmable 2^n factor. Factor n is defined by bit fields DFA02, DFA04, DFA06 and DFA07 of control register

CKBCTR. A bit field value of 15 disables the related prescaler and selects alternate sources for clock bus lines 2, 4, 6 and 7. For clock bus line CLK2, a bit field value of 14 selects an alternate source.

For clock bus line CLK3, the 2-bit wide bit field DFA03 of control register CKBCTR selects one of the four available clocks.

The LTC prescaler clock LTCPRE is generated by dividing the f_{GPTA} module clock by a factor defined by the 3-bit wide bit field DFALTC of control register CKBCTR. Note that the LTCPRE clock is not a part of the clock bus but a clock signal that is distributed directly from the CDC to each LTC except LTC63.

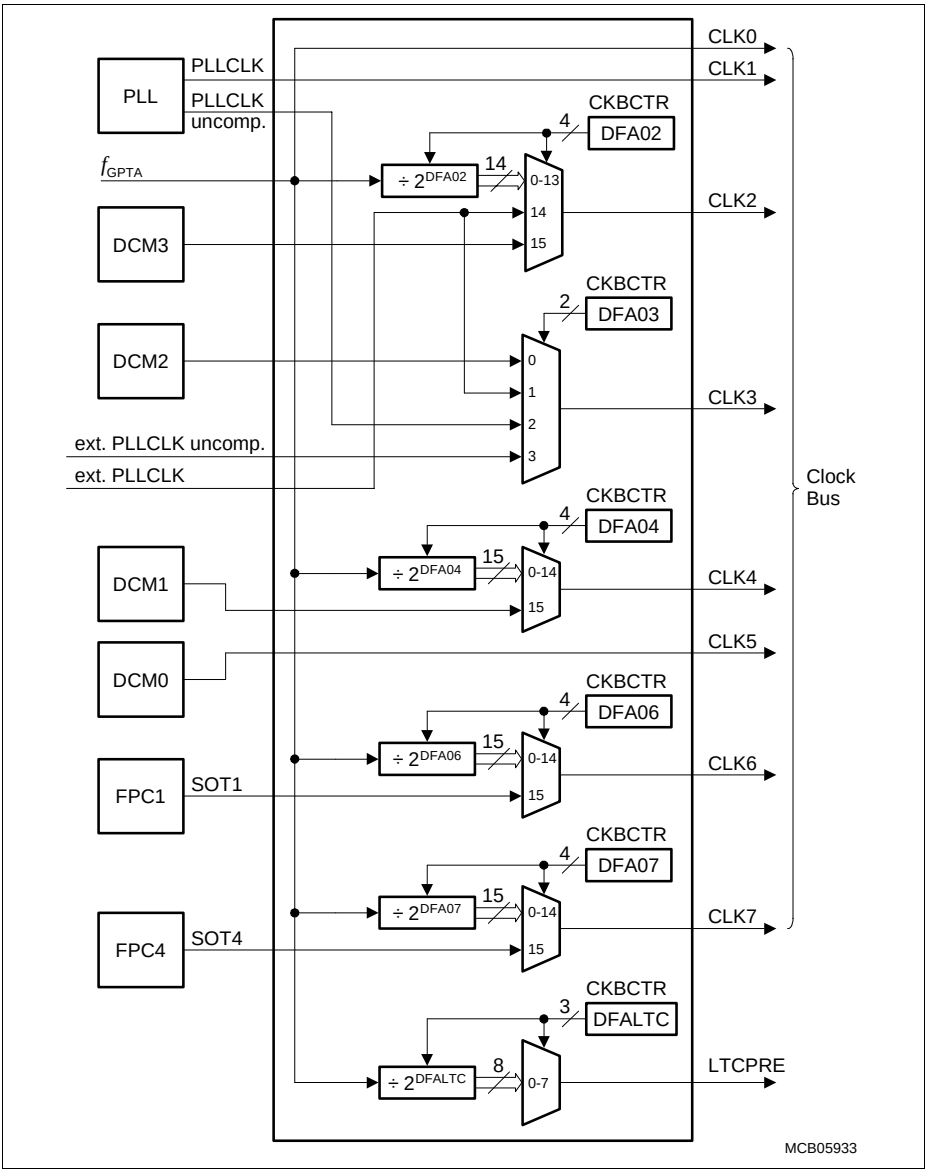


Figure 28-24 Block Diagram of Clock Distribution Cells

28.3.3 Signal Generation Cells

As described in detail in the following sections, the Signal Generation Cells contains the following types of cells:

- Global Timer (GT)
- Global Timer Cell (GTC)
- Local Timer Cell (LTC)

28.3.3.1 Global Timers (GT)

The GPTA®v5 provides two global 24-bit timers (GT) that are connected to the clock bus with its eight clock lines. Each GT is locally equipped with a clock source multiplexer, a 24-bit up-counter, a 24-bit reload register, and a 24-bit greater/equal comparator (see **Figure 28-25**).

Note: Index variable k (= 0, 1) determines the number of the Global Timer.

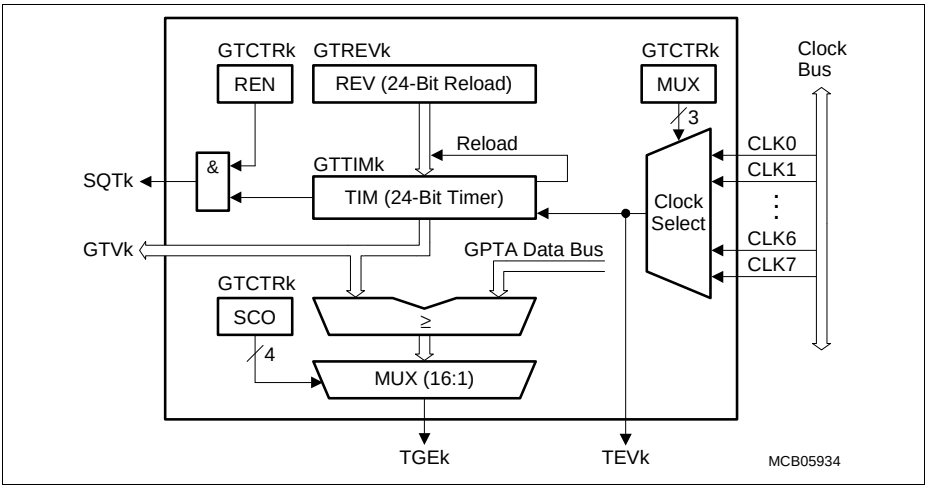


Figure 28-25 Block Diagram of Global Timer (GT)

The following registers are assigned to the Global Timers GTk (k = 0, 1):

- GTCTRk = Global Timer Control Register k (see **Page 28-182**)
- GTREVk = Global Timer Reload Value Register k (see **Page 28-184**)
- GTTIMk = Global Timer Register k (see **Page 28-183**)
- SRSC0 = Service Request State Clear Register 0 (see **Page 28-223**)
- SRSS0 = Service Request State Set Register 0 (see **Page 28-225**)

Each of the two GT cells provides the following input/output signals:

- Eight clock inputs, connected to the clock bus from the clock distribution cells (CDC)
- Global timer value bus GTVk (outputs), carrying the 24-bit GTk counter value
- TEVk output, indicating a GT counter update
- TGEk output, indicating the result of a compare operation
- SQTk service request output, triggered at a timer overflow.

The Global Timer output signals GTVk, TEVk, and TGEk are available as input signals at each GTC (see also **Page 28-56**).

Global timer k can be initialized with a start value, that is written by software into the GTTIMk register. The 24-bit Global Timer value GTTIMk.TIM is incremented by each rising edge of clock input signal TEVk that is selected from the 8-bit clock bus via bit field GTCTRk.MUX. On a Global Timer overflow (transition of $FFFFFF_H$ to 000000_H), the following events occur:

- The 24-bit reload value GTREVk.REV is copied into GTTIMk.TIM
- Bit SRSC0.GT0k is set
- The service request output SQTk is activated (if enabled by bit GTCTRk.REN)

A free-running timer is configured by programming GTREVk.REV with 000000_H.

The “Timer Event” (TEVk) output is activated if the GTk value changes because of a clock edge, a timer reload operation, or a software write access to GTCTRk. The TEVk output is connected to all GTCs. TEVk is used in the GTCs to trigger a compare operation, re-checking the equality of their compare register contents and the updated Global Timer value.

GT Interrupt Control

Each of the GTs is able to generate a service request output signal SQTk. This signal is controlled as shown in **Figure 28-26**. On a GTk timer overflow, the service request flag GT0k is always set. The service request output SQTk is activated only if it is enabled by the enable bit GTCTRk.REN. Additional information about service request and interrupt handling is given in section **"Interrupt Sharing Block (IS)" on Page 28-123**.

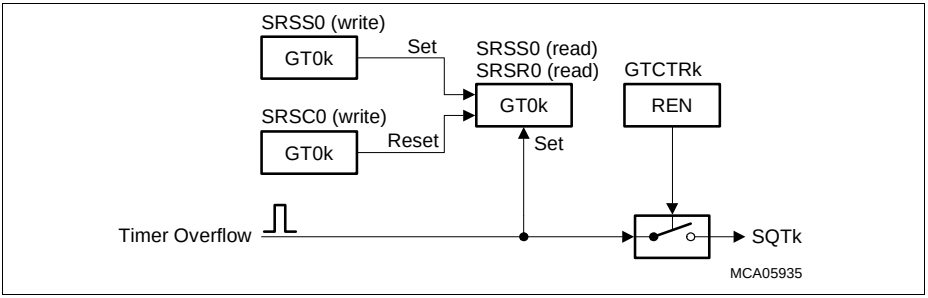


Figure 28-26 GTk Service Request Generation

Synchronization of Global Timers

Both Global Timers, GT0 and GT1, can be enabled and disabled individually. Each GT has its own run signal GTkRUN that is generated outside the GPTA®v5 kernel (see also **Page 28-8**). Signal GTkRUN is generated in a GPTA®v5 clock control circuitry. This external control capability allows the run signals GTkRUN to be controlled in a way that all Global Timers of one ore more GPTA®v5 units can be enabled/disabled synchronously.

The two Global Timers will run synchronously only if all of the following conditions are true:

- Timers use the same input signal
- Timers are started (and stopped, if required) synchronously
- Timers use identical start and reload values
- Timers are not written while they are running

Scalable Signed Greater or Equal Compare

This section (up to **Page 28-54**) explains the **classical timer update problem**, and the solutions supported by the GPTA®v5.

The two Global Timers embedded into the GPTA®v5 include a 24-bit greater/equal comparator. This comparator cell performs compare operations between the GT timer contents and the data value found on the GPTA®v5-internal data bus (coming from a GTC compare register update). The goal of this comparator is to be able to perform an action immediately if the compare cell is updated with a new threshold but the timer has already passed this value. **Figure 28-27** gives an example on this greater/equal concept.

Assumption: a timer is running and a new threshold (value T) is set.

The different points Px represent different cases of present time. When at P1 or P2, the moment represented by T lies in the future and no action is yet required. When at P3 or P4, the moment represented by T lies in the past, and an action is required immediately.

So, the problem is to determine if the threshold T has been passed or not.

Considering an **infinite counter**, the situation is simple. The evaluation consists in determining if point P is before or after T.

Considering a **reloaded counter**, as the timer rolls over at its maximum value, the situation is more complex.

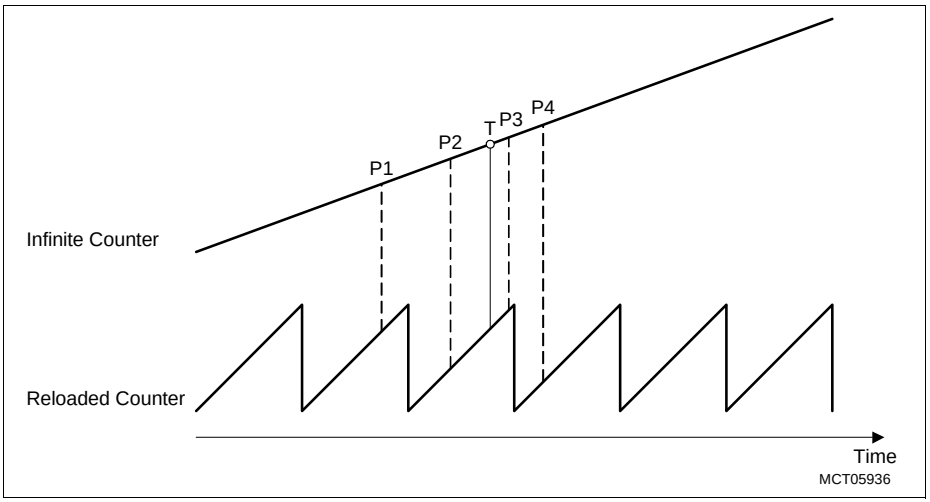


Figure 28-27 Greater/Equal Concept

The **observation window** determines the space in time where writing the value T to the comparator will lead to correct observation (meaning, there is an event if “After”; there is no event if “Before”). Considering an observation window, an event (threshold T) is

programmed and then the window is split into two windows, the “After” window and the “Before” window (**Figure 28-28**). If the timer lies in the “After” window at the time of programming the threshold, the event is performed immediately. If it lies in the “Before” window, the event will happen later when the timer reaches the threshold T. The “Before” window refers to a “prediction range”, and the “After” window refers to the “history buffer”.

From a practical point of view, once the value T is determined, it is necessary to calculate the observation window (position and width). Before updating the value T, the application must assure that the observation window was entered but has not yet been left.

The width of the **observation window** cannot exceed the timer period. To support reloaded counters where the overflow can occur within the observation window, a **signed** comparison is performed.

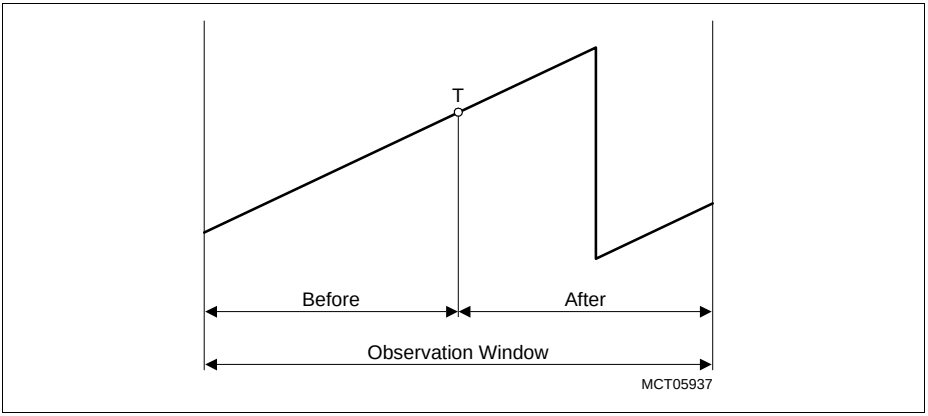


Figure 28-28 Before and After Windows

Comparison Between Unsigned and Signed Compare

To be able to support different timer periods and to support correct observation even beyond timer overflow, the GPTA®v5 embeds the **scalable** and **signed** greater/equal comparator. Using a signed comparison allows one overflow of the timer to occur within the observation window. This is illustrated in **Figure 28-29**.

Using a signed compare in order to take into account the timer overflow, the comparator window is introduced. The comparator window is centered to the point T and its width can be selected by the user.

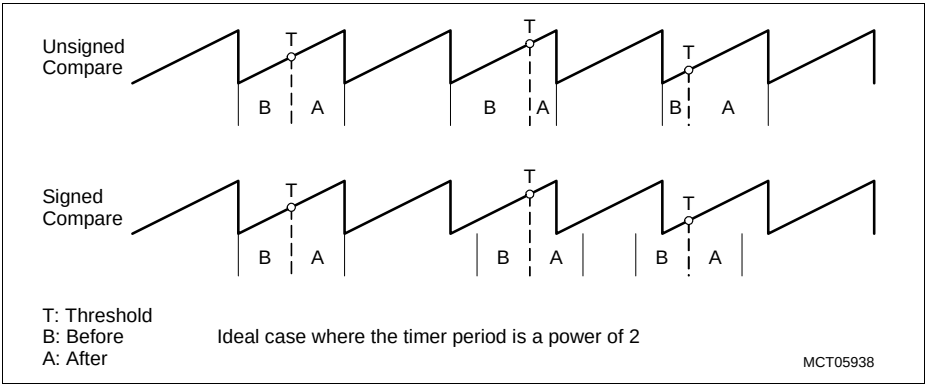


Figure 28-29 Unsigned Versus Signed Compare

When the timer range is a multiple of 2 and because the comparator is scalable, the observation window and the comparator window are identical. See **Figure 28-30**.

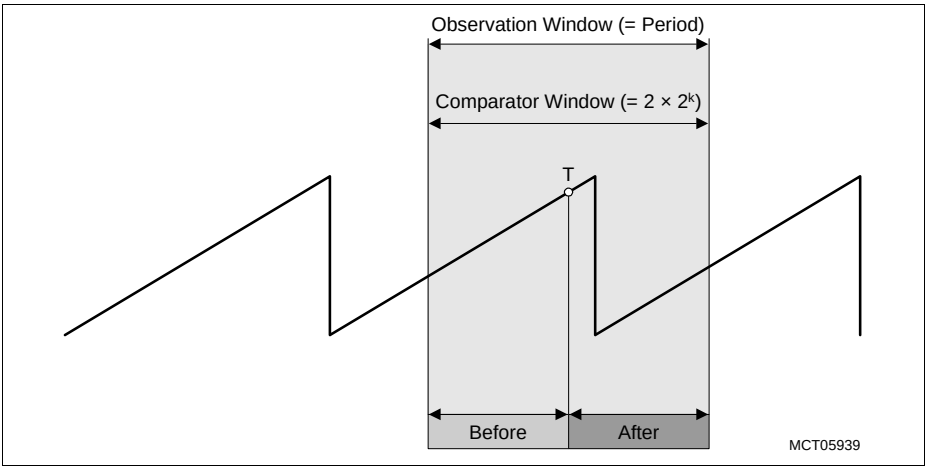


Figure 28-30 Observation and Comparator Windows (timer is a power of 2)

The scalable and signed greater/equal comparator scheme leads to a limitation that must be considered when programming the GPTA®v5 Module. If the timer range is not a power of 2, the comparator window (always a power of 2) will no longer match the timer period. This will impact the observation window as described in the following paragraph.

Observation window for reloaded timers (period is not a power of 2)

In that case, the comparator window must exceed the timer period. The user must find the comparator window (by selecting the scale factor k) which fits best the timer period.

The following equation must apply:

$$2^k < \text{Period} \leq 2 \times 2^k \quad (28.1)$$

Figure 28-31 and **Figure 28-32** show that one part of the comparator window must be discarded in order to avoid inconsistency, resulting in the observation window.

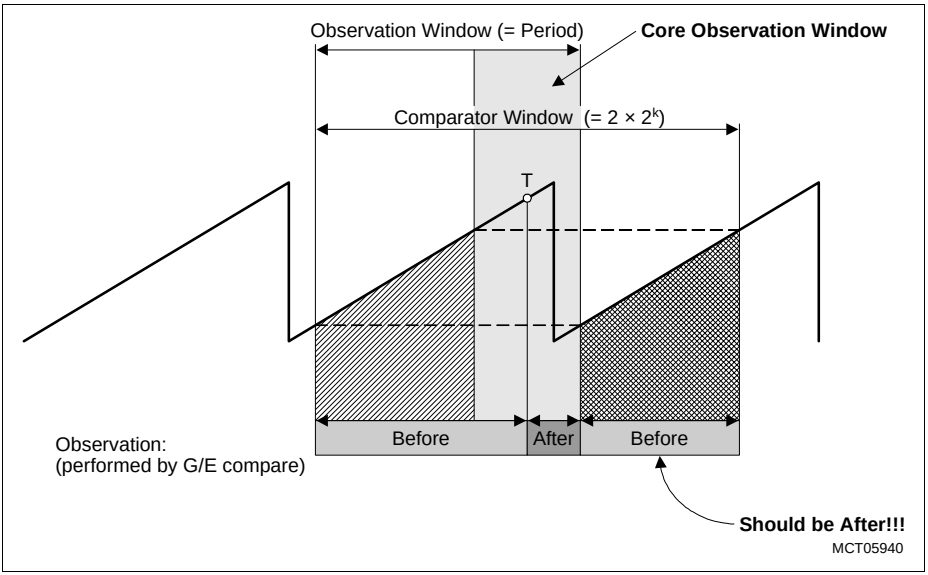


Figure 28-31 Observation Window when Threshold T is High

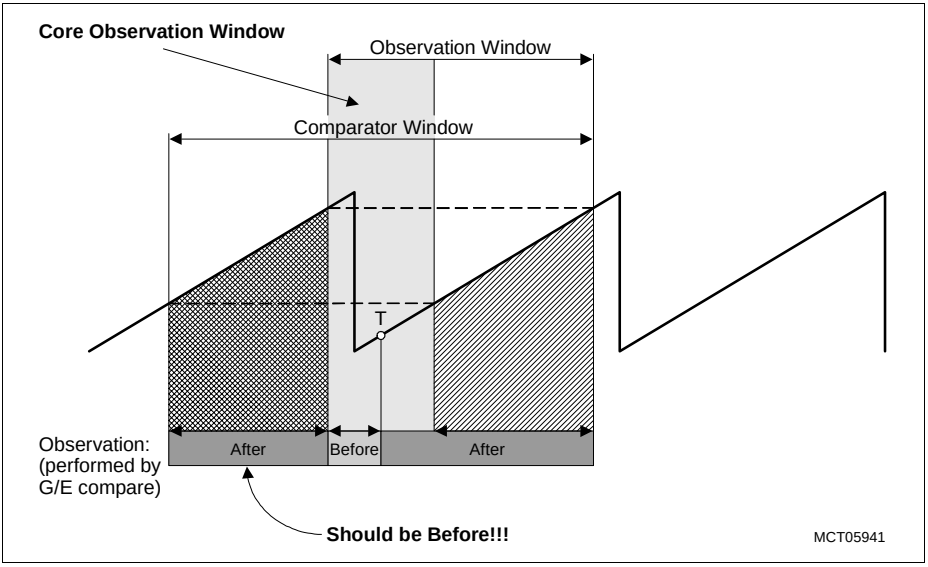


Figure 28-32 Observation Window when Threshold T is Low

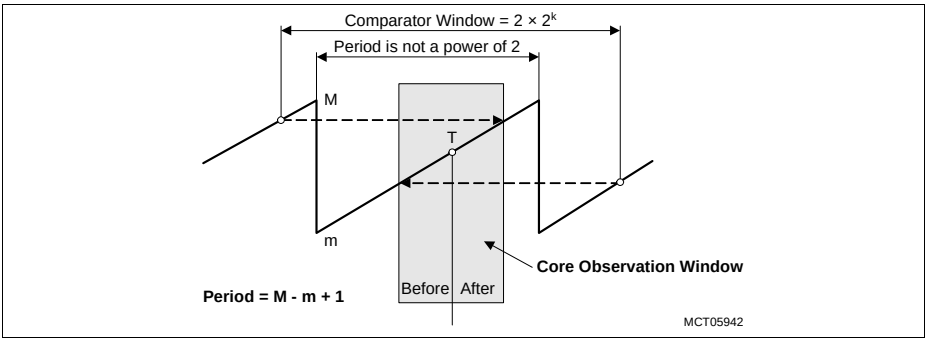


Figure 28-33 The Core Observation Window

A comparison of the previous figures shows that the position of the observation window with respect to T is dependent on the value of T itself. That means the user, before updating the comparator with T, needs to calculate the observation window as a function of T. To avoid this calculation, a **core observation window** can be defined that is independent of T. It will always be centered on T, whatever its value. However, one particularity exists when using the core observation window: the size of the core observation window varies depending on two static values: the timer period and the comparator window's sizes. In particular, the core observation window reduces as the value of the timer period is just after a power of 2. This is shown in **Figure 28-34**.

For any timer period (whatever the range) and any threshold position, a symmetrical core observation window of a statically defined size can be determined.

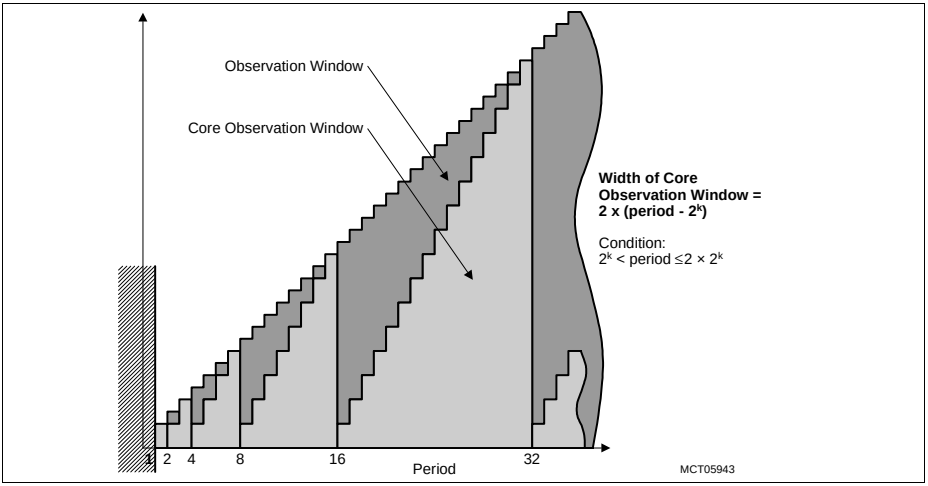


Figure 28-34 Core Observation Window Sizes Versus Period Sizes

Implementation

The hardware implementation of the **scalable and Signed/Unsigned** Greater/Equal compare is illustrated in **Figure 28-35**. The function consists of subtracting the threshold T from the GT timer value. The result is in 2s complement format. The result's sign bit and the 15 most significant bits are at available for observation. One of those bits is selected according to the mode of operation (Unsigned or Signed) and the period length (bit field GTCTRk.SCO). This bit drives the TGE (Timer Greater Equal) flag.

Unsigned compare: Select Sign bit (SCO = $0F_H$)

Signed compare: Select one of the 15 most significant result bits (SCO = 00_H to $0E_H$)

Note: How to choose one of the 15 bits is explained later.

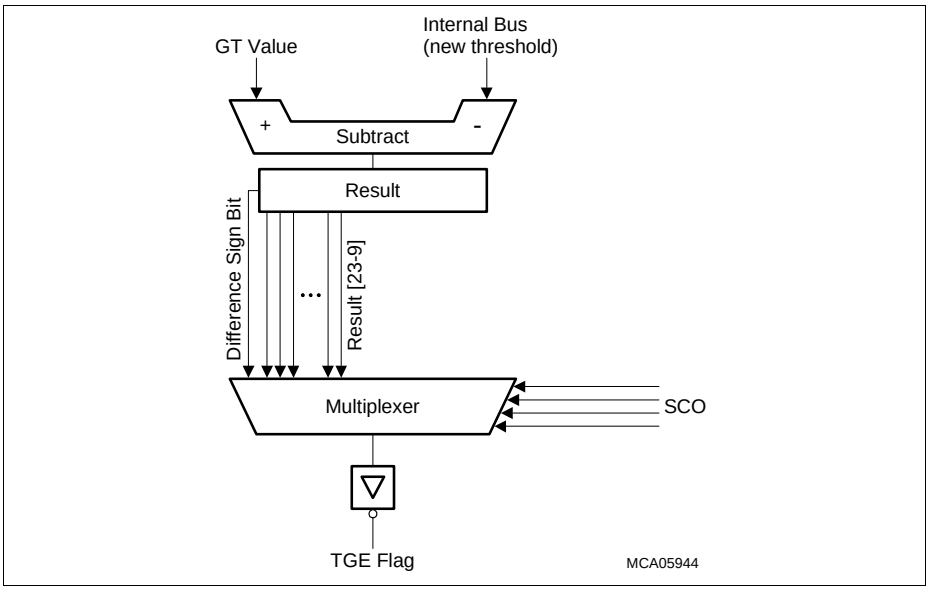


Figure 28-35 Comparator Implemented by a Subtraction Circuitry

The interpretation of the selected result bit is provided in the following simple example: For a 4-bit timer, the subtraction of the threshold T from the timer value, leads to a 4-bit signed result, as illustrated in **Figure 28-36**. This example is selected for simplicity although 4-bit periods are not covered by the implementation.

When using Unsigned compare, the sign bit S is selected. If it equals 0, the result is positive, indicating that the timer is greater or equal the threshold, and hence **After**. If it equals 1, the result is negative, and the observation indicates **Before**.

When using Signed compare, the result bit R_3 can be selected and interpreted, provided that the timer period is at least 9. Here, the range of the result can be split into four sub-

ranges. Because the result is in 2s complement format, a value of 0 for R_3 is interpreted as **After**, and a value of 1 is interpreted as **Before**. A comparison of **Figure 28-36** and **Figure 28-37** shows why this proceeding leads to correct interpretation within the observation window. **Figure 28-37** shows the case of a period equal a multiple of 2.

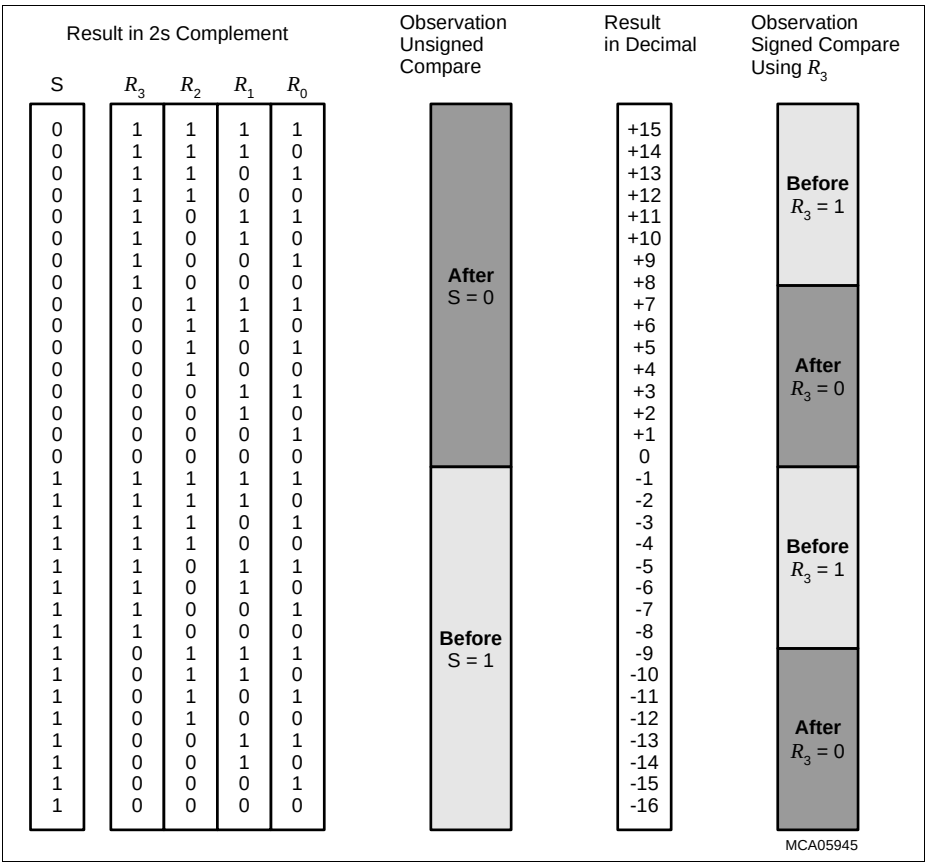


Figure 28-36 Result and Observation for a 4-Bit Timer

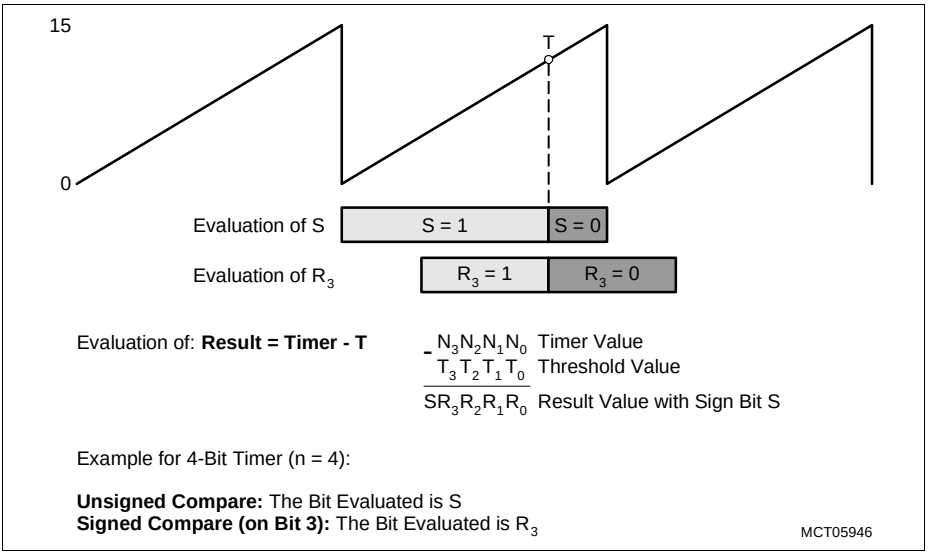


Figure 28-37 Result and Observation (Period = 16)

Figure 28-38 shows the case of a period of 12 which is not a power of 2. Here again, the Table in **Figure 28-36** applies.

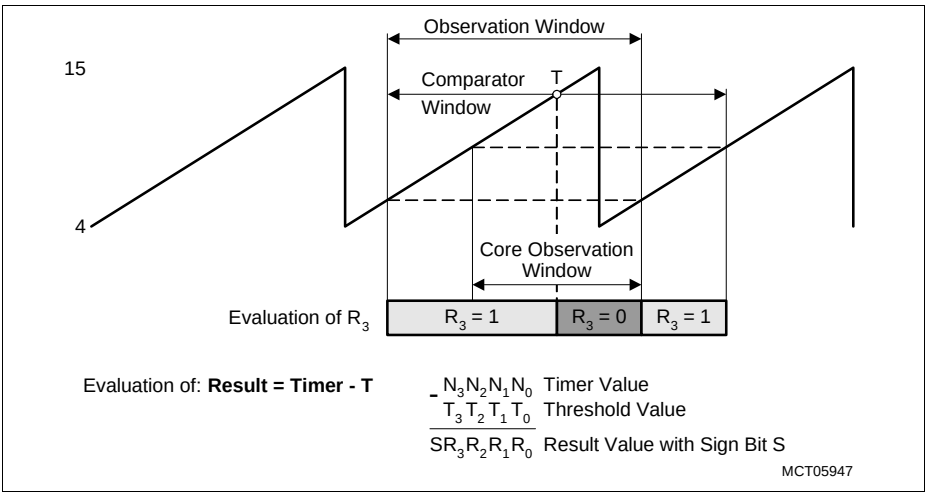


Figure 28-38 Result and Observation (Period = 12)

The previous examples show that the result bit to select for observation (R_3) corresponds to the comparator window's size (k = 3).

Considering the case in which the period is not a multiple of 2, choose a comparator window whose width is between 1 and 2 times the timer period:

$$2^k < \text{Period} \leq 2 \times 2^k \quad (28.2)$$

In no case may the comparator window be equal to or greater than twice the period.

k represents the Result bit to select.

How to Proceed

- Unsigned greater/equal compare:

SCO bit field = $0F_H$ (15_d)

Thereby, the sign bit of the result is selected to drive TGE flag.

This setting is valid for all possible periods. The observation window always matches the period.

- Signed greater/equal compare:

Depending on the period, the appropriate k is selected, so that:

$$\text{Period} = M - m + 1 \; (= \text{Max} - \text{Min} + 1) \quad (28.3)$$

$$2^k < \text{Period} \leq 2 \times 2^k \quad (28.4)$$

SCO bit field = 0 to $0E_H$ (0 to 14_d)

Thereby, the result bit R_k is selected to drive TGE flag.

This setting is possible for periods greater than 512.

Table 28-1 Period Range Depending on Selected k

$2^k < Period \leq 2 \times 2^k$	k	SCO Bit Field (decimal)
0 < period ≤ 512	Not covered by implementation	
512 < period ≤ 1024	9	0
1024 < period ≤ 2048	10	1
2048 < period ≤ 4096	11	2
4096 < period ≤ 8192	12	3
8192 < period ≤ 16384	13	4
16384 < period ≤ 32768	14	5
32768 < period ≤ 65536	15	6
65536 < period ≤ 131072	16	7
131072 < period ≤ 262144	17	8
262144 < period ≤ 524288	18	9
524288 < period ≤ 1048576	19	10
1048576 < period ≤ 2097152	20	11
2097152 < period ≤ 4194304	21	12
4194304 < period ≤ 8388608	22	13
8388608 < period ≤ 16777216	23	14

The width of the core observation window is defined by:

$$2 \times (period - 2^k) \quad (28.5)$$

As a consequence, the width of the “Before” window within the core observation window is (period - 2^k) and the width of the “After” window within the core observation window is (period - 2^k), including the value T.

Additional Information: Illustration on the General Case

The previous section illustrated the greater/equal compare for the particular case of a 4-bit timer. The purpose of this section is to describe the implementation from a general point of view, that is, for a timer period equal to M - m + 1.

In the following figures, the X axis indicates the timer value (elapsing time) and the Y axis indicates the threshold value T. The 45° line starting at (m, m) represents the position in time of T. The graphic shows the observation performed by the hardware for all cases of T (m ≤ T ≤ M).

Figure 28-39 illustrates the Unsigned compare. A particular case is shown in which, for a higher value of T, the observation indicates “Before” at the beginning of the period, and until the timer reaches the value T. Thereafter, the observation switches to “After” and remains there until the timer exits the period.

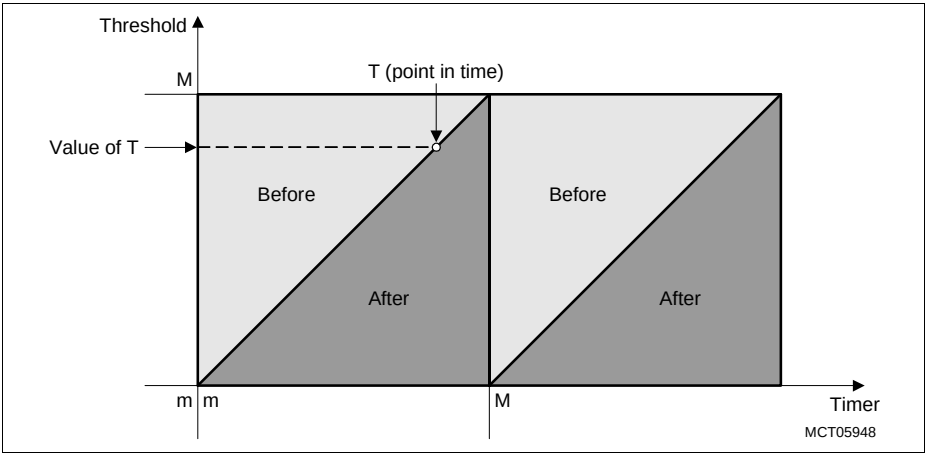


Figure 28-39 Graphical Representation of Unsigned Compare

Figure 28-40 illustrates the Signed compare where the period equals a multiple of 2 (that means $M - m + 1 = 2 \times 2^k$). In this case, for a higher value of T, the observation indicates “After” at the beginning of the period (not yet inside the observation window). When entering the observation window, “Before” is indicated until the timer reaches the value T. Thereafter, the observation switches to “After” and remains there until the timer exits the observation window. This graphic can be related to Table 28-37 where the comparator window equals the period, and the observation window is always centered on the threshold T.

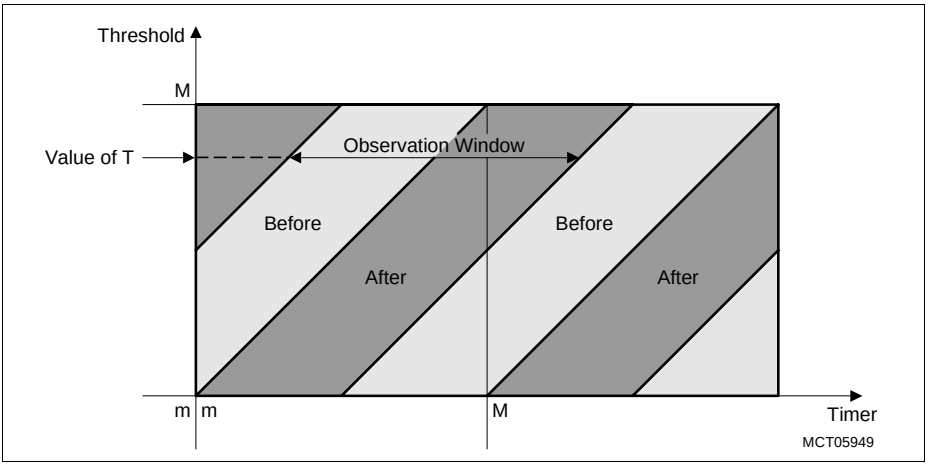


Figure 28-40 Graphical Representation of Signed Compare (Period = 2×2^k)

The **Figure 28-41** illustrates the Signed compare where the period may also be unequal a multiple of 2. The graphical representation of this general case is analogous to the one described in **Figure 28-31**.

If the period is not a multiple of 2, the graphical representation of the Signed compare shows a discontinuity in the “Before” and “After” ranges. Indeed, the widths of the “Before” and “After” windows are not constant, as they depend on the value T. As a consequence, the observation window is not centered on T. The result is that the position of the observation window would have to be re-evaluated for each value T (i.e. determining the widths of the “After” and the “Before” window). For this calculation, the principal characteristic is shown in **Table 28-41** (2×2^k - period = comparator window - period).

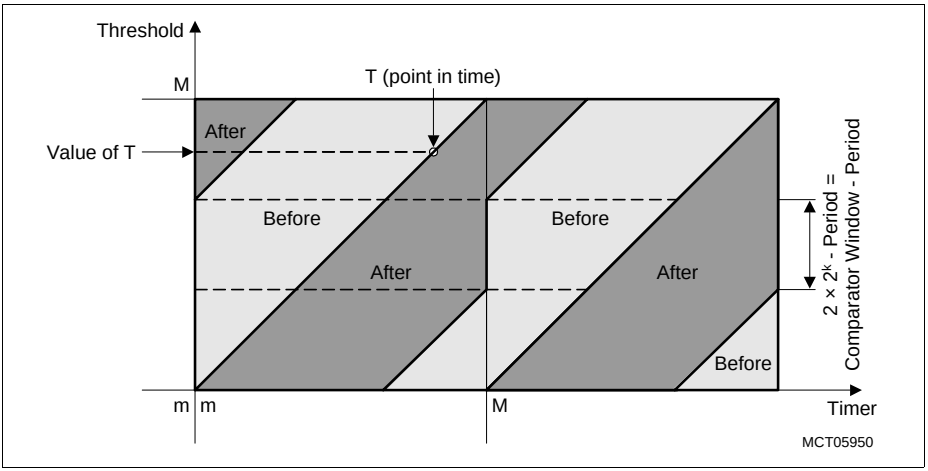


Figure 28-41 Graphical Representation of Signed Compare (2^k < Period ≤ 2 × 2^k)

Figure 28-42 shows how the observation window is positioned with respect to T. It also shows the **core observation window** that is always centered on T and which has a constant width.

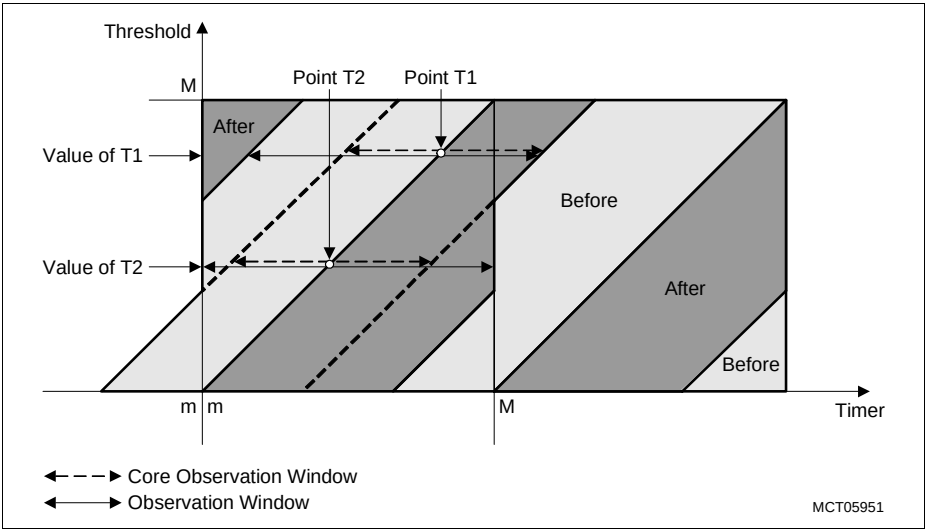


Figure 28-42 Core Observation Window in the Graphic

28.3.3.2 Global Timer Cell (GTC)

The GPTA®v5 provides 32 Global Timer Cells (GTC00 to GTC31) used for capture/compare operations.

Registers

The following registers are assigned to a GTCk (k = 00-31):

- GTCCTRk = Global Timer Cell Control Register k (see **Page 28-187**)
- GTCXRk = Global Timer Cell X Register k (see **Page 28-191**)
- SRSC1 = Service Request State Clear Register 1 (see **Page 28-226**)
- SRSS1 = Service Request State Set Register 1 (see **Page 28-227**)

Features

- **24-bit based timer cells** related to two Global Timers GT0 and GT1.
- **Capture Mode** on rising, falling or both edges with following actions:
  - Service request generation
  - Output signal transition generation (set, reset, toggle the output signal)
- **Compare Mode** on equal compare, or greater than, or equal to compare with following actions:
  - Service request generation
  - Output signal transition generation (set, reset, toggle the output signal)
  - Capture (after compare match) the value of the selected Global Timer or the opposite Global Timer
- **One Shot Mode** allows the selected (capture or compare) mode to be stopped after the first event.
- **Flexible mechanism** to link pin actions and allow complex combination of cells. (A cell has the ability to propagate actions over adjacent cells with higher number, in order to perform complex waveforms such as PWMs).

Architecture

The architecture of a GTC is shown in **Figure 28-43**. Each GTC has a multiplexer that allows selection of the GT0 or GT1 Global Timer value bus as data source, a 24-bit capture/compare register GTCXRk, and a 24-bit equal comparator.

The 32 Global Timer Cells (GTC00 to GTC31) have the following inputs:

- Two Global Timer value buses, GTV0 and GTV1, coming from the two Global Timers and carrying the GT0 and GT1 timer values
- Two inputs, TEV0 and TEV1, reporting GT0 and GT1 timer value updates
- Two inputs, TGE0 and TGE1, reporting the result of the GT0 and GT1 compare operations
- A trigger input (GTCkIN) that is connected via the GTC input multiplexer to one of the following signal sources:

  - External port lines
  - Local Timer Cell outputs
  - Filter and Prescaler Cell outputs
  - Internal input signals INTx
- Two action mode inputs (M0I, M1I) coming from the adjacent GTC with lower order number (M1I and M0I of GTC00 are 0)

Each GTC provides the following outputs:

- One data output (GTCkOUT) that can be connected to:
  - External port lines
  - Inputs of an MSC module
  - Outputs and/or inputs of Local Timer Cell inputs
- Two action mode outputs (M0O, M1O) going to the adjacent GTC with higher order number
- One service request line (SQSk) triggered by a capture/compare event.

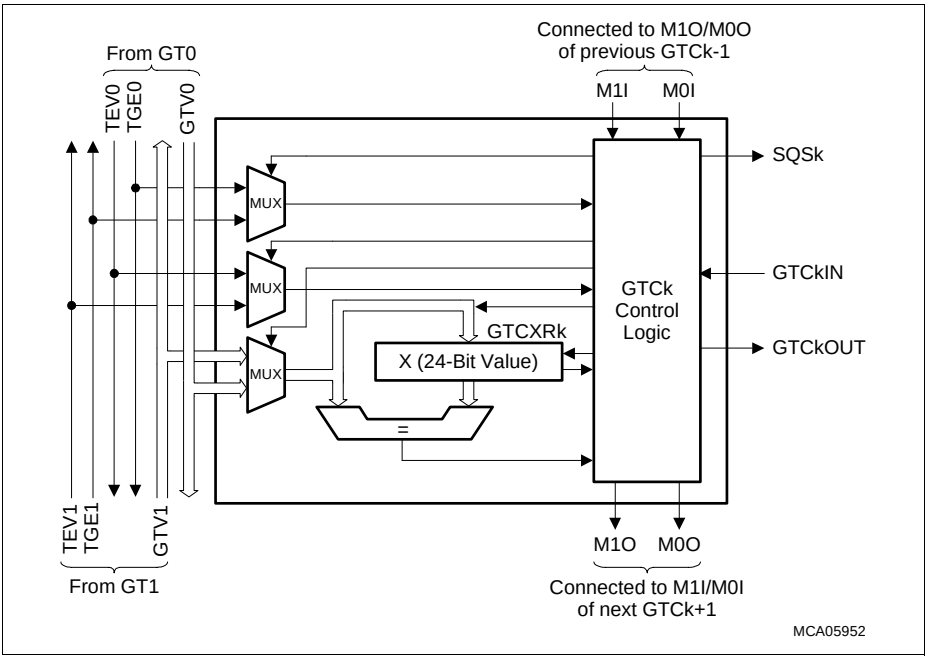


Figure 28-43 Architecture of Global Timer Cells

Figure 28-44 shows how the GTCs are arranged and connected to the adjacent GTCs and with the Global Timers GT0 and GT1.

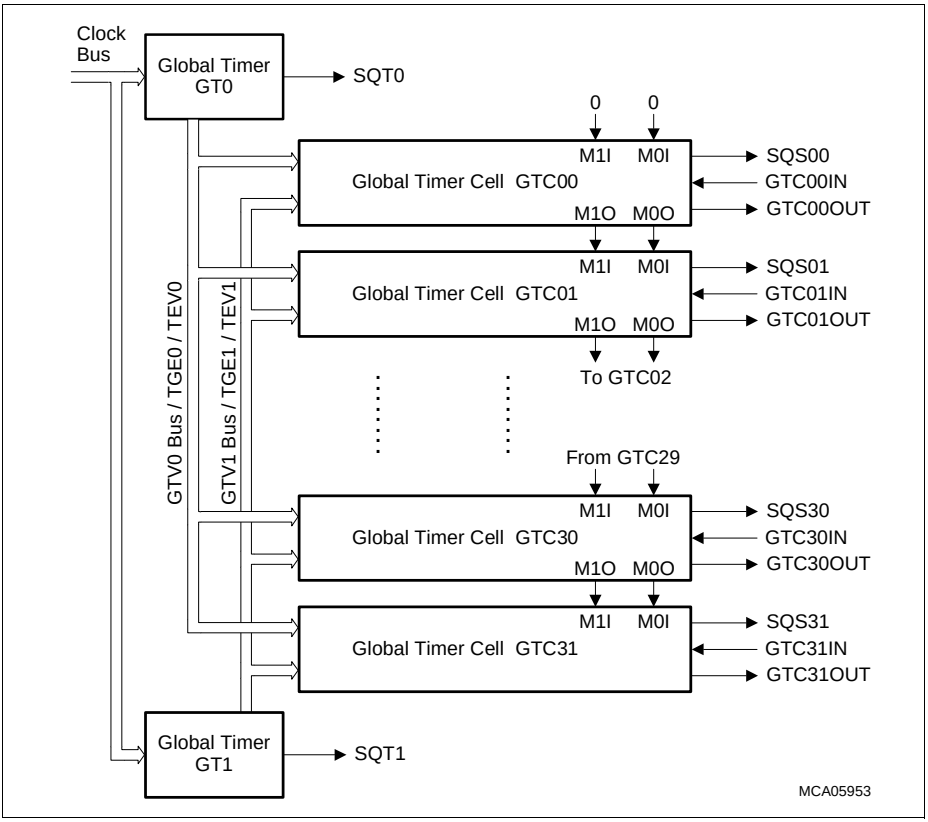


Figure 28-44 GTC Interconnections

Note: Cascading of GTCs is limited. TC1798 specific details are given on Page 28-306.

Capture Mode

The capture function of a GTCk cell is performed on a rising edge (GTCCTRk.RED = 1), a falling edge (GTCCTRk.FED = 1) or both edges of the selected GTCkIN input signal. On the requested event, the GTC:

- Copies the 24-bit value of the selected Global Timer into the 24-bit capture/compare register GTCXRk.X,
- Sets the GTCk service request flag in register SRSS1/SRSC1,
- Activates the service request output SQSk if control register bit GTCCTRk.REN = 1,
- Performs an GTCkOUT output signal line manipulation (set, reset, toggle, unchanged) as defined by bit field GTCCTRk.OCM,
- Transfers an action request, generated by an internal event or received on the M1I, M0I input lines, to the M1O, M0O output lines.

Compare Mode

In the Compare Code of a GTCk cell, several functions can be performed when the value of the selected Global Timer matches and/or exceeds the value stored in register GTCXR. With GTCCTRk.GES = 0 an “Equal Compare” match is selected while GTCCTRk.GES = 1 selects a “Greater Equal Compare” match. On the requested event, the GTC:

- Sets the GTCk service request flag in register SRSS1/SRSC1,
- Activates service request output SQSk if control register bit GTCCTRk.REN = 1,
- Performs an GTCkOUT output signal line manipulation (set, reset, toggle, unchanged) as defined by bit field GTCCTRk.OCM,
- Transfers an action request, generated by an internal event or received on the M1I, M0I input lines, to the M1O, M0O output lines.

If a greater or equal compare is selected, the condition is evaluated only when the compare value is written to the GTCXRk register. The user should then assure that the GTC is already enabled so that the evaluation can take place.

Capture after Compare Mode

When bit GTCCTRk.CAC = 1 and a compare event has occurred, register GTCXR is loaded with:

- The Global Timer value as selected by bit field GTCCTRk.MOD (GTCCTRk.CAT = 0),
- The alternate Global Timer value (GTCCTRk.CAT = 1). If a greater or equal compare match has been detected, the GTCk should be set into One Shot Mode in order to prevent double capturing.

One Shot Mode

In One Shot Mode (GTCCTRk.OSM = 1), a self-disable of GTCk is executed after each GTC event (GTCCTRk.CEN = 0). The current state of a GTCk can be evaluated by reading the control register flag bit GTCCTRk.CEN.

Note: The contents of the GTCk capture/compare register GTCXRk are write-protected for Capture_After_Compare in Single Shot Mode. Write protection is activated when the compare value is reached and released after a read access of register GTCXRk occurred.

Data Output Line Control

The data output GTCkOUT can be controlled by the GTCk itself and by adjacent GTCs with a lower order number. For this purpose, two communication signals between GTCs are available connecting all GTCs via their M1I/M0I inputs and their M1O/ M0O outputs respectively (see **Figure 28-45**).

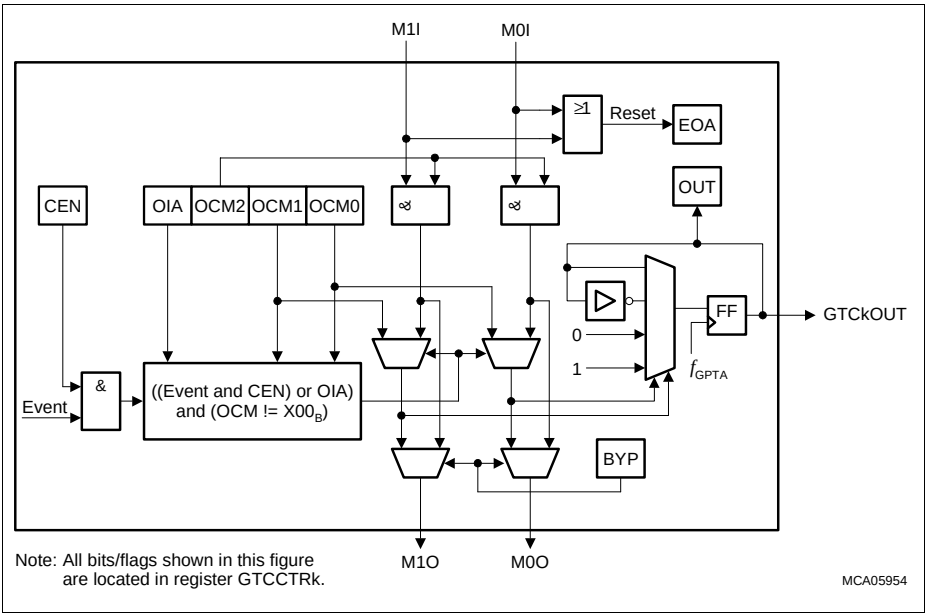


Figure 28-45 GTC Output Operation and Action Transfer

When bit GTCCTRk.OCM2 is reset, the data output GTCkOUT is only controlled by the local GTCk. A set, reset, toggle, or hold operation can be performed as selected by bits GTCCTRk.OCM1 and GTCCTRk.OCM0 (Table 28-2).

When bit GTCCTRk.OCM2 is set, the data output GTCkOUT is affected either by the local GTCCTRk.OCM1 and GTCCTRk.OCM0 bits or by the M1I/M0I input lines, which are connected to the adjacent GTCk-1 Global Timer output lines M1O/M0O. An enabled GTCk event superimposes an action request generated simultaneously by the M1I/M0I inputs.

When the bypass bit GTCCTRk.BYP is cleared, the M1O/M0O output lines logically OR together the local GTCk events and, if enabled by bit GTCCTRk.OCM2, the action requests received via the M1I/M0I input lines.

When bit GTCCTRk.BYP is set to 1, a local GTCk event will not modify the M1O/M0O output lines.

Table 28-2 Selection of GTC Output Operations and Action Transfer Modes

Bit Field OCM[2:0]	Local Capture or Compare Event	M1O/M0O BYP = 0		M1O/M0O BYP = 1		State of Local Data Output Line
0 0 0	not occurred	0	0	0	0	not modified
	occurred	0	0	0	0	not modified
0 0 1	not occurred	0	0	0	0	not modified
	occurred	0	1	0	0	inverted
0 1 0	not occurred	0	0	0	0	not modified
	occurred	1	0	0	0	0
0 1 1	not occurred	0	0	0	0	not modified
	occurred	1	1	0	0	1
1 0 0	not occurred	M1I	M0I	M1I	M0I	modified according M1I/M0I
	occurred	M1I	M0I	M1I	M0I	modified according M1I/M0I
1 0 1	not occurred	M1I	M0I	M1I	M0I	modified according M1I/M0I
	occurred	0	1	M1I	M0I	inverted
1 1 0	not occurred	M1I	M0I	M1I	M0I	modified according M1I/M0I
	occurred	1	0	M1I	M0I	0
1 1 1	not occurred	M1I	M0I	M1I	M0I	modified according M1I/M0I
	occurred	1	1	M1I	M0I	1

The GTCkOUT output line can be connected to output ports, on-chip peripheral inputs, and/or LTC inputs via the I/O Line Sharing Block (see Page 28-98). GTCkOUT can be updated directly by software (setting bit GTCCTRk.OIA = 1) or upon a timer, capture or compare event within the local GTCk or a preceding GTC. The current state of the data output line can be evaluated by reading status flag GTCCTRk.OUT.

Cell Enabling

After reset all GTCs are disabled. A GTC may be enabled by resetting GTCTRk.**EOA** (Enable-Of-Action) to 0 in Capture Mode or Compare Mode using a standard write assembler operation[1]. Because bit **EOA** is hardware protected, intrinsic read-modify-write assembler operations[2] only enable the GTC if bit **EOA** is modified from 1 to 0.

Cell Deactivation

By programming a GTC to Capture Mode with no edge selected (GTCCTRk.FED = GTCCTRk.RED = 0), an enabled cell becomes inactive and performs no action, but continues passing action commands via the communication link from M1I/M0I to M1O/M0O.

Cell Enabling on Event

A GTC can be enabled by an event in a GTC with lower index number. For this purpose, the local event function of an GTC must be temporary disabled by setting GTCCTRk.EOA (Enable-Of-Action) to 1. Because bit EOA is hardware protected, intrinsic read-modify-write assembler operations[2] only disable the GTC if bit EOA is modified from 0 to 1. Both operations will clear GTCCTRk.CEN and now a local event cannot affect the GTC. When a preceding GTC generates and communicates an event (or OIA) via its communication link M1O/M0O, at least one of the M1I/ M0I input lines changes its state to 1. This condition clears bit GTCCTRk.EOA of the disabled GTC via the OR gate as shown in **Figure 28-45**. Now GTCCTRk.CEN is set and the cell is enabled for local events.

It is also possible to enable the following GTC via the communication link for local events. For this purpose, the GTCCTRk.EOA bit of the following GTC must be set, too. If bit GTCCTRk.OCM2 of the preceding GTC is 1, the enable action will take place at the same time as in the preceding GTC. Otherwise, the GTC will be enabled later on a capture/compare event in the preceding GTC, provided OCM0 or OCM1 of this GTC is different from 0.

In this way, several GTCs can be enabled at the same time or one after the other. Normally, the cells will be used in One Shot Mode, and an interrupt will be generated after the last event to evaluate the data and to prepare the next enable sequence.

A disabled GTC (GTCCTRk.CEN = 0) behaves as an inactive cell.

1) Standard TriCore® write operations: ST.A, ST.B, ST.D, ST.DA, ST.DD, ST.HST.Q, ST.W
Standard PCP write operations: ST.F, ST.IF,BCOPY, COPY

2) Intrinsic TriCore® read-modify-write Operations: LDMST, ST.T, SWAP
Intrinsic PCP read-modify-write Operations: SET.F, XCH.F, CLR.F

Logical Operating Cells

The inter-cell communication architecture allows implementation of a complex waveform generation to be distributed over several GTCs, controlling a common port pin.

For example, one GTC may be configured in Capture Mode triggered by a rising edge detected on the associated input pin line. The related interrupt service routine can increment the captured timer value by a delay offset and store the result in the GTCXR register of the adjacent GTC configured in Compare Mode. Upon a compare event in the second GTC, the output port line of a third GTC can be set via M1O, M0O interface lines. When the GTCXR register of the third cell is loaded with another compare value by the interrupt service routine related to the second GTC, the output port line may be reset by the next compare event within GTC3.

This logical operating cell provides an output signal with programmable pulse width and configurable delay with minimal software overhead.

GTC Service Request

The service request output SQSk of a Global Timer Cell GTCk is controlled as shown in **Figure 28-46**. When the GTCk service request condition becomes active, the service request flag always becomes set. The service request output SQSk is only activated if it is enabled by the enable bit GTCCTRk.REN. Additional information about service request and interrupt handling is given on **Page 28-123**.

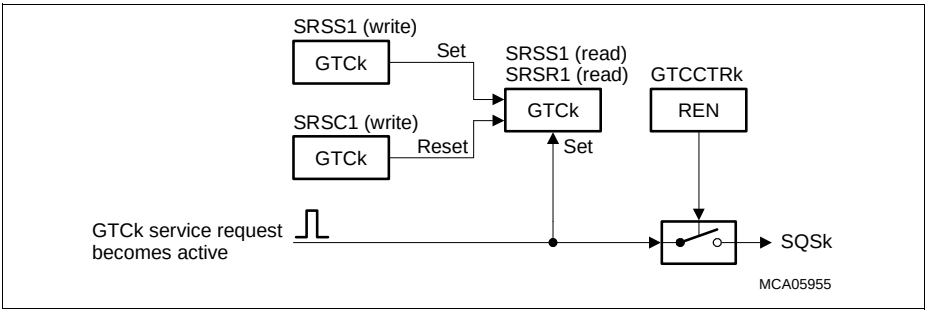


Figure 28-46 GTCk Service Request Generation

GTC Application Examples

The Global Timers together with GTCs can typically be used for input signal timing analysis of very complex input signals as well as for generation of complex output signals. **Figure 28-47** shows a configuration with Global Timer 0 and four GTCs, which is used in the following two examples:

- Example 1: Complex input signal capturing and analyzing
- Example 2: Complex periodical output signal generation

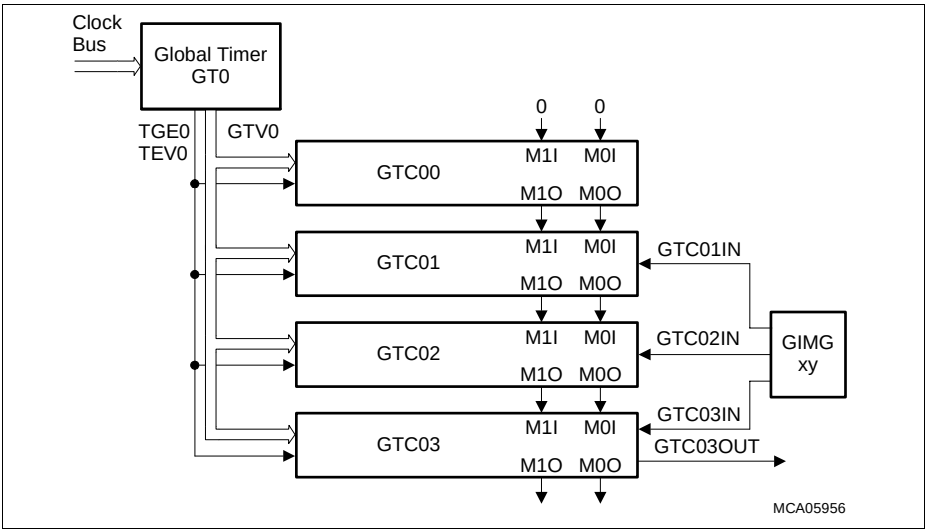


Figure 28-47 Complex Input/Output Signal Capturing/Generation with GTs and GTCs

Complex Input Signal Capturing and Analyzing

In this application example, one input signal from a GTC input multiplexer group becomes analyzed from a timing reference point for three consecutive signal transitions. This common input signal (e.g. a port line) is selected by a GTC input multiplexer group (GIMG) common for GTC01, GTC02, and GTC03 (see also **Page 28-111**). The GTCs are configured in the following way:

- GT0 operates as free-running up-counting 24-bit timer with reload to GTREV0.REV on overflow. It is clocked by one clock signal from the clock bus.
- GTC00 operates in Compare Mode with timer GT0. The compare match event is reported on the M0O/M1O output lines to the GTC01.
- GTC01 operates in Capture Mode at **rising** edge with enable-on-action set (EOA set) and One Shot Mode enabled (OSM set).

- GTC02 operates in Capture Mode at **falling** edge with enable-on-action set (EOA set) and One Shot Mode enabled (OSM set).
- GTC03 operates in Capture Mode at **rising** edge with enable-on-action set (EOA set) and One Shot Mode enabled (OSM set).

With the compare event of GTC00 (time stamp), GTC01 becomes active and waits for the next rising edge at its data input GTC01IN. While GTC01 is active, GTC02 and GTC03 are inactive.

When GTC01 detects a rising edge at its data input, it captures the current GT0 value into its GTCXR01 register, enables GTC02, and becomes disabled afterwards because it was operating in One Shot Mode. When GTC02 detects a falling edge at its data input, it captures the current GT0 value into its GTCXR02 register, enables GTC03, and becomes disabled afterwards because it was operating in One Shot Mode. When GTC03 detects a rising edge at its data input, it captures the current GT0 value into its GTCXR03 register and becomes disabled afterwards because it was operating in One Shot Mode. Optionally, the capture event at GTC03 may generate a service request to indicate that the three capture events have occurred and the captured values can be checked by software. Note that all of these capture events are executed by the GPTA®v5 hardware without any software interactions and with a resolution of the GT0 clock rate.

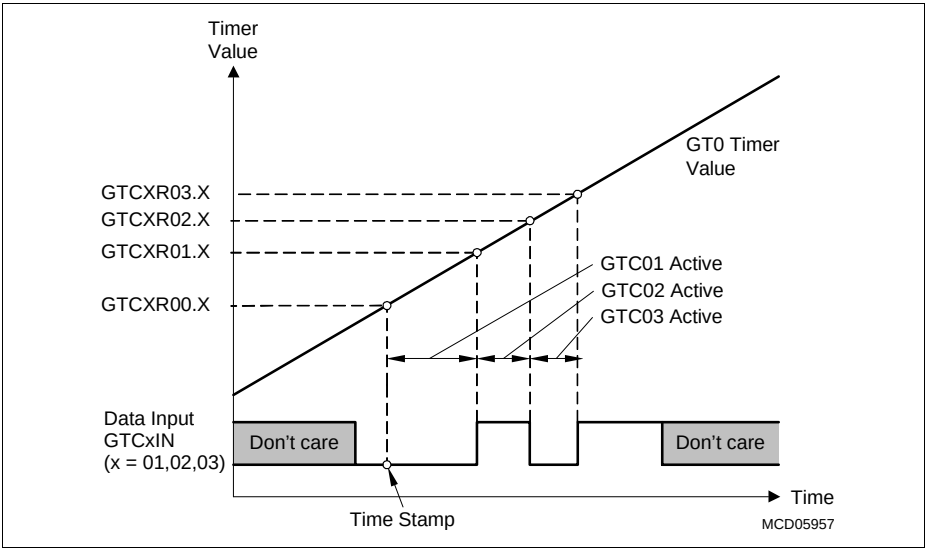


Figure 28-48 Complex Input Signal Analysis/Capturing with GTCs

Complex Periodic Output Signal Generation

This application example uses the GT/GTC configuration as shown in **Figure 28-47**. The generated output signal is available at GTC03OUT. The GTC input signals of the GT/GTC configuration are not used in this example.

- GT0 operates as free-running up-counting 24-bit timer with reload to GTREV0.REV on overflow. It is clocked by a clock signal from the clock bus. Its reload period determines the period of the generated PWM output signal.
- GTC00 operates in Compare Mode with timer GT0 with enable-on-action set (EOA set) and One Shot Mode enabled (OSM set). Furthermore, the output GTC03OUT becomes **set** on a local event (OCM = $X11_B$).
- GTC01 operates in Compare Mode with timer GT0 with enable-on-action set (EOA set) and One Shot Mode enabled (OSM set). Furthermore, the output GTC03OUT becomes **reset** on a local event (OCM = 110_B).
- GTC02 operates in Compare Mode with timer GT0 with enable-on-action set (EOA set) and One Shot Mode enabled (OSM set). Furthermore, the output GTC03OUT becomes **set** on a local event (OCM = 111_B).
- GTC03 operates in Compare Mode with timer GT0 with enable-on-action set (EOA set) and One Shot Mode enabled (OSM set). Furthermore, the output GTC03OUT becomes **reset** on a local event (OCM = 110_B).

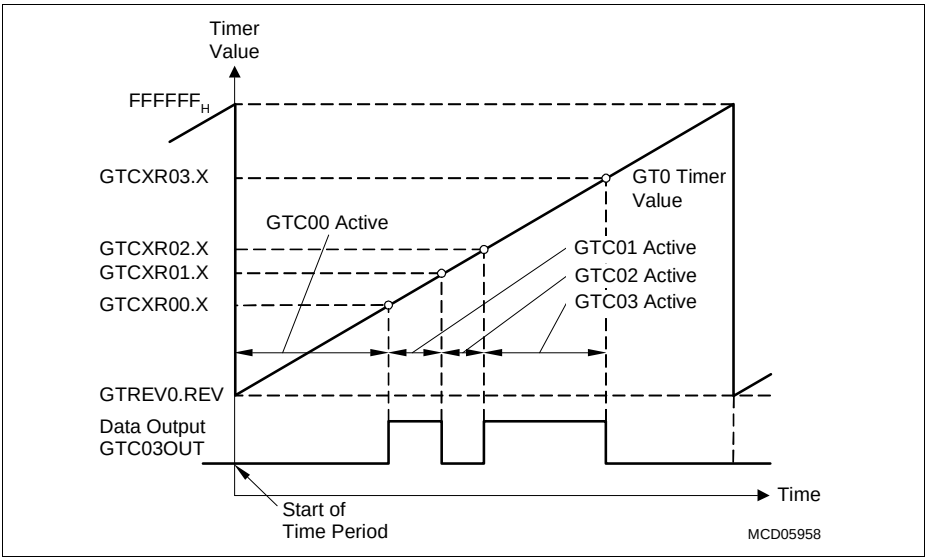


Figure 28-49 Complex Output Signal Generation with GTCs

At the start of the time period (reload of GT0), GTC00 becomes active and waits for the compare event. At this event, it sets the output signal GTC03OUT, enables GTC01 for

compare operation, and becomes disabled afterwards because it was operating in One Shot Mode. When the GTC01 compare event occurs, the output signal GTC03OUT is reset, GTC02 becomes enabled, and GTC01becomes disabled because it was operating in One Shot Mode. When the GTC02 compare event occurs, the output signal GTC03OUT is set, GTC03 becomes enabled, and GTC02 becomes disabled because it was operating in One Shot Mode. When the GTC03 compare event occurs, the output signal GTC03OUT is reset, and GTC02 becomes disabled because it was operating in One Shot Mode.

The capture event at GTC03 should generate a service request to indicate that the three compare events have occurred and that GTC01 can be enabled again (setting EOA and OSM). Note that all of the compare events are executed by the GPTA®v5 hardware without any software interactions and with a resolution of the GT0 clock rate.

28.3.3.3 Local Timer Cell (LTC00 to LTC62)

LTC00 to LTC62 are functionally identical. The functionality of LTC63 is different to LTC00 to LTC62 and therefore described separately at **Page 28-79**.

Registers

The following registers are assigned to a Local Timer Cell LTCk (k = 00-62):

- LTCCTRk = Local Timer Cell Control Register k (see **Page 28-192**)
- LTCXRk = Local Timer Cell X Register k (see **Page 28-205**)
- SRSC2 = Service Request State Clear Register 2 (see **Page 28-228**)
- SRSC3 = Service Request State Clear Register 3 (see **Page 28-230**)
- SRSS2 = Service Request State Set Register 2 (see **Page 28-229**)
- SRSS3 = Service Request State Set Register 3 (see **Page 28-231**)

Features

- **16-bit based timer cells** providing capture, compare, and timer functions.
- **Capture Mode** on rising, falling or both edges with following actions:
  - Service request generation
  - Output signal transition generation (set, reset, toggle the output signal).
- **Compare Mode** on equal compare of the corresponding (Reset-)Timer LTC with following actions:
  - Service request generation
  - Output signal transition generation (set, reset, toggle the output signal).
- **Timer Mode** incremented on hardware signal with following actions:
  - Event generation at overflow
  - Service request generation
  - Output signal transition generation (set, reset, toggle the output signal).
- **Reset Timer Mode** allows the selected LTC to be reset by an adjacent cell. Coherent update capability of adjacent LTCs for PWM management is provided.
- **One Shot Mode** allows the selected (capture, compare, timer or reset timer) mode to be stopped after the first event.
- **Flexible mechanism** to link pin actions and allow complex combination of cells. (A cell has the ability to propagate actions over adjacent cells with higher number, in order to perform complex waveforms such as multi channel PWMs).

Architecture

The architecture of an LTC is shown in **Figure 28-50**. Each LTC has a 16-bit capture/compare register and a 16-bit equal to comparator.

The first 63 Local Timer Cells (LTC00 to LTC62) have the following inputs:

- A local input data bus (YI) carrying the local timer value of the adjacent LTC with lower order number (YI of LTC00 is always 0000_H)

- A TI input reporting the occurrence of a local timer value update of the adjacent LTC with lower order number (TI of LTC00 is 0)
- A SI input used by the LTC in Compare Mode as enable line (SI of LTC00 is 0)
- Four action mode inputs (M3I, M2I, M1I, M0I) coming from the adjacent LTC cell with lower order number (M3I, M2I, M1I, and M0I of LTC00 are 0)
- An EI input reporting an event coming from the adjacent LTC with higher order number
- A trigger/clock/enable input LTCkIN hooked to one of the following signals sources:
  - External port lines
  - GTC00 to GTC31 outputs
  - Clock bus signals
  - PDL0 or PDL1 outputs
  - Internal GPTA®v5 kernel input signals INTx (x = 0-3)

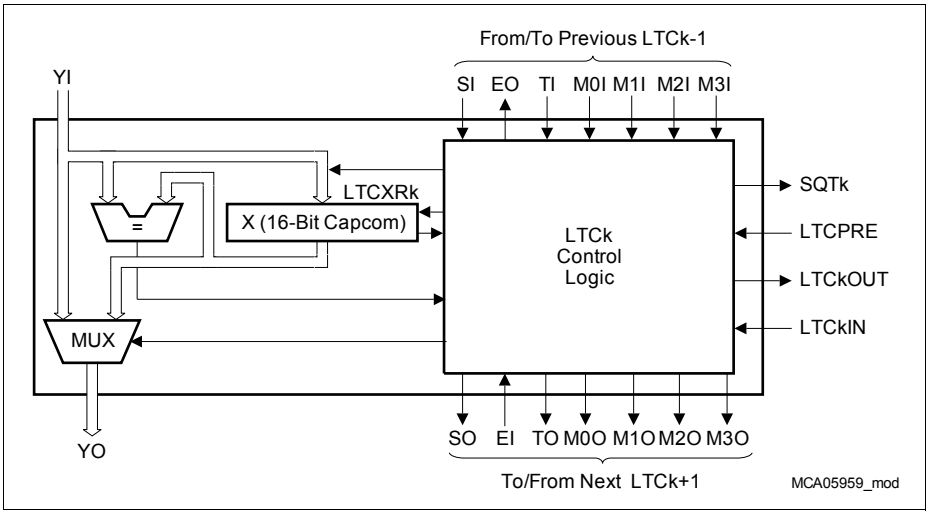


Figure 28-50 Architecture of Local Timer Cells

Each LTC provides the following input / output signals:

- One data output line (LTCkOUT) that can be connected to:
  - External port lines
  - Inputs of an MSC module
  - Outputs and/or inputs of Global Timer Cell inputs
- One LTC prescaler clock input (LTCPRE) for Timer Mode
- One service request line (SQT) triggered by a capture/compare event
- A local output data bus (YO) carrying the local timer value to the adjacent LTC with higher order number or the value on YI

- A TO output reporting the occurrence of a local timer value update to the adjacent LTC with higher order number
- An SO output used by the adjacent LTC with higher order number as enable signal for a compare function
- An EO output reporting the occurrence of a local event to the adjacent LTC with lower order number
- Four mode lines (M3O, M2O, M1O, M0O) going to the adjacent LTC with higher order number.

Figure 28-51 shows the arrangement of the LTCs and the connections with adjacent LTCs. LTC63 is a Local Timer Cell that differs from all other LTCs (LTC00 to LTC62). LTC63 is described in detail on **Page 28-79**.

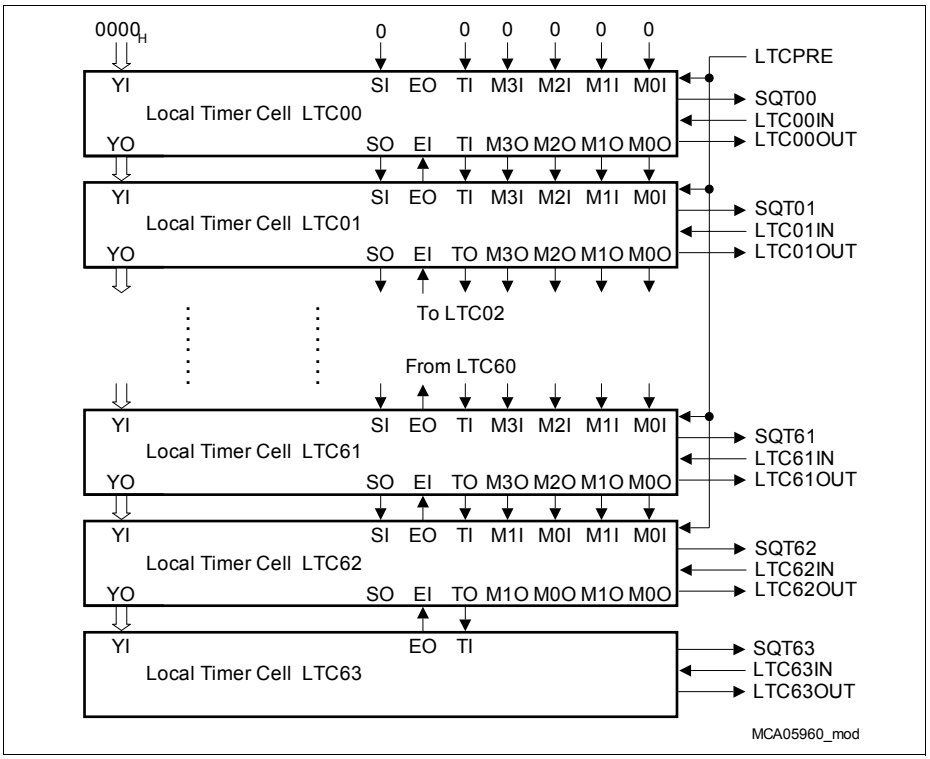


Figure 28-51 Interconnections between the LTCs

*Note: Cascading of LTCs is limited. TC1798 specific details are given on **Page 28-306**.*

Operating Mode Selection

The operating mode of an LTC – Free-Running Timer, Reset Timer, Capture, or Compare Mode – is defined by bit field LTCCTRk.MOD.

Free-Running Timer Mode

The content of the Local Timer Cell Register LTCXRk is initialized by a software write operation. LTCXRk is incremented by the selected LTCkIN input signal. Level or Edge Sensitive Mode can be selected for LTCkIN (see **Page 28-72**). In Level Sensitive Mode prescaler clock from the CDC (LTCPRE) can be used to reduce the timer frequency. Every change of the Local Timer Cell Register LTCXRk (increment, reset, or write access) is indicated by output signal TO = 1. When the timer reaches its overflow value ($FFFF_H$),

- the LTCk service request flag is set,
- the service request output SQTk is activated if control register bit LTCCTRk.REN = 1,
- the LTCk output line LTCkOUT can be altered (set, reset, toggle, unchanged),
- the LTCkOUT output line can be altered (set, reset, toggle, unchanged), depending on bit field LTCCTRk.OCM,
- an action request, generated by an LTCk internal event or received on the M1I/M0I input lines, is transferred via the M1O/M0O output lines to the LTC with higher order number (LTCk+1).

The event output line EO is also activated (set to high) by a software reset when writing $FFFF_H$ to register LTCXRk.

Reset Timer Mode

An LTC that is configured in Reset Timer Mode provides the same functionality as in Free-Running Timer Mode, but is extended by two additional features:

- The Local Timer Cell Register LTCXRk can be reset to $FFFF_H$ via the EI line, which can be activated by an event that occurred in the adjacent LTC with higher order number.
- If bit LTCCTRk.CUD is set to 1, the EI line reset event also toggles the logic state of the SO output line before it clears register bit LTCCTRk.CUD automatically. By accessing register bit LTCCTRk.SLO, the state of the timer's output line SO can be read or explicitly written.

Capture Mode

In Capture Mode, the LTCkIN input signal is used for capture function. Level or edge Sensitive Modes can be selected (see **Page 28-72**). On a capture event, the LTCk:

- copies the state of the local input data bus (YI) to the LTCXRk register (LTC00 always copies 0000_H),
- sets the LTCk service request flag,

- activates the service request line SQTk, if LTCCTRk.REN is set to 1,
- changes the LTCkOUT output line state (set, reset, toggle, unchanged), depending on bit field LTCCTRk.OCM and the M1I/ M0I input line state,
- generates and/or passes an action request via the M1O/M0O output lines to the LTC with higher order number (LTCk+1),
- sets the event output EO to high level for one f_{GPTA} clock cycle.

Compare Mode

The Compare Mode can be enabled on a low, high, or both levels of the select input line SI (LTCCTRk.SOL = 1, LTCCTRk.SOH = 1). The current state of SI is indicated by bit field LTCCTRk.SLL and can be read. When the value of the local input data bus (YI) matches the LTCXRk contents,

- The LTCk service request flag is set,
- The service request line SQTk is activated if LTCCTRk.REN is set to 1,
- The LTCkOUT output line state is changed (set, reset, toggle, unchanged), depending on bit field LTCCTRk.OCM,
- An action request is generated and/or passed via the M1O/M0O output lines to the LTC with higher order number (LTCk+1),
- The event output EO is set to high level for one f_{GPTA} clock cycle.

Note: To enable the compare function in all cases (on every timer or compare register update caused by a software write access, a reset event or a compare match), bits LTCCTRk.SOL and LTCCTRk.SOH must be set to 1.

An inactive cell (LTCCTRk.SOL = LTCCTRk.SOH = 0, or SI does not match the programmed value) will transfer the state of the event input line EI to the event output line EO.

One Shot Operation

When bit LTCCTRk.OSM is set to 1, a self-disable is executed after each LTC event. The current state of LTCk can be checked by reading the control register flag bit LTCCTRk.CEN.

Data Input Line Control

The data input line LTCkIN can operate in two modes (selected by bit LTCCTRk.ILM):

- Level Sensitive or
- Edge Sensitive.

In Edge Sensitive Mode, the active edges are selected by bits LTCCTRk.FED and LTCCTRk.RED. For the Level Sensitive Mode, the active level of the input signal can be selected by bit FED/AIL of register LTCCTRk.

Depending on which source is selected for the input line by the input multiplexer, different clocking modes of the LTC cell are possible (**Table 28-3**).

Table 28-3 LTC Data Input Line Operation (in Timer Mode)

Input Source	Level Sensitive Input Line LTCCTRk.ILM = 1	Edge Sensitive Input Line LTCCTRk.ILM = 0
External Signal (Port line)	The external signal operates as gating signal for the cell. The active input level can be selected with control register bit AIL. Additionally, the LTC prescaler mode can be enabled with LTCCTRk.PEN to reduce the timer frequency. The programmed function of the LTC is performed with the GPTA®v5 module clock frequency, or with the programmed prescaler clock LTCPRE (see **Page 28-37**).	The programmed function of the LTC cell is performed on selected edge(s).
Internal Clock Bus Line or PDL output or INT input	The programmed function is performed with the internal clock or PDL/INT signal. Note that all internal clock bus lines and PDL signals are active high pulses. The LTC Prescaler Mode and the input signal inversion must not be used.	The programmed function of the LTC cell is performed on selected edge(s). In case of full speed GPTA®v5 module clock selection as input clock, the Level Sensitive Mode must be selected. The Edge Sensitive Mode will not produce an event in this special case.

Table 28-3 LTC Data Input Line Operation (in Timer Mode) (cont'd)

Input Source	Level Sensitive Input Line LTCCTRk.ILM = 1	Edge Sensitive Input Line LTCCTRk.ILM = 0
GTC output	The GTC output signal operates as gating signal for the cell. The active input level can be selected with bit LTCCTRk.AIL. Additionally, the LTC prescaler clock LTCPRE can be enabled with bit LTCCTRk.PEN to reduce the timer frequency.	The programmed function of the LTC cell is performed on selected edge(s).

Note: If Capture Mode and level sensitive input is selected for an LTCk (bit LTCCTRk.ILM = 1), a capture event occurs on every LTC timer clock event if the corresponding LTC input signal is a high level.

Data Output Line Control

The data output LTCkOUT can be controlled by the LTCk itself and by adjacent LTCs with a lower order number. For this purpose, two communication signals between LTCs are available that make it possible to connect all LTCs via their M1I/M0I inputs and their M1O/ M0O outputs respectively (**Figure 28-52**).

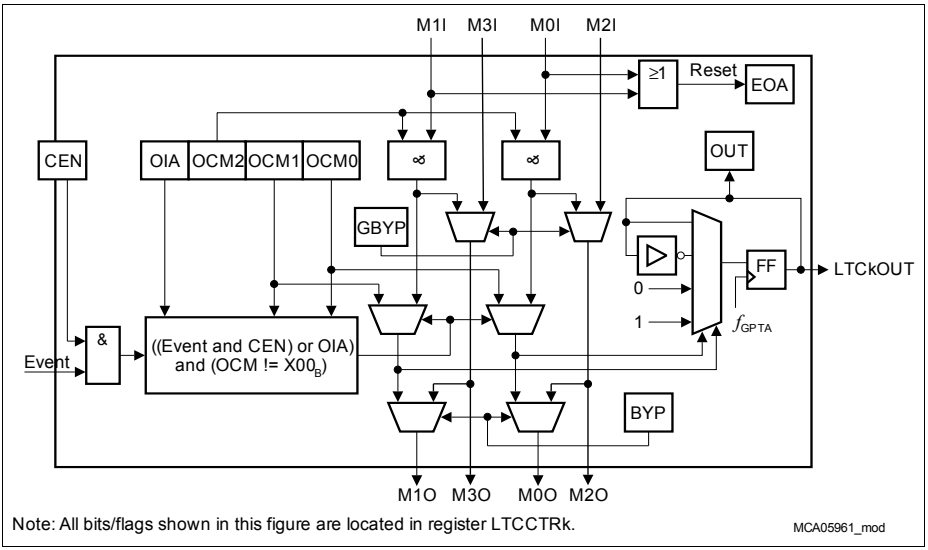


Figure 28-52 LTC Output Operation and Action Transfer

When bit LTCCTRk.OCM2 is reset, the data output LTCkOUT is controlled only by the local LTCk. A set, reset, toggle, or hold operation can be performed as selected by bits LTCCTRk.OCM1 and LTCCTRk.OCM0 (see **Table 28-4**).

When bit LTCCTRk.OCM2 is set, the data output LTCkOUT is affected either by the local LTCCTRk.OCM1 and LTCCTRk.OCM0 bits or by the M1I/M0I input lines, which are connected to the adjacent LTCk-1 Global Timer output lines M1O/M0O. An enabled LTCk event superimposes an action request generated simultaneously by the M1I/M0I inputs.

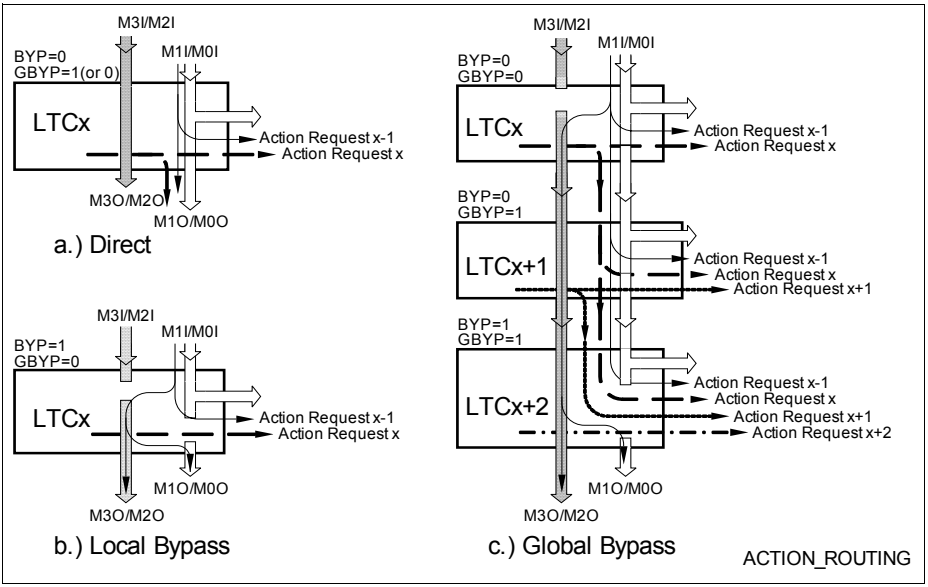


Figure 28-53 Direct, Local Bypass, and Global Bypass Action Request Routing

When the bypass bit LTCCTRk.BYP is cleared, the M1O/M0O output lines logically OR together the local LTCk events and, if enabled by bit LTCCTRk.OCM2, the action requests received via the M1I/M0I input lines.

When the bypass bit LTCCTRk.GBYP is cleared, the action requests received via M1I/M0I input lines, if enabled by bit LTCCTRk.OCM2, are forwarded to the subsequent LTCk+1 via the M3O/M2O output lines. If LTCCTRk.GBYP is set to 1, the action requests received via M3I/M2I input lines are forwarded to the subsequent LTCk+1 via the M3O/M2O output lines. Therefore the M3I/M2I may be used to pass the action requests of a reseted timer cross a group of LTC generating a complex signal or providing coherent update.

The two bypass bit LTCCTRk.BYP and LTCCTRk.GBYP enable three different types of action request routing, a direct routing, a local bypass routing and a global bypass

routing. These three different types of action request routing is sketched in **Figure 28-53**. The direct routing uses only the action request lines M1I/M0I. All action request run done the same path. The M3I/M2I are forwarded unchanged to M3O/M2O (next cells).

The local bypass copies all action request coming into a cell (M1I/M0I) to the outputs of the cell (M1O/M0O and M3O/M2O. The following cells do not see any action request generated within this locally bypassed cell.

The global bypass routing copies all action request coming into a group of sequential cells (M1I/M0I) to the outputs of this group of sequential cells (M1O/M0O and M3O/M2O. The following cells do not see any action request generated within this group of cells. Typically for edge aligned signals, the one action request for the edge is globally or locally bypassed, an all non edge aligned action request then locally generated within the group or local bypassed cell. Within a group complex signals may be generated or two cells used for local coherent update (double action principle).

Table 28-4 Selection of LTC Output Operations and Action Transfer Modes

Bit Field OCM [2:0]	Local Event	M1O/M0O								State of Local Data Output Line
		BYP = 0				BYP = 1				
		GBYP =0		GBYP=1		GBYP = 0		GBYP = 1		
0 0 0	No	0	0	0	0	0	0	M3I	M2I	not modified
	Yes	0	0	0	0	0	0	M3I	M2I	not modified
0 0 1	No	0	0	0	0	0	0	M3I	M2I	not modified
	Yes	0	1	0	1	0	0	M3I	M2I	inverted
0 1 0	No	0	0	0	0	0	0	M3I	M2I	not modified
	Yes	1	0	1	0	0	0	M3I	M2I	0
0 1 1	No	0	0	0	0	0	0	M3I	M2I	not modified
	Yes	1	1	1	1	0	0	M3I	M2I	1
1 0 0	No	M1I	M0I	M1I	M0I	M1I	M0I	M3I	M2I	modified according M1I/M0I
	Yes	M1I	M0I	M1I	M0I	M1I	M0I	M3I	M2I	modified according M1I/M0I
1 0 1	No	M1I	M0I	M1I	M0I	M1I	M0I	M3I	M2I	modified according M1I/M0I
	Yes	0	1	0	1	M1I	M0I	M3I	M2I	inverted
1 1 0	No	M1I	M0I	M1I	M0I	M1I	M0I	M3I	M2I	modified according M1I/M0I
	Yes	1	0	1	0	M1I	M0I	M3I	M2I	0
1 1 1	No	M1I	M0I	M1I	M0I	M1I	M0I	M3I	M2I	modified according M1I/M0I
	Yes	1	1	1	1	M1I	M0I	M3I	M2I	1
		M3O/M2O = [1]		M3O/M2O = M3I/M2I		M3O/M2O = [1]		M3O/M2O = M3I/M2I		

1) If OCM2 = 0: M3O/M2O = 0/0
If OCM2 = 1: M3O/M2O = M1I/M0I

The LTCkOUT output line can be connected to output ports, on-chip peripheral inputs (OTGS) and/or LTC inputs via the I/O Line Sharing Block (see **Page 28-98**). LTCkOUT can be updated directly by software (setting bit LTCCTRk.OIA = 1) or upon a timer, capture, or compare event within the local LTCk or a preceding LTC. The current state of the data output line can be evaluated by reading status flag LTCCTRk.OUT.

Global bypass may also be used to move a group of Local Timer Cells (Consecutive Local Timer Cells using the same Local Timer) into the previous group of Local Timer to e.g. hit a specific output pin. The previous Local Timer Group will therefore have some Local Timer before and some after the to be moved Local Timer Group. Because the Local Time Bus YI and YO is driven by every LTC configured as timer regardless of the chosen bypass mechanism, special care has to be taken. An example is sketched in **Figure 28-54**. Three Local Timer for an edge aligned PWM, using the same time base as the local Timer Cell Group1 but different offsets (not edge aligned), is inserted into another group of Local Timer Cells implementing an independent other signal.

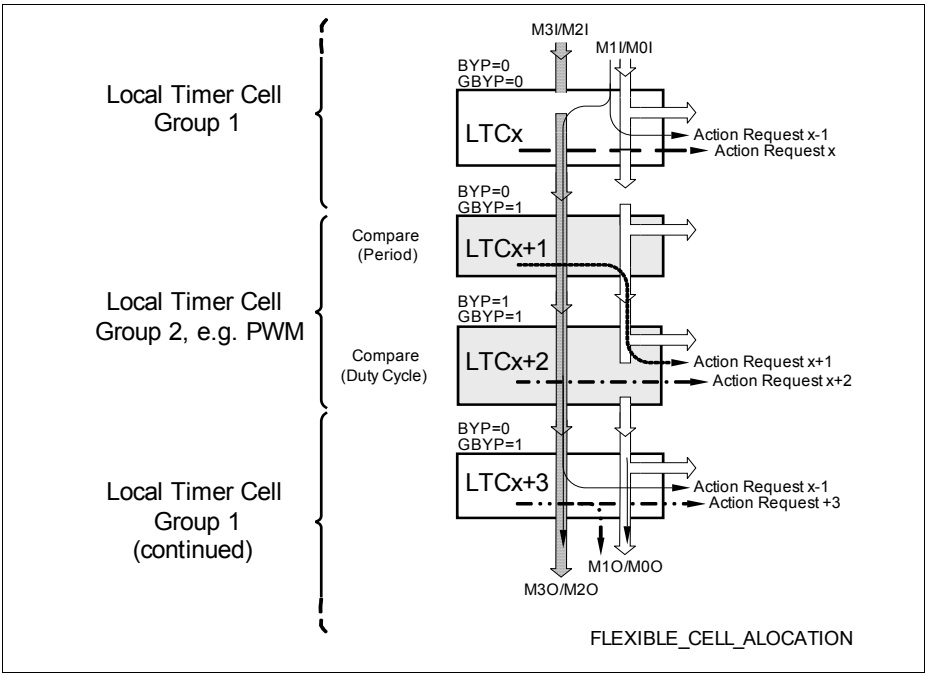


Figure 28-54 Global Bypass Action Request Routing for Flexible Cell Allocation

Cell Enabling

After reset all LTCs are disabled. An LTC may be enabled by resetting LTCCTRk.**EOA** (Enable-Of-Action) to 0 in Capture Mode or Compare Mode using a standard write assembler operation[1]. Because bit **EOA** is hardware protected, intrinsic read-modify-write assembler operations[2] only enable the LTC in Capture Mode or Compare Mode if bit **EOA** is modified from 1 to 0. If switching to Timer Mode, the LTC cell is enabled. In Timer Mode every write operation to bit 0…7 of LTCCTRk will enable the LTC.

Cell Deactivation

By programming an LTC to Capture Mode with no edge selected (LTCCTRk.ILM = LTCCTRk.FED = LTCCTRk.RED = 0), an enabled cell becomes inactive and performs no action, but continues passing action commands via the communication link from M1I/M0I to M1O/M0O. Output EO is inactive.

Alternatively, the LTC can be deactivated by setting it into Compare Mode with no active select line level (LTCCTRk.SOL = LTCCTRk.SOH = 0) but the communication link remains active. In this mode configuration, EI will be passed to EO.

Cell Enabling on Event

An LTC can be enabled in Capture Mode or Compare Mode by an event in an LTC with lower index number. For this purpose, the local event function of an LTC must be temporary disabled by setting LTCCTRk.EOA (Enable-Of-Action) to 1. Because bit EOA is hardware protected, intrinsic read-modify-write assembler operations[2] only disables the LTC if bit EOA is modified from 0 to 1. Both operations will clear LTCCTRk.CEN and now a local event cannot affect the LTC. When a preceding LTC generates and communicates an event (or OIA) via the communication link M1O/M0O, at least one of the M1I/M0I input lines changes its state to 1. This condition clears bit LTCCTRk.EOA of the disabled LTC via the OR gate as shown in **Figure 28-52**. Now LTCCTRk.CEN is set and the LTC is enabled for local events.

It is also possible to enable the following LTC via the communication link for local events. For this purpose, the bit LTCCTRk.EOA of this cell must be set, too. If bit LTCCTRk.OCM2 of the preceding cell is 1, the enable action will take place at the same time as in the preceding cell. Otherwise, the LTC will be enabled later on a capture/compare event in the preceding LTC, provided LTCCTRk.OCM0 or LTCCTRk.OCM1 of this cell is different from 0.

In this way, several LTCs can be enabled at the same time or one after the other. Normally, the LTCs will be used in One Shot Mode, and a service request will be

1) Standard TriCore® write operations: ST.A, ST.B, ST.D, ST.DA, ST.DD, ST.HST.Q, ST.W
Standard PCP write operations: ST.F, ST.IF,BCOPY, COPY

2) Intrinsic TriCore® read-modify-write Operations: LDMST, ST.T, SWAP
Intrinsic PCP read-modify-write Operations: SET.F, XCH.F, CLR.F

generated after the last event to evaluate the data and to prepare the next enable sequence. A disabled LTC (LTCCTRk.CEN = 0) behaves as an inactive capture LTC.

Logical Operating Cells

The inter-cell communication architecture allows concatenation of several LTCs to a logical cell. A logical cell contains any number of LTCs communicating via M1 and M0 lines and ends at an LTC disabled for action input or transfer (such as an LTC configured as timer, reset timer or LTC initiated with LTCCTRk.OCM2 = 0).

Therefore, the LTC with the lowest order number should be configured in Reset Timer Mode, thus providing all other LTCs of the logical cell with a time base (YO) and a compare enable signal (SO). Another LTC of the same logical cell can be initiated in Compare Mode to reset the LTC via its event output line EO, when a programmed threshold value is reached (register LTCXR) and the current state of its select line input SI matches the condition selected by the LTCCTRk bits SOH/SOL. Additional LTCs of the same logical cell can operate in Capture Mode triggered by a rising edge, falling edge, or both edges of a GPTA®v5 input line or a clock line of the clock bus. On the generated event, these LTCs capture the current contents of the timer cell, can generate a service request, can perform a manipulation of a GPTA®v5 output line (set, reset or toggle), and can also reset the LTC via the event output line EO.

LTC Service Request

The service request output SQTk of a Local Timer Cell LTCk is controlled as shown in **Figure 28-55**. When the LTCk service request condition becomes active, the service request flag becomes always set. The service request output SQTk is only activated if it is enabled by the enable bit LTCCTRk.REN. Additional information about service request and interrupt handling is given on **Page 28-123**.

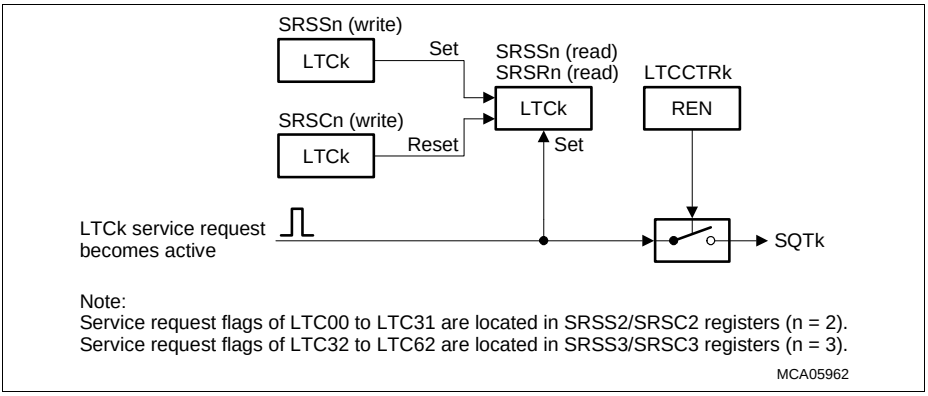


Figure 28-55 LTCk Service Request Generation

28.3.3.4 Local Timer Cell LTC63

The functionality of LTC63 is different to LTC00 to LTC62 and therefore described below.

Registers

The following registers are assigned to Local Timer Cell LTC63:

- LTCCTR63 = Local Timer Cell Control Register 63 (see **Page 28-204**)
- LTCXR63 = Local Timer Cell X Register 63 (see **Page 28-206**)
- SRSC3 = Service Request State Clear Register 3 (see **Page 28-230**)
- SRSS3 = Service Request State Set Register 3 (see **Page 28-231**)

Features

The GPTA®v5 Local Timer Cell array has one special cell, LTC63, which provides the following special features:

- **Compare Mode** on greater equal compare of the last timer, 16-bit based with following actions:
  - Service request generation
  - Output signal transition generation (set, reset, toggle the output signal).
- **Bit Reversal Mode:**
  - Timer can be selected to enable a special PWM Mode, called pulse count modulation (PCM)
- **Compare Value Switching** can be triggered by a hardware signal. This function can generate a service request. One Shot Mode makes it possible to stop the function after the first event.

Architecture

LTC63 is locally equipped with a 16-bit compare register, a 16-bit shadow register and a 16-bit greater comparator (**Figure 28-56**).

The LTC63 has the following inputs:

- A local input data bus (YI) carrying the local timer value of the adjacent LTC with lower order number
- A TI input reporting the occurrence of a local timer value update of the adjacent LTC with lower order number
- A trigger/enable input LTCkIN for compare value switching hooked to one of the following signals sources:
  - External port lines
  - GTC00 to GTC31 outputs
  - Clock bus signals
  - PDL0 or PDL1 outputs
  - Internal GPTA®v5 kernel input signals INTx (x = 0-3)

The LTC63 provides the following output signals:

- One data output line (LTCkOUT) that can be connected to:
  - External port lines
  - Inputs of an MSC module
  - Outputs and/or inputs of Global Timer Cell inputs
- One service request line (SQT) triggered by a compare or copy event
- An EO output reporting the occurrence of a local event to the adjacent LTC with lower order number

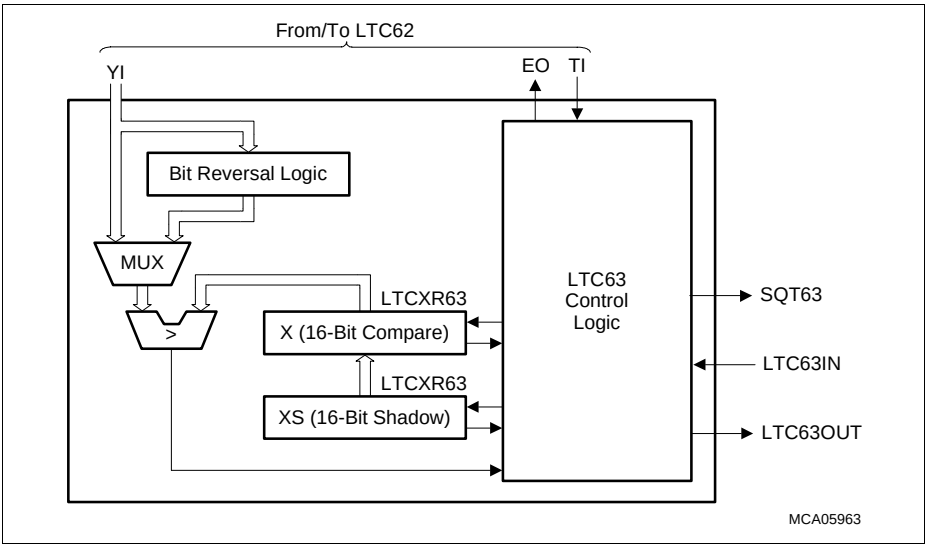


Figure 28-56 Architecture of Local Timer Cell 63

Compare

The compare function is always enabled. As long as the 16-bit compare value LTCXR63.X is greater than the timer value provided at YI, the comparator output signal is 1. The timer value at YI comes from the LTC62 either in original or in reversed order (Bit0 <-> Bit15, Bit1 <-> Bit14, etc.). The greater comparator output is connected directly to the output line LTC63OUT.

The 16-bit compare value LTCXR63.X is never greater than the LTC timer value ($FFFF_H$) coming from YI and which is used on LTC timer reset. Without special measures, a duty cycle of 100% cannot be achieved. There is always one LTC timer clock missing. Therefore, additional logic generates a permanent high signal whenever the 16-bit compare value LTCXR63.X is $FFFF_H$.

When the comparator output signal changes from 1 to 0,

- the service request flag LTC63 is set,
- an interrupt request will be activated if enabled by bit field LTCCTR63.REN,
- the event output line EO is set to high level for one f_{GPTA} clock cycle.

As well as the16-bit compare register LTCXR63.X, the LTC63 also contains a 16-bit shadow register LTCXR63.XS. Both 16-bit registers are combined in the 32-bit register LTCXR. On an LTC input signal selected via the LTC input multiplexer, the contents of the shadow register are copied to the compare register.

Standard PWM Mode

The LTC63 can be used for standard PWM duty cycle generation with enhanced update features. For this purpose, a pair of LTCs with lower index is configured as reset timer/period compare register. The user must set the period compare register to the desired period - 2 and LTC63 to the desired duty cycle. With LTCCTR63.BRM = 0 (Bit Reversal Mode), timer bit reversal is disabled. LTC63 is used for standard PWM Mode but with enhanced update features due to the “greater” comparator. The compare register LTCXR63.X can be written on-the-fly. If the duty cycle is changed at an arbitrary time, the actual duty cycle for the current period will reflect the old duty cycle, the new one, or a mixture of both. A duty cycle of 100% will be generated if the compare register is set to $FFFF_H$.

Pulse Count Modulation Mode (PCM)

With a period of 100 clocks and a duty cycle of 64%, standard PWM will produce an output signal that is ON for 64 clock cycles and OFF for the remaining 36 clock cycles. In contrast, pulse count modulation will generate 64 ON pulses and 36 OFF pulses distributed over the whole period as evenly as possible. PCM offers higher output frequency than standard PWM. This allows faster settling time e.g. when building a D/A converter in conjunction with an external low-pass filter. Only for very short or very long duty cycles does the method show no advantage or just little advantage compared to standard PWM.

As with standard PWM, a pair of LTCs with lower index is configured as reset timer/period compare register and LTC63 is used as duty cycle compare register. But now, Bit BRM (Bit Reversal Mode) in the LTCCTR63 register is set to 1 which enables the timer bit reversal to activate PCM.

The algorithm will also work if fewer than 16 timer bits are effectively used, even if the period is not a power of two. In any case, the user must write the duty cycle in unsigned 16-bit fractional format to the compare register.

Figure 28-57 shows an PCM example for an effective period of 6 clocks.

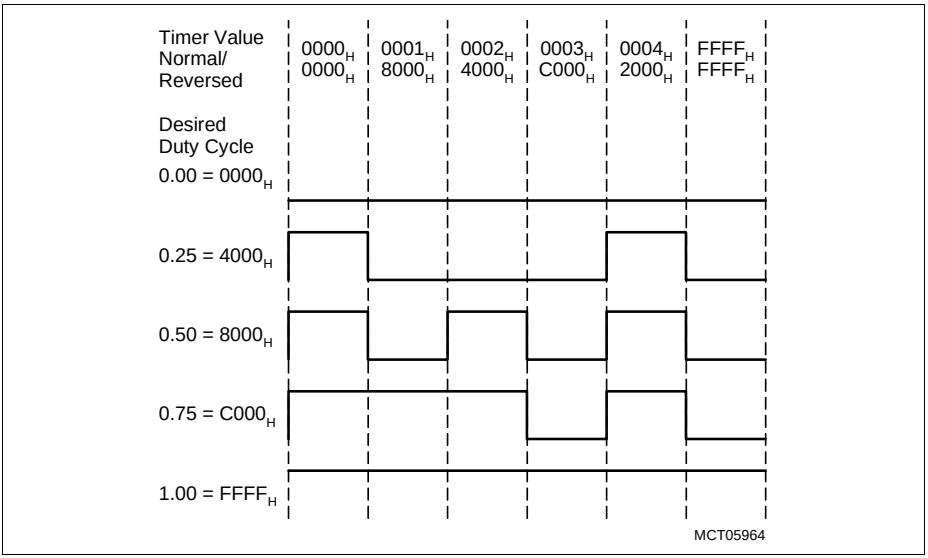


Figure 28-57 Pulse Count Modulation Example 1

Table 28-5 shows the rounding behavior for a period of 100 clocks.

Table 28-5 Implicit PCM Rounding

Desired Duty Cycle	Expected ON Pulses	Actual ON Pulses
0.000 = 0000	0	0
0.100 = $199A_H$	10	11
0.500 = 8000_H	50	50
0.800 = $CCCD_H$	80	82
0.900 = $E666_H$	90	90
0.999 = $FFBE_H$	100	99
1.000 = $FFFF_H$	100	100

The output is OFF for the remaining cycles of the period. The worst case error is approximately +2/-1 ON pulses. A subtraction performed via software may be used to reduce the worst case error.

If the duty cycle is changed at an arbitrary time, the actual duty cycle for the entire current period will reflect the old duty cycle, the new one, or a mixture of both.

Figure 28-58 shows another PCM example that demonstrates the difference between a standard PWM signal and the derived PCM signal. During one PWM period (128 clock cycles), the standard PWM signal is ON for 8 clock cycles and OFF for the remaining 120 clock cycles (duty cycle of 6.25%). The PCM signal operates with a PCM duty cycle of 1/8 = 0.125 resulting in 8 ON pulses of 1 clock cycle width within 1 PWM period.

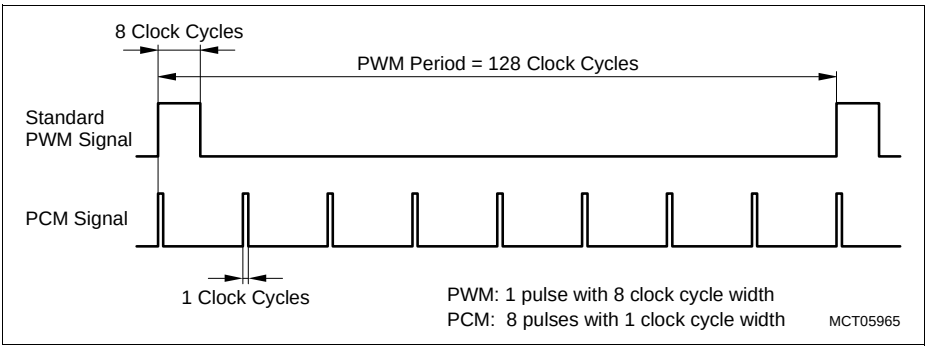


Figure 28-58 Pulse Count Modulation Example 2

Compare Value Switching

In both pulse modulation modes, it is possible to change the duty cycle either by software or on an LTC input signal. LTC63 contains two registers, the compare register and a shadow register. For software access, the compare register LTCXR63.X (= 16-bit low part of LTCXR63) is written directly.

For compare value switching triggered by hardware, the shadow register LTCXR63.XS (= 16-bit high part of LTCXR63) is pre-loaded with the desired duty cycle. On an LTC input signal selected via the LTC input multiplexer,

- The shadow register content LTCXR63.XS is copied to the compare register LTCXR63.X,
- The LTC63 service request flag is set,
- An interrupt request will be activated if enabled by bit field LTCCTR63.REN.

The data input line LTC63IN can operate in two modes (selected by bit LTCCTR63.ILM):

- Level Sensitive Mode or
- Edge Sensitive Mode

In Edge Sensitive Mode, the active edges are selected by bits LTCCTR63.FED and LTCCTR63.RED. In Level Sensitive Mode, the data input line LTCkIN is sensitive on a high level.

Various clocking modes of the LTC63 copy function are possible, depending on the source selected for the input line by the input multiplexer (see Table 28-6).

Table 28-6 LTC63 Data Input Line Operation

Input Source	Level Sensitive Input Line	Edge Sensitive Input Line
External Signal (Port line)	The external signal operates as gating signal for the cell. If the input is high the copy function of the LTC cell is performed with each rising edge of the GPTA®v5 module clock f_{GPTA}.	The copy function of the LTC cell is performed on selected edge(s).
Internal Clock Bus Line or PDL output or INT input	The copy function is performed with the internal clock or PDL/INT signal.	The copy function of the LTC cell is performed on selected edge(s). In case of full speed GPTA®v5 module clock selection, the Level Sensitive Mode must be selected. The Edge Sensitive Mode will not produce an event in this special case.
GTC output	The GTC output signal operates as gating signal for the cell. If the input is high the copy function of the LTC cell is performed with each rising edge of the GPTA®v5 module clock f_{GPTA}.	The copy function of the LTC cell is performed on selected edge(s).

When bit LTCCTR63.OSM is set to 1, a self-disable is executed after each copy event (PWM is not affected). The current state of the LTC copy enable may be evaluated by reading the control register flag bit LTCCTR63.CEN.

The output can be switched immediately to 0 or 1 in any pulse modulation mode by writing 0000_H or $FFFF_H$ to the duty cycle compare register LTCXR63.X.

LTC63 Service Request

The service request SQT63 can be generated by one of the following events:

- Comparator output changes from 1 to 0 (this makes sense mainly for standard PWM),
- Copy event.

Bit combinations 01_B and 10_B of bit field LTCCTR63.REN selects one of the two service request sources and enables it. Output SQT63 becomes active in these two cases. With the other two bit combinations of bit field LTCCTR63.REN (00_B, 11_B), the SQT63 output will not be activated. The LTC63 service request flag SRSS3.LTC63 will be set on a service request independently of LTCCTR63.REN. Additional information on service request and interrupt handling is provided on **Page 28-123**.

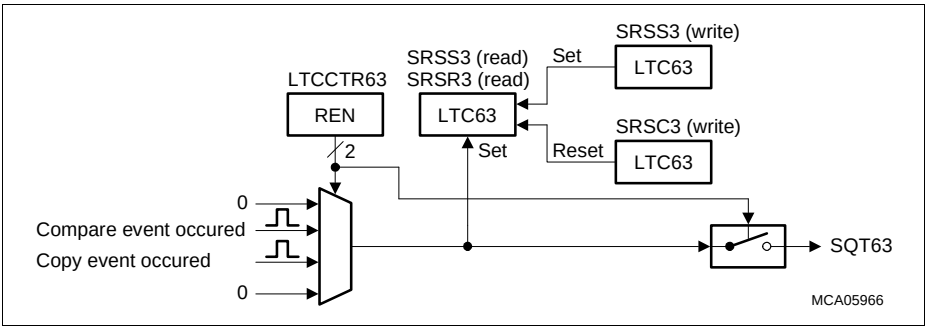


Figure 28-59 LTC63 Service Request Generation

28.3.3.5 Coherent Update

This section describes the two different mechanism to update signal features (e.g. period, duty cycle) if using Local Timer Cells. Both mechanism grant a coherent update only if a single update within a group of Local Timer Cells using a common Local Timer is performed within a timer period. So coherent update can only be granted if between coherent updating routine exit and coherent updating routine entry a time period of more then a period is maintained. If updating more frequently, software has to take care of coherency.

Global Coherent Update

The first mechanism, the so called global coherent update, is very useful to update a number of Local Timer Cells simultaneously. Furthermore this is the only way to grant a coherent update of a Local Timer Cell used as the period cell for a Reseted Timer. This global coherent update uses a common signal line (SI/SO) within a group of Local Timer Cells (all Local Timer Cells following an LTC configured as Timer). A pair of Local Timer Cells are configured so one cell being active on a high level of this SI/SO

(LTCCTRk.SOH = 1, LTCCTRk.SOL = 0) signal and the other cell being active on a low level of this SI/SO (LTCCTRk.SOH = 0, LTCCTRk.SOL = 1) signal. This pair of Local Timer Cells are configured to generate both action request for a single output signal (e.g. pin). If the global SI/SO is in a low state, all Local Timer Cells to be active on a high level of SI/SO can be configured (programmed with new values) without distortion of the output signal, because of being inactive. By setting the LTCCTRk.CUD bit within the Local TImer Cell used as Local Timer, the SI/SO bit will be toggled at the start of the next timer period, so all pair of Local Timer Cells simultaneously switch from active to passive (LTCCTRk.SOH = 0, LTCCTRk.SOL = 1) or passive to active state. Now the Local Timer Cells being inactive (LTCCTRk.SOH = 0, LTCCTRk.SOL = 1) may be configured (programmed) for the next update. No Local Timer Cell may be configured (programmed) while respective timer bit LTCCTRk.CUD =1, else wise a coherent update is no longer granted. Either the LTCCTRk.CUD has to be reset to 0 by software or a update of the Local Timer Registers have to be delayed to the next start of the period (LTCCTRk.CUD is reset by hardware to 0). The following example shows a PWM using global coherent update.

Fully Programmable PWM Signal Generation with 5 LTCs (global coherent update)

As shown in **Figure 28-59**, a logical cell of five LTCs can be used to generate a PWM signal with a programmable duty cycle, period length, and fully global coherent update of the period and duty cycle. In this example, LTC00 up to LTC04 are used to generate a PWM signal at the output of LTC04. To reduce complexity of this example, only a single duty cycle pair is described in the following text. More duty cycle cells may follow using the same reseted timer and pair of period cells. So if requiring a second duty cycle LTC pair, the first pair would be located to LTC2 and LTC6, the next pair on LTC 3 and LTC7 and the period cells would be assigned to LTC1 and LTC4.

LTC00 is configured in Reset Timer Mode thus providing all subsequent cells with a time base. LTC00 is clocked by a clock signal at the LTC00IN which has been selected by the LTC input multiplexer. LTC00 counts after reseted by LTC01 or LTC02 from $FFFF_H$, 0000_H, 0001_H … LTCXR01.X or LTCXR01.X. The period of the generated PWM is therefore LTCXR01.X +2 or LTCXR02.X + 2.

LTC01 and LTC02 are configured in Compare Mode. They are enabled if its SI inputs are at low level and responsible for the LTC04OUT signal generation in Phase 1. With the programmed values from **Table 28-7**, the LTC04OUT signal of Phase 1 has a period of 1000_D (= $3E8_H$) clocks of the LTC00IN clock signal and a duty cycle of 20% (= 200_D or $C8_H$).

LTC01 is configured in such a way (LTCCTR01.OCM = 011_B) that its output LTC01OUT is set to 1 whenever the LTC00 timer value LTCXR00.X is equal to the LTC01 compare value LTCXR01.X.

LTC02 is configured in such a way (LTCCTR02.OCM = 110_B) that its output LTC02OUT is reset whenever the LTC00 timer value LTCXR00.X is equal to the LTC02 compare value LTCXR02.X or it copies the action from the previous LTC01.

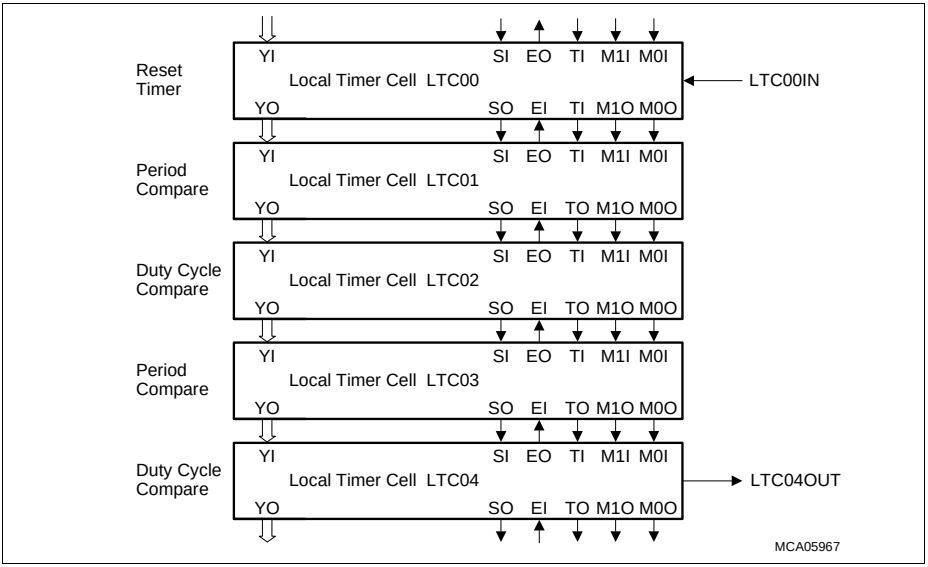


Figure 28-60 PWM Signal Generation with LTCs (Global Coherent Update)

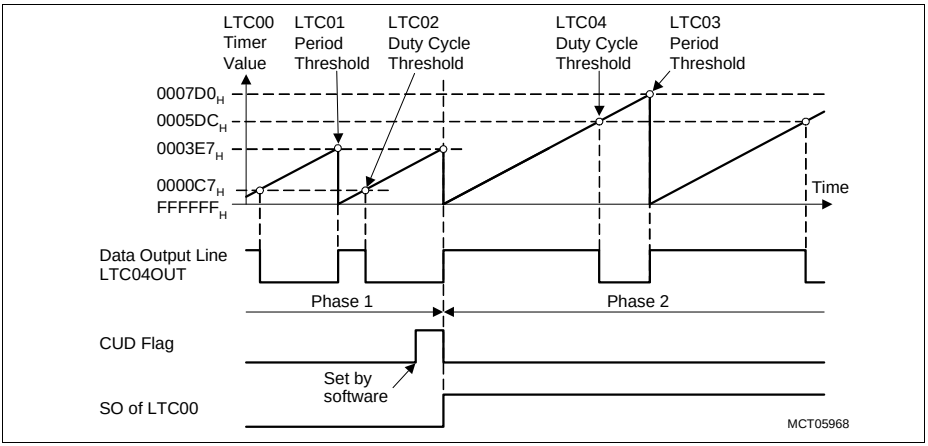


Figure 28-61 Internal Signal States of the PWM Signal Generation with 5 LTCs

LTC03 and LTC04 are configured in Compare Mode. They are enabled if its SI inputs are at high level and are responsible for the LTC04OUT signal generation in Phase 2. With the programmed values from **Table 28-7**, the LTC04OUT signal of Phase 2 has a period of 2000_D (= $7D0_H$) clocks of the LTC00IN clock signal and a duty cycle of 75% (= 1500_D or $5DC_H$).

LTC00 to LTC04 for the PWM example must be configured as defined in **Table 28-7**.

Note: Special care has to be taken not to reprogrammed the group of local timer cells (LTC) CAPCOM register before the previous global or local coherent update has been completed (end of current local timer period). Therefore maximum only one global coherent update within a timer period is possible! No Local coherent updates may be activated while a global coherent update modifying the period has not been completed.

Note: If several sequential coherent updates within a group of Local Timer Cells (LTC) is required, instead of using the global coherent update feature, the local coherent update mechanism (double action principle) is preferable. Mixing both principle, so updating the period using the coherent update and updating one or more duty cycle using local coherent update (double action principle) may result under specific condition in distorted signals (new duty cycle, old period or old duty cycle and new period). Therefore within a period either a global coherent update or multiple local coherent updates may be scheduled.

Note: To generate an output signal having 0% duty cycle (continuously low), the duty compare of the active cells must be set to $FFFF_H$. The timer sets the data output line by generating a respective signal on MO0 and MO1, but this signal is overruled by the dominating duty compare cell resetting the same data output line and therefore not passing the MI0 and MI1 signal from the timer to the data output line. This result in a data output line remaining continuously low.

Note: To generate an output signal having 100% duty cycle (continuously high), the duty cycle threshold must be set above the period threshold value. Therefore no reset event for the data line is generated and periodically the timer generates a set event. This result in a data output line remaining continuously high.

Table 28-7 Programming Values for PWM Signal Generation with 5 LTCs

Register	Value	Function
LTC00 Configuration Setup		
GPTA0_LTCXR00	0000 0000_H	LTC00 data register value = 0
GPTA0_LTCCTR00	0001 0413_H	MOD = 11_B: Reset Timer Mode selected OSM = 0: LTC00 continuously enabled ILM = 0, RED = 1, FED = 0: Input LTC00IN operates in Edge Sensitive Mode with rising edge; one clock bus signal is selected via the LTC input multiplexer SLO = 0: state of select line output SO is 0 CEN = 0: enable LTC00 for local events OCM = 000_B: hold LTC00OUT state
LTC01 Configuration Setup		
GPTA0_LTCXR01	0000 $03E7_H$	Load compare value = $3E7_H$ = 999_D
GPTA0_LTCCTR01	0001 $5C11_H$	MOD = 01_B: Compare Mode with LTC00 selected OSM = 0: LTC01 continuously enabled SOH = 0, SOL = 1: compare enabled by low level at SI BYP = 0: local bypass in LTC01 is disabled GBYP = 1: global bypass in LTC01 is disabled EOA = 0: LTC02 enabled for local events OCM = 011_B: set LTC01OUT by a local event only OIA = 1: output action defined by OCM must be performed immediately
LTC02 Configuration Setup		
GPTA0_LTCXR02	0000 $00C7_H$	Load compare value = $C7_H$ = 199_D
GPTA0_LTCCTR02	0001 3411_H	MOD = 01_B: Compare Mode with LTC00 selected OSM = 0: LTC02 continuously enabled SOH = 0, SOL = 1: compare enabled by low level at SI BYP = 0: local bypass in LTC02 is disabled GBYP = 1: global bypass in LTC02 is disabled EOA = 0: LTC02 enabled for local events OCM = 110_B: reset LTC02OUT by a local event or copy the previous cell action OIA = 0: no immediate output action required

Table 28-7 Programming Values for PWM Signal Generation with 5 LTCs (cont'd)

Register	Value	Function
LTC03 Configuration Setup		
GPTA0_LTCXR03	0000 $07CF_H$	Load compare value = $7CF_H$ = 1999_D
GPTA0_LTCCTR03	0001 $7C21_H$	MOD = 01_B: Compare Mode with LTC00 selected OSM = 0: LTC03 continuously enabled SOH = 1, SOL = 0: compare enabled by high level at SI BYP = 0: local bypass in LTC03 is disabled GBYP = 1: global bypass in LTC03 is disabled EOA = 0: LTC03 enabled for local events OCM = 111_B: set LTC04OUT by a local event or copy the previous cell action OIA = 1: output action defined by OCM must be performed immediately
LTC04 Configuration Setup		
GPTA0_LTCXR04	0000 $05DB_H$	Load compare value = $5DB_H$ = 1499_D
GPTA0_LTCCTR04	0001 3421_H	MOD = 01_B: Compare Mode with LTC00 selected OSM = 0: LTC04 continuously enabled SOH = 1, SOL = 0: compare enabled by high level at SI BYP = 0: local bypass in LTC04 is disabled GBYP = 1: global bypass in LTC04 is disabled EOA = 0: LTC04 enabled for local events OCM = 110_B: reset LTC04OUT by a local event or copy the previous cell action OIA = 0: no immediate output action required

Local Coherent Update

The second mechanism, the so called local coherent update or double action principle, is very useful to update single Local Timer Cells without signal distortion (no other signal output beside the previously configured and the new configured). This coherent update may not be used for Local Timer Cells generating toggle action requests (LTCCTRk.OCM = OCM = $x01_B$). The local coherent update is useful to configure (programme) several Local Timer Cells within a group of Local Timer Cells (all using the same Local Timer Cell as time base) sequentially (not simultaneously), e.g. within different routines of the application software. The only restriction to grant non distorted output signals by hardware is to update (configure or programme) every single pair of Local Timer Cells no often than once within a timer period (time measured from previous routine exit and current routine entry), else wise software has to take care of coherency (non distorted signals). A pair of Local Timer Cells are configured one cell being active (LTCCTRk.SOH = 1, LTCCTRk.SOL = 1) and the other being inactive (LTCCTRk.SOH = 0, LTCCTRk.SOL = 0, LTCCTRk.CEN = 0). This pair of Local Timer Cells are configured to generate both action requests for a single output signal (e.g. pin). A Local Timer Cell being inactive may be configured (programmed with a new value) without distortion of the output signal, because of being inactive. By activating the newly configured Local Timer Cell (LTCCTRk.SOH = 1, LTCCTRk.SOL = 1, LTCCTRk.OSM = 0), now two Local Timer Cells generate the same type of action request. The one being earlier within the period will now drive the output signal (either the newly configured or the previously configured one). Now the Local Timer Cell being active before configuration is coherently deactivated (LTCCTRk.OSM = 1) on its next action. So one period later this cell will be inactive (LTCCTRk.CEN = 0) and may be used for the next local coherent update. Local and coherent update may be used simultaneously within a group of Local Timer Cells. The following example shows a PWM using local coherent update. To reduce complexity of this example, only a single duty cycle pair is described in the following text. More duty cycle cells may follow using the same reseted timer and pair of period cells. So if requiring a second duty cycle LTC pair, the first pair would remain on LTC2 and LTC3 and the next pair on LTC 4and LTC5 using LTC05 as output.

Programmable PWM Signal Generation with 4 LTCs (local coherent update)

As shown in **Figure 28-62**, a logical cell of four LTCs can be used to generate a PWM signal with a programmable duty cycle and local coherent update of this duty cycle. In this example, LTC00 up to LTC03 are used to generate a PWM signal at the output of LTC03.

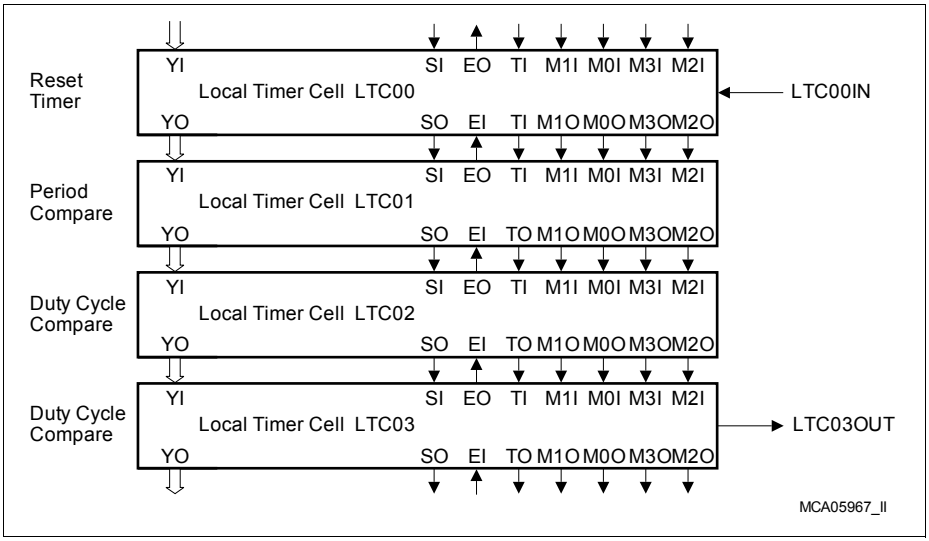


Figure 28-62 PWM Signal Generation with LTCs (Local Coherent Update)

LTC00 is configured in Reset Timer Mode thus providing all subsequent cells with a time base. LTC00 is clocked by a clock signal at the LTC00IN which has been selected by the LTC input multiplexer. LTC00 counts after reseted by LTC01 or LTC02 from $FFFF_H$, 0000_H, 0001_H … LTCXR01.X or LTCXR01.X. The period of the generated PWM is therefore LTCXR01.X +2 or LTCXR02.X + 2.

LTC01 is configured in Compare Mode. It is always active and responsible for the LTC03OUT signal generation in Phase 1. With the programmed value from **Table 28-8**, the LTC03OUT signal of Phase 1 has a period of 1000_D (= $3E8_H$) clocks of the LTC00IN clock signal and a duty cycle of 20% (= 200_D or $C8_H$).

LTC01 is configured in such a way (LTCCTR01.OCM = 011_B) that its output LTC01OUT is set to 1 whenever the LTC00 timer value LTCXR00.X is equal to the LTC01 compare value LTCXR01.X.

LTC02 and LTC03 are configured in Compare Mode. They are responsible for the LTC03OUT signal generation in Phase 2. With the programmed values from **Table 28-8**, the LTC03OUT signal of Phase 2 has a duty cycle of 77% (= 770_D or 302_H).

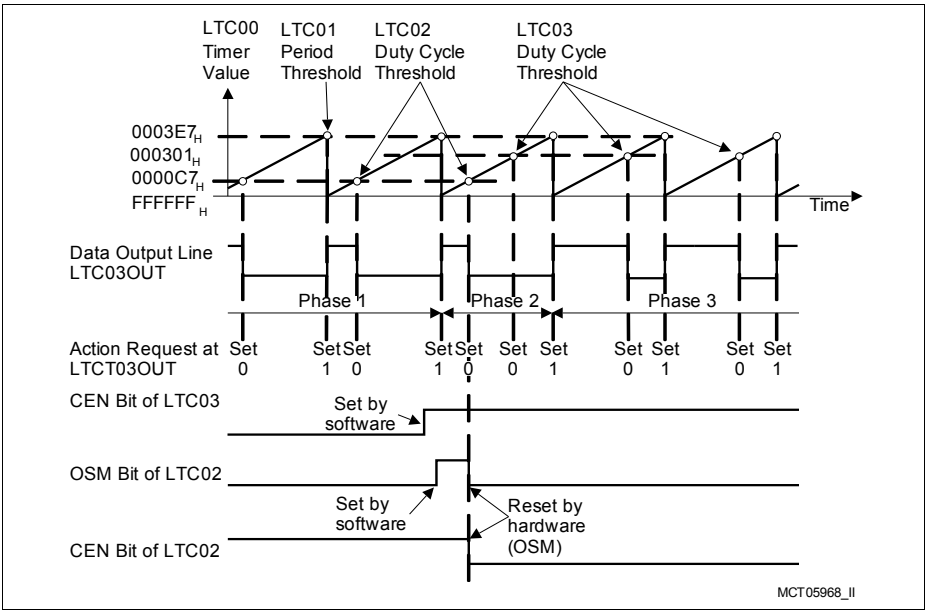


Figure 28-63 Internal Signal States of the PWM Signal Generation with 4 LTCs

LTC00 to LTC03 for the PWM example must be configured as defined in **Table 28-8**.

Note: Special care has to be taken not to reprogram LTCXR02.X or LTCXR03.X before the previous local coherent update has been completed (LTCXR02.CEN = 0 or LTCXR03.CEN = 0). Therefore maximum one coherent update within a timer period is possible (measured from previous routine exit to current routine entry)!

Note: If simultaneous coherent updates of several Local Timer Cells within a group of Local Timer Cells (LTC) is required, instead of using the local coherent update (double action principle), the global coherent update mechanism must be used.

Note: If coherent updating the period of a Timer in Reset Timer Mode is required, the global coherent update mechanism must be used.

Note: Global bypass may be used to route e.g. period action request (edge aligned PWM) around the pair of locally coherent updated Local Timer Cells to following Local Timer Cells. But special care has to be taken, because the timer bus is not routed over a LTC configured as timer.

Note: This scheme activates for one period two cells in parallel. Therefore, if enabled, also two interrupts for this one signal are generated, one for the old (previous) edge, one for the new (updated) edge.

Note: To generate an output signal having 0% duty cycle (continuously low), the duty compare of the active cells must be set to $FFFF_H$. The timer sets the data output line by generating a respective signal on MO0 and MO1, but this signal is overruled by the dominating duty compare cell resetting the same data output line and therefore not passing the MI0 and MI1 signal from the timer to the data output line. This result in a data output line remaining continuously low.

Note: To generate an output signal having 100% duty cycle (continuously high), the duty cycle threshold must be set above the period threshold value. Therefore no reset event for the data line is generated and periodically the timer generates a set event. This result in a data output line remaining continuously high.

Table 28-8 Programming Values for PWM Signal Generation with 4 LTCs

Register	Value	Function
LTC00 Configuration Setup		
GPTA0_LTCXR00	0000 0000_H	LTC00 data register value = 0
GPTA0_LTCCTR00	0000 0413_H	MOD = 11_B: Reset Timer Mode selected OSM = 0: LTC00 continuously enabled ILM = 0, RED = 1, FED = 0: Input LTC00IN operates in Edge Sensitive Mode with rising edge; one clock bus signal is selected via the LTC input multiplexer SLO = 0: state of select line output SO is 0 CEN = 0: enable LTC00 for local events OCM = 000_B: hold LTC00OUT state
LTC01 Configuration Setup		
GPTA0_LTCXR01	0000 $03E7_H$	Load compare value = $3E7_H$ = 999_D
GPTA0_LTCCTR01	0000 $5C11_H$	MOD = 01_B: Compare Mode with LTC00 selected OSM = 0: LTC01 continuously enabled SOH = 1, SOL = 1: enabled by both level at SI BYP = 0: bypass in LTC02 is disabled GBYP = 0: global bypass in LTC02 is disabled EOA = 0: LTC02 enabled for local events OCM = 011_B: set LTC01OUT by a local event only OIA = 1: output action defined by OCM must be performed immediately

Table 28-8 Programming Values for PWM Signal Generation with 4 LTCs (cont'd)

Register	Value	Function
LTC02 Configuration Setup		
GPTA0_LTCXR02	0000 00C7$_H$	Load compare value = C7$_H$ = 199$_D$
GPTA0_LTCCTR02	0000 3431$_H$	MOD = 01$_B$: Compare Mode with LTC00 selected OSM = 0: LTC02 continuously enabled SOH = 1, SOL = 1: compare enabled by low and high level at SI BYP = 0: local bypass in LTC02 is disabled GBYP = 0: begin of global bypass in LTC02 EOA = 0: LTC02 enabled for local events OCM = 110$_B$: reset LTC02OUT by a local event or copy the previous cell action OIA = 0: no immediate output action required
LTC03 Configuration Setup		
GPTA0_LTCXR03	0000 0301$_H$	Load compare value = 301$_H$ = 769$_D$
GPTA0_LTCCTR03	0001 3401$_H$	MOD = 01$_B$: Compare Mode with LTC00 selected OSM = 0: LTC03 continuously enabled SOH = 0, SOL = 0: compare disabled by low and high level at SI BYP = 1: local bypass in LTC03 is disabled GBYP = 1: end of global bypass in LTC03 EOA = 0: LTC04 enabled for local events OCM = 110$_B$: reset LTC03OUT by a local event or copy the previous cell action OIA = 0: no immediate output action required

The following code exemplifies the scheme to update the duty cycle of the PWM signal generation with 4 LTCs

```
Read LTCCTR02
If ( LTCCTR02.SOL=1 and LTCCTR02.SOH=1 and LTCCTR02.CEN=1 and
    LTCCTR02.OSM=0) Then
   Write New_Value into LTCXR03 of LTC03
   Set LTCCTR03.OSM=0 and LTCCTR03.SOL=LTCCTR03.SOH=1 for LTC03
    (Do not use LOAD/MODIFY/STORE, SWAP, or CLEAR_BIT assembler instructions)
   Set LTCCTR02.OSM=1 of LTC02
     (Use LOAD/MODIFY/STORE, SWAP, or CLEAR_BIT assembler instructions)
   Read LTCXR02
   Read LTCXR00
   If LTCXR00>Read_LTCXR02 then
      Clear LTCCTR02.SOL=LTCCTR02.SOH=0 of LTC02
   End If
Else
   Write New_Value into LTCXR02 of LTC02
   Set LTCCTR02.OSM=0 and LTCCTR02.SOL=LTCCTR02.SOH=1 for LTC02
    (Do not use LOAD/MODIFY/STORE, SWAP, or CLEAR_BIT assembler instructions)
   Set LTCCTR03.OSM=1 of LTC03
     (Use LOAD/MODIFY/STORE, SWAP, or CLEAR_BIT assembler instructions)
   Read LTCXR03
   Read LTCXR00
   If LTCXR00>Read_LTCXR03 then
      Clear LTCCTR03.SOL=LTCCTR03.SOH=0 of LTC03
   End If
End If
```

28.3.4 Input/Output Line Sharing Block (IOLS)

The I/O Line Sharing Block allows the 56 inputs and 112 outputs of the GPTA®v5 units to be routed with high flexibility between I/O lines, output lines, clock inputs, other on-chip peripherals and other GPTA®v5 cells. The GPTA®v5 module provides a total of 56 input lines and 112 output lines, assigned to seven I/O groups IOG[6:0], two on-chip trigger and gating signal groups OTG[1:0], and seven output groups OG[6:0].

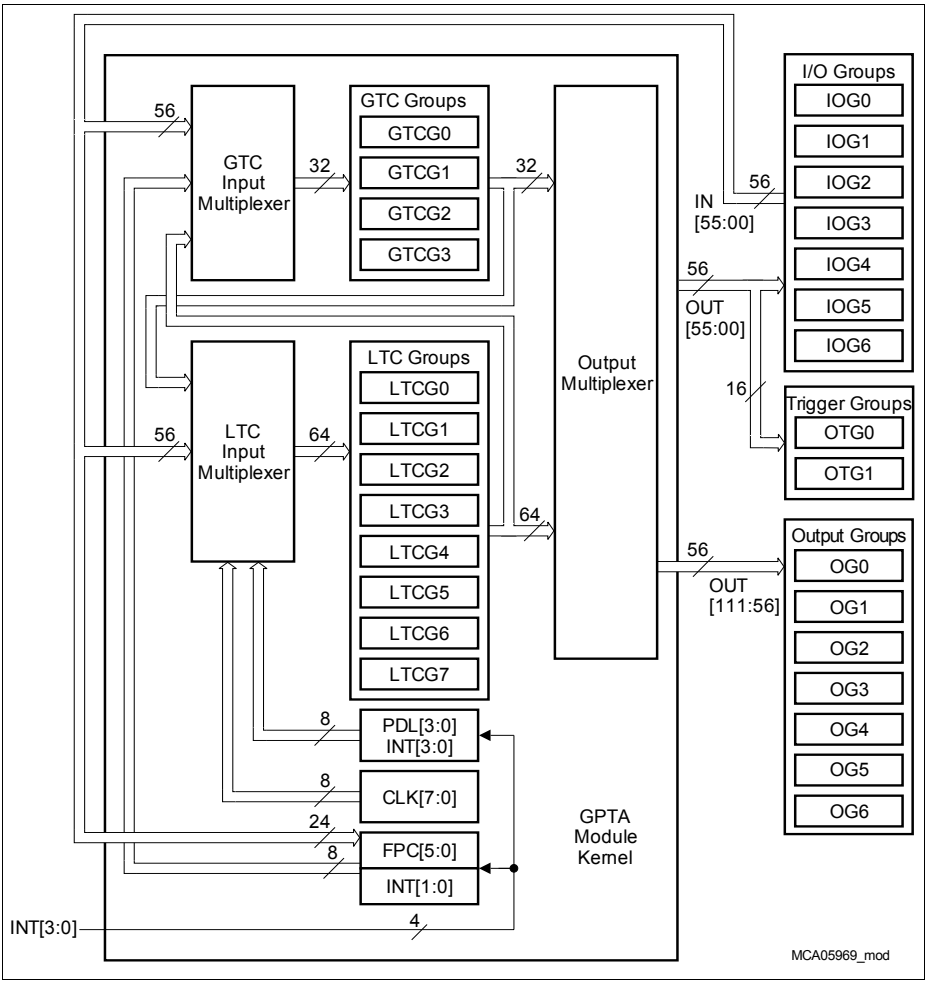


Figure 28-64 Input/Output Line Sharing Block Overview

The I/O Line Sharing Block does the following selections:

- FPC input line selection
- GTC and LTC output multiplexer selection
- On-chip trigger and gating signal selection
- GTC input multiplexer selection
- LTC input multiplexer selection

For choosing these selection, the input and output lines of the related cells are integrated into groups with eight parts each. Seven I/O groups, two on-chip and gating signal groups, seven output groups, four GTC groups, eight LTC groups, one clock group, one FPC/INT group, and one PDL/INT group are defined.

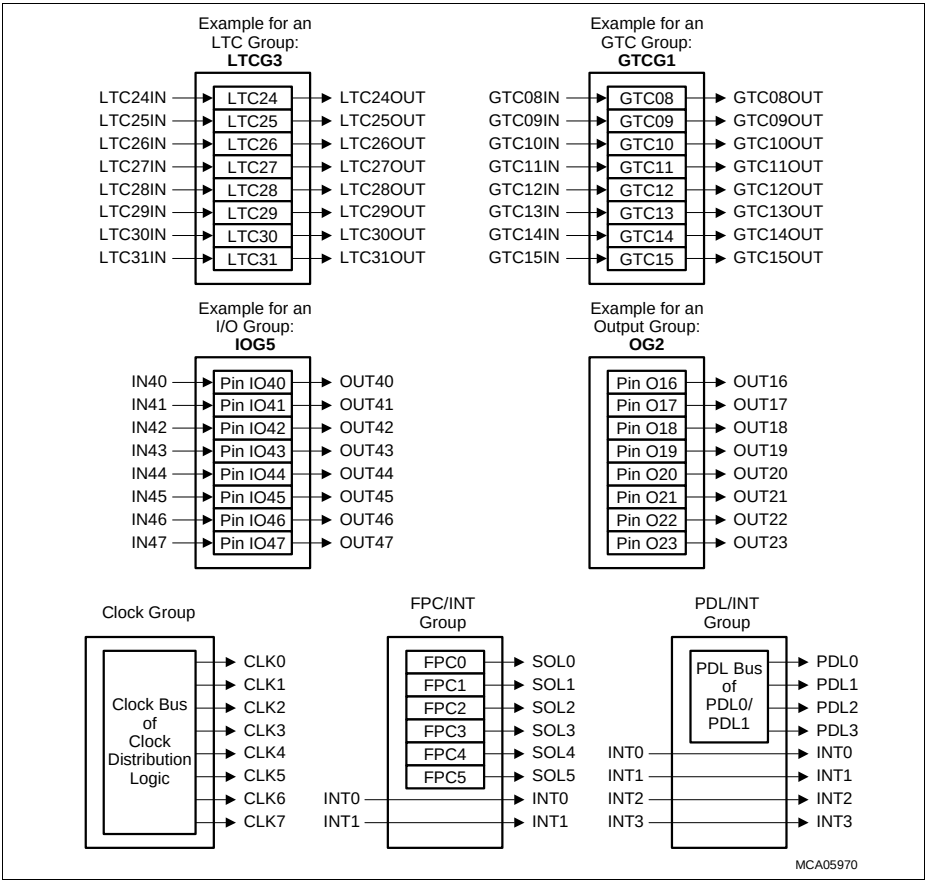


Figure 28-65 Groups Definitions for I/O Line Sharing Block

An **LTC group** combines eight LTC cells with its input and output lines. This results in eight LTC groups, LTCG0 to LTCG7.

A **GTC group** combines eight GTC cells with its input and output lines. This results in four GTC groups, GTCG0 to GTCG3.

An **I/O group** combines eight GPTA®v5 I/O lines connected to bi-directional device pins with its input and output lines. This results in seven I/O groups, IOG0 to IOG6, supporting 56 I/O lines.

An **Output group** combines eight GPTA®v5 output lines connected to device pins as an output. This results in seven output groups, OG0 to OG6, supporting 56 output lines.

The **Clock group** is a group that combines the eight clock bus output signals CLK[7:0] generated by the clock distribution cells.

The **FPC/INT group** is a group that combines the six level output signals SOL[5:0] of the FPCs with two external input lines INT[1:0] of the GPTA®v5 unit.

The **PDL/INT group** is a group that combines the four PDL output lines of the PDL bus with four external input lines INT[3:0] of the GPTA®v5 unit.

An **On-chip trigger and gating signal group** combines eight GPTA®v5 output lines connected to on-chip peripherals. This results in two on-chip trigger and gating signal groups, OTG0 to OG1, supporting 16 on-chip trigger and gating lines.

Table 28-9 Group to I/O Line/Cell Assignment

Group/Unit	Cell/Line	Input	Output
LTC Groups			
LTCG0	LTC[07:00]	LTC[07:00]IN	LTC[07:00]OUT
LTCG1	LTC[15:08]	LTC[15:08]IN	LTC[15:08]OUT
LTCG2	LTC[23:16]	LTC[23:16]IN	LTC[23:16]OUT
LTCG3	LTC[31:24]	LTC[31:24]IN	LTC[31:24]OUT
LTCG4	LTC[39:32]	LTC[39:32]IN	LTC[39:32]OUT
LTCG5	LTC[47:40]	LTC[47:40]IN	LTC[47:40]OUT
LTCG6	LTC[55:48]	LTC[55:48]IN	LTC[55:48]OUT
LTCG7	LTC[63:56]	LTC[63:56]IN	LTC[63:56]OUT
GTC Groups			
GTCG0	GTC[07:00]	GTC[07:00]IN	GTC[07:00]OUT
GTCG1	GTC[15:08]	GTC[15:08]IN	GTC[15:08]OUT
GTCG2	GTC[23:16]	GTC[23:16]IN	GTC[23:16]OUT
GTCG3	GTC[31:24]	GTC[31:24]IN	GTC[31:24]OUT

Table 28-9 Group to I/O Line/Cell Assignment (cont'd)

Group/Unit	Cell/Line	Input	Output
I/O Groups			
IOG0	–	IN[07:00]	OUT[07:00]
IOG1	–	IN[15:08]	OUT[15:08]
IOG2	–	IN[23:16]	OUT[23:16]
IOG3	–	IN[31:24]	OUT[31:24]
IOG4	–	IN[39:32]	OUT[39:32]
IOG5	–	IN[47:40]	OUT[47:40]
IOG6	–	IN[55:48]	OUT[55:48]
Output Groups			
OG0	–	–	OUT[63:56]
OG1	–	–	OUT[71:64]
OG2	–	–	OUT[79:72]
OG3	–	–	OUT[87:80]
OG4	–	–	OUT[95:88]
OG5	–	–	OUT[103:96]
OG6	–	–	OUT[111:104]
On-Chip Trigger and Gating Signals Groups			
OTG0	–	–	OTGS[07:00]
OTG1	–	–	OTGS[15:08]
Clock Group			
–	–	–	CLK[7:0]
FPC/INT Groups			
FPC[5:0]	–	–	SOL[5:0]
External Input [1:0]	–	–	INT[1:0]
PDL/INT Groups			
PDL[1:0] PDL Bus	–	–	PDL[3:0]
External Input [3:0]	–	–	INT[3:0]

28.3.4.1 FPC Input Line Selection

As shown on **Page 28-12**, each FPC cell can be connected to one out of four input lines SINk[3:0], to the GPTA®v5 module clock f_{GPTA}, or to the output of the preceding FPC. In total, 24 input lines out of the 56 input lines IN[55:00] from the I/O groups are connected (not programmable) with the FPCk inputs. The FPCk input line selection is controlled by the FPCCTRk.IPS bit fields. **Table 28-10** shows the FPC input line connections.

Table 28-10 FPC Input Line Assignments

FPC Control Register	Bit Field IPS	Selected Input Signal
FPCCTR0	000_B	IN0
	001_B	IN12
	010_B	IN24
	011_B	IN36
FPCCTR1	000_B	IN2
	001_B	IN14
	010_B	IN26
	011_B	IN38
FPCCTR2	000_B	IN4
	001_B	IN16
	010_B	IN28
	011_B	IN40
FPCCTR3	000_B	IN6
	001_B	IN18
	010_B	IN30
	011_B	IN42
FPCCTR4	000_B	IN8
	001_B	IN20
	010_B	IN32
	011_B	IN44
FPCCTR5	000_B	IN10
	001_B	IN22
	010_B	IN34
	011_B	IN46

28.3.4.2 GTC and LTC Output Multiplexer Selection

The output multiplexer shown in **Figure 28-64** and **Figure 28-66** below connects the 32 GTC output lines and the 64 LTC output lines with the I/O groups (7 × 8 = 56 output lines) and the output groups (7 × 8 = 56 output lines).

In case of low pin count packages, not all I/O groups may be routed to a pin.

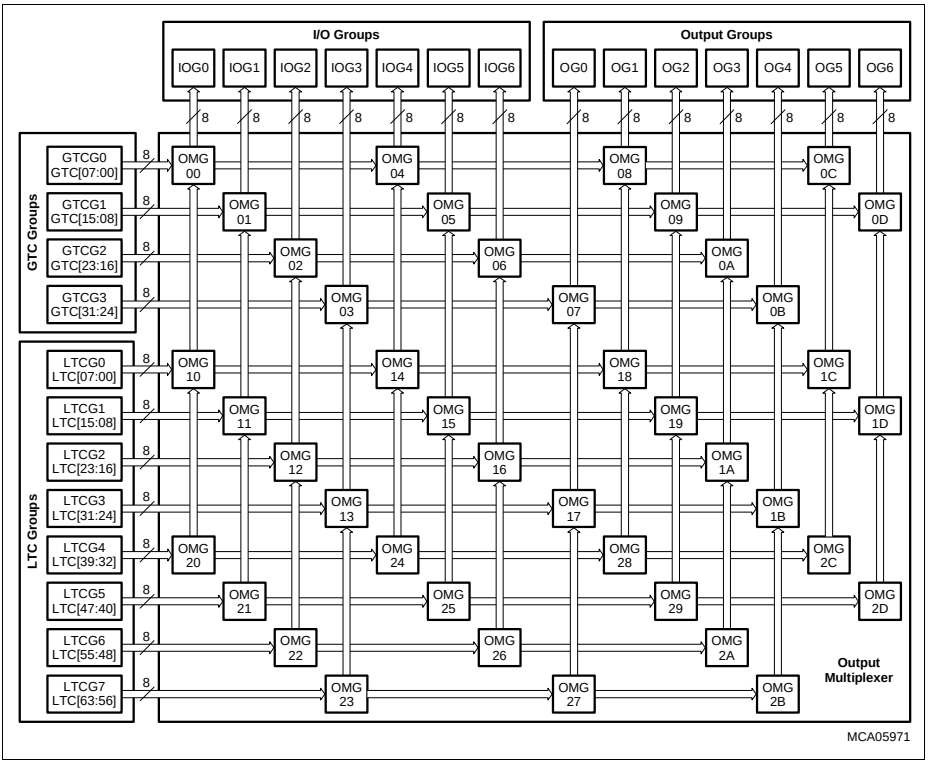


Figure 28-66 Output Multiplexer

The output multiplexer contains Output Multiplexer Groups (OMGs) that connect the Global Timer Cells or Local Timer Cells with the input lines of the I/O groups and output groups. GTCs and LTCs are grouped into four GTC groups (GTCG[3:0]) and eight LTC groups (LTCG[7:0]) with 8 cells each. In the same way, I/O groups and output groups are grouped into 14 groups (seven I/O groups and seven output groups) with 8 lines each.

Figure 28-67 shows the logical structure of an OMG.

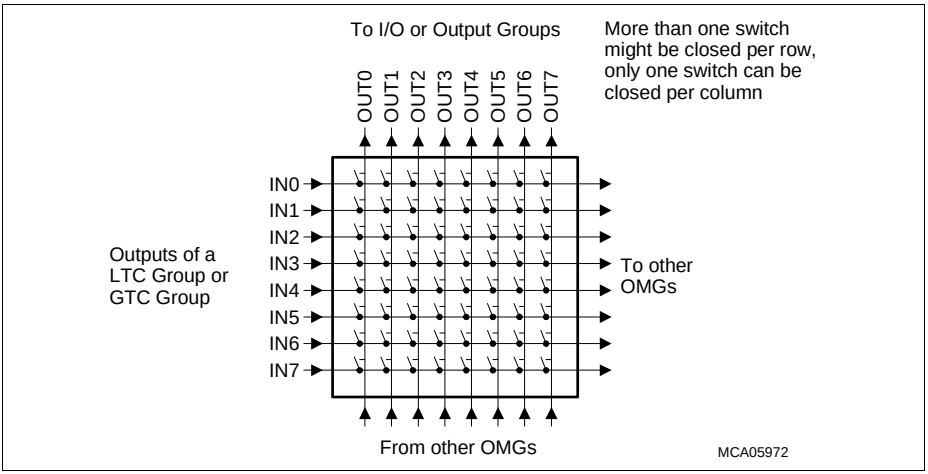


Figure 28-67 Output Multiplexer Group (OMG) Structure

Rules for connections to Output Multiplexer Group OMG:

- Within a GTC or LTC group, the output of the cell with the lowest index number is connected to OMG input line IN0. The remaining cells of a cell group are connected to OMG input lines IN1 to IN7 with ascending cell index numbers.
  Example: for OMG13 (see Figure 28-66), the cells LTC24 up to LTC31 are wired to the OMG13 input lines IN0 to line IN7.
- OMG output line OUT0 is always connected to the input of an I/O or output group with the lowest index. The remaining output lines OUT1 to OUT7 are connected to the I/O or Output lines with ascending index.
  Example: for OMG13 (see Figure 28-66), the outputs OUT0 to OUT7 are wired (via OMG03) to input lines 0 to 7 of I/O group 3 (IOG3).
- One input of an I/O or output group can be connected to the output of only one timer cell. This is guaranteed by the OMG control register layout. Otherwise, short circuits and unpredictable behavior would occur. On the other hand, it is permissible for the output of a GTC or LTC to be connected to more than one input of an I/O or output group.

The output multiplexer group configuration is based on the following principles:

- Each OMG is referenced with two index variables: n and g (OMGng)
- Index n is a group number. Global timer cell groups GTCG[3:0] have the group number 0, Local Timer Cell Groups LTCG[3:0] have the group number 1, and Local Timer Cell Groups LTCG[7:4] have the group number 2.

- Index g indicates the number of an I/O or output group g (g = 0-13$_D$) to which the outputs of the output multiplexer group OMGng are connected. I/O groups IOG0 to IOG6 are assigned to index variable g = 0 to 6 and output groups OG0 to OG6 are assigned to index variable g = 7 to 13.

The output multiplexer logic as seen for programming is shown in **Figure 28-68**. With this logic, always three GTC or LTC group signals are combined to one output line that leads to the input of an I/O or output group. For example, when looking at **Figure 28-66**, each of the eight output multiplexer output lines to I/O group IOG5 is connected via three OMGn5 (n = 0, 1, 2) with the eight outputs of one GTC group (GTCG1) and two LTC groups (LTCG1 and LTCG5).

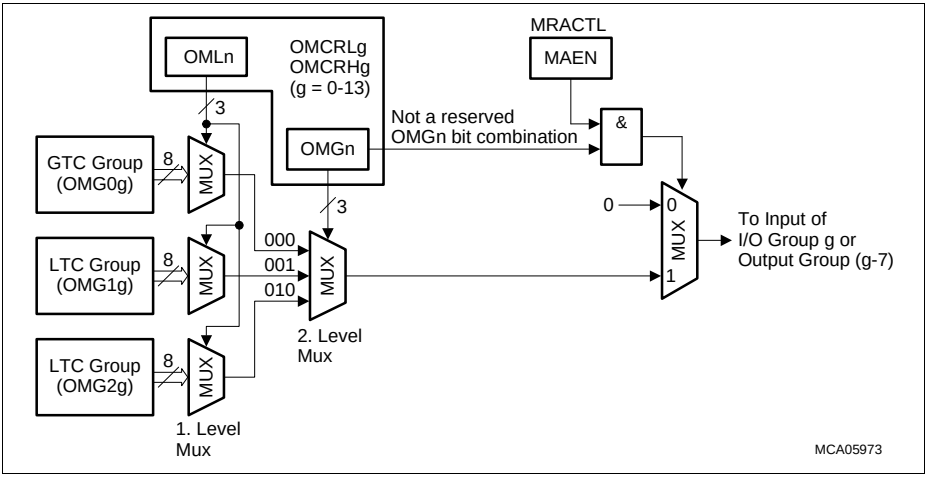


Figure 28-68 Output Multiplexer Group (Programmer's View)

The 1. level multiplexer is built up by three 8:1 multiplexers that are controlled in parallel by bit field OMLn. Bit field OMGn controls the 2. level multiplexer and connects one of the 1. level multiplexer outputs to output n. The output of the 2. level multiplexer is connected only to the input of an I/O group or output group if bit MRACTL.MAEN is set (multiplexer array enabled) and no reserved bit combination of OMGn is selected. If one of these conditions is not true, the corresponding OMG output will be held at a low level.

Two Output GPTA®v5, OMCRL and OMCRH (see also **Page 28-121**), are assigned to each of the I/O or output groups. Therefore, a total of 28 registers control the connections within the output multiplexer of the GPTA®v5 module.

The OMCRL registers control the OMG output lines 0 to 3. The OMCRH registers control the OMG output lines 4 to 7. **Table 28-11** lists all Output Multiplexer Control Registers with its control functions. Please note that the Output Multiplexer Control Registers are

not directly accessible but must be written or read using a FIFO array structure as described on Page 28-121.

Table 28-11 Output Multiplexer Control Register Assignments

I/O Group or Output Group		Controlled by Multiplexer Control Register	Selectable Groups via OMGng
IOG0	IN[03:00]/OUT[03:00]	OMCRL0	GTCG0, LTCG0, LTCG4
	IN[07:04]/OUT[07:04]	OMCRH0	
IOG1	IN[11:08]/OUT[11:08]	OMCRL1	GTCG1, LTCG1, LTCG5
	IN[15:12]/OUT[15:12]	OMCRH1	
IOG2	IN[19:16]/OUT[19:16]	OMCRL2	GTCG2, LTCG2, LTCG6
	IN[23:20]/OUT[23:20]	OMCRH2	
IOG3	IN[27:24]/OUT[27:24]	OMCRL3	GTCG3, LTCG3, LTCG7
	IN[31:28]/OUT[31:28]	OMCRH3	
IOG4	IN[35:32]/OUT[35:32]	OMCRL4	GTCG0, LTCG0, LTCG4
	IN[39:36]/OUT[39:36]	OMCRH4	
IOG5	IN[43:40]/OUT[43:40]	OMCRL5	GTCG1, LTCG1, LTCG5
	IN[47:44]/OUT[47:44]	OMCRH5	
IOG6	IN[51:48]/OUT[51:48]	OMCRL6	GTCG2, LTCG2, LTCG6
	IN[55:52]/OUT[55:52]	OMCRH6	
OG0	OUT[59:56]	OMCRL7	GTCG3, LTCG3, LTCG7
	OUT[63:60]	OMCRH7	
OG1	OUT[67:64]	OMCRL8	GTCG0, LTCG0, LTCG4
	OUT[71:68]	OMCRH8	
OG2	OUT[75:72]	OMCRL9	GTCG1, LTCG1, LTCG5
	OUT[79:76]	OMCRH9	
OG3	OUT[83:80]	OMCRL10	GTCG2, LTCG2, LTCG6
	OUT[87:84]	OMCRH10	
OG4	OUT[91:88]	OMCRL11	GTCG3, LTCG3, LTCG7
	OUT[95:92]	OMCRH11	
OG5	OUT[99:96]	OMCRL12	GTCG0, LTCG0, LTCG4
	OUT[103:100]	OMCRH12	

Table 28-11 Output Multiplexer Control Register Assignments (cont'd)

I/O Group or Output Group		Controlled by Multiplexer Control Register	Selectable Groups via OMGng
OG6	OUT[107:104]	OMCRL13	GTCG1, LTCG1, LTCG5
	OUT[111:108]	OMCRH13	

28.3.4.3 On-chip Trigger and Gating Output Multiplexer Selection

The On-chip Trigger and Gating Signal (OTGS) multiplexer shown in **Figure 28-64** and **Figure 28-69** below connects the 32 GTC output lines and the 64 LTC output lines with the on-chip trigger and gating signal groups ($2 \times 8 = 16$ output lines).

In case of low pin count packages, not all I/O groups may be routed to a pin.

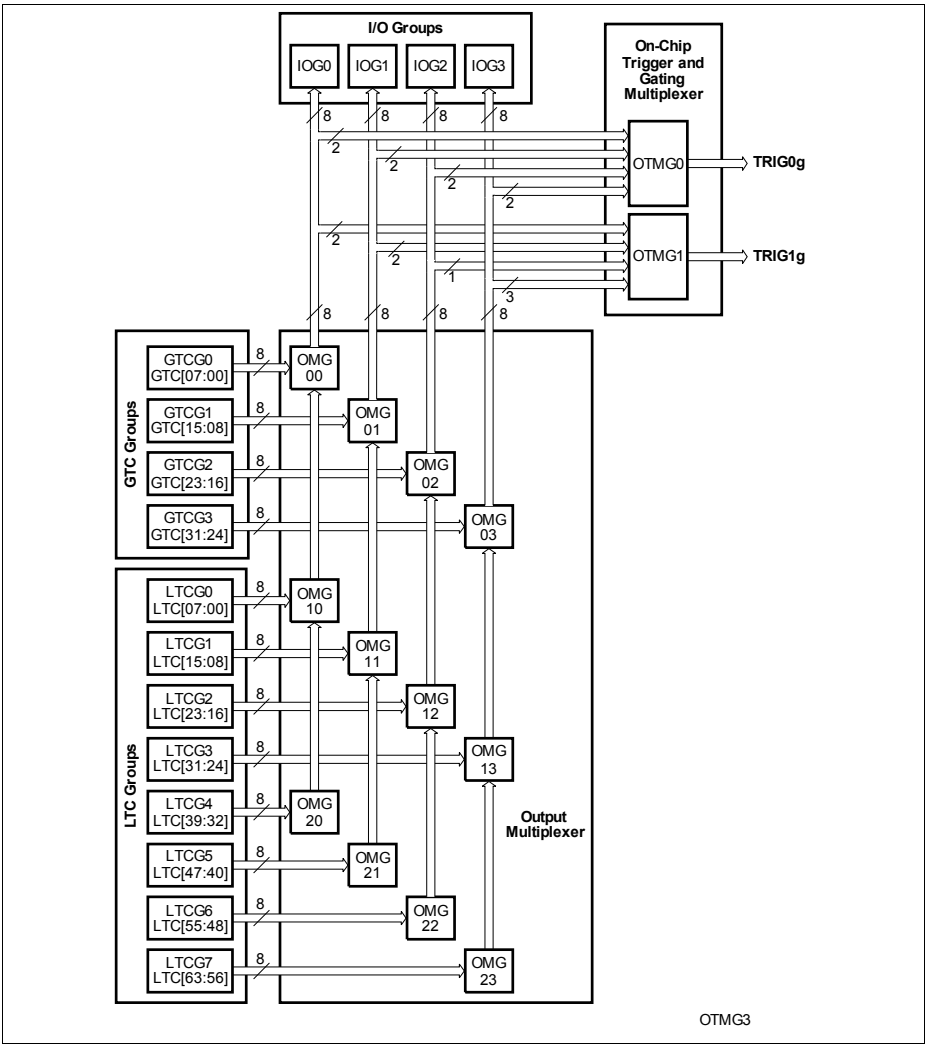


Figure 28-69 On-Chip Trigger and Gating Signal Multiplexer

The On-chip Trigger and Gating Signal multiplexer contains Output Multiplexer Groups (OMGs) that connect the Outputs of the I/O groups with the On-Chip Trigger Signals. These On-Chip Trigger Signals are grouped into two On-Chip Trigger groups (OTMG[1:0]) with 8 cells each.

Figure 28-67 shows the logical structure of an OTMG.

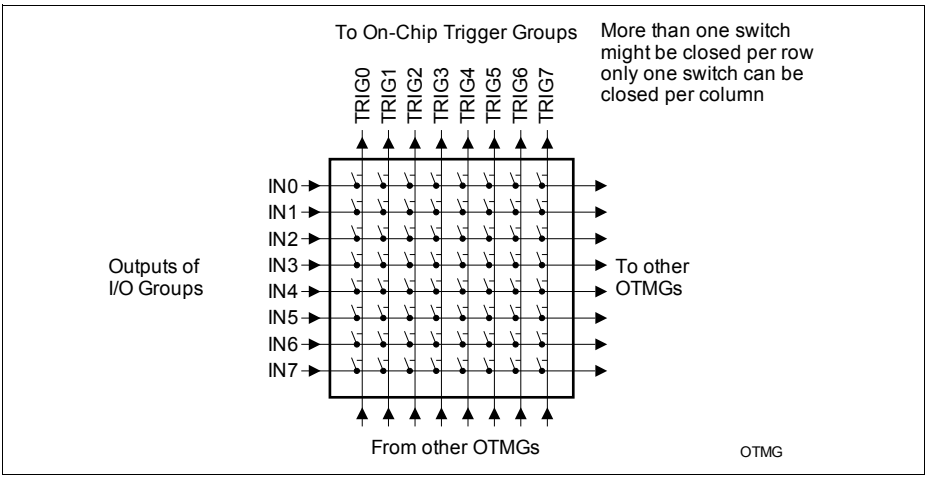


Figure 28-70 On-Chip Trigger and Gating Multiplexer Group (OTMG) Structure

Rules for connections to Output Multiplexer Group OTMG:

- Only one input of an On-chip Trigger and Gating Signal group can be connected to a On-chip Trigger and Gating Signal (TRIG). This is guaranteed by the OTMG control register layout. Otherwise, short circuits and unpredictable behavior would occur. On the other hand, it is permissible for the output of a I/O Group to be connected to more than one on-chip trigger and gating signal (TRIG).

The on-chip trigger and gating multiplexer group configuration is based on the following principles:

- Each OTMG is referenced with a single index variables: g (OTMGg)
- Index g indicates the number of an On-Chip Trigger and Gating Signal multiplexer group g (g = 0-1_D) to which the outputs of the On-Chip Trigger and Gating Signal multiplexer group OTMGg are connected. TRIG00 to TRIG07 are assigned to OTMG0 and TRIG10 to TRIG17 are assigned to OTMG1.

The on-chip trigger and gating signal multiplexer logic as seen for programming is shown in **Figure 28-71**.

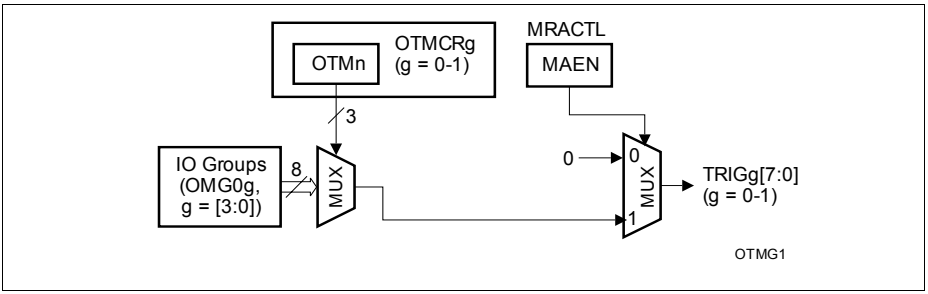


Figure 28-71 On-Chip Trigger and Gating Multiplexer Group (Programmer's View)

The multiplexer is built up by three 8:1 multiplexer that is controlled by bit field OTMn. Bit field The output of the multiplexer is connected only to the on-chip trigger and gating signal TRIGn if bit MRACTL.MAEN is set (multiplexer array enabled). If this condition is not true, the corresponding OTMG output will be held at a low level.

Sixteen on-chip trigger and gating signals are assigned to the GPTA0. Therefore, a total of 2 registers control the connections within the on-chip gating and trigger signal multiplexer of the GPTA0 unit.

Further sixteen on-chip trigger and gating signals are assigned to the GPTA1. Therefore, a total of 2 registers control the connections within the on-chip gating and trigger signal multiplexer of the GPTA1 unit.

The OTMCR0 register control the OTMG output lines TRIG00 to TRIG07. The OTMCR1 register control the OTMG output lines TRIG10 to TRIG17. **Table 28-12** lists all On-Chip Trigger and Gating Signal Multiplexer Control Registers with its control functions. Please note that the On-Chip Trigger and Gating Signal Multiplexer Control Registers are not directly accessible but must be written or read using a FIFO array structure as described on **Page 28-121**.

Table 28-12 On-Chip Trigger/Gating Multiplexer Control Register Assignments

I/O Group Signal		OTMG Input Signal	Controlled by Multiplexer Control Register	Trigger/Gating Signal (x=0-7)	Selectable Groups via OMGng
IOG0	OUT00	IN00	OTMCR0	TRIG0x	GTCG0, LTCG0, LTCG4
IOG0	OUT02	IN01	OTMCR0	TRIG0x	GTCG0, LTCG0, LTCG4
IOG1	OUT08	IN02	OTMCR0	TRIG0x	GTCG1, LTCG1, LTCG5
IOG1	OUT10	IN03	OTMCR0	TRIG0x	GTCG1, LTCG1, LTCG5
IOG2	OUT16	IN04	OTMCR0	TRIG0x	GTCG2, LTCG2, LTCG6
IOG2	OUT19	IN05	OTMCR0	TRIG0x	GTCG2, LTCG2, LTCG6
IOG3	OUT24	IN06	OTMCR0	TRIG0x	GTCG3, LTCG3, LTCG7
IOG3	OUT27	IN07	OTMCR0	TRIG0x	GTCG3, LTCG3, LTCG7
IOG0	OUT01	IN10	OTMCR1	TRIG1x	GTCG0, LTCG0, LTCG4
IOG0	OUT03	IN11	OTMCR1	TRIG1x	GTCG0, LTCG0, LTCG4
IOG1	OUT09	IN12	OTMCR1	TRIG1x	GTCG1, LTCG1, LTCG5
IOG1	OUT11	IN13	OTMCR1	TRIG1x	GTCG1, LTCG1, LTCG5
IOG2	OUT18	IN14	OTMCR1	TRIG1x	GTCG2, LTCG2, LTCG6
IOG3	OUT25	IN15	OTMCR1	TRIG1x	GTCG3, LTCG3, LTCG7
IOG3	OUT26	IN16	OTMCR1	TRIG1x	GTCG3, LTCG3, LTCG7
IOG3	OUT28	IN17	OTMCR1	TRIG1x	GTCG3, LTCG3, LTCG7

28.3.4.4 GTC Input Multiplexer Selection

The GTC input multiplexer as shown in **Figure 28-64** and **Figure 28-72** connects the 56 (= 7 × 8) input lines of the I/O groups, the 64 LTC output lines of the eight LTC groups, the six FPC output lines, and two internal input lines INT[1:0] with the 32 (= 4 × 8) LTC input lines, organized into eight LTC groups.

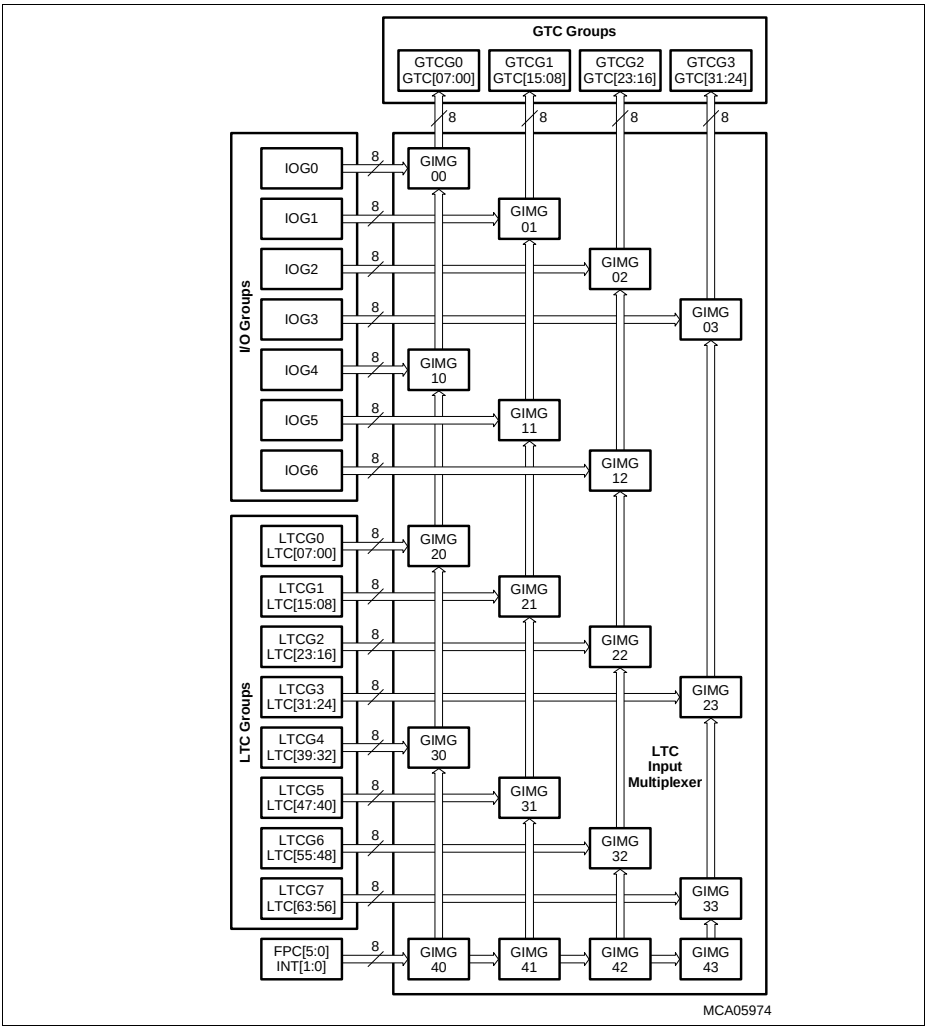


Figure 28-72 GTC Input Multiplexer

The GTC input multiplexer contains GTC input Multiplexer Groups (GIMGs) that connect the I/O groups or Local Timer Cells with the input lines of the GTC input lines, organized into four GTC groups with 8 cells each. GTC input Multiplexer Group are grouped into seven IOGs (IOG[6:0]) with eight lines each and eight LTC groups (LTCG[7:0]) with 8 cells each. One special FPC/INT group with eight outputs is established that combines the six FPC outputs and two internal input lines INT[1:0] as a group of GIMGs inputs.

Figure 28-73 shows the logical structure of a GIMG.

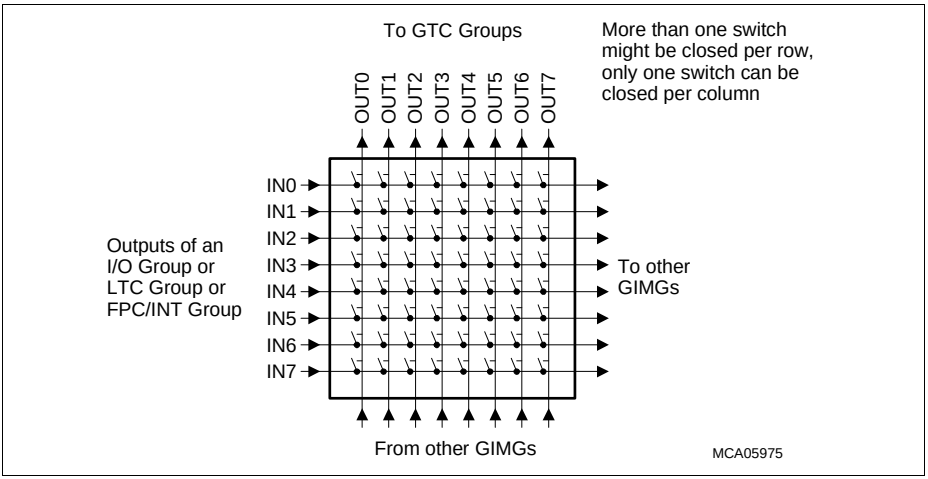


Figure 28-73 GTC Input Multiplexer Group (GIMG) Structure

Rules for connections to GTC Input Multiplexer Group GIMG:

- Within a I/O group or LTC group, the line or the output of the cell with the lowest index number is connected to GIMG input line IN0. The remaining lines, cells or lines of a group are connected to GIMG input lines IN1 to IN7 with ascending index numbers. At the FPC/INT group, FPC[5:0] is connected to IN[5:0] and INT[1:0] is connected to IN[7:6].
  Example: for GIMG23 (see Figure 28-72), the cells LTC24 up to LTC31 are wired to the GIMG23 input lines IN0 to line IN7.
- Multiplexer output OUT0 is always connected to the input of a GTC group with the lowest index. The remaining output lines OUT1 to OUT7 are connected to the GTC inputs with ascending index.
  Example: for GIMG23 (see Figure 28-72), the outputs OUT0 to OUT7 are wired to the inputs of GTC16 to GTC23.
- A GTC input can be connected either to an I/O group output, or to an LTC output, or to an FPC/INT output. This is guaranteed by the GIMG control register layout. Otherwise, short circuits and unpredictable behavior would occur. In contrast, it is permissible for an I/O group output, or an LTC output, or an FPC/INT output to be connected to more than one GTC input.

The GTC input multiplexer group configuration is based on the following principles:

- Each GIMG is referenced with two index variables: n and g (GIMGng)
- Index n is a group number. I/O groups IOG[3:0] have group number 0, I/O groups IOG[6:4] have group number 1, Local Timer Cell Groups LTCG[3:0] have group

number 2, Local Timer Cell Groups LTCG[7:4] have group number 3, and the FPC/INT group has group number 4.

- Index g indicates the number of the GTC group g (g = 0-3) to which the outputs of the input multiplexer group GIMGng are connected.

The GTC input multiplexer logic as seen for programming is shown in **Figure 28-74**. With this logic, five group signals (from an I/O group, LTC group, or FPC/INT group) are always combined to one output line that leads to the input of a GTC of GTC group g. For example, when looking at **Figure 28-73**, each of the eight GTC input multiplexer output lines to GTC group GTCG2 is connected via five OMGn2 (n = 0-4) with the eight outputs of two I/O group (IOG2 and IOG6), two LTC groups (LTCG2 and LTCG6), and the FPC/INT group.

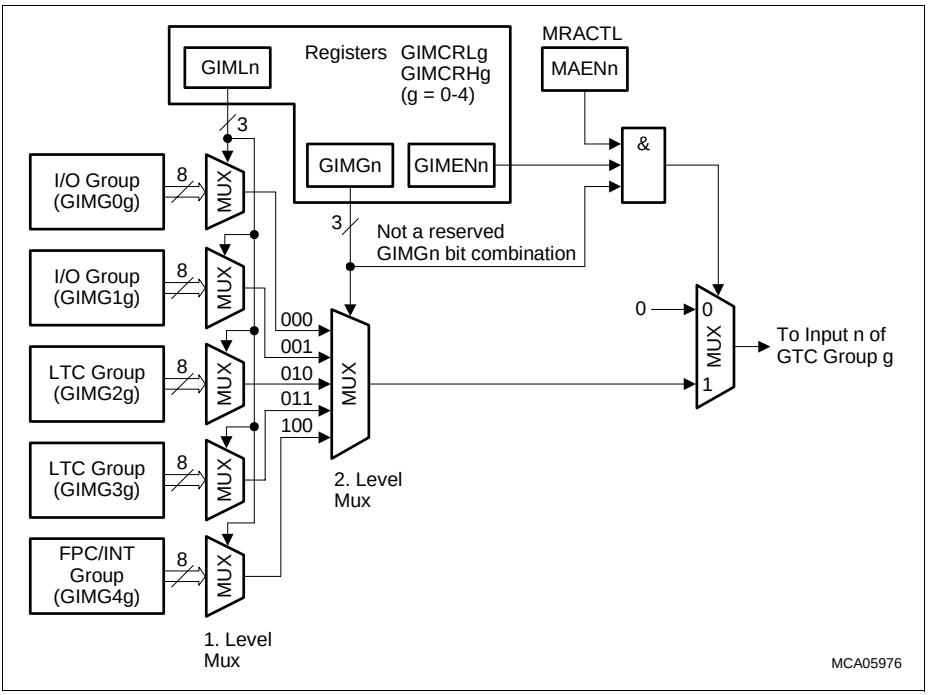


Figure 28-74 GTC Input Multiplexer Group (Programmer's View)

The 1. level multiplexer is built up by five 8:1 multiplexers that are controlled in parallel by bit field GIMLn. Bit field GIMGn controls the 2. level multiplexer and connects one of the 1. level multiplexer outputs to one of the GIMGng outputs. The output of the 2. level multiplexer is only connected to the input of an GTC if bit GIMENn (enable multiplexer connection) is set, and bit MRACTL.AEN is set (multiplexer array enabled), and no

reserved bit combination of GIMGn is selected. If one of these conditions is not true, the corresponding GIMG output will be held at a low level.

If one of these bit is not set, the corresponding GTC input will be held at a low level.

Two GTC Input Multiplexer Control Registers, GIMCRL and GIMCRH (see also Page 28-215), are assigned to each of the GTC groups. Therefore, a total of eight registers control the connections within the GTC input multiplexer of the GPTA®v5 module.

The GIMCRL registers control the GIMG output lines 0 to 3 and the GIMCRH registers control the GIMG output lines 4 to 7. **Table 28-13** lists all of the GTC Input Multiplexer Control Registers with its control functions. Please note that all GTC Input Multiplexer Control Registers are not directly accessible but must be written or read using a FIFO array structure as described on Page 28-121.

Table 28-13 GTC Input Multiplexer Control Register Assignments

GTC Group and GTCs		Controlled by Multiplexer Control Register	Selectable Groups via GIMGng
GTCG0	GTC[03:00]	GIMCRL0	IOG0, IOG4, LTCG0, LTCG4, FPC/INT
	GTC[07:04]	GIMCRH0	
GTCG1	GTC[11:08]	GIMCRL1	IOG1, IOG5, LTCG1, LTCG5, FPC/INT
	GTC[15:12]	GIMCRH1	
GTCG2	GTC[19:16]	GIMCRL2	IOG2, IOG6, LTCG2, LTCG6, FPC/INT
	GTC[23:20]	GIMCRH2	
GTCG3	GTC[27:24]	GIMCRL3	IOG3, LTCG3, LTCG7, FPC/INT
	GTC[31:28]	GIMCRH3	

28.3.4.5 LTC Input Multiplexer Selection

The LTC input multiplexer as shown in **Figure 28-64** and **Figure 28-75** connects the 56 (= 7 × 8) input lines of the I/O groups, the 32 (= 4 × 8) GTC output lines of the GTC groups, the eight clock bus lines, or the four PDL output lines with four internal input lines INT[3:0] with the 64 (= 8 × 8) LTC input lines, organized into eight LTC groups.

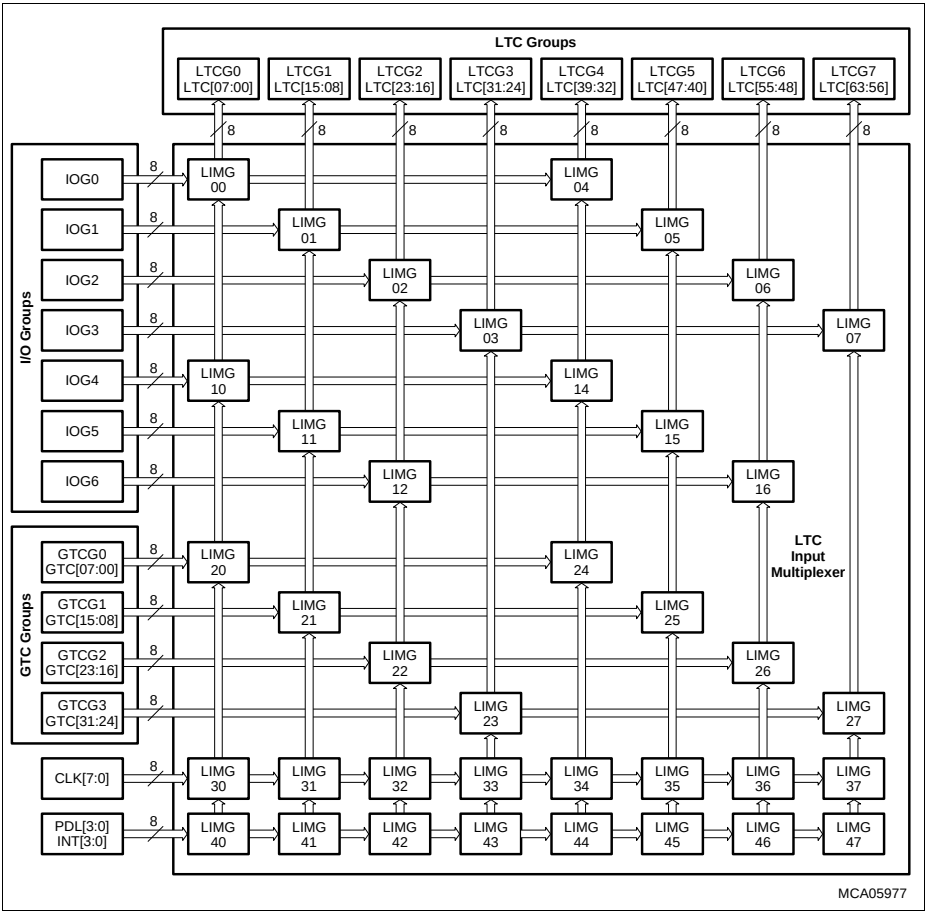


Figure 28-75 LTC Input Multiplexer

The LTC input multiplexer contains LTC input Multiplexer Groups (LIMGs) that connect the I/O groups or Global Timer Cells with the input lines of the LTCs, organized into eight LTC groups with 8 cells each. IOGs and GTCs are grouped into seven IOGs (IOG[6:0]) with eight lines each and four GTC groups (GTCG[3:0]) with 8 cells each. Two special groups are available: a clock group with eight lines representing the clock bus lines CLK[7:0] of the clock distribution cells and a PDL/INT group with eight outputs that combines the four PDL outputs and four internal input lines INT[3:0] as a group of LIMGs inputs.

Note: GPTA0 generates the clock bus lines CLK[7:0] and the four PDL outputs.

Figure 28-76 shows the logical structure of a LIMG.

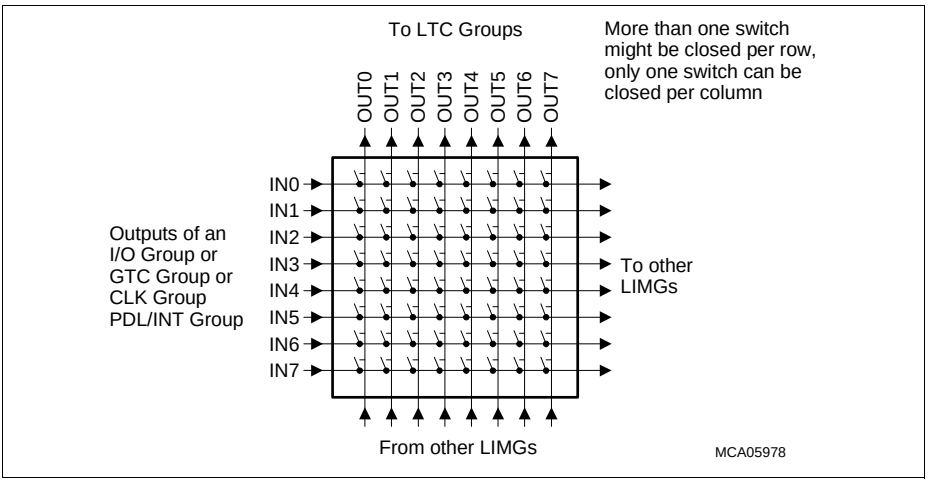


Figure 28-76 LTC Input Multiplexer Group (LIMG) Structure

Rules for connections to LTC Input Multiplexer Group LIMG:

- Within a I/O group or GTC group, the line or the output of the cell with the lowest index number is connected to LIMG input line IN0. The remaining lines, cells or lines of a group are connected to LIMG input lines IN1 to IN7 with ascending index numbers. At the clock group, CLK0 is connected to IN0 and the remaining clock lines are connected to LIMG input lines IN1 to IN7 with ascending index numbers. At the PDL/INT group, PDL[3:0] (see **Page 28-22**) is connected to IN[3:0] and INT[3:0] is connected to IN[7:4].
  Example: for LIMG23 (see **Figure 28-75**), the cells GTC24 up to GTC31 are wired to the LIMG23 input lines IN0 to line IN7.
- Multiplexer output OUT0 is always connected to the input of an LTC group with the lowest index. The remaining output lines OUT1 to OUT7 are connected to the LTC inputs with ascending index.

Example: for LIMG23 (see **Figure 28-75**), the outputs OUT0 to OUT7 are wired to the inputs of LTC24 to GTC31.

- An LTC input can be connected either to an I/O group output, or to an GTC output, or to a clock bus output, or to an PDL/INT output. This is guaranteed by the LIMG control register layout. Otherwise, short circuits and unpredictable behavior would occur. In contrast, it is permitted that an I/O group output, or an GTC output, or an PDL/INT output is connected to more than one LTC input.

The LTC input multiplexer group configuration is based on the following principles:

- Each LIMG is referenced with two index variables: n and g (LIMGng)
- Index n is a group number. I/O groups IOG[3:0] have group number 0, I/O groups IOG[6:4] have group number 1, Global Timer Cell Groups GTCG[3:0] have group number 2, clock bus lines CLK[7:0] have group number 3, and the PDL/INT group has group number 4.
- Index g indicates the number of the LTC group g (g = 0-7) to which the outputs of the input multiplexer group LIMGng are connected.

The LTC input multiplexer logic as seen for programming is shown in **Figure 28-77**. With this logic, five group signals (from an I/O group, GTC group, clock group, or PDL/INT group) are always combined to one output line that leads to the input of an LTC of LTC group g. For example, when looking at **Figure 28-75**, each of the eight LTC input multiplexer output lines to LTC group LTCG2 is connected via five LIMGn2 (n = 0-4) with the eight outputs of two I/O group (IOG2 and IOG6), one GTC group (GTCG2), the clock group, and the PDL/INT group.

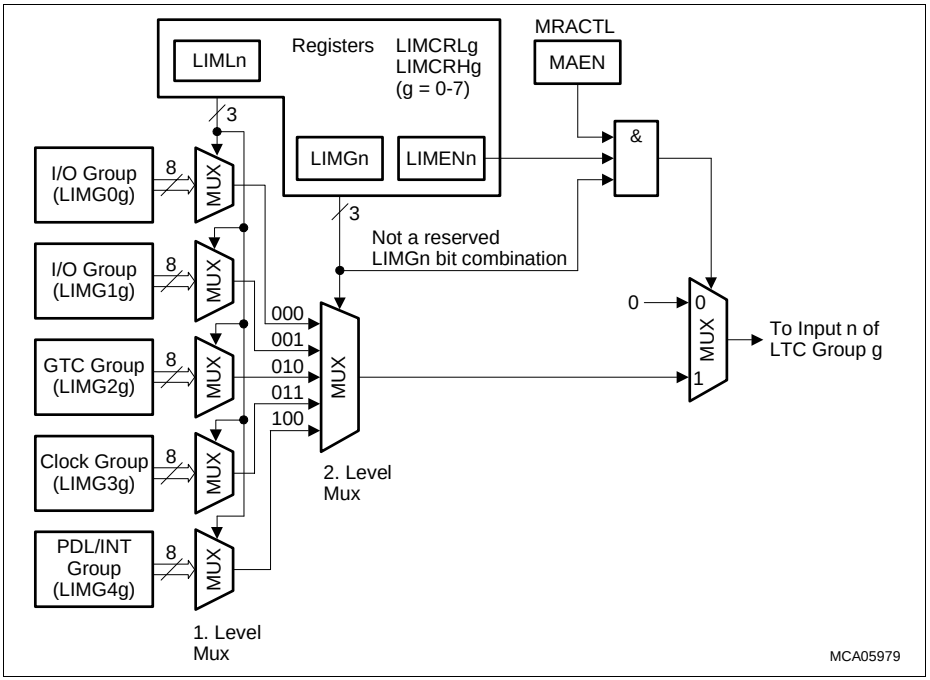


Figure 28-77 LTC Input Multiplexer Group (Programmer's View)

The 1. level multiplexer is built up by five 8:1 multiplexers that are controlled in parallel by bit field LIMLn. Bit field LIMGn controls the 2. level multiplexer and connects one of the 1. level multiplexer outputs to one of the LIMGng outputs. The output of the 2. level multiplexer is connected only to the input of an LTC if bit LIMENn is set (enable multiplexer connection), and bit MRACTL.AEN is set (multiplexer array enabled), and no reserved bit combination of LIMGn is selected. If one of these conditions is not true, the corresponding LTC input will be held at a low level.

Two LTC Input Multiplexer Control Registers, LIMCRL and LIMCRH (see also **Page 28-219**), are assigned to each of the LTC groups. Therefore, in total sixteen registers control the connections within the LTC input multiplexer of the GPTA®v5 module.

The LIMCRL registers control the LIMG output lines 0 to 3 and the GIMCRH registers control the LIMG output lines 4 to 7. **Table 28-14** lists all LTC Input Multiplexer Control Registers with its control functions. Please note that all LTC Input Multiplexer Control Registers are not directly accessible but must be written or read using a FIFO array structure as described on **Page 28-121**.

Table 28-14 LTC Input Multiplexer Control Register Assignments

LTC Group and LTCs		Controlled by Register	Selectable Groups via LIMGng
LTCG0	LTC[03:00]	LIMCRL0	IOG0, IOG4, GTCG0, CLOCK, PDL/INT
	LTC[07:04]	LIMCRH0	
LTCG1	LTC[11:08]	LIMCRL1	IOG1, IOG5, GTCG1, CLOCK, PDL/INT
	LTC[15:12]	LIMCRH1	
LTCG2	LTC[19:16]	LIMCRL2	IOG2, IOG6, GTCG2, CLOCK, PDL/INT
	LTC[23:20]	LIMCRH2	
LTCG3	LTC[27:24]	LIMCRL3	IOG3, GTCG3, CLOCK, PDL/INT
	LTC[31:28]	LIMCRH3	
LTCG4	LTC[35:32]	LIMCRL4	IOG0, IOG4, GTCG0, CLOCK, PDL/INT
	LTC[39:36]	LIMCRH4	
LTCG5	LTC[43:40]	LIMCRL5	IOG1, IOG5, GTCG1, CLOCK, PDL/INT
	LTC[47:44]	LIMCRH5	
LTCG6	LTC[51:48]	LIMCRL6	IOG2, IOG6, GTCG2, CLOCK, PDL/INT
	LTC[55:52]	LIMCRH6	
LTCG7	LTC[59:56]	LIMCRL7	IOG3, GTCG3, CLOCK, PDL/INT
	LTC[63:60]	LIMCRH7	

28.3.4.6 Multiplexer Register Array Programming

A total of 54 control registers are required to program the configuration of the output multiplexer, the On-chip trigger and gating multiplexer, and the two input multiplexers of the Input/Output Line Sharing Block. These IOLS control registers are combined into a Multiplexer Register Array FIFO that can only be read or written sequentially. Therefore, the control registers values cannot be accessed directly but must be accessed in a specific sequential order.

Three registers are available for controlling the Multiplexer Register Array:

- Multiplexer Register Array Control Register MRACTL
- Multiplexer Register Array Data In Register MRADIN
- Multiplexer Register Array Data Out Register MRADOUT

Figure 28-78 shows the structure of the multiplexer array FIFO with the arrangement of the multiplexer control registers.

For programming of the multiplexer array FIFO, the following steps must be executed:

1. Disable interconnections of the multiplexer array by writing MRACTL.MAEN = 0 (default after reset). The multiplexer array is disabled, all cell input lines are driven with 0, and device pins assigned to GPTA®v5 I/O lines or output lines are disconnected.
2. Reset the write cycle counter to 0 by writing MRACTL.WCRES = 1.
3. Write sequentially the multiplexer control register contents one after the other (54 values) into MRADIN, starting with the register values for OTMCR1, OTMCR0, … up to GIMCRH0, GIMCRL0 (see **Figure 28-78**). After the first MRADIN write operation, the contents for OTMCR1 is at FIFO position 1. With each following MRADIN write operation, it becomes shifted one FIFO position upwards. After the 54. MRADIN write operation, the OTMCR1 value is at its final position. The contents of FIFO position 54 can be read via register MRADOUT. With each MRADIN write operation the write cycle counter MRACTL.FIFOFILLCNT is incremented by 1. After all FIFO entries have been written, the FIFO is locked, bit MRACTL.FIFOFULL is set, and further MRADIN write operations are discarded until bit MRACTL.WCRES is written again with a 0.
4. Enable the multiplexer array by writing MRACTL.MAEN = 1. This establishes and enables all programmed interconnections.

To check the FIFO contents, the FIFO can be written a second time. At this check MRADIN is written before MRADOUT is read. This will return the FIFO contents of the first write sequence in the order of OTMCR1, OTMCR0, …, GIMCRH0, GIMCRL0.

Before disabling the multiplexer array FIFO, GPTA®v5 output pins that are already enabled as GPTA®v5 output should be switched to GPIO function to avoid output spikes. After enabling the multiplexer array FIFO again, the GPTA®v5 output can be switched again back to GPTA®v5 output function.

Shifting the write data through the FIFO requires a few clock cycles. When new data becomes written before the FIFO is ready to accept them, wait states will be inserted into the write access.

If the OMCRLg register bit field OMGn of the multiplexer array is programmed with an invalid (reserved) value, the related outputs will be forced to 0. When the array is disabled (MRACTL.MAEN = 0), all cell inputs and outputs are disconnected from the GPIO lines and are driven with 0.

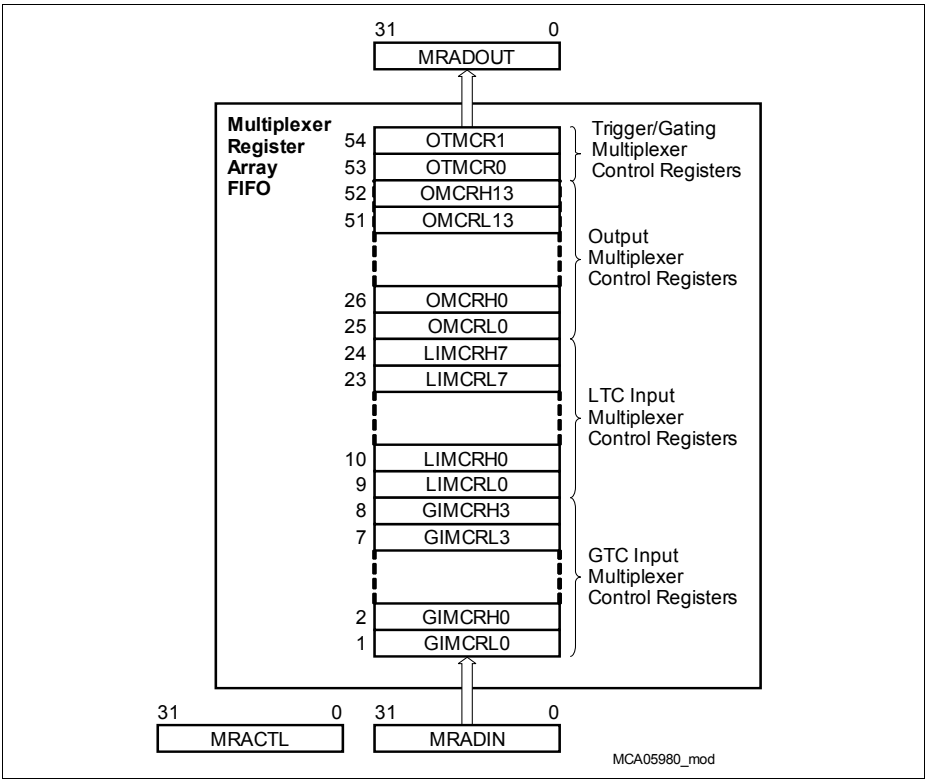


Figure 28-78 GPTA®v5 Multiplexer Array Control Register FIFO Structure

28.3.5 Interrupt Sharing Block (IS)

The GPTA®v5 provides 111 service request sources. These service request sources are generated by different cell types, as shown in **Table 28-15**.

Table 28-15 GPTA®v5 Number of Service Request Sources

Cell Type	Number of Cells	Number of Service Request Sources/Cell	Total Number of Request Sources
DCM	4	3	12
PLL	1	1	1
GT	2	1	2
GTC	32	1	32
LTC	64	1	64
			Sum: 111

To reduce hardware and software overhead, at maximum five request sources are combined together in service request groups. A service request group has up to five service request inputs and one service request output SRy which is typically connected outside the GPTA®v5 kernel with a standard interrupt node y and controlled by its SRCy register.

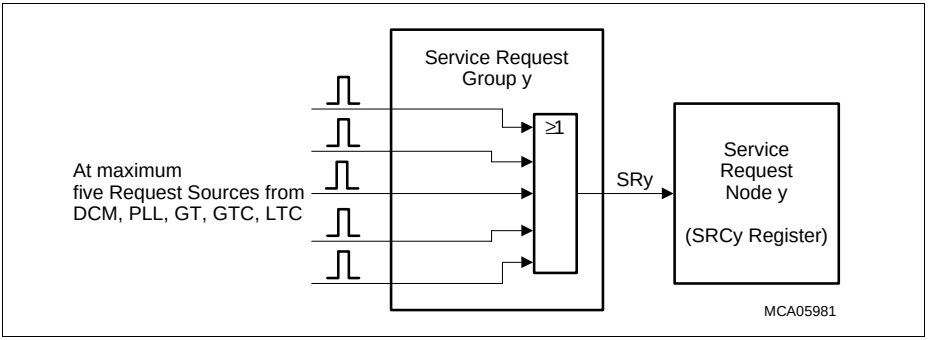


Figure 28-79 Service Request Groups

The bits in the Service Request State Registers (SRSSx and SRSCx) are service request status flags that are set by hardware (type “h”) when the related event occurs. Each GPTA®v5 service request source has its own service request flag. This flag is normally set by hardware but can be set and reset by software. Each service request status flag can be read twice, at the same bit location in the SRSCx register and in the SRSSx register, and cleared or set by software when writing to the corresponding request bit in SRSCx or SRSSx. When writing to SRSCx or SRSSx, several request flags

can be cleared at once by one write operation. Request flags of bit positions that are written with 0 are not changed. This feature allows fast, simple clearing or setting of request flags without affecting other bits in the same service request state register.

Note that service request flag is always set independently of whether it is enabled or disabled by the related cell; but the service request line to the corresponding service request group becomes only active if the corresponding service request is enabled by the related cell. Finally, each service request group y must be enabled by the enable flag that is located in SRC register y.

Table 28-16 lists all of the service requests groups with its request sources. Note that service requests of GTCs with an odd index number k can be individually redirected via register SRNR to a service request group that is assigned mainly to four LTCs.

Table 28-16 GPTA®v5 Service Request Groups

Service Request Group Number y	Request Source 1	Request Source 2	Request Source 3	Request Source 4	Request Source 5
00	DCM0 rising	DCM0 falling	DCM0 comp.	–	–
01	DCM1 rising	DCM1 falling	DCM1 comp.	–	–
02	DCM2 rising	DCM2 falling	DCM2 comp.	–	–
03	DCM3 rising	DCM3 falling	DCM3 comp.	–	–
04	PLL	–	–	–	–
05	GT0	GT1	–	–	–
06	GTC00	GTC01[1)]	–	–	–
07	GTC02	GTC03[1)]	–	–	–
08	GTC04	GTC05[1)]	–	–	–
09	GTC06	GTC07[1)]	–	–	–
10	GTC08	GTC09[1)]	–	–	–
11	GTC10	GTC11[1)]	–	–	–
12	GTC12	GTC13[1)]	–	–	–
13	GTC14	GTC15[1)]	–	–	–
14	GTC16	GTC17[1)]	–	–	–
15	GTC18	GTC19[1)]	–	–	–
16	GTC20	GTC21[1)]	–	–	–
17	GTC22	GTC23[1)]	–	–	–
18	GTC24	GTC25[1)]	–	–	–
19	GTC26	GTC27[1)]	–	–	–

Table 28-16 GPTA®v5 Service Request Groups (cont'd)

Service Request Group Number y	Request Source 1	Request Source 2	Request Source 3	Request Source 4	Request Source 5
20	GTC28	GTC29[1)]	–	–	–
21	GTC30	GTC31[1)]	–	–	–
22	LTC00	LTC01	LTC02	LTC03	GTC01[2)]
23	LTC04	LTC05	LTC06	LTC07	GTC03[2)]
24	LTC08	LTC09	LTC10	LTC11	GTC05[2)]
25	LTC12	LTC13	LTC14	LTC15	GTC07[2)]
26	LTC16	LTC17	LTC18	LTC19	GTC09[2)]
27	LTC20	LTC21	LTC22	LTC23	GTC11[2)]
28	LTC24	LTC25	LTC26	LTC27	GTC13[2)]
29	LTC28	LTC29	LTC30	LTC31	GTC15[2)]
30	LTC32	LTC33	LTC34	LTC35	GTC17[2)]
31	LTC36	LTC37	LTC38	LTC39	GTC19[2)]
32	LTC40	LTC41	LTC42	LTC43	GTC21[2)]
33	LTC44	LTC45	LTC46	LTC47	GTC23[2)]
34	LTC48	LTC49	LTC50	LTC51	GTC25[2)]
35	LTC52	LTC53	LTC54	LTC55	GTC27[2)]
36	LTC56	LTC57	LTC58	LTC59	GTC29[2)]
37	LTC60	LTC61	LTC62	LTC63	GTC31[2)]

1) Redirection bit SRNR.GTCkR = 0 (k = 01, 03, 05, … 27, 29, 31).

2) Redirection bit SRNR.GTCkR = 1 (k = 01, 03, 05, … 27, 29, 31).

28.3.6 Pseudo Code Description of GPTA®v5 Kernel Functionality

This section describes the functional algorithms of the GPTA®v5 cells in a pseudo code language.

28.3.6.1 FPC Algorithm

FPCk_Control_Logic() “to be performed every GPTA®v5 clock”

```
switch (FPCk.Mode)
  case PRESCALER_RISING:
    if (FPCk.Rising_Edge) then
      Prescaler()
    endif
    break
  case PRESCALER_FALLING:
    if (FPCk.Falling_Edge) then
      Prescaler()
    endif
    break
  case DELAYED_FILTER_BOTH:
    Delayed_Filter()
    break
  case IMMEDIATE_FILTER_BOTH:
  case IMMEDIATE_FILTER_RISING:
  case IMMEDIATE_FILTER_FALLING:
    Immediate_Filter()
    break
  case MIXED_FILTER_RISING_DELAYED:
    if (FPCk.Signal_Filtered == 0) then
      Delayed_Filter()
    else
      Immediate_Filter()
    endif
    break
  case MIXED_FILTER_RISING_IMMEDIATE:
    if (FPCk.Signal_Filtered == 0) then
      Immediate_Filter()
    else
      Delayed_Filter()
    endif
    break
endswitch
```

Delayed_Filter()

```
if (FPCk.Filter_Clock[n]) then
  if (FPCk.Timer >= FPCk.Compare_Value) then
    if (FPCk.Compare_Value == 0) then    //by-pass
      if (FPCk.Signal_Output.Level != FPCk.Signal_Input[m]) then
        generate pulse on FPCk.Signal_Output.Transition
        FPCk.Signal_Output.Level = FPCk.Signal_Input[m]
        FPCk.Signal_Filtered = FPCk.Signal_Output.Level
      endif
    else    //delay time is over
      generate pulse on FPCk.Signal_Output.Transition
      FPCk.Signal_Output.Level = !FPCk.Signal_Output.Level
      FPCk.Signal_Filtered = FPCk.Signal_Output.Level
    endif
    FPCk.Timer = 0
  else
    if (FPCk.Timer != 0) then      //delay time is running
      if (FPCk.Rising_Edge is detected) then      //edge detection done at clock input
        FPCk.Rising_Edge_Glitch = 1
      else
        if (FPCk.Falling_Edge is detected) then     //edge detection done at clock input
          FPCk.Falling_Edge_Glitch = 1
        endif
      endif
    endif
    if (FPCk.Signal_Output.Level != FPCk.Signal_Input[m])
    then    //expected level
      FPCk.Timer ++
    else    //unexpected level
      if (FPCk.Timer != 0) then
        if (FPCk.Reset_Timer) then
          FPCk.Timer = 0
        else
          FPCk.Timer --
        endif
      endif
    endif
  endif
endif
```

Prescaler()

```
if (FPCk.Timer >= FPCk.Compare_Value) then
  generate pulse on FPCk.Signal_Output.Transition
  generate pulse on FPCk.Signal_Output.Level
  FPCk.Timer = 0
else
  FPCk.Timer ++
endif
```

Immediate_Filter()

```
if (FPCk.Filter_Clock[n]) then
  if (FPCk.Timer == 0) then
    if (FPCk.Signal_Output.Level != FPCk.Signal_Input[m]) ) then    //change detected
      generate pulse on FPCk.Signal_Output.Transition
      FPCk.Signal_Output.Level = FPCk.Signal_Input[m]
      if ( (FPCk.Compare_Value == 0) or
      ((FPCk.Mode == IMMEDIATE_FILTER_RISING) and !FPCk.Signal_Input[m]) or
      ((FPCk.Mode == IMMEDIATE_FILTER_FALLING) and FPCk.Signal_Input[m]) )
      then    //by-pass
        FPCk.Signal_Filtered = FPCk.Signal_Output.Level
      else    //start delay time
        FPCk.Timer ++
      endif
    endif
  else
    if (FPCk.Timer >= FPCk.Compare_Value) then    //delay time is over
      FPCk.Timer = 0
      FPCk.Signal_Filtered = FPCk.Signal_Output.Level
    else    //delay time is running
      FPCk.Timer ++
      if (FPCk.Rising_Edge) then
        FPCk.Rising_Edge_Glitch = 1
      else
        if (FPCk.Falling_Edge) then
          FPCk.Falling_Edge_Glitch = 1
        endif
      endif
    endif
  endif
endif
```

Variables

Input, Local, Output variables of the cell (I, L, O)

Name k = [0 to 5] for FPC m = [0 to 5] for Signal n = [0 to 3] for Clock	Short Name (*)FPC	Used (ILO)	Comment
FPCk.Signal_Input[m]	*SINm	I	Signal input selected by FPCk.Input_Source
FPCk.Filter_Clock[n]	*CINn	I	Filter Clock selected by FPCk.Clock_Source
FPCk.Rising_Edge	*RE	L	Signal coming from the edge detect
FPCk.Falling_Edge	*FE	L	Signal coming from the edge detect
FPCk.Signal_Filtered	*SF	L	Filtered output signal (after delay time), initialized to 0 at reset
FPCk.Signal_Output.Transition FPCk.Signal_Output.Level	*SOTk *SOLk	O	Transition/Level of the output signal, initialized to 0 at reset

Global variables

Name k = [0 to 5] for FPC	Short Name (*)FPC	Size (bits)	Function
FPCk.Mode	*MODk	3	Selects one of these modes: DELAYED_FILTER_BOTH IMMEDIATE_FILTER_BOTH IMMEDIATE_FILTER_RISING IMMEDIATE_FILTER_FALLING MIXED_FILTER_RISING_DELAYED MIXED_FILTER_RISING_IMMEDIATE PRESCALER_RISING PRESCALER_FALLING
FPCk.Input_Source	*IPSk	3	Selects input signal
FPCk.Clock_Source	*CLKk	2	Selects FPC clock
FPCk.Rising_Edge_Glitch	*REGk	1	Bit is set when rising edge glitch occurs during filtering
FPCk.Falling_Edge_Glitch	*FEGk	1	Bit is set when falling edge glitch occurs during filtering
FPCk.Timer	*TIMk	16	Timer value
FPCk.Reset_Timer	*RTGk	1	Reset timer on glitch in Delayed Filter Mode
FPCk.Compare_Value	*CMPk	16	Compare value

28.3.6.2 PDL-Algorithm

PDLx_Control_Logic() “to be performed every GPTA®v5 clock”

```
if (x == 0) then
  S1.Level = FPC0.Signal_Output.Level
  S1.Transition = FPC0.Signal_Output.Transition
  S2.Level = FPC1.Signal_Output.Level
  S2.Transition = FPC1.Signal_Output.Transition
  S3.Level = FPC2.Signal_Output.Level
  S3.Transition = FPC2.Signal_Output.Transition
else   //x = 1
  S1.Level = FPC3.Signal_Output.Level
  S1.Transition = FPC3.Signal_Output.Transition
  S2.Level = FPC4.Signal_Output.Level
  S2.Transition = FPC4.Signal_Output.Transition
  S3.Level = FPC5.Signal_Output.Level
  S3.Transition = FPC5.Signal_Output.Transition
endif

if (PDLx.Three_Sensors_Enable) then
  Three_Sensors()
else
  Two_Sensors()
endif

if (PDLx.Mux) then
  PDLx.Signal_Output1.Level = 1
  if (PDLx.Signal_Forward or PDLx.Signal_Backward) then
    PDLx.Signal_Output1.Transition = 1
  else
    PDLx.Signal_Output1.Transition = 0
  endif
else
  PDLx.Signal_Output1.Transition = S1.Transition
  PDLx.Signal_Output1.Level = S1.Level
endif
```

Two_Sensors()

```
if ( ( S1.Level and !S2.Level and S1.Transition) or
     ( S1.Level and  S2.Level and S2.Transition) or
     (!S1.Level and  S2.Level and S1.Transition) or
     (!S1.Level and !S2.Level and S2.Transition) ) then
   generate pulse on PDLx.Signal_Forward
else
   if ( ( S1.Level and  S2.Level and S1.Transition) or
        (!S1.Level and  S2.Level and S2.Transition) or
        (!S1.Level and !S2.Level and S1.Transition) or
        ( S1.Level and !S2.Level and S2.Transition) ) then
      generate pulse on PDLx.Signal_Backward
   endif
endif

PDLx.Signal_Output2.Level = S3.Level
PDLx.Signal_Output2.Transition = S3.Transition
```

Three_Sensors()

```
if ( ( S1.Level and !S2.Level and  S3.Level and S1.Transition) or
     ( S1.Level and !S2.Level and !S3.Level and S3.Transition) or
     ( S1.Level and  S2.Level and !S3.Level and S2.Transition) or
     (!S1.Level and  S2.Level and !S3.Level and S1.Transition) or
     (!S1.Level and  S2.Level and  S3.Level and S3.Transition) or
     (!S1.Level and !S2.Level and  S3.Level and S2.Transition) ) then
   generate pulse on PDLx.Signal_Forward
else
   if ( ( S1.Level and  S2.Level and !S3.Level and S1.Transition) or
        (!S1.Level and  S2.Level and !S3.Level and S3.Transition) or
        (!S1.Level and  S2.Level and  S3.Level and S2.Transition) or
        (!S1.Level and !S2.Level and  S3.Level and S1.Transition) or
        ( S1.Level and !S2.Level and  S3.Level and S3.Transition) or
        ( S1.Level and !S2.Level and !S3.Level and S2.Transition) ) then
      generate pulse on PDLx.Signal_Backward
   endif
endif

if ( (S1.Level == S2.Level) and (S1.Level == S3.Level) ) then    //error
   if (!PDLx.Signal_Output2.Level) then    //rising edge
      generate pulse on PDLx.Signal_Output2.Transition
   endif
   PDLx.Signal_Output2.Level = 1
   PDLx.Error = 1
else    //no error
   if (PDLx.Signal_Output2.Level) then    //falling edge
      generate pulse on PDLx.Signal_Output2.Transition
   endif
   PDLx.Signal_Output2.Level = 0
endif
```

Variables

Input, Local, Output variables of the cell (I, L, O)

Name x = [0,1] for PDL k = [0 to 5] for FPC	Short Name (*)PDL	Used (ILO)	Comment
FPCk.Signal_Output.Transition FPCk.Signal_Output.Level	SOTk SOLk	I	Transition/Level of signals coming from FPC
S1.Transition, S1.Level S2.Transition, S2.Level S3.Transition, S3.Level	S1T, S1L S2T, S2L S3T, S3L	L	Transition/Level of Local FPC signals
PDLx.Signal_Output1.Transition PDLx.Signal_Output1.Level	SIT0, SIL0 SIT2, SIL2	O	Transition/Level of Output 1 signal going to DCM0/DCM2
PDLx.Signal_Output2.Transition PDLx.Signal_Output2.Level	SIT1, SIL1 SIT3, SIL3	O	Transition/Level of Output 2 signal going to DCM1/DCM3
PDLx.Signal_Forward	*F0 *F1	O	Forward signals to be counted by LTC
PDLx.Signal_Backward	*B0 *B1	O	Backward signals to be counted by LTC

Global variables

Name x = [0,1] for PDL	Short Name (*)PDL	Size (bits)	Function
PDLx.Mux	*MUXx	1	Selects PDL speed signal (instead of FPC feed-through signal) for output 1
PDLx.Three_Sensors_Enable	*TSEx	1	Selects 3-sensor option and PDL error signal (instead of FPC feed-through signal) for output 2
PDLx.Error	*ERRx	1	Allows the software to read PDL error

28.3.6.3 DCM-Algorithm

DCMk_Control_Logic() “to be performed every GPTA®v5 clock”

```
Compare()
Add_Clock()
Check_Input()
```

Compare()

```
if (DCMk.Timer == DCMk.Capcom_Value) then
  trig(DCMk.Service_Request_Compare)
endif
```

Add_Clock()

```
if (DCMk.Clock_Request) then
  Generate DCMk.Signal_Output
  DCMk.Clock_Request = 0
endif
```

Check_Input()

```
if (DCMk.Signal_Input.Transition) then
  if (DCMk.Signal_Input.Level) then    //rising edge
    trig(DCMk.Service_Request_Rising)
    if (DCMk.Capture_On_Rising_Edge) then
      DCMk.Capture_Value = DCMk.Timer
    else
      if (DCMk.Capcom_Opposite) then
        DCMk.Capcom_Value = DCMk.Timer
      endif
    endif
    if (DCMk.Clear_On_Rising_Edge) then
      DCMk.Timer = 0
    else DCMk.Timer ++
    endif
    if (DCMk.Clock_On_Rising_Edge) then
      Generate pulse on DCMk.Signal_Output
    endif
  else    //falling edge
    trig(DCMk.Service_Request_Falling)
    if (!DCMk.Capture_On_Rising_Edge) then
      DCMk.Capture_Value = DCMk.Timer
    else
      if (DCMk.Capcom_Opposite) then
        DCMk.Capcom_Value = DCMk.Timer
      endif
    endif
    if (DCMk.Clear_On_Falling_Edge) then
      DCMk.Timer = 0
    else DCMk.Timer ++
    endif
    if (DCMk.Clock_On_Falling_Edge) then
      Generate pulse on DCMk.Signal_Output
    endif
  endif
else DCMk.Timer ++
endif
```

Variables

Input, Local, Output variables of the cell (I, L, O)

Name k = [0 to 3] for DCM	Short Name	Used (ILO)	Comment
DCMk.Signal_Input.Transition DCMk.Signal_Input.Level	*SITk *SILk	I	Input of the cell
DCMk.Signal_Output	*SOk	O	Output of the cell
DCMk.Service_Request_Rising	*RTQk	O	Service request on rising edge
DCMk.Service_Request_Falling	*FTQk	O	Service request on falling edge
DCMk.Service_Request_Compare	*CTQk	O	Service request on compare event

Global variables

Name k = [0 to 3] for DCM	Short Name (*)DCM	Size (bits)	Function
DCMk.Capture_On_Rising_Edge	*RCAk	1	Capture into Capture_Value on rising edge
DCMk.Capcom_Opposite	*OCAk	1	Capture into Capcom_Value on opposite edge defined by RCAk
DCMk.Clear_On_Rising_Edge	*RZEk	1	Clear Timer on rising edge
DCMk.Clear_On_Falling_Edge	*FZEk	1	Clear Timer on falling edge
DCMk.Clock_On_Rising_Edge	*RCKk	1	Generate a single clock pulse on rising edge
DCMk.Clock_On_Falling_Edge	*FCKk	1	Generate a single clock pulse on falling edge
DCMk.Clock_Request	*QCKk	1	Generate a single clock pulse immediately
DCMk.Request_Enable_Rising	*RREk	1	Enable request on rising edge
DCMk.Request_Enable_Falling	*FREk	1	Enable request on falling edge
DCMk.Request_Enable_Compare	*CREk	1	Request enable on compare
DCMk.Timer	*TIMk	24	Timer value
DCMk.Capture_Value	*CAVk	24	Capture value
DCMk.Capcom_Value	*COVk	24	Capture/compare value

28.3.6.4 PLL-Algorithm

PLL_Control_Logic() “to be performed every GPTA®v5 clock”

```
if ( (Pll.Automatic_End) and (Pll.Event) ) then    //allow compensation
  Pll.Perform_End = 1
endif

if ( (Pll.Counter_Mtick == 0) and ((Pll.Perform_End) or (!Pll.Automatic_End)) )
then    //compensation finished or no automatic compensation
  Pll.Counter_Mtick = Pll.Number_Mtick
  Pll.Perfom_End = 0
endif

if ( (Pll.Counter_Mtick != 0) and ((Pll.Perform_End) or (Bit 24 of Pll.Delta)) )
then    //output pulse is necessary
  generate pulse on Pll.Signal_Output
  Pll.Counter_Mtick --
  if (Pll.Counter_Mtick == 0) then
    trig(Pll.Service_Request_Trigger)
  endif
endif

if (Bit 24 of Pll.Delta) then    //delta is < 0
  Pll.Delta = Pll.Delta + Pll.Reload_Value
  generate pulse on Pll.Signal_Uncomp
else    //delta is >= 0
  Pll.Delta = Pll.Delta + (0xFFFF0000 or (Pll.Step))
endif
```

Variables

Input, Local, Output variables of the cell (I, L, O)

Name k = [0 to 3] for DCM	Short Name (*)PLL	Used (ILO)	Comment
DCMk.Signal_Output	SOk	I	Input of the cell from DCM
Pll.Event	*EVE	L	Input selected by the multiplexer
Pll.Signal_Output	*SO	O	Output of the cell
Pll.Signal_Uncomp	*SU	O	Uncompensated output of the cell
Pll.Service_Request_Trigger	*SQT	O	Service request when Counter reaches zero

Global variables

Name	Short Name (*)PLL	Size (bits)	Function
Pll.Mux	*MUX	2	Selects the signal input for PLL
Pll.Automatic_End	*AEN	1	Performs the acceleration/ deceleration correction
Pll.Perform_End	*PEN	1	Makes it possible to decrement the Counter at full speed
Pll.Request_Enable	*REN	1	Allows a request when microtick counter reaches zero
Pll.Number_Mtick	*MTI	16	Number of microticks per input signal period
Pll.Counter_Mtick	*CNT	16	Microtick counter
Pll.Step	*STP	16	Step value, to be added to positive/zero delta register
Pll.Reload_Value	*REV	24	Reload value, to be added to negative delta register
Pll.Delta	*DTR	25	Delta register

28.3.6.5 GT-Algorithm

GTm_Control_Logic() “to be performed every GPTA®v5 clock”

```
if (GTm.Run) then
  if (Event on GTm.Clock_In[p] selected by GTm.Clock_Mux) then
    GTm.Timer ++
    if (Overflow of GTm.Timer) then
      GTm.Timer = GTm.Reload_Value
      trig(GTm.Service_Request_Trigger)
    endif
  endif
endif
```

Variables

Input, Local, Output variables of the cell (I, L, O)

Name m = [0, 1] for GT p = [0 to 7] for Clock Bus	Short Name (*)GT	Used (ILO)	Comment
GTm.Clock_In[p]	*CINmp	I	Input coming from clock bus
GTm.Timer_Greater_Equal_Comp	TGEm	O	Timer is greater or equal
GTm.Timer_Event	TEVm	O	Signal for timer change
GTm.Service_Request_Trigger	*SQTm	O	Service request line

Global variables

Name m = [0, 1] for GT	Short Name (*)GT	Size (bits)	Function
GTm.Run	*RUNm	1	Enables timer
GTm.Scale_Compare	*SCOm	4	Selects compare flag
GTm.Clock_Mux	*MUXm	3	Selects clock from clock bus
GTm.Request_Enable	*RENm	1	Allows a request when timer overflows
GTm.Timer	*TIMm	24	Timer value
GTm.Reload_Value	*REVm	24	Reload value when timer overflows

28.3.6.6 GTC-Algorithm

GTCk_Control_Logic() “to be performed every GPTA®v5 clock”

```
if (GTCk.Cell_Enable) then
  switch (GTCk.Mode)
    case CAPTURE_T0:
      Capture(0)
      break
    case CAPTURE_T1:
      Capture(1)
      break
    case COMPARE_T0:
      Compare(0)
      break
    case COMPARE_T1:
      Compare(1)
  endswitch

  if ( (GTCk.One_Shot_Mode) and (GTCk.Event) ) then
    GTCk.Cell_Enable = 0
  endif
endif

Manage_Mux()
```

```
Capture(m)
```

```
if (GTCk.Signal_Input) then
  trig(GTCk.Service_Request_Trigger)
  GTCk.X = GTm.Timer
  GTCk.Event = 1
else
  GTCk.Event = 0
endif
Ck.Event = 0
```

Compare(m)

```
if ( ((GTCk.X == GTm.Timer) and ((GTCk.X_Write_Access) or (GTm.Timer_Event))) or
   ((GTCk.Greater_Equal_Select) and (GTCk.X_Write_Access)
   and (GTm.Timer_Greater_Equal_Comp)) ) then
   if (GTCk.Capture_After_Compare) then
      if (GTCk.Capture_Alternate_Timer) then
         GTCk.X = GT(!m).Timer
      else
         GTCk.X = GTm.Timer
      endif
   endif
   trig(GTCk.Service_Request_Trigger)
   GTCk.Event = 1
else
   GTCk.Event = 0
endif
```

Set_Data_Out(mode)

```
switch (mode)
   case 00B:    //no change
      break
   case 01B:    //toggle
      GTCk.Data_Out = !GTCk.Data_Out
      break
   case 10B:    //clear
      GTCk.Data_Out = 0
      break
   case 11B:    //set
      GTCk.Data_Out = 1
      break
endswitch
GTCk.Output_State = GTCk.Data_Out
```

Manage_Mux()

```
if ((GTCk.Event or GTCk.OIA) and GTCk.OCM != x00) then    //local event
  Set_Data_Out(GTCk.Output_Control_Mode.[1:0])
  if (!GTCk.Bypass) then    //no bypass
    GTCk.Output_Mode_Out = GTCk.Output_Control_Mode.[1:0]
  else
    if (GTCk.Output_Control_Mode.2) then    //bypass, input link enabled
      GTCk.Output_Mode_Out = GTCk.Output_Mode_In
    else    //bypass, input link disabled
      GTCk.Output_Mode_Out = 00B
    endif
  endif
else    //no local event
  if (GTCk.Output_Control_Mode.2) then    //input link enabled
    Set_Data_Out(GTCk.Output_Mode_In)
    GTCk.Output_Mode_Out = GTCk.Output_Mode_In
  else    //input link disabled
    Set_Data_Out(00B)
    GTCk.Output_Mode_Out = 00B
  endif
endif
if ( (GTCk.Enable_Of_Action) and
    ((GTCk.Output_Mode_In.1) or (GTCk.Output_Mode_In.0)) ) then
  GTCk.Cell_Enable = 1
  GTCk.Enable_Of_Action = 0
endif
```

Variables

Input, Local, Output variables of the cell (I, L, O)

Name k = [0 to 31] for GTC m = [0, 1] for GT	Short Name (*)GTC	Used (ILO)	Comment
GTm.Timer_Greater_Equal_Comp	TGEm	I	Timer is greater or equal
GTm.Timer_Event	TEVm	I	Signal for timer change
GTm.Timer	*TIMm	I	Timer value
GTCk.Data_In	*DINk	I	Data input from input multiplexer
GTCk.Output_Mode_In	*M1Ik *M0Ik	I	Link signals from preceding cell
GTCk.X_Write_Access	*XWA	L	Indicates that GTCk.X was modified
GTCk.Event	*EVE	L	Local event
GTCk.Signal_Input	*INS	L	Qualified input signal
GTCk.Service_Request_Trigger	*SQSk	O	Service request line
GTCk.Data_Out	*DOUk	O	Data output for output multiplexer
GTCk.Output_Mode_Out	*M1Ok *M0Ok	O	Link signals to following cell

Global variables

Name k = [0 to 31] for GTC	Short Name (*)GTC	Size (bits)	Comment
GTCk.Mode	*MODk	2	Operation mode: CAPTURE_T0, CAPTURE_T1, COMPARE_T0, COMPARE_T1
GTCk.One_Shot_Mode	*OSMk	1	One shot mode
GTCk.Request_Enable	*RENk	1	Allows a request on event
GTCk.Input_Rising_Edge_Select (Capture Mode)	*REDk	1	Selects rising edge of input pin
GTCk.Greater_Equal_Select (Compare Mode)	*GESk	1	Selects >= Compare Mode
GTCk.Input_Falling_Edge_Select (Capture Mode)	*FEDk	1	Selects falling edge of input pin
GTCk.Capture_After_Compare (Compare Mode)	*CACk	1	Selects capture after compare
GTCk.Capture_Alternate_Timer (Compare Mode)	*CATk	1	Capture alternate global timer after compare
GTCk.Bypass	*BYPk	1	Local events bypassed for output link
GTCk.Enable_Of_Action	*EOAk	1	Enables cell on action communicated via link
GTCk.Cell_Enable	*CENk	1	Cell enable state
GTCk.Output_Control_Mode	*OCMk	3	Output control mode
GTCk.Output_Immediate_Action	*OIAk	1	Forces immediate action
GTCk.Output_State	*OUTk	1	Read value of Data_Out
GTCk.X	*Xk	24	Capture/Compare value

28.3.6.7 LTC-Algorithm for Cells 0 to 62

LTCk_Control_Logic() “to be performed every GPTA®v5 clock”

```
if (LTCk.Cell_Enable) then
  switch (LTCk.Mode)
    case TIMER_FREE_RUN:
      LTCk.Reset_Timer_Bit = 0
      Timer()
      break
    case TIMER_RESET:
      if (LTCk.Event_In) then
        LTCk.Reset_Timer_Bit = 1
      endif
      Timer()
      break;
    case CAPTURE:
      Capture()
      break
    case COMPARE:
      Compare()
      break
  endswitch
  if ((LTCk.One_Shot_Mode) and (LTCk.Event)) then
    LTCk.Cell_Enable = 0
  endif
endif

Manage_Mux()
```

Timer()

```
if ( (LTCk.X == 0xFFFF) and (LTCk.X_Write_Access) ) then
  //above condition is also true for timer overflow or software reset
  trig(LTCk.Service_Request_Trigger)
  LTCk.Event = 1
else
  LTCk.Event = 0
endif
if (LTCk.Signal_Input) then
  if (LTCk.Reset_Timer_Bit) then    //timer must be reset
    LTCk.Reset_Timer_Bit = 0
    LTCk.X = 0xFFFF
    if (LTCk.Coherent_Update_Enable) then
      LTCk.Select_Line_Value = !LTCk.Select_Line_Value
      LTCk.Coherent_Update_Enable = 0
    endif
  else    //timer runs normally
    LTCk.X ++
  endif
endif
LTCk.Event_Out = LTCk.Event
```

Capture()

```
if (LTCk.Signal_Input) then
  trig(LTCk.Service_Request_Trigger)
  LTCk.X = LTCk.Y_In
  LTCk.Event = 1
else
  LTCk.Event = 0
endif
LTCk.Event_Out = LTCk.Event
```

Compare()

```
if ( ((LTCk.Select_In) and (LTCk.Select_On_High_Level)) or
  ((!LTCk.Select_In) and (LTCk.Select_On_Low_Level)) ) then    //cell is active
  if ( (LTCk.X == LTCk.Y_In) and
    ((LTCk.X_Write_Access) or (LTCk.Timer_Event_In)) ) then    //event
    trig(LTCk.Service_Request_Trigger)
    LTCk.Event = 1
  else
    LTCk.Event = 0
  endif
  LTCk.Event_Out = LTCk.Event
else    //cell is inactive
  LTCk.Event_Out = LTCk.Event_In
endif
```

Manage_Mux()

```
if ( (LTCk.Mode == TIMER_FREE_RUN) or (LTCk.Mode == TIMER_RESET) ) then
  LTCk.Y_Out = LTCk.X
  if (the timer has been modified) then    //increment, reset, software overwrite
    LTCk.Timer_Event_Out = 1
  else
    LTCk.Timer_Event_Out = 0
  endif
  LTCk.Select_Out = LTCk.Select_Line_Value
else    //capture mode or compare mode
  LTCk.Y_Out = LTCk.Y_In
  LTCk.Timer_Event_Out = LTCk.Timer_Event_In
  LTCk.Select_Line_Value = LTCk.Select_In
  LTCk.Select_Out = LTCk.Select_In
endif
if (LTCk.Event) then    //local event
  Set_Data_Out(LTCk.Output_Control_Mode.[1:0])
  if (!LTCk.Bypass) then    //no bypass
    LTCk.Output_Mode_Out = LTCk.Output_Control_Mode.[1:0]
  endif
else    //no local event
  if (LTCk.Output_Control_Mode.2)    //input link enabled
    Set_Data_Out(LTCk.Output_Mode_In)
    if (!LTCk.Bypass) then    //no bypass
      LTCk.Output_Mode_Out = LTCk.Output_Mode_In
    endif
  else    //input link disabled
    Set_Data_Out(00B)
    if (!LTCk.Bypass) then    //no bypass
      LTCk.Output_Mode_Out = 00B
    endif
  endif
endif
```

Manage_Mux() - continued

```
if (LTCk.GlobalBypass) then    //global bypass
  LTCk.Output_Mode_Alternate_Out = LTCk.Output_Mode_Alternate_In
  if (LTCk.Bypass) then    // bypass
    LTCk.Output_Mode_Out = LTCk.Output_Mode_Alternate_In
  endif
else
  if (LTCk.Output_Control_Mode.2) then    //bypass, input link enabled
    LTCk.Output_Mode_Alternate_Out = LTCk.Output_Mode_In
    if (LTCk.Bypass) then    // bypass
      LTCk.Output_Mode_Out = LTCk.Output_Mode_In
    endif
  else    //bypass, input link disabled
    LTCk.Output_Mode_Alternate_Out = 00B
    if (LTCk.Bypass) then    // bypass
      LTCk.Output_Mode_Out = 00B
    endif
  endif
endif
if ( (LTCk.Enable_Of_Action) and
   ((LTCk.Output_Mode_In.1) or (LTCk.Output_Mode_In.0)) ) then    //enable condition
  LTCk.Cell_Enable = 1
  LTCk.Enable_Of_Action = 0
endif
```

Set_Data_Out(mode)

```
switch (mode)
  case 00B:    //no change
    break
  case 01B:    //toggle
    LTCk.Data_Out = !LTCk.Data_Out
    break
  case 10B:    //clear
    LTCk.Data_Out = 0
    break
  case 11B:    //set
    LTCk.Data_Out = 1
    break
endswitch
LTCk.Output_State = LTCk.Data_Out
```

Variables

Input, Local, Output variables of the cell (I, L, O)

Name	Short Name (*)LTC	Used (ILO)	Comment
LTCk.Data_In	*DINkp	I	Data input from input multiplexer
LTCk.Y_In	*YIk	I	Timer coming from preceding cell
LTCk.Output_Mode_In	*M1Ik *M0Ik	I	Link signals coming from preceding cell
LTCk.Output_Mode_Alternate_In	*M3Ik *M2Ik	I	Alternative Link signals coming from preceding cell
LTCk.Timer_Event_In	*TIk	I	Signal for timer change from preceding cell
LTCk.Event_In	*EIk	I	Signal for event from following cell
LTCk.Select_In	*SI	I	Select signal from preceding cell
LTCk.X_Write_Access	*XWA	L	Indicates that LTCk.X was modified
LTCk.Select_Line_Value	*SLV	L	Internal value for select line reset value: 0
LTCk.Signal_Input	*INS	L	Qualified input signal for Timer Mode and Capture Mode
LTCk.Reset_Timer_Bit	*RTM	L	Flip-flop to reset timer on next clock
LTCk.Event	*EVE	L	Local event
LTCk.Data_Out	*DOUk	O	Data output for output multiplexer
LTCk.Service_Request_Trigger	*SQTk	O	Service request line
LTCk.Y_Out	*YOk	O	Timer going to following cell
LTCk.Output_Mode_Out	*M1Ok *M0Ok	O	Link signals to following cell
LTCk.Output_Mode_Alternate_Out	*M3Ok *M2Ok	O	Link signals to following cell
LTCk.Timer_Event_Out	*TOk	O	Event output to following cell
LTCk.Select_Out	*SO	O	Select output to following cell
LTCk.Event_Out	*EOk	O	Event output to preceding cell

Global variables

Name k = [0 to 62] for LTC	Short Name (*)LTC	Size (bits)	Comment
LTCk.Mode	*MODk	2	Operation mode: TIMER, TIMER_RESET, CAPTURE, COMPARE
LTCk.One_Shot_Mode	*OSMk	1	One shot mode
LTCk.Request_Enable	*RENk	1	Allows a request on event
LTCk.Input_Rising_Edge_Select (Timer Mode, Capture Mode) LTCk.Select_On_Low_Level (Compare Mode)	*REDk *SOLk	1 1	Selects rising edge of input pin Enables compare on low level of select line
LTCk.Input_Falling_Edge_Select (Timer Mode, Capture Mode) LTCk.Select_On_High_Level (Compare Mode)	*FEDk *SOHk	1 1	Selects falling edge of input pin Enables compare on high level of select line
LTCk.Bypass (Capture Mode, Compare Mode)	*BYPk	1	Local events bypassed for output link
LTCk.GlobalBypass	*GBYPk	1	Alternative output links forwarded to alternative output link
LTCk.Enable_Of_Action (Capture Mode, Compare Mode)	*EOAk	1	Enables cell on action communicated via link
LTCk.Input_Line_Mode	*ILMk	1	Selects edge input line mode
LTCk.Coherent_Update_Enable (Timer Mode) LTCk.Select_Line_Level (Capture Mode, Compare Mode)	*CUDk *SLLk	1 1	Selects coherent update Select line level
LTCk.Cell_Enable	*CENk	1	Cell enable state
LTCk.Output_Control_Mode	*OCMk	3	Output control mode
LTCk.Output_Immediate_Action	*OIAk	1	Forces immediate action
LTCk.Output_State	*OUTk	1	Read value of Data_Out
LTCk.X	*Xk	16	Timer/Capture/Compare value

28.3.6.8 LTC Algorithm for Cell 63

LTC63_Control_Logic() “to be performed every GPTA®v5 clock”

```
Copy()
Compare()
```

Copy()

```
if (LTC63.Cell_Enable) then
  if (LTC63.Signal_Input) then
    LTC63.X = LTC63.X_Shadow
    trig(LTC63.Service_Request_Trigger)
    if (LTC63.One_Shot_Mode) then
      LTC63.Cell_Enable = 0
    endif
  endif
endif
```

Compare()

```
if ( (LTC63.X_Write_Access) or (LTC63.Timer_Event_In) ) then
  if (LTC63.Bit_Rev_Mode) then
    LTC63.Y_Comp = LTC63.Y_Rev
  else
    LTC63.Y_Comp = LTC63.Y_In
  endif
  if ( (LTC63.X > LTC63.Y_Comp) or (LTC63.X == FFFFH) ) then    //output must be 1
    LTC63.Data_Out = 1
    LTC63.Event_Out = 0
  else    //output must be 0
    if (LTC63.Data_Out == 1) then    //falling edge on output
      trig(LTC63.Service_Request_Trigger)
      LTC63.Event_Out = 1
    else
      LTC63.Event_Out = 0
    endif
    LTC63.Data_Out = 0
  endif
  LTC63.Output_State = LTC63.Data_Out
endif
```

Variables

Input, Local, Output variables of the cell (I, L, O)

Name	Short Name (*)LTC	Used (ILO)	Comment
LTC63.Data_In	*DIN63	I	Data input from input multiplexer
LTC63.Y_In	*YI63	I	Timer coming from preceding cell
LTC63.Timer_Event_In	*TI63	I	Signal for timer change from preceding cell
LTC63.Y_Rev	*YR	L	Timer coming from preceding cell, bit reversed
LTC63.Y_Comp	*YC	L	Timer actually used for compare
LTC63.X_Write_Access	*XWA	L	Indicates that LTC63.X was modified
LTC63.Signal_Input	*INS	L	Qualified input signal
LTC63.Data_Out	*DOU63	O	Data output for output multiplexer
LTC63.Service_Request_Trigger	*SQT63	O	Service request line
LTC63.Event_Out	*EO63	O	Event output to preceding cell

Global variables

Name	Short Name (*)LTC	Size (bits)	Comment
LTC63.Bit_Rev_Mode	*BRM63	1	Bit reverse mode
LTC63.One_Shot_Mode	*OSM63	1	One shot mode for copy
LTC63.Request_Enable	*REN63	2	Allows a request on compare or copy
LTC63.Input_Rising_Edge_Select	*RED63	1	Selects rising edge of input pin
LTC63.Input_Falling_Edge_Select	*FED63	1	Selects falling edge of input pin
LTC63.Input_Line_Mode	*ILM63	1	Selects edge input line mode
LTC63.Cell_Enable	*CEN63	1	Cell enable state for copy
LTC63.Output_State	*OUT63	1	Read value of Data_Out
LTC63.X	*X63	16	Compare value
LTC63.X_Shadow	*XS63	16	Shadow compare value

28.3.7 Programming of a GPTA®v5 Unit

A hierarchical top-down design approach may be used to implement a complex signal processing circuitry as follows:

- Partitioning the complex signal processing circuitry into simple function cells.
- Implementing each simple function cell by configuring the LTC and/or GTC cells which can be tied together for realizing a common signal operation.
- Implementing necessary signal pre-processing tasks by configuring the FPC, PDL, DCM and PLL cells accordingly.
- Defining and configuring all input/output port pins required as clock source, trigger input or signal output.

Table 28-17 summarizes all of the software tasks to be implemented for getting a GPTA®v5 unit into operation.

Table 28-17 Software Tasks Controlling a GPTA®v5 Unit

GPTA®v5 Shell Initialization	
GPTA®v5 Module Clock Enable	
Fractional Divider Setting	
Unit Enable	
Configuration of Interrupt Handling	
GPTA®v5 Kernel Initialization	
FPC:	**PDL:**
Selection of Operating Mode (Prescaler, Filter or Feed-Through)	Selection of Operating Mode (Phase Discriminator or Feed-Through)
Input Channel Selection	2- or 3-Sensor Mode Selection
Clock Selection	**PLL:**
Configuration of Prescaler Factor or Debounce Mode	Selection of Input Channel
DCM:	Estimation of Input Signal Period Width
Selection of Reset Event for Timer	Configuration of Output Signal Frequency
Selection of Trigger Source for Capture Event	Handling of Input Signal Period Length Variation
Selection of Trigger Source for Capture Compare Register Update	Interrupt Request Enable on End of Output Pulse Generation
Interrupt Request Enable on Input Edge or Compare Event	

Table 28-17 Software Tasks Controlling a GPTA®v5 Unit (cont'd)

Clock Bus Setup	
Selection and Configuration of 8 Clock Sources for GT, GTC and LTC Cells	
GT:	**GTC:**
Selection of Timer Clock Source	Selection of Operating Mode (Capture or Compare) and Time Base (GT0 or GT1)
Configuration of Timer Width (Reload Value, TGE Flag)	Configuration of Trigger Events for Capture Mode or Selection of a Relational Operator for Compare Mode
Interrupt Request Enable on Timer Overflow	Interrupt Request Enable on Capture or Compare Event
Start Global Timer(s)	Configuration of Data Output triggered by a GTC Event
LTC:	**IOLS:**
Selection of Operating Mode (Timer, Capture or Compare)	Configuration of the Multiplexer Array to link GTC and LTC data outputs/inputs to external Port Pins or other cells by writing the Multiplexer Register Array FIFO Configuration of the On-chip Trigger and Gating Signal Multiplexer Array to link GTC and LTC data outputs to on-chip modules by writing the Multiplexer Register Array FIFO
Selection of Trigger Source for Timer, Capture or Compare Mode	Configuration of Port Output Source
Configuration of Trigger Event for Timer, Capture or Compare Mode	
Interrupt Request Enable on Timer, Capture or Compare Event	
Configuration of Data Output triggered by an LTC Event	
Port Initialization	
Definition of Electrical Port Characteristic	
Configuration of Port Pin Direction (Input or Output)	

28.4 GPTA0/1 Kernel Registers

This section describes the kernel registers of the GPTA0 and GPTA1 unit.

GPTA0/1 Kernel Register Overview

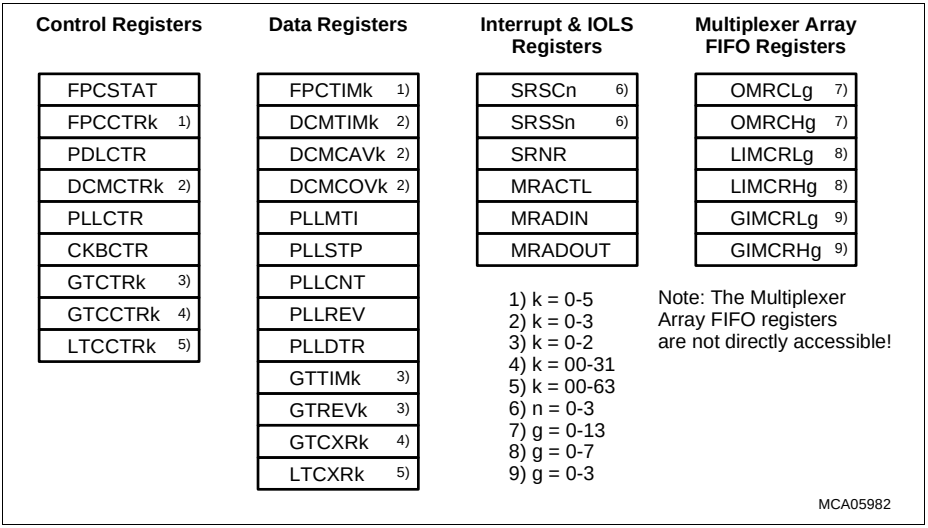


Figure 28-80 GPTA0 and GPTA1 Kernel Registers

In the TC1798, the registers of the GPTA®v5 units are located in the following address ranges.

Table 28-18 Registers Address Space

Module	Base Address	End Address	Note
GPTA0	F000 1800_H	F000 $1FFF_H$	-
GPTA1	F000 2000_H	F000 $27FF_H$	-
LTCA2	F000 2800_H	F000 $2FFF_H$	-

Table 28-19 Registers Overview - GPTA0 and GPTA1 Kernel Registers

Register Short Name	Register Long Name	Offset Addr.[1]	Access Mode		Reset Class	Description see
			Read	Write		
GPTA0_CLC[2]	GPTA Clock Control Register	0000_H	U, SV	SV, E	3	Page 28-300
GPTA0_DBGCTR[2]	GPTA Debug Clock Control Register	0004_H	U, SV	U, SV	3	Page 28-305
ID	GPTA Identification Register	0008_H	U, SV	nBE	3	Page 28-166
GPTA0_FDR[2]	GPTA Fractional Divider Register	$000C_H$	U, SV	SV, E	3	Page 28-301
SRSC0	Service Request State Clear Register 0	010_H	U, SV	U, SV	3	Page 28-223
SRSS0	Service Request State Set Register 0	014_H	U, SV	U, SV	3	Page 28-225
SRSC1	Service Request State Clear Register 1	018_H	U, SV	U, SV	3	Page 28-226
SRSS1	Service Request State Set Register 1	$01C_H$	U, SV	U, SV	3	Page 28-227
SRSC2	Service Request State Clear Register 2	020_H	U, SV	U, SV	3	Page 28-228
SRSS2	Service Request State Set Register 2	024_H	U, SV	U, SV	3	Page 28-229
SRSC3	Service Request State Clear Register 3	028_H	U, SV	U, SV	3	Page 28-230
SRSS3	Service Request State Set Register 3	$02C_H$	U, SV	U, SV	3	Page 28-231
SRNR	Service Request Node Redirection Register	030_H	U, SV	U, SV	3	Page 28-232
MRACTL	Multiplexer Register Array Control Register	0038_H	U, SV	U, SV	3	Page 28-207
MRADIN	Multiplexer Register Array Data In Register	$003C_H$	U, SV, 32	U, SV, 32	3	Page 28-208
MRADOUT	Multiplexer Register Array Data Out Register	0040_H	U, SV, 32	U, SV, 32	3	Page 28-209

Table 28-19 Registers Overview - GPTA0 and GPTA1 Kernel Registers (cont'd)

Register Short Name	Register Long Name	Offset Addr.[1)]	Access Mode		Reset Class	Description see
			Read	Write		
FPCSTAT	Filter and Prescaler Cell Status Register	0044_H	U, SV	U, SV	3	Page 28-167
FPCCTRk	Filter and Prescaler Cell Control Register k (k = 0-5)	$0048_H + k \times 8$	U, SV	U, SV	3	Page 28-168
FPCTIMk	Filter and Prescaler Cell Timer Register k (k = 0-5)	$004C_H + k \times 8$	U, SV	U, SV	3	Page 28-170
PDLCTR	Phase Discrimination Logic Control Register	0078_H	U, SV	U, SV	3	Page 28-171
DCMCTRk	Duty Cycle Measurement Control Register k (k = 0-3)	$0080_H + k \times 16$	U, SV	U, SV	3	Page 28-173
DCMTIMk	Duty Cycle Measurement Timer Register k (k = 0-3)	$0084_H + k \times 16$	U, SV	U, SV	3	Page 28-175
DCMCAVk	Duty Cycle Measurement Capture Register k (k = 0-3)	$0088_H + k \times 16$	U, SV	U, SV	3	Page 28-175
DCMCOVk	Duty Cycle Measurement Capture/Compare Register k (k = 0-3)	$008C_H + k \times 16$	U, SV	U, SV	3	Page 28-176
PLLCTR	Phase Locked Loop Control Register	$00C0_H$	U, SV	U, SV	3	Page 28-177
PLLMTI	Phase Locked Loop Micro Tick Register	$00C4_H$	U, SV	U, SV	3	Page 28-178
PLLCNT	Phase Locked Loop Counter Register	$00C8_H$	U, SV	U, SV	3	Page 28-179
PLLSTP	Phase Locked Loop Step Register	$00CC_H$	U, SV	U, SV	3	Page 28-179
PLLREV	Phase Locked Loop Reload Register	$00D0_H$	U, SV	U, SV	3	Page 28-180

Table 28-19 Registers Overview - GPTA0 and GPTA1 Kernel Registers (cont'd)

Register Short Name	Register Long Name	Offset Addr.[1]	Access Mode		Reset Class	Description see
			Read	Write		
PLLDTR	Phase Locked Loop Delta Register	$00D4_H$	U, SV	U, SV	3	Page 28-181
CKBCTR	Clock Bus Control Register	$00D8_H$	U, SV	U, SV	3	Page 28-185
GTCTRk	Global Timer Control Register k (k = 0, 1)	$00E0_H + k \times 16$	U, SV	U, SV	3	Page 28-182
GTREVk	Global Timer Reload Value Register k (k = 0, 1)	$00E4_H + k \times 16$	U, SV	U, SV	3	Page 28-184
GTTIMk	Global Timer Register k (k = 0, 1)	$00E8_H + k \times 16$	U, SV	U, SV	3	Page 28-183
GTCCTRk	Global Timer Cell Control Register k (k = 00-31)	$0100_H + k \times 8$	U, SV	U, SV	3	Page 28-187 Page 28-189
GTCXRk	Global Timer Cell X Register k (k = 00-31)	$0104_H + k \times 8$	U, SV	U, SV	3	Page 28-191
LTCCTRk	Local Timer Cell Control Register k (k = 00-62)	$0200_H + k \times 8$	U, SV	U, SV	3	Page 28-192 Page 28-198 Page 28-201
LTCXRk	Local Timer Cell X Register k (k = 00-62)	$0204_H + k \times 8$	U, SV	U, SV	3	Page 28-205
LTCCTR63	Local Timer Cell Control Register 63	$03F8_H$	U, SV	U, SV	3	Page 28-204
LTCXR63	Local Timer Cell X Register 63	$03FC_H$	U, SV	U, SV	3	Page 28-206
GPTA0_EDCTR[2]	GPTA Clock Enable/Disable Control Register	0400_H	U, SV	U, SV	3	Page 28-303

Table 28-19 Registers Overview - GPTA0 and GPTA1 Kernel Registers (cont'd)

Register Short Name	Register Long Name	Offset Addr.[1]	Access Mode		Reset Class	Description see
			Read	Write		
OTMCRg	On-Chip Trigger and Gating Signal Multiplexer Control Register of Group g (g = 0-1)	not directly address -able; see Page 28 -121	n.a.	n.a.	3	Page 28-214
OMCRLg	Output Multiplexer Control Register for Lower Half of Group g (g = 0-13)		n.a.	n.a.	3	Page 28-210
OMCRHg	Output Multiplexer Control Register for Upper Half of Group g (g = 0-13)		n.a.	n.a.	3	Page 28-212
GIMCRLg	Input Multiplexer Control Register for Lower Half of GTC Group g (g = 0-3)		n.a.	n.a.	3	Page 28-215
GIMCRHg	Input Multiplexer Control Register for Lower Half of GTC Group g (g = 0-3)		n.a.	n.a.	3	Page 28-217
LIMCRLg	Input Multiplexer Control Register for Upper Half of LTC Group g (g = 0-7)	not directly address -able; see Page 28 -121	n.a.	n.a.	3	Page 28-219
LIMCRLg	Input Multiplexer Control Register for Upper Half of LTC Group g (g = 0-7)		n.a.	n.a.	3	Page 28-221

1) The absolute register address is calculated as follows:
Unit Base Address + Offset Address (shown in this column)

2) Only implemented in GPTA0 kernel.

Bit Protection

Bits with bit protection (this is valid, for example, for all bits in the Service Request State Registers) are not changed during a read-modify-write instruction, for example when

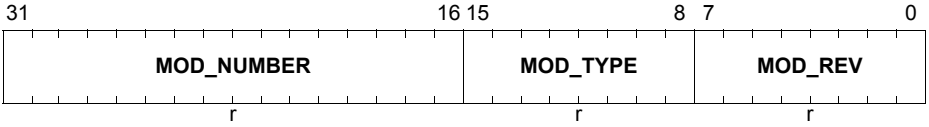
hardware sets a request state bit between the read and the write of the read-modify-write sequence. For bit protected bits it is guaranteed that a hardware setting operation always has priority. Thus, no hardware triggered events are lost.

Bits with bit protection are marked in the corresponding bit descriptions.

28.4.1 GPTA®v5 Identification Register

The GPTA®v5 Identification Register ID contains read-only information about the module version.

GPTA0_ID
GPTA0 Identification Register **(08_H)** **Reset Value: 0029 C0XX$_H$**
GPTA1_ID
GPTA1 Identification Register **(08_H)** **Reset Value: 0029 C0XX$_H$**
LTCA2_ID
LTCA2 Identification Register **(08_H)** **Reset Value: 002A C0XX$_H$**



Field	Bits	Type	Description
MOD_REV	[7:0]	r	**Module Revision Number** MOD_REV defines the Module revision number. The value of a module revision starts with 01_H (first revision). GPTAv5 will start with module revision 05_H.
MOD_TYPE	[15:8]	r	**Module Number Value** This bit field defines the module as a 32 bit module: $C0_H$
MOD_NUM	[31:16]	r	**Module Number Value** This bit field defines the identification number for the GPTA: 0029_H and LTCA: $002A_H$

28.4.2 FPC Registers

GPTA0_FPCSTAT
GPTA0 Filter and Prescaler Cell Status Register
(044_H) **Reset Value: 0000 0000$_H$**

GPTA1_FPCSTAT
GPTA1 Filter and Prescaler Cell Status Register
(044_H) **Reset Value: 0000 0000$_H$**

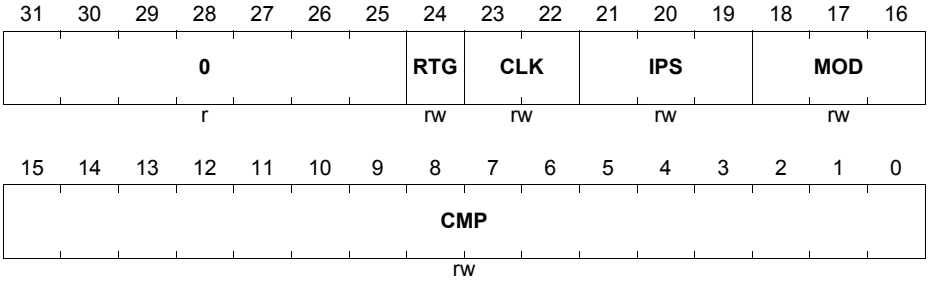
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0		FEG 5	FEG 4	FEG 3	FEG 2	FEG 1	FEG 0	0		REG 5	REG 4	REG 3	REG 2	REG 1	REG 0
r		rwh	rwh	rwh	rwh	rwh	rwh	r		rwh	rwh	rwh	rwh	rwh	rwh

Field	Bits	Type	Description
REGk (k = 0-5)	k	rwh	**Rising Edge Glitch Flag for FPCk** 0_B No rising edge of glitch detected during filtering 1_B Rising edge of glitch detected during filtering Bits REGk are bit protected (see **Section 28.4.2**).
FEGk (k = 0-5)	k+8	rwh	**Falling Edge Glitch Flag for FPCk** 0_B No falling edge of glitch detected during filtering 1_B Falling edge of glitch detected during filtering Bits FEGk are bit protected (see **Section 28.4.2**).
0	[7:6], [31:14]	r	**Reserved** Read as 0; should be written with 0.

GPTA0_FPCCTRk (k = 0-5)
GPTA0 Filter and Prescaler Cell Control Register k
(048_H+k*8_H) **Reset Value: 0000 0000_H**

GPTA1_FPCCTRk (k = 0-5)
GPTA1 Filter and Prescaler Cell Control Register k
(048_H+k*8_H) **Reset Value: 0000 0000_H**

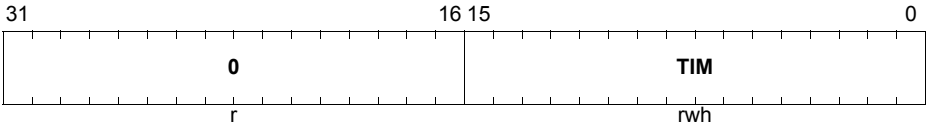


Field	Bits	Type	Description
CMP	[15:0]	rw	**Threshold Value of Filter and Prescaler Cell k** CMP is the 16-bit threshold value that is compared with the 16-bit timer value FPCTIMk.TIM.
MOD	[18:16]	rw	**Operation Mode Selection for FPCk** 000_B Delayed Debounce Filter Mode on both edges 001_B Immediate Debounce Filter Mode on both edges 010_B Rising edge: Immediate Debounce Filter Mode, falling edge: no filtering 011_B Rising edge: no filtering, falling edge: Immediate Debounce Filter Mode 100_B Rising edge: Delayed Debounce Filter Mode, falling edge: Immediate Debounce Filter Mode 101_B Rising edge: Immediate Debounce Filter Mode, falling edge: Delayed Debounce Filter Mode 110_B Prescaler Mode (triggered on rising edge) 111_B Prescaler Mode (triggered on falling edge)

Field	Bits	Type	Description
IPS	[21:19]	rw	**Input Line Selection for FPCk** IPS determines the signal input used for edge detection. 000_B Signal input SINk0 selected 001_B Signal input SINk1 selected 010_B Signal input SINk2 selected 011_B Signal input SINk3 selected 100_B Signal input SINk4 = GPTA®v5 module clock f_{GPTA} selected 101_B Signal input SINk5 = preceding FPC output SOLk-1 selected; SIN05 is connected to SOL5 $11X_B$ Reserved
CLK	[23:22]	rw	**Clock Selection for FPCk** CLK selects the clock signal used for edge detection. 00_B Clock input line 0 selected (GPTA®v5 module clock f_{GPTA}) 01_B Clock bus line 1 selected (local PLL clock) 10_B Clock bus line 2 selected (prescaled) GPTA®v5 module clock f_{GPTA} or PLL clock from other unit or DCM 3 clock 11_B Clock bus line 3 selected DCM 2 clock or PLL clock of other unit or uncompensated PLL clock or uncompensated PLL clock of other unit
RTG	24	rw	**Reset Timer for FPCk on Glitch** 0_B Timer for FPCk is decremented on glitch 1_B Timer for FPCk is cleared on glitch This bit is effective in Delayed Debounce Filter Mode only.
0	[31:25]	r	**Reserved** Read as 0; should be written with 0.

GPTA0_FPCTIMk (k = 0-5)
GPTA0 Filter and Prescaler Cell Timer Register k
(048_H+k*8_H+4_H) **Reset Value: 0000 0000_H**

GPTA1_FPCTIMk (k = 0-5)
GPTA1 Filter and Prescaler Cell Timer Register k
(048_H+k*8_H+4_H) **Reset Value: 0000 0000_H**

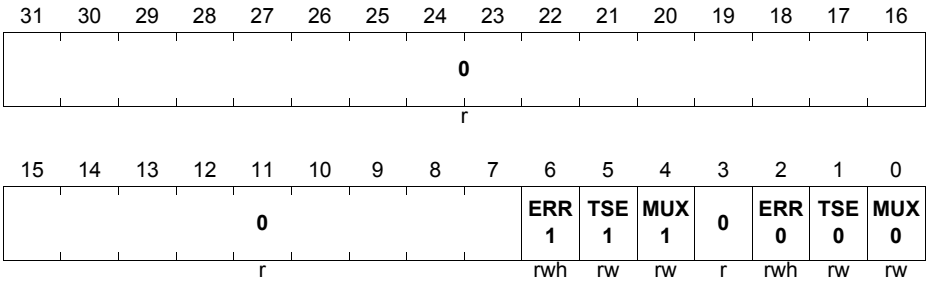


Field	Bits	Type	Description
TIM	[15:0]	rwh	**Timer Value of Filter and Prescaler Cell k**
0	[31:16]	r	**Reserved** Read as 0; should be written with 0.

28.4.3 Phase Discriminator Registers

GPTA0_PDLCTR
GPTA0 Phase Discrimination Logic Control Register
(078$_H$) **Reset Value: 0000 0000$_H$**

GPTA1_PDLCTR
GPTA1 Phase Discrimination Logic Control Register
(078$_H$) **Reset Value: 0000 0000$_H$**



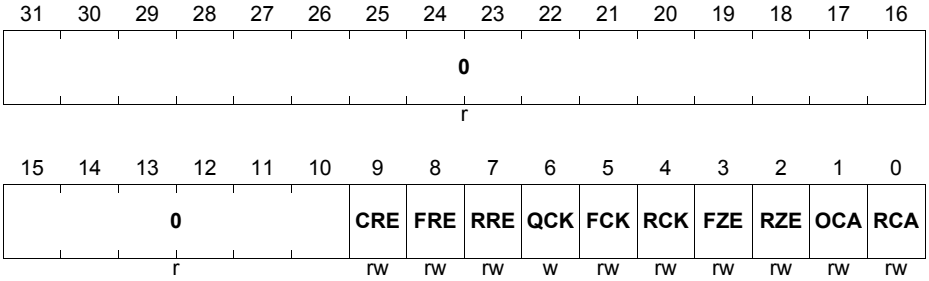
Field	Bits	Type	Description
MUX0	0	rw	**Output Signal Source Selection for PDL0** 0_B DCM0 cell input is driven by fed-through FPC0 output lines 1_B DCM0 cell input is provided with PDL0 “Forward” and “Backward” pulses
TSE0	1	rw	**3-Sensor Mode Enable for PDL0** 0_B PDL0 operates in “2-Sensor Mode” and DCM1 cell input is driven by fed-through FPC2 output lines 1_B PDL0 operates in “3-Sensor Mode” and DCM1 cell input is provided with PDL0 error information
ERR0	2	rwh	**Error Flag for PDL0** 0_B No error has occurred 1_B Error detected in “3-Sensor Mode”: all PDL0 input signals are simultaneously provided with high or low level Bit ERR0 is bit protected (see **Page 28-167**).
MUX1	4	rw	**Output Signal Source Selection for PDL1** 0_B DCM2 cell input is driven by fed-through FPC3 output lines 1_B DCM2 cell input is provided with PDL1 “Forward” and “Backward” pulses

Field	Bits	Type	Description
TSE1	5	rw	**3-Sensor Mode Enable for PDL1** 0_B PDL1 operates in “2-Sensor Mode” and DCM3 cell input is driven by fed-through FPC5 output lines 1_B PDL1 operates in “3-Sensor Mode” and DCM3 cell input is provided with PDL1 error information
ERR1	6	rwh	**Error Flag for PDL1** 0_B No error has occurred 1_B Error detected in “3-Sensor Mode”: all PDL1 input signals are simultaneously provided with high or low level Bit ERR1 is bit protected (see **Page 28-167**).
0	3, [31:7]	r	**Reserved** Read as 0; should be written with 0.

28.4.4 Duty Cycle Measurement Registers

GPTA0_DCMCTRk (k = 0-3)
GPTA0 Duty Cycle Measurement Control Register k
(080_H+k*10_H) **Reset Value: 0000 0000_H**

GPTA1_DCMCTRk (k = 0-3)
GPTA1 Duty Cycle Measurement Control Register k
(080_H+k*10_H) **Reset Value: 0000 0000_H**

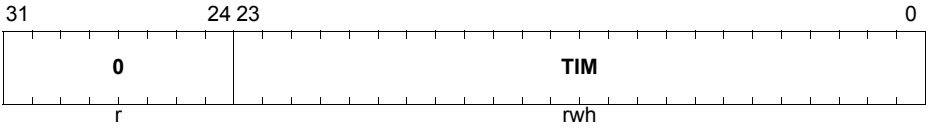


Field	Bits	Type	Description
RCA	0	rw	**Trigger Source Selection for Capture Event** 0_B Timer contents are copied to DCMCAVk capture register on a falling input signal edge 1_B Timer contents are copied to capture register on a rising input signal edge
OCA	1	rw	**Trigger Source for Capture/Compare Register Update** 0_B Capture/Compare register DCMCOVk is not affected. 1_B Timer contents are copied to DCMCOVk capture/compare register on the opposite edge selected by RCAk.
RZE	2	rw	**Timer Reset on Rising Edge** 0_B Timer is not affected 1_B Timer is reset on a rising input signal edge
FZE	3	rw	**Timer Reset on Falling Edge** 0_B Timer is not affected 1_B Timer is reset on a falling input signal edge
RCK	4	rw	**Output Pulse on Rising Edge** 0_B DCM output line is not affected 1_B DCM output line is provided with a single clock pulse generated on a rising input signal edge

Field	Bits	Type	Description
FCK	5	rw	**Output Pulse on Falling Edge** 0_B DCM output line is not affected 1_B DCM output line is provided with a single clock pulse generated on a falling input signal edge
QCK	6	w	**Additional Output Pulse Generation** 0_B DCM output line is not affected 1_B DCM output line is immediately provided with a single clock pulse QCK is always read as 0.
RRE	7	rw	**Interrupt Request on Rising Edge** 0_B Interrupt request is not affected 1_B Interrupt request is set on rising input signal edge
FRE	8	rw	**Interrupt Request on Falling Edge** 0_B Interrupt request is not affected 1_B Interrupt request is set on falling input signal edge
CRE	9	rw	**Interrupt Request on Compare Event** 0_B Interrupt request is not affected 1_B Interrupt request is set when the timer matches capture/compare register DCMCOVk
0	[31:10]	r	**Reserved** Read as 0; should be written with 0.

GPTA0_DCMTIMk (k = 0-3)
GPTA0 Duty Cycle Measurement Timer Register k
(080_H+k*10_H+4_H) **Reset Value: 0000 0000_H**

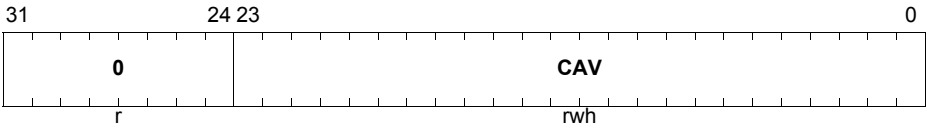
GPTA1_DCMTIMk (k = 0-3)
GPTA1 Duty Cycle Measurement Timer Register k
(080_H+k*10_H+4_H) **Reset Value: 0000 0000_H**



Field	Bits	Type	Description
TIM	[23:0]	rwh	**Timer Value of DCMk**
0	[31:24]	r	**Reserved** Read as 0; should be written with 0.

GPTA0_DCMCAVk (k = 0-3)
GPTA0 Duty Cycle Measurement Capture Register k
(088_H+k*10_H) **Reset Value: 0000 0000_H**

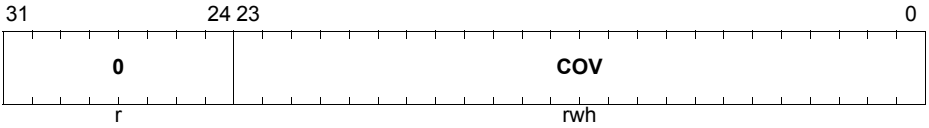
GPTA1_DCMCAVk (k = 0-3)
GPTA1 Duty Cycle Measurement Capture Register k
(088_H+k*10_H) **Reset Value: 0000 0000_H**



Field	Bits	Type	Description
CAV	[23:0]	rwh	**Capture Value of DCMk**
0	[31:24]	r	**Reserved** Read as 0; should be written with 0.

GPTA0_DCMCOVk (k = 0-3)
GPTA0 Duty Cycle Measurement Capture/Compare Register k
($08C_H$+k*10_H) **Reset Value: 0000 0000_H**

GPTA1_DCMCOVk (k = 0-3)
GPTA1 Duty Cycle Measurement Capture/Compare Register k
($08C_H$+k*10_H) **Reset Value: 0000 0000_H**

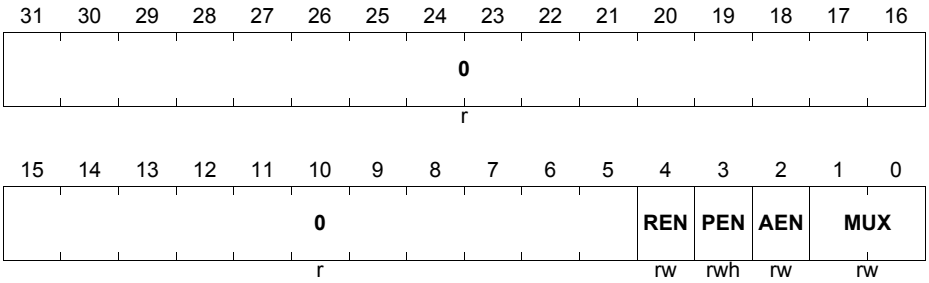


Field	Bits	Type	Description
COV	[23:0]	rwh	**Capture/Compare Register Value of DCMk**
0	[31:24]	r	**Reserved** Read as 0; should be written with 0.

28.4.5 Digital Phase Locked Loop Registers

GPTA0_PLLCTR
GPTA0 Phase Locked Loop Control Register
($0C0_H$) **Reset Value: $0000\ 0000_H$**

GPTA1_PLLCTR
GPTA1 Phase Locked Loop Control Register
($0C0_H$) **Reset Value: $0000\ 0000_H$**

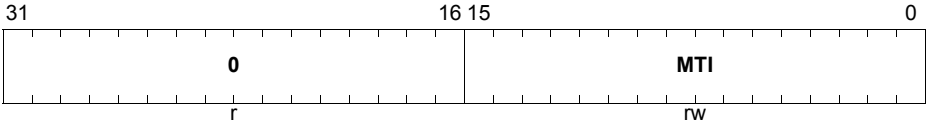


Field	Bits	Type	Description
MUX	[1:0]	rw	**Trigger Input Channel Selection** 00_B DCM0 output is selected as PLL input 01_B DCM1 output is selected as PLL input 10_B DCM2 output is selected as PLL input 11_B DCM3 output is selected as PLL input
AEN	2	rw	**Automatic End Mode Enable** With the Automatic End Mode compensation of input signal's period length variation (acceleration, deceleration) is requested 0_B Automatic End Mode is disabled 1_B Automatic End Mode is enabled
PEN	3	rwh	**Unexpected Period End Behavior** 0_B Counter decrements with constant frequency 1_B Counter is allowed to decrement with f_{GPTA} frequency in case of an input signal period length' reduction Programming PEN to 1 immediately changes the microtick counter to decrement with f_{GPTA} frequency. This bit is protected during read-modify-write operations (hardware will win).

Field	Bits	Type	Description
REN	4	rw	**Interrupt Service Request Enable** 0_B Interrupt request is disabled 1_B An interrupt request is set when the number of remaining output pulses to be generated reaches zero
0	[31:5]	r	**Reserved** Read as 0; should be written with 0.

GPTA0_PLLMTI
GPTA0 Phase Locked Loop Microtick Register
($0C4_H$) **Reset Value: $0000\ 0000_H$**

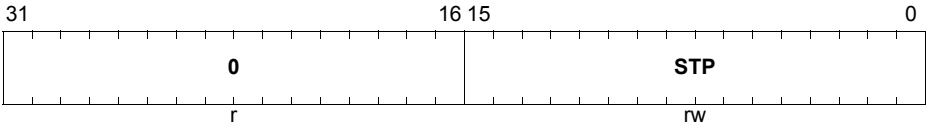
GPTA1_PLLMTI
GPTA1 Phase Locked Loop Microtick Register
($0C4_H$) **Reset Value: $0000\ 0000_H$**



Field	Bits	Type	Description
MTI	[15:0]	rw	**Microtick Value** Number of output pulses to be generated within one input signal period.
0	[31:16]	r	**Reserved** Read as 0; should be written with 0.

GPTA0_PLLSTP
GPTA0 Phase Locked Loop Step Register
($0CC_H$) **Reset Value: 0000 0000$_H$**

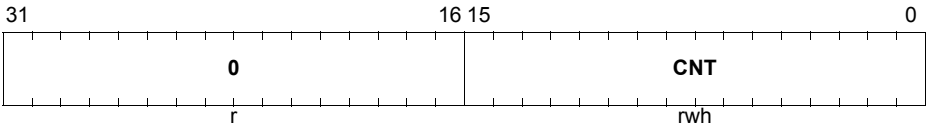
GPTA1_PLLSTP
GPTA1 Phase Locked Loop Step Register
($0CC_H$) **Reset Value: 0000 0000$_H$**



Field	Bits	Type	Description
STP	[15:0]	rw	**Step Value** Number of output pulses to be generated within one input signal period (2-complement data format).
0	[31:16]	r	**Reserved** Read as 0; should be written with 0.

GPTA0_PLLCNT
GPTA0 Phase Locked Loop Counter Register
($0C8_H$) **Reset Value: 0000 0000$_H$**

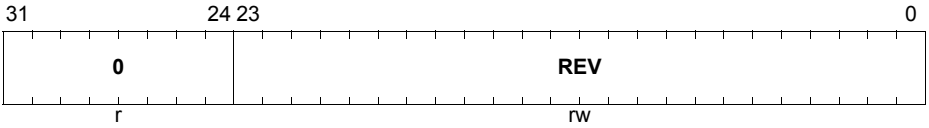
GPTA1_PLLCNT
GPTA1 Phase Locked Loop Counter Register
($0C8_H$) **Reset Value: 0000 0000$_H$**



Field	Bits	Type	Description
CNT	[15:0]	rwh	**Pulse Counter** Counter for the number of remaining output pulses to be generated.
0	[31:16]	r	**Reserved** Read as 0; should be written with 0.

GPTA0_PLLREV
GPTA0 Phase Locked Loop Reload Register
($0D0_H$) **Reset Value: $0000\ 0000_H$**

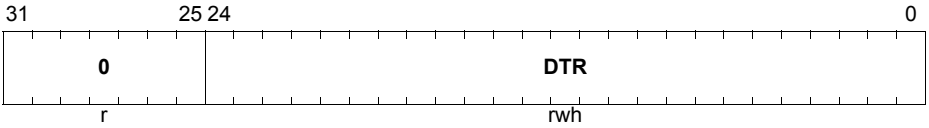
GPTA1_PLLREV
GPTA1 Phase Locked Loop Reload Register
($0D0_H$) **Reset Value: $0000\ 0000_H$**



Field	Bits	Type	Description
REV	[23:0]	rw	**Reload Value** Reload value calculated by a subtraction of the number of output pulses to be generated within one input signal period from the input signal's period length (measured in number of GPTA®v5 module clocks).
0	[31:24]	r	**Reserved** Read as 0; should be written with 0.

GPTA0_PLLDTR
GPTA0 Phase Locked Loop Delta Register
($0D4_H$) **Reset Value: $0000\ 0000_H$**

GPTA1_PLLDTR
GPTA1 Phase Locked Loop Delta Register
($0D4_H$) **Reset Value: $0000\ 0000_H$**

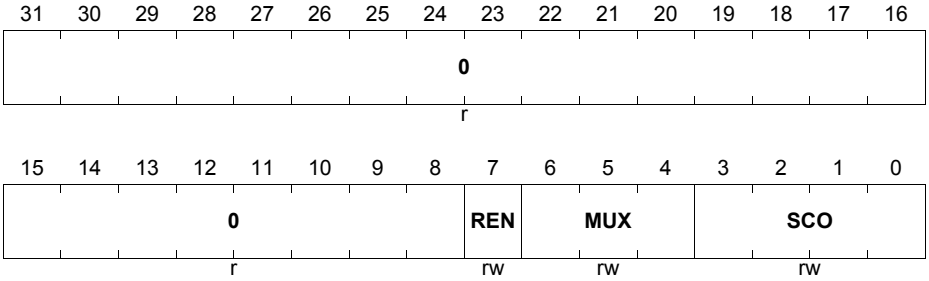


Field	Bits	Type	Description
DTR	[24:0]	rwh	**Delta Register Value** Internal register used to store intermediate results for output pulse generation. **Do not write to this register while PLL is running!**
0	[31:25]	r	**Reserved** Read as 0; should be written with 0.

28.4.6 Global Timer Registers

GPTA0_GTCTRk (k = 0-1)
GPTA0 Global Timer Control Register k
($0E0_H$+k*10_H) **Reset Value: 0000 0000_H**

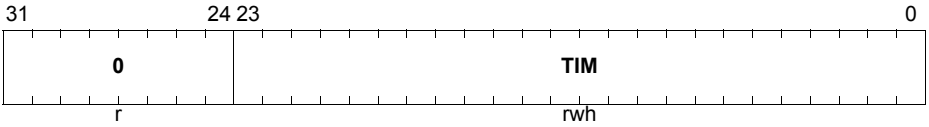
GPTA1_GTCTRk (k = 0-1)
GPTA1 Global Timer Control Register k
($0E0_H$+k*10_H) **Reset Value: 0000 0000_H**



Field	Bits	Type	Description
SCO	[3:0]	rw	**TGE Flag Source Selection** This bit field determines the bit of the operation result “GTk timer value - data bus value” which is used as TGE flag. 0000_B 10^{th} bit is used as TGE flag. 0001_B 11^{th} bit is used as TGE flag. …B … 1110_B 24^{th} bit is used as TGE flag. 1111_B 25^{th} bit is used as TGE flag.
MUX	[6:4]	rw	**Timer Clock Selection** One of eight available clock bus lines is selected as the timer GTk clock. 000_B Clock bus line CLK0 selected 001_B Clock bus line CLK1 selected 010_B Clock bus line CLK2 selected 011_B Clock bus line CLK3 selected 100_B Clock bus line CLK4 selected 101_B Clock bus line CLK5 selected 110_B Clock bus line CLK6 selected 111_B Clock bus line CLK7 selected

Field	Bits	Type	Description
REN	7	rw	**Interrupt Request Enable** 0_B The interrupt request is disabled 1_B An interrupt request is generated when timer GTk overflows
0	[31:8]	r	**Reserved** Read as 0; should be written with 0.

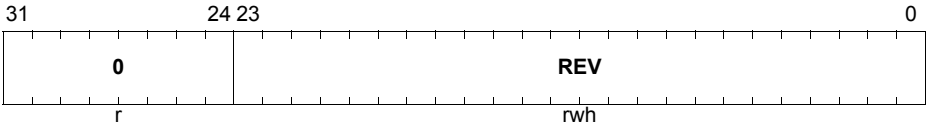
GPTA0_GTTIMk (k = 0-1)
GPTA0 Global Timer Register k **($0E8_H$+k*10_H)** **Reset Value: 0000 0000_H**
GPTA1_GTTIMk (k = 0-1)
GPTA1 Global Timer Register k **($0E8_H$+k*10_H)** **Reset Value: 0000 0000_H**



Field	Bits	Type	Description
TIM	[23:0]	rwh	**Timer Value of Global Timer k**
0	[31:24]	r	**Reserved** Read as 0; should be written with 0.

GPTA0_GTREVk (k = 0-1)
GPTA0 Global Timer Reload Value Register k
($0E4_H$+k*10_H) **Reset Value: 0000 0000_H**

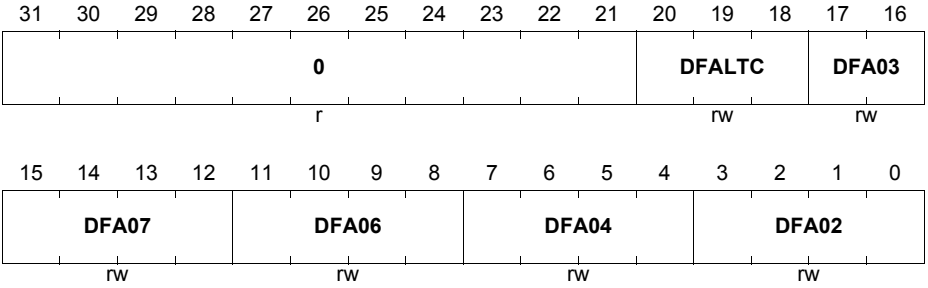
GPTA1_GTREVk (k = 0-1)
GPTA1 Global Timer Reload Value Register k
($0E4_H$+k*10_H) **Reset Value: 0000 0000_H**



Field	Bits	Type	Description
REV	[23:0]	rw	**Reload Value of Global Timer k** Reload value for timer GTk after an overflow
0	[31:24]	r	**Reserved** Read as 0; should be written with 0.

28.4.7 Clock Bus Register

GPTA0_CKBCTR
GPTA0 Clock Bus Control Register ($0D8_H$) Reset Value: 0000 FFFF$_H$
GPTA1_CKBCTR
GPTA1 Clock Bus Control Register ($0D8_H$) Reset Value: 0000 FFFF$_H$



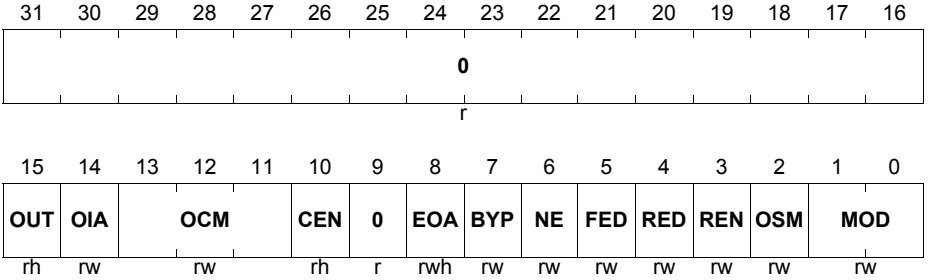
Field	Bits	Type	Description
DFA02	[3:0]	rw	**Clock Line 2 Driving Source Selection** 0_D CLK2 is provided with the GPTA®v5 module clock f_{GPTA} divided by 2^{DFA02} 1_D CLK2 is provided with the GPTA®v5 module clock f_{GPTA} divided by 2^{DFA02} ... 13_D CLK2 is provided with the GPTA®v5 module clock f_{GPTA} divided by 2^{DFA02} 14_D CLK2 is driven by PLL clock of other GPTA®v5 unit 15_D CLK2 is driven by DCM3 output
DFA04	[7:4]	rw	**Clock Line 4 Driving Source Selection** 0_D CLK4 is provided with the GPTA®v5 module clock f_{GPTA} divided by 2^{DFA04} 1_D CLK4 is provided with the GPTA®v5 module clock f_{GPTA} divided by 2^{DFA04} ... 14_D CLK4 is provided with the GPTA®v5 module clock f_{GPTA} divided by 2^{DFA04} 15_D CLK4 is driven by DCM1 output

Field	Bits	Type	Description
DFA06	[11:8]	rw	**Clock Line 6 Driving Source Selection** 0_D CLK6 is provided with the GPTA®v5 module clock f_{GPTA} divided by 2^{DFA06} 1_D CLK6 is provided with the GPTA®v5 module clock f_{GPTA} divided by 2^{DFA06} ... 14_D CLK6 is provided with the GPTA®v5 module clock f_{GPTA} divided by 2^{DFA06} 15_D CLK6 is driven by FPC1 output
DFA07	[15:12]	rw	**Clock Line 7 Driving Source Selection** 0_D CLK7 is provided with the GPTA®v5 module clock f_{GPTA} divided by 2^{DFA07} 1_D CLK7 is provided with the GPTA®v5 module clock f_{GPTA} divided by 2^{DFA07} ... 14_D CLK7 is provided with the GPTA®v5 module clock f_{GPTA} divided by 2^{DFA07} 15_D CLK7 is driven by FPC4 output
DFA03	[17:16]	rw	**Clock Line 3 Driving Source Selection** 0_D CLK3 is driven by DCM2 output 1_D CLK3 is driven by PLL clock of other GPTA®v5 unit 2_D CLK3 is driven by uncompensated PLL clock 3_D CLK3 is driven by uncompensated PLL clock of other GPTA®v5 unit
DFALTC	[20:18]	rw	**Dividing Factor for LTC Prescaler Clock Selection** 0_D The LTCPRE clock is provided with the GPTA®v5 module clock f_{GPTA} divided by 2^{DFALTC}. 1_D The LTCPRE clock is provided with the GPTA®v5 module clock f_{GPTA} divided by 2^{DFALTC}. ... 7_D The LTCPRE clock is provided with the GPTA®v5 module clock f_{GPTA} divided by 2^{DFALTC}.
0	[31:21]	r	**Reserved** Read as 0; should be written with 0.

28.4.8 Global Timer Cell Registers

GPTA0_GTCCTRk (k = 00-31)
GPTA0 Global Timer Cell Control Register k [Capture Mode]
(100_H+k*8_H) **Reset Value: 0000 0000_H**

GPTA1_GTCCTRk (k = 00-31)
GPTA1 Global Timer Cell Control Register k [Capture Mode]
(100_H+k*8_H) **Reset Value: 0000 0000_H**



Field	Bits	Type	Description
MOD	[1:0]	rw	**Mode Control Bits** 00_B GTCk operates in Capture Mode hooked to GT0. 01_B GTCk operates in Capture Mode hooked to GT1. 10_B GTCk operates in Compare Mode hooked to GT0. 11_B GTCk operates in Compare Mode hooked to GT1.
OSM	2	rw	**One Shot Mode Enable** 0_B GTCk is continuously enabled. 1_B GTCk is enabled for one event only.
REN	3	rw	**Interrupt Request Enable** 0_B Service request is disabled. 1_B Service request line SQSk is activated when a capture or compare event has occurred.
RED	4	rw	**Input Rising Edge Select** 0_B Capture event is not triggered by a rising edge. 1_B Capture event is triggered by a rising edge on the GTCkIN input line.
FED	5	rw	**Input Falling Edge Select** 0_B Capture event is not triggered by a falling edge. 1_B Capture event is triggered by a falling edge on the GTCkIN input line.

Field	Bits	Type	Description
NE	6	rw	**Not Effective** Reserved
BYP	7	rw	**Bypass** 0_B M0O/M1O lines are affected either by M0I/M1I lines or by OCM0/OCM1 bits. 1_B M0O/M1O lines are affected only by M0I/M1I lines. *Note: OCM2 must be set in any case to enable reaction on M0I/M1I changes.*
EOA	8	rwh	**Enable On Action** 0_B GTCk is enabled for local events. 1_B GTCk is disabled for local events. On an event on the communication link via M0I/M1I lines, EOA will be cleared and local events will be enabled. EOA is bit protected (see **Section 28.4.2**). EOA is cleared if mode is switched to Timer Mode.
CEN	10	rh	**Cell Enable** 0_B GTCk is currently disabled for local events. 1_B GTCk is currently enabled for local events.
OCM	[13:11]	rw	**Output Control Mode Select** 000_B Current state of GTCkOUT output line is hold 001_B Current state of GTCkOUT output line is toggled by an internal GTCk event otherwise hold 010_B GTCkOUT output line is forced to 0 by an internal GTCk event otherwise hold 011_B GTCkOUT output line is forced to 1 by an internal GTCk event otherwise hold $1XX_B$ GTCkOUT output line state is affected by an internal GTCk event and/or by an operation occurred in an adjacent GTCn (n = less or equal k) and reported by the M1I, M0I interface lines.
OIA	14	rw	**Output Immediate Action** 0_B No immediate action required. 1_B Action defined by OCM must be performed immediately. Reading bit OIA always returns 0.
OUT	15	rh	**Output State** 0_B GTCkOUT output line is 0. 1_B GTCkOUT output line is 1.

Field	Bits	Type	Description
0	9, [31:16]	r	**Reserved** Read as 0; should be written with 0.

GPTA0_GTCCTRk (k = 00-31)
GPTA0 Global Timer Cell Control Register k [Compare Mode]
(100_H+k*8_H) **Reset Value: 0000 0000_H**

GPTA1_GTCCTRk (k = 00-31)
GPTA1 Global Timer Cell Control Register k [Compare Mode]
(100_H+k*8_H) **Reset Value: 0000 0000_H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUT	**OIA**	**OCM**			**CEN**	**0**	**EOA**	**BYP**	**CAT**	**CAC**	**GES**	**REN**	**OSM**	**MOD**	
rh	rw	rw			rh	r	rwh	rw	rw	rw	rw	rw	rw	rw	

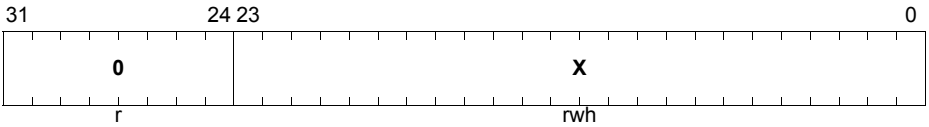
Field	Bits	Type	Description
MOD	[1:0]	rw	**Mode Control Bits** 00_B GTCk operates in Capture Mode hooked to GT0. 01_B GTCk operates in Capture Mode hooked to GT1. 10_B GTCk operates in Compare Mode hooked to GT0. 11_B GTCk operates in Compare Mode hooked to GT1.
OSM	2	rw	**One Shot Mode Enable** 0_B GTCk is continuously enabled. 1_B GTCk is enabled for one event only.
REN	3	rw	**Interrupt Request Enable** 0_B Service request is disabled. 1_B Service request line SQSk is activated when a capture or compare event has occurred.
GES	4	rw	**Greater Equal Select** 0_B An “equal” compare is selected. 1_B A “greater equal” compare is required.

Field	Bits	Type	Description
CAC	5	rw	**Capture after Compare Select** 0_B Capture after compare is disabled. 1_B After a compare event, the contents of the associated Global Timer as selected by MOD or (depending on control bit CAT) the contents of the alternate Global Timer are copied to the capture/compare register GTCXRk.
CAT	6	rw	**Capture Alternate Timer** 0_B The Global Timer as selected by MOD is captured, if enabled by control bit CAC = 1. 1_B The alternate Global Timer is captured.
BYP	7	rw	**Bypass** 0_B M1O/M0O lines are affected either by M1I/M0I lines or by OCM1/OCM0 bits. 1_B M0O/M1O lines are affected only by M0I/M1I lines. *Note: OCM2 must be set in any case to enable reaction on M0I/M1I changes.*
EOA	8	rwh	**Enable On Action** 0_B GTCk is enabled for local events. 1_B GTCk is disabled for local events. On an event on the communication link via M0I/M1I lines, EOA will be cleared and local events will be enabled. EOA is bit protected (see **Section 28.4.2**). EOA is cleared if mode is switched to Timer Mode.
CEN	10	rh	**Cell Enable** 0_B GTCk is currently disabled for local events. 1_B GTCk is currently enabled for local events.
OCM	[13:11]	rw	**Output Control Mode Select** 000_B Current state of GTCkOUT output line is hold 001_B Current state of GTCkOUT output line is toggled by an internal GTCk event otherwise hold 010_B GTCkOUT output line is forced to 0 by an internal GTCk event otherwise hold 011_B GTCkOUT output line is forced to 1 by an internal GTCk event otherwise hold $1XX_B$ GTCkOUT output line state is affected by an internal GTCk event and/or by an operation occurred in an adjacent GTCn (n = less or equal k) and reported by the M1I, M0I interface lines.

Field	Bits	Type	Description
OIA	14	rw	**Output Immediate Action** 0_B No immediate action required. 1_B Action defined by OCM must be performed immediately. Reading bit OIA always returns 0.
OUT	15	rh	**Output State** 0_B GTCkOUT output line is 0. 1_B GTCkOUT output line is 1.
0	9, [31:16]	r	**Reserved** Read as 0; should be written with 0.

GPTA0_GTCXRk (k = 00-31)
GPTA0 Global Timer Cell X Register k
(104_H+k*8_H) **Reset Value: 0000 0000_H**

GPTA1_GTCXRk (k = 00-31)
GPTA1 Global Timer Cell X Register k
(104_H+k*8_H) **Reset Value: 0000 0000_H**



Field	Bits	Type	Description
X	[23:0]	rwh	**Capture/Compare Register Contents of GTCk**
0	[31:24]	r	**Reserved** Read as 0; should be written with 0.

Note: GTCXRk is write-protected when control bits CAC and OSM are set to 1 (“capture after compare” in Single Shot Mode). Write protection is activated, when the value of the selected GT timer matches and/or exceeds the capture/compare register contents. Write protection is released after a software access to register GTCXRk.

28.4.9 Local Timer Cell Registers

GPTA0_LTCCTRk (k = 00-62)
GPTA0 Local Timer Cell Control Register k [Timer Mode ILM=0]
(200_H+k*8_H) Reset Value: 0000 0000_H

GPTA1_LTCCTRk (k = 00-62)
GPTA1 Local Timer Cell Control Register k [Timer Mode ILM=0]
(200_H+k*8_H) Reset Value: 0000 0000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															GBYP
r															rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUT	OIA	OCM			CEN	CUD	ILM	CUD CLR	SLO	FED	RED	REN	OSM	MOD	
rh	rw	rw			rh	rwh	rw	w	rwh	rw	rw	rw	rw	rw	

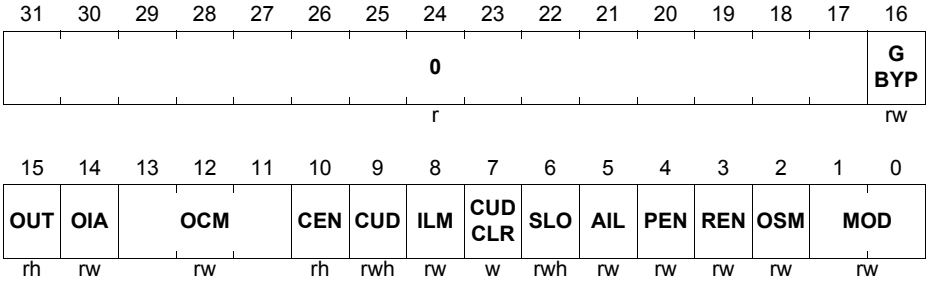
Field	Bits	Type	Description
MOD	[1:0]	rw	**Mode Control Bits** 00_B LTCk operates in Capture Mode. 01_B LTCk operates in Compare Mode. 10_B LTCk operates in Free-Running Timer Mode. 11_B LTCk operates in reset Timer Mode.
OSM	2	rw	**One Shot Mode Enable** 0_B LTCk is continuously enabled. 1_B LTCk is enabled for one event only.
REN	3	rw	**Request Enable** 0_B Service request is disabled. 1_B Service request SQSk is activated when a - capture event has occurred - compare event has occurred - timer overflow has happened depending on the operation mode selected by bit field MOD.
RED	4	rw	**Input Rising Edge Select** 0_B Timer is not updated by a rising edge. 1_B Timer is updated by a rising edge on the LTCkIN input line.

Field	Bits	Type	Description
FED	5	rw	**Input Falling Edge Select** 0_B Timer is not updated by a falling edge. 1_B Timer is updated by a falling edge on the LTCkIN input line.
SLO	6	rwh	**Select Line Output** 0_B State of select line output SO is 0. 1_B State of select line output SO is 1. SLO is bit protected (see **Page 28-167**).
CUDCLR	7	w	**Coherent Update Disable** 0_B No effect. 1_B Coherent update disabled (bit CUD is cleared). If bits CUD and CUDCLR are both written with 1, bit CUD will be set. CUDCLR is always read as 0.
ILM	8	rw	**Input Line Mode** 0_B Input line is operating in Edge Sensitive Mode. 1_B Input line is operating in Level Sensitive Mode. In case of full speed GPTA®v5 module clock selection as input clock, Level Sensitive Mode must be selected. In this case the Edge Sensitive Mode will not produce any event.
CUD	9	rwh	**Coherent Update Enable** 0_B Select output SO is not toggled on timer reset overflow. 1_B Select output SO is toggled on next timer reset overflow. When CUD is set by software, it remains set until the next timer reset overflow (LTCk reset event) occurs and is cleared by hardware afterwards. CUD can be reset by software by writing bit CUDCLR with 1 and CUD with 0. CUD is automatically cleared after LTCk reset event and when mode is switched to another mode than Reset Timer Mode. This bit can only be set in Reset Timer Mode. If bits CUD and CUDCLR are both written with 1, bit CUD will be set. CUDCLR is always read as 0.
CEN	10	rh	**Cell Enable** 0_B LTCk is currently disabled for local events. 1_B LTCk is currently enabled for local events.

Field	Bits	Type	Description
OCM	[13:11]	rw	**Output Control Mode Select** 000_B Current state of LTCkOUT output line is hold 001_B Current state of LTCkOUT output line is toggled by an internal LTCk event otherwise hold 010_B LTCkOUT output line is forced to 0 by an internal LTCk event otherwise hold 011_B LTCkOUT output line is forced to 1 by an internal LTCk event otherwise hold $1XX_B$ LTCkOUT output line state is affected by an internal LTCk event and/or by an operation occurred in an adjacent LTCk cell (reported by M1I/M0I interface lines).
OIA	14	rw	**Output Immediate Action** 0_B No immediate action required. 1_B Action defined by bit field OCM must be performed immediately. OIA is always read as 0.
OUT	15	rh	**Output State** 0_B LTCkOUT output line is 0. 1_B LTCkOUT output line is 1.
GBYP	16	rw	**Global Bypass** 0_B M3O/M2O lines are affected by M1I/M0I lines. 1_B M3O/M2O lines are affected by M3I/M2I lines.
0	[31:17]	r	**Reserved** Read as 0; should be written with 0.

GPTA0_LTCCTRk (k = 00-62)
GPTA0 Local Timer Cell Control Register k [Timer Mode ILM=1]
(200_H+k*8_H) **Reset Value: 0000 0000_H**

GPTA1_LTCCTRk (k = 00-62)
GPTA1 Local Timer Cell Control Register k [Timer Mode ILM=1]
(200_H+k*8_H) **Reset Value: 0000 0000_H**



Field	Bits	Type	Description
MOD	[1:0]	rw	**Mode Control Bits** 00_B LTCk operates in Capture Mode. 01_B LTCk operates in Compare Mode. 10_B LTCk operates in Free-Running Timer Mode. 11_B LTCk operates in reset Timer Mode.
OSM	2	rw	**One Shot Mode Enable** 0_B LTCk is continuously enabled. 1_B LTCk is enabled for one event only.
REN	3	rw	**Request Enable** 0_B Service request is disabled. 1_B Service request SQSk is activated when a - capture event has occurred - compare event has occurred - timer overflow has happened depending on the operation mode selected by bit field MOD.
PEN	4	rw	**LTC Prescaler Enable** 0_B LTC Prescaler Mode is disabled. 1_B LTC Prescaler Mode with LTC prescaler clock LTCPRE is enabled.

Field	Bits	Type	Description
AIL	5	rw	**Active Input Level Select** 0_B Input signal is active high. 1_B Input signal is active low.
SLO	6	rwh	**Select Line Output** 0_B State of select line output SO is 0. 1_B State of select line output SO is 1. SLO is bit protected (see **Page 28-167**).
CUDCLR	7	w	**Coherent Update Disable** 0_B No effect. 1_B Coherent update disabled (bit CUD is cleared). If bits CUD and CUDCLR are both written with 1, bit CUD will be set. CUDCLR is always read as 0.
ILM	8	rw	**Input Line Mode** 0_B Input line is operating in Edge Sensitive Mode. 1_B Input line is operating in Level Sensitive Mode. In case of full speed GPTA®v5 module clock selection as input clock, Level Sensitive Mode must be selected. In this case the Edge Sensitive Mode will not produce any event.
CUD	9	rwh	**Coherent Update Enable** 0_B Select output SO is not toggled on timer reset overflow. 1_B Select output SO is toggled on next timer reset overflow. When CUD is set by software, it remains set until the next timer reset overflow (LTCk reset event) occurs and is cleared by hardware afterwards. CUD can be reset by software by writing bit CUDCLR with 1 and CUD with 0. CUD is automatically cleared after LTCk reset event and when mode is switched to another mode than Reset Timer Mode. This bit can only be set in Reset Timer Mode. If bits CUD and CUDCLR are both written with 1, bit CUD will be set. CUDCLR is always read as 0.
CEN	10	rh	**Cell Enable** 0_B LTCk is currently disabled for local events. 1_B LTCk is currently enabled for local events.

Field	Bits	Type	Description
OCM	[13:11]	rw	**Output Control Mode Select** 000_B Current state of LTCkOUT output line is hold 001_B Current state of LTCkOUT output line is toggled by an internal LTCk event otherwise hold 010_B LTCkOUT output line is forced to 0 by an internal LTCk event otherwise hold 011_B LTCkOUT output line is forced to 1 by an internal LTCk event otherwise hold $1XX_B$ LTCkOUT output line state is affected by an internal LTCk event and/or by an operation occurred in an adjacent LTCk cell (reported by M1I/M0I interface lines).
OIA	14	rw	**Output Immediate Action** 0_B No immediate action required. 1_B Action defined by bit field OCM must be performed immediately. OIA is always read as 0.
OUT	15	rh	**Output State** 0_B LTCkOUT output line is 0. 1_B LTCkOUT output line is 1.
GBYP	16	rw	**Global Bypass** 0_B M3O/M2O lines are affected by M1I/M0I lines. 1_B M3O/M2O lines are affected by M3I/M2I lines.
0	[31:17]	r	**Reserved** Read as 0; should be written with 0.

GPTA0_LTCCTRk (k = 00-62)
GPTA0 Local Timer Cell Control Register k [Capture Mode]
(200_H+k*8_H) **Reset Value: 0000 0000_H**

GPTA1_LTCCTRk (k = 00-62)
GPTA1 Local Timer Cell Control Register k [Capture Mode]
(200_H+k*8_H) **Reset Value: 0000 0000_H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															GBYP
r															rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUT	OIA	OCM			CEN	SLL	ILM	EOA	BYP	FED	RED	REN	OSM	MOD	
rh	rw	rw			rh	rh	rw	rwh	rw	rw	rw	rw	rw	rw	

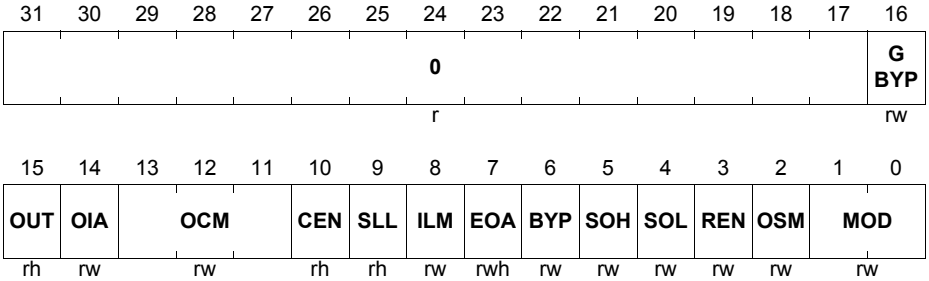
Field	Bits	Type	Description
MOD	[1:0]	rw	**Mode Control Bits** 00_B LTCk operates in Capture Mode. 01_B LTCk operates in Compare Mode. 10_B LTCk operates in Free-Running Timer Mode. 11_B LTCk operates in reset Timer Mode.
OSM	2	rw	**One Shot Mode Enable** 0_B LTCk is continuously enabled. 1_B LTCk is enabled for one event only.
REN	3	rw	**Request Enable** 0_B Service request is disabled. 1_B Service request SQSk is activated when a - capture event has occurred - compare event has occurred - timer overflow has happened depending on the operation mode selected by bit field MOD.
RED	4	rw	**Input Rising Edge Select** 0_B Capture event is not triggered by a rising edge. 1_B Capture event is triggered by a rising edge on the LTCkIN input line.

Field	Bits	Type	Description
FED	5	rw	**Input Falling Edge Select** 0_B Capture event is not triggered by a falling edge. 1_B Capture event is triggered by a falling edge on the LTCkIN input line.
BYP	6	rw	**Local Bypass** 0_B M1O/M0O lines are affected either by M1I/M0I lines or by OCM1/OCM0 bits. 1_B M1O/M0O lines are affected only by M1I/M0I (GBYP = 0) or M2I/M2I (GBYP = 1) lines. This bit is cleared if mode is switched to Timer Mode. OCM2 must be set in any case to enable reaction on M1I/M0I change.
EOA	7	rwh	**Enable On Action** 0_B LTCk is enabled for local events. 1_B LTCk is disabled for local events. On an event on the communication link via M0I/M1I lines, EOA will be cleared and local events will be enabled. EOA is bit protected (see **Section 28.4.2**). EOA is cleared if mode is switched to Timer Mode.
ILM	8	rw	**Input Line Mode** 0_B Input line is operating in Edge Sensitive Mode. 1_B Input line is operating in Level Sensitive Mode. In case of full speed GPTA®v5 module clock selection as input clock, Level Sensitive Mode must be selected. In this case the Edge Sensitive Mode will not produce any event.
SLL	9	rh	**Capture & Compare Mode: Select Line Level** 0_B Current state of select input SI is 0. 1_B Current state of select input SI is 1.
CEN	10	rh	**Cell Enable** 0_B LTCk is currently disabled for local events. 1_B LTCk is currently enabled for local events.

Field	Bits	Type	Description
OCM	[13:11]	rw	**Output Control Mode Select** 000_B Current state of LTCkOUT output line is hold 001_B Current state of LTCkOUT output line is toggled by an internal LTCk event otherwise hold 010_B LTCkOUT output line is forced to 0 by an internal LTCk event otherwise hold 011_B LTCkOUT output line is forced to 1 by an internal LTCk event otherwise hold $1XX_B$ LTCkOUT output line state is affected by an internal LTCk event and/or by an operation occurred in an adjacent LTCk cell (reported by M1I/M0I interface lines).
OIA	14	rw	**Output Immediate Action** 0_B No immediate action required. 1_B Action defined by bit field OCM must be performed immediately. OIA is always read as 0.
OUT	15	rh	**Output State** 0_B LTCkOUT output line is 0. 1_B LTCkOUT output line is 1.
GBYP	16	rw	**Global Bypass** 0_B M3O/M2O lines are affected by M1I/M0I lines. 1_B M3O/M2O lines are affected by M3I/M2I lines.
0	[31:17]	r	**Reserved** Read as 0; should be written with 0.

GPTA0_LTCCTRk (k = 00-62)
GPTA0 Local Timer Cell Control Register k [Compare Mode]
(200_H+k*8_H) **Reset Value: 0000 0000_H**

GPTA1_LTCCTRk (k = 00-62)
GPTA1 Local Timer Cell Control Register k [Compare Mode]
(200_H+k*8_H) **Reset Value: 0000 0000_H**



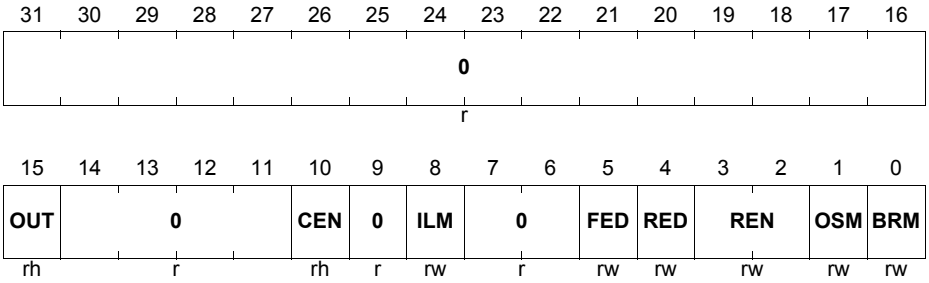
Field	Bits	Type	Description
MOD	[1:0]	rw	**Mode Control Bits** 00_B LTCk operates in Capture Mode. 01_B LTCk operates in Compare Mode. 10_B LTCk operates in Free-Running Timer Mode. 11_B LTCk operates in reset Timer Mode.
OSM	2	rw	**One Shot Mode Enable** 0_B LTCk is continuously enabled. 1_B LTCk is enabled for one event only.
REN	3	rw	**Request Enable** 0_B Service request is disabled. 1_B Service request SQSk is activated when a - capture event has occurred - compare event has occurred - timer overflow has happened depending on the operation mode selected by bit field MOD.
SOL	4	rw	**Compare Mode: Select Output Low** 0_B Compare is deactivated or on high level. 1_B Compare operation is enabled by a low level on select input SI[1)].

Field	Bits	Type	Description
SOH	5	rw	**Compare Mode: Select Output High** 0_B Compare is deactivated or on high level. 1_B Compare operation is enabled by a high level on select input SI[1)].
BYP	6	rw	**Bypass** 0_B M1O/M0O lines are affected either by M1I/M0I lines or by OCM1/OCM0 bits. 1_B M1O/M0O lines are affected only by M1I/M0I lines. This bit is cleared if mode is switched to Timer Mode. OCM2 must be set in any case to enable reaction on M1I/M0I change.
EOA	7	rwh	**Enable On Action** 0_B LTCk is enabled for local events. 1_B LTCk is disabled for local events. On an event on the communication link via M0I/M1I lines, EOA will be cleared and local events will be enabled. EOA is bit protected (see **Section 28.4.2**). EOA is cleared if mode is switched to Timer Mode.
ILM	8	rw	**Input Line Mode** 0_B Input line is operating in Edge Sensitive Mode. 1_B Input line is operating in Level Sensitive Mode. In case of full speed GPTA®v5 module clock selection as input clock, Level Sensitive Mode must be selected. In this case the Edge Sensitive Mode will not produce any event.
SLL	9	rh	**Select Line Level** 0_B Current state of select input SI is 0. 1_B Current state of select input SI is 1.
CEN	10	rh	**Cell Enable** 0_B LTCk is currently disabled for local events. 1_B LTCk is currently enabled for local events.

Field	Bits	Type	Description
OCM	[13:11]	rw	**Output Control Mode Select** 000_B Current state of LTCkOUT output line is hold 001_B Current state of LTCkOUT output line is toggled by an internal LTCk event otherwise hold 010_B LTCkOUT output line is forced to 0 by an internal LTCk event otherwise hold 011_B LTCkOUT output line is forced to 1 by an internal LTCk event otherwise hold $1XX_B$ LTCkOUT output line state is affected by an internal LTCk event and/or by an operation occurred in an adjacent LTCk cell (reported by M1I/M0I interface lines).
OIA	14	rw	**Output Immediate Action** 0_B No immediate action required. 1_B Action defined by bit field OCM must be performed immediately. OIA is always read as 0.
OUT	15	rh	**Output State** 0_B LTCkOUT output line is 0. 1_B LTCkOUT output line is 1.
GBYP	16	rw	**Global Bypass** 0_B M3O/M2O lines are affected by M1I/M0I lines. 1_B M3O/M2O lines are affected by M3I/M2I lines.
0	[31:17]	r	**Reserved** Read as 0; should be written with 0.

1) To enable Compare Mode in all cases, SOL and SOH bits must be set to 1.

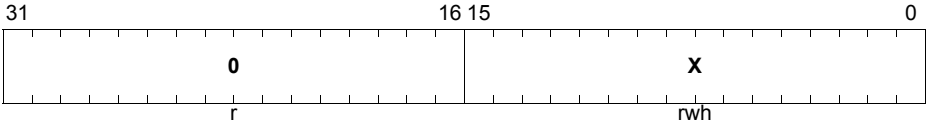
GPTA0_LTCCTR63
GPTA0 Local Timer Cell Control Register 63($3F8_H$) **Reset Value: $0000\ 0000_H$**
GPTA1_LTCCTR63
GPTA1 Local Timer Cell Control Register 63($3F8_H$) **Reset Value: $0000\ 0000_H$**



Field	Bits	Type	Description
BRM	0	rw	**Bit Reversal Mode Control** 0_B Compare uses normal sequence of local input data bus (YI) bits. 1_B Compare uses reversed sequence of local input data bus (YI) bits.
OSM	1	rw	**One Shot Mode Enable for Shadow Register Copy** 0_B Shadow register copy is continuously enabled. 1_B Shadow register copy is enabled for one event only.
REN	[3:2]	rw	**Request Enable** 00_B Service request SQT63 is disabled. 01_B Service request SQT63 is generated when a compare event has occurred. 10_B Service request SQT63 is generated when a shadow register copy event has occurred. 11_B Reserved.
RED	4	rw	**Rising Edge Select for Shadow Register Copy** 0_B Shadow register copy is not triggered by a rising edge on the LTC63IN input line. 1_B Shadow register copy is triggered by a rising edge on the LTC63IN input line.

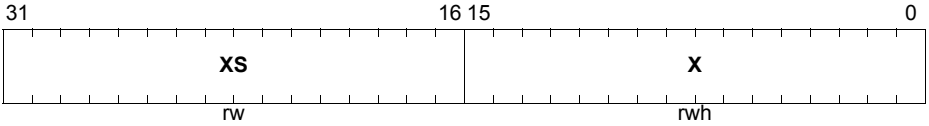
Field	Bits	Type	Description
FED	5	rw	**Falling Edge Select for Shadow Register Copy** 0_B Shadow register copy is not triggered by a falling edge on the LTC63IN input line. 1_B Shadow register copy is triggered by a falling edge on the LTC63IN input line.
ILM	8	rw	**Shadow Register Copy Input Line Mode** 0_B LTC63IN is operating in Edge Sensitive Mode. 1_B LTC63IN is operating in Level Sensitive Mode.
CEN	10	rh	**Enable for Shadow Register Copy** 0_B Shadow register copy is currently disabled. 1_B Shadow register copy is currently enabled.
OUT	15	rh	**Output State** 0_B LTC63OUT output line is 0. 1_B LTC63OUT output line is 1.
0	[7:6], 9, [14:11], [31:16]	r	**Reserved** Read as 0; should be written with 0.

GPTA0_LTCXRk (k = 00-62)
GPTA0 Local Timer Cell X Register k(204_H+k*8_H) **Reset Value: 0000 0000_H**
GPTA1_LTCXRk (k = 00-62)
GPTA1 Local Timer Cell X Register k(204_H+k*8_H) **Reset Value: 0000 0000_H**



Field	Bits	Type	Description
X	[15:0]	rwh	**Local Timer Data Register Value**
0	[31:16]	r	**Reserved** Read as 0; should be written with 0.

GPTA0_LTCXR63
GPTA0 Local Timer Cell X Register 63(3FC$_H$) **Reset Value: 0000 0000$_H$**
GPTA1_LTCXR63
GPTA1 Local Timer Cell X Register 63(3FC$_H$) **Reset Value: 0000 0000$_H$**



Field	Bits	Type	Description
X	[15:0]	rwh	**Compare Register Value** Software write operations has priority above a simultaneous hardware update.
XS	[31:16]	rw	**Shadow Register Value**

28.4.10 Multiplexer Control Registers

These registers are not directly accessible and can be written and read only via the multiplexer register array FIFO (see **Page 28-121**).

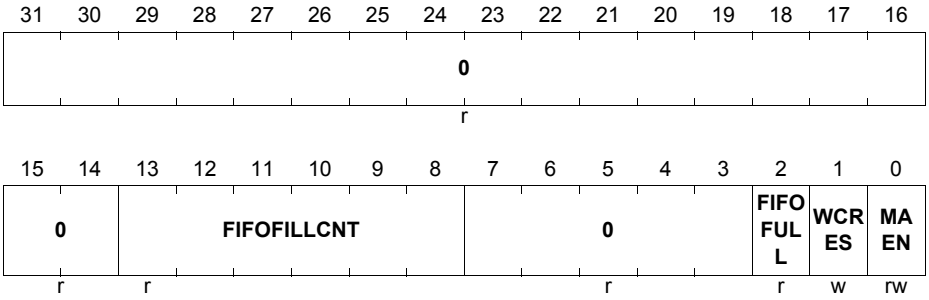
I/O Sharing Block Registers

The three registers MRACTL, MRADIN, and MRADOUT are used to write data to and read data from the GTCA Multiplexer Register Array FIFO. The Multiplexer Register Array FIFO controls the operation of the Input/Output Line Sharing Block (see **"Input/Output Line Sharing Block (IOLS)" on Page 28-235**).

The Multiplexer Register Array Control register controls the operation of the Multiplexer Register Array FIFO.

GPTA0_MRACTL
GPTA0 Multiplexer Register Array Control Register
(038_H) **Reset Value: 0000 0000$_H$**

GPTA1_MRACTL
GPTA1 Multiplexer Register Array Control Register
(038_H) **Reset Value: 0000 0000$_H$**



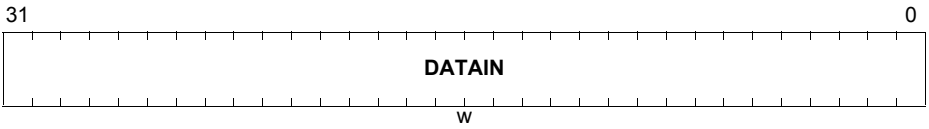
Field	Bits	Type	Description
MAEN	0	rw	**Multiplexer Array Enable** Bit field MAEN enables/disables the programming and the interconnections of the multiplexer array. 0_B Multiplexer array is disabled; all cell inputs are driven with 0, GPTA®v5 I/O lines (pins) are disconnected and FIFO writing is enabled. 1_B Multiplexer array is enabled; all cell and I/O line interconnections are established as previously programmed and FIFO writing is disabled.

Field	Bits	Type	Description
WCRES	1	w	**Write Count Reset** Writing WCRES with 1 while the array is disabled (MAEN = 0), resets the write cycle counter to zero and the FIFO written sequentially (initialized). WCRES is always read as 0.
FIFOFULL	2	r	**FIFO Full Status** 0_B FIFO not completely written (write access to MRADIN allowed). 1_B FIFO completely written (write access to MRADIN ignored). Must be re-enabled via WCRES before array can be re-initialized.
FIFOFILLCNT	[13:8]	r	**FIFO Fill Count** This bit field shows the current contents of the write cycle counter.
0	[7:3], [31:14]	r	**Reserved** Read as 0; should be written with 0.

The Multiplexer Register Array Data In register is used to **write** data to the Multiplexer Register Array FIFO. The Multiplexer Register Array Data Out register is used to **read** data from the Multiplexer Register Array FIFO.

GPTA0_MRADIN
GPTA0 Multiplexer Register Array Data In Register
($03C_H$) **Reset Value: $0000\ 0000_H$**

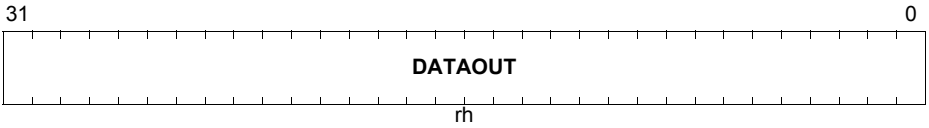
GPTA1_MRADIN
GPTA1 Multiplexer Register Array Data In Register
($03C_H$) **Reset Value: $0000\ 0000_H$**



Field	Bits	Type	Description
DATAIN	[31:0]	w	**FIFO Write Data** This register contains the FIFO write data as defined for the Output Multiplexer Control Registers and the Input Multiplexer Control Registers.

GPTA0_MRADOUT
GPTA0 Multiplexer Register Array Data Out Register
(040_H) **Reset Value: 0000 0000_H**

GPTA1_MRADOUT
GPTA1 Multiplexer Register Array Data Out Register
(040_H) **Reset Value: 0000 0000_H**



Field	Bits	Type	Description
DATAOUT	[31:0]	rh	**FIFO Read Data** This register contains the FIFO read data as assigned for the Output Multiplexer Control Registers and the Input Multiplexer Control Registers.

Note: For correct operation, the MRADIN and MRADIN registers must be always read or written 32-bit wide. 8-bit and 16-bit accesses are ignored without any bus error!

Output Multiplexer Control Registers

Two registers, OMCRL and OMCRH, are assigned to each I/O Group IOG[6:0] and each Output Group OG[6:0]. OMCRL[6:0]/OMCRH[6:0] are assigned to IOG[6:0] and OMCRL[13:7]/OMCRH[13:7] are assigned to OG[6:0].

OMCRL controls the connections of group pins 0 to 3. OMCRH controls the connections of group pins 4 to 7.

GPTA0_OMCRLg (g = 0-13)
GPTA0 Output Multiplexer Control Register for Lower Half of Group g
Reset Value: 0000 0000$_H$

GPTA1_OMCRLg (g = 0-13)
GPTA1 Output Multiplexer Control Register for Lower Half of Group g
Reset Value: 0000 0000$_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	OMG3			0	OML3			0	OMG2			0	OML2		
r	rw			r	rw			r	rw			r	rw		

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	OMG1			0	OML1			0	OMG0			0	OML0		
r	rw			r	rw			r	rw			r	rw		

Field	Bits	Type	Description
OML0, OML1, OML2, OML3	[2:0], [10:8], [18:16], [26:24]	rw	**Multiplexer Line Selection** This bit field selects the input line of a OMG that can be selected by bit field OMGn for OMG output n. 000_B OMG input IN0 selected 001_B OMG input IN1 selected 010_B OMG input IN2 selected 011_B OMG input IN3 selected 100_B OMG input IN4 selected 101_B OMG input IN5 selected 110_B OMG input IN6 selected 111_B OMG input IN7 selected
OMG0, OMG1, OMG2, OMG3	[6:4], [14:12], [22:20], [30:28]	rw	**Multiplexer Group Selection** This bit field determines the OMGng which is connected to input n of I/O Group g or Output group g-7. $X00_B$ OMG0g selected $X01_B$ OMG1g selected $X10_B$ OMG2g selected All other combinations are reserved. If a reserved combination of OMGn value is selected, the corresponding OMG output is forced to 0 level. For compatibility reasons, OMGn[2] = 0 should be used (as value for X) for OMGn bit field programming.
0	3, 7, 11, 15, 19, 23, 27, 31	r	**Reserved** Read as 0; should be written with 0.

GPTA0_OMCRHg (g = 0-13)
Output Multiplexer Control Register for Upper Half of Pin Group g
Reset Value: 0000 0000$_H$

GPTA1_OMCRHg (g = 0-13)
Output Multiplexer Control Register for Upper Half of Pin Group g
Reset Value: 0000 0000$_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	**OMG7**			**0**	**OML7**			**0**	**OMG6**			**0**	**OML6**		
r	rw			r	rw			r	rw			r	rw		

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	**OMG5**			**0**	**OML5**			**0**	**OMG4**			**0**	**OML4**		
r	rw			r	rw			r	rw			r	rw		

Field	Bits	Type	Description
OML4, OML5, OML6, OML7	[2:0], [10:8], [18:16], [26:24]	rw	**Multiplexer Line Selection** This bit field selects the input line of a OMG that can be selected by bit field OMGn for OMG output n. 000_B OMG input IN0 selected 001_B OMG input IN1 selected 010_B OMG input IN2 selected 011_B OMG input IN3 selected 100_B OMG input IN4 selected 101_B OMG input IN5 selected 110_B OMG input IN6 selected 111_B OMG input IN7 selected
OMG4, OMG5, OMG6, OMG7	[6:4], [14:12], [22:20], [30:28]	rw	**Multiplexer Group Selection** This bit field determines the OMGng which is connected to input n of I/O Group g or Output group g-7. $X00_B$ OMG0g selected $X01_B$ OMG1g selected $X10_B$ OMG2g selected All other combinations are reserved. If a reserved combination of OMGn value is selected, the corresponding OMG output is forced to 0 level. For compatibility reasons, OMGn[2] = 0 should be used (as value for X) for OMGn bit field programming.

Field	Bits	Type	Description
0	3, 7, 11, 15, 19, 23, 27, 31	r	**Reserved** Read as 0; should be written with 0.

On-Chip Trigger and Gating Signal Multiplexer Control Registers

OTMCR controls the connections of I/O output group signals to the Trigger and Gating Signals TRIGgn

GPTA0_OTMCRg (g = 0-1)
GPTA0 On-Chip Trigger and Gating Multiplexer Control Register of Group g
Reset Value: 0000 0000$_H$

GPTA1_OTMCRg (g = 0-1)
GPTA1 On-Chip Trigger and Gating Multiplexer Control Register of Group g
Reset Value: 0000 0000$_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	**OTM7**			**0**	**OTM6**			**0**	**OTM5**			**0**	**OTM4**		
r	rw			r	rw			r	rw			r	rw		

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	**OTM3**			**0**	**OTM2**			**0**	**OTM1**			**0**	**OTM0**		
r	rw			r	rw			r	rw			r	rw		

Field	Bits	Type	Description
OTMn, (n=0...7)	[4 x (n + 4):4 x n]	rw	**Multiplexer Line Selection** This bit field selects the input line of a OMG that can be selected by bit field OMGn for OMG output n. 000_B OTMG input IN0 selected 001_B OTMG input IN1 selected 010_B OTMG input IN2 selected 011_B OTMG input IN3 selected 100_B OTMG input IN4 selected 101_B OTMG input IN5 selected 110_B OTMG input IN6 selected 111_B OTMG input IN7 selected
0	3, 7, 11, 15, 19, 23, 27, 31	r	**Reserved** Read as 0; should be written with 0.

GTC Input Multiplexer Control Registers

Two registers, GIMCRL and GIMCRH, are assigned to each GTCG[3:0]. GIMCRL controls the connections of cells 0 to 3 in a GTC Group. GIMCRH controls the connections of cells 4 to 7 in a GTC Group.

*Note: These registers are not directly accessible and can be written and read only via the multiplexer register array FIFO (see **Section 28.3.4.6**).*

GPTA0_GIMCRLg (g = 0-3)
GPTA0 Input Multiplexer Control Register for Lower Half of GTC Group g
Reset Value: 0000 0000$_H$

GPTA1_GIMCRLg (g = 0-3)
GPTA1 Input Multiplexer Control Register for Lower Half of GTC Group g
Reset Value: 0000 0000$_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
GIMEN3	GIMG3			0	GIML3			GIMEN2	GIMG2			0	GIML2		
r	rw			r	rw			r	rw			r	rw		

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GIMEN1	GIMG1			0	GIML1			GIMEN0	GIMG0			0	GIML0		
rw	rw			r	rw			rw	rw			r	rw		

Field	Bits	Type	Description
GIML0, GIML1, GIML2, GIML3	[2:0], [10:8], [18:16], [26:24]	rw	**Multiplexer Line Selection** This bit field selects the input line of a GIMG that can be selected by bit field GIMGn for GIMG output n. 000_B GIMG input IN0 selected 001_B GIMG input IN1 selected 010_B GIMG input IN2 selected 011_B GIMG input IN3 selected 100_B GIMG input IN4 selected 101_B GIMG input IN5 selected 110_B GIMG input IN6 selected 111_B GIMG input IN7 selected

Field	Bits	Type	Description
GIMG0, GIMG1, GIMG2, GIMG3	[6:4], [14:12], [22:20], [30:28]	rw	**Multiplexer Group Selection** This bit field determines the GIMGng which is connected to input n of GTC group g. 000_B GIMG0g selected 001_B GIMG1g selected (reserved for g = 3) 010_B GIMG2g selected 011_B GIMG3g selected 100_B GIMG4g selected All other combinations are reserved.
GIMEN0, GIMEN1, GIMEN2, GIMEN3	7, 15, 23, 31	rw	**Enable Multiplexer Connection** 0_B Input n is not connected to any line. 1_B Input n is connected to the line defined by GIMLn and GIMGn.
0	3, 11, 19, 27	r	**Reserved** Read as 0; should be written with 0.

GPTA0_GIMCRHg (g = 0-3)
GPTA0 Input Multiplexer Control Register for Upper Half of GTC Group g
Reset Value: 0000 0000$_H$

GPTA1_GIMCRHg (g = 0-3)
GPTA1 Input Multiplexer Control Register for Upper Half of GTC Group g
Reset Value: 0000 0000$_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
GIM EN7	GIMG7			0	GIML7			GIM EN6	GIMG6			0	GIML6		
r	rw			r	rw			r	rw			r	rw		

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GIM EN5	GIMG5			0	GIML5			GIM EN4	GIMG4			0	GIML4		
r	rw			r	rw			r	rw			r	rw		

Field	Bits	Type	Description
GIML4, GIML5, GIML6, GIML7	[2:0], [10:8], [18:16], [26:24]	rw	**Multiplexer Line Selection** This bit field selects the input line of a GIMG that can be selected by bit field GIMGn for GIMG output n. 000_B GIMG input IN0 selected 001_B GIMG input IN1 selected 010_B GIMG input IN2 selected 011_B GIMG input IN3 selected 100_B GIMG input IN4 selected 101_B GIMG input IN5 selected 110_B GIMG input IN6 selected 111_B GIMG input IN7 selected
GIMG4, GIMG5, GIMG6, GIMG7	[6:4], [14:12], [22:20], [30:28]	rw	**Multiplexer Group Selection** This bit field determines the GIMGng which is connected to input n of GTC group g. 000_B GIMG0g selected 001_B GIMG1g selected (reserved for g = 3) 010_B GIMG2g selected 011_B GIMG3g selected 100_B GIMG4g selected All other combinations are reserved.

Field	Bits	Type	Description
GIMEN4, GIMEN5, GIMEN6, GIMEN7	7, 15, 23, 31	rw	**Enable Multiplexer Connection** 0_B Input n is not connected to any line. 1_B Input n is connected to the line defined by GIMLn and GIMGn.
0	3, 11, 19, 27	r	**Reserved** Read as 0; should be written with 0.

LTC Input Multiplexer Control Registers

Two registers, LIMCRL and LIMCRH, are assigned to each LTC group. LIMCRL controls the connections of LTC group cells with index 0 to 3. LIMCRH controls the connections of LTC group cells with index 4 to 7.

*Note: These registers are not directly accessible and can be written and read only via the multiplexer register array FIFO (see **Section 28.3.4.6**).*

GPTA0_LIMCRLg (g = 0-7)
GPTA0 Input Multiplexer Control Register for Lower Half of LTC Group g
Reset Value: 0000 0000$_H$

GPTA1_LIMCRLg (g = 0-7)
GPTA1 Input Multiplexer Control Register for Lower Half of LTC Group g
Reset Value: 0000 0000$_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LIM EN3	LIMG3			0	LIML3			LIM EN2	LIMG2			0	LIML2		
r	rw			r	rw			r	rw			r	rw		

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LIM EN1	LIMG1			0	LIML1			LIM EN0	LIMG0			0	LIML0		
r	rw			r	rw			r	rw			r	rw		

Field	Bits	Type	Description
LIML0, LIML1, LIML2, LIML3	[2:0], [10:8], [18:16], [26:24]	rw	**Multiplexer Line Selection** This bit field selects the input line of a LIMG that can be selected by bit field LIMGn for LIMG output n. 000_B LIMG input IN0 selected 001_B LIMG input IN1 selected 010_B LIMG input IN2 selected 011_B LIMG input IN3 selected 100_B LIMG input IN4 selected 101_B LIMG input IN5 selected 110_B LIMG input IN6 selected 111_B LIMG input IN7 selected

Field	Bits	Type	Description
LIMG0, LIMG1, LIMG2, LIMG3	[6:4], [14:12], [22:20], [30:28]	rw	**Multiplexer Group Selection** This bit field determines the LIMGng which is connected to input n of LTC group g. 000_B LIMG0g selected 001_B LIMG1g selected (reserved for g = 3) 010_B LIMG2g selected 011_B LIMG3g selected 100_B LIMG4g selected All other combinations are reserved.
LIMEN0, LIMEN1, LIMEN2, LIMEN3	7, 15, 23, 31	rw	**Enable Multiplexer Connection** 0_B Input n is not connected to any line. 1_B Input n is connected to the line defined by LIMLn and LIMGn.
0	3, 11, 19, 27	r	**Reserved** Read as 0; should be written with 0.

GPTA0_LIMCRHg (g = 0-7)
GPTA0 Input Multiplexer Control Register for Upper Half of LTC Group g
Reset Value: 0000 0000$_H$

GPTA1_LIMCRHg (g = 0-7)
GPTA1 Input Multiplexer Control Register for Upper Half of LTC Group g
Reset Value: 0000 0000$_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LIM EN7	LIMG7			0	LIML7			LIM EN6	LIMG6			0	LIML6		
r	rw			r	rw			r	rw			r	rw		

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LIM EN5	LIMG5			0	LIML5			LIM EN4	LIMG4			0	LIML4		
r	rw			r	rw			r	rw			r	rw		

Field	Bits	Type	Description
LIML4, LIML5, LIML6, LIML7	[2:0], [10:8], [18:16], [26:24]	rw	**Multiplexer Line Selection** This bit field selects the input line of a LIMG that can be selected by bit field LIMGn for LIMG output n. 000_B LIMG input IN0 selected 001_B LIMG input IN1 selected 010_B LIMG input IN2 selected 011_B LIMG input IN3 selected 100_B LIMG input IN4 selected 101_B LIMG input IN5 selected 110_B LIMG input IN6 selected 111_B LIMG input IN7 selected
LIMG4, LIMG5, LIMG6, LIMG7	[6:4], [14:12], [22:20], [30:28]	rw	**Multiplexer Group Selection** This bit field determines the LIMGng which is connected to input n of LTC group g. 000_B LIMG0g selected 001_B LIMG1g selected (reserved for g = 3) 010_B LIMG2g selected 011_B LIMG3g selected 100_B LIMG4g selected All other combinations are reserved.

Field	Bits	Type	Description
LIMEN4, **LIMEN5,** **LIMEN6,** **LIMEN7**	7, 15, 23, 31	rw	**Enable Multiplexer Connection** 0_B Input n is not connected to any line. 1_B Input n is connected to the line defined by LIMLn and LIMGn.
0	3, 11, 19, 27	r	**Reserved** Read as 0; should be written with 0.

28.4.11 Service Request Registers

The bits in the Service Request State Registers are service request status flags that are set by hardware (type “h”) when the related event occurs, regardless if a respective Interrupt Request is enabled. Each service request status flag can be read twice (in SRSCx register and in SRSSx register, x = 0-3) and cleared or set by software when writing to the specific request bit in SRSCx or SRSSx. If enabled, a interrupt request is generated regardless of the content of the SRSSx or SRSCx registers.

The service request status flags can be reset (cleared) by software when writing a 1 to the corresponding bit location in the SRSCx registers. Writing a 0 has no effect.

The service request status flags can be set by software when writing a 1 to the corresponding bit location in the SRSSx registers. Writing a 0 has no effect.

GPTA0_SRSC0
GPTA0 Service Request State Clear Register 0
(010_H) **Reset Value: $0000\ 0000_H$**

GPTA1_SRSC0
GPTA1 Service Request State Clear Register 0
(010_H) **Reset Value: $0000\ 0000_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	GT 01	GT 00	PLL	DCM 03C	DCM 03F	DCM 03R	DCM 02C	DCM 02F	DCM 02R	DCM 01C	DCM 01F	DCM 01R	DCM 00C	DCM 00F	DCM 00R
r	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh

Field	Bits	Type	Description
DCM00R, **DCM01R,** **DCM02R,** **DCM03R**	0, 3, 6, 9	rwh[1)]	**DCMk[2)] Rising Edge Event Service Request State** 0_B No service is requested. 1_B Service is requested due to a rising edge detected on the DCMk input signal line.
DCM00F, **DCM01F,** **DCM02F,** **DCM03F**	1, 4, 7, 10	rwh[1)]	**DCMk[2)] Falling Edge Event Service Request State** 0_B No service is requested. 1_B Service is requested due to a falling edge detected on the DCMk input signal line.

Field	Bits	Type	Description
DCM00C, DCM01C, DCM02C, DCM03C	2, 5, 8, 11	rwh[1]	**DCMk[2] Compare Event Service Request State** 0_B No service is requested. 1_B Service is requested due to a compare event occurred in DCMk cell (k = 0-3).
PLL	12	rwh[1]	**Counter Service Request State for PLL** 0_B No service is requested. 1_B Service is requested because the counter for the number remaining output pulses decremented to 0.
GT00	13	rwh[1]	**GT0 Timer Service Request State** 0_B No service is requested. 1_B Service is requested due to a GT0 timer overflow.
GT01	14	rwh[1]	**GT1 Timer Service Request State** 0_B No service is requested. 1_B Service is requested due to a GT1 timer overflow.
0	[31:15]	r	**Reserved** Read as 0; should be written with 0.

1) Writing an one to a set bit clears the bit. All other write operations have no effect.

2) k = 0-3; k = 0 refers to DCM00R, DCM00F, or DCM00C; k = 1 refers to DCM01R, DCM01F, or DCM01C; k = 2 refers to DCM02R, DCM02F, or DCM02C; k = 3 refers to DCM03R, DCM03F, or DCM03C.

GPTA0_SRSS0
GPTA0 Service Request State Set Register 0
(014_H) **Reset Value: 0000 0000$_H$**

GPTA1_SRSS0
GPTA1 Service Request State Set Register 0
(014_H) **Reset Value: 0000 0000$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	GT 01	GT 00	PLL	DCM 03C	DCM 03F	DCM 03R	DCM 02C	DCM 02F	DCM 02R	DCM 01C	DCM 01F	DCM 01R	DCM 00C	DCM 00F	DCM 00R
r	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh

Field	Bits	Type	Description
DCM00R, **DCM01R,** **DCM02R,** **DCM03R**	0, 3, 6, 9	rwh[1)]	**DCMk[2)] Rising Edge Event Service Request State** 0_B No service is requested. 1_B Service is requested due to a rising edge detected on DCMk input signal line.
DCM00F, **DCM01F,** **DCM02F,** **DCM03F**	1, 4, 7, 10	rwh[1)]	**DCMk[2)] Falling Edge Event Service Request State** 0_B No service is requested. 1_B Service is requested due to a falling edge detected on DCMk input signal line.
DCM00C, **DCM01C,** **DCM02C,** **DCM03C**	2, 5, 8, 11	rwh[1)]	**DCMk[2)] Compare Event Service Request State** 0_B No service is requested. 1_B Service is requested due to a compare event occurred in DCMk cell.
PLL	12	rwh[1)]	**Counter Service Request State for PLL** 0_B No service is requested 1_B Service is requested because the counter for the number remaining output pulses decremented to 0.
GT00	13	rwh[1)]	**GT0 Timer Service Request State** 0_B No service is requested. 1_B Service is requested due to a GT0 timer overflow.

Field	Bits	Type	Description
GT01	14	rwh[1)]	**GT1 Timer Service Request State** 0_B No service is requested. 1_B Service is requested due to a GT1 timer overflow.
0	[31:15]	r	**Reserved** Read as 0; should be written with 0.

1) Writing a one to a cleared bit sets the bit. All other write operations have no effect.

2) k = 0-3; k = 0 refers to DCM00R, DCM00F, or DCM00C; k = 1 refers to DCM01R, DCM01F, or DCM01C; k = 2 refers to DCM02R, DCM02F, or DCM02C; k = 3 refers to DCM03R, DCM03F, or DCM03C.

GPTA0_SRSC1
GPTA0 Service Request State Clear Register 1
(018_H) **Reset Value: 0000 0000$_H$**

GPTA1_SRSC1
GPTA1 Service Request State Clear Register 1
(018_H) **Reset Value: 0000 0000$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
GTC 31	**GTC 30**	**GTC 29**	**GTC 28**	**GTC 27**	**GTC 26**	**GTC 25**	**GTC 24**	**GTC 23**	**GTC 22**	**GTC 21**	**GTC 20**	**GTC 19**	**GTC 18**	**GTC 17**	**GTC 16**
rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GTC 15	**GTC 14**	**GTC 13**	**GTC 12**	**GTC 11**	**GTC 10**	**GTC 09**	**GTC 08**	**GTC 07**	**GTC 06**	**GTC 05**	**GTC 04**	**GTC 03**	**GTC 02**	**GTC 01**	**GTC 00**
rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh

Field	Bits	Type	Description
GTCk (k = 00-31)	k	rwh[1)]	**GTCk Capture/Compare Service Request State** 0_B No service is requested. 1_B Service is requested due to a capture or compare event occurred in GTCk.

1) Writing an one to a set bit clears the bit. All other write operations have no effect.

GPTA0_SRSS1
GPTA0 Service Request State Set Register 1
(01C$_H$) **Reset Value: 0000 0000$_H$**

GPTA1_SRSS1
GPTA1 Service Request State Set Register 1
(01C$_H$) **Reset Value: 0000 0000$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
GTC 31	**GTC 30**	**GTC 29**	**GTC 28**	**GTC 27**	**GTC 26**	**GTC 25**	**GTC 24**	**GTC 23**	**GTC 22**	**GTC 21**	**GTC 20**	**GTC 19**	**GTC 18**	**GTC 17**	**GTC 16**
rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GTC 15	**GTC 14**	**GTC 13**	**GTC 12**	**GTC 11**	**GTC 10**	**GTC 09**	**GTC 08**	**GTC 07**	**GTC 06**	**GTC 05**	**GTC 04**	**GTC 03**	**GTC 02**	**GTC 01**	**GTC 00**
rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh

Field	Bits	Type	Description
GTCk (k = 00-31)	k	rwh[1)]	**GTCk Capture/Compare Service Request State** 0_B No service is requested. 1_B Service is requested due to a capture or compare event occurred in GTCk.

1) Writing a one to a cleared bit sets the bit. All other write operations have no effect.

GPTA0_SRSC2
GPTA0 Service Request State Clear Register 2
(020_H) **Reset Value: 0000 0000$_H$**

GPTA1_SRSC2
GPTA1 Service Request State Clear Register 2
(020_H) **Reset Value: 0000 0000$_H$**

LTCA2_SRSC2
LTCA2 Service Request State Clear Register 2
(020_H) **Reset Value: 0000 0000$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LTC 31	**LTC 30**	**LTC 29**	**LTC 28**	**LTC 27**	**LTC 26**	**LTC 25**	**LTC 24**	**LTC 23**	**LTC 22**	**LTC 21**	**LTC 20**	**LTC 19**	**LTC 18**	**LTC 17**	**LTC 16**
rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LTC 15	**LTC 14**	**LTC 13**	**LTC 12**	**LTC 11**	**LTC 10**	**LTC 09**	**LTC 08**	**LTC 07**	**LTC 06**	**LTC 05**	**LTC 04**	**LTC 03**	**LTC 02**	**LTC 01**	**LTC 00**
rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh

Field	Bits	Type	Description
LTCk (k = 00-31)	k	rwh[1)]	**LTCk Timer/Capture/Compare Service Request State** 0_B No service is requested. 1_B Service is requested due to a timer overflow, capture, or compare event that occurred in LTCk.

1) Writing an one to a set bit clears the bit. All other write operations have no effect.

GPTA0_SRSS2
GPTA0 Service Request State Set Register 2
(024_H) **Reset Value: 0000 0000$_H$**

GPTA1_SRSS2
GPTA1 Service Request State Set Register 2
(024_H) **Reset Value: 0000 0000$_H$**

LTCA2_SRSS2
LTCA2 Service Request State Set Register 2
(024_H) **Reset Value: 0000 0000$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LTC 31	**LTC 30**	**LTC 29**	**LTC 28**	**LTC 27**	**LTC 26**	**LTC 25**	**LTC 24**	**LTC 23**	**LTC 22**	**LTC 21**	**LTC 20**	**LTC 19**	**LTC 18**	**LTC 17**	**LTC 16**
rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LTC 15	**LTC 14**	**LTC 13**	**LTC 12**	**LTC 11**	**LTC 10**	**LTC 09**	**LTC 08**	**LTC 07**	**LTC 06**	**LTC 05**	**LTC 04**	**LTC 03**	**LTC 02**	**LTC 01**	**LTC 00**
rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh

Field	Bits	Type	Description
LTCk (k = 00-31)	k	rwh[1)]	**LTCk Timer/Capture/Compare Service Request State** 0_B No service is requested. 1_B Service is requested due to a timer overflow, capture, or compare event that occurred in LTCk.

1) Writing a one to a cleared bit sets the bit. All other write operations have no effect.

GPTA0_SRSC3
GPTA0 Service Request State Clear Register 3
(028_H) **Reset Value: 0000 0000$_H$**

GPTA1_SRSC3
GPTA1 Service Request State Clear Register 3
(028_H) **Reset Value: 0000 0000$_H$**

LTCA2_SRSC3
LTCA2 Service Request State Clear Register 3
(028_H) **Reset Value: 0000 0000$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LTC 63	**LTC 62**	**LTC 61**	**LTC 60**	**LTC 59**	**LTC 58**	**LTC 57**	**LTC 56**	**LTC 55**	**LTC 54**	**LTC 53**	**LTC 52**	**LTC 51**	**LTC 50**	**LTC 49**	**LTC 48**
rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LTC 47	**LTC 46**	**LTC 45**	**LTC 44**	**LTC 43**	**LTC 42**	**LTC 41**	**LTC 40**	**LTC 39**	**LTC 38**	**LTC 37**	**LTC 36**	**LTC 35**	**LTC 34**	**LTC 33**	**LTC 32**
rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh

Field	Bits	Type	Description
LTCk (k = 32-63)	k-32	rwh[1)]	**LTCk Timer/Capture/Compare Service Request State** 0_B No service is requested. 1_B Service is requested due to a timer overflow, capture, or compare event that occurred in LTCk.

1) Writing an one to a set bit clears the bit. All other write operations have no effect.

GPTA0_SRSS3
GPTA0 Service Request State Set Register 3
($02C_H$) **Reset Value: $0000\ 0000_H$**

GPTA1_SRSS3
GPTA1 Service Request State Set Register 3
($02C_H$) **Reset Value: $0000\ 0000_H$**

LTCA2_SRSS3
LTCA2 Service Request State Set Register 3
($02C_H$) **Reset Value: $0000\ 0000_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LTC 63	**LTC 62**	**LTC 61**	**LTC 60**	**LTC 59**	**LTC 58**	**LTC 57**	**LTC 56**	**LTC 55**	**LTC 54**	**LTC 53**	**LTC 52**	**LTC 51**	**LTC 50**	**LTC 49**	**LTC 48**
rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LTC 47	**LTC 46**	**LTC 45**	**LTC 44**	**LTC 43**	**LTC 42**	**LTC 41**	**LTC 40**	**LTC 39**	**LTC 38**	**LTC 37**	**LTC 36**	**LTC 35**	**LTC 34**	**LTC 33**	**LTC 32**
rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh

Field	Bits	Type	Description
LTCk (k = 32-63)	k-32	rwh[1)]	**LTCk Timer/Capture/Compare Service Request State** 0_B No service is requested. 1_B Service is requested due to a timer overflow, capture, or compare event that occurred in LTCk.

1) Writing a one to a cleared bit sets the bit. All other write operations have no effect.

Node Redirection Register

The Service Request Node Redirection Register allows that GTC service requests of GTCs with an odd index number k can be individually redirected via register SRNR to a service request group that is assigned mainly to four LTCs. More details are provided on Page 28-124.

GPTA0_SRNR
GPTA0 Service Request Node Redirection Register
(030_H) **Reset Value: 0000 0000$_H$**

GPTA1_SRNR
GPTA1 Service Request Node Redirection Register
(030_H) **Reset Value: 0000 0000$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GTC 31R	GTC 29R	GTC 27R	GTC 25R	GTC 23R	GTC 21R	GTC 19R	GTC 17R	GTC 15R	GTC 13R	GTC 11R	GTC 09R	GTC 07R	GTC 05R	GTC 03R	GTC 01R
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
GTC01R, **GTC03R,** **GTC05R,** **GTC07R,** **GTC09R,** **GTC11R,** **GTC13R,** **GTC15R,** **GTC17R,** **GTC19R,** **GTC21R,** **GTC23R,** **GTC25R,** **GTC27R,** **GTC29R,** **GTC31R**	0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15	rw	**Global Timer Cell k Redirection** 0_B No redirection of GTC service requests. 1_B Redirection of GTC service request to LTC service request groups (see Page 28-124).

Field	Bits	Type	Description
0	[31:16]	r	**Reserved** Read as 0; should be written with 0.

28.5 LTCA Kernel Description

The Local Timer Cell Array (LTCA2) is a unit that contains signal generation cells with 64 Local Timer Cells. These LTCs have identical functionality as the LTCs which are available in the signal generation cells of the GPTA®v5 module.

The Local Timer Cells (LTC00 to LTC62) can be configured to operate in different modes: Capture Mode, Compare Mode, Free-Running Timer Mode, Reset Timer Mode, and One Shot Mode. Adjacent cells may be combined to operate on the same pin, thus generating complex waveforms. One LTC (LTC63) can be used for special compare modes.

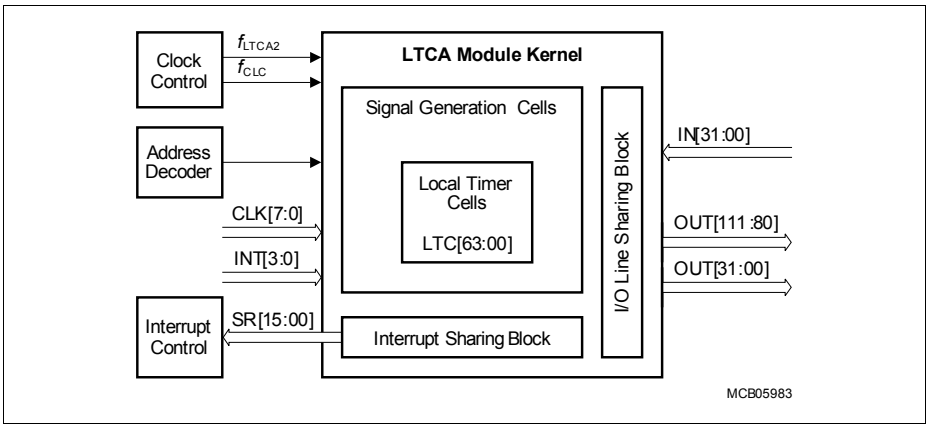


Figure 28-81 Block Diagram of LTCA Unit Kernel

The LTCA Unit Kernel contains Signal Generation Cells that contains all Local Timer Cells including an I/O Line Sharing Block that controls the LTC connections to the I/O lines and output lines. I/O lines are supposed to be connected to I/O port lines while the output lines are typically connected to a MSC interface that is especially able to control external power devices via a serial connection. The LTCs can be further connected to input signals of an external clock bus and input lines coming e.g. from other on-chip peripheral modules.

The clock control cells generates two modules clocks that are required for LTCA operation. An address decoder generates the select signals for the LTC registers. Service requests, coming from the LTCs, are able to generate interrupts via the Interrupt Sharing Block. The interrupts are handled by the external interrupt logic.

28.5.1 Local Timer Cell (LTC00 to LTC63)

LTC00 to LTC62 are fully identical with the Local Timer Cells in the GPTA0 and GPTA1 units. Its functionalities are described in GPTA®v5 section **"Local Timer Cell (LTC00 to LTC62)" on Page 28-67** and LTC63 functionalities are described in GPTA®v5 section **"Local Timer Cell LTC63" on Page 28-79**.

28.5.2 Input/Output Line Sharing Block (IOLS)

The I/O Line Sharing Block allows the inputs and outputs of the LTCA unit to be routed with high flexibility between I/O lines, output lines, clock inputs, and other on-chip peripherals. The LTCA unit provides a total of 32 input lines and 64 output lines, that are connected to four I/O groups IOG[3:0] and four output groups OG[6:3].

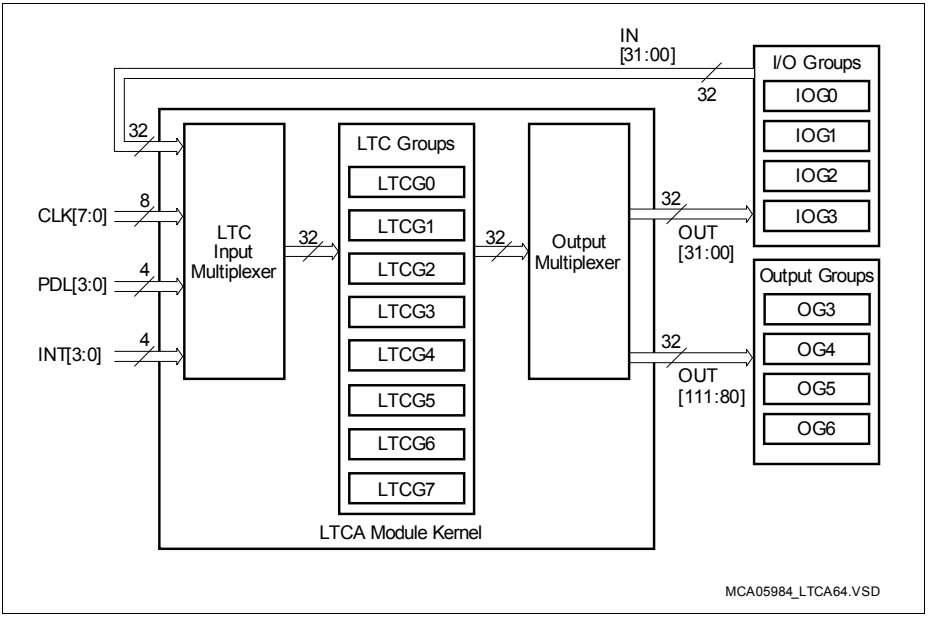


Figure 28-82 Input/Output Line Sharing Block Overview

The LTCA I/O Line Sharing Block makes the following two selections:

- LTC output multiplexer selection
- LTC input multiplexer selection

To choose these selection, the input and output lines of the related cells are integrated into groups with eight parts, each. There are I/O groups, output groups, LTC groups, and a PDL/INT group.

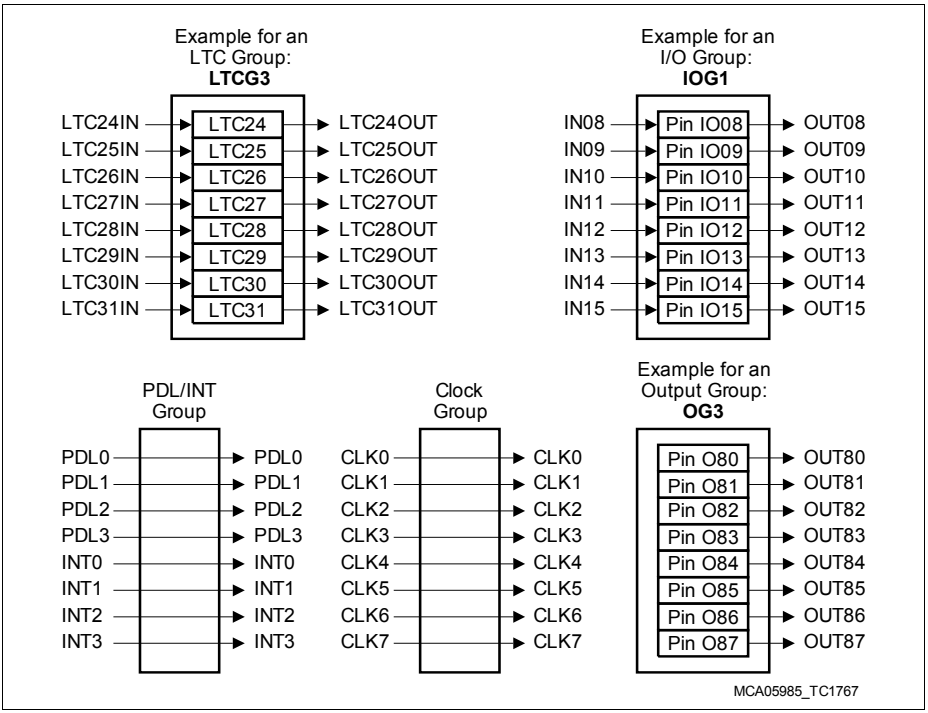


Figure 28-83 Groups Definitions for I/O Line Sharing Block

An **LTC group** combines eight LTC cells with its input and output lines. This results in eight LTC groups, LTCG0 to LTCG7.

An **I/O group** combines eight LTCA I/O lines connected to bi-directional device pins with its input and output lines. This results in four I/O groups, IOG0 to IOG3, supporting 32 I/O lines.

An **output group** combines four LTCA output lines connected to device pins as an output. This results in four output groups, OG3 to OG6, supporting 32 output lines.

The **PDL/INT group** is a logical group that combines the LTCA unit inputs PDL[3:0] together with the inputs INT[3:0].

The **clock group** is a logical group that combines the eight LTCA unit clock inputs CLK[7:0].

Table 28-20 Group to I/O Line/Cell Assignment

Group/Unit	Cell/Line	Input	Output
LTC Groups			
LTCG0	LTC[07:00]	LTC[07:00]IN	LTC[07:00]OUT
LTCG1	LTC[15:08]	LTC[15:08]IN	LTC[15:08]OUT
LTCG2	LTC[23:16]	LTC[23:16]IN	LTC[23:16]OUT
LTCG3	LTC[31:24]	LTC[31:24]IN	LTC[31:24]OUT
LTCG4	LTC[39:32]	LTC[39:32]IN	LTC[39:32]OUT
LTCG5	LTC[47:40]	LTC[47:40]IN	LTC[47:40]OUT
LTCG6	LTC[55:48]	LTC[55:48]IN	LTC[55:48]OUT
LTCG7	LTC[63:56]	LTC[63:56]IN	LTC[63:56]OUT
I/O Groups			
IOG0	–	IN[07:00]	OUT[07:00]
IOG1	–	IN[15:08]	OUT[15:08]
IOG2	–	IN[23:16]	OUT[23:16]
IOG3	–	IN[31:24]	OUT[31:24]
Output Groups			
OG3	–	–	OUT[87:80]
OG4	–	–	OUT[95:88]
OG5	–	–	OUT[103:96]
OG6	–	–	OUT[111:104]
Clock Group			
–	–	CLK[7:0]	CLK[7:0]
PDL/INT Groups			
PDL[1:0] PDL Bus	–	PDL[3:0]	PDL[3:0]
External Input [3:0]	–	INT[3:0]	INT[3:0]

28.5.2.1 Output Multiplexer

The output multiplexer shown in **Figure 28-84** and **Figure 28-86** connects the 64 LTC output lines with the I/O groups ($4 \times 8 = 32$ output lines) and the output groups ($4 \times 8 = 32$ output lines).

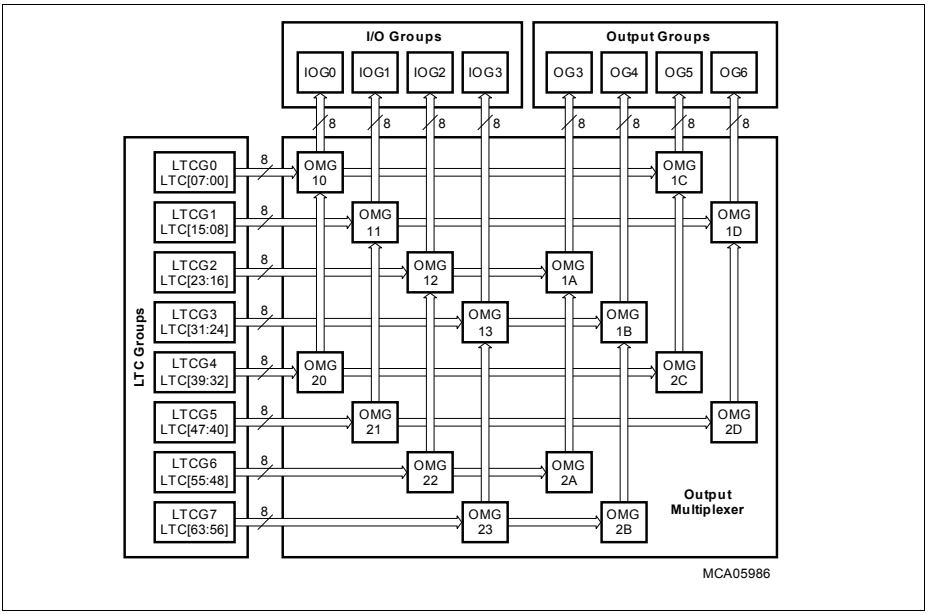


Figure 28-84 Output Multiplexer of LTCA

The output multiplexer contains Output Multiplexer Groups (OMGs) that connect the Local Timer Cells with the input lines of the I/O groups and output groups. The LTCs are grouped into eight LTC groups (LTCG[7:0]) with 8 cells each. In the same way, I/O groups and output groups are grouped into 8 groups (four I/O groups and four output groups) with 8 lines each.

Figure 28-85 shows the logical structure of an OMG.

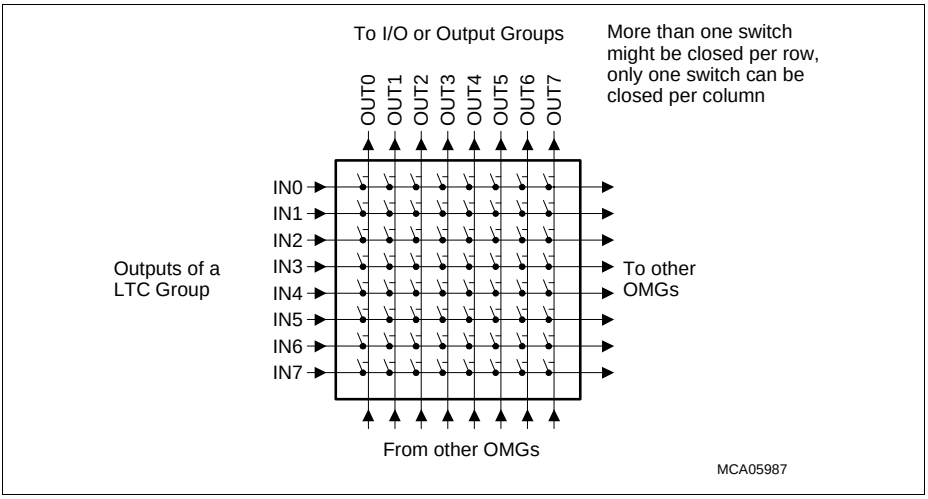


Figure 28-85 Output Multiplexer Group (OMG) Structure

Rules for connections to Output Multiplexer Group OMG:

- OMG output line OUT0 is always connected to the input of an I/O or output group with the lowest index. The remaining output lines OUT1 to OUT7 are connected to the I/O or Output lines with ascending index.
  Example: for OMG13 (see **Figure 28-84**), the outputs OUT0 to OUT7 are wired to input lines 0 to 7 of I/O group 3 (IOG3).
- One input of an I/O or output group can be connected only to the output of one timer cell. This is guaranteed by the OMG control register layout. Otherwise, short circuits and unpredictable behavior would occur. On the other hand, it is permitted that for the output of an LTC cell to be connected to more than one input of an I/O or output group.

The output multiplexer group configuration is based on the following principles:

- Each OMG is referenced with two index variables: n and g (OMGng)
- Index n is a group number. Local Timer Cell Groups LTCG[3:0] have the group number 1, and Local Timer Cell Groups LTCG[7:4] have the group number 2.
- Index g indicates the number of an I/O or output group g ($g = 3\text{-}7_D$) to which the outputs of the output multiplexer group OMGng are connected. I/O groups OG0 to OG3 are assigned to index variable g = 0 to 3 and output groups OG3 to OG6 are assigned to index variable g = 10 to 13. Index g = 4, 5, 6, 7, 8, 9 are not available.

The output multiplexer logic as seen for programming is shown in **Figure 28-86**. With this logic, one LTC group signal is always combined to one output line that leads to the

input of an I/O or output group. For example, when looking at **Figure 28-84**, each of the eight output multiplexer output lines to I/O group IOG0 is connected via two OMGs (OMG10 and OMG20) with the eight outputs of two LTC groups (LTCG0 and LTCG4).

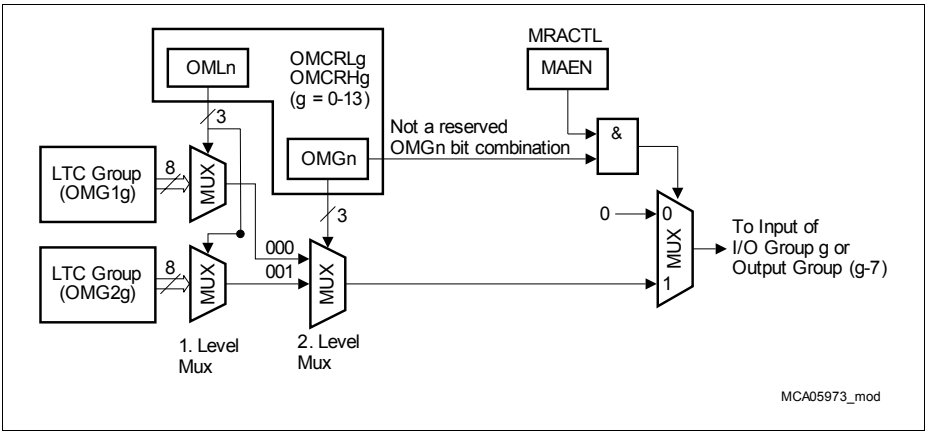


Figure 28-86 OMG Multiplexer (Programmer's View)

The 1. level multiplexer is built up by two 8:1 multiplexers that are controlled in parallel by bit field OMLn. Bit field OMGn controls the 2. level multiplexer and connects one of the 1. level multiplexer outputs to the 2. level inputs.The output of the 2. level multiplexer is connected only to the input of an I/O group or output group if bit MRACTL.MAEN (multiplexer array enabled) is set. If MRACTL.MAEN = 0, the corresponding OMG output will be held at a low level.

Two Output Multiplexer Control Registers, OMCRL and OMCRH (see also **Page 28-210**), are assigned to each of the I/O or output groups. Therefore, in total 16 registers control the connections within the output multiplexer of the LTCA unit.

The OMCRL registers control the OMG output lines 0 to 3 and the OMCRH registers control the OMG output lines 4 to 7. **Table 28-21** lists all Output Multiplexer Control Registers with its control functions. Please note that all Output Multiplexer Control Registers are not directly accessible but must be written or read using the FIFO array structure as described on **Page 28-210**.

Table 28-21 Output Multiplexer Control Register Assignments

I/O Group or Output Group		Controlled by Multiplexer Control Register	Selectable Groups via OMGng
IOG0	IN[03:00]/OUT[03:00]	OMCRL0	LTCG0 / LTCG4
	IN[07:04]/OUT[07:04]	OMCRH0	
IOG1	IN[11:08]/OUT[11:08]	OMCRL1	LTCG1 / LTCG5
	IN[15:12]/OUT[15:12]	OMCRH1	
IOG2	IN[19:16]/OUT[19:16]	OMCRL2	LTCG2 / LTCG6
	IN[23:20]/OUT[23:20]	OMCRH2	
IOG3	IN[27:24]/OUT[27:24]	OMCRL3	LTCG3 / LTCG7
	IN[31:28]/OUT[31:28]	OMCRH3	
OG0	OUT[59:56][1)]	OMCRL07	LTCG3 / LTCG7
	OUT[63:60]	OMCRH07	
OG1	OUT[67:64]	OMCRL08	LTCG0 / LTCG4
	OUT[71:68]	OMCRH08	
OG2	OUT[75:72]	OMCRL09	LTCG1 / LTCG5
	OUT[79:76]	OMCRH09	
OG3	OUT[83:80]	OMCRL10	LTCG2 / LTCG6
	OUT[87:84]	OMCRH10	
OG4	OUT[91:88]	OMCRL11	LTCG3 / LTCG7
	OUT[95:92]	OMCRH11	
OG5	OUT[99:96]	OMCRL12	LTCG0 / LTCG4
	OUT[103:100]	OMCRH12	
OG6	OUT[107:104]	OMCRL13	LTCG1 / LTCG5
	OUT[111:108]	OMCRH13	

1) OUT[55:32] is not available.

28.5.2.2 LTC Input Multiplexing Scheme

The LTC input multiplexer as shown in **Figure 28-87** and **Figure 28-89** connects the 32 (= 4 × 8) input lines of the I/O groups, the eight clock bus input lines, or the four PDL input lines PDL[3:0] and the four internal input lines INT[3:0] with the 64 (= 8 × 8) LTC inputs, organized in eight LTC groups.

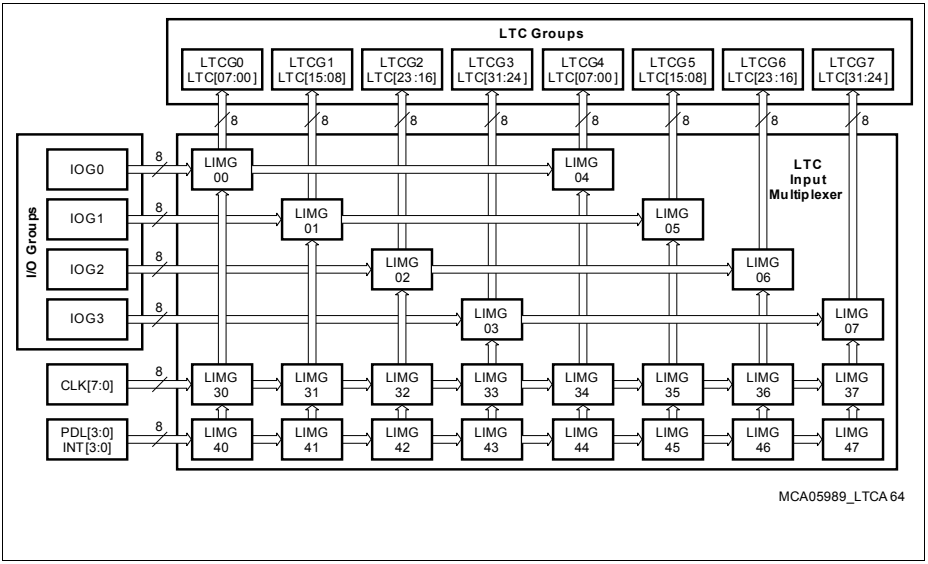


Figure 28-87 LTC Input Multiplexer of LTCA

The LTC input multiplexer contains LTC input Multiplexer Groups (LIMGs) that connect the I/O groups or the clock, PDL, or INT inputs to the input lines of the LTCs, organized in eight LTC groups with 8 cells each. IOGs are grouped into four IOGs (IOG[3:0]) with eight lines each. Two special groups are available, a clock group with eight lines representing the clock bus inputs CLK[7:0] and a PDL/INT group with eight outputs that combines the four PDL inputs and the four inputs INT[3:0] as a group of LIMGs inputs.

Figure 28-88 shows the logical structure of a LIMG.

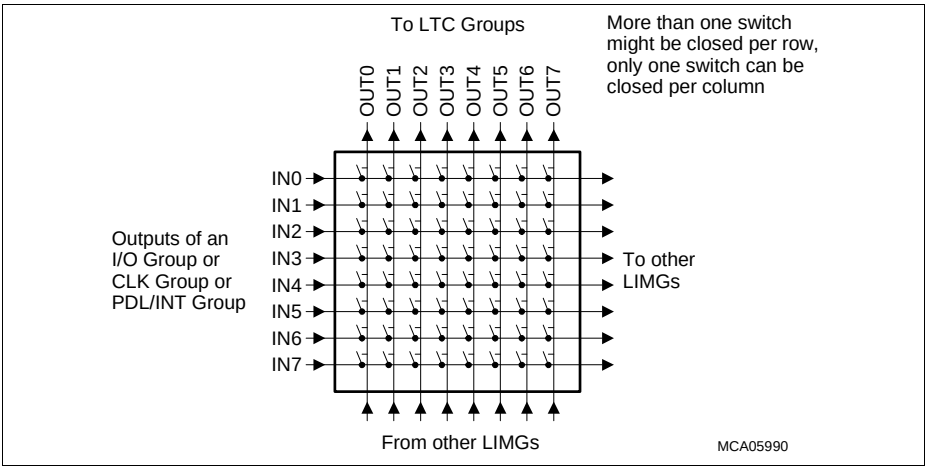


Figure 28-88 LTC Input Multiplexer Group (LIMG) Structure

Rules for connections to LTC Input Multiplexer Group LIMG:

- Within a I/O group, the line or the output of the cell with the lowest index number is connected to LIMG input line IN0. The remaining lines, cells or lines of a group are connected to LIMG input lines IN1 to IN7 with ascending index numbers. At the clock group, CLK0 is connected to IN0 and the remaining clock lines are connected to LIMG input lines IN1 to IN7 with ascending index numbers. At the PDL/INT group, PDL[3:0] (see **Page 28-22**) are connected to IN[3:0] and INT[3:0] are connected to IN[7:4].
  Example: for LIMG04 (see **Figure 28-87**), the I/O lines of IOG0 (IN00 up to IN07) are wired to its input lines IN0 to line IN7.
- Multiplexer output OUT0 of a LIMG is always connected to the input of an LTC group with the lowest index. The remaining output lines OUT1 to OUT7 are connected to the LTC inputs with ascending index.
  Example: for LIMG04 (see **Figure 28-87**), the outputs OUT0 to OUT7 are wired to the inputs of LTC32 to LTC39.
- An LTC input can be connected either to an I/O group output, or to a clock bus output, or to an PDL/INT output. This is guaranteed by the LIMG control register layout.

Otherwise, short circuits and unpredictable behavior would occur. In contrast, it is permitted that an I/O group output, or to a clock bus output, or a PDL/INT output is connected to more than one LTC input.

The LTC input multiplexer group configuration is based on the following principles:

- Each LIMG is referenced with two index variables: n and g (LIMGng)
- Index n is a group number. I/O groups IOG[3:0] have group number 0, I/O group IOG4 is not implemented, clock bus lines CLK[7:0] have group number 3, and the PDL/INT group has group number 4.
- Index g indicates the number of the LTC group g (g = 0-7) to which the outputs of the input multiplexer group LIMGng are connected.

The LTC input multiplexer logic as seen for programming is shown in **Figure 28-89**. With this logic, three group signals (from I/O groups, clock group, or PDL/INT group) are always combined to one output line that leads to an LTC input of LTC group g. For example, when looking at **Figure 28-87**, each of the eight LTC input multiplexer output lines to LTC group LTCG2 is connected via three LIMGn2 (n = 0, 3, 4) to the eight outputs of I/O group IOG2, the clock group, and the PDL/INT group.

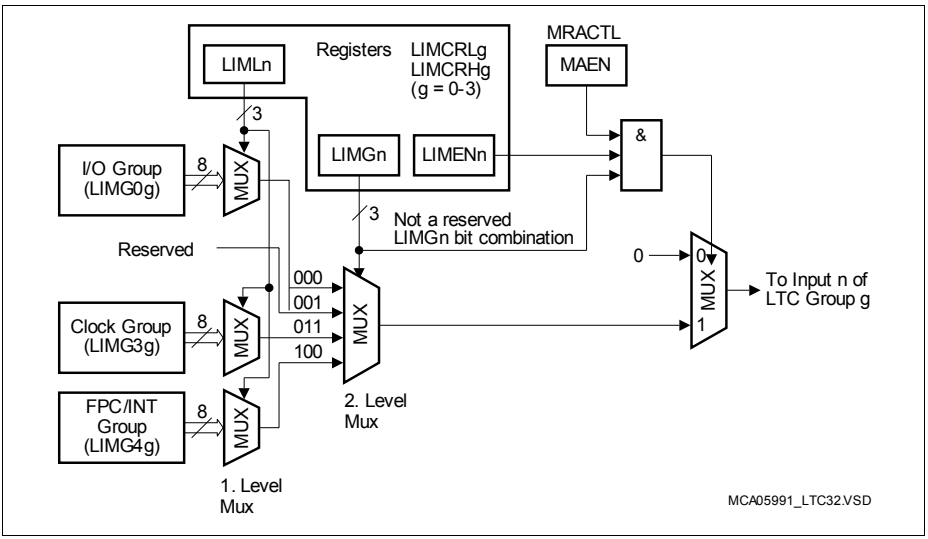


Figure 28-89 LTC Input Multiplexer (Programmer's View)

The 1. level multiplexer is built up by four three 8:1 multiplexers that are controlled in parallel by bit field LIMLn. The output of the multiplexer is connected only to the input of an LTC if bit LIMENn is set (enable multiplexer connection), and bit MRACTL.AEN is set (multiplexer array enabled), and no reserved bit combination is selected. If one of these conditions is not true, the corresponding LTC input will be held at a low level.

Two LTC Input Multiplexer Control Registers, LIMCRL (see also Page 28-271 and Page 28-272), are assigned to each of the LTC groups. Therefore, in total sixteen registers control the connections within the LTC input multiplexer of the LTCA unit.

The LIMCRL registers control the LIMG output lines 0 to 3 and the LIMCRH registers control the LIMG output lines 4 to 7. Table 28-22 lists all LTC Input Multiplexer Control Registers with its control functions. Please note that all LTC Input Multiplexer Control Registers are not directly accessible but must be written or read using a FIFO array structure as described on Page 28-121.

Table 28-22 LTC Input Multiplexer Control Register Assignments

LTC Group and LTCs		Controlled by Register	Selectable Groups via LIMGng
LTCG0	LTC[03:00]	LIMCRL0	IOG0, CLOCK, PDL/INT
	LTC[07:04]	LIMCRH0	
LTCG1	LTC[11:08]	LIMCRL1	IOG1, CLOCK, PDL/INT
	LTC[15:12]	LIMCRH1	
LTCG2	LTC[19:16]	LIMCRL2	IOG2, CLOCK, PDL/INT
	LTC[23:20]	LIMCRH2	
LTCG3	LTC[27:24]	LIMCRL3	IOG3, CLOCK, PDL/INT
	LTC[31:28]	LIMCRH3	
LTCG4	LTC[35:32]	LIMCRL4	IOG0, CLOCK, PDL/INT
	LTC[39:36]	LIMCRH4	
LTCG5	LTC[43:40]	LIMCRL5	IOG1, CLOCK, PDL/INT
	LTC[47:44]	LIMCRH5	
LTCG6	LTC[51:48]	LIMCRL6	IOG2, CLOCK, PDL/INT
	LTC[55:52]	LIMCRH6	
LTCG7	LTC[59:56]	LIMCRL7	IOG3, CLOCK, PDL/INT
	LTC[63:60]	LIMCRH7	

28.5.2.3 Multiplexer Register Array Programming

A total of 38 control registers are required to program the configuration of the output multiplexer and the LTC input multiplexer of the Input/Output Line Sharing Block. These IOLS control registers are combined into a Multiplexer Register Array FIFO that can only be read or written sequentially. Therefore, the control registers values cannot be accessed directly but must be accessed in a specific sequential order.

Three registers are available for controlling the Multiplexer Register Array:

- Multiplexer Register Array Control Register MRACTL

- Multiplexer Register Array Data Out Register MRADOUT
- Multiplexer Register Array Data In Register MRADIN

Figure 28-90 shows the structure of the multiplexer array FIFO with the arrangement of the multiplexer control registers.

For programming of the multiplexer array FIFO, the following steps must be executed:

1. Disable interconnections of the multiplexer array by writing MRACTL.MAEN = 0 (default after reset). The multiplexer array is disabled, all cell input lines are driven with 0, and device pins assigned to LTCA I/O lines or output lines are disconnected.
2. Reset the write cycle counter to 0 by writing MRACTL.WCRES = 1.
3. Write sequentially the multiplexer control register contents one after the other (38 values) into MRADIN, starting with the register values for OMCRH10, OMCRL10, … up to LIMCRH0, LIMCRL0 (see **Figure 28-90**). After the first MRADIN write operation, the contents for OMCRH10 is at FIFO position 1. With each following MRADIN write operation, it becomes shifted one FIFO position upwards. After the 38. MRADIN write operation, the OMCRH10 value is at its final position. The contents of FIFO position 38 can be read via register MRADOUT. With each MRADIN write operation the write cycle counter MRACTL.FIFOFILLCNT is incremented by 1. After all FIFO entries have been written, the FIFO is locked, bit MRACTL.FIFOFULL is set, and further MRADIN write operations are discarded until bit MRACTL.WCRES is written again with a 0.
4. Enable the multiplexer array by writing MRACTL.MAEN = 1. This establishes and enables all programmed interconnections.

To check the FIFO contents, the FIFO can be written a second time. At this check MRADIN is written before MRADOUT is read. This will return the FIFO contents of the first write sequence in the order of OMCRH10, OMCRL10, …, LIMCRL0.

Before disabling the multiplexer array FIFO, LTCA output pins that are already enabled as LTCA output should be switched to GPIO function to avoid output spikes. After enabling the multiplexer array FIFO again, the LTCA output can be switched again back to LTCA output function.

Shifting the write data through the FIFO requires a few clock cycles. When new data becomes written before the FIFO is ready to accept them, wait states will be inserted into the write access.

If the OMCRLg register bit field OMGn of the multiplexer array is programmed with an invalid (reserved) value, the related outputs will be forced to 0. When the array is disabled (MRACTL.MAEN = 0), all cell inputs and outputs are disconnected from the GPIO lines and are driven with 0.

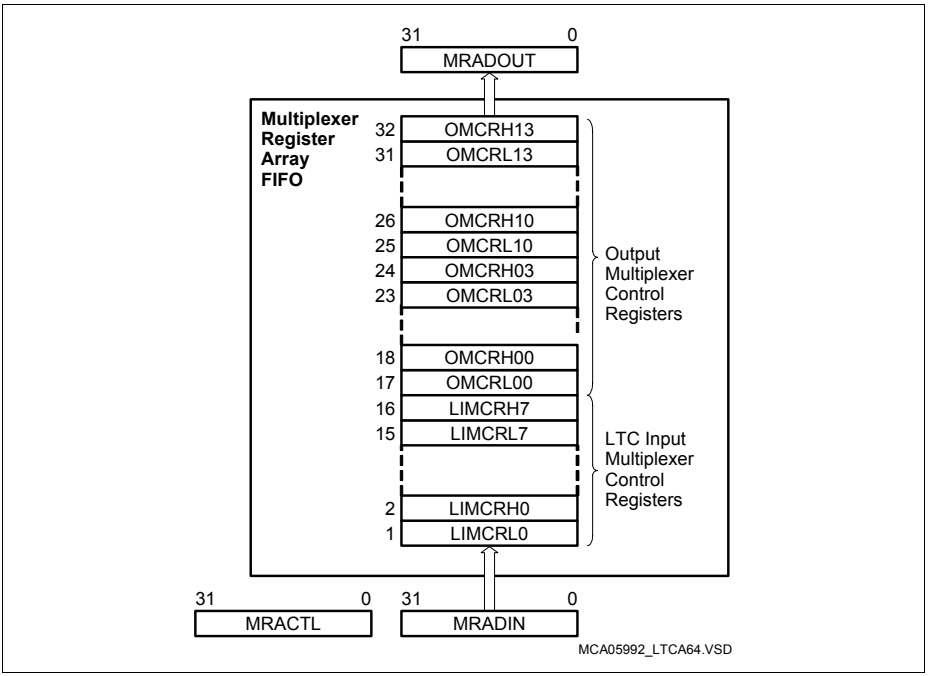


Figure 28-90 LTCA Multiplexer Array Control Register FIFO Structure

28.5.3 Interrupt Sharing Block (IS)

The LTCA provides 16 service request sources. These service request sources are generated by the LTCs.

Table 28-23 LTCA Number of Service Request Sources

Cell Type	Number of Cells	Number of Service Request Sources/Cell	Total Number of Request Sources
LTC	64	1	16

To reduce hardware and software overhead, four request sources are combined together in service request groups. A service request group y (y = 00-15) has four service request inputs and one service request output SRy which is typically connected outside the LTCA kernel to a standard interrupt node y and controlled by its SRCy register.

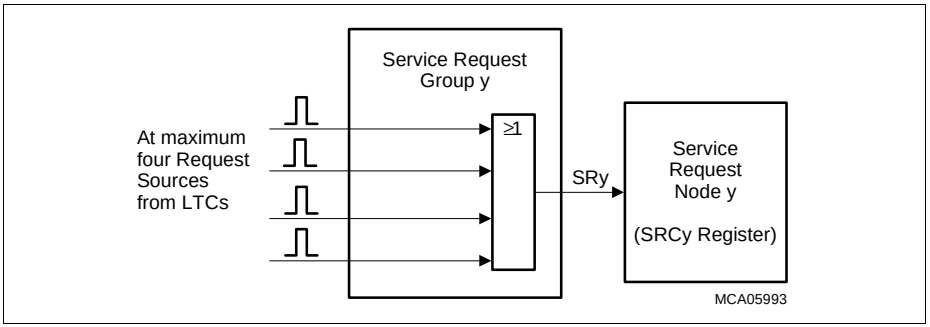


Figure 28-91 Service Request Groups

The bits in the Service Request State Registers (SRSSx and SRSCx, x = 3, 2) are service request status flags that are set by hardware (type “h”) when the related event occurs. Each LTCA service request source has its own service request flag. This flag is normally set by hardware but can be set and reset by software. Each service request status flag can be read twice, at the same bit location in SRSCx register and in SRSSx register, and cleared or set by software when writing to the corresponding request bit in SRSCx or SRSSx. When writing to SRSCx or SRSSx, several flags can be cleared at once by one write operation. Flags written with 0 are not influenced. This feature allows fast, simple clearing or setting of request flags without affecting other bits in the same register.

Note that the service request flag is always set by the service request event even if the corresponding service request is disabled in the interrupt node.

Table 28-24 lists the interrupt requests used by LTCA.

Table 28-24 LTCA Service Request Groups

Service Request Group Number	Source 1	Source 2	Source 3	Source 4
00	LTC00	LTC01	LTC02	LTC03
01	LTC04	LTC05	LTC06	LTC07
02	LTC08	LTC09	LTC10	LTC11
03	LTC12	LTC13	LTC14	LTC15
04	LTC16	LTC17	LTC18	LTC19
05	LTC20	LTC21	LTC22	LTC23
06	LTC24	LTC25	LTC26	LTC27
07	LTC28	LTC29	LTC30	LTC31
08	LTC32	LTC33	LTC34	LTC35
09	LTC36	LTC37	LTC38	LTC39
10	LTC40	LTC41	LTC42	LTC43
11	LTC44	LTC45	LTC46	LTC47
12	LTC48	LTC49	LTC50	LTC51
13	LTC52	LTC53	LTC54	LTC55
14	LTC56	LTC57	LTC58	LTC59
15	LTC60	LTC61	LTC62	LTC63

28.6 LTCA Kernel Registers

This section describes the LTCA kernel registers. Some of the kernel registers (SRSCn, SRSSn, LTCCTRk, and LTCXRk) are already described as GPTA®v5 kernel register at the pages as referenced in column “Description see” of **Table 28-25**. The multiplexer array FIFO registers are LTCA specific and therefore defined on the next pages.

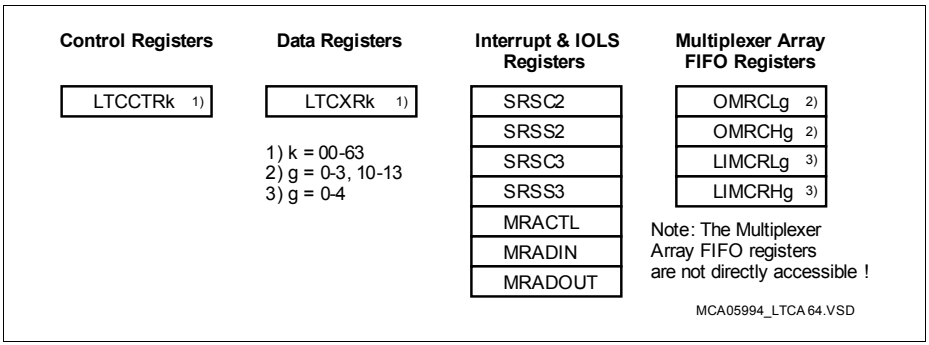


Figure 28-92 LTCA2 Kernel Registers

Table 28-25 LTCA2 Kernel Registers

Register Short Name	Register Long Name	Offset Addr.	Access Mode		Reset Class	Description see
			Read	Write		
ID	LTCA Identification Register	0008_H	U, SV	nBE	1	**Page 28-166**
SRSC2	Service Request State Clear Register 2	0020_H	U, SV	SV, E	3	**Page 28-228**
SRSS2	Service Request State Set Register 2	0024_H	U, SV	SV, E	3	**Page 28-229**
SRSC3	Service Request State Clear Register 3	0028_H	U, SV	SV, E	3	**Page 28-230**
SRSS3	Service Request State Set Register 3	$002C_H$	U, SV	SV, E	3	**Page 28-231**
MRACTL	Multiplexer Register Array Control Register	0038_H	U, SV	U, SV	3	**Page 28-264**
MRADIN	Multiplexer Register Array Data In Register	$003C_H$	U, SV, 32	U, SV, 32	3	**Page 28-266**

Table 28-25 LTCA2 Kernel Registers (cont'd)

Register Short Name	Register Long Name	Offset Addr.	Access Mode		Reset Class	Description see
			Read	Write		
MRADOUT	Multiplexer Register Array Data Out Register	0040_H	U, SV, 32	U, SV, 32	3	Page 28-266
LTCCTRk	Local Timer Cell Control Register k (k = 00-62)	$0200_H + k \times 8$	U, SV	U, SV	3	Page 28-252 Page 28-255 Page 28-258
LTCXRk	Local Timer Cell X Register k (k = 00-62)	$0204_H + k \times 8$	U, SV	U, SV	3	Page 28-263
LTCCTR63	Local Timer Cell Control Register 63	$0200_H + 63 \times 8$	U, SV	U, SV	3	Page 28-261
LTCXR63	Local Timer Cell X Register 63	$0204_H + 63 \times 8$	U, SV	U, SV	3	Page 28-263
OMCRLg	Output Multiplexer Control Register for Lower Half of Group g (g = 0-3, 10-13)	not directly address-able see Page 28-245	n.a.	n.a.	3	Page 28-268
OMCRHg	Output Multiplexer Control Register for Upper Half of Group g (g = 0-3, 10-13)		n.a.	n.a.	3	Page 28-269
LIMCRLg	Input Multiplexer Control Register for Lower Half of LTC Group g (g = 0-7)	not directly address-able see Page 28-245	n.a.	n.a.	3	Page 28-271
LIMCRHg	Input Multiplexer Control Register for Upper Half of LTC Group g (g = 0-7)		n.a.	n.a.	3	Page 28-272

28.6.1 Bit Protection

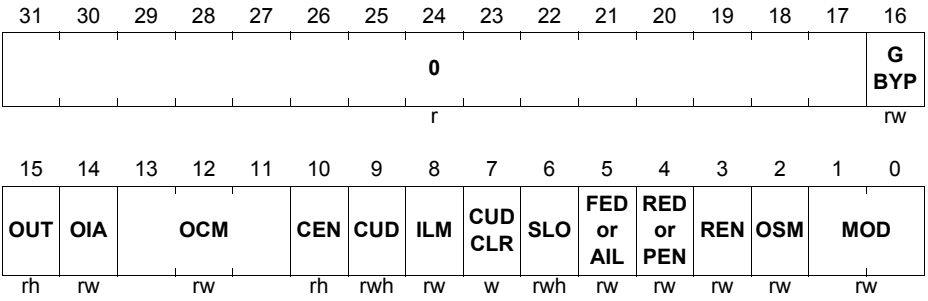
Bits with bit protection (this is valid, for example, for all bits in the Service Request State Registers) are not changed during a read-modify-write instruction, that is when hardware sets a request state bit between the read and the write of the read-modify-write sequence. For bit protected bits it is guaranteed that a hardware setting operation always has priority. Thus, no hardware triggered events are lost.

28.6.2 Service Request Registers

See **"GPTA0_SRSC2" on Page 28-228**.

28.6.3 Local Timer Cell Registers

LTCA2_LTCCTRk (k = 00-62)
Local Timer Cell Control Register k [Timer Mode]
(200_H+k*8_H) **Reset Value: 0000 0000_H**



Field	Bits	Type	Description
MOD	[1:0]	rw	**Mode Control Bits** 00_B LTCk operates in Capture Mode 01_B LTCk operates in Compare Mode 10_B LTCk operates in Free-Running Timer Mode 11_B LTCk operates in reset Timer Mode
OSM	2	rw	**One Shot Mode Enable** 0_B LTCk is continuously enabled 1_B LTCk is enabled for one event only
REN	3	rw	**Request Enable** 0_B Service request is disabled. 1_B Service request SQSk is activated when a - capture event has occurred - compare event has occurred - timer overflow has happened depending on the operation mode selected by bit field MOD.

Field	Bits	Type	Description
RED	4	rw	**ILM = 0: Input Rising Edge Select** 0_B Timer is not updated by a rising edge 1_B Timer is updated by a rising edge on the LTCkIN input line
PEN	4	rw	**ILM = 1: LTC Prescaler Enable** 0_B LTC Prescaler Mode is disabled 1_B LTC Prescaler Mode with LTC prescaler clock LTCPRE is enabled
FED	5	rw	**ILM = 0: Input Falling Edge Select** 0_B Timer is not updated by a falling edge 1_B Timer is updated by a falling edge on the LTCkIN input line
AIL	5	rw	**ILM = 1: Active Input Level Select** 0_B Input signal is active high 1_B Input signal is active low
SLO	6	rwh	**Select Line Output** 0_B State of select line output SO is 0 1_B State of select line output SO is 1 SLO is bit protected (see **Page 28-167**).
CUDCLR	7	w	**Coherent Update Disable** 0_B No effect 1_B Coherent update disabled (bit CUD is cleared) If bits CUD and CUDCLR are both written with 1, bit CUD will be set. CUDCLR is always read as 0.
ILM	8	rw	**Input Line Mode** 0_B Input line is operating in Edge Sensitive Mode. 1_B Input line is operating in Level Sensitive Mode. In case of full speed GPTA®v5 module clock selection as input clock, Level Sensitive Mode must be selected. In this case the Edge Sensitive Mode will not produce any event.
CUD	9	rwh	**Coherent Update Enable** 0_B Select output SO is not toggled on timer reset overflow 1_B Select output SO is toggled on next timer reset overflow When CUD is set by software (writing CUD and CUDCLR both with 1), it remains set until the next timer reset overflow (LTCk reset event) occurs and is cleared by hardware afterwards. CUD can be reset by software by writing bit CUDCLR with 1 and CUD with 0.

Field	Bits	Type	Description
CEN	10	rh	**Cell Enable** 0_B LTCk is currently disabled for local events 1_B LTCk is currently enabled for local events
OCM	[13:11]	rw	**Output Control Mode Select** 000_B Current state of LTCkOUT output line is hold 001_B Current state of LTCkOUT output line is toggled by an internal LTCk event otherwise hold 010_B LTCkOUT output line is forced to 0 by an internal LTCk event otherwise hold 011_B LTCkOUT output line is forced to 1 by an internal LTCk event otherwise hold $1XX_B$ LTCkOUT output line state is affected by an internal LTCk event and/or by an operation occurred in an adjacent LTCk cell (reported by M1I/M0I interface lines)
OIA	14	rw	**Output Immediate Action** 0_B No immediate action required 1_B Action defined by bit field OCM must be performed immediately OIA is always read as 0.
OUT	15	rh	**Output State** 0_B LTCkOUT output line is 0 1_B LTCkOUT output line is 1
GBYP	16	rw	**Global Bypass** 0_B M3O/M2O lines are affected by M1I/M0I lines 1_B M3O/M2O lines are affected by M3I/M2I lines
0	[31:17]	r	**Reserved** Read as 0; should be written with 0.

LTCA2_LTCCTRk (k = 00-62)
Local Timer Cell Control Register k [Capture Mode]
(200_H+k*8_H) **Reset Value: 0000 0000_H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															GBYP
r															rw

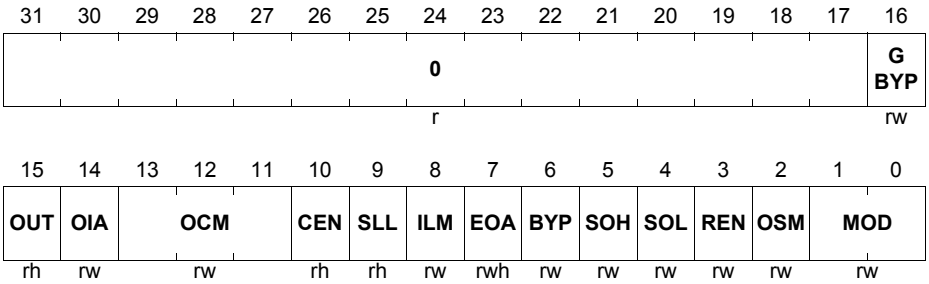
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
OUT	OIA	OCM			CEN	SLL	ILM	EOA	BYP	FED	RED	REN	OSM	MOD	
rh	rw	rw			rh	rh	rw	rwh	rw	rw	rw	rw	rw	rw	

Field	Bits	Type	Description
MOD	[1:0]	rw	**Mode Control Bits** 00_B LTCk operates in Capture Mode. 01_B LTCk operates in Compare Mode. 10_B LTCk operates in Free-Running Timer Mode. 11_B LTCk operates in reset Timer Mode.
OSM	2	rw	**One Shot Mode Enable** 0_B LTCk is continuously enabled. 1_B LTCk is enabled for one event only.
REN	3	rw	**Request Enable** 0_B Service request is disabled. 1_B Service request SQSk is activated when a - capture event has occurred - compare event has occurred - timer overflow has happened depending on the operation mode selected by bit field MOD.
RED	4	rw	**Input Rising Edge Select** 0_B Capture event is not triggered by a rising edge. 1_B Capture event is triggered by a rising edge on the LTCkIN input line.
FED	5	rw	**Input Falling Edge Select** 0_B Capture event is not triggered by a falling edge. 1_B Capture event is triggered by a falling edge on the LTCkIN input line.

Field	Bits	Type	Description
BYP	6	rw	**Local Bypass** 0_B M1O/M0O lines are affected either by M1I/M0I lines or by OCM1/OCM0 bits. 1_B M1O/M0O lines are affected only by M1I/M0I (GBYP = 0) or M2I/M2I (GBYP = 1) lines. This bit is cleared if mode is switched to Timer Mode. OCM2 must be set in any case to enable reaction on M1I/M0I change.
EOA	7	rwh	**Enable On Action** 0_B LTCk is enabled for local events. 1_B LTCk is disabled for local events. On an event on the communication link via M0I/M1I lines, EOA will be cleared and local events will be enabled. EOA is bit protected (see **Section 28.4.2**). EOA is cleared if mode is switched to Timer Mode.
ILM	8	rw	**Input Line Mode** 0_B Input line is operating in Edge Sensitive Mode. 1_B Input line is operating in Level Sensitive Mode. In case of full speed GPTA®v5 module clock selection as input clock, Level Sensitive Mode must be selected. In this case the Edge Sensitive Mode will not produce any event.
SLL	9	rh	**Capture & Compare Mode: Select Line Level** 0_B Current state of select input SI is 0. 1_B Current state of select input SI is 1.
CEN	10	rh	**Cell Enable** 0_B LTCk is currently disabled for local events. 1_B LTCk is currently enabled for local events.
OCM	[13:11]	rw	**Output Control Mode Select** 000_B Current state of LTCkOUT output line is hold 001_B Current state of LTCkOUT output line is toggled by an internal LTCk event otherwise hold 010_B LTCkOUT output line is forced to 0 by an internal LTCk event otherwise hold 011_B LTCkOUT output line is forced to 1 by an internal LTCk event otherwise hold $1XX_B$ LTCkOUT output line state is affected by an internal LTCk event and/or by an operation occurred in an adjacent LTCk cell (reported by M1I/M0I interface lines).

Field	Bits	Type	Description
OIA	14	rw	**Output Immediate Action** 0_B No immediate action required. 1_B Action defined by bit field OCM must be performed immediately. OIA is always read as 0.
OUT	15	rh	**Output State** 0_B LTCkOUT output line is 0. 1_B LTCkOUT output line is 1.
GBYP	16	rw	**Global Bypass** 0_B M3O/M2O lines are affected by M1I/M0I lines. 1_B M3O/M2O lines are affected by M3I/M2I lines.
0	[31:17]	r	**Reserved** Read as 0; should be written with 0.

LTCA2_LTCCTRk (k = 00-62)
Local Timer Cell Control Register k [Compare Mode]
(200_H+k*8_H) **Reset Value: 0000 0000_H**



Field	Bits	Type	Description
MOD	[1:0]	rw	**Mode Control Bits** 00_B LTCk operates in Capture Mode. 01_B LTCk operates in Compare Mode. 10_B LTCk operates in Free-Running Timer Mode. 11_B LTCk operates in reset Timer Mode.
OSM	2	rw	**One Shot Mode Enable** 0_B LTCk is continuously enabled. 1_B LTCk is enabled for one event only.
REN	3	rw	**Request Enable** 0_B Service request is disabled. 1_B Service request SQSk is activated when a - capture event has occurred - compare event has occurred - timer overflow has happened depending on the operation mode selected by bit field MOD.
SOL	4	rw	**Compare Mode: Select Output Low** 0_B Compare is deactivated or on high level. 1_B Compare operation is enabled by a low level on select input SI[1)].
SOH	5	rw	**Compare Mode: Select Output High** 0_B Compare is deactivated or on high level. 1_B Compare operation is enabled by a high level on select input SI[1)].

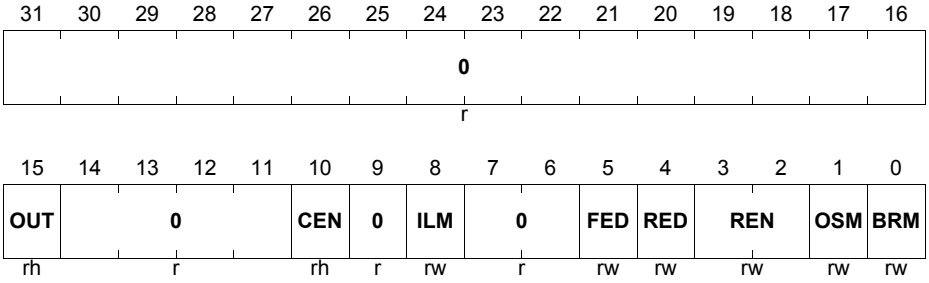
Field	Bits	Type	Description
BYP	6	rw	**Bypass** 0_B M1O/M0O lines are affected either by M1I/M0I lines or by OCM1/OCM0 bits. 1_B M1O/M0O lines are affected only by M1I/M0I lines. This bit is cleared if mode is switched to Timer Mode. OCM2 must be set in any case to enable reaction on M1I/M0I change.
EOA	7	rwh	**Enable On Action** 0_B LTCk is enabled for local events. 1_B LTCk is disabled for local events. On an event on the communication link via M0I/M1I lines, EOA will be cleared and local events will be enabled. EOA is bit protected (see **Section 28.4.2**). EOA is cleared if mode is switched to Timer Mode.
ILM	8	rw	**Input Line Mode** 0_B Input line is operating in Edge Sensitive Mode. 1_B Input line is operating in Level Sensitive Mode. In case of full speed GPTA®v5 module clock selection as input clock, Level Sensitive Mode must be selected. In this case the Edge Sensitive Mode will not produce any event.
SLL	9	rh	**Select Line Level** 0_B Current state of select input SI is 0. 1_B Current state of select input SI is 1.
CEN	10	rh	**Cell Enable** 0_B LTCk is currently disabled for local events. 1_B LTCk is currently enabled for local events.
OCM	[13:11]	rw	**Output Control Mode Select** 000_B Current state of LTCkOUT output line is hold 001_B Current state of LTCkOUT output line is toggled by an internal LTCk event otherwise hold 010_B LTCkOUT output line is forced to 0 by an internal LTCk event otherwise hold 011_B LTCkOUT output line is forced to 1 by an internal LTCk event otherwise hold $1XX_B$ LTCkOUT output line state is affected by an internal LTCk event and/or by an operation occurred in an adjacent LTCk cell (reported by M1I/M0I interface lines).

Field	Bits	Type	Description
OIA	14	rw	**Output Immediate Action** 0_B No immediate action required. 1_B Action defined by bit field OCM must be performed immediately. OIA is always read as 0.
OUT	15	rh	**Output State** 0_B LTCkOUT output line is 0. 1_B LTCkOUT output line is 1.
GBYP	16	rw	**Global Bypass** 0_B M3O/M2O lines are affected by M1I/M0I lines. 1_B M3O/M2O lines are affected by M3I/M2I lines.
0	[31:17]	r	**Reserved** Read as 0; should be written with 0.

1) To enable Compare Mode in all cases, SOL and SOH bits must be set to 1.

LTCA2_LTCCTR63

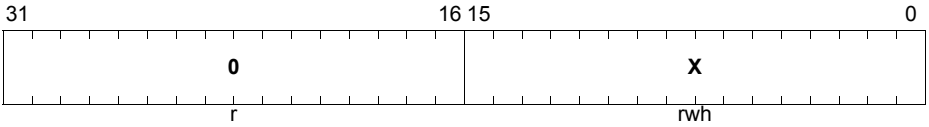
Local Timer Cell Control Register 63 ($3F8_H$) **Reset Value: $0000\ 0000_H$**



Field	Bits	Type	Description
BRM	0	rw	**Bit Reversal Mode Control** 0_B Compare uses normal sequence of local input data bus (YI) bits. 1_B Compare uses reversed sequence of local input data bus (YI) bits.
OSM	1	rw	**One Shot Mode Enable for Shadow Register Copy** 0_B Shadow register copy is continuously enabled. 1_B Shadow register copy is enabled for one event only.
REN	[3:2]	rw	**Request Enable** 00_B Service request SQT63 is disabled. 01_B Service request SQT63 is generated when a compare event has occurred. 10_B Service request SQT63 is generated when a shadow register copy event has occurred. 11_B Reserved.
RED	4	rw	**Rising Edge Select for Shadow Register Copy** 0_B Shadow register copy is not triggered by a rising edge on the LTC63IN input line. 1_B Shadow register copy is triggered by a rising edge on the LTC63IN input line.
FED	5	rw	**Falling Edge Select for Shadow Register Copy** 0_B Shadow register copy is not triggered by a falling edge on the LTC63IN input line. 1_B Shadow register copy is triggered by a falling edge on the LTC63IN input line.

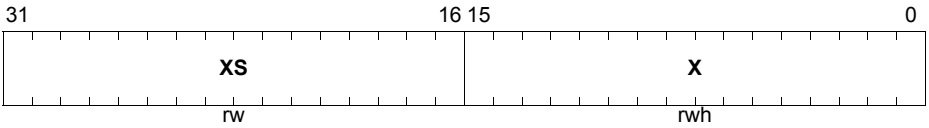
Field	Bits	Type	Description
ILM	8	rw	**Shadow Register Copy Input Line Mode** 0_B LTC63IN is operating in Edge Sensitive Mode. 1_B LTC63IN is operating in Level Sensitive Mode.
CEN	10	rh	**Enable for Shadow Register Copy** 0_B Shadow register copy is currently disabled. 1_B Shadow register copy is currently enabled.
OUT	15	rh	**Output State** 0_B LTC63OUT output line is 0. 1_B LTC63OUT output line is 1.
0	[7:6], 9, [14:11], [31:16]	r	**Reserved** Read as 0; should be written with 0.

LTCA2_LTCXRk (k = 00-62)
Local Timer Cell X Register k **(204_H+k*8_H)** **Reset Value: 0000 0000_H**



Field	Bits	Type	Description
X	[15:0]	rwh	**Local Timer Data Register Value**
0	[31:16]	r	**Reserved** Read as 0; should be written with 0.

LTCA2_LTCXR63
Local Timer Cell X Register 63 **($3FC_H$)** **Reset Value: 0000 0000_H**



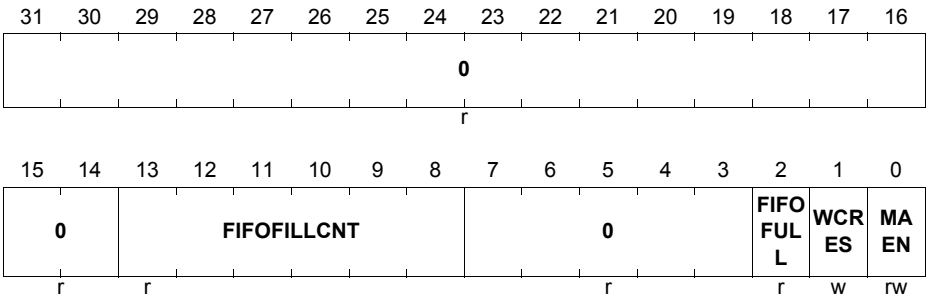
Field	Bits	Type	Description
X	[15:0]	rwh	**Compare Register Value** Software write operations has priority above a simultaneous hardware update.
XS	[31:16]	rw	**Shadow Register Value**

28.6.4 I/O Sharing Block Registers

The three registers MRACTL, MRADIN, and MRADOUT are used to write data to and read data from the LTCA Multiplexer Register Array FIFO. The Multiplexer Register Array FIFO controls the operation of the Input/Output Line Sharing Block (see **“Input/Output Line Sharing Block (IOLS)” on Page 28-98**).

The Multiplexer Register Array Control register controls the operation of the Multiplexer Register Array FIFO.

LTCA2_MRACTL
Multiplexer Register Array Control Register
(038_H) **Reset Value: $0000\ 0000_H$**

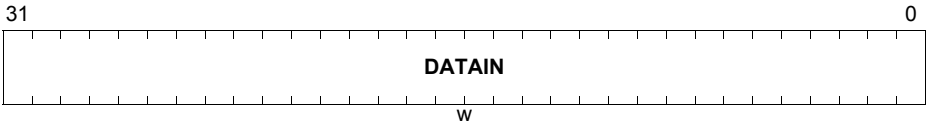


Field	Bits	Type	Description
MAEN	0	rw	**Multiplexer Array Enable** Bit field MAEN enables/disables the programming and the interconnections of the multiplexer array. 0_B Multiplexer array is disabled; all cell inputs are driven with 0, LTCA I/O lines (pins) are disconnected and FIFO writing is enabled. 1_B Multiplexer array is enabled; all cell and I/O line interconnections are established as previously programmed and FIFO writing is disabled.
WCRES	1	w	**Write Count Reset** Writing WCRES with 1 while the array is disabled (MAEN = 0), resets the write cycle counter to zero and the FIFO written sequentially (initialized). WCRES is always read as 0.
FIFOFULL	2	r	**FIFO Full Status** 0_B FIFO not completely written (write access to MRADIN allowed). 1_B FIFO completely written (write access to MRADIN ignored). Must be re-enabled via WCRES before array can be re-initialized.

Field	Bits	Type	Description
FIFOFILLCNT	[13:8]	r	**FIFO Fill Count** This bit field shows the current contents of the write cycle counter.
0	[7:3], [31:14]	r	**Reserved** Read as 0; should be written with 0.

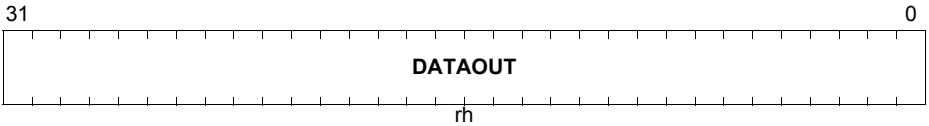
The Multiplexer Register Array Data In register is used to **write** data to the Multiplexer Register Array FIFO. The Multiplexer Register Array Data Out register is used to **read** data from the Multiplexer Register Array FIFO.

LTCA2_MRADIN
Multiplexer Register Array Data In Register
($03C_H$) **Reset Value: 0000 0000$_H$**



Field	Bits	Type	Description
DATAIN	[31:0]	w	**FIFO Write Data** This register contains the FIFO write data as defined for the LTC Output Multiplexer Control Registers and the LTC Input Multiplexer Control Registers.

LTCA2_MRADOUT
Multiplexer Register Array Data Out Register
(040_H) **Reset Value: 0000 0000$_H$**



Field	Bits	Type	Description
DATAOUT	[31:0]	rh	**FIFO Read Data** This register contains the FIFO read data as assigned for the LTC Output Multiplexer Control Registers and the LTC Input Multiplexer Control Registers.

Note: For correct operation, the MRADIN and MRADIN registers must be always read or written 32-bit wide. 8-bit and 16-bit accesses are ignored without any bus error!

28.6.5 Multiplexer Control Registers

These registers are not directly accessible and can be written and read only via the multiplexer register array FIFO (see **Page 28-121**).

28.6.5.1 Output Multiplexer Control Registers

Two registers, OMCRL and OMCRH, are assigned to each I/O Group IOG[3:0] and each Output Group OG[3:0]. OMCRL[3:0]/OMCRH[3:0] are assigned to IOG[3:0] and OMCRL[13:10]/OMCRH[13:10] are assigned to OG[6:3].

OMCRL controls the connections of group pins 0 to 3. OMCRH controls the connections of group pins 4 to 7.

LTCA2_OMCRLg (g = 0-3, 10-13)
Output Multiplexer Control Register for Lower Half of Pin Group g

Reset Value: 0000 0000$_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	OMG3			0	OML3			0	OMG2			0	OML2		
r	rw			r	rw			r	rw			r	rw		

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	OMG1			0	OML1			0	OMG0			0	OML0		
r	rw			r	rw			r	rw			r	rw		

Field	Bits	Type	Description
OML0, OML1, OML2, OML3	[2:0], [10:8], [18:16], [26:24]	rw	**Multiplexer Line Selection** This bit field selects the input line of a OMG that can be selected by bit field OMGn for OMG output n. 000_B OMG input IN0 selected 001_B OMG input IN1 selected 010_B OMG input IN2 selected 011_B OMG input IN3 selected 100_B OMG input IN4 selected 101_B OMG input IN5 selected 110_B OMG input IN6 selected 111_B OMG input IN7 selected
OMG0, OMG1, OMG2, OMG3	[6:4], [14:12], [22:20], [30:28]	rw	**Multiplexer Group Selection** This bit field determines the OMGng which is connected to input n of I/O Group g or Output group g-7. $X00_B$ OMG2g selected $X01_B$ OMG1g selected All other combinations are reserved. If a reserved combination of OMGn value is selected, the corresponding OMG output is forced to 0 level. For compatibility reasons, the value 001_B (for $XX1_B$) should be used for OMGn bit field programming.
0	3, 7, 11, 15, 19, 23, 27, 31	r	**Reserved** Read as 0; should be written with 0.

LTCA2_OMCRHg (g = 0-3, 10-13)
Output Multiplexer Control Register for Upper Half of Pin Group g

Reset Value: 0000 0000$_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	**OMG7**			**0**	**OML7**			**0**	**OMG6**			**0**	**OML6**		
r	rw			r	rw			r	rw			r	rw		

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	**OMG5**			**0**	**OML5**			**0**	**OMG4**			**0**	**OML4**		
r	rw			r	rw			r	rw			r	rw		

Field	Bits	Type	Description
OML4, OML5, OML6, OML7	[2:0], [10:8], [18:16], [26:24]	rw	**Multiplexer Line Selection** This bit field selects the input line of a OMG that can be selected by bit field OMGn for OMG output n. 000_B OMG input IN0 selected 001_B OMG input IN1 selected 010_B OMG input IN2 selected 011_B OMG input IN3 selected 100_B OMG input IN4 selected 101_B OMG input IN5 selected 110_B OMG input IN6 selected 111_B OMG input IN7 selected
OMG4, OMG5, OMG6, OMG7	[6:4], [14:12], [22:20], [30:28]	rw	**Multiplexer Group Selection** This bit field determines the OMGng which is connected to input n of I/O Group g or Output group g-7. $X00_B$ OMG2g selected $X01_B$ OMG1g selected All other combinations are reserved and if selected, the corresponding OMG output is forced to 0 level. For compatibility reasons, the value 001_B (for $XX1_B$) should be used for OMGn bit field programming.
0	3, 7, 11, 15, 19, 23, 27, 31	r	**Reserved** Read as 0; should be written with 0.

28.6.5.2 LTC Input Multiplexer Control Registers

Two registers, LIMCRL and LIMCRH, are assigned to each LTC group. LIMCRL controls the connections of LTC group cells with index 0 to 3. LIMCRH controls the connections of LTC group cells with index 4 to 7.

LTCA2_LIMCRLg (g = 0-7)

Input Multiplexer Control Register for Lower Half of LTC Group g

Reset Value: 0000 0000$_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
LIM EN3	LIMG3			0	LIML3			LIM EN2	LIMG2			0	LIML2		
r	rw			r	rw			r	rw			r	rw		

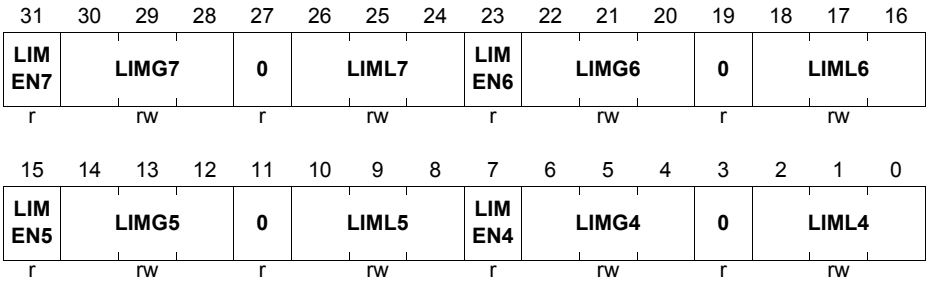
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LIM EN1	LIMG1			0	LIML1			LIM EN0	LIMG0			0	LIML0		
r	rw			r	rw			r	rw			r	rw		

Field	Bits	Type	Description
LIML0, LIML1, LIML2, LIML3	[2:0], [10:8], [18:16], [26:24]	rw	**Multiplexer Line Selection** This bit field selects the input line of a LIMG that can be selected by bit field LIMGn for LIMG output n. 000_B LIMG input IN0 selected 001_B LIMG input IN1 selected 010_B LIMG input IN2 selected 011_B LIMG input IN3 selected 100_B LIMG input IN4 selected 101_B LIMG input IN5 selected 110_B LIMG input IN6 selected 111_B LIMG input IN7 selected
LIMG0, LIMG1, LIMG2, LIMG3	[6:4], [14:12], [22:20], [30:28]	rw	**Multiplexer Group Selection** This bit field determines the LIMGng which is connected to input n of LTC group g. 000_B LIMG0g selected 011_B LIMG3g selected 100_B LIMG4g selected All other combinations are reserved. If a reserved combination of LIMGn is selected, or if LIMENn = 0, the corresponding LIMG output is forced to 0 level.
LIMEN0, LIMEN1, LIMEN2, LIMEN3	7, 15, 23, 31	rw	**Enable Multiplexer Connection** 0_B Input n is not connected to any line. 1_B Input n is connected to the line defined by LIMLn and LIMGn.

Field	Bits	Type	Description
0	3, 11, 19, 27	r	**Reserved** Read as 0; should be written with 0.

LTCA2_LIMCRHg (g = 0-7)
Input Multiplexer Control Register for Upper Half of LTC Group g

Reset Value: 0000 0000$_H$



Field	Bits	Type	Description
LIML4, LIML5, LIML6, LIML7	[2:0], [10:8], [18:16], [26:24]	rw	**Multiplexer Line Selection** This bit field selects the input line of a LIMG that can be selected by bit field LIMGn for LIMG output n. 000_B LIMG input IN0 selected 001_B LIMG input IN1 selected 010_B LIMG input IN2 selected 011_B LIMG input IN3 selected 100_B LIMG input IN4 selected 101_B LIMG input IN5 selected 110_B LIMG input IN6 selected 111_B LIMG input IN7 selected
LIMG4, LIMG5, LIMG6, LIMG7	[6:4], [14:12], [22:20], [30:28]	rw	**Multiplexer Group Selection** This bit field determines the LIMGng which is connected to input n of LTC group g. 000_B LIMG0g selected 011_B LIMG3g selected 100_B LIMG4g selected All other combinations are reserved. If a reserved combination of LIMGn is selected, or if LIMENn = 0, the corresponding LIMG output is forced to 0 level.

Field	Bits	Type	Description
LIMEN4, **LIMEN5,** **LIMEN6,** **LIMEN7**	7, 15, 23, 31	rw	**Enable Multiplexer Connection** 0_B Input n is not connected to any line. 1_B Input n is connected to the line defined by LIMLn and LIMGn.
0	3, 11, 19, 27	r	**Reserved** Read as 0; should be written with 0.

28.7 GPTA®v5 Module Implementation

This section describes the GPTA®v5 interfaces as implemented in TC1798 with the clock control, port and Micro Second Channel connections, interrupt control, and address decoding.

28.7.1 Interconnections of GPTA0/GPTA1/LTCA2 Units

The following items are described in this section:

- GPTA®v5 module (kernel) external registers
- Port control and connections
  - I/O port line assignment
  - I/O function selection
  - Pad driver characteristics selection
  - Emergency control of GPTA®v5 outputs
- On-chip connections
  - Clock bus connections
  - MSC controller connections
  - FADC connections
  - MultiCAN, SCU, and DMA connections
  - SCU connections (ADC, DMA)
- Module clock generation
- Interrupt registers
- GPTA®v5 address map

Figure 28-93 shows the TC1798 specific implementation details and interconnections of the units GPTA0/GPTA1/LTCA2.The units are supplied by clock control and address decoding logic.

Additional connections are described in the following sections.

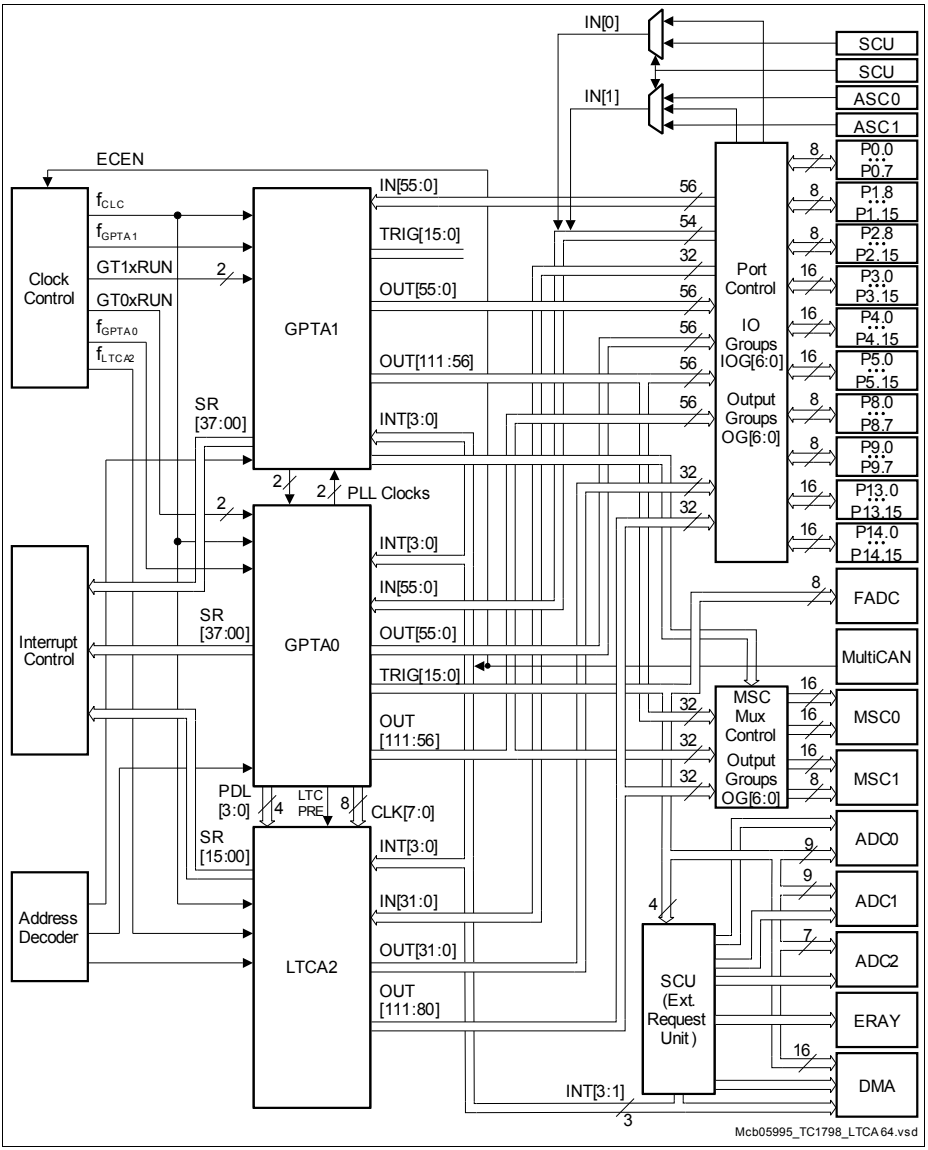


Figure 28-93 Block Diagram of GPTA®v5 Implementation

28.7.2 GPTA®v5 Module External Registers

Figure 28-94 summarizes the GPTA®v5 module related external registers that are required for GPTA0/GPTA1/LTCA2 programming. These registers are referenced and (some of it) described in detail in the following sub-sections.

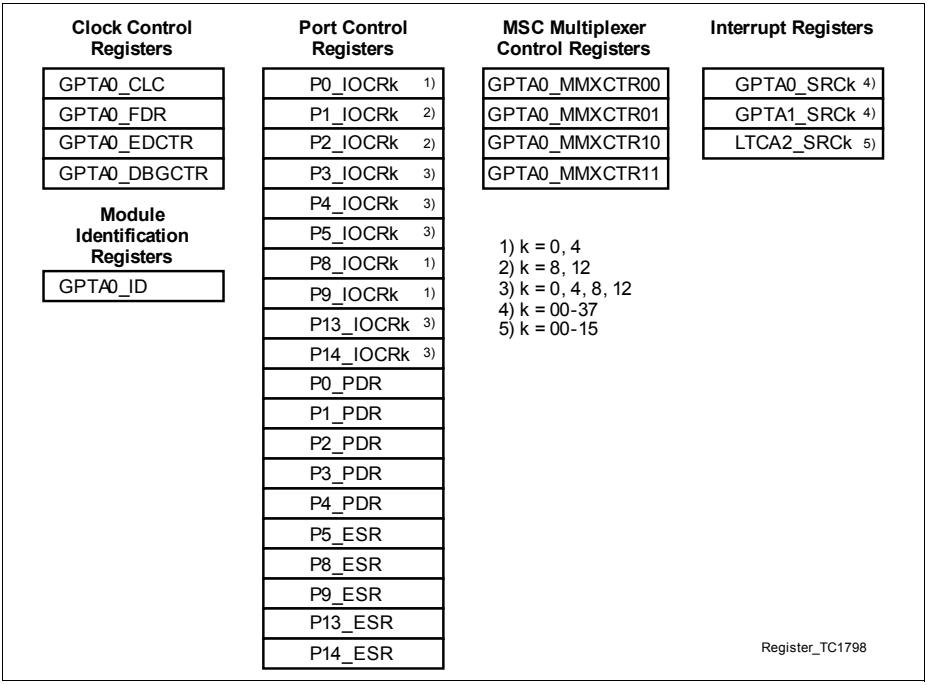


Figure 28-94 GPTA®v5 Implementation-Specific Special Function Registers

28.7.3 Port Control and Connections

This section describes the I/O connections of the GPTA0 unit.

28.7.3.1 I/O Port Line Assignment

In the TC1798, the seven I/O groups and seven output groups of GPTA0 and GPTA1 with their input lines IN[55:0] and output lines OUT[111:0] are assigned to seven 8-bit port groups as shown in Figure 28-95. Within an 8-bit I/O group, the IN/OUT line with lowest index number is assigned to the port line with the lowest index number. The remaining lines are assigned linearly with increasing index numbers. For example, P3.15 is assigned to IN13/OUT13. In the TC1798, the four I/O groups and seven output groups of LTCA2 with their input lines IN[31:0] and output lines OUT[56:0] are assigned to five

8-bit port groups Therefore, the LTCA does not have IOG4, IOG5, and IOG6 and therefore it has no connection to Port 8 or Port 9 pins and only output connections to Port 4, pins 15 down to 8.

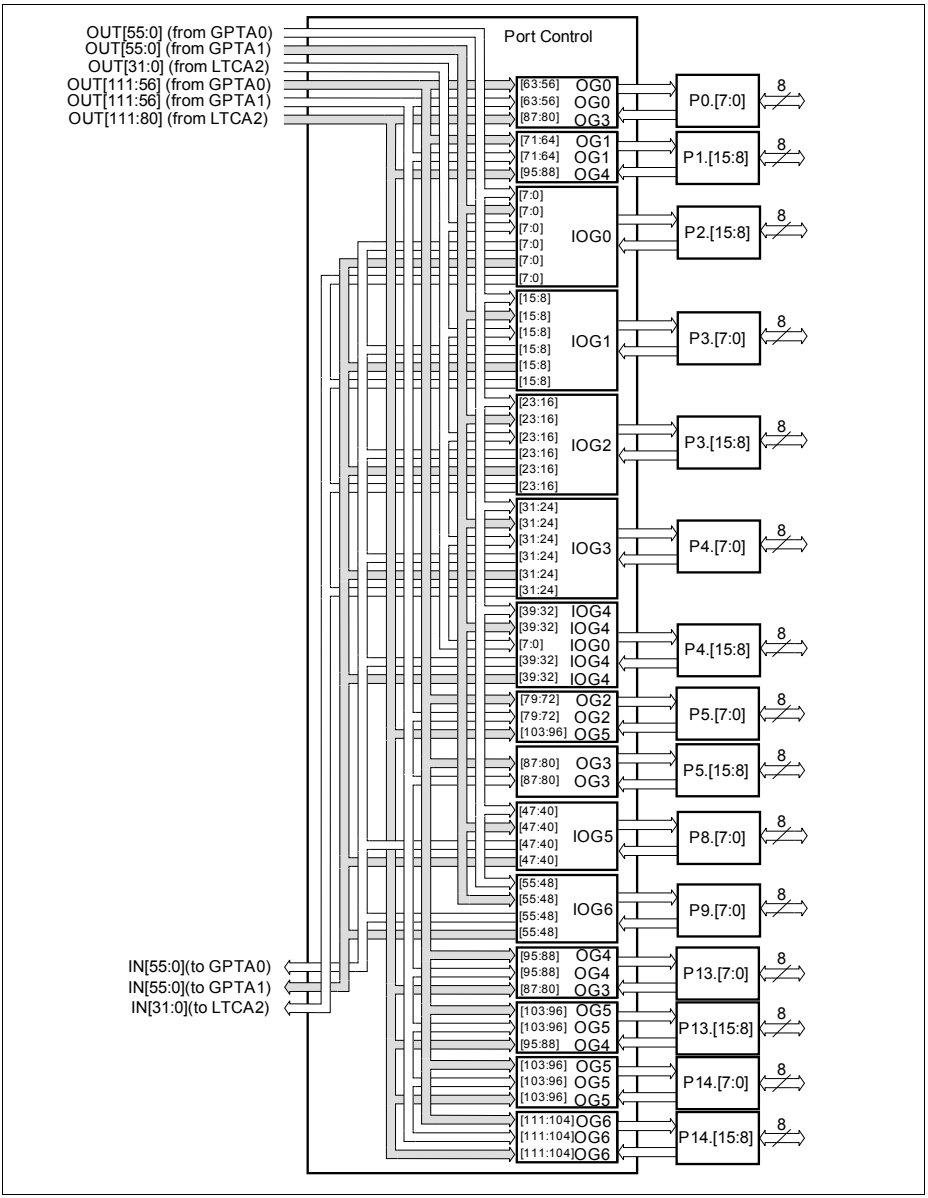


Figure 28-95 I/O Port Line Assignment

The interconnections between the GPTA0 unit and the port I/O lines are controlled in the port logics. The following port control operations selections must be executed:

- Input/output function selection (IOCR registers)
- Pad driver characteristics selection for outputs (PDR registers)

28.7.3.2 Input/Output Function Selection

Table 28-26 shows the GPTA0/GPTA1/LTCA2 I/O lines mapping to the ports. Note that GPTA0/GPTA1/LTCA2 input P2.8/IN0 (see Page 28-296) and GPTA0/GPTA1/LTCA2 input P2.9/IN1 (see Page 28-296) has special connections.

Table 28-26 IOCR Assignment for GPTA®v5 Port Lines PG-LFBGA 516

Ports for GPTA®v5	GPTA0 I/O Lines		GPTA1 I/O Lines		LTCA2 I/O Lines	
	Input	Output	Input	Output	Input	Output
P0.[3:0]		OUT[59:56]		OUT[59:56]		OUT[83:80]
P0.[7:4]		OUT[63:60]		OUT[63:60]		
P1.[11:8]		OUT[67:64]3)		OUT[67:64]3)		OUT[91:88]1)
P1.[15:12]		OUT[71:68]		OUT[71:68]		OUT[95:92]2)
P2.[11:8]	IN[3:0]3)	OUT[3:0]	IN[3:0]4)	OUT[3:0]	IN[3:0]3)	OUT[3:0]
P2.[15:12]	IN[7:4]	OUT[7:4]	IN[7:4]	OUT[7:4]	IN[7:4]	OUT[7:4]
P3.[3:0]	IN[11:8]	OUT[11:8]	IN[11:8]	OUT[11:8]	IN[11:8]	OUT[11:8]
P3.[7:4]	IN[15:12]	OUT[15:12]	IN[15:12]	OUT[15:12]	IN[15:12]	OUT[15:12]
P3.[11:8]	IN[19:16]	OUT[19:16]	IN[19:16]	OUT[19:16]	IN[19:16]	OUT[19:16]
P3.[15:12]	IN[23:20]	OUT[23:20]	IN[23:20]	OUT[23:20]	IN[23:20]	OUT[23:20]
P4.[3:0]	IN[27:24]	OUT[27:24]	IN[27:24]	OUT[27:24]	IN[27:24]	
P4.[7:4]	IN[31:28]	OUT[31:28]	IN[31:28]	OUT[31:28]	IN[31:28]	
P4.[11:8]	IN[35:32]	OUT[35:32]	IN[35:32]	OUT[35:32]		OUT[3:0]
P4.[15:12]	IN[39:36]	OUT[39:36]	IN[39:36]	OUT[39:36]		OUT[7:4]
P5.[3:0]		OUT[75:72]		OUT[75:72]		
P5.[7:4]		OUT[79:76]5)		OUT[79:76]6)		OUT[103:100]7)
P5.[11:8]		OUT[83:80]				
P5.[15:12]		OUT[87:84]		OUT[87:84]		
P8.[3:0]	IN[43:40]	OUT[43:40]8)	IN[43:40]	OUT[42]		
P8.[7:4]	IN[47:44]	OUT[47:44]	IN[47:44]			

Table 28-26 IOCR Assignment for GPTA®v5 Port Lines (cont'd)**PG-LFBGA 516**

Ports for GPTA®v5	GPTA0 I/O Lines		GPTA1 I/O Lines		LTCA2 I/O Lines	
	Input	Output	Input	Output	Input	Output
P9.[3:0]	IN[51:48]		IN[51:48]	OUT[51:48]		
P9.[7:4]	IN[55:52]	OUT[55:52][9)]	IN[55:52]	OUT[53:52]		
P13.[3:0]		OUT[91:88]		OUT[91:88]		OUT[83:80]
P13.[7:4]		OUT[95:92]		OUT[95:92]		OUT[87:84]
P13.[11:8]		OUT[99:96]		OUT[99:96]		OUT[91:88]
P13.[15:12]		OUT[103:100]		OUT[103:100]		OUT[95:92]
P14.[3:0]				OUT[99:96]		OUT[99:96]
P14.[7:4]				OUT[103:100]		OUT[103:100]
P14.[11:8]						OUT[107:104]
P14.[15:12]		OUT[111:108][10)]		OUT[111:108]		OUT[111:108]

1) Out[89] is not available as output on a pin.
2) Out[92] is not available as output on a pin.
3) There is a special connection provided for GPTA0/GPTA1 input line IN0 (see **Page 28-296**) and IN1 (see **Page 28-296**).
4) There is a special connection provided for GPTA0/GPTA1 input line IN0 (see **Page 28-296**) and IN1 (see **Page 28-296**).
5) OUT[78] is not available as output on a pin.
6) OUT[65], OUT[76], and OUT[78] are only as output of GPTA0 available on a pin.
7) OUT[100], OUT[102] and OUT[103] are not connected to this port.
8) OUT[42] is not available as output on a pin.
9) OUT[52] and OUT[53] are not available as output on a pin.
10) OUT[108] and OUT[109] are not available as output on a pin.

Table 28-27 IOCR Assignment for GPTA®v5 Port Lines PG-LFBGA 416

Ports for GPTA®v5	GPTA0 I/O Lines		GPTA1 I/O Lines		LTCA2 I/O Lines	
	Input	Output	Input	Output	Input	Output
P0.[3:0]		OUT[59:56]		OUT[59:56]		OUT[83:80]
P0.[7:4]		OUT[63:60]		OUT[63:60]		

Table 28-27 IOCR Assignment for GPTA®v5 Port Lines (cont'd)**PG-LFBGA 416**

Ports for GPTA®v5	GPTA0 I/O Lines		GPTA1 I/O Lines		LTCA2 I/O Lines	
	Input	Output	Input	Output	Input	Output
P1.[11:8]		OUT[67:64]		OUT[67:64][1)]		OUT[91:88][2)]
P1.[15:12]		OUT[71:68]		OUT[71:68]		OUT[95:92][3)]
P2.[11:8]	IN[3:0][4)]	OUT[3:0]	IN[3:0][5)]	OUT[3:0]	IN[3:0][3)]	OUT[3:0]
P2.[15:12]	IN[7:4]	OUT[7:4]	IN[7:4]	OUT[7:4]	IN[7:4]	OUT[7:4]
P3.[3:0]	IN[11:8]	OUT[11:8]	IN[11:8]	OUT[11:8]	IN[11:8]	OUT[11:8]
P3.[7:4]	IN[15:12]	OUT[15:12]	IN[15:12]	OUT[15:12]	IN[15:12]	OUT[15:12]
P3.[11:8]	IN[19:16]	OUT[19:16]	IN[19:16]	OUT[19:16]	IN[19:16]	OUT[19:16]
P3.[15:12]	IN[23:20]	OUT[23:20]	IN[23:20]	OUT[23:20]	IN[23:20]	OUT[23:20]
P4.[3:0]	IN[27:24]	OUT[27:24]	IN[27:24]	OUT[27:24]	IN[27:24]	
P4.[7:4]	IN[31:28]	OUT[31:28]	IN[31:28]	OUT[31:28]	IN[31:28]	
P4.[11:8]	IN[35:32]	OUT[35:32]	IN[35:32]	OUT[35:32]		OUT[3:0]
P4.[15:12]	IN[39:36]	OUT[39:36]	IN[39:36]	OUT[39:36]		OUT[7:4]
P5.[3:0]		OUT[75:72]		OUT[75:72]		
P5.[7:4]		OUT[79:76][6)]		OUT[79:76][7)]		OUT[103:100][8)]
P5.[11:8]		OUT[83:80]				
P5.[15:12]		OUT[87:84]		OUT[87:84]		
P8.[3:0]	IN[43:40]	OUT[43:40][9)]	IN[43:40]	OUT[43:40] [10)]		
P8.[7:4]	IN[47:44]	OUT[47:44]	IN[47:44]	OUT[45]		
P9.[3:0]	IN[51:48]		IN[51:48]	OUT[51:48]		
P9.[7:4]	IN[55:52]	OUT[55:52] [11)]	IN[55:52]	OUT[55:52] [12)]		
P13.[3:0]		OUT[91:88]		OUT[91:88]		OUT[83:80]
P13.[7:4]		OUT[95:92]		OUT[95:92]		OUT[87:84]
P13.[11:8]		OUT[99:96]		OUT[99:96]		OUT[91:88]
P13.[15:12]		OUT[103:100]		OUT[103:100]		OUT[95:92]
P14.[3:0]				OUT[99:96]		OUT[99:96]

Table 28-27 IOCR Assignment for GPTA®v5 Port Lines (cont'd)**PG-LFBGA 416**

Ports for GPTA®v5	GPTA0 I/O Lines		GPTA1 I/O Lines		LTCA2 I/O Lines	
	Input	Output	Input	Output	Input	Output
P14.[7:4]				OUT[103:100]		OUT[103:100]
P14.[11:8]				OUT[105]		OUT[107:104]
P14.[15:12]		OUT[111:108][13)]		OUT[111:108]		OUT[111:108]

1) OUT[65] is not available on a pin.
2) Out[89] is not available as output on a pin.
3) Out[92] is not available as output on a pin.
4) There is a special connection provided for GPTA0/GPTA1 input line IN0 (see Page 28-296) and IN1 (see Page 28-296).
5) There is a special connection provided for GPTA0/GPTA1 input line IN0 (see Page 28-296) and IN1 (see Page 28-296).
6) OUT[78] is not available as output on a pin.
7) OUT[76], and OUT[78] are only as output of GPTA0 available on a pin.
8) OUT[100], OUT[102] and OUT[103] are not connected to this port.
9) OUT[42] is not available as output on a pin.
10) OUT[40] and OUT[41] are not available on a pin.
11) OUT[52] and OUT[53] are not available as output on a pin.
12) OUt[54] and OUT[55] are not available on a pin.
13) OUT[108] and OUT[109] are not available as output on a pin.

Table 28-28 IOCR Assignment for GPTA®v5 Port Lines PG-LFBGA 292

Ports for GPTA®v5	GPTA0 I/O Lines		GPTA1 I/O Lines		LTCA2 I/O Lines	
	Input	Output	Input	Output	Input	Output
P0.[3:0]		OUT[59:56]		OUT[59:56]		OUT[83:80]
P0.[7:4]		OUT[63:60]		OUT[63:60]		
P1.9		OUT[65]				
P1.12		OUT[68]		OUT[68]		
P2.8	IN[0][1)]	OUT[0]	IN[0][2)]	OUT[0]	IN[0]	OUT[0]
P2.10	IN[2]	OUT[2]	IN[2]	OUT[2]	IN[2]	OUT[2]
P2.12	IN[4]	OUT[4]	IN[4]	OUT[4]	IN[4]	OUT[4]

Table 28-28 IOCR Assignment for GPTA®v5 Port Lines (cont'd)**PG-LFBGA 292**

Ports for GPTA®v5	GPTA0 I/O Lines		GPTA1 I/O Lines		LTCA2 I/O Lines	
	Input	Output	Input	Output	Input	Output
P2.10	IN[6]	OUT[6]	IN[6]	OUT[6]	IN[6]	OUT[6]
P3.0	IN[8]	OUT[8]	IN[8]	OUT[8]	IN[8]	OUT[8]
P3.2	IN[10]	OUT[10]	IN[10]	OUT[10]	IN[10]	OUT[10]
P3.4	IN[12]	OUT[12]	IN[12]	OUT[12]	IN[12]	OUT[12]
P3.6	IN[14]	OUT[14]	IN[14]	OUT[14]	IN[14]	OUT[14]
P3.8	IN[16]	OUT[16]	IN[16]	OUT[16]	IN[16]	OUT[16]
P3.10	IN[18]	OUT[18]	IN[18]	OUT[18]	IN[18]	OUT[18]
P3.12	IN[20]	OUT[20]	IN[20]	OUT[20]	IN[20]	OUT[20]
P3.14	IN[22]	OUT[22]	IN[22]	OUT[22]	IN[22]	OUT[22]
P4.[3:0]	IN[27:24]	OUT[27:24]	IN[27:24]	OUT[27:24]	IN[27:24]	
P4.[7:4]	IN[31:28]	OUT[31:28]	IN[31:28]	OUT[31:28]	IN[31:28]	
P4.[10:8]	IN[34:32]	OUT[34:32]	IN[34:32]	OUT[34:32]		OUT[2:0]
P4.12	IN[36]	OUT[36]	IN[36]	OUT[36]		OUT[4]
P4.14	IN[38]	OUT[38]	IN[38]	OUT[38]		OUT[6]
P5.[3:0]		OUT[75:72]		OUT[75:72]		
P5.[7:4]		OUT[79:76][3)]		OUT[79:76][4)]		OUT[103:100][5)]
P5.[11:8]		OUT[83:80]				
P8.[3:0]	IN[43:40]	OUT[43:40][6)]	IN[43:40]	OUT[42]		
P8.[7:4]	IN[47:44]	OUT[47:44]	IN[47:44]			
P9.[3:0]	IN[51:48]		IN[51:48]	OUT[51:48]		
P9.[7:4]	IN[55:52]	OUT[55:52][7)]	IN[55:52]	OUT[53:52]		
P13.0		OUT[91:88]		OUT[91:88]		OUT[83:80]
P13.[7:4]		OUT[95:92]		OUT[95:92]		OUT[87:84]
P13.[11:8]		OUT[99:96]		OUT[99:96]		OUT[91:88]
P13.[15:12]		OUT[103:100]		OUT[103:100]		OUT[95:92]
P14.0				OUT[96]		OUT[96]
P14.2				OUT[98]		OUT[98]

Table 28-28 IOCR Assignment for GPTA®v5 Port Lines (cont'd)**PG-LFBGA 292**

Ports for GPTA®v5	GPTA0 I/O Lines		GPTA1 I/O Lines		LTCA2 I/O Lines	
	Input	Output	Input	Output	Input	Output
P14.4				OUT[100]		OUT[100]
P14.6				OUT[102]		OUT[102]
P14.8						OUT[104]

1) There is a special connection provided for GPTA0/GPTA1 input line IN0 (see Page 28-296).
2) There is a special connection provided for GPTA0/GPTA1 input line IN0 (see Page 28-296).
3) OUT[78] is not available as output on a pin.
4) OUT[65], OUT[76], and OUT[78] are only as output of GPTA0 available on a pin.
5) OUT[100], OUT[102] and OUT[103] are not connected to this port.
6) OUT[42] is not available as output on a pin.
7) OUT[52] and OUT[53] are not available as output on a pin.

A port line that is programmed as input can be used by the GPTA0 or other units simultaneously as input.

Port lines selected as GPTA0/GPTA1/LTCA2 output are forced to a 0 level if the related multiplexer array in the I/O Line Sharing Block is disabled or if a reserved combination of an OMGn value is selected. Therefore, no glitches and spikes can occur during the programming of the related multiplexer array.

28.7.3.3 Emergency Control of GPTA®v5 Output Ports Lines

Port lines connected to GPTA0/GPTA1/LTCA2 unit output pins can be selectively switched into an Emergency Mode. In this mode, GPTA0/GPTA1/LTCA2 unit output pins react immediately to an active input signal P10.1 (HWCFG1) and drive a logic level that has been programmed in the port output register. As a result, in Emergency Mode a GPTA0/GPTA1/LTCA2 unit output pin drives a predefined value instead of the corresponding logic level that is provided on the related GPTA0/GPTA1/LTCA2 unit output line.

All GPTA®v5 pins at Port 0, Port 1, Port 2, Port 3, Port 4, Port 8, Port 9, Port 13, and Port 14 are connected to one common emergency stop signal that is generated in the System Control Unit of the TC1798. More details about the generation of this emergency stop signal are described in the "System Control Unit" chapter of the TC1798 System Units User´s Manual.

The emergency stop signal always controls 8-bit groups of port lines. The enable function is controlled for each pin by bits ENy (y = number of port line) which are located in the Px_ESR (x = port number) registers. When the emergency stop signal generated in the SCU becomes active and bit Px_ESR.ENy set, output line Px.y is set to the value

of register Px_OUT.Py (emergency enabled). Output Px.y is not affected by the emergency stop signal when bit Px_OUT.Py is reset (emergency disabled).

When the emergency stop signal is released, Pin x.y is switched back to the previously selected GPTA®v5 output function without reprogramming the related port registers.

Table 28-29 Emergency Control for GPTA®v5 Port Output Lines

Port	ESR Register	ESR Enable Bits	GPTA®v5 Output Lines	LTCA Output Lines
Port 0	P0_ESR	EN[7:0]	OUT[63:56]	OUT[87:80]
Port 1	P1_ESR	EN[15:8]	OUT[71:64]	OUT[95:88]
Port 2	P2_ESR	EN[15:8]	OUT[7:0]	OUT[7:0]
Port 3	P3_ESR	EN[15:0]	OUT[23:8]	OUT[23:8]
Port 4	P4_ESR	EN[15:0]	OUT[39:24]	OUT[31:24], OUT[7:0]
Port 5	P5_ESR	EN[15:0]	OUT[87:72]	OUT[111:96]
Port 8	P8_ESR	EN[7:0]	OUT[47:40]	
Port 9	P9_ESR	EN[7:0]	OUT[55:48]	
Port 13	P13_ESR	EN[15:0]	OUT[103:88]	OUT[95:80]
Port 14	P14_ESR	EN[15:0]	OUT[111:96]	OUT[111:96]

28.7.4 On-Chip Connections

This section describes all on-chip interconnections of the GPTA0/GPTA1/LTCA2 units except the connections to I/O ports (see **Section 28.7.3**).

28.7.4.1 Clock Bus Connections

The clock bus signals generated in the GPTA0 and GPTA1 clock distribution cells and PLL clocks are interconnected between the GPTA0/GPTA1/LTCA2 units as shown in **Figure 28-96**.

The GPTA0 clock bus drives Global Timers (GTs), Global Timer Cells (GTCs), and Local Timer Cells (LTCs) of the GPTA0 unit **and** the LTCs of the LTCA2 unit. The GPTA1 clock bus drives its GTs, GTCs, and LTCs.

Each GPTA0 and GPTA1 clock distribution cells has two pairs for PLL clock inputs, an input pair for the local PLL clocks and an input pair for unit-external PLL clocks. The GPTA0 and GPTA1 units are capable to use the PLL clocks from each other.

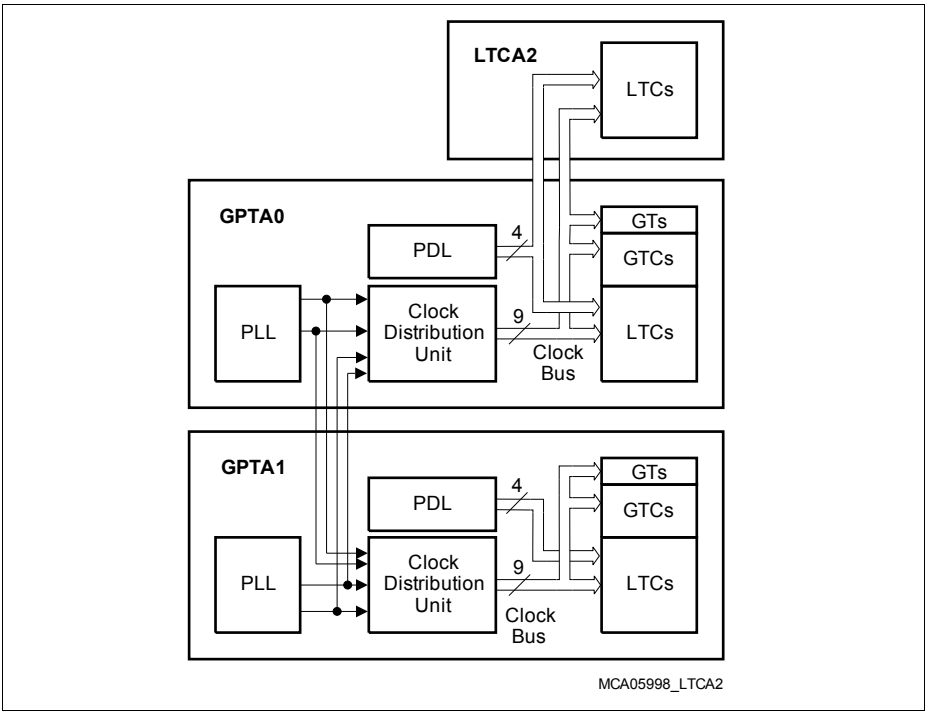


Figure 28-96 Clock Bus Connections of GPTA0/GPTA1/LTCA2

28.7.4.2 MSC Controller Connections

The MSC interfaces (MSC0 and MSC1) provide a serial communication link typically used to connect power switches or other peripheral devices. Each output multiplexers of GPTA0/GPTA1 generate 7 × 8 = 56 output lines OUT[111:56] grouped into seven output groups. Each output multiplexers of LTCA2 generate 4 × 8 = 32 output lines OUT[111:80] grouped into four output groups. All these output lines are wired to 32 MSC0 inputs. Up to 32 MSC0 and 24 MSC1 output extension lines (bits) can be connected to the GPTA®v5. **Figure 28-97** shows the interconnections among the MSC0/1 modules and the GPTA®v5 units. The source for each line of the ALTINL/ALTINH MSC input buses can be selected via a multiplexer connected either to GPTA0 output OUTx(x = 56-111), GPTA1 output OUTx(x = 56-111), LTCA2 output OUTx(x = 80-111).

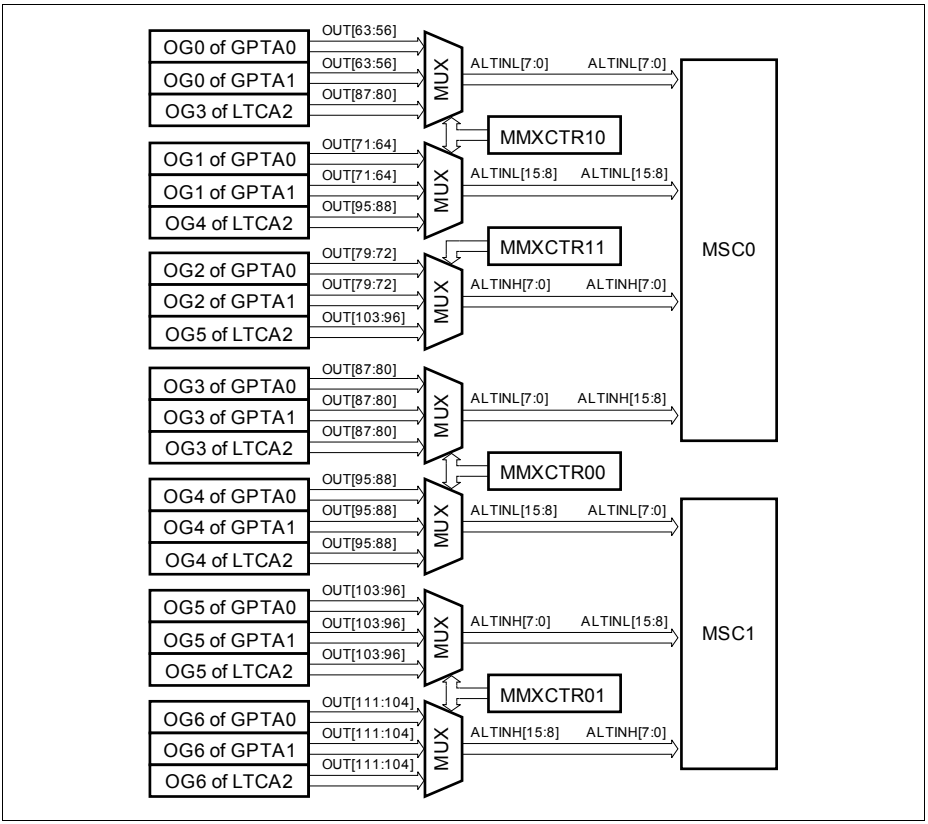


Figure 28-97 GPTA®v5-to-MSC Multiplexer

The multiplexer selection is controlled by four multiplexer control registers that are logically assigned to the GPTA0 unit address range (but described in this section).

Note: Note that eight ALTINH inputs (ALTINH[15:8]) of the MSC1 module are not connected.

Table 28-30 and **Table 28-31** shows the GPTA®v5-to-MSC interconnection assignment.

*Note: **Table 28-30** and **Table 28-31** also shows the assignment of the GPTA0/GPTA1/LTCA2 unit's seven OGx output group lines OGx.y to the output signals OUT[111:56].*

Table 28-30 GPTA0/GPTA1/LTCA2 to MSC0 Interconnection Assignment

MSC0 Input Line	Assigned GPTA0/ GPTA1 Output Line	Assigned LTCA2 Output Line	MSC0 Input Line	Assigned GPTA0/GPTA1 Output Line	Assigned LTCA2 Output Line
ALTINL.0	OUT56 / OG0.0	OUT80 / OG3.0	ALTINH.0	OUT72 / OG2.0	OUT96 / OG5.0
ALTINL.1	OUT57 / OG0.1	OUT81 / OG3.1	ALTINH.1	OUT73 / OG2.1	OUT97 / OG5.1
ALTINL.2	OUT58 / OG0.2	OUT82 / OG3.2	ALTINH.2	OUT74 / OG2.2	OUT98 / OG5.2
ALTINL.3	OUT59 / OG0.3	OUT83 / OG3.3	ALTINH.3	OUT75 / OG2.3	OUT99 / OG5.3
ALTINL.4	OUT60 / OG0.4	OUT84 / OG3.4	ALTINH.4	OUT76 / OG2.4	OUT100 / OG5.4
ALTINL.5	OUT61 / OG0.5	OUT85 / OG3.5	ALTINH.5	OUT77 / OG2.5	OUT101 / OG5.5
ALTINL.6	OUT62 / OG0.6	OUT86 / OG3.6	ALTINH.6	OUT78 / OG2.6	OUT102 / OG5.6
ALTINL.7	OUT63 / OG0.7	OUT87 / OG3.7	ALTINH.7	OUT79 / OG2.7	OUT103 / OG5.7
ALTINL.8	OUT64 / OG1.0	OUT88 / OG4.0	ALTINH.8	OUT80 / OG3.0	OUT104 / OG6.0
ALTINL.9	OUT65 / OG1.1	OUT89 / OG4.1	ALTINH.9	OUT81 / OG3.1	OUT105 / OG6.1
ALTINL.10	OUT66 / OG1.2	OUT90 / OG4.2	ALTINH.10	OUT82 / OG3.2	OUT106 / OG6.2

Table 28-30 GPTA0/GPTA1/LTCA2 to MSC0 Interconnection Assignment (cont'd)

MSC0 Input Line	Assigned GPTA0/ GPTA1 Output Line	Assigned LTCA2 Output Line	MSC0 Input Line	Assigned GPTA0/GPTA1 Output Line	Assigned LTCA2 Output Line
ALTINL.11	OUT67 / OG1.3	OUT91 / OG4.3	ALTINH.11	OUT83 / OG3.3	OUT107 / OG6.3
ALTINL.12	OUT68 / OG1.4	OUT92 / OG4.4	ALTINH.12	OUT84 / OG3.4	OUT108 / OG6.4
ALTINL.13	OUT69 / OG1.5	OUT93 / OG4.5	ALTINH.13	OUT85 / OG3.5	OUT109 / OG6.5
ALTINL.14	OUT70 / OG1.6	OUT94 / OG5.0	ALTINH.14	OUT86 / OG3.6	OUT110 / OG6.6
ALTINL.15	OUT71 / OG1.7	OUT95 / OG5.1	ALTINH.15	OUT87 / OG3.7	OUT111 / OG6.7

Table 28-31 GPTA0/GPTA1/LTCA2 to MSC1 Interconnection Assignment

MSC1 Input Line	Assigned GPTA0/ GPTA1/LTCA2 Output Line	MSC1 Input Line	Assigned GPTA0/ GPTA1/LTCA2 Output Line
ALTINL.0	OUT88 / OG4.0	ALTINH.0	OUT104 / OG6.0
ALTINL.1	OUT89 / OG4.1	ALTINH.1	OUT105 / OG6.1
ALTINL.2	OUT90 / OG4.2	ALTINH.2	OUT106 / OG6.2
ALTINL.3	OUT91 / OG4.3	ALTINH.3	OUT107 / OG6.3
ALTINL.4	OUT92 / OG4.4	ALTINH.4	OUT108 / OG6.4
ALTINL.5	OUT93 / OG4.5	ALTINH.5	OUT109 / OG6.5
ALTINL.6	OUT94 / OG4.6	ALTINH.6	OUT110 / OG6.6
ALTINL.7	OUT95 / OG4.7	ALTINH.7	OUT111 / OG6.7
ALTINL.8	OUT96 / OG5.0	ALTINH.8	
ALTINL.9	OUT97 / OG5.1	ALTINH.9	
ALTINL.10	OUT98 / OG5.2	ALTINH.10	
ALTINL.11	OUT99 / OG5.3	ALTINH.11	
ALTINL.12	OUT100 / OG5.4	ALTINH.12	
ALTINL.13	OUT101 / OG5.5	ALTINH.13	

Table 28-31 GPTA0/GPTA1/LTCA2 to MSC1 Interconnection Assignment (cont'd)

MSC1 Input Line	Assigned GPTA0/ GPTA1/LTCA2 Output Line	MSC1 Input Line	Assigned GPTA0/ GPTA1/LTCA2 Output Line
ALTINL.14	OUT102 / OG5.6	ALTINH.14	
ALTINL.15	OUT103 / OG5.7	ALTINH.15	

GPTA®v5-to-MSC Multiplexer Control Registers

The following registers are required for GPTA®v5-to-MSC multiplexer control:

- **GPTA0_MMXCTR00** controls the interconnections of GPTA®v5 Units to the MSC0 ALTINH[15:8] and MSC1 ALTINL[7:0] inputs.
- **GPTA0_MMXCTR01** controls the interconnections of GPTA®v5 Units to the MSC0 ALTINH[15:0] inputs. MSC1 ALTINL[15:8] inputs and MSC1 ALTINH[7:0] inputs.
- **GPTA0_MMXCTR10** controls the interconnections of GPTA®v5 Units to the MSC0 ALTINL[15:0] inputs.
- **GPTA0_MMXCTR11** controls the interconnections of GPTA®v5 Units to the MSC0 ALTINH[7:0] inputs.

For each of the ALTINL/ALTINH inputs of the MSC, the 2-bit bit fields in these registers determine which unit output is selected.

GPTA0_MMXCTR00
GPTA-to-MSC Multiplexer Control Register 00
(700_H) **Reset Value: $0000\ 0000_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MUX 15				MUX 14				MUX 13				MUX 12				MUX 11				MUX 10				MUX 9				MUX 8			
rw				rw				rw				rw				rw				rw				rw				rw			

MUX 7				MUX 6				MUX 5				MUX 4				MUX 3				MUX 2				MUX 1				MUX 0			
rw				rw				rw				rw				rw				rw				rw				rw			

Field	Bits	Type	Description
MUXn (n = 0-7)	[2*n+1:2*n]	rw	**Multiplexer Control for MSC0 Inputs ALTINH.(n+8)** 00_B GPTA0 output OUT[80+n] selected and connected to MSC0 ALTINH.(n+8) 01_B GPTA1 output OUT[80+n] selected and connected to MSC0 ALTINH.(n+8) 10_B LTCA2 output OUT[80+n] selected and connected to MSC0 ALTINH.(n+8) 11_B Reserved
MUXn (n = 8-15)	[2*n+1:2*n]	rw	**Multiplexer Control for MSC1 Inputs ALTINL(n-8)** 00_B GPTA0 output OUT[80+n] selected and connected to ALTINL.(n-8) 01_B GPTA1 output OUT[80+n] selected and connected to MSC1 ALTINL.(n-8) 10_B LTCA2 output OUT[80+n] selected and connected to MSC1 ALTINL.(n-8) 11_B Reserved

GPTA0_MMXCTR01
GPTA-to-MSC Multiplexer Control Register 01
(704_H) **Reset Value: $0000\ 0000_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MUX 15				MUX 14				MUX 13				MUX 12				MUX 11				MUX 10				MUX 9				MUX 8			
rw				rw				rw				rw				rw				rw				rw				rw			

MUX 7				MUX 6				MUX 5				MUX 4				MUX 3				MUX 2				MUX 1				MUX 0			
rw				rw				rw				rw				rw				rw				rw				rw			

Field	Bits	Type	Description
MUXn (n = 0-7)	[2*n+1:2*n]	rw	**Multiplexer Control for MSC1 Inputs ALTINL.(n+8)** 00_B GPTA0 output OUT[96+n] selected and connected to MSC1 ALTINL.(n+8) 01_B GPTA1 output OUT[96+n] selected and connected to MSC1 ALTINL.(n+8) 10_B LTCA2 output OUT[96+n] selected and connected to MSC1 ALTINL.(n+8) 11_B Reserved
MUXn (n = 8-15)	[2*n+1:2*n]	rw	**Multiplexer Control for MSC1 Inputs ALTINH.(n-8)** 00_B GPTA0 output OUT[96+n] selected and connected to MSC1 ALTINH.(n-8) 01_B GPTA1 output OUT[96+n] selected and connected to MSC1 ALTINH.(n-8) 10_B LTCA2 output OUT[96+n] selected and connected to MSC1 ALTINH.(n-8) 11_B Reserved

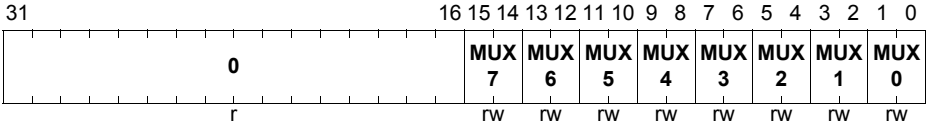
GPTA0_MMXCTR10
GPTA-to-MSC Multiplexer Control Register 10
(708_H) **Reset Value: $0000\ 0000_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MUX 15		MUX 14		MUX 13		MUX 12		MUX 11		MUX 10		MUX 9		MUX 8		MUX 7		MUX 6		MUX 5		MUX 4		MUX 3		MUX 2		MUX 1		MUX 0	
rw		rw		rw		rw		rw		rw		rw		rw		rw		rw		rw		rw		rw		rw		rw		rw	

Field	Bits	Type	Description
MUXn (n = 0-15)	[2*n+1:2*n]	rw	**Multiplexer Control for MSC0 Inputs ALTINL.n** 00_B GPTA0 output OUT[56+n] selected and connected to MSC0 ALTINL.n 01_B GPTA1 output OUT[56+n] selected and connected to MSC0 ALTINL.n 10_B LTCA2 output OUT[80+n] selected and connected to MSC0 ALTINL.n 11_B Reserved

GPTA0_MMXCTR11
GPTA-to-MSC Multiplexer Control Register 11

(70C$_H$) Reset Value: 0000 0000$_H$



Field	Bits	Type	Description
MUXn (n = 0-7)	[2*n+1:2*n]	rw	**Multiplexer Control for MSC0 Inputs ALTINH.n** 00_B GPTA0 output OUT[72+n] selected and connected to MSC0 ALTINH.n 01_B GPTA1 output OUT[72+n] selected and connected to MSC0 ALTINH.n 10_B LTCA2 output OUT[96+n] selected and connected to MSC0 ALTINH.n 11_B Reserved
0	[31:15]	r	**Reserved** Read as 0; should be written with 0.

28.7.4.3 Connections to SCU, MultiCAN, FADC, DMA, Ports

The GPTA0/GPTA1/LTCA2 units of the TC1798 GPTA®v5 module have several on-chip interconnections with the SCU, MultiCAN, FADC, DMA modules. **Figure 28-98** shows these interconnections.

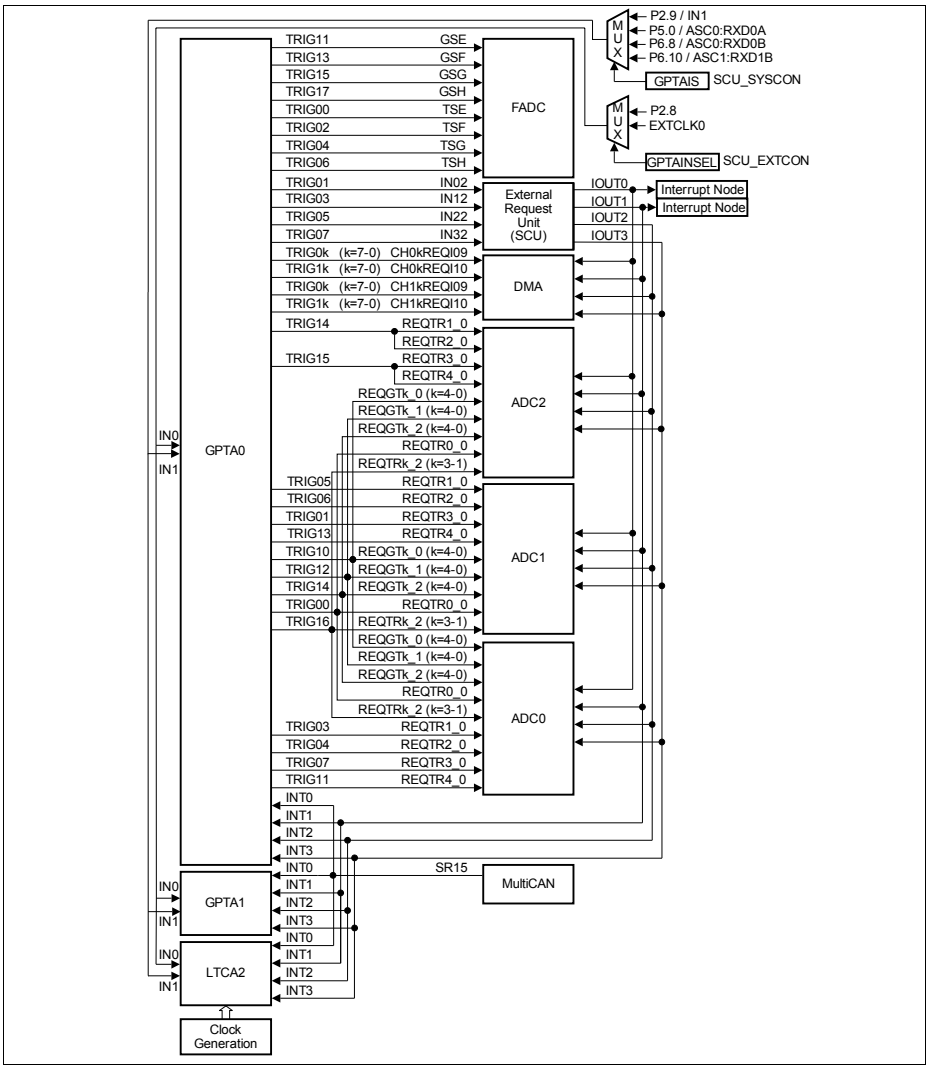


Figure 28-98 Connections of GPTA®v5 with On-Chip Modules

System Control Unit

The SCU contains the external request unit (ERU), which is especially responsible for controlling requests coming from the MSC modules, port pins, or from the GPTA0/GPTA1/LTCA2 unit and passing these request to AD converters, DMA controller, ERAY communication controller or interrupt nodes.

MultiCAN Connections

The MultiCAN controller has the following connections to the GPTA0/GPTA1/LTCA2 unit:

- MultiCAN service request output SR15 is connected to the INT0 input of GPTA0/GPTA1/LTCA2.
- GPTA0 output line OUT5 is connected to the external time trigger input ECTT3 of the MultiCAN module.

DMA Controller

As shown in **Figure 28-98**, eight GPTA0 on-chip trigger and gating output lines are connected as trigger input signals to the DMA request inputs. Furthermore the external request unit generates four DMA request output signals (IOUT[3:0]) that can be activated via port pins, the MSC clock outputs, or the four GPTA®v5 output lines. Three of these four DMA request output signals are connected to the GPTA0/GPTA1/LTCA2 internal inputs INT[3:1]. These connections allow, for example, GTC or LTC events in the GPTA®v5 units to be triggered by a request coming from a port pin or from the MSC clock.

ADC Connections

As shown in **Figure 28-98**, for each ADC nine GPTA0 on-chip trigger and gating output lines are connected as trigger input signals or gating input signals to the channel trigger logic of the ADC. Thus dedicated GPTA0 outputs can generate trigger events or act as gating signals for ADC channels. Furthermore the external request unit generates two ADC conversion trigger signals (IOUT[3:2]) and two ADC conversion gating signals (PDOUT[3:2]) that can be activated each via port pins, the MSC clock outputs, or two GPTA®v5 output lines.

FADC Connections

As shown in **Figure 28-98**, eight GPTA0 on-chip trigger and gating output lines are connected as trigger input signals or gating input signals to the channel trigger logic of the FADC. Thus dedicated GPTA0 outputs can generate trigger events or act as gating signals for FADC channels.

Port Connections of Input IN0

The common input line IN0 of the GPTA0/GPTA1/LTCA2 unit is connected to the output of a 2-to-1 multiplexer. This multiplexer is controlled by bit field SCU_EXTCON.GPTAINSEL and allows the common GPTA0/GPTA1/LTCA2 input IN0 to be connected to one out of two input lines. This feature especially allows the number of clock of the PLL (to determine clock stability) to be measured by GTs (Global Timers) or FPC0 (Filter and Prescaler Cell) of the GPTA0/GPTA1.

Table 28-32 GPTA0 Input Line IN0 Connections

SCU_EXTCON. GPTAINSEL	GPTA0/GPTA1/LTCA2 Input IN0 Connected to
00_B	P2.9 / IN0 (default after reset)
01_B	SCU: EXTCLK0

Port Connections of Input IN1

The common input line IN1 of the GPTA0/GPTA1/LTCA2 unit is connected to the output of a 4-to-1 multiplexer. This multiplexer is controlled by bit field SCU_SYSCON.GPTAIS and allows the common GPTA0/GPTA1/LTCA2 input IN1 to be connected to one out of four port input lines. This feature especially allows the baud rates of an ASC0 or ASC1 receiver input signal to be measured by timers of the GPTA0/GPTA1/LTCA2.

Table 28-33 GPTA0 Input Line IN1 Connections

SCU_SYSCON. GPTAIS	GPTA0/GPTA1/LTCA2 Input IN1 Connected to
00_B	P2.9 / IN1 (default after reset)
01_B	P5.0 / ASC0: RXD0A
10_B	P6.8 ASC0: RXD0B
11_B	P6.10 / ASC1: RXD1B

28.7.5 Module Clock Generation

As shown in **Figure 28-99**, the clock signals for the GPTA0/GPTA1/LTCA2 units are generated and controlled by one clock generation circuitry. This clock generation circuitry is responsible for the enable/disable control, the clock frequency adjustment, and the debug clock control. The circuitry includes the following registers:

- **Clock Control Register GPTA0_CLC** (see **Page 28-300**), responsible for the generation of the control clock f_{CLC} that is used by each of the units.
- **Fractional Divider Register GPTA0_FDR** (see **Page 28-301**), responsible for the frequency control of the module timer clock f_{GPTA}.

- **Clock Enable/Disable Control Register GPTA0_EDCTR** (see **Page 28-303**), responsible for the enable/disable control of the different units as clocks f_{GPTA0},f_{GPTA1}/f_{LTCA2}, and for the run control for the Global Timers in GPTA0 and GPTA1.
- **Debug Clock Control Register GPTA0_DBGCTR** (see **Page 28-305**), responsible for the module timer clock control in Debug Mode.

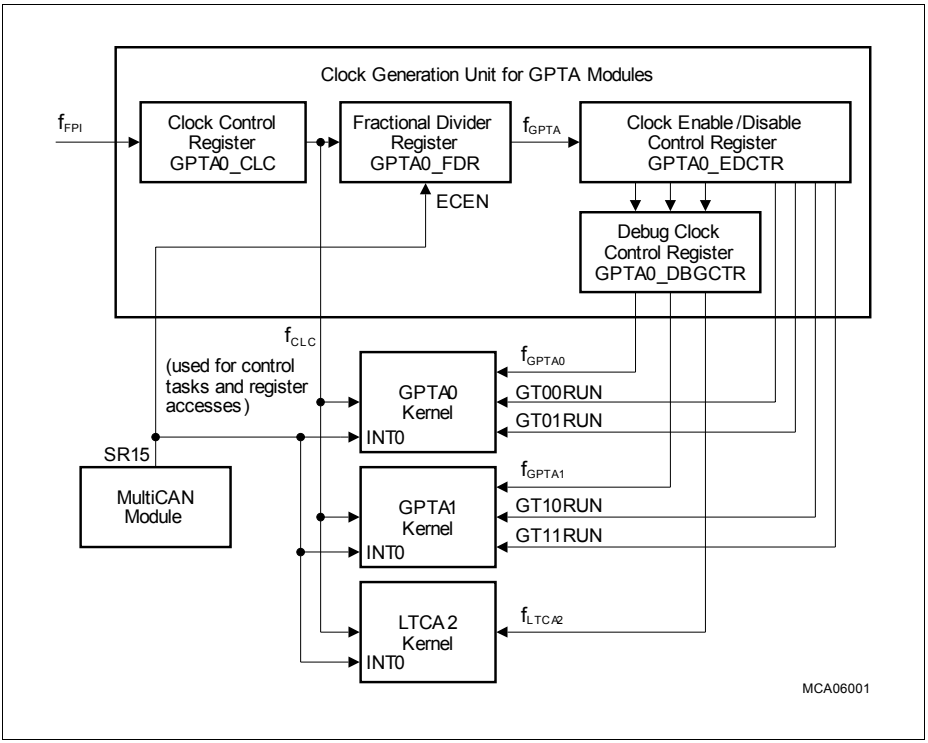


Figure 28-99 GPTA®v5 Clock Generation for the units

Note: Registers GPTA0_CLC, GPTA0_FDR, GPTA0_EDCTR and GPTA0_DBGCTR are located in the address space of GPTA0.

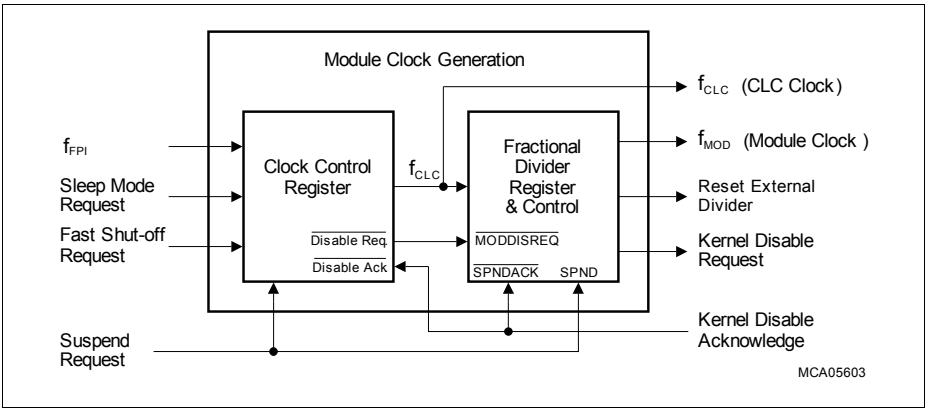


Figure 28-100Details on Module Clock Generation

The GPTA®v5 module control clock f_{CLC} is used inside the GPTA®v5 module kernels for control purposes such as clocking of control logic and register operations. The frequency of f_{CLC} is identical to the clock frequency f_{FPI}. The clock control registers GPTA0_CLC make it possible to enable/disable f_{CLC} under certain conditions.

The separate GPTA®v5 unit clocks f_{GPTA0}, f_{GPTA1}, f_{LTCA2} are used inside the GPTA®v5 units as input clocks for the timers. All unit clocks have the same frequency as f_{GPTA} (as selected through register GPTA0_FDR) and can be enabled/disabled separately each through register GPTA0_ECDTR.

Note: If f_{GPTA0}, f_{GPTA1}, f_{LTCA2} are disabled by the enable bits in register GPTA0_ECDTR, f_{CLC} keeps running. In this case, that means that register accesses to the GPTA®v5 units are possible.

The frequency of f_{GPTA} is defined by:

$$f_{GPTA} = f_{FPI} \times \frac{1}{n} \quad \text{with n = 1024 - FDR.STEP or} \tag{28.6}$$

$$f_{GPTA} = f_{FPI} \times \frac{n}{1024} \quad \text{with n = 0-1023} \tag{28.7}$$

Note: The upper formula applies to normal divider mode of the fractional divider (GPTA0_FDR.DM = 01_B). The lower formula applies to fractional divider mode (GPTA0_FDR.DM = 10_B).

The debug clock control register additionally makes it possible to control the timer clocks f_{GPTA0}, f_{GPTA1}, f_{LTCA2} for debug purposes on basis of a clock counter.

If the debug clock feature is enabled (GPTA0_DBGCTR.DBGCEN = 1) and bit GPTA0_DBGCTR.DBGCST is set, the timer clocks f_{GPTA0}, f_{GPTA1}, f_{LTCA2} will be activated in parallel for as many clock cycles as have been programmed into bit field GPTA0_DBGCTR.CLKCNT. When the debug clock feature becomes enabled, bit field CLKCNT counts down and stops counting at 0000_H. Bit DBGCST is again reset by hardware after the programmed number of clock pulses has been issued. This feature makes it possible to single step the GPTA®v5 units with a programmable timer clock granularity.

Note: The GPTA®v5 module is disabled after reset. In general, after reset, the GPTA®v5 module control clock f_{CLC} must be switched on (writing to register GPTA0_CLC) before the frequency of the GPTA®v5 module timer clock f_{GPTA} is defined (writing to register GPTA0_FDR).

28.7.5.1 Clock Control Registers

The clock control register makes it possible to control (enable/disable) the GPTA®v5 module control clock f_{CLC}. The clock signal f_{CLC} is used by the GPTA0/GPTA1/LTCA2 as a clock for internal control operations but not for timer purposes.

GPTA0_CLC
GPTA Clock Control Register (000_H) Reset Value: 0000 0003$_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0										FSOE	SBWE	EDIS	SPEN	DISS	DISR
r										rw	w	rw	rw	r	rw

Field	Bits	Type	Description
DISR	0	rw	**GPTA®v5 Module Disable Request Bit** Used for enable/disable control of the GPTA®v5 module.
DISS	1	r	**GPTA®v5 Module Disable Status Bit** Bit indicates the current status of the GPTA®v5 module.
SPEN	2	rw	**GPTA®v5 Module Suspend Enable for OCDS** Used to enable the suspend mode.
EDIS	3	rw	**External Request Disable** Used to control the external clock disable request.
SBWE	4	w	**GPTA®v5 Module Suspend Bit Write Enable for OCDS** Determines whether SPEN and FSOE are write-protected.
FSOE	5	rw	**Fast Switch Off Enable** Used for fast clock switch off in suspend mode.
0	[31:6]	r	**Reserved** Read as 0; should be written with 0.

Note: After a hardware reset operation, the f_{CLC} clock is disabled (DISS set). Therefore, the GPTA®v5 module clock generation is completely disabled.

Note: In disabled state, no registers of GPTA®v5 module can be read or written except the GPTA_CLC register.

28.7.5.2 Fractional Divider Register

The fractional divider makes it possible to generate a GPTA®v5 module clock from an input clock using a programmable divider. The fractional divider divides the input clock f_{CLC} either by the factor 1/n or by a fraction of n/1024 for any value of n from 0 to 1023, and outputs the clock signal, f_{GPTA}. The fractional divider is controlled by the FDR register.

The fractional divider register controls the clock frequency of the GPTA®v5 module timer clock f_{GPTA}. The clock frequency of f_{GPTA0}, f_{GPTA1}, f_{LTCA2} is identical to the one of f_{GPTA}.

GPTA0_FDR
GPTA Fractional Divider Register (00C$_H$) Reset Value: 0000 0000$_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DIS CLK	EN HW	SUS REQ	SUS ACK	0		RESULT									
rwh	rw	rh	rh	r		rh									

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DM		SC		SM	FDIS	STEP									
rw		rw		rw	rw	rw									

Field	Bits	Type	Description
STEP	[9:0]	rw	**Step Value** Reload or addition value for RESULT.
FDIS	10	rw	**Freeze Disable** This bit controls the freeze function for this module. 0_B Module operates on corrected clock, with reduced modulation jitter 1_B Module operates on uncorrected clock with full modulation jitter
SM	11	rw	**Suspend Mode** SM selects between granted or immediate suspend mode.
SC	[13:12]	rw	**Suspend Control** This bit field determines the behavior of the fractional divider in suspend mode.
DM	[15:14]	rw	**Divider Mode** This bit field selects normal divider mode, fractional divider mode, and off-state.

Field	Bits	Type	Description
RESULT	[25:16]	rh	**Result Value** Bit field for the addition result.
SUSACK	28	rh	**Suspend Mode Acknowledge** Indicates state of SPNDACK signal.
SUSREQ	29	rh	**Suspend Mode Request** Indicates state of SPND signal.
ENHW	30	rw	**Enable Hardware Clock Control** Controls operation of ECEN input and DISCLK bit.
DISCLK	31	rwh	**Disable Clock** Hardware controlled disable for f_{OUT} signal.
0	[27:26]	r	**Reserved** Read as 0; should be written with 0.

The clock enable/disable control register controls two functions: clock enable/disable control for each Global Timer in the GPTA0/GPTA1 units and enable/disable control for the GPTA®v5 unit clocks, separately for each clock f_{GPTA0}, f_{GPTA1}, f_{LTCA2}.

GPTA0_EDCTR
GPTA Clock Enable/Disable Control Register
(400_H) **Reset Value: $0000\ 0000_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

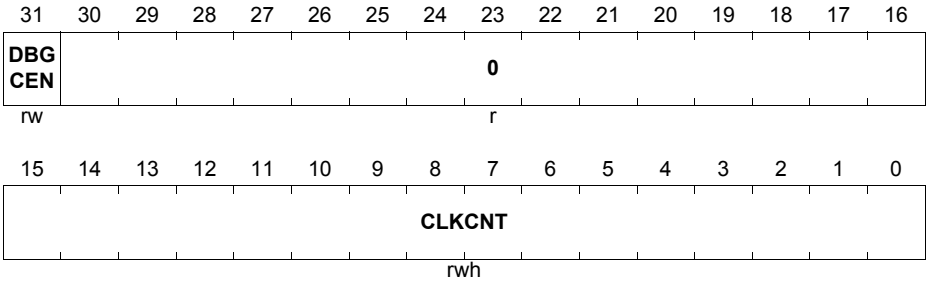
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0					L2EN	G1EN	G0EN	0				GT11RUN	GT10RUN	GT01RUN	GT00RUN
r					rw	rw	rw	r				rw	rw	rw	rw

Field	Bits	Type	Description
GT00RUN	0	rw	**GPTA0 Global Timer 0 Run Control** 0_B GPTA0 Global Timer 0 clock is stopped. 1_B GPTA0 Global Timer 0 clock is started/running.
GT01RUN	1	rw	**GPTA0 Global Timer 1 Run Control** 0_B GPTA0 Global Timer 1 clock is stopped. 1_B GPTA0 Global Timer 1 clock is started/running.
GT10RUN	2	rw	**GPTA1 Global Timer 0 Run Control** 0_B GPTA1 Global Timer 0 clock is stopped. 1_B GPTA1 Global Timer 0 clock is started/running.
GT11RUN	3	rw	**GPTA1 Global Timer 1 Run Control** 0_B GPTA1 Global Timer 1 clock is stopped. 1_B GPTA1 Global Timer 1 clock is started/running.
G0EN	8	rw	**GPTA0 Timer Clock Enable** 0_B GPTA0 timer clock f_{GPTA0} is disabled. 1_B GPTA0 timer clock f_{GPTA0} is enabled.
G1EN	9	rw	**GPTA1 Timer Clock Enable** 0_B GPTA1 timer clock f_{GPTA1} is disabled. 1_B GPTA1 timer clock f_{GPTA1} is enabled.

Field	Bits	Type	Description
L2EN	10	rw	**LTCA2 Timer Clock Enable** 0_B LTCA2 timer clock f_{LTCA2} is disabled. 1_B LTCA2 timer clock f_{LTCA2} is enabled.
0	[7:4], [31:11]	r	**Reserved** Read as 0; should be written with 0.

The debug clock control register makes it possible to control the GPTA®v5 unit clocks f_{GPTA0}, f_{GPTA1}, f_{LTCA2} for debug purposes on the basis of a clock counter.

GPTA0_DBGCTR
GPTA Debug Clock Control Register (004_H) **Reset Value: $0000\ 0000_H$**



Field	Bits	Type	Description
CLKCNT	[15:0]	rwh	**Debug Clock Count** This bit field determines the number of clock pulses to be issued when the debug clock feature is enabled (DBGCEN = 1). CLKCNT counts down to 0000_H and stops when the debug clock feature is enabled.
DBGCEN	31	rw	**Debug Clock Enable** 0_B The debug clock feature is disabled. The GPTA®v5 unit clocks are always enabled. 1_B The debug clock feature is enabled. If a non-zero value is written to bit field CLKCNT the related number of clock pulses is issued at f_{GPTA0}, f_{GPTA1}, f_{LTCA2}.
0	[30:16]	r	**Reserved** Read as 0; should be written with 0.

28.7.6 Limits of Cascading GTCs and LTCs

As shown on **Page 28-57** and **Page 28-69**, a maximum of 32 GTCs and a maximum of 64 LTCs can be cascaded. In the TC1798, however cascading of GTCs and LTCs is limited under certain conditions.

If the LTCs are running with the maximum GPTA®v5 unit clock of $f_{GPTA} = f_{FPI}$ = 90 MHz, a maximum of 16 GTCs and 16 LTCs can be connected together. If the GPTA®v5 unit clock f_{GPTA} is reduced, the number of LTCs that can be cascaded increases accordingly. Only the integer part of the divider ratio as selected by the GPTA0_FDR fractional divider register determines the maximum number of cascaded GTCs and LTCs.

Table 28-34 Limits of Cascading GTCs and LTCs

f_{FPI}	Selected Clock Divider Ratio[1)]	Max. Number of Cascaded GTCs/LTCs
90 MHz	$1 <= f_{FPI}/f_{GPTA} < 2$	16 GTCs, 16 LTCs
	$2 <= f_{FPI}/f_{GPTA} < 3$	no limits for GTCs, 32 LTCs
	$3 <= f_{FPI}/f_{GPTA} < 4$	no limits for GTCs, 48 LTCs
	$4 <= f_{FPI}/f_{GPTA}$	no limits for GTCs and LTCs
45 MHz	$1 <= f_{FPI}/f_{GPTA} < 2$	no limits for GTCs, 32 LTCs
	$2 <= f_{FPI}/f_{GPTA}$	no limits for GTCs and LTCs

1) Selected by the GPTA0_FDR fractional divider register.

28.7.7 Interrupt Registers

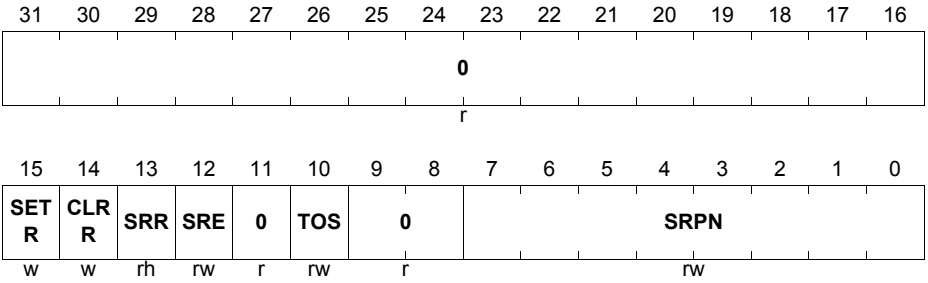
Each of the service request outputs of the GPTA0/GPTA1/LTCA2 units is able to generate an interrupt and is controlled by an interrupt service request control register GPTA_SRCk. Therefore, the following interrupt service request control registers are available:

- GPTA0: GPTA0_SRC[37:00]
- GPTA1: GPTA1_SRC[37:00]
- LTCA2: LTCA2_SRC[15:00]

GPTA0_SRCk (k = 00-37)
GPTA0 Interrupt Service Request Control Register k
($7FC_H$-k*4_H) **Reset Value: $0000\ 0000_H$**

GPTA1_SRCk (k = 00-37)
GPTA1 Interrupt Service Request Control Register k
($7FC_H$-k*4_H) **Reset Value: $0000\ 0000_H$**

LTCA2_SRCk (k = 00-15)
LTCA2 Interrupt Service Request Control Register k
($7FC_H$-k*4_H) **Reset Value: $0000\ 0000_H$**



Field	Bits	Type	Description
SRPN	[7:0]	rw	**Service Request Priority Number**
TOS	10	rw	**Type of Service Control**
SRE	12	rw	**Service Request Enable**
SRR	13	rh	**Service Request Flag**
CLRR	14	w	**Request Clear Bit**
SETR	15	w	**Request Set Bit**
0	[9:8], 11, [31:16]	r	**Reserved** Read as 0; should be written with 0.

Note: Additional details on service request nodes and the service request control registers are described in the Interrupt chapter of the TC1798 User´s Manual System Units part (Volume 1).

28.7.8 GPTA Register Address Map

The GPTA0 and GPTA1 register map shown in **Figure 28-101**. The LTCA2 register map shown in **Figure 28-102**.

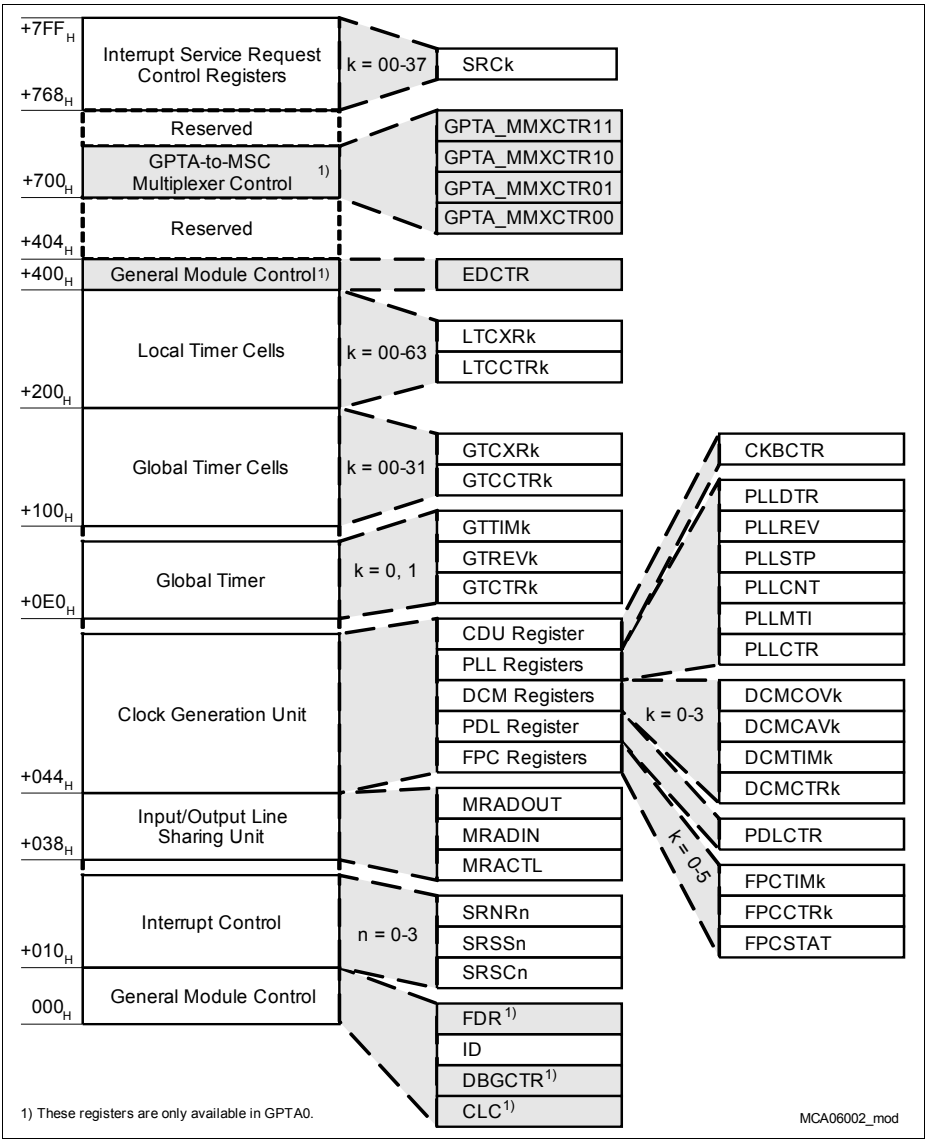


Figure 28-101GPTA0/GPTA1 Register Map

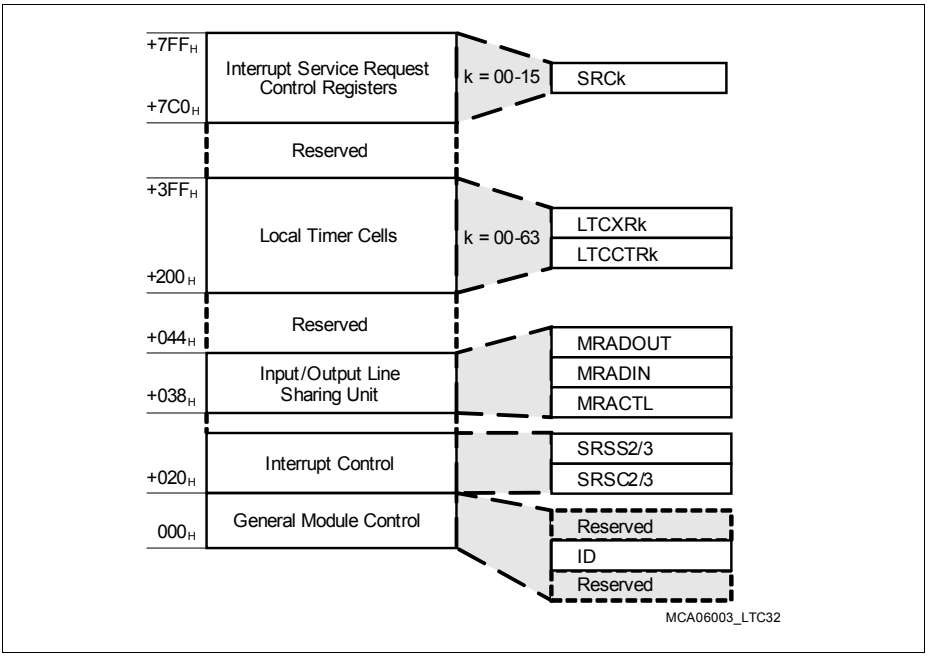


Figure 28-102LTCA2 Register Map

28.8 Revision History

This chapter gives a summary of recent changes within this specification.

Table 28-35 Revision History

Version Number	Changes to Previous Version
Rev_1.11	Modified the tables “PDR Assignment for GPTA®v5 Port Lines” in TC7197, TC1767, and TC1736 specifications. Included the Pad Classes in PDR assignment table. Included PDx description for A1 and F pad class. Table on On-Chip Trigger/Gating Multiplexer Control Register Assignments modified. For LTCA2 the numbering of the Output Groups was done consistently as OG3-OG6. Further more the Output Multiplexer of LTCA2 has been made consistently to be 0-3/4 and 7/10-13. OUT[65], OUT[76] and OUT[78] are marked as signals not available as output for GPTA1.
Rev_1.12	- Add to What’s new section: To be consistent to TC1797, the double connected input group of IOG3 is renamed to IOG6 and the Output Group OG1-7 are renamed to OG0-OG6 and the OG0 is renamed to IOG7. - Section ’Functionality of LTCA2; remove plural for LTCAs and double centence: The Local Timer Cell Array (LTCA2) provide a set of hardware cells required for high-speed digital signal processing - Add term input to LTC signal overview - Add ILM indication to LTCCTRk register and split register view to different modes - Change for registers SRSC0, SRSC1, SRSC2 and SRSC3 in footnote 1) zero to one - Add LTCA2 outputs for port 5 to IOCR Assigment table for TC1797 - Add footnote 1) and 2) to IOCR Assigment table for TC1797 - changed bit description for bit fileds OCM in order to allow bit extraction
Rev_1.13	- split registers GTCCTRk for timer mode into ILM = 0 and ILM = 1 views - remove some redundant sentense at the beginning of the implementation part - improve tables “IOCR Assignment for GPTA Port Lines” to cover the different packages - remove table for PCx Coding as redundant to port chapter - remove table for PDR Assignmemt for GPTA Port Lines as redundant to port chapter
Rev_1.14	- improve bit field description for GTCCTRk and LTCCTRk register bit fields OCM

29 Capture/Compare Unit 6 (CCU6)

The CCU6 is a high-resolution 16-bit capture and compare unit with application specific modes, mainly for AC drive control. Special operating modes support the control of Brushless DC-motors using Hall sensors or Back-EMF detection. Furthermore, block commutation and control mechanisms for multi-phase machines are supported.
It also supports inputs to start several timers synchronously, an important feature in devices with several CCU6 modules.

This chapter is structured as follows:

- Introduction (see **Section 29.1**)
  including register overview (see **Section 29.1.3**)
- Operating T12 (see **Section 29.2**)
  including T12-related registers (see **Section 29.2.8**)
  and capture/compare control registers (see **Section 29.2.9**)
- Operating T13 (see **Section 29.3**)
  including T13-related registers (see **Section 29.3.6**)
- Synchronous start feature (see **Section 29.4**)
- Trap handling (see **Section 29.5**)
- Multi-Channel mode (see **Section 29.6**)
- Hall sensor mode (see **Section 29.7**)
- Modulation control registers (see **Section 29.8**)
- Interrupt handling (see **Section 29.9**)
  including interrupt registers (see **Section 29.9.2**)
- General module operation (see **Section 29.10**)
  including general registers (see **Section 29.10.4**)
- Module implementation (see **Section 29.11**)

29.1 Introduction

The CCU6 unit is made up of a Timer T12 Block with three capture/compare channels and a Timer T13 Block with one compare channel. The T12 channels can independently generate PWM signals or accept capture triggers, or they can jointly generate control signal patterns to drive AC-motors or inverters.

A rich set of status bits, synchronized updating of parameter values via shadow registers, and flexible generation of interrupt request signals provide means for efficient software-control.

Note: The capture/compare module itself is named CCU6 (capture/compare unit 6).
A capture/compare channel inside this module is named CC6x.

29.1.1 Feature Set Overview

This section gives an overview over the different building blocks and their main features.

Timer 12 Block Features

- Three capture/compare channels, each channel can be used either as capture or as compare channel
- Generation of a three-phase PWM supported (six outputs, individual signals for high-side and low-side switches)
- 16-bit resolution, maximum count frequency = peripheral clock
- Dead-time control for each channel to avoid short-circuits in the power stage
- Concurrent update of T12 registers
- Center-aligned and edge-aligned PWM can be generated
- Single-shot mode supported
- Start can be controlled by external events
- Capability of counting external events
- Many interrupt request sources
- Hysteresis-like control mode

Timer 13 Block Features

- One independent compare channel with one output
- 16-bit resolution, maximum count frequency = peripheral clock
- Concurrent update of T13 registers
- Can be synchronized to T12
- Interrupt generation at period-match and compare-match
- Single-shot mode supported
- Start can be controlled by external events
- Capability of counting external events

Additional Specific Functions

- Block commutation for Brushless DC-drives implemented
- Position detection via Hall-sensor pattern
- Noise filter supported for position input signals
- Automatic rotational speed measurement and commutation control for block commutation
- Integrated error handling
- Fast emergency stop without CPU load via external signal ($\overline{\text{CTRAP}}$)
- Control modes for multi-channel AC-drives
- Output levels can be selected and adapted to the power stage

29.1.2 Block Diagram

The Timer T12 can operate in capture and/or compare mode for its three channels. The modes can also be combined (e.g. a channel operates in compare mode, whereas another channel operates in capture mode). The Timer T13 can operate in compare mode only. The multi-channel control unit generates output patterns which can be modulated by T12 and/or T13. The modulation sources can be selected and combined for the signal modulation.

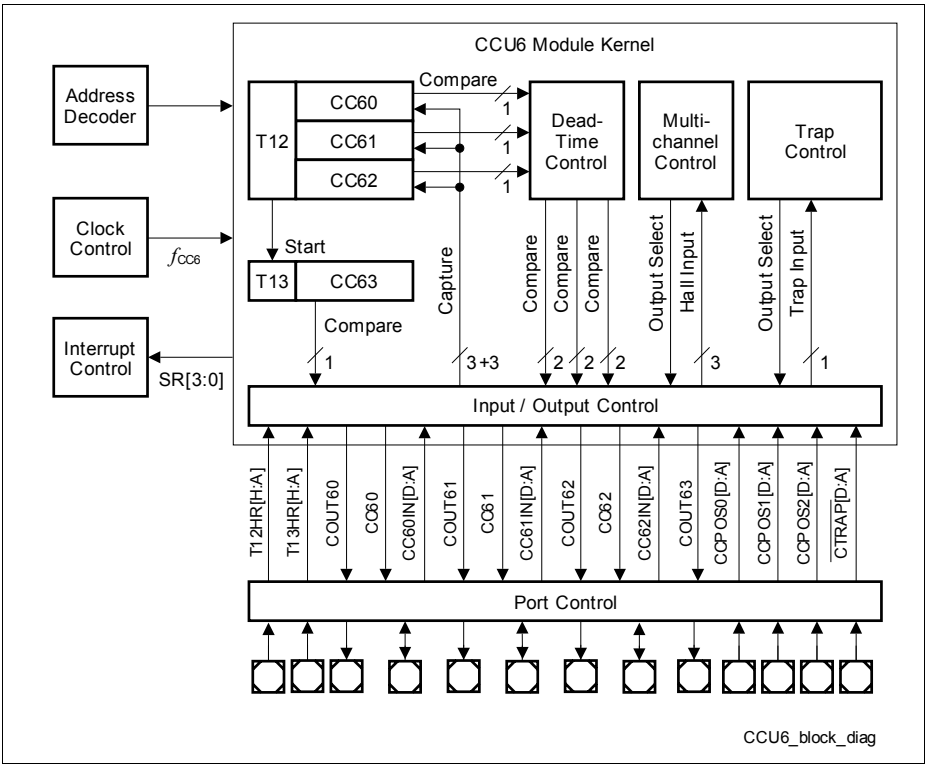


Figure 29-1 CCU6 Block Diagram

29.1.3 CCU6 Kernel Registers

For the generation of the overall register table, the prefix “CCU6x_” has to be added to the register names in this table to identify the registers of different CCU6 modules that are implemented. In this naming convention, x indicates the module number.

Table 29-1 shows all registers required for programming of a CCU6 module. It summarizes the CCU6 kernel registers and defines their offset addresses.

CCU6 Kernel Register Overview

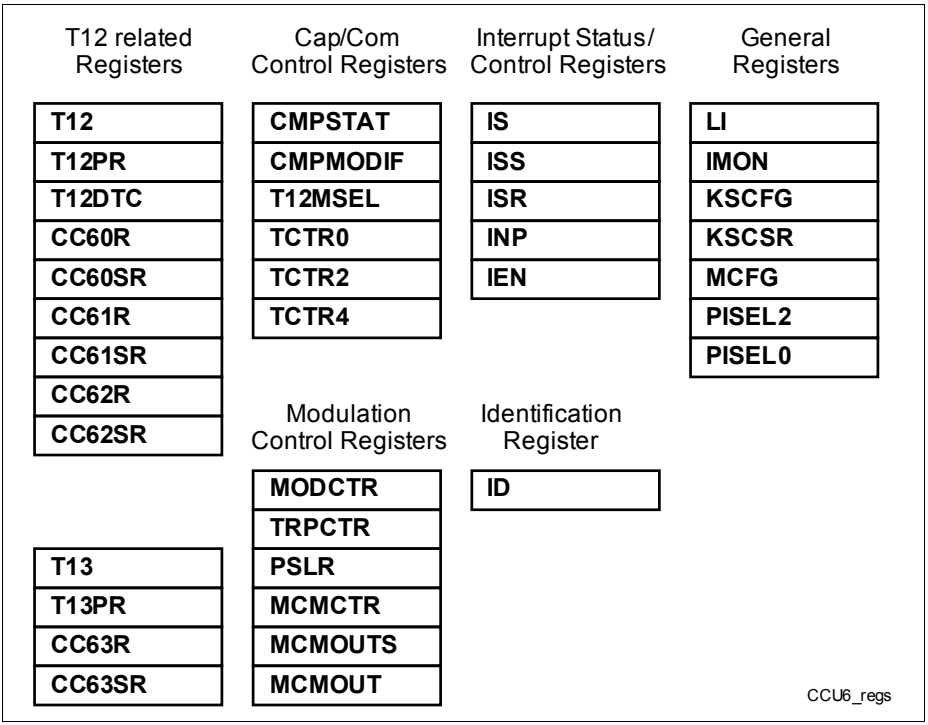


Figure 29-2 CCU6 Registers

Note: In the case of a write access to addresses inside the address range (that is covered by the same chip select signal), but that are not the addresses explicitly mentioned for the module, the write access is not taken into account for the module. The same principle is valid for read accesses. In case of a read access to another address, the module does not react.

*Note: The exact register address is given by the relative address of the register (given in **Table 29-1**) plus the kernel base address (given in **Table 29-14**) of the kernel.*

Table 29-1 CCU6 Module Registers

Register Short Name	Register Long Name	Offset Addr.	Access Mode		Reset Value	Reset	Page
			Read	Write			
General Registers							
ID	Module Identification Register	08_H	U, SV	U, SV	0000 54XX$_H$	Class 3	29-118
PISEL0	Port Input Select Register 0	10_H	U, SV	U, SV	0000 0000$_H$	Class 3	29-119
PISEL2	Port Input Select Register 2	14_H	U, SV	U, SV	0000 0000$_H$	Class 3	29-121
KSCFG	Kernel State Configuration Register	18_H	U, SV	U,SV	0000 0000$_H$	Class3/ Class 1, see Section 29.10.4.3	29-124
KSCSR	Kernel State Control Sensitivity Register	$1C_H$	U, SV	U,SV	0000 0000$_H$	Class 3	29-127
MCFG	Module Configuration Register	04_H	U, SV	U,SV	0000 007$_H$	Class 3	29-128
IMON	Input Monitoring Register	98_H	U, SV	U, SV	0000 0000$_H$	Class 3	29-130
LI	Lost Indicator Register	$9C_H$	U, SV	U, SV	0000 0000$_H$	Class 3	29-133
SRCx x = 0 - 3	Service Request Control Registers	$FC_H - x * 4_H$	U, SV	U, SV	0000 0000$_H$	Class 3	29-112

Table 29-1 CCU6 Module Registers (cont'd)

Register Short Name	Register Long Name	Offset Addr.	Access Mode		Reset Value	Reset	Page
			Read	Write			
Timer T12 related Registers							
T12	Timer 12 Counter Register	20_H	U, SV	U, SV	0000 0000_H	Class 3	29-35
T12PR	Timer 12 Period Register	24_H	U, SV	U, SV	0000 0000_H	Class 3	29-36
T12DTC	Dead-Time Control Register for Timer T12	28_H	U, SV	U, SV	0000 0000_H	Class 3	29-39
CC60R	Capture/Compare Register Channel CC60	30_H	U, SV	U,SV	0000 0000_H	Class 3	29-37
CC61R	Capture/Compare Register Channel CC61	34_H	U, SV	U,SV	0000 0000_H	Class 3	29-37
CC62R	Capture/Compare Register Channel CC62	38_H	U, SV	U,SV	0000 0000_H	Class 3	29-37
CC60SR	Capture/Compare Shadow Register Channel CC60	40_H	U, SV	U, SV	0000 0000_H	Class 3	29-38
CC61SR	Capture/Compare Shadow Register Channel CC61	44_H	U, SV	U, SV	0000 0000_H	Class 3	29-38

Table 29-1 CCU6 Module Registers (cont'd)

Register Short Name	Register Long Name	Offset Addr.	Access Mode		Reset Value	Reset	Page
			Read	Write			
CC62SR	Capture/Compare Shadow Register Channel CC62	48_H	U, SV	U, SV	0000 0000_H	Class 3	29-38
Capture/Compare Control Registers							
CMPSTAT	Compare State Register	60_H	U, SV	U, SV	0000 0000_H	Class 3	29-41
CMPMODIF	Compare State Modification Register	64_H	U, SV	U, SV	0000 0000_H	Class 3	29-44
T12MSEL	T12 Capture/Compare Mode Select Register	68_H	U, SV	U, SV	0000 0000_H	Class 3	29-45
TCTR0	Timer Control Register 0	70_H	U, SV	U, SV	0000 0000_H	Class 3	29-46
TCTR2	Timer Control Register 2	74_H	U, SV	U, SV	0000 0000_H	Class 3	29-50
TCTR4	Timer Control Register 4	78_H	U, SV	U, SV	0000 0000_H	Class 3	29-53
Timer T13 related Registers							
T13	Timer 13 Counter Register	50_H	U, SV	U, SV	0000 0000_H	Class 3	29-68
T13PR	Timer 13 Period Register	54_H	U, SV	U, SV	0000 0000_H	Class 3	29-69

Table 29-1 CCU6 Module Registers (cont'd)

Register Short Name	Register Long Name	Offset Addr.	Access Mode		Reset Value	Reset	Page
			Read	Write			
CC63R	Compare Register for Timer 13	58_H	U, SV	U,SV	0000 0000_H	Class 3	29-70
CC63SR	Compare Shadow Register for Timer 13	$5C_H$	U, SV	U, SV	0000 0000_H	Class 3	29-71
Modulation Control Registers							
MODCTR	Modulation Control Register	80_H	U, SV	U, SV	0000 0000_H	Class 3	29-85
TRPCTR	Trap Control Register	84_H	U, SV	U, SV	0000 0000_H	Class 3	29-87
PSLR	Passive State Level Register	88_H	U, SV	U, SV	0000 0000_H	Class 3	29-90
MCMOUTS	Multi-Channel Mode Output Shadow Register	$8C_H$	U, SV	U, SV	0000 0000_H	Class 3	29-94
MCMOUT	Multi-Channel Mode Output Register	90_H	U, SV	U,SV	0000 0000_H	Class 3	29-95
MCMCTR	Multi-Channel Mode Control Register	94_H	U, SV	U, SV	0000 0000_H	Class 3	29-91
Interrupt Status and Node Registers							

Table 29-1 CCU6 Module Registers (cont'd)

Register Short Name	Register Long Name	Offset Addr.	Access Mode		Reset Value	Reset	Page
			Read	Write			
IS	Interrupt Status Register	$A0_H$	U, SV	U,SV	$0000\ 0000_H$	Class 3	29-100
ISS	Interrupt Status Set Register	$A4_H$	U, SV	U, SV	$0000\ 0000_H$	Class 3	29-103
ISR	Interrupt Status Reset Register	$A8_H$	U, SV	U, SV	$0000\ 0000_H$	Class 3	29-105
INP	Interrupt Node Pointer Register	AC_H	U, SV	U, SV	$0000\ 3940_H$	Class 3	29-110
IEN	Interrupt Node Pointer Register	$B0_H$	U, SV	U, SV	$0000\ 0000_H$	Class 3	29-107

29.2 Operating Timer T12

The timer T12 block is the main unit to generate the 3-phase PWM signals. A 16-bit counter is connected to 3 channel registers via comparators, that generate a signal when the counter contents match one of the channel register contents. A variety of control functions facilitate the adaptation of the T12 structure to different application needs.
Besides the 3-phase PWM generation, the T12 block offers options for individual compare and capture functions, as well as dead-time control and hysteresis-like compare mode.

This section provides information about:

- T12 overview (see **Section 29.2.1**)
- Counting scheme (see **Section 29.2.2**)
- Compare modes (see **Section 29.2.3**)
- Compare mode output path (see **Section 29.2.4**)
- Capture modes (see **Section 29.2.5**)
- Shadow transfer (see **Section 29.2.6**)
- T12 operating mode selection (see **Section 29.2.7**)
- T12 register description (see **Section 29.2.8**

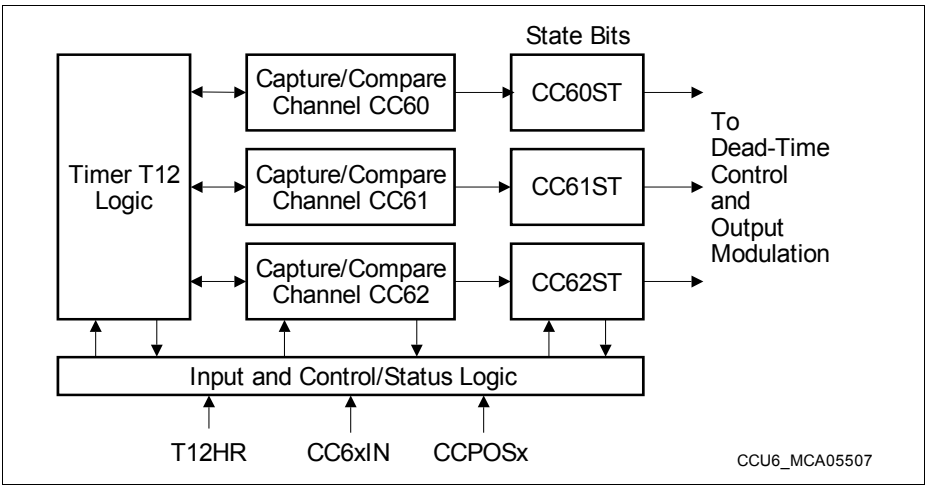


Figure 29-3 Overview Diagram of the Timer T12 Block

29.2.1 T12 Overview

Figure 29-4 shows a detailed block diagram of Timer T12. The functions of the timer T12 block are controlled by bits in registers **TCTR0**, **TCTR2**, and **PISEL0**.

Timer T12 receives its input clock (f_{T12}) from the module clock f_{CC6} via a programmable prescaler and an optional 1/256 divider or from an input signal T12HR. These options are controlled via bit fields T12CLK and T12PRE (see **Table 29-2**). T12 can count up or down, depending on the selected operation mode. A direction flag, CDIR, indicates the current counting direction.

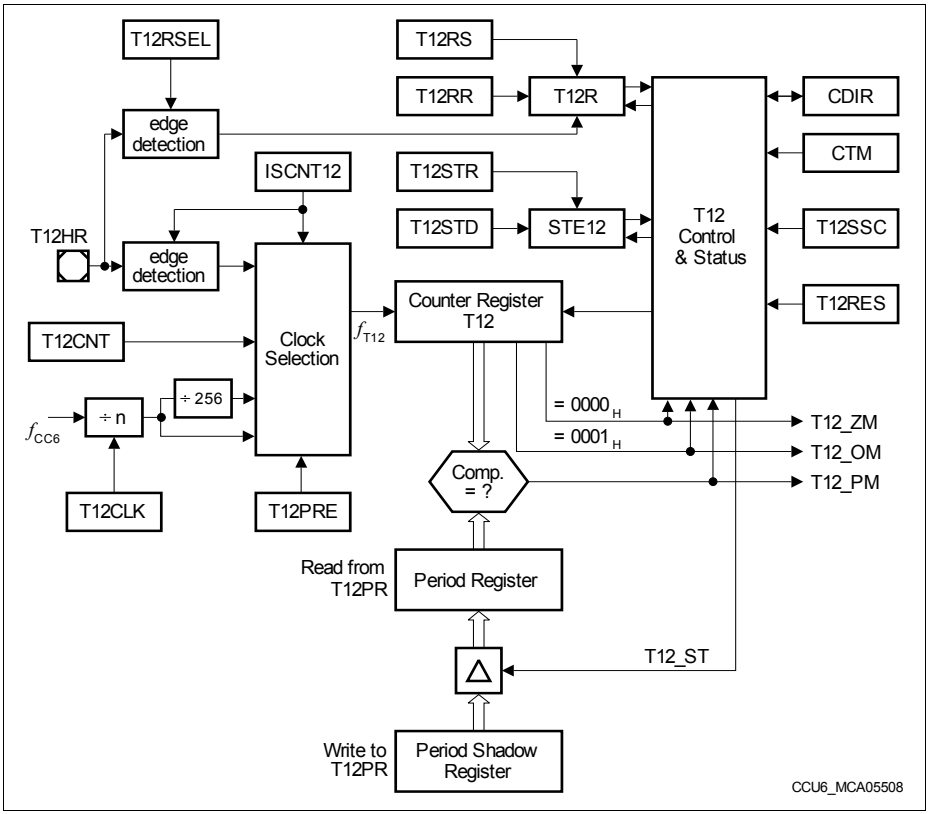


Figure 29-4 Timer T12 Logic and Period Comparators

Via a comparator, the T12 counter register **T12** is connected to a Period Register **T12PR**. This register determines the maximum count value for T12.

In Edge-Aligned mode, T12 is cleared to 0000_H after it has reached the period value defined by T12PR. In Center-Aligned mode, the count direction of T12 is set from ‘up’ to

‘down’ after it has reached the period value (please note that in this mode, T12 exceeds the period value by one before counting down). In both cases, signal T12_PM (T12 Period Match) is generated. The Period Register receives a new period value from its Shadow Period Register.
A read access to T12PR delivers the current period value at the comparator, whereas a write access targets the Shadow Period Register to prepare another period value. The transfer of a new period value from the Shadow Period Register into the Period Register (see **Section 29.2.6**) is controlled via the ‘T12 Shadow Transfer’ control signal, T12_ST. The generation of this signal depends on the operating mode and on the shadow transfer enable bit STE12. Providing a shadow register for the period value as well as for other values related to the generation of the PWM signal allows a concurrent update by software for all relevant parameters.
Two further signals indicate whether the counter contents are equal to 0000_H (T12_ZM = zero match) or 0001_H (T12_OM = one match). These signals control the counting and switching behavior of T12.

The basic operating mode of T12, either Edge-Aligned mode (**Figure 29-5**) or Center-Aligned mode (**Figure 29-6**), is selected via bit CTM. A Single-Shot control bit, T12SSC, enables an automatic stop of the timer when the current counting period is finished (see **Figure 29-7** and **Figure 29-8**).

The start or stop of T12 is controlled by the Run bit T12R that can be modified by bits in register **TCTR4**. The run bit can be set/cleared by software via the associated set/clear bits T12RS or T12RR, it can be set by a selectable edge of the input signal T12HR (**TCTR2**.T12RSEL), or it is cleared by hardware according to preselected conditions.
The timer T12 run bit T12R must not be set while the applied T12 period value is zero.
Timer T12 can be cleared via control bit T12RES. Setting this write-only bit does only clear the timer contents, but has no further effects, for example, it does not stop the timer.

The generation of the T12 shadow transfer control signal, T12_ST, is enabled via bit STE12. This bit can be set or reset by software indirectly through its associated set/clear control bits T12STR and T12STD.
While Timer T12 is running, write accesses to the count register T12 are not taken into account. If T12 is stopped and the Dead-Time counters are 0, write actions to register T12 are immediately taken into account.

29.2.2 T12 Counting Scheme

This section describes the clocking and counting capabilities of T12.

29.2.2.1 Clock Selection

In **Timer Mode** (**PISEL2**.ISCNT12 = 00_B), the input clock f_{T12} of Timer T12 is derived from the internal module clock f_{CC6} through a programmable prescaler and an optional 1/256 divider. The resulting prescaler factors are listed in **Table 29-2**. The prescaler of T12 is cleared while T12 is not running (**TCTR0**.T12R = 0) to ensure reproducible timings and delays.

Table 29-2 Timer T12 Input Frequency Options

T12CLK	Resulting Input Clock f_{T12} Prescaler Off (T12PRE = 0)	Resulting Input Clock f_{T12} Prescaler On (T12PRE = 1)
000_B	f_{CC6}	f_{CC6} / 256
001_B	f_{CC6} / 2	f_{CC6} / 512
010_B	f_{CC6} / 4	f_{CC6} / 1024
011_B	f_{CC6} / 8	f_{CC6} / 2048
100_B	f_{CC6} / 16	f_{CC6} / 4096
101_B	f_{CC6} / 32	f_{CC6} / 8192
110_B	f_{CC6} / 64	f_{CC6} / 16384
111_B	f_{CC6} / 128	f_{CC6} / 32768

In **Counter Mode**, timer T12 counts one step:

- If a 1 is written to **TCTR4**.T12CNT and **PISEL2**.ISCNT12 = 01_B
- If a rising edge of input signal T12HR is detected and **PISEL2**.ISCNT12 = 10_B
- If a falling edge of input signal T12HR is detected and **PISEL2**.ISCNT12 = 11_B

29.2.2.2 Edge-Aligned / Center-Aligned Mode

In **Edge-Aligned Mode** (CTM = 0), timer T12 is always counting upwards (CDIR = 0). When reaching the value given by the period register (period-match T12_PM), the value of T12 is cleared with the next counting step (saw tooth shape).

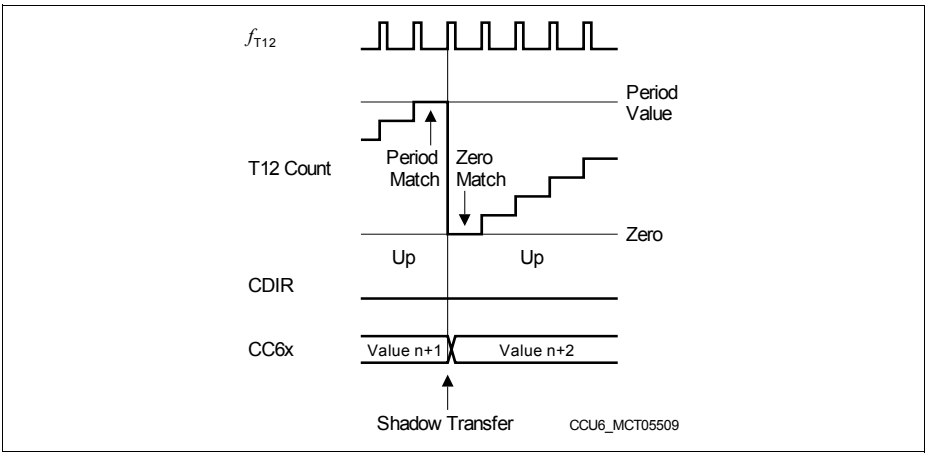


Figure 29-5 T12 Operation in Edge-Aligned Mode

As a result, in Edge-Aligned mode, the timer period is given by:

$$T12_{PER} = \text{<Period-Value>} + 1; \text{ in T12 clocks } (f_{T12}) \quad (29.1)$$

In **Center-Aligned Mode** (CTM = 1), timer T12 is counting upwards or downwards (triangular shape). When reaching the value given by the period register (period-match T12_PM) while counting upwards (CDIR = 0), the counting direction control bit CDIR is changed to downwards (CDIR = 1) with the next counting step.
When reaching the value 0001_H (one-match T12_OM) while counting downwards, the counting direction control bit CDIR is changed to upwards with the next counting step.

As a result, in Center.Aligned mode, the timer period is given by:

$$T12_{PER} = (\text{<Period-Value>} + 1) \times 2; \text{ in T12 clocks } (f_{T12}) \quad (29.2)$$

- With the next clock event of f_{T12} the count direction is set to counting up (CDIR = 0) when the counter reaches 0001_H while counting down.
- With the next clock event of f_{T12} the count direction is set to counting down (CDIR = 1) when the Period-Match is detected while counting up.
- With the next clock event of f_{T12} the counter counts up while CDIR = 0 and it counts down while CDIR = 1.

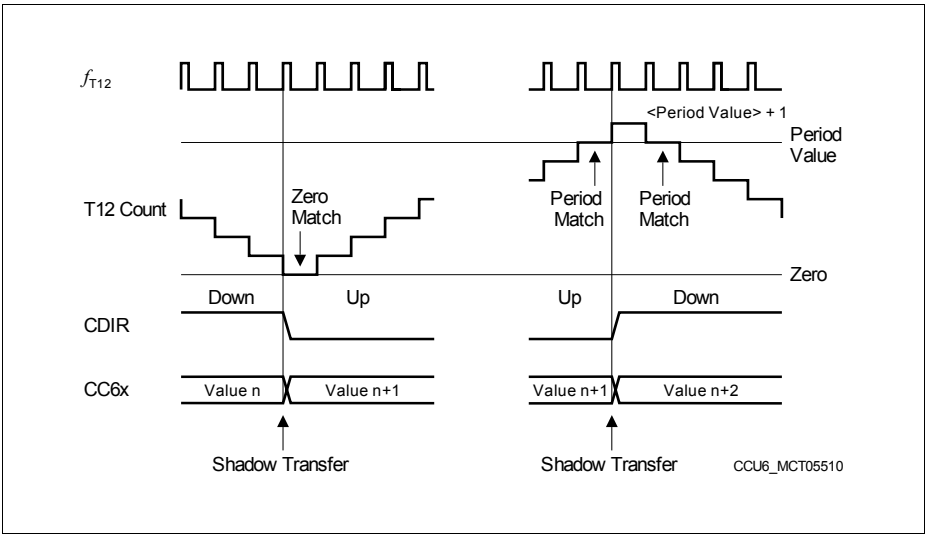


Figure 29-6 T12 Operation in Center-Aligned Mode

*Note: Bit CDIR changes with the next timer clock event after the one-match or the period-match. Therefore, the timer continues counting in the previous direction for one cycle before actually changing its direction (see **Figure 29-6**).*

29.2.2.3 Single-Shot Mode

In Single-Shot Mode, the timer run bit T12R is cleared by hardware. If bit T12SSC = 1, the timer T12 will stop when the current timer period is finished.

In Edge-Aligned mode, T12R is cleared when the timer becomes zero after having reached the period value (see **Figure 29-7**).

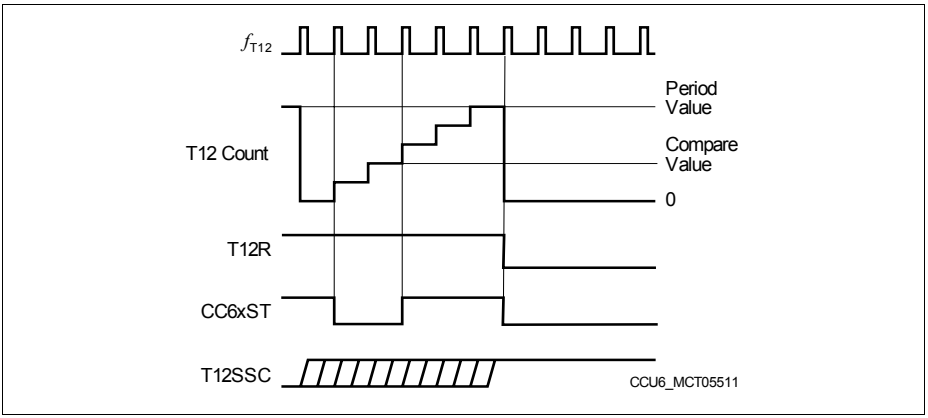


Figure 29-7 Single-Shot Operation in Edge-Aligned Mode

In Center-Aligned mode, the period is finished when the timer has counted down to zero (one clock cycle after the one-match while counting down, see **Figure 29-8**).

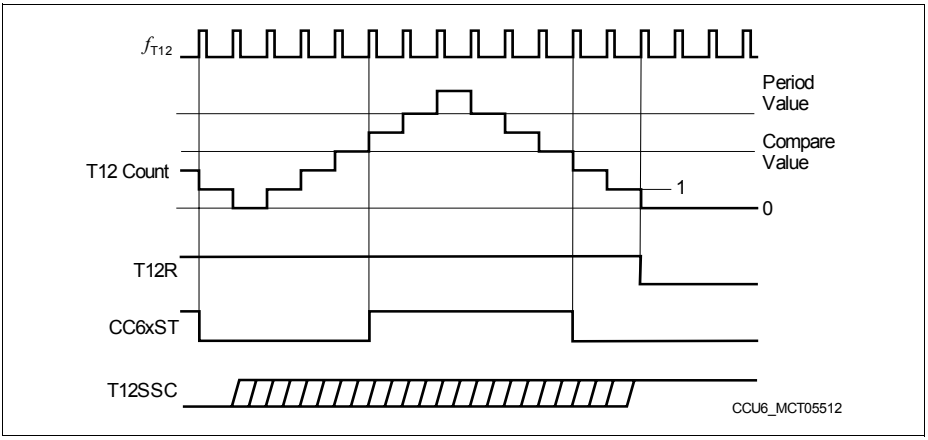


Figure 29-8 Single-Shot Operation in Center-Aligned Mode

29.2.3 T12 Compare Mode

Associated with Timer T12 are three individual capture/compare channels, that can perform compare or capture operations with regard to the contents of the T12 counter. The capture functions are explained in **Section 29.2.5**.

29.2.3.1 Compare Channels

In Compare Mode (see **Figure 29-9**), the three individual compare channels CC60 CC61, and CC62 can generate a three-phase PWM pattern.

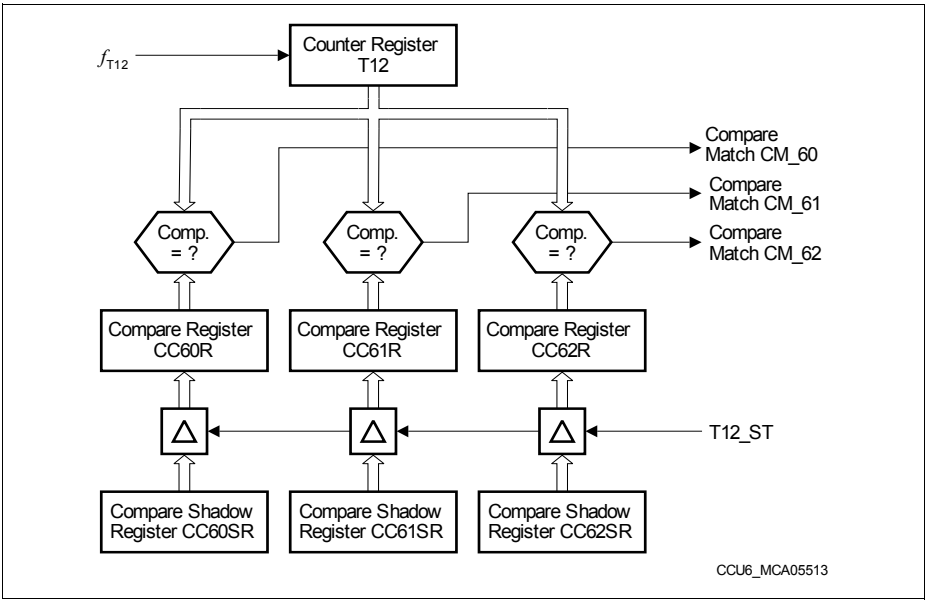


Figure 29-9 T12 Channel Comparators

Each compare channel is connected to the T12 counter register via its individual equal-to comparator, generating a match signal when the contents of the counter matches the contents of the associated compare register. Each channel consists of the comparator and a double register structure - the actual compare register CC6xR, feeding the comparator, and an associated shadow register CC6xSR, that is preloaded by software and transferred into the compare register when signal T12 shadow transfer, T12_ST, gets active. Providing a shadow register for the compare value as well as for other values related to the generation of the PWM signal facilitates a concurrent update by software for all relevant parameters of a three-phase PWM.

29.2.3.2 Channel State Bits

Associated with each (compare) channel is a State Bit, **CMPSTAT**.CC6xST, holding the status of the compare (or capture) operation (see **Figure 29-10**). In compare mode, the State Bits are modified according to a set of switching rules, depending on the current status of timer T12.

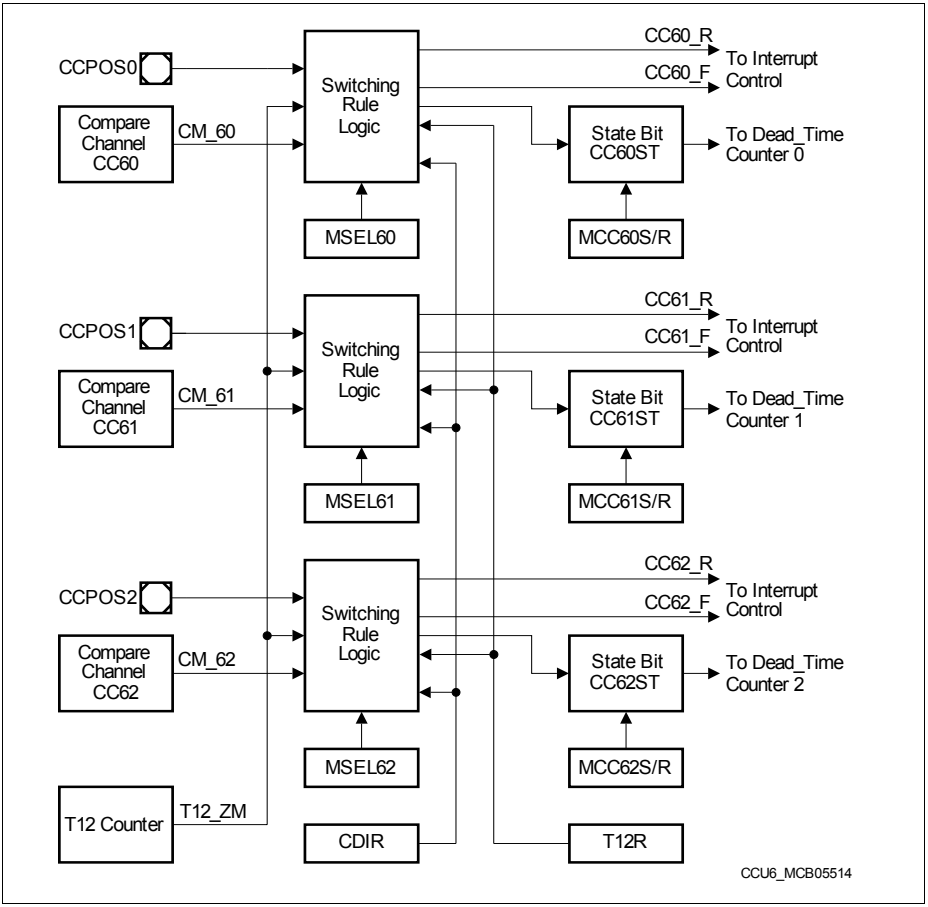


Figure 29-10 Compare State Bits for Compare Mode

The inputs to the switching rule logic for the CC6xST bits are the timer direction (CDIR), the timer run bit (T12R), the timer T12 zero-match signal (T12_ZM), and the actual individual compare-match signals CM_6x as well as the mode control bits, **T12MSEL**.MSEL6x.

In addition, each state bit can be set or cleared by software via the appropriate set and reset bits in register **CMPMODIF**, MCC6xS and MCC6xR. The input signals CCPOSx are used in hysteresis-like compare mode, whereas in normal compare mode, these inputs are ignored.

Note: In Hall Sensor, single shot or capture modes, additional/different rules are taken into account (see related sections).

A compare interrupt event CC6x_R is signaled when a compare match is detected while counting upwards, whereas the compare interrupt event CC6x_F is signaled when a compare match is detected while counting down. The actual setting of a State Bit has no influence on the interrupt generation in compare mode.

A modification of a State Bit CC6xST by the switching rule logic due to a compare action is only possible while Timer T12 is running (T12R = 1). If this is the case, the following switching rules apply for setting and clearing the State Bits in Compare Mode (illustrated in **Figure 29-11** and **Figure 29-12**):

A State Bit **CC6xST is set** to 1:

- with the next T12 clock (f_{T12}) after a compare-match when T12 is counting up (i.e., when the counter is incremented above the compare value);
- with the next T12 clock (f_{T12}) after a zero-match AND a parallel compare-match when T12 is counting up.

A State Bit **CC6xST is cleared** to 0:

- with the next T12 clock (f_{T12}) after a compare-match when T12 is counting down (i.e., when the counter is decremented below the compare value in center-aligned mode);
- with the next T12 clock (f_{T12}) after a zero-match AND NO parallel compare-match when T12 is counting up.

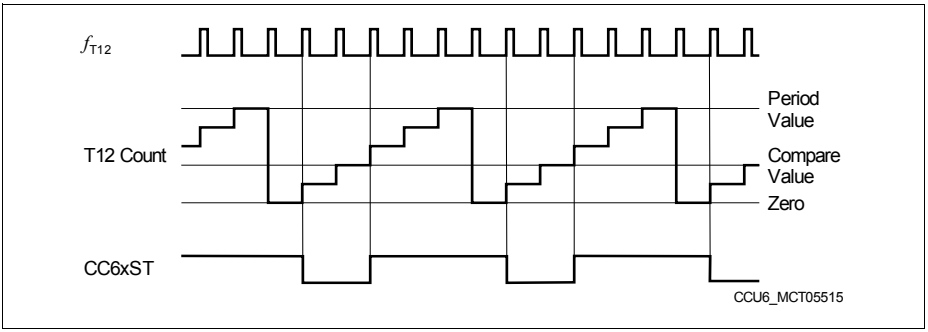


Figure 29-11 Compare Operation, Edge-Aligned Mode

Figure 29-13 illustrates some more examples for compare waveforms. It is important to note that in these examples, it is assumed that some of the compare values are changed

while the timer is running. This change is performed via a software preload of the Shadow Register, CC6xSR. The value is transferred to the actual Compare Register CC6xR with the T12 Shadow Transfer signal, T12_ST, that is assumed to be enabled.

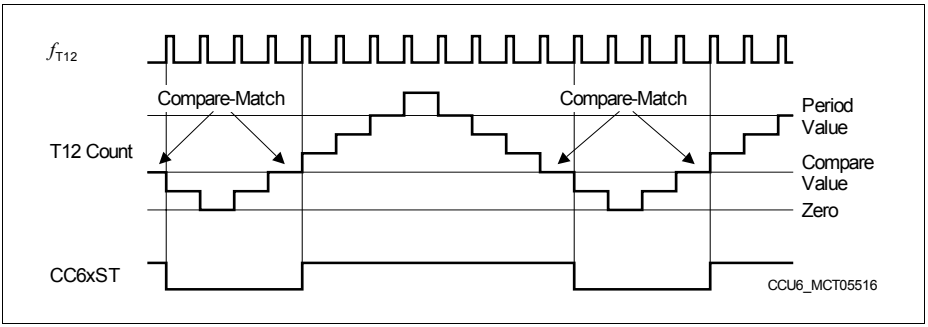


Figure 29-12 Compare Operation, Center-Aligned Mode

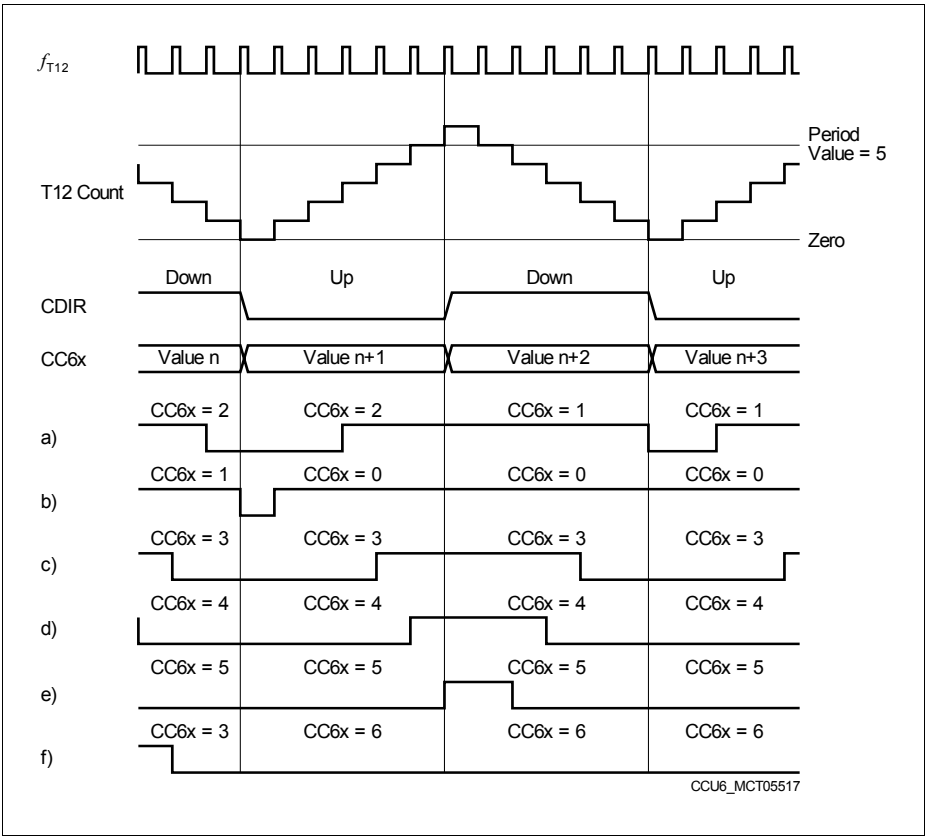


Figure 29-13 Compare Waveform Examples

Example b) illustrates the transition to a duty cycle of 100%. First, a compare value of 0001_H is used, then changed to 0000_H. Please note that a low pulse with the length of one T12 clock is still produced in the cycle where the new value 0000_H is in effect; this pulse originates from the previous value 0001_H. In the following timer cycles, the State Bit CC6xST remains at 1, producing a 100% duty cycle signal. In this case, the compare rule ‘zero-match AND compare-match’ is in effect.

Example f) shows the transition to a duty cycle of 0%. The new compare value is set to <Period-Value> + 1, and the State Bit CC6ST remains cleared.

Figure 29-14 illustrates an example for the waveforms of all three channels. With the appropriate dead-time control and output modulation, a very efficient 3-phase PWM signal can be generated.

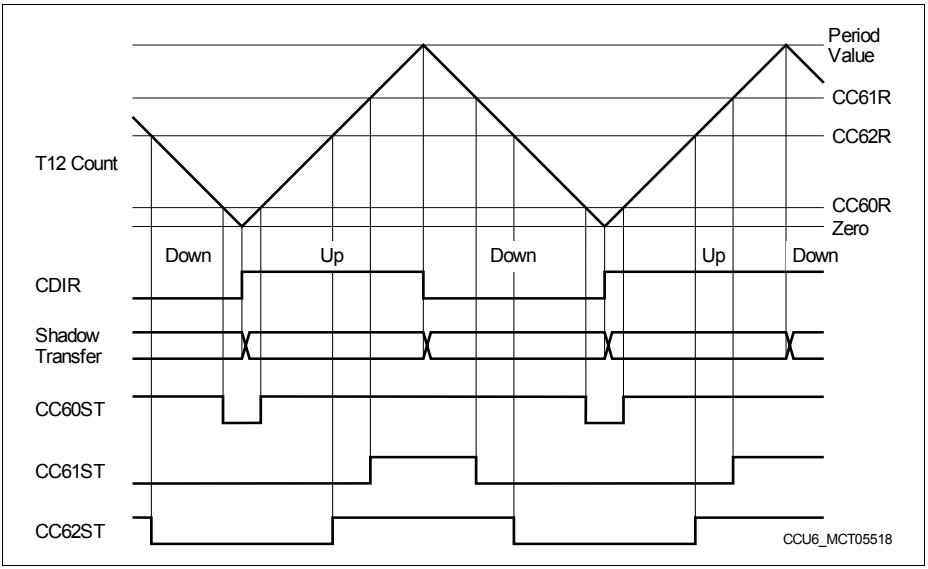


Figure 29-14 Three-Channel Compare Waveforms

29.2.3.3 Hysteresis-Like Control Mode

The hysteresis-like control mode (**T12MSEL**.MSEL6x = 1001_B) offers the possibility to switch off the PWM output if the input CCPOSx becomes 0 by clearing the State Bit CC6xST. This can be used as a simple motor control feature by using a comparator indicating, e.g., overcurrent. While CCPOSx = 0, the PWM outputs of the corresponding channel are driving their passive levels, because the setting of bit CC6xST is only possible while CCPOSx = 1.
As long as input CCPOSx is 0, the corresponding State Bit is held 0. When CCPOSx is at high level, the outputs can be in active state and are determined by bit CC6xST (see **Figure 29-10** for the state bit logic and **Figure 29-15** for the output paths).
The CCPOSx inputs are evaluated with f_{CC6}.

This mode can be used to introduce a timing-related behavior to a hysteresis controller. A standard hysteresis controller detects if a value exceeds a limit and switches its output according to the compare result. Depending on the operating conditions, the switching frequency and the duty cycle are not fixed, but change permanently.

If (outer) time-related control loops based on a hysteresis controller in an inner loop should be implemented, the outer loops show a better behavior if they are synchronized to the inner loops. Therefore, the hysteresis-like mode can be used, that combines timer-related switching with a hysteresis controller behavior. For example, in this mode, an output can be switched on according to a fixed time base, but it is switched off as soon as a falling edge is detected at input CCPOSx.

This mode can also be used for standard PWM with overcurrent protection. As long as there is no low level signal at pin CCPOSx, the output signals are generated in the normal manner as described in the previous sections. Only if input CCPOSx shows a low level, e.g. due to the detection of overcurrent, the outputs are shut off to avoid harmful stress to the system.

29.2.4 Compare Mode Output Path

Figure 29-15 gives an overview on the signal path from a channel State Bit to its output pin in its simplest form. As illustrated, a user has a variety of controls to determine the desired output signal switching behavior in relation to the current state of the State Bit, CC6xST. Please refer to **Section 29.2.4.3** for details on the output modulation.

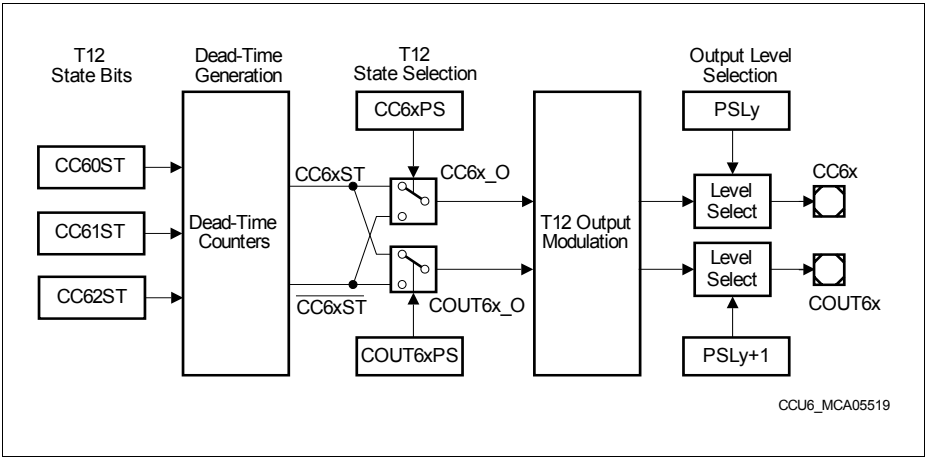


Figure 29-15 Compare Mode Simplified Output Path Diagram

The output path is based on signals that are defined as active or passive. The terms active and passive are not related to output levels, but to internal actions. This mainly applies for the modulation, where T12 and T13 signals are combined with the multi-channel signals and the trap function. The Output level Selection allows the user to define the output level at the output pin for the passive state (inverted level for the active state). It is recommended to configure this block in a way that an external power switch is switched off while the CCU6 delivers an output signal in the passive state.

29.2.4.1 Dead-Time Generation

The generation of (complementary) signals for the high-side and the low-side switches of one power inverter phase is based on the same compare channel. For example, if the high-side switch should be active while the T12 counter value is above the compare value (State Bit = 1), then the low-side switch should be active while the counter value is below the compare value (State Bit = 0).

In most cases, the switching behavior of the connected power switches is not symmetrical concerning the switch-on and switch-off times. A general problem arises if the time for switch-on is smaller than the time for switch-off of the power device. In this case, a short-circuit can occur in the inverter bridge leg, which may damage the complete system. In order to solve this problem by HW, this capture/compare unit

contains a programmable Dead-Time Generation Block, that delays the passive to active edge of the switching signals by a programmable time (the active to passive edge is not delayed).

The Dead-Time Generation Block, illustrated in **Figure 29-16**, is built in a similar way for all three channels of T12. It is controlled by bits in register **T12DTC**. Any change of a CC6xST State Bit activates the corresponding Dead-Time Counter, that is clocked with the same input clock as T12 (f_{T12}). The length of the dead-time can be programmed by bit field DTM. This value is identical for all three channels. Writing **TCTR4**.DTRES = 1 sets all dead-times to passive.

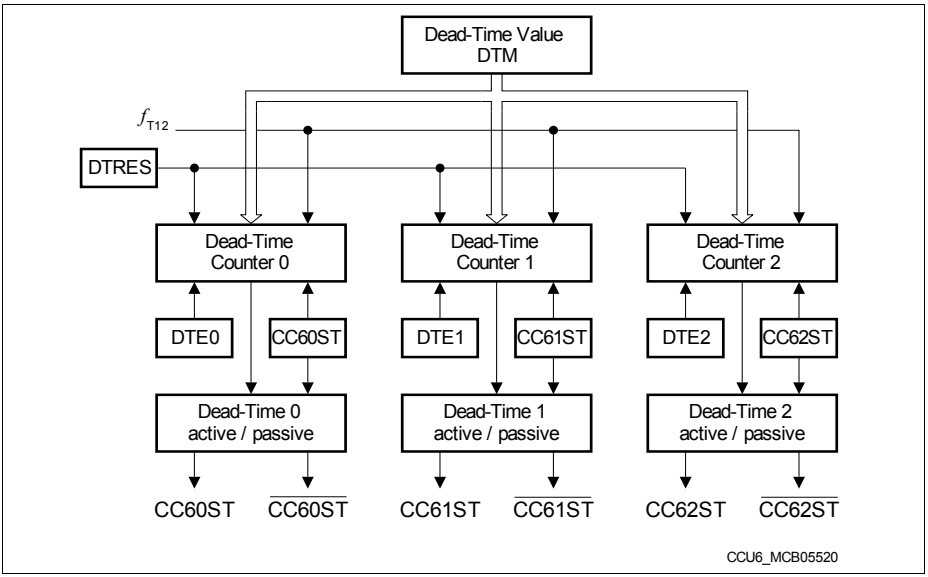


Figure 29-16 Dead-Time Generation Block Diagram

Each of the three dead-time counters has its individual dead-time enable bit, DTEx. An enabled dead-time counter generates a dead-time delaying the passive-to-active edge of the channel output signal. The change in a State Bit CC6xST is not taken into account while the dead-time generation of this channel is currently in progress (active). This avoids an unintentional additional dead-time if a State Bit CC6xST changes too early.
A disabled dead-time counter is always considered as passive and does not delay any edge of CC6xST.
Based on the State Bits CC6xST, the Dead-Time Generation Block outputs a direct signal CC6xST and an inverted signal $\overline{CC6xST}$ for each compare channel, each masked with the effect of the related Dead-Time Counters (waveforms illustrated in **Figure 29-17**).

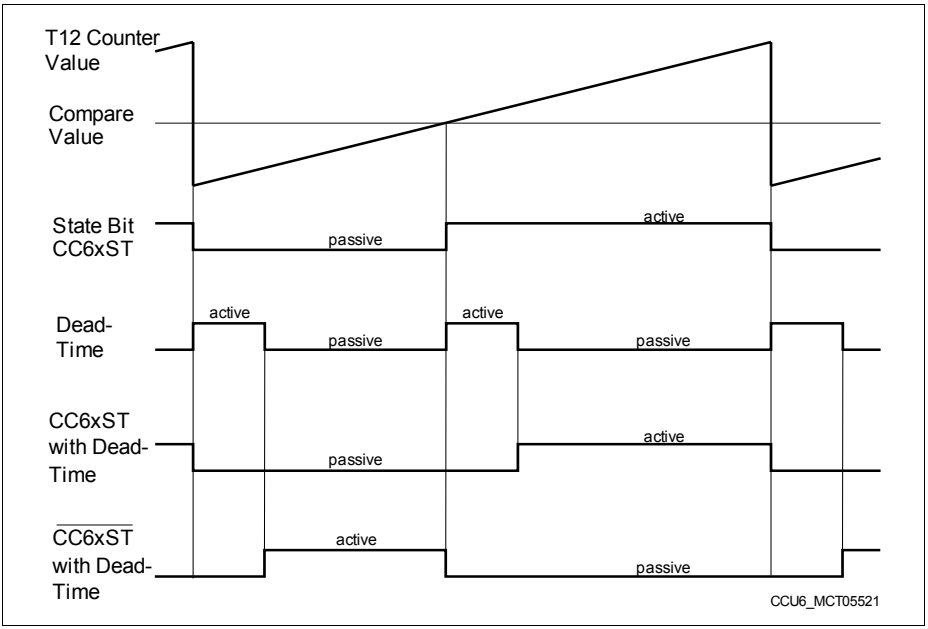


Figure 29-17 Dead-Time Generation Waveforms

29.2.4.2 State Selection

To support a wide range of power switches and drivers, the state selection offers the flexibility to define when an output can be active and can be modulated, especially useful for **complementary or multi-phase PWM** signals.

The state selection is based on the signals CC6xST and $\overline{\text{CC6xST}}$ delivered by the dead-time generator (see **Figure 29-15**). Both signals are never active at the same time, but can be passive at the same time. This happens during the dead-time of each compare channel after a change of the corresponding State Bit CC6xST.

The user can select independently for each output signal CC6xO and COUT6xO if it should be active before or after the compare value has been reached (see register **CMPSTAT**). With this selection, the active (conducting) phases of complementary power switches in a power inverter bridge leg can be positioned with respect to the compare value (e.g. signal CC6xO can be active before, whereas COUT6xO can be active after the compare value is reached). Like this, the output modulation, the trap logic and the output level selection can be programmed independently for each output signal, although two output signals are referring to the same compare channel.

29.2.4.3 Output Modulation and Level Selection

The last block of the data path is the Output Modulation block. Here, all the modulation sources and the trap functionality are combined and control the actual level of the output pins (controlled by the modulation enable bits T1xMODENy and MCMEN in register **MODCTR**). The following signal sources can be combined here **for each T12 output signal** (see **Figure 29-18** for compare channel CC60):

- A **T12 related compare signal** CC6x_O (for outputs CC6x) or COUT6x_O (for outputs COUT6x) delivered by the T12 block (state selection with dead-time) with an individual enable bit T12MODENy per output signal (y = 0, 2, 4 for outputs CC6x and y = 1, 3, 5 for outputs COUT6x)
- The **T13 related compare signal** CC63_O delivered by the T13 state selection with an individual enable bit T13MODENy per output signal (y = 0, 2, 4 for outputs CC6x and y = 1, 3, 5 for outputs COUT6x)
- A **multi-channel output signal** MCMPy (y = 0, 2, 4 for outputs CC6x and y = 1, 3, 5 for outputs COUT6x) with a common enable bit MCMEN
- The **trap state** TRPS with an individual enable bit TRPENy per output signal (y = 0, 2, 4 for outputs CC6x and y = 1, 3, 5 for outputs COUT6x)

If one of the modulation input signals CC6x_O/COUT6x_O, CC63_O, or MCMPy of an output modulation block is enabled and is at passive state, the modulated is also in passive state, regardless of the state of the other signals that are enabled. Only if all enabled signals are in active state the modulated output shows an active state. If no modulation input is enabled, the output is in passive state.
If the Trap State is active (TRPS = 1), then the outputs that are enabled for the trap signal (by TRPENy = 1) are set to the passive state.

The output of each of the modulation control blocks is connected to a level select block that is configured by register **PSLR**. It offers the option to determine the actual output level of a pin, depending on the state of the output line (decoupling of active/passive state and output polarity) as specified by the Passive State Select bit PSLy. If the modulated output signal is in the passive state, the level specified directly by PSLy is output. If it is in the active state, the inverted level of PSLy is output. This allows the user to adapt the polarity of an active output signal to the connected circuitry.

The PSLy bits have shadow registers to allow for updates without undesired pulses on the output lines. The bits related to CC6x and COUT6x (x = 0, 1, 2) are updated with the T12 shadow transfer signal (T12_ST). A read action returns the actually used values, whereas a write action targets the shadow bits. Providing a shadow register for the PSL value as well as for other values related to the generation of the PWM signal facilitates a concurrent update by software for all relevant parameters.

Figure 29-18 shows the output modulation structure for compare channel CC60 (output signals CC60 and COUT60). A similar structure is implemented for the other two compare channels CC61 and CC62.

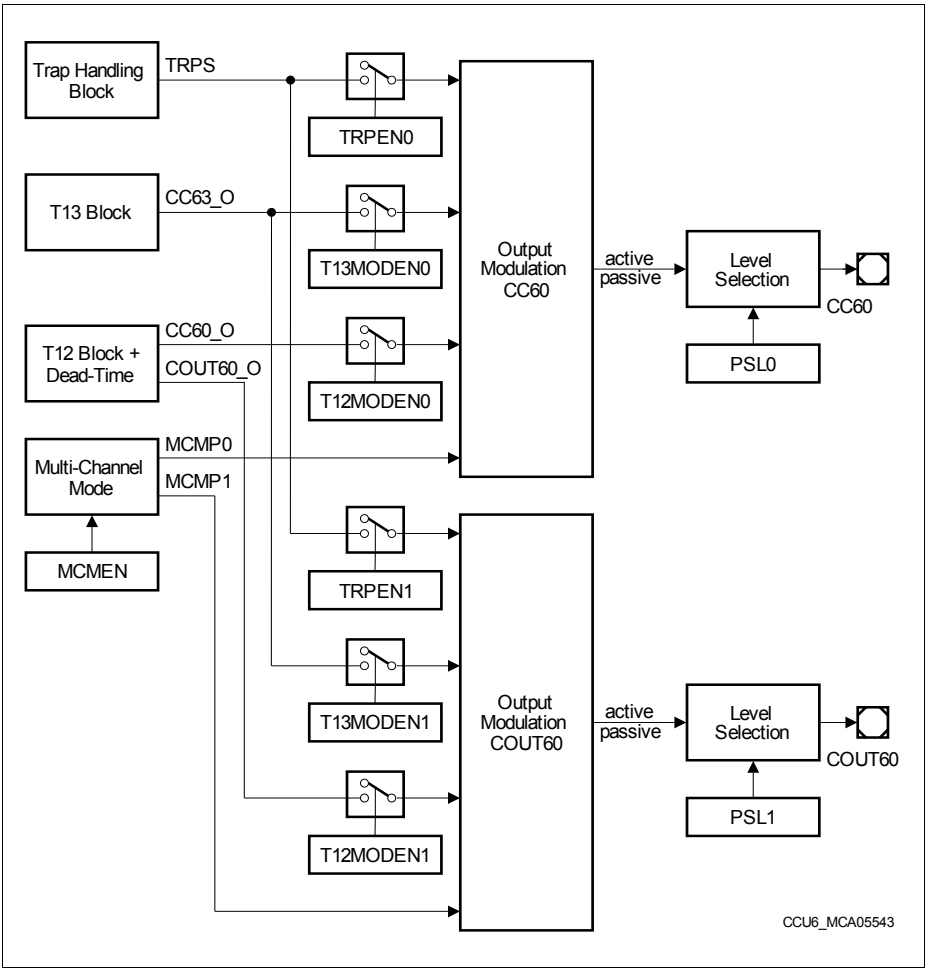


Figure 29-18 Output Modulation for Compare Channel CC60

29.2.5 T12 Capture Modes

Each of the three channels of the T12 Block can also be used to capture T12 time information in response to an external signal CC6xIN.
In capture mode, the interrupt event CC6x_R is detected when a rising edge is detected at the input CC6xIN, whereas the interrupt event CC6x_F is detected when a falling edge is detected.

There are a number of different modes for capture operation. In all modes, both of the registers of a channel are used. The selection of the capture modes is done via the **T12MSEL**.MSEL6x bit fields and can be selected individually for each of the channels.

Table 29-3 Capture Modes Overview

MSEL6x	Mode	Signal	Active Edge	CC6nSR Stored in	T12 Stored in
0100_B	1	CC6xIN	Rising	–	CC6xR
		CC6xIN	Falling	–	CC6xSR
0101_B	2	CC6xIN	Rising	CC6xR	CC6xSR
0110_B	3	CC6xIN	Falling	CC6xR	CC6xSR
0111_B	4	CC6xIN	Any	CC6xR	CC6xSR

Figure 29-19 illustrates **Capture Mode 1**. When a rising edge (0-to-1 transition) is detected at the corresponding input signal CC6xIN, the current contents of Timer T12 are captured into register CC6xR. When a falling edge (1-to-0 transition) is detected at the input signal CC6xIN, the contents of Timer T12 are captured into register CC6xSR.

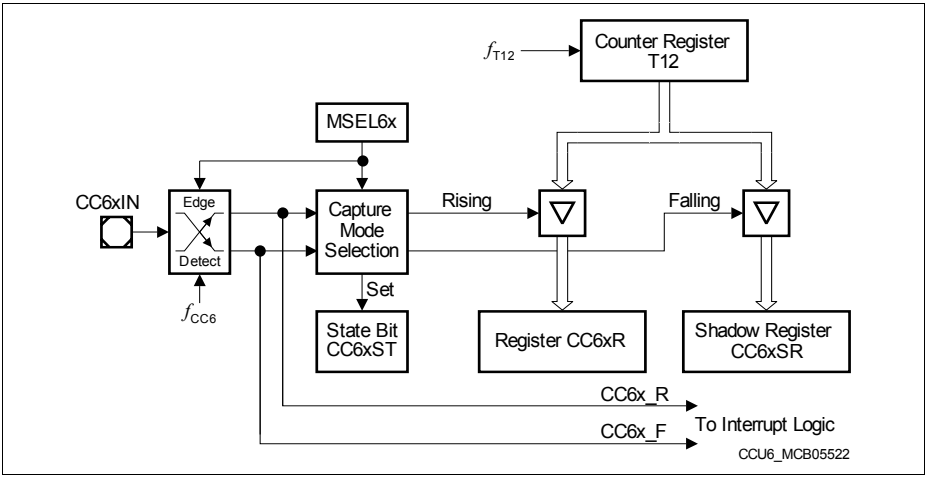


Figure 29-19 Capture Mode 1 Block Diagram

Capture Modes 2, 3 and 4 are shown in **Figure 29-20**. They differ only in the active edge causing the capture operation. In each of the three modes, when the selected edge is detected at the corresponding input signal CC6xIN, the current contents of the shadow register CC6xSR are transferred into register CC6xR, and the current Timer T12 contents are captured in register CC6xSR (simultaneous transfer). The active edge is a rising edge of CC6xIN for Capture Mode 2, a falling edge for Mode 3, and both, a rising or a falling edge for Capture Mode 4, as shown in **Table 29-3**. These capture modes are very useful in cases where there is little time between two consecutive edges of the input signal.

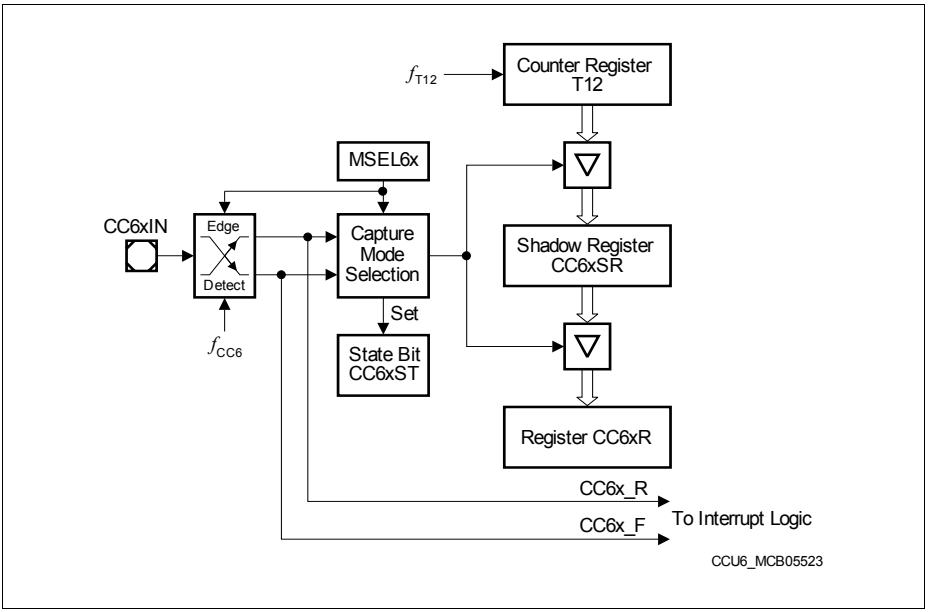


Figure 29-20 Capture Modes 2, 3 and 4 Block Diagram

Five further capture modes are called **Multi-Input Capture Modes**, as they use two different external inputs, signal CC6xIN and signal CCPOSx.

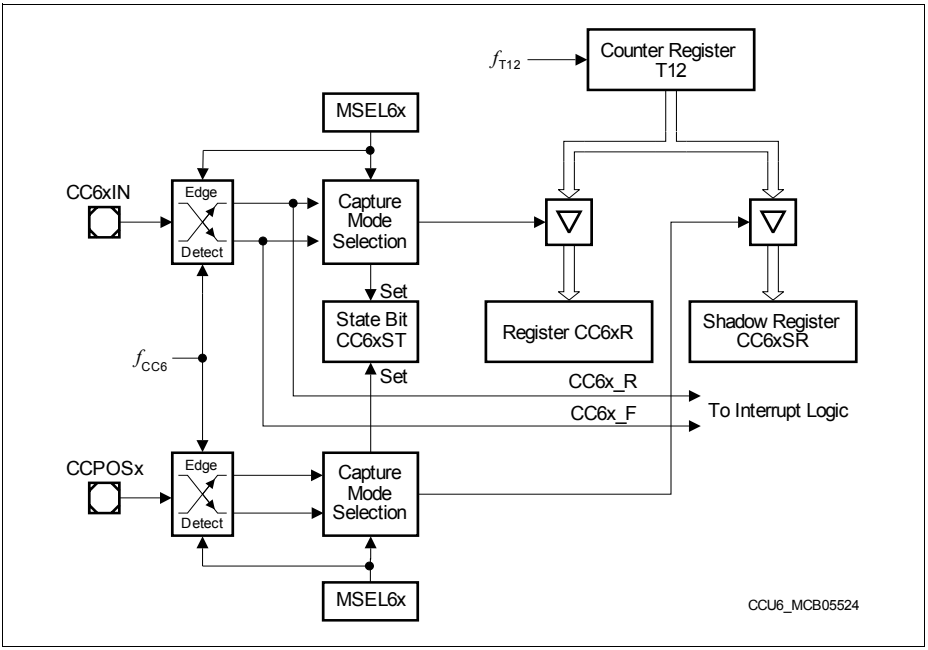


Figure 29-21 Multi-Input Capture Modes Block Diagram

In each of these modes, the current T12 contents are captured in register CC6xR in response to a selected event at signal CC6xIN, and in register CC6xSR in response to a selected event at signal CCPOSx. The possible events can be opposite input transitions, or the same transitions, or any transition at the two inputs. The different options are detailed in **Table 29-4**.

In each of the various capture modes, the Channel State Bit, CC6xST, is set to 1 when the selected capture trigger event at signal CC6xIN or CCPOSx has occurred. The State Bit is not cleared by hardware, but can be cleared by software.

In addition, appropriate signal lines to the interrupt logic are activated, that can generate an interrupt request to the CPU. Regardless of the selected active edge, all edges detected at signal CC6xIN can lead to the activation of the appropriate interrupt request line (see also **Section 29.9**).

Table 29-4 Multi-Input Capture Modes Overview

MSEL6x	Mode	Signal	Active Edge	T12 Stored in
1010_B	5	CC6xIN	Rising	CC6xR
		CCPOSx	Falling	CC6xSR
1011_B	6	CC6xIN	Falling	CC6xR
		CCPOSx	Rising	CC6xSR
1100_B	7	CC6xIN	Rising	CC6xR
		CCPOSx	Rising	CC6xSR
1101_B	8	CC6xIN	Falling	CC6xR
		CCPOSx	Falling	CC6xSR
1110_B	9	CC6xIN	Any	CC6xR
		CCPOSx	Any	CC6xSR
1111_B	–	reserved (no capture or compare action)		

29.2.6 T12 Shadow Register Transfer

A special shadow transfer signal (T12_ST) can be generated to facilitate updating the period and compare values of the compare channels CC60, CC61, and CC62 synchronously to the operation of T12. Providing a shadow register for values defining one PWM period facilitates a concurrent update by software for all relevant parameters. The next PWM period can run with a new set of parameters. The generation of this signal is requested by software via bit **TCTR0**.STE12 (set by writing 1 to the write-only bit **TCTR4**.T12STR, cleared by writing 1 to the write-only bit **TCTR4**.T12STD).

Figure 29-22 shows the shadow register structure and the shadow transfer signals, as well as on the read/write accessibility of the various registers.

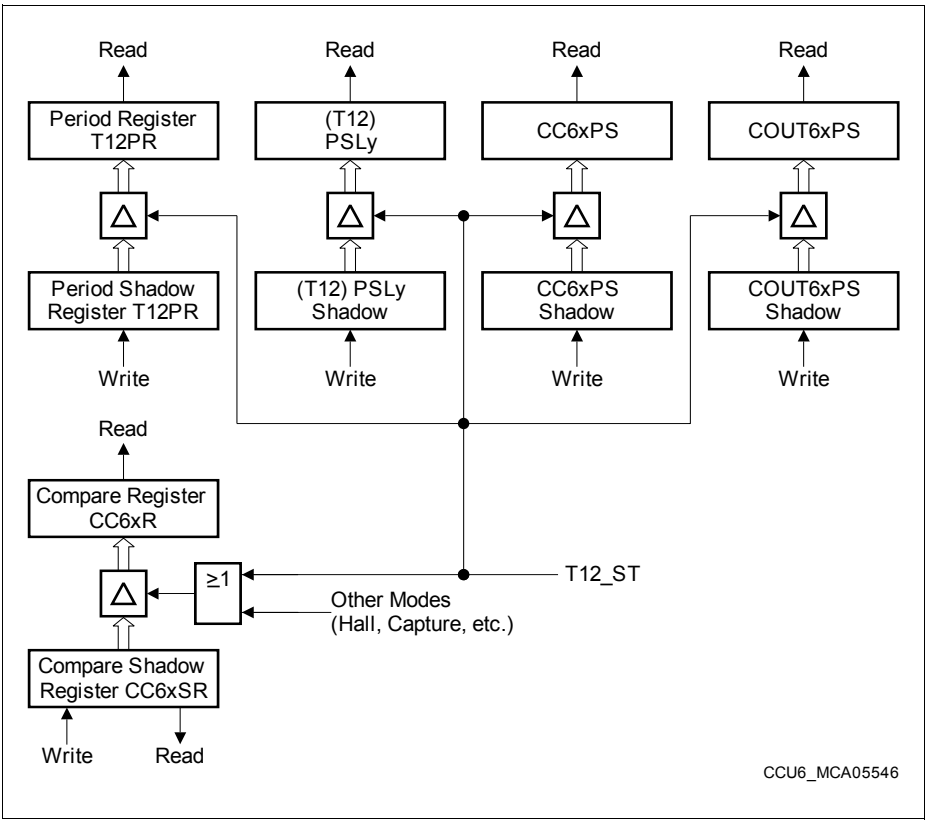


Figure 29-22 T12 Shadow Register Overview

A T12 shadow register transfer takes place (T12_ST active):

- while timer T12 is not running (T12R = 0), or
- STE12 = 1 and a Period-Match is detected while counting up, or
- STE12 = 1 and a One-Match is detected while counting down

When signal T12_ST is active, a shadow register transfer is triggered with the next cycle of the T12 clock. Bit STE12 is automatically cleared with the shadow register transfer.

29.2.7 Timer T12 Operating Mode Selection

The operating mode for the T12 channels are defined by the bit fields **T12MSEL**.MSEL6x.

Table 29-5 T12 Capture/Compare Modes Overview

MSEL6x	Selected Operating Mode
0000_B, 1111_B	Capture/Compare modes switched off
0001_B, 0010_B, 0011_B	Compare mode, see **Section 29.2.3** same behavior for all three codings
$01XX_B$	Double-Register Capture modes, see **Section 29.2.5**
1000_B	Hall Sensor Mode, see **Section 29.7** In order to properly enable this mode, all three MSEL6x fields have to be programmed to Hall Sensor mode.
1001_B	Hysteresis-like compare mode, see **Section 29.2.3.3**
1010_B 1011_B, 1100_B, 1101_B 1110_B	Multi-Input Capture modes, see **Section 29.2.5**

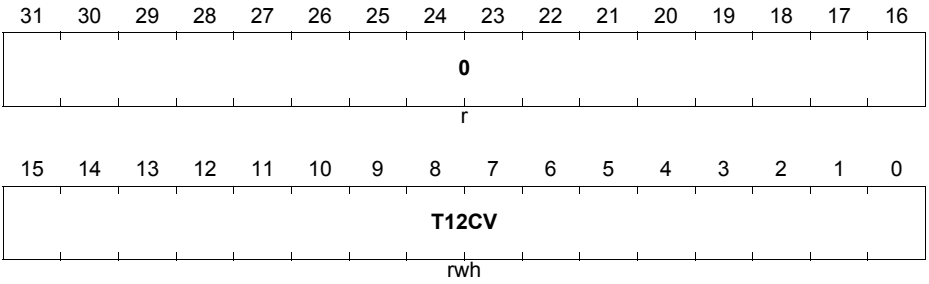
The clocking and counting scheme of the timers are controlled by the timer control registers **TCTR0** and **TCTR2**. Specific actions are triggered by write operations to register **TCTR4**.

29.2.8 T12 related Registers

29.2.8.1 T12 Counter Register

Register T12 represents the counting value of timer T12. It can only be written while the timer T12 is stopped. Write actions while T12 is running are not taken into account. Register T12 can always be read by SW.
In edge-aligned mode, T12 only counts up, whereas in center-aligned mode, T12 can count up and down.

T12
Timer T12 Counter Register **(20_H)** **Reset Value: $0000\ 0000_H$**



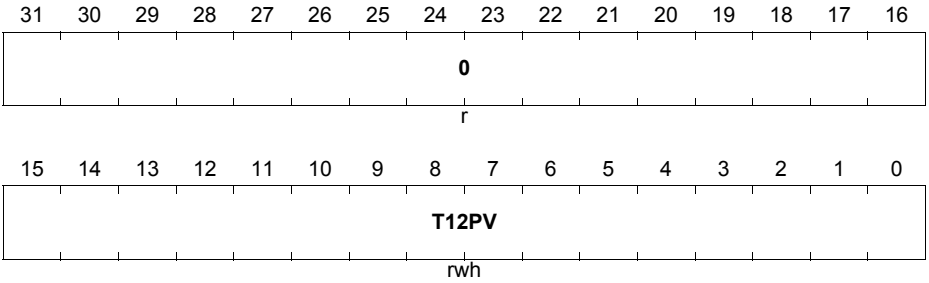
Field	Bits	Type	Description
T12CV	[15:0]	rwh	**Timer 12 Counter Value** This register represents the 16-bit counter value of Timer12.
0	[31:16]	r	**Reserved;** Returns 0 if read; should be written with 0.

Note: While timer T12 is stopped, the internal clock divider is reset in order to ensure reproducible timings and delays.

29.2.8.2 Period Register

Register T12PR contains the period value for timer T12. The period value is compared to the actual counter value of T12 and the resulting counter actions depend on the defined counting rules. This register has a shadow register and the shadow transfer is controlled by bit STE12. A read action by SW delivers the value that is currently used for the compare action, whereas the write action targets a shadow register. The shadow register structure allows a concurrent update of all T12-related values.

T12PR
Timer 12 Period Register **(24_H)** **Reset Value: 0000 0000_H**



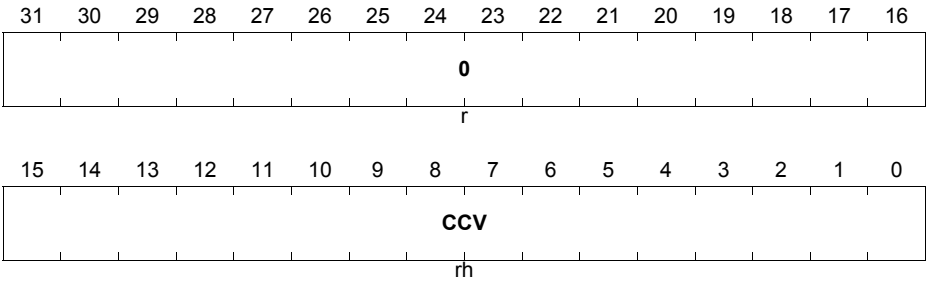
Field	Bits	Type	Description
T12PV	[15:0]	rwh	**T12 Period Value** The value T12PV defines the counter value for T12 leading to a period-match. When reaching this value, the timerT12 is set to zero (edge-aligned mode) or changes its count direction to down counting (center-aligned mode).
0	[31:16]	r	**Reserved;** Returns 0 if read; should be written with 0.

29.2.8.3 Capture/Compare Registers

In compare mode, the registers CC6xR (x = 0 - 2) are the actual compare registers for T12. The values stored in CC6xR are compared (all three channels in parallel) to the counter value of T12. In capture mode, the current value of the T12 counter register is captured by registers CC6xR if the corresponding capture event is detected.

CC6xR (x = 0-2)
Capture/Compare Register for Channel CC6x

(30_H + 4*x) **Reset Value: 0000 0000_H**

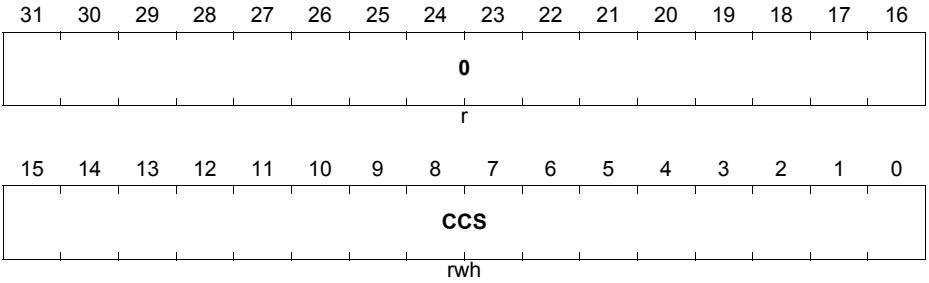


Field	Bits	Type	Description
CCV	[15:0]	rh	**Capture/Compare Value** In compare mode, the bit fields CCV contain the values, that are compared to the T12 counter value. In capture mode, the captured value of T12 can be read from these registers.
0	[31:16]	r	**Reserved;** Returns 0 if read; should be written with 0.

29.2.8.4 Capture/Compare Shadow Registers

The registers CC6xR can only be read by SW, the modification of the value is done by a shadow register transfer from register CC6xSR. The corresponding shadow registers CC6xSR can be read and written by SW. In capture mode, the value of the T12 counter register can also be captured by registers CC6xSR if the selected capture event is detected (depending on the selected capture mode).

CC6xSR (x=0-2)
Capture/Compare Shadow Reg. for Channel CC6x
(40_H+4*x) **Reset Value: 0000 0000_H**



Field	Bits	Type	Description
CCS	[15:0]	rwh	**Shadow Register for Channel x Capture/Compare Value** In compare mode, the bit fields contents of CCS are transferred to the bit fields CCV for the corresponding channel during a shadow transfer. In capture mode, the captured value of T12 can be read from these registers.
0	[31:16]	r	**Reserved;** Returns 0 if read; should be written with 0.

Note: The shadow registers can also be written by SW in capture mode. In this case, the HW capture event wins over the SW write if both happen in the same cycle (the SW write is discarded).

29.2.8.5 Dead-time Control Register

Register T12DTC controls the dead-time generation for the timer T12 compare channels. Each channel can be independently enabled/disabled for dead-time generation. If enabled, the transition from passive state to active state is delayed by the value defined by bit field DTM.
The dead time counters are clocked with the same frequency as T12.
This structure allows symmetrical dead-time generation in center-aligned and in edge-aligned PWM mode. A duty cycle of 50% leads to CC6x, COUT6x switched on for: 0.5 * period - dead time.

Note: The dead-time counters are not reset by bit T12RES, but by bit DTRES.

T12DTC
Dead-Time Control Register for Timer12

(28_H) **Reset Value: 0000 0000$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	DTR2	DTR1	DTR0	0	DTE2	DTE1	DTE0	DTM							
r	rh	rh	rh	r	rw	rw	rw	rw							

Field	Bits	Type	Description
DTM	[7:0]	rw	**Dead-Time** Bit field DTM determines the programmable delay between switching from the passive state to the active state of the selected outputs. The switching from the active state to the passive state is not delayed.
DTE2, DTE1, DTE0	10, 9, 8	rw	**Dead Time Enable Bits** Bits DTE0..DTE2 enable and disable the dead time generation for each compare channel (0, 1, 2) of timer T12. 0_B Dead-Time Counter x is disabled. The corresponding outputs switch from the passive state to the active state (according to the actual compare status) without any delay. 1_B Dead-Time Counter x is enabled. The corresponding outputs switch from the passive state to the active state (according to the compare status) with the delay programmed in bit field DTM.
DTR2, DTR1, DTR0	14, 13, 12	rh	**Dead Time Run Indication Bits** Bits DTR0..DTR2 indicate the status of the dead time generation for each compare channel (0, 1, 2) of timer T12. 0_B Dead-Time Counter x is currently in the passive state. 1_B Dead-Time Counter x is currently in the active state.
0	11, [31:15]	r	**Reserved;** Returns 0 if read; should be written with 0.

29.2.9 Capture/Compare Control Registers

29.2.9.1 Channel State Bits

The Compare State Register CMPSTAT contains status bits monitoring the current capture and compare state and control bits defining the active/passive state of the compare channels.

CMPSTAT
Compare State Register **(60_H)** **Reset Value: 0000 0000_H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
T13IM	COUT63PS	COUT62PS	CC62PS	COUT61PS	CC61PS	COUT60PS	CC60PS	0	CC63ST	CCPOS62	CCPOS61	CCPOS60	CC62ST	CC61ST	CC60ST
rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	r	rh	rh	rh	rh	rh	rh	rh

Field	Bits	Type	Description
CC60ST, CC61ST, CC62ST, CC63ST [1]	0, 1, 2, 6	rh	**Capture/Compare State Bits** Bits CC6xST monitor the state of the capture/compare channels. Bits CC6xST (x = 0, 1, 2) are related to T12, bit CC63ST is related to T13. 0_B In compare mode, the timer count is less than the compare value. In capture mode, the selected edge has not yet been detected since the bit has been cleared by SW the last time. 1_B In compare mode, the counter value is greater than or equal to the compare value. In capture mode, the selected edge has been detected.
CCPOS60, CCPOS61, CCPOS62	3, 4, 5	rh	**Sampled Hall Pattern Bits** Bits CCPOS6x (x = 0, 1, 2) are indicating the value of the input Hall pattern that has been compared to the current and expected value. The value is sampled when the event HCRDY (Hall Compare Ready) occurs. 0_B The input CCPOSx has been sampled as 0. 1_B The input CCPOSx has been sampled as 1.
CC60PS, CC61PS, CC62PS, COUT60PS, COUT61PS, COUT62PS, COUT63PS [2]	8, 10, 12, 9, 11, 13, 14	rwh	**Passive State Select for Compare Outputs** Bits CC6xPS, COUT6xPS select the state of the corresponding compare channel, that is considered to be the passive state. During the passive state, the passive level (defined in register PSLR) is driven by the output pin. Bits CC6xPS, COUT6xPS (x = 0, 1, 2) are related to T12, bit CC63PS is related to T13. 0_B The corresponding compare signal is in passive state while CC6xST is 0. 1_B The corresponding compare signal is in passive state while CC6xST is 1. In capture mode, these bits are not used.

Field	Bits	Type	Description
T13IM[3]	15	rwh	**T13 Inverted Modulation** Bit T13IM inverts the T13 signal for the modulation of the CC6x and COUT6x (x = 0, 1, 2) signals. 0_B T13 output CC63_O is equal to CC63ST. 1_B T13 output CC63_O is equal to $\overline{\text{CC63ST}}$.
0	7, [31:16]	r	**Reserved;** Returns 0 if read; should be written with 0.

1) These bits are set and cleared according to the T12, T13 switching rules

2) These bits have shadow bits and are updated in parallel to the capture/compare registers of T12, T13 respectively. A read action targets the actually used values, whereas a write action targets the shadow bits.

3) This bit has a shadow bit and is updated in parallel to the compare and period registers of T13. A read action targets the actually used values, whereas a write action targets the shadow bit.

The Compare Status Modification Register CMPMODIF provides software-control (independent set and clear conditions) for the channel state bits CC6xST. This feature enables the user to individually change the status of the output lines by software, for example when the corresponding compare timer is stopped.

CMPMODIF
Compare State Modification Register

(64_H) **Reset Value: $0000\ 0000_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

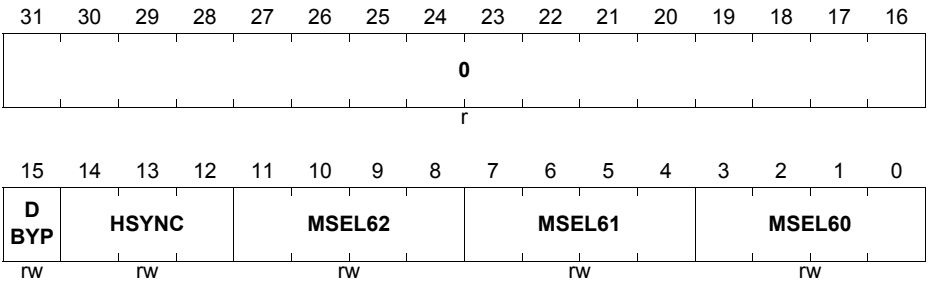
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	MCC 63R	0			MCC 62R	MCC 61R	MCC 60R	0	MCC 63S	0			MCC 62S	MCC 61S	MCC 60S
r	w	r			w	w	w	r	w	r			w	w	w

Field	Bits	Type	Description
MCC60S, **MCC61S,** **MCC62S,** **MCC63S,** **MCC60R,** **MCC61R,** **MCC62R,** **MCC63R**	0, 1, 2, 7, 8, 9, 10, 14	w	**Capture/Compare Status Modification Bits** These bits are used to bits to set (MCC6xS) or to clear (MCC6xR) the corresponding bits CC6xST by SW. This feature allows the user to individually change the status of the output lines by SW, e.g. when the corresponding compare timer is stopped. This allows a bit manipulation of CC6xST-bits by a single data write action. The following functionality of a write access to bits concerning the same capture/compare state bit is provided: [MCC6xR, MCC6xS] = 00_B Bit CC6xST is not changed. 01_B Bit CC6xST is set. 10_B Bit CC6xST is cleared. 11_B reserved
0	[5:3], 7, [13:11], [31:15]	r	**Reserved;** Returns 0 if read; should be written with 0.

29.2.9.2 T12 Mode Control Register

Register T12MSEL contains control bits to select the capture/compare functionality of the three channels of Timer T12.

T12MSEL
T12 Mode Select Register **(68_H)** **Reset Value: 0000 0000$_H$**



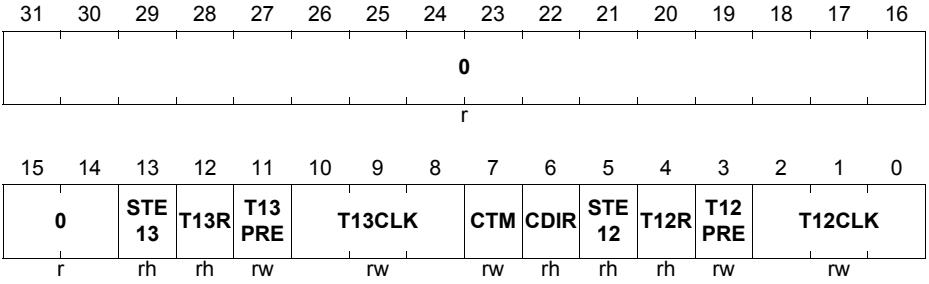
Field	Bits	Type	Description
MSEL60, MSEL61, MSEL62	[3:0], [7:4], [11:8]	rw	**Capture/Compare Mode Selection** These bit fields select the operating mode of the three T12 capture/compare channels. Each channel (x = 0, 1, 2) can be programmed individually for one of these modes (except for Hall Sensor Mode). Coding see **Table 29-5**.
HSYNC	[14:12]	rw	**Hall Synchronization** Bit field HSYNC defines the source for the sampling of the Hall input pattern and the comparison to the current and the expected Hall pattern bit fields. Coding see **Table 29-11**.
DBYP	15	rw	**Delay Bypass** DBYP controls whether the source signal for the sampling of the Hall input pattern (selected by HSYNC) is delayed by the Dead-Time Counter 0. 0_B The bypass is not active. Dead-Time Counter 0 is generating a delay after the source signal becomes active. 1_B The bypass is active. Dead-Time Counter 0 is not used for a delay.
0	[31:16]	r	**Reserved;** Returns 0 if read; should be written with 0.

29.2.9.3 Timer Control Registers

Register TCTR0 controls the basic functionality of both timers, T12 and T13.

Note: A write action to the bit fields T12CLK or T12PRE is only taken into account while the timer T12 is not running (T12R=0). A write action to the bit fields T13CLK or T13PRE is only taken into account while the timer T13 is not running (T13R=0).

TCTR0
Timer Control Register 0 **(70_H)** **Reset Value: $0000\ 0000_H$**



Field	Bits	Type	Description
T12CLK	[2:0]	rw	**Timer T12 Input Clock Select** Selects the input clock for timer T12 that is derived from the peripheral clock according to the equation $f_{T12} = f_{CC6} / 2^{<T12CLK>}$. 000_B $f_{T12} = f_{CC6}$ 001_B $f_{T12} = f_{CC6} / 2$ 010_B $f_{T12} = f_{CC6} / 4$ 011_B $f_{T12} = f_{CC6} / 8$ 100_B $f_{T12} = f_{CC6} / 16$ 101_B $f_{T12} = f_{CC6} / 32$ 110_B $f_{T12} = f_{CC6} / 64$ 111_B $f_{T12} = f_{CC6} / 128$
T12PRE	3	rw	**Timer T12 Prescaler Bit** In order to support higher clock frequencies, an additional prescaler factor of 1/256 can be enabled for the prescaler for T12. 0_B The additional prescaler for T12 is disabled. 1_B The additional prescaler for T12 is enabled.

Field	Bits	Type	Description
T12R	4	rh	**Timer T12 Run Bit**[1)] T12R starts and stops timer T12. It is set/cleared by SW by setting bits T12RR or T12RS or it is cleared by HW according to the function defined by bit field T12SSC. 0_B Timer T12 is stopped. 1_B Timer T12 is running.
STE12	5	rh	**Timer T12 Shadow Transfer Enable** Bit STE12 enables or disables the shadow transfer of the T12 period value, the compare values and passive state select bits and levels from their shadow registers to the actual registers if a T12 shadow transfer event is detected. Bit STE12 is cleared by hardware after the shadow transfer. A T12 shadow transfer event is a period-match while counting up or a one-match while counting down. 0_B The shadow register transfer is disabled. 1_B The shadow register transfer is enabled.
CDIR	6	rh	**Count Direction of Timer T12** This bit is set/cleared according to the counting rules of T12. 0_B T12 counts up. 1_B T12 counts down.
CTM	7	rw	**T12 Operating Mode** 0_B Edge-aligned Mode: T12 always counts up and continues counting from zero after reaching the period value. 1_B Center-aligned Mode: T12 counts down after detecting a period-match and counts up after detecting a one-match.

Field	Bits	Type	Description
T13CLK	[10:8]	rw	**Timer T13 Input Clock Select** Selects the input clock for timer T13 that is derived from the peripheral clock according to the equation $f_{T13} = f_{CC6} / 2^{<T13CLK>}$. 000_B $f_{T13} = f_{CC6}$ 001_B $f_{T13} = f_{CC6} / 2$ 010_B $f_{T13} = f_{CC6} / 4$ 011_B $f_{T13} = f_{CC6} / 8$ 100_B $f_{T13} = f_{CC6} / 16$ 101_B $f_{T13} = f_{CC6} / 32$ 110_B $f_{T13} = f_{CC6} / 64$ 111_B $f_{T13} = f_{CC6} / 128$
T13PRE	11	rw	**Timer T13 Prescaler Bit** In order to support higher clock frequencies, an additional prescaler factor of 1/256 can be enabled for the prescaler for T13. 0_B The additional prescaler for T13 is disabled. 1_B The additional prescaler for T13 is enabled.
T13R	12	rh	**Timer T13 Run Bit**[2)] T13R starts and stops timer T13. It is set/cleared by SW by setting bits T13RR orT13RS or it is set/cleared by HW according to the function defined by bit fields T13SSC, T13TEC and T13TED. 0_B Timer T13 is stopped. 1_B Timer T13 is running.
STE13	13	rh	**Timer T13 Shadow Transfer Enable** Bit STE13 enables or disables the shadow transfer of the T13 period value, the compare value and passive state select bit and level from their shadow registers to the actual registers if a T13 shadow transfer event is detected. Bit STE13 is cleared by hardware after the shadow transfer. A T13 shadow transfer event is a period-match. 0_B The shadow register transfer is disabled. 1_B The shadow register transfer is enabled.
0	[31:14]	r	**Reserved;** Returns 0 if read; should be written with 0.

1) A concurrent set/clear action on T12R (from T12SSC, T12RR or T12RS) will have no effect. The bit T12R will remain unchanged.

2) A concurrent set/cleared action on T13R (from T13SSC, T13TEC, T13RR or T13RS) will have no effect. The bit T12R will remain unchanged.

Register TCTR2 controls the single-shot and the synchronization functionality of both timers T12 and T13. Both timers can run in single-shot mode. In this mode they stop their counting sequence automatically after one counting period with a count value of zero. The single-shot mode and the synchronization feature of T13 to T12 allow the generation of events with a programmable delay after well-defined PWM actions of T12.

TCTR2
Timer Control Register 2 **(74_H)** **Reset Value: 0000 0000_H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0				T13 RSEL		T12 RSEL		0	T13 TED		T13 TEC			T13 SSC	T12 SSC
r				rw		rw		r	rw		rw			rw	rw

Field	Bits	Type	Description
T12SSC	0	rw	**Timer T12 Single Shot Control** This bit controls the single shot-mode of T12. 0_B The single-shot mode is disabled, no HW action on T12R. 1_B The single shot mode is enabled, the bit T12R is cleared by HW if - T12 reaches its period value in edge-aligned mode - T12 reaches the value 1 while down counting in center-aligned mode. In parallel to the clear action of bit T12R, the bits CC6xST (x=0, 1, 2) are cleared.
T13SSC	1	rw	**Timer T13 Single Shot Control** This bit controls the single shot-mode of T13. 0_B No HW action on T13R 1_B The single-shot mode is enabled, the bit T13R is cleared by HW if T13 reaches its period value. In parallel to the clear action of bit T13R, the bit CC63ST is cleared.

Field	Bits	Type	Description
T13TEC	[4:2]	rw	**T13 Trigger Event Control** Bit field T13TEC selects the trigger event to start T13 (automatic set of T13R for synchronization to T12 compare signals) according to following combinations: 000_B no action 001_B set T13R on a T12 compare event on channel 0 010_B set T13R on a T12 compare event on channel 1 011_B set T13R on a T12 compare event on channel 2 100_B set T13R on any T12 compare event (ch. 0, 1, 2) 101_B set T13R upon a period-match of T12 110_B set T13R upon a zero-match of T12 (while counting up) 111_B set T13R on any edge of inputs CCPOSx
T13TED	[6:5]	rw	**Timer T13 Trigger Event Direction**[1)] Bit field T13TED delivers additional information to control the automatic set of bit T13R in the case that the trigger action defined by T13TEC is detected. 00_B reserved, no action 01_B while T12 is counting up 10_B while T12 is counting down 11_B independent on the count direction of T12
T12RSEL	[9:8]	rw	**Timer T12 External Run Selection** Bit field T12RSEL defines the event of signal T12HR that can set the run bit T12R by HW. 00_B The external setting of T12R is disabled. 01_B Bit T12R is set if a rising edge of signal T12HR is detected. 10_B Bit T12R is set if a falling edge of signal T12HR is detected. 11_B Bit T12R is set if an edge of signal T12HR is detected.

Field	Bits	Type	Description
T13RSEL	[11:10]	rw	**Timer T13 External Run Selection** Bit field T13RSEL defines the event of signal T13HR that can set the run bit T13R by HW. 00_B The external setting of T13R is disabled. 01_B Bit T13R is set if a rising edge of signal T13HR is detected. 10_B Bit T13R is set if a falling edge of signal T13HR is detected. 11_B Bit T13R is set if an edge of signal T13HR is detected.
0	7, [31:12]	r	**Reserved;** Returns 0 if read; should be written with 0;

1) Example:
If the timer T13 is intended to start at any compare event on T12 (T13TEC=100) the trigger event direction can be programmed to
- counting up >> a T12 channel 0, 1, 2 compare match triggers T13R only while T12 is counting up
- counting down >> a T12 channel 0, 1, 2 compare match triggers T13R only while T12 is counting down
- independent from bit CDIR >> each T12 channel 0, 1, 2 compare match triggers T13R

The timer count direction is taken from the value of bit CDIR. As a result, if T12 is running in edge-aligned mode (counting up only), T13 can only be started automatically if bit field T13TED=01 or 11.

Register TCTR4 provides software-control (independent set and clear conditions) for the run bits T12R and T13R. Furthermore, the timers can be reset (while running) and bits STE12 and STE13 can be controlled by software. Reading these bits always returns 0.

TCTR4
Timer Control Register 4 **(78_H)** **Reset Value: $0000\ 0000_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
T13 STD	T13 STR	T13 CNT	0		T13 RES	T13 RS	T13 RR	T12 STD	T12 STR	T12 CNT	0	DT RES	T12 RES	T12 RS	T12 RR
w	w	w	r		w	w	w	w	w	w	r	w	w	w	w

Field	Bits	Type	Description
T12RR	0	w	**Timer T12 Run Reset** Setting this bit clears the T12R bit. 0_B T12R is not influenced. 1_B T12R is cleared, T12 stops counting.
T12RS	1	w	**Timer T12 Run Set** Setting this bit sets the T12R bit. 0_B T12R is not influenced. 1_B T12R is set, T12 starts counting.
T12RES	2	w	**Timer T12 Reset** 0_B No effect on T12. 1_B The T12 counter register is cleared to zero. The switching of the output signals is according to the switching rules. Setting of T12RES has no impact on bit T12R.
DTRES	3	w	**Dead-Time Counter Reset** 0_B No effect on the dead-time counters. 1_B The three dead-time counter channels are cleared to zero.
T12CNT	5	w	**Timer T12 Count Event** 0_B No action 1_B If enabled (PISEL2), timer T12 counts one step.

Field	Bits	Type	Description
T12STR	6	w	**Timer T12 Shadow Transfer Request** 0_B No action 1_B STE12 is set, enabling the shadow transfer.
T12STD	7	w	**Timer T12 Shadow Transfer Disable** 0_B No action 1_B STE12 is cleared without triggering the shadow transfer.
T13RR	8	w	**Timer T13 Run Reset** Setting this bit clears the T13R bit. 0_B T13R is not influenced. 1_B T13R is cleared, T13 stops counting.
T13RS	9	w	**Timer T13 Run Set** Setting this bit sets the T13R bit. 0_B T13R is not influenced. 1_B T13R is set, T13 starts counting.
T13RES	10	w	**Timer T13 Reset** 0_B No effect on T13. 1_B The T13 counter register is cleared to zero. The switching of the output signals is according to the switching rules. Setting of T13RES has no impact on bit T13R.
T13CNT	13	w	**Timer T13 Count Event** 0_B No action 1_B If enabled (PISEL2), timer T13 counts one step.
T13STR	14	w	**Timer T13 Shadow Transfer Request** 0_B No action 1_B STE13 is set, enabling the shadow transfer.
T13STD	15	w	**Timer T13 Shadow Transfer Disable** 0_B No action 1_B STE13 is cleared without triggering the shadow transfer.
0	4, [12:11], [31:16]	r	**reserved;** returns 0 if read; should be written with 0;

Note: A simultaneous write of a 1 to bits that set and clear the same bit will trigger no action. The corresponding bit will remain unchanged.

29.3 Operating Timer T13

Timer T13 is implemented similarly to Timer T12, but only with one channel in compare mode. A 16-bit up-counter is connected to a channel register via a comparator, that generates a signal when the counter contents match the contents of the channel register. A variety of control functions facilitate the adaptation of the T13 structure to different application needs. In addition, T13 can be started synchronously to timer T12 events.

This section provides information about:

- T13 overview (see **Section 29.3.1**)
- Counting scheme (see **Section 29.3.2**)
- Compare mode (see **Section 29.3.3**)
- Compare output path (see **Section 29.3.4**)
- Shadow register transfer (see **Section 29.3.5**)
- T13 counter register description (see **Section 29.3.6**)

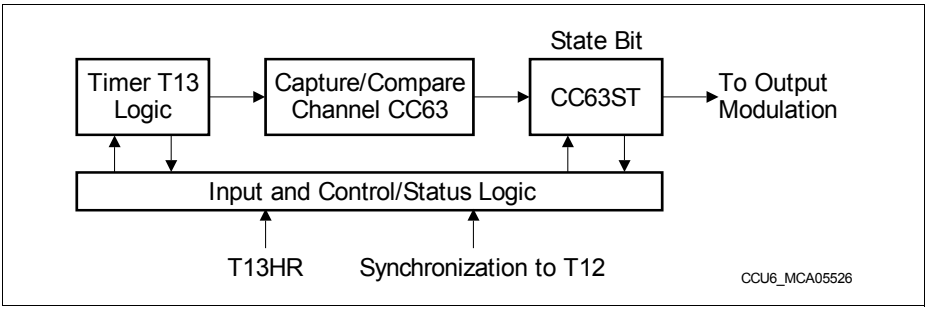


Figure 29-23 Overview Diagram of the Timer T13 Block

29.3.1 T13 Overview

Figure 29-24 shows a detailed block diagram of Timer T13. The functions of the timer T12 block are controlled by bits in registers **TCTR0**, **TCTR2**, and **PISEL2**.
Timer T13 receives its input clock, f_{T13}, from the module clock f_{CC6} via a programmable prescaler and an optional 1/256 divider or from an input signal T13HR. T13 can only count up (similar to the Edge-Aligned mode of T12).

Via a comparator, the timer T13 Counter Register **T13** is connected to the Period Register **T13PR**. This register determines the maximum count value for T13. When T13 reaches the period value, signal T13_PM (T13 Period Match) is generated and T13 is cleared to 0000_H with the next T13 clock edge. The Period Register receives a new period value from its Shadow Period Register, T13PS, that is loaded via software. The transfer of a new period value from the shadow register into T13PR is controlled via the 'T13 Shadow Transfer' control signal, T13_ST. The generation of this signal depends on the associated control bit STE13. Providing a shadow register for the period value as

well as for other values related to the generation of the PWM signal facilitates a concurrent update by software for all relevant parameters (refer to **Table 29.3.5**).
Another signal indicates whether the counter contents are equal to 0000_H (T13_ZM).

A Single-Shot control bit, T13SSC, enables an automatic stop of the timer when the current counting period is finished (see **Figure 29-26**).

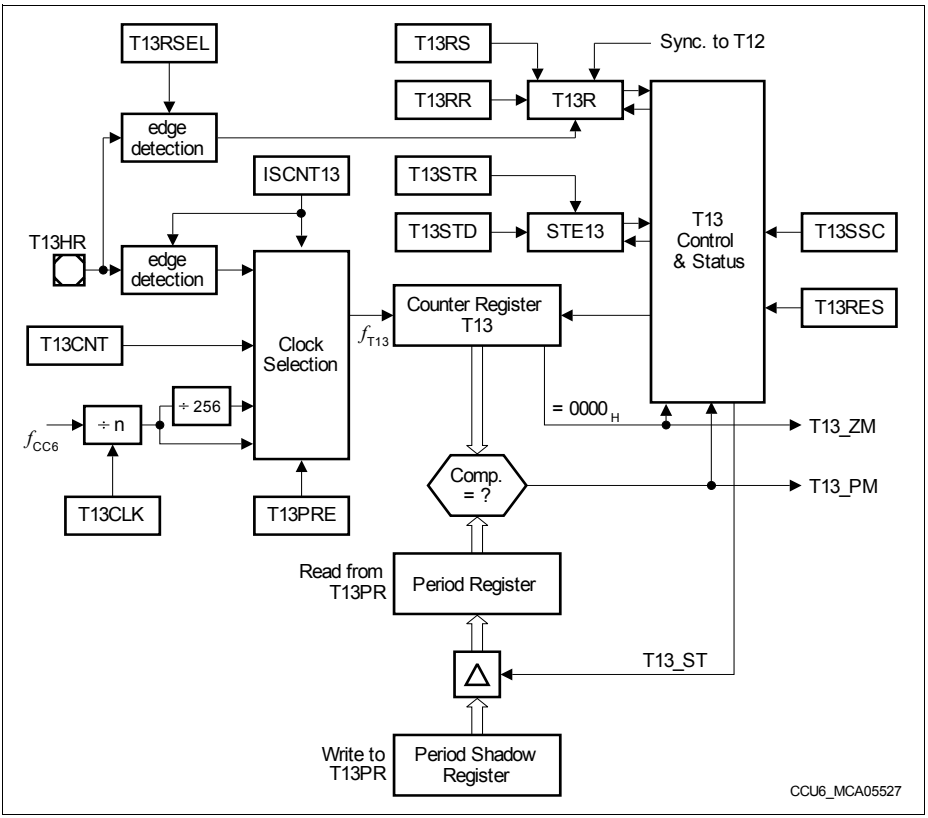


Figure 29-24 T13 Counter Logic and Period Comparators

The start or stop of T13 is controlled by the Run bit, T13R. This control bit can be set by software via the associated set/clear bits T13RS or T13RR in register **TCTR4**, or it is cleared by hardware according to preselected conditions (single-shot mode).
The timer T13 run bit T13R must not be set while the applied T13 period value is zero.
Bit T13R can be set automatically if an event of T12 is detected to synchronize T13 timings to T12 events, e.g. to generate a programmable delay via T13 after an edge of a T12 compare channel before triggering an AD conversion (T13 can trigger ADC

conversions).
Timer T13 can be cleared to 0000_H via control bit T13RES. Setting this write-only bit only clears the timer contents, but has no further effects, e.g., it does not stop the timer.

The generation of the T13 shadow transfer control signal, T13_ST, is enabled via bit STE13. This bit can be set or cleared by software indirectly through its associated set/reset control bits T13STR and T13STD.

Two bit fields, T13TEC and T13TED, control the synchronization of T13 to Timer T12 events. T13TEC selects the trigger event, while T13TED determines for which T12 count direction the trigger should be active.
While Timer T13 is running, write accesses to the count register T13 are not taken into account. If T13 is stopped, write actions to register T13 are immediately taken into account.

Note: The T13 Period Register and its associated shadow register are located at the same physical address. A write access to this address targets the Shadow Register, while a read access reads from the actual period register.

29.3.2 T13 Counting Scheme

This section describes the clocking and the counting capabilities of T13.

29.3.2.1 Clock Selection

In **Timer Mode** (**PISEL2**. ISCNT13 = 00_B), the input clock f_{T13} of Timer T13 is derived from the internal module clock f_{CC6} through a programmable prescaler and an optional 1/256 divider. The resulting prescaler factors are listed in **Table 29-6**. The prescaler of T13 is cleared while T13 is not running (**TCTR0**.T13R = 0) to ensure reproducible timings and delays.

Table 29-6 Timer T13 Input Clock Options

T13CLK	Resulting Input Clock f_{T13} Prescaler Off (T13PRE = 0)	Resulting Input Clock f_{T13} Prescaler On (T13PRE = 1)
000_B	f_{CC6}	f_{CC6} / 256
001_B	f_{CC6} / 2	f_{CC6} / 512
010_B	f_{CC6} / 4	f_{CC6} / 1024
011_B	f_{CC6} / 8	f_{CC6} / 2048
100_B	f_{CC6} / 16	f_{CC6} / 4096
101_B	f_{CC6} / 32	f_{CC6} / 8192
110_B	f_{CC6} / 64	f_{CC6} / 16384
111_B	f_{CC6} / 128	f_{CC6} / 32768

In **Counter Mode**, timer T13 counts one step:

- If a 1 is written to **TCTR4**.T13CNT and **PISEL2**.ISCNT13 = 01_B
- If a rising edge of input signal T13HR is detected and **PISEL2**.ISCNT13 = 10_B
- If a falling edge of input signal T13HR is detected and **PISEL2**.ISCNT13 = 11_B

29.3.2.2 T13 Counting

The period of the timer is determined by the value in the period Register T13PR according to the following formula:

$T13_{PER}$ = <Period-Value> + 1; in T13 clocks (f_{T13}) (29.3)

Timer T13 can only count up, comparable to the Edge-Aligned mode of T12. This leads to very simple ‘counting rule’ for the T13 counter:

- The counter is cleared with the next T13 clock edge if a Period-Match is detected. The counting direction is always upwards.

The behavior of T13 is illustrated in **Figure 29-25**.

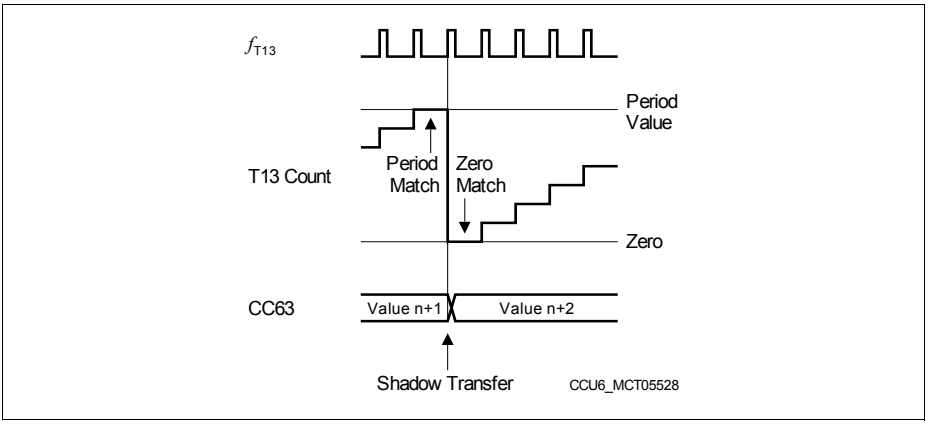


Figure 29-25 T13 Counting Sequence

29.3.2.3 Single-Shot Mode

In Single-Shot Mode, the timer run bit T13R is cleared by hardware. If bit T13SSC = 1, the timer T13 will stop when the current timer period is finished.

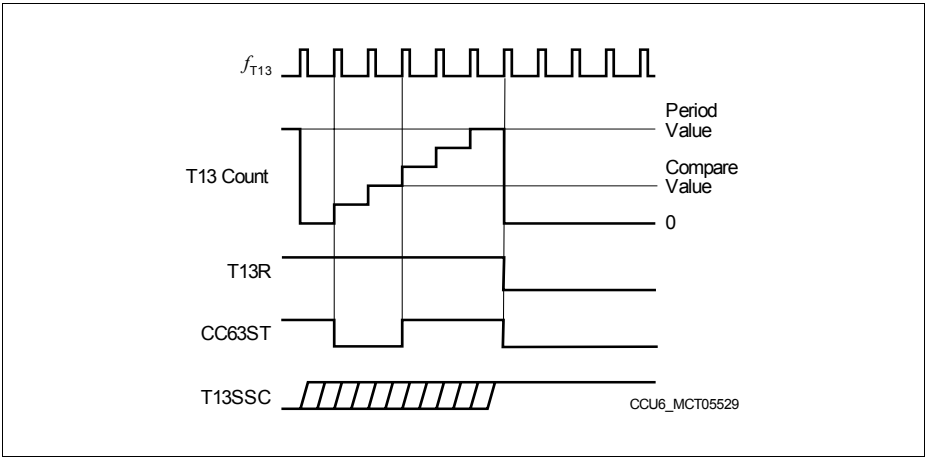


Figure 29-26 Single-Shot Operation of Timer T13

29.3.2.4 Synchronization to T12

Timer T13 can be synchronized to a T12 event. Bit fields T13TEC and T13TED select the event that is used to start Timer T13. The selected event sets bit T13R via HW, and T13 starts counting. Combined with the Single-Shot mode, this feature can be used to generate a programmable delay after a T12 event.

Figure 29-27 shows an example for the synchronization of T13 to a T12 event. Here, the selected event is a compare-match (compare value = 2) while counting up. The clocks of T12 and T13 can be different (other prescaler factor); the figure shows an example in which T13 is clocked with half the frequency of T12.

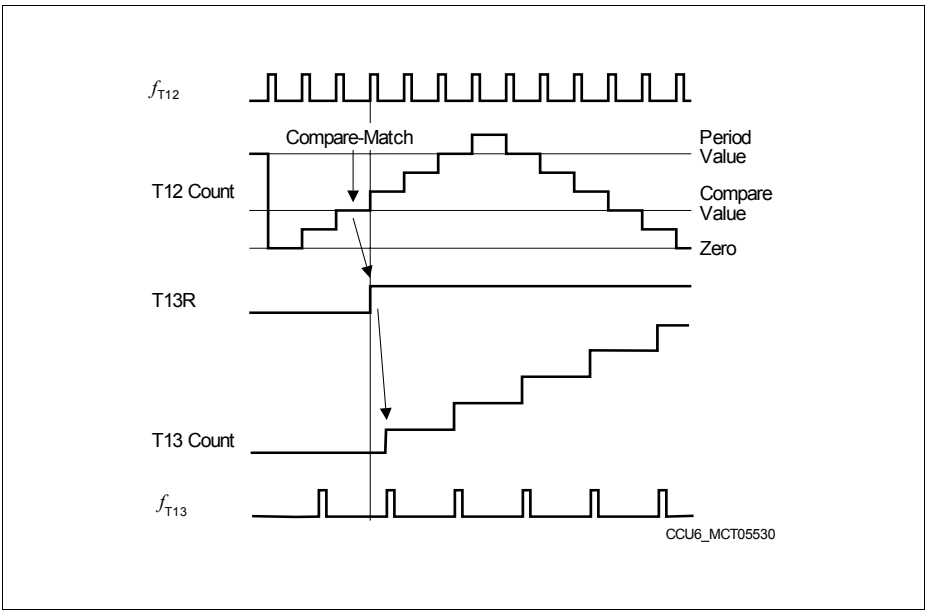


Figure 29-27 Synchronization of T13 to T12 Compare Match

Bit field T13TEC selects the trigger event to start T13 (automatic set of T13R for synchronization to T12 compare signals) according to the combinations shown in **Table 29-7**. Bit field T13TED additionally specifies for which count direction of T12 the selected trigger event should be regarded (see **Table 29-8**).

Table 29-7 T12 Trigger Event Selection

T13TEC	Selected Event
000_B	None
001_B	T12 Compare Event on Channel 0 (CM_CC60)
010_B	T12 Compare Event on Channel 1 (CM_CC61)
011_B	T12 Compare Event on Channel 2 (CM_CC62)
100_B	T12 Compare Event on any Channel (0, 1, 2)
101_B	T12 Period-Match (T12_PM)
110_B	T12 Zero-Match while counting up (T12_ZM and CDIR = 0)
111_B	Any Hall State Change

Table 29-8 T12 Trigger Event Additional Specifier

T13TED	Selected Event Specifier
00_B	Reserved, no action
01_B	Selected event is active while T12 is counting up (CDIR = 0)
10_B	Selected event is active while T12 is counting down (CDIR = 1)
11_B	Selected event is active independently of the count direction of T12

29.3.3 T13 Compare Mode

Associated with Timer T13 is one compare channel, that can perform compare operations with regard to the contents of the T13 counter.

Figure 29-23 gives an overview on the T13 channel in Compare Mode. The channel is connected to the T13 counter register via an equal-to comparator, generating a compare match signal when the contents of the counter matches the contents of the compare register.

The channel consists of the comparator and a double register structure - the actual compare register, **CC63R**, feeding the comparator, and an associated shadow register, **CC63SR**, that is preloaded by software and transferred into the compare register when signal T13 shadow transfer, T13_ST, gets active. Providing a shadow register for the compare value as well as for other values related to the generation of the PWM signal facilitates a concurrent update by software for all relevant parameters.

Associated with the channel is a State Bit, **CMPSTAT**.CC63ST, holding the status of the compare operation. **Figure 29-28** gives an overview on the logic for the State Bit.

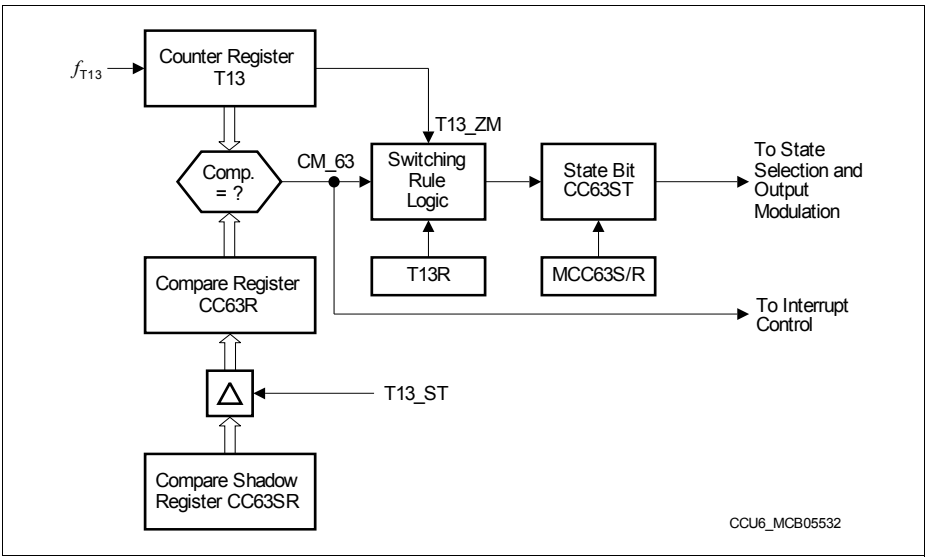


Figure 29-28 T13 State Bit Block Diagram

A compare interrupt event CM_63 is signaled when a compare match is detected. The actual setting of a State Bit has no influence on the interrupt generation.

The inputs to the switching rule logic for the CC63ST bit are the timer run bit (T13R), the timer zero-match signal (T13_ZM), and the actual individual compare-match signal CM_63. In addition, the state bit can be set or cleared by software via bits MCC63S and

MCC63R in register **CMPMODIF**.
A modification of the State Bit CC63ST by hardware is only possible while Timer T13 is running (T13R = 1). If this is the case, the following switching rules apply for setting and resetting the State Bit in Compare Mode:

State Bit **CC63ST is set** to 1

- with the next T13 clock (f_{T13}) after a compare-match (T13 is always counting up) (i.e., when the counter is incremented above the compare value);
- with the next T13 clock (f_{T13}) after a zero-match AND a parallel compare-match.

State Bit **CC63ST is cleared** to 0

- with the next T13 clock (f_{T13}) after a zero-match AND NO parallel compare-match.

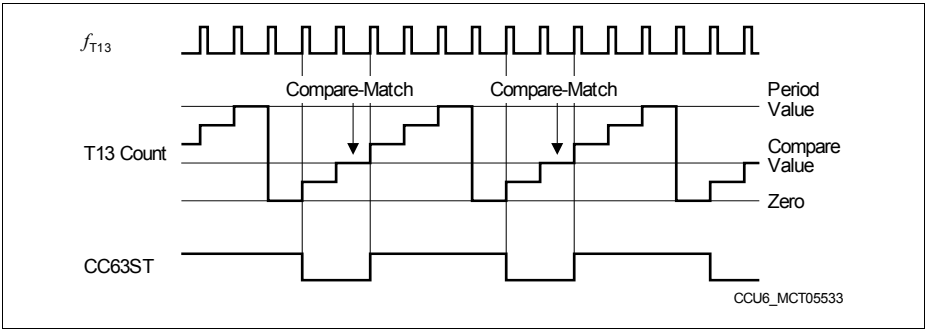


Figure 29-29 T13 Compare Operation

29.3.4 Compare Mode Output Path

Figure 29-30 gives an overview on the signal path from the channel State Bit CC63ST to its output pin COUT63. As illustrated, a user can determine the desired output behavior in relation to the current state of CC63ST. Please refer to Section 29.2.4.3 for detailed information on the output modulation for T12 signals.

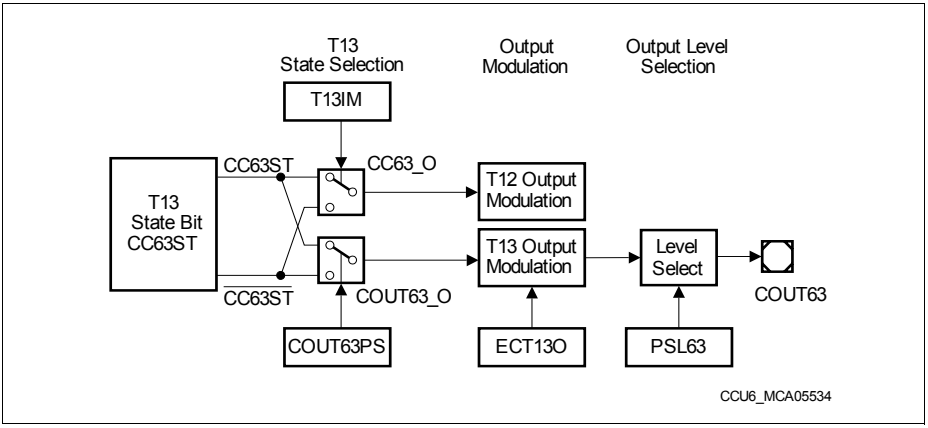


Figure 29-30 Channel 63 Output Path

The output line COUT63_O can generate a T13 PWM at the output pin COUT63. The signal CC63_O can be used to modulate the T12-related output signals with a T13 PWM. In order to decouple COUT63 from the internal modulation, the compare state leading to an active signal can be selected independently by bits T13IM and COUT63PS.

The last block of the data path is the Output Modulation block. Here, the modulation source T13 and the trap functionality are combined and control the actual level of the output pin COUT63 (see Figure 29-31):

- The **T13 related compare signal** COUT63_O delivered by the T13 state selection with the enable bit **MODCTR**.ECT13O
- The **trap state** TRPS with an individual enable bit **TRPCTR**.TRPEN13

If the modulation input signal COUT63_O is enabled (ECT13O = 1) and is at passive state, the modulated is also in passive state. If the modulation input is not enabled, the output is in passive state.
If the Trap State is active (TRPS = 1), then the output enabled for the trap signal (by TRPEN13 = 1) is set to the passive state.

The output of the modulation control block is connected to a level select block. It offers the option to determine the actual output level of a pin, depending on the state of the output line (decoupling of active/passive state and output polarity) as specified by the Passive State Select bit **PSLR**.PSL63. If the modulated output signal is in the passive

state, the level specified directly by PSL63 is output. If it is in the active state, the inverted level of PSL63 is output. This allows the user to adapt the polarity of an active output signal to the connected circuitry.

The PSL63 bit has a shadow register to allow for updates with the T13 shadow transfer signal (T13_ST) without undesired pulses on the output lines. A read action returns the actually used value, whereas a write action targets the shadow bit. Providing a shadow register for the PSL value as well as for other values related to the generation of the PWM signal facilitates a concurrent update by software for all relevant parameters.

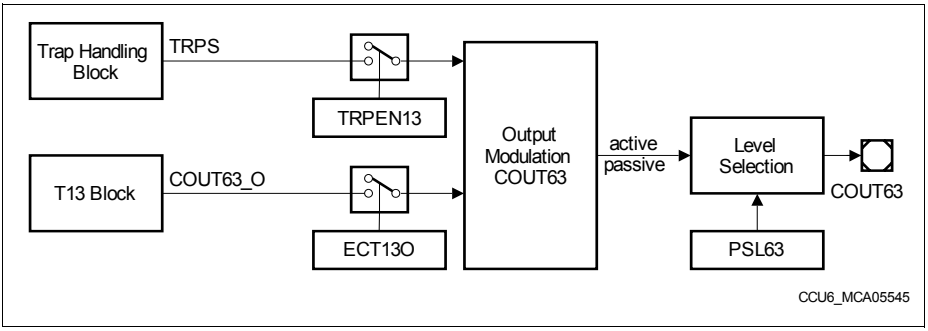


Figure 29-31 T13 Output Modulation

29.3.5 T13 Shadow Register Transfer

A special shadow transfer signal (T13_ST) can be generated to facilitate updating the period and compare values of the compare channel CC63 synchronously to the operation of T13. Providing a shadow register for values defining one PWM period facilitates a concurrent update by software for all relevant parameters. The next PWM period can run with a new set of parameters. The generation of this signal is requested by software via bit **TCTR0**.STE13 (set by writing 1 to the write-only bit **TCTR4**.T13STR, cleared by writing 1 to the write-only bit **TCTR4**.T13STD).
When signal T13_ST is active, a shadow register transfer is triggered with the next cycle of the T13 clock. Bit STE13 is automatically cleared with the shadow register transfer.
A T13 shadow register transfer takes place (T13_ST active):

- while timer T13 is not running (T13R = 0), or
- STE13 = 1 and a Period-Match is detected while T13R = 1

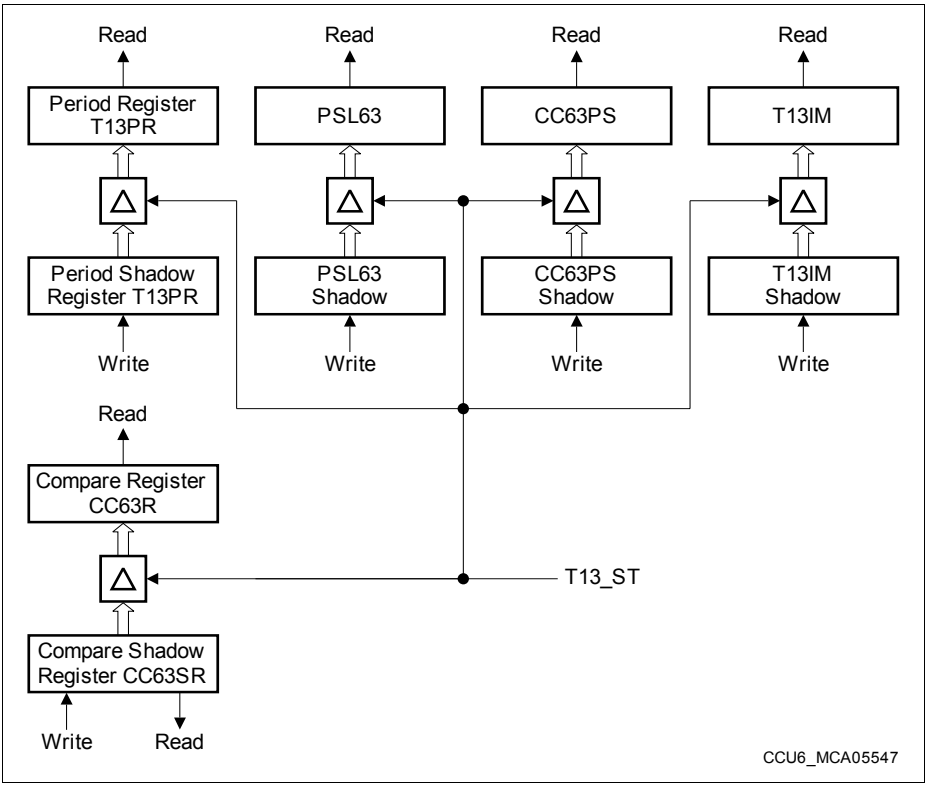


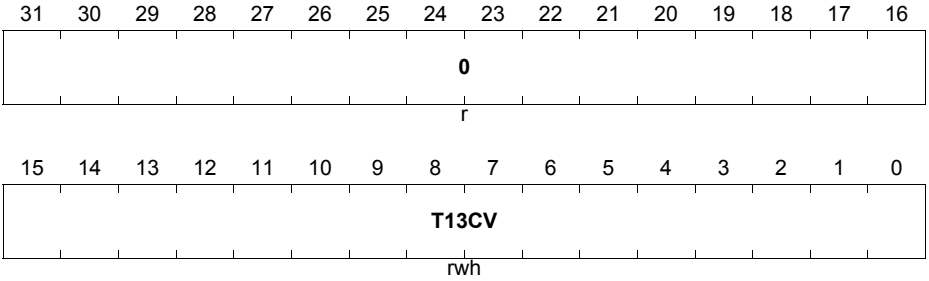
Figure 29-32 T13 Shadow Register Overview

29.3.6 T13 related Registers

29.3.6.1 T13 Counter Register

The generation of the patterns for a single channel pulse width modulation (PWM) is based on timer T13. The registers related to timer T13 can be concurrently updated (with well-defined conditions) in order to ensure consistency of the PWM signal. T13 can be synchronized to several timer T12 events.
Timer T13 only supports compare mode on its compare channel CC63.
Register T13 represents the counting value of timer T13. It can only be written while the timer T13 is stopped. Write actions while T13 is running are not taken into account. Register T13 can always be read by SW.
Timer T13 only supports edge-aligned mode (counting up).

T13
Timer T13 Counter Register **(50_H)** **Reset Value: 0000 0000_H**



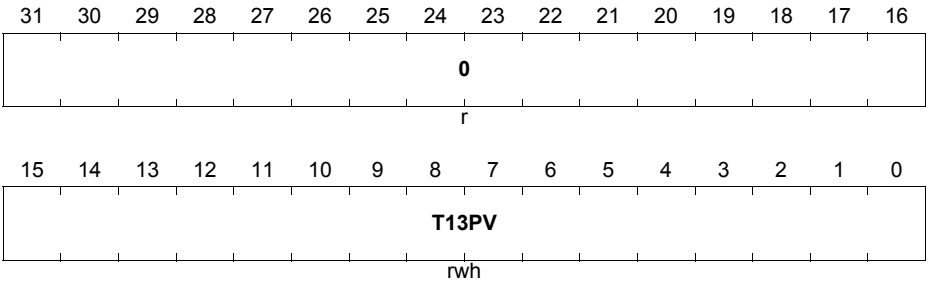
Field	Bits	Type	Description
T13CV	[15:0]	rwh	**Timer 13 Counter Value** This register represents the 16-bit counter value of Timer13.
0	[31:16]	r	**Reserved;** Returns 0 if read; should be written with 0.

Note: While timer T13 is stopped, the internal clock divider is reset in order to ensure reproducible timings and delays.

29.3.6.2 Period Register

Register T13PR contains the period value for timer T13. The period value is compared to the actual counter value of T13 and the resulting counter actions depend on the defined counting rules. This register has a shadow register and the shadow transfer is controlled by bit STE13. A read action by SW delivers the value currently used for the compare action, whereas the write action targets a shadow register. The shadow register structure allows a concurrent update of all T13-related values.

T13PR
Timer 13 Period Register **(54_H)** **Reset Value: 0000 0000_H**

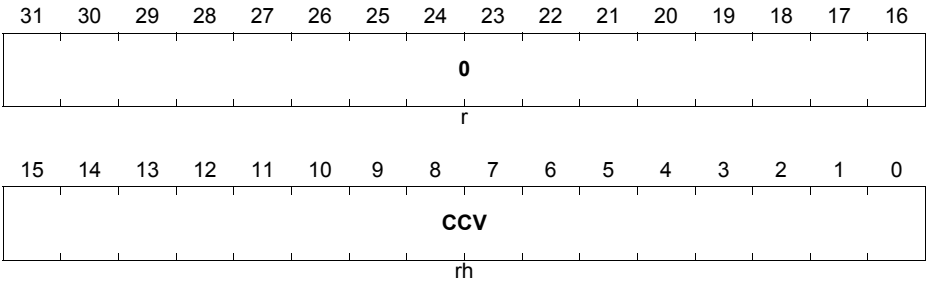


Field	Bits	Type	Description
T13PV	[15:0]	rwh	**T13 Period Value** The value T13PV defines the counter value for T13 leading to a period-match. When reaching this value, the timer T13 is set to zero.
0	[31:16]	r	**Reserved;** Returns 0 if read; should be written with 0.

29.3.6.3 Compare Register

Registers CC63R is the actual compare register for T13. The values stored in CC63R is compared to the counter value of T13. The State Bit CC63ST is located in register **CMPSTAT**.

CC63R
Compare Register for T13 **(58_H)** **Reset Value: 0000 0000$_H$**



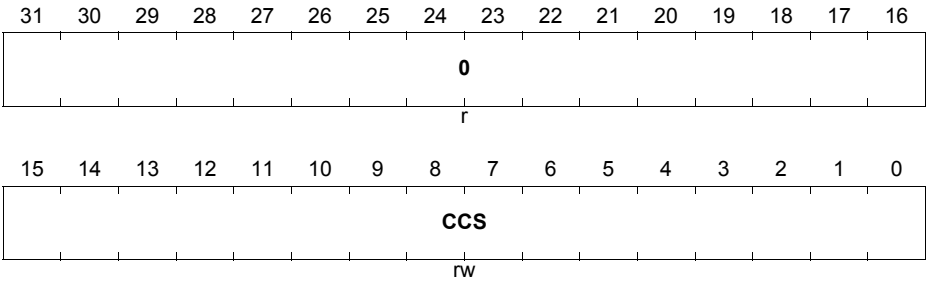
Field	Bits	Type	Description
CCV	[15:0]	rh	**Channel CC63 Compare Value** The bit field CCV contains the value, that is compared to the T13 counter value.
0	[31:16]	r	**Reserved;** Returns 0 if read; should be written with 0.

29.3.6.4 Compare Shadow Register

The register CC63R can only be read by SW, the modification of the value is done by a shadow register transfer from register CC63SR. The corresponding shadow register CC63SR can be read and written by SW.

CC63SR
Compare Shadow Register for T13

($5C_H$) **Reset Value: 0000 0000_H**



Field	Bits	Type	Description
CCS	[15:0]	rw	**Shadow Register for Channel CC63 Compare Value** The bit field contents of CCS is transferred to the bit field CCV during a shadow transfer.
0	[31:16]	r	**Reserved;** Returns 0 if read; should be written with 0.

29.4 Synchronous Start Feature

The T12 and T13 timers can be started synchronously through the T12HR and T13HR inputs of all CCU6x kernels.

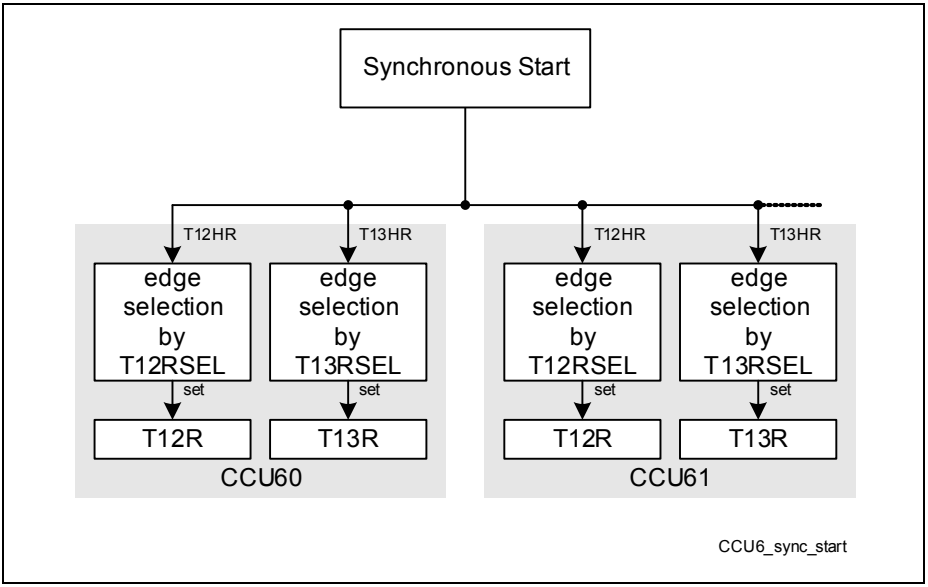


Figure 29-33 Synchronization Concept

29.5 Trap Handling

The trap functionality permits the PWM outputs to react on the state of the input signal CTRAP. This functionality can be used to switch off the power devices if the trap input becomes active (e.g. to perform an emergency stop). The trap handling and the effect on the output modulation are controlled by the bits in the trap control register **TRPCTR**. The trap flags TRPF and TRPS are located in register **IS** and can be set/cleared by SW by writing to registers **ISS** and **ISR**.
Figure 29-34 gives an overview on the trap function.

The Trap Flag TRPF monitors the trap input and initiates the entry into the Trap State. The Trap State Bit TRPS determines the effect on the outputs and controls the exit of the Trap State.
When a trap condition is detected ($\overline{\text{CTRAP}}$ = 0) and the input is enabled (TRPPEN = 1), both, the Trap Flag TRPF and the Trap State Bit TRPS, are set to 1 (trap state active). The output of the Trap State Bit TRPS leads to the Output Modulation Blocks (for T12 and for T13) and can there deactivate the outputs (set them to the passive state). Individual enable control bits for each of the six T12-related outputs and the T13-related output facilitate a flexible adaptation to the application needs.

There are a number of different ways to exit the Trap State. This offers SW the option to select the best operation for the application. Exiting the Trap State can be done either immediately when the trap condition is removed ($\overline{\text{CTRAP}}$ = 1 or TRPPEN = 0), or under software control, or synchronously to the PWM generated by either Timer T12 or Timer T13.

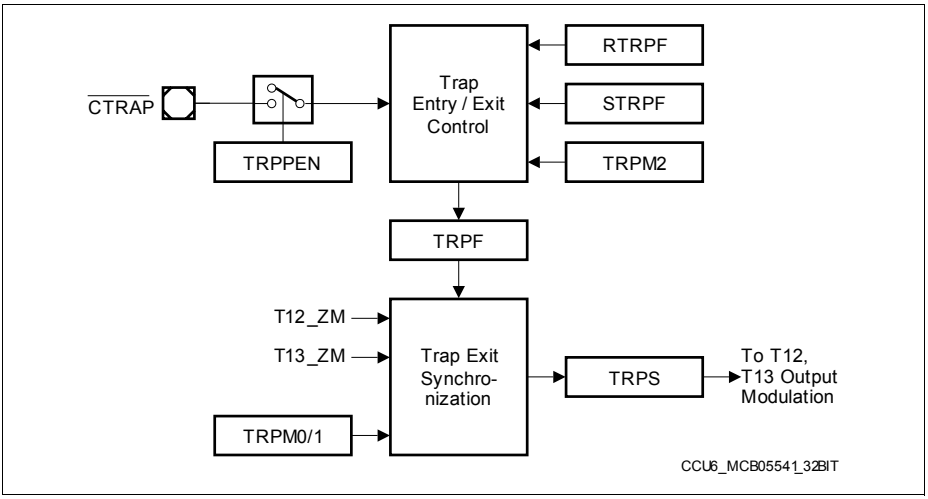


Figure 29-34 Trap Logic Block Diagram

Clearing of TRPF is controlled by the mode control bit TRPM2. If TRPM2 = 0, TRPF is automatically cleared by HW when $\overline{\text{CTRAP}}$ returns to the inactive level ($\overline{\text{CTRAP}}$ = 1) or if the trap input is disabled (TRPPEN = 0). When TRPM2 = 1, TRPF must be reset by SW after $\overline{\text{CTRAP}}$ has become inactive.

Clearing of TRPS is controlled by the mode control bits TRPM1 and TRPM0 (located in the Trap Control Register TRPCTR). A reset of TRPS terminates the Trap State and returns to normal operation. There are three options selected by TRPM1 and TRPM0. One is that the Trap State is left immediately when the Trap Flag TRPF is cleared, without any synchronization to timers T12 or T13. The other two options facilitate the synchronization of the termination of the Trap State to the count periods of either Timer T12 or Timer T13. **Figure 29-35** gives an overview on the associated operation.

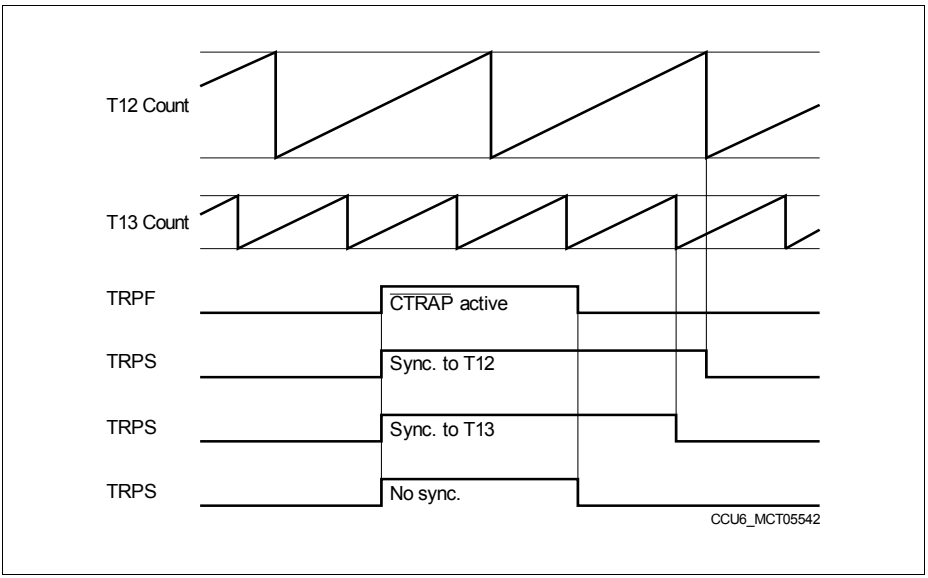


Figure 29-35 Trap State Synchronization (with TRPM2 = 0)

29.6 Multi-Channel Mode

The Multi-Channel mode offers the possibility to modulate all six T12-related output signals with one instruction. The bits in bit field **MCMOUT**.MCMP are used to specify the outputs that may become active. If Multi-Channel mode is enabled (bit **MODCTR**.MCMEN = 1), only those outputs may become active, that have a 1 at the corresponding bit position in bit field MCMP.
This bit field has its own shadow bit field **MCMOUTS**.MCMPS, that can be written by software. The transfer of the new value in MCMPS to the bit field MCMP can be triggered by, and synchronized to, T12 or T13 events. This structure permits the software to write the new value, that is then taken into account by the hardware at a well-defined moment and synchronized to a PWM signal. This avoids unintended pulses due to unsynchronized modulation sources.

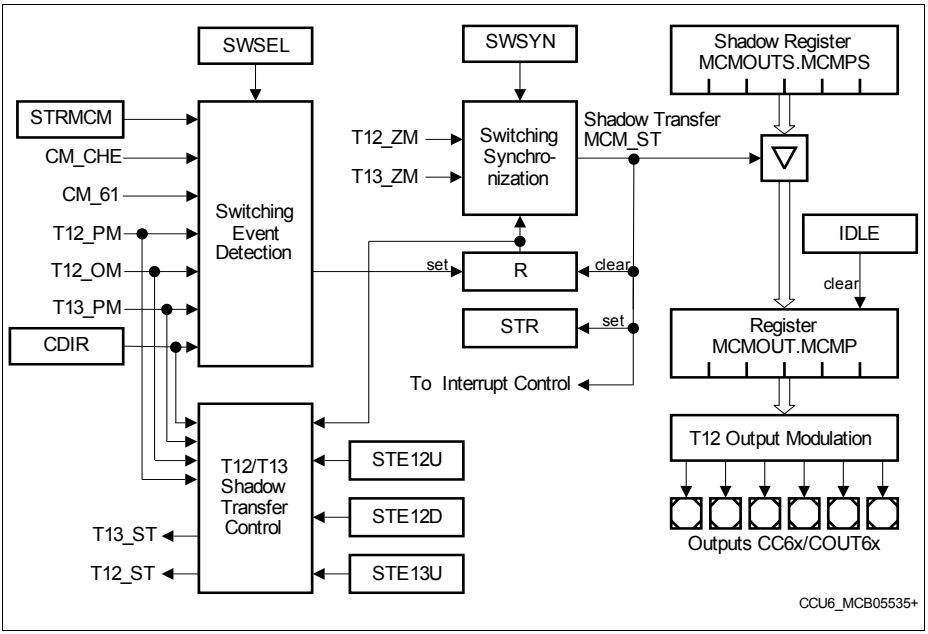


Figure 29-36 Multi-Channel Mode Block Diagram

Figure 29-36 shows the functional blocks for the Multi-Channel operation, controlled by bit fields in register **MCMCTR**. The event that triggers the update of bit field MCMP is chosen by SWSEL. In order to synchronize the update of MCMP to a PWM generated by T12 or T13, bit field SWSYN allows the selection of the synchronization event leading to the transfer from MCMPS to MCMP. Due to this structure, an update takes place with a new PWM period. A reminder flag R is set when the selected switching event occurs

(the event is not necessarily synchronous to the modulating PWM), and is cleared when the transfer takes place. This flag can be monitored by software to check for the status of this logic block. If the shadow transfer from MCMPS to MCMP takes place, bit **IS**.STR becomes set and an interrupt can be generated.
In addition to the Multi-Channel shadow transfer event MCM_ST, the shadow transfers for T12 (T12_ST) and T13 (T13_ST) can be generated to allow concurrent updates of applied duty cycles for T12 and/or T13 modulation and Multi-Channel patterns.

If it is explicitly desired, the update takes place immediately with the occurrence of the selected event when the direct synchronization mode is selected. The update can also be requested by software by writing to bit field MCMPS with the shadow transfer request bit STRMCM = 1. The option to trigger an update by SW is possible for all settings of SWSEL.
By using the direct mode and bit STRMCM = 1, the update takes place completely under software control.

Table 29-9 Multi-Channel Mode Switching Event Selection

SWSEL	Selected Event (see register MCMCTR)
000_B	No automatic event detection
001_B	Correct Hall Event (CM_CHE) detected at input signals CCPOSx without additional delay
010_B	T13 Period-Match (T13_PM)
011_B	T12 One-Match while counting down (T12_OM and CDIR = 1)
100_B	T12 Compare Channel 1 Event while counting up (CM_61 and CDIR = 0) to support the phase delay function by CC61 for block commutation mode.
101_B	T12 Period-Match while counting up (T12_PM and CDIR = 0)
110_B, 111_B	Reserved, no action

Table 29-10 Multi-Channel Mode Switching Synchronization

SWSYN	Synchronization Event (see register MCMCTR)
00_B	Direct Mode: the trigger event directly causes the shadow transfer
01_B	T13 Zero-Match (T13_ZM), the MCM shadow transfer is synchronized to a T13 PWM
10_B	T12 Zero-Match (T12_ZM), the MCM shadow transfer is synchronized to a T12 PWM
11_B	Reserved, no action

29.7 Hall Sensor Mode

For Brushless DC-Motors in block commutation mode, the Multi-Channel Mode has been introduced to provide efficient means for switching pattern generation. These patterns need to be output in relation to the angular position of the motor. For this, usually Hall sensors or Back-EMF sensing are used to determine the angular rotor position. The CCU6 provides three inputs, CCPOS0, CCPOS1, and CCPOS2, that can be used as inputs for the Hall sensors or the Back-EMF detection signals.

There is a strong correlation between the motor position and the output modulation pattern. When a certain position of the motor has been reached, indicated by the sampled Hall sensor inputs (the Hall pattern), the next, pre-determined Multi-Channel Modulation pattern has to be output. Because of different machine types, the modulation pattern for driving the motor can vary. Therefore, it is wishful to have a wide flexibility in defining the correlation between the Hall pattern and the corresponding Modulation pattern. Furthermore, a hardware mechanism significantly reduces the CPU for block-commutation.

The CCU6 offers the flexibility by having a register containing the currently assumed Hall pattern (CURH), the next expected Hall pattern (EXPH) and the corresponding output pattern (MCMP). A new Modulation pattern is output when the sampled Hall inputs match the expected ones (EXPH). To detect the next rotation phase (segment for block commutation), the CCU6 monitors the Hall inputs for changes. When the next expected Hall pattern is detected, the next corresponding Modulation pattern is output.

To increase for noise immunity (to a certain extend), the CCU6 offers the possibility to introduce a sampling delay for the Hall inputs. Some changes of the Hall inputs are not leading to the expected Hall pattern, because they are only short spikes due to noise. The Hall pattern compare logic compares the Hall inputs to the next expected pattern and also to the currently assumed pattern to filter out spikes.

For the Hall and Modulation output patterns, a double-register structure is implemented. While register **MCMOUT** holds the actually used values, its shadow register **MCMOUTS** can be loaded by software from a pre-defined table, holding the appropriate Hall and Modulation patterns for the given motor control.
A transfer from the shadow register into register MCMOUT can take place when a correct Hall pattern change is detected. Software can then load the next values into register MCMOUTS. It is also possible by software to force a transfer from MCMOUTS into MCMOUT.

Note: The Hall input signals CCPOSx and the CURH and EXPH bit fields are arranged in the following order:
CCPOS0 corresponds to CURH.0 (LSB) and EXPH.0 (LSB)
CCPOS1 corresponds to CURH.1 and EXPH.1
CCPOS2 corresponds to CURH.2 (MSB) and EXPH.2 (MSB)

29.7.1 Hall Pattern Evaluation

The Hall sensor inputs CCPOSx can be permanently monitored via an edge detection block (with the module clock f_{CC6}). In order to suppress spikes on the Hall inputs due to noise in rugged inverter environment, two optional noise filtering methods are supported by the Hall logic (both methods can be combined).

- Noise filtering with delay:
  For this function, the mode control bit fields MSEL6x for all T12 compare channels must be programmed to 1000_B and DBYP = 0. The selected event triggers Dead-Time Counter 0 to generate a programmable delay (defined by bit field DTM). When the delay has elapsed, the evaluation signal HCRDY becomes activated.
  Output modulation with T12 PWM signals is not possible in this mode.
- Noise filtering by synchronization to PWM:
  The Hall inputs are not permanently monitored by the edge detection block, but samples are taken only at defined points in time during a PWM period. This can be used to sample the Hall inputs when the switching noise (due to PWM) does not disturb the Hall input signals.

If neither the delay function of Dead-Time Counter 0 is not used for the Hall pattern evaluation nor the Hall mode for Brushless DC-Drive control is enabled, the timer T12 block is available for PWM generation and output modulation.

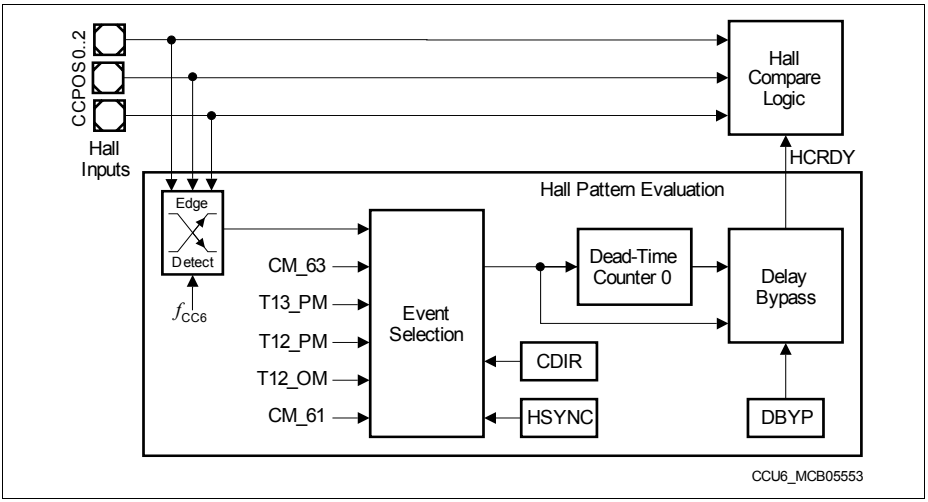


Figure 29-37 Hall Pattern Evaluation

If the evaluation signal HCRDY (Hall Compare Ready, see **Figure 29-38**) becomes activated, the Hall inputs are sampled and the Hall compare logic starts the evaluation of the Hall inputs.

Figure 29-37 illustrates the events for Hall pattern evaluation and the noise filter logic, Table 29-11 summarizes the selectable trigger input signals.

Table 29-11 Hall Sensor Mode Trigger Event Selection

HSYNC	Selected Event (see register T12MSEL)
000_B	Any edge at any of the inputs CCPOSx, independent from any PWM signal (permanent check).
001_B	A T13 Compare-Match (CM_63).
010_B	A T13 Period-Match (T13_PM).
011_B	Hall sampling triggered by HW sources is switched off.
100_B	A T12 Period-Match while counting up (T12_PM and CDIR = 0).
101_B	A T12 One-Match while counting down (T12_OM and CDIR = 1).
110_B	A T12 Compare-Match of compare channel CC61 while counting up (CM_61 and CDIR = 0).
111_B	A T12 Compare-Match of compare channel CC61 while counting down (CM_61 and CDIR = 1).

29.7.2 Hall Pattern Compare Logic

Figure 29-38 gives an overview on the double-register structure and the pattern compare logic. Software writes the next modulation pattern (MCMPS) and the corresponding current (CURHS) and expected (EXPHS) Hall patterns into the shadow register MCMOUTS. Register MCMOUT holds the actually used values CURH and EXPH. The modulation pattern MCMP is provided to the T12 Output Modulation block. The current (CURH) and expected (EXPH) Hall patterns are compared to the sampled Hall sensor inputs (visible in register **CMPSTAT**). Sampling of the inputs and the evaluation of the comparator outputs is triggered by the evaluation signal HCRDY (Hall Compare Ready), that is detailed in the next section.

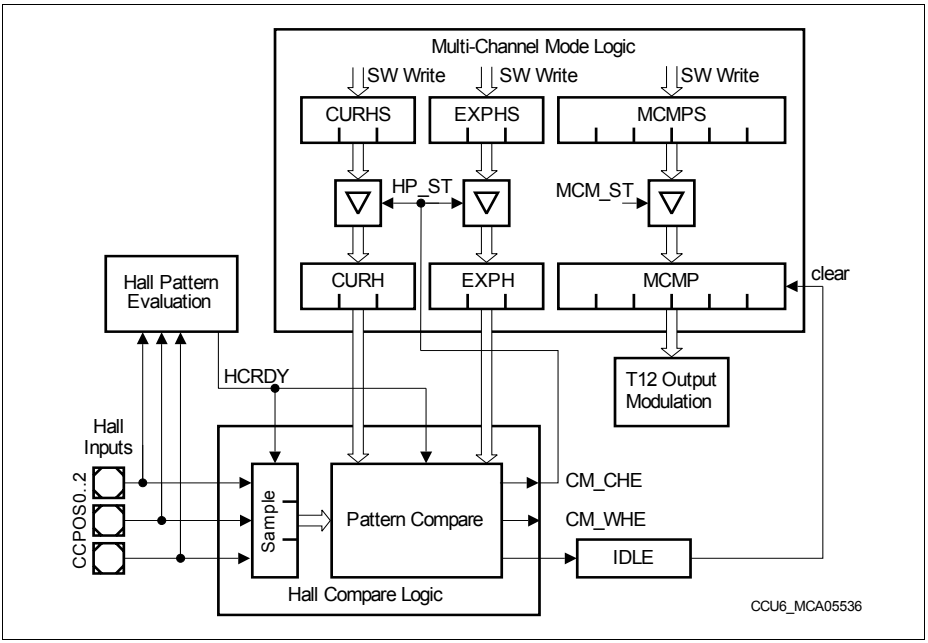


Figure 29-38 Hall Pattern Compare Logic

- If the sampled Hall pattern matches the value programmed in CURH, the detected transition was a spike (no Hall event) and no further actions are necessary.
- If the sampled Hall pattern matches the value programmed in EXPH, the detected transition was the expected event (correct Hall event CM_CHE) and the MCMP value has to change.
- If the sampled Hall pattern matches neither CURH nor EXPH, the transition was due to a major error (wrong Hall event CM_CWE) and can lead to an emergency shut down (IDLE).

At every correct Hall event (CM_CHE), the next Hall patterns are transferred from the shadow register MCMOUTS into MCMOUT (Hall pattern shadow transfer HP_ST), and a new Hall pattern with its corresponding output pattern can be loaded (e.g. from a predefined table in memory) by software into MCMOUTS. For the Modulation patterns, signal MCM_ST is used to trigger the transfer.
Loading this shadow register can also be done by writing MCMOUTS.STRHP = 1 (for EXPH and CURH) or MCMOUTS.STRMCMP = 1 (for MCMP).

29.7.3 Hall Mode Flags

Depending on the Hall pattern compare operation, a number of flags are set in order to indicate the status of the module and to trigger further actions and interrupt requests.

Flag **IS**.CHE (Correct Hall Event) is set by signal CM_CHE when the sampled Hall pattern matches the expected one (EXPH). This flag can also be set by SW by setting bit **ISS**.SCHE = 1. If enabled by bit **IEN**.ENCHE = 1, the set signal for CHE can also generate an interrupt request to the CPU. Bit field **INP**.INPCHE defines which service request output becomes activated in case of an interrupt request.To clear flag CHE, SW needs to write **ISR**.RCHE = 1.
Flag IS.WHE indicates a Wrong Hall Event. Its handling for flag setting and resetting as well as interrupt request generation are similar to the mechanism for flag CHE.
The implementation of flag STR is done in the same way as for CHE and WHE. This flag is set by HW by the shadow transfer signal MCM_ST (see also **Figure 29-36**).

Please note that for flags CHE, WHE, and STR, the interrupt request generation is triggered by the set signal for the flag. That means, a request can be generated even if the flag is already set. There is no need to clear the flag in order to enable further interrupt requests.

The implementation for the IDLE flag is different. It is set by HW through signal CM_WHE if enabled by bit ENIDLE. Software can also set the flag via bit SIDLE. As long as bit IDLE is set, the modulation pattern field MCMP is cleared to force the outputs to the passive state. Flag IDLE must be cleared by software by writing RIDLE = 1 in order to return to normal operation. To fully restart from IDLE mode, the transfer requests for the bit fields in register MCMOUTS to register MCMOUT have to be initiated by software via bits STRMCM and STRHP in register MCMOUTS. In this way, the release from IDLE mode is under software control, but can be performed synchronously to the PWM signal.

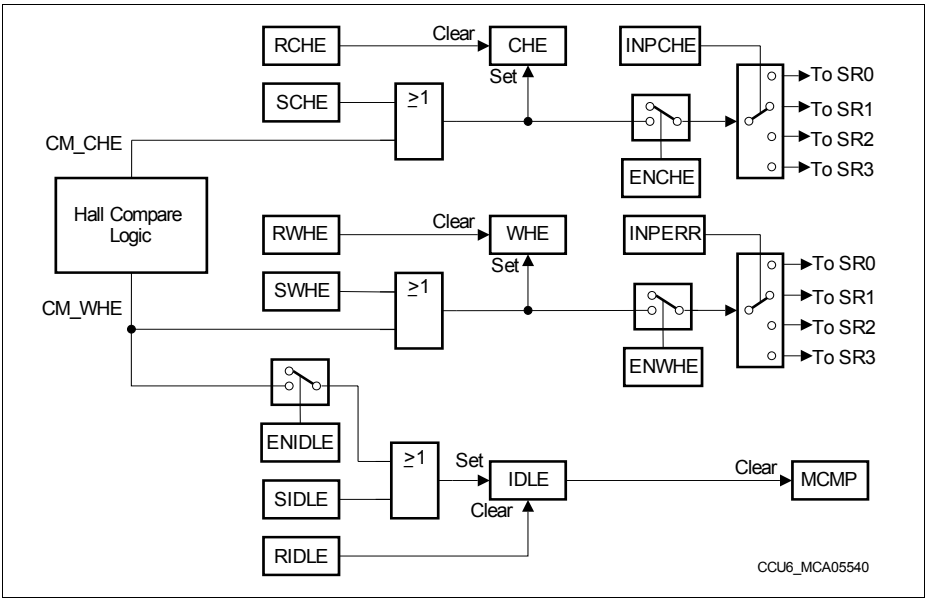


Figure 29-39 Hall Mode Flags

29.7.4 Hall Mode for Brushless DC-Motor Control

The CCU6 provides a mode for the Timer T12 Block especially targeted for convenient control of block commutation patterns for Brushless DC-Motors. This mode is selected by setting all **T12MSEL**.MSEL6x bit fields of the three T12 Channels to 1000_B.
In this mode, illustrated in **Figure 29-40**, channel CC60 is placed in capture mode to measure the time elapsed between the last two correct Hall events, channel CC61 in compare mode to provide a programmable phase delay between the Hall event and the application of a new PWM output pattern, and channel CC62 also in compare mode as first time-out criterion. A second time-out criterion can be built by the T12 period match event.

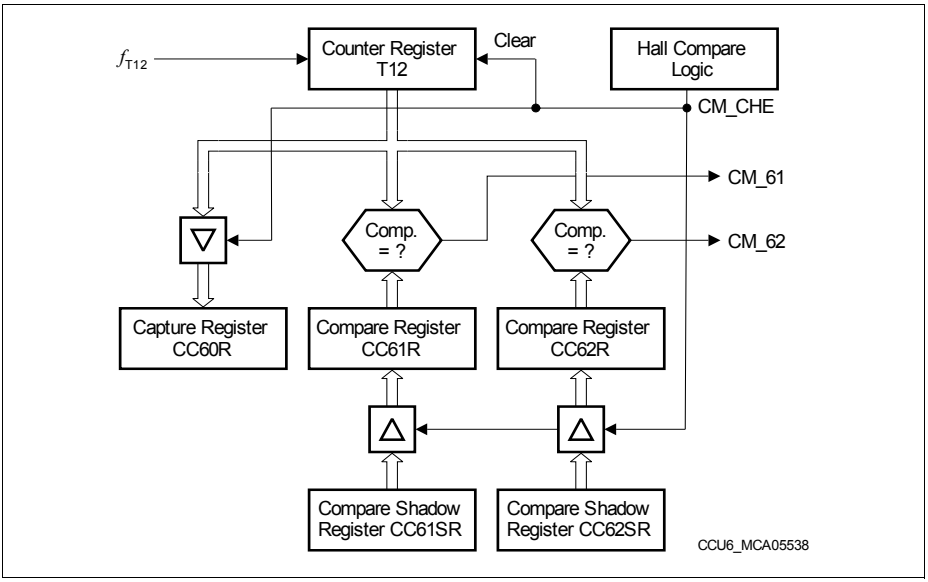


Figure 29-40 T12 Block in Hall Sensor Mode

The signal CM_CHE from the Hall compare logic is used to transfer the new compare values from the shadow registers CC6xSR into the actual compare registers CC6xR, performs the shadow transfer for the T12 period register, to capture the current T12 contents into register CC60R, and to clear T12.

Note: In this mode, the shadow transfer signal T12_ST is not generated. Not all shadow bits, such as the PSLy bits, will be transferred to their main registers. To program the main registers, SW needs to write to these registers while Timer T12 is stopped. In this case, a SW write actualizes both registers.

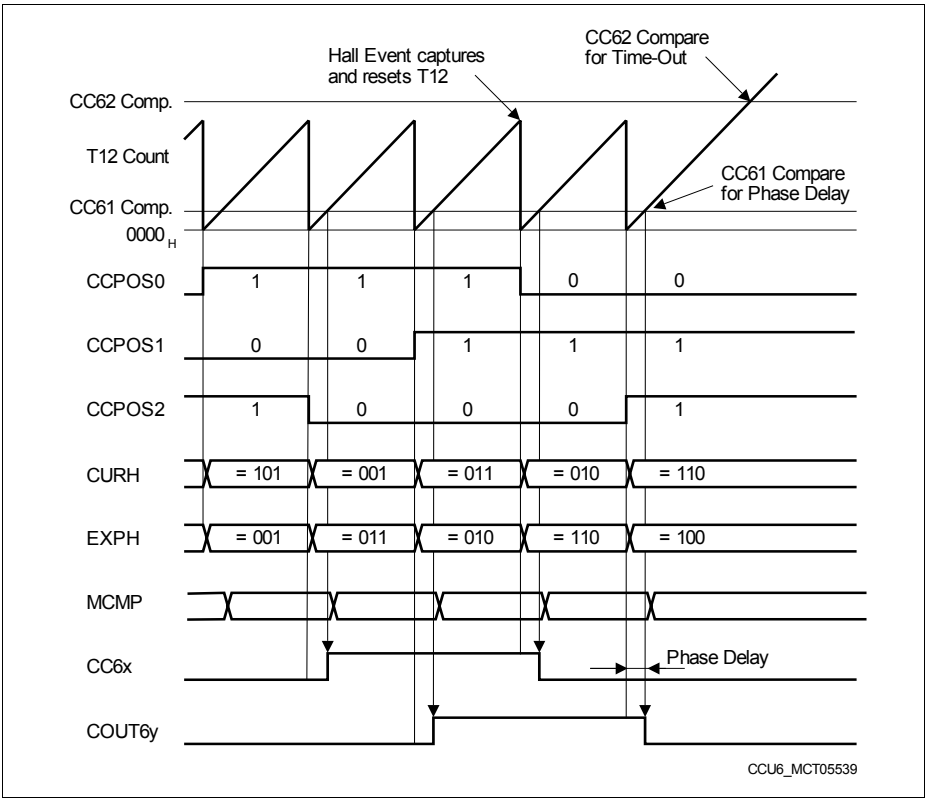


Figure 29-41 Brushless DC-Motor Control Example (all MSEL6x = 1000_B)

After the detection of an expected Hall pattern (CM_CHE active), the T12 count value is captured into channel CC60 (representing the actual rotor speed by measuring the elapsed time between the last two correct Hall events), and T12 is reset. When the timer reaches the compare value in channel CC61, the next multi-channel state is switched by triggering the shadow transfer of bit field MCMP (if enabled in bit field **SWEN**). This trigger event can be combined with the synchronization of the next multi-channel state to the PWM source (to avoid spikes on the output lines, see **Section 29.6**). This compare function of channel CC61 can be used as a phase delay from the position sensor input signals to the switching of the output signals, that is necessary if a sensorless back-EMF technique or Hall sensors are used. The compare value in channel CC62 can be used as a time-out trigger (interrupt), indicating that the actual motor speed is far below the desired destination value. An abnormal load change can be detected with this feature and PWM generation can be disabled.

29.8 Modulation Control Registers

29.8.1 Modulation Control

This register contains bits enabling the modulation of the corresponding output signal by PWM pattern generated by the timers T12 and T13. Furthermore, the multi-channel mode can be enabled as additional modulation source for the output signals.

MODCTR
Modulation Control Register **(80_H)** **Reset Value: 0000 0000_H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ECT 13O	0	T13MODEN						MCM EN	0	T12MODEN					
rw	r	rw						rw	r	rw					

Field	Bits	Type	Description
T12MODEN	[5:0]	rw	**T12 Modulation Enable** These bits enable the modulation of the corresponding output signal by a PWM pattern generated by timer T12. T12MODEN0 = MODCTR.0 for output CC60 T12MODEN1 = MODCTR.1 for output COUT60 T12MODEN2 = MODCTR.2 for output CC61 T12MODEN3 = MODCTR.3 for output COUT61 T12MODEN4 = MODCTR.4 for output CC62 T12MODEN5 = MODCTR.5 for output COUT62 0_B The modulation of the corresponding output signal by a T12 PWM pattern is disabled. 1_B The modulation of the corresponding output signal by a T12 PWM pattern is enabled.
MCMEN	7	rw	**Multi-Channel Mode Enable** 0_B The modulation of the corresponding output signal by a multi-channel pattern according to bit field MCMOUT is disabled. 1_B The modulation of the corresponding output signal by a multi-channel pattern according to bit field MCMOUT is enabled.
T13MODEN	[13:8]	rw	**T13 Modulation Enable** These bits enable the modulation of the corresponding output signal by the PWM pattern CC63_O generated by timer T13. T13MODEN0 = MODCTR.8 for output CC60 T13MODEN1 = MODCTR.9 for output COUT60 T13MODEN2 = MODCTR.10 for output CC61 T13MODEN3 = MODCTR.11 for output COUT61 T13MODEN4 = MODCTR.12 for output CC62 T13MODEN5 = MODCTR.13 for output COUT62 0_B The modulation of the corresponding output signal by a T13 PWM pattern is disabled. 1_B The modulation of the corresponding output signal by a T13 PWM pattern is enabled.

Field	Bits	Type	Description
ECT13O	15	rw	**Enable Compare Timer T13 Output** 0_B The output COUT63 is in the passive state. 1_B The output COUT63 is enabled for the PWM signal generated by T13.
0	6, 14, [31:16]	r	**Reserved;** Returns 0 if read; should be written with 0.

29.8.2 Trap Control Register

The register TRPCTR controls the trap functionality. It contains independent enable bits for each output signal and control bits to select the behavior in case of a trap condition. The trap condition is a low level on the $\overline{\text{CTRAP}}$ input pin, that is monitored (inverted level) by bit IS.TRPF. While TRPF=1 (trap input active), the trap state bit IS.TRPS is set to 1.

TRPCTR
Trap Control Register **(84_H)** **Reset Value: 0000 0000$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TRPPEN	TRPEN13	TRPEN						0					TRPM2	TRPM1	TRPM0
rw	rw	rw						r					rw	rw	rw

Field	Bits	Type	Description
TRPM1, TRPM0	1, 0	rw	**Trap Mode Control Bits 1, 0** These two bits define the behavior of the selected outputs when leaving the trap state after the trap condition has become inactive again. A synchronization to the timer driving the PWM pattern avoids unintended pulses when leaving the trap state. The combination [TRPM1, TRPM0] leads to: 00_B The trap state is left (return to normal operation) after TRPF has become 0 again when a zero-match of T12 (while counting up) is detected (synchronization to T12). 01_B The trap state is left (return to normal operation) after TRPF has become 0 again when a zero-match of T13 is detected (synchronization to T13). 10_B reserved 11_B The trap state is left (return to normal operation) immediately after TRPF has become 0 again without any synchronization to T12 or T13.
TRPM2	2	rw	**Trap Mode Control Bit 2** This bit defines how the trap flag TRPF can be cleared after the trap input condition ($\overline{\text{CTRAP}}$ = 0 and TRPPEN = 1) is no longer valid (either by $\overline{\text{CTRAP}}$ = 1 or by TRPPEN = 0). 0_B Automatic Mode: Bit TRPF is cleared by HW if the trap input condition is no longer valid. 1_B Manual Mode: Bit TRPF stays 0 after the trap input condition is no longer valid. It has to be cleared by SW by writing ISR.RTRPF = 1.

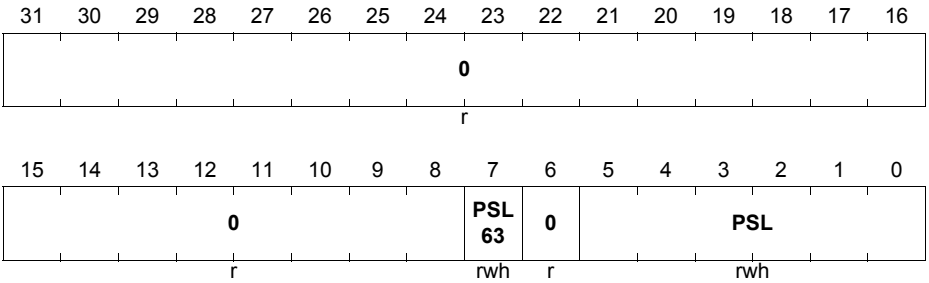
Field	Bits	Type	Description
TRPEN	[13:8]	rw	**Trap Enable Control** Setting a bit enables the trap functionality for the following corresponding output signals: TRPEN0 = TRPCTR.8 for output CC60 TRPEN1 = TRPCTR.9 for output COUT60 TRPEN2 = TRPCTR.10 for output CC61 TRPEN3 = TRPCTR.11 for output COUT61 TRPEN4 = TRPCTR.12 for output CC62 TRPEN5 = TRPCTR.13 for output COUT62 0_B The trap functionality of the corresponding output signal is disabled. The output state is independent from bit IS.TRPS. 1_B The trap functionality of the corresponding output signal is enabled. The output state is set to the passive while IS.TRPS=1.
TRPEN13	14	rw	**Trap Enable Control for Timer T13** 0_B The trap functionality for output COUT63 is disabled. The output state is independent from bit IS.TRPS. 1_B The trap functionality for output COUT63 is enabled. The output state is set to the passive while IS.TRPS=1.
TRPPEN	15	rw	**Trap Pin Enable** This bit enables the input (pin) function for the trap generation. An interrupt can only be generated if a falling edge is detected at pin $\overline{\text{CTRAP}}$ while TRPPEN = 1. 0_B The CCU6 trap functionality based on the input $\overline{\text{CTRAP}}$ is disabled. A CCU6 trap can only be generated by SW by setting bit TRPF. 1_B The CCU6 trap functionality based on the input $\overline{\text{CTRAP}}$ is enabled. A CCU6 trap can be generated by SW by setting bit TRPF or by $\overline{\text{CTRAP}}$=0.
0	[7:3], [31:16]	r	**Reserved;** Returns 0 if read; should be written with 0.

29.8.3 Passive State Level Register

Register PSLR defines the passive state level of the PWM outputs of the module. The passive state level is the value that is driven during the passive state of the output. During the active state, the corresponding output pin drives the active state level, that is the inverted passive state level. The passive state level permits to adapt the driven output levels to the driver polarity (inverted, not inverted) of the connected power stage. The bits in this register have shadow bit fields to permit a concurrent update of all PWM-related parameters (bit field PSL is updated with T12_ST, whereas PSL63 is updated with T13_ST). The actually used values can be read (attribute “rh”), whereas the shadow bits can only be written (attribute “w”).

PSLR

Passive State Level Register **(88_H)** **Reset Value: $0000\ 0000_H$**



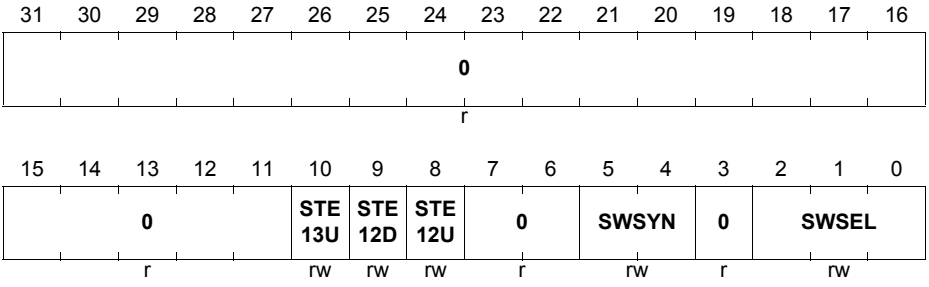
Field	Bits	Type	Description
PSL	[5:0]	rwh	**Compare Outputs Passive State Level** These bits define the passive level driven by the module outputs during the passive state. PSL0 = PSLR.0 for output CC60 PSL1 = PSLR.1 for output COUT60 PSL2 = PSLR.2 for output CC61 PSL3 = PSLR.3 for output COUT61 PSL4 = PSLR.4 for output CC62 PSL5 = PSLR.5 for output COUT62 0_B The passive level is 0. 1_B The passive level is 1.
PSL63	7	rwh	**Passive State Level of Output COUT63** This bit defines the passive level driven by the module output COUT63 during the passive state. 0_B The passive level is 0. 1_B The passive level is 1.
0	6, [31:8]	r	**Reserved;** Returns 0 if read; should be written with 0.

29.8.4 Multi-Channel Mode Registers

Register MCMCTR contains control bits for the multi-channel functionality.

MCMCTR
Multi-Channel Mode Control Register

(94_H) **Reset Value: 0000 0000$_H$**



Field	Bits	Type	Description
SWSEL	[2:0]	rw	**Switching Selection** Bit field SWSEL selects one of the following trigger request sources (next multi-channel event) for the shadow transfer MCM_ST from MCMPS to MCMP. The trigger request is stored in the reminder flag R until the shadow transfer is done and flag R is cleared automatically with the shadow transfer. The shadow transfer takes place synchronously with an event selected in bit field SWSYN. 000_B No trigger request will be generated 001_B Correct Hall pattern detected (CM_CHE) 010_B T13 period-match detected (while counting up) 011_B T12 one-match (while counting down) 100_B T12 channel 1 compare-match detected (phase delay function) 101_B T12 period match detected (while counting up) 110_B reserved, no trigger request will be generated 111_B reserved, no trigger request will be generated
SWSYN	[5:4]	rw	**Switching Synchronization** Bit field SWSYN defines the synchronization mechanism of the shadow transfer event MCM_ST if it has been requested before (flag R set by an event selected by SWSEL) and if MCMEN = 1. This feature permits the synchronization of the outputs to the PWM source, that is used for modulation (T12 or T13). 00_B Direct; the trigger event immediately leads to the shadow transfer 01_B A T13 zero-match triggers the shadow transfer 10_B A T12 zero-match (while counting up) triggers the shadow transfer 11_B reserved; no action
STE12U	8	rw	**Shadow Transfer Enable for T12 Upcounting** This bit enables the shadow transfer T12_ST if flag MCMOUT.R is set or becomes set while a T12 period match is detected while counting up. 0_B No action 1_B The T12_ST shadow transfer mechanism is enabled if MCMEN = 1.

Field	Bits	Type	Description
STE12D	9	rw	**Shadow Transfer Enable for T12 Downcounting** This bit enables the shadow transfer T12_ST if flag MCMOUT.R is set or becomes set while a T12 one match is detected while counting down. 0_B No action 1_B The T12_ST shadow transfer mechanism is enabled if MCMEN = 1.
STE13U	10	rw	**Shadow Transfer Enable for T13 Upcounting** This bit enables the shadow transfer T13_ST if flag MCMOUT.R is set or becomes set while a T13 period match is detected. 0_B No action 1_B The T13_ST shadow transfer mechanism is enabled if MCMEN = 1.
0	3, [7:6], [31:11]	r	**Reserved;** Returns 0 if read; should be written with 0.

Register MCMOUTS contains bits used as pattern input for the multi-channel mode and the Hall mode. This register is a shadow register (that can be read and written) for register MCMOUT, indicating the currently active signals.

MCMOUTS
Multi-Channel Mode Output Shadow Register

($8C_H$) **Reset Value: $0000\ 0000_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STRHP	0	CURHS			EXPHS			STRMCM	0	MCMPS					
w	r	rw			rw			w	r	rw					

Field	Bits	Type	Description
MCMPS	[5:0]	rw	**Multi-Channel PWM Pattern Shadow** Bit field MCMPS is the shadow bit field for bit field MCMP. The multi-channel shadow transfer is triggered by MCM_ST according to the transfer conditions defined by register MCMCTR.
STRMCM	7	w	**Shadow Transfer Request for MCMPS** Writing STRMCM = 1 leads to an immediate activation of MCM_ST to update bit field MCMP by the value of MCMPS. When read, this bit always delivers 0. 0_B No action. 1_B Bit field MCMP is updated.
EXPHS	[10:8]	rw	**Expected Hall Pattern Shadow** Bit field EXPHS is the shadow bit field for bit field EXPH. The shadow transfer takes place when a correct Hall event is detected (CM_CHE).
CURHS	[13:11]	rw	**Current Hall Pattern Shadow** Bit field CURHS is the shadow bit field for bit field CURH. The shadow transfer takes place when a correct Hall event is detected (CM_CHE).

Field	Bits	Type	Description
STRHP	15	w	**Shadow Transfer Request for the Hall Pattern** Writing STRHP = 1 leads to an immediate activation of HP_ST to update bit fields EXPH and CURH by EXPHS and CURHS. When read, this bit always delivers 0. 0_B No action. 1_B Bit fields EXPH and CURH are updated.
0	6, 14 [31:16]	r	**Reserved;** Returns 0 if read; should be written with 0.

MCMOUT
Multi-Channel Mode Output Register

(90_H) **Reset Value: 0000 0000$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0		**CURH**			**EXPH**			**0**	**R**	**MCMP**					
r		rh			rh			r	rh	rh					

Field	Bits	Type	Description
MCMP	[5:0]	rh	**Multi-Channel PWM Pattern** Bit field MCMP defines the output pattern for the multi-channel mode. If this mode is enabled by MODCTR.MCMEN = 1, the output state of all T12 related PWM outputs can be modified. This bit field is 0 while IS.IDLE = 1. MCMP0 = MCMOUT.0 for output CC60 MCMP1 = MCMOUT.1 for output COUT60 MCMP2 = MCMOUT.2 for output CC61 MCMP3 = MCMOUT.3 for output COUT61 MCMP4 = MCMOUT.4 for output CC62 MCMP5 = MCMOUT.5 for output COUT62 0_B The output is set to the passive state. A PWM generated by T12 or T13 are not taken into account. 1_B The output can be in the active state, depending on the enabled PWM modulation signals generated by T12, T13 and the trap state.
R	6	rh	**Reminder Flag** This flag indicates that the shadow transfer from MCMPS to MCMP has been requested by the selected trigger source. It is cleared when the shadow transfer takes place or while MCMEN=0. 0_B A shadow transfer MCM_ST is not requested. 1_B A shadow transfer MCM_ST is requested, but has not yet been executed, because the selected synchronization condition has not yet occurred.
EXPH	[10:8]	rh	**Expected Hall Pattern** Bit field EXPH is updated by a shadow transfer HP_ST from bit field EXPHS. If HCRDY = 1, EXPH is compared to the sampled CCPOSx inputs in order to detect the occurrence of the next desired (=expected) hall pattern or a wrong pattern. If the sampled hall pattern at the hall input pins is equal to bit field EXPH, a correct Hall event has been detected (CM_CHE).

Field	Bits	Type	Description
CURH	[13:11]	rh	**Current Hall Pattern** Bit field CURH is updated by a shadow transfer HP_ST from bit field CURHS. If HCRDY = 1, CURH is compared to the sampled CCPOSx inputs in order to detect a spike. If the sampled Hall pattern at the Hall input pins is equal to bit field CURH, no Hall event has been detected. If the sampled Hall input pattern is neither equal to CURH nor equal to EXPH, the Hall event was not the desired one and may be due to a fatal error (e.g. blocked rotor, etc.). In this case, a wrong Hall event has been detected (CM_WHE).
0	7, [31:14]	r	**Reserved;** Returns 0 if read; should be written with 0.

29.9 Interrupt Handling

This section describes the interrupt handling of the CCU6 module.

29.9.1 Interrupt Structure

The HW interrupt event or the SW setting of the corresponding interrupt set bit (in register ISS) sets the event indication flags (in register IS) and can trigger the interrupt generation. The interrupt pulse is generated independently from the interrupt status flag in register IS (it is not necessary to clear the related status bit to be able to generate another interrupt). The interrupt flag can be cleared by SW by writing to the corresponding bit in register ISR.

If enabled by the related interrupt enable bit in register IEN, an interrupt pulse can be generated on one of the four service request outputs (SR0 to SR3) of the module. If more than one interrupt source is connected to the same interrupt node pointer (in register INP), the requests are logically OR-combined to one common service request output (see **Figure 29-42**).

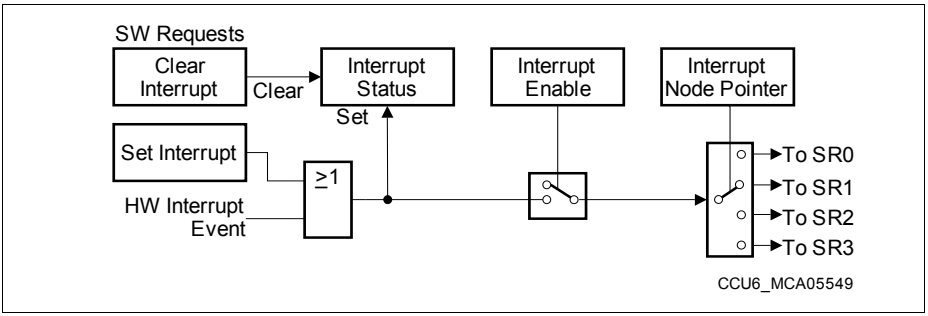


Figure 29-42 General Interrupt Structure

The available interrupt events in the CCU6 are shown in **Figure 29-43**.

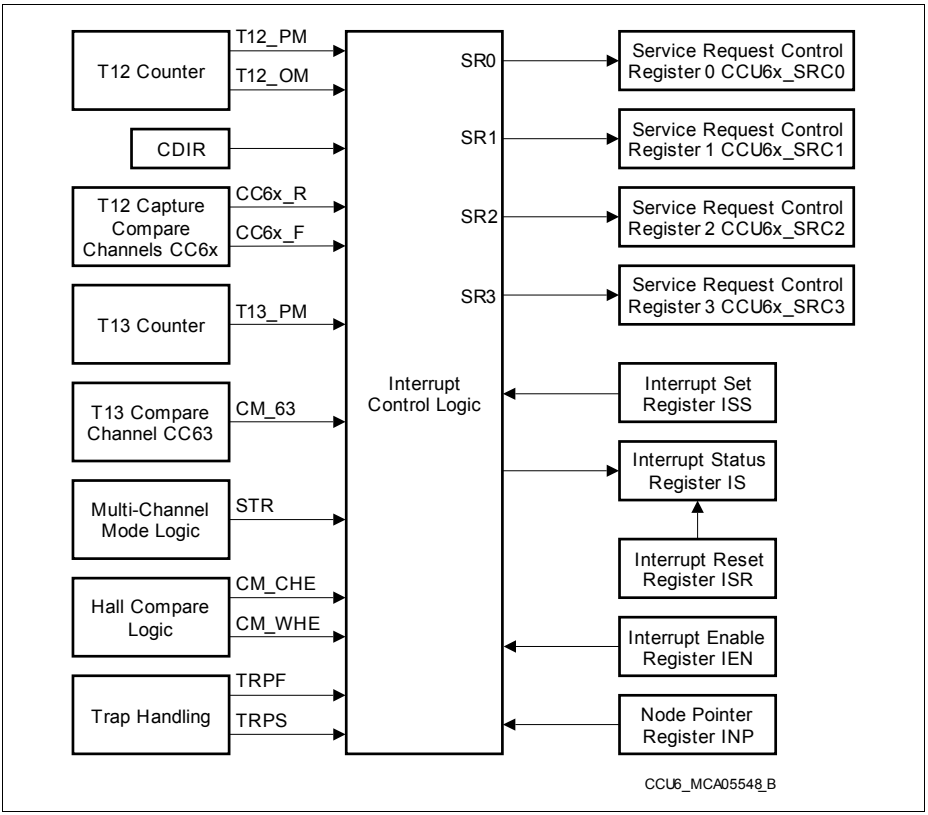


Figure 29-43 Interrupt Sources and Events

29.9.2 Interrupt Registers

29.9.2.1 Interrupt Status Register

Register IS contains the individual interrupt request bits. This register can only be read, write actions have no impact on the contents of this register. The SW can set or clear the bits individually by writing to the registers ISS (to set the bits) or to register ISR (to clear the bits).

The interrupt generation is independent from the value of the bits in register IS, e.g. the interrupt will be generated (if enabled) even if the corresponding bit is already set. The trigger for an interrupt generation is the detection of a set condition (by HW or SW) for the corresponding bit in register IS.

In compare mode (and hall mode), the timer-related interrupts are only generated while the timer is running (T1xR=1). In capture mode, the capture interrupts are also generated while the timer T12 is stopped.

Note: Not all bits in register IS can generate an interrupt. Other status bits have been added, that have a similar structure for their set and clear actions. It is recommended that SW checks the interrupt bits bit-wisely (instead of common OR over the bits).

IS
Interrupt Status Register **($A0_H$)** **Reset Value: $0000\ 0000_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
STR	IDLE	WHE	CHE	TRPS	TRPF	T13PM	T13CM	T12PM	T12OM	ICC62F	ICC62R	ICC61F	ICC61R	ICC60F	ICC60R
rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh	rh

Field	Bits	Type	Description
ICC60R, ICC61R, ICC62R	0, 2, 4	rh	**Capture, Compare-Match Rising Edge Flag** This bit indicates that event CC6x_R has been detected. This event occurs in compare mode when a compare-match is detected while T12 is counting up (CM_6x and CDIR = 0) and in capture mode when a rising edge is detected at the related input CC6xIN. 0_B The event has not yet been detected. 1_B The event has been detected.
ICC60F, ICC61F, ICC62F	1, 3, 5	rh	**Capture, Compare-Match Falling Edge Flag** This bit indicates that event CC6x_F has been detected. This event occurs in compare mode when a compare-match is detected while T12 is counting down (CM_6x and CDIR = 1) and in capture mode when a falling edge is detected at the related input CC6xIN. 0_B The event has not yet been detected. 1_B The event has been detected.
T12OM	6	rh	**Timer T12 One-Match Flag** This bit indicates that a timer T12 one-match while counting down (T12_OM and CDIR = 1) has been detected. 0_B The event has not yet been detected. 1_B The event has been detected.
T12PM	7	rh	**Timer T12 Period-Match Flag** This bit indicates that a timer T12 period-match while counting up (T12_PM and CDIR = 0) has been detected. 0_B The event has not yet been detected. 1_B The event has been detected.
T13CM	8	rh	**Timer T13 Compare-Match Flag** This bit indicates that a timer T13 compare-match (CM_63) has been detected. 0_B The event has not yet been detected. 1_B The event has been detected.
T13PM	9	rh	**Timer T13 Period-Match Flag** This bit indicates that a timer T13 period-match (T13_PM) has been detected. 0_B The event has not yet been detected. 1_B The event has been detected.

Field	Bits	Type	Description
TRPF	10	rh	**Trap Flag** This bit indicates if a trap condition (input $\overline{\text{CTRAP}}$ = 0 or by SW) is / has been detected. If TRPM2= 0, it becomes cleared automatically if $\overline{\text{CTRAP}}$ = 1 or TRPPEN = 0, whereas if TRPM2 = 1, it has to be cleared by writing RTRPF = 1. 0_B The trap condition has not been detected. 1_B The trap condition is / has been detected.
TRPS	11	rh	**Trap State**[1)] This bit indicates the actual trap state. It is set if TRPF = 1 and becomes cleared according to the mode selected in register TRPCTR. 0_B The trap state is not active. 1_B The trap state is active.
CHE	12	rh	**Correct Hall Event** This bit indicates that a correct Hall event (CM_CHE) has been detected. 0_B The event has not yet been detected. 1_B The event has been detected.
WHE	13	rh	**Wrong Hall Event** This bit indicates that a wrong Hall event (CM_WHE) has been detected. 0_B The event has not yet been detected. 1_B The event has been detected.
IDLE	14	rh	**IDLE State** If enabled by ENIDLE = 1, this bit is set together with bit WHE and it has to be cleared by SW. 0_B No action. 1_B Bit field MCMP is cleared, the selected outputs are set to passive state.
STR	15	rh	**Multi-Channel Mode Shadow Transfer Request** This bit indicates that a shadow transfer from MCMPS to MCMP (MCM_ST) has taken place. 0_B The event has not yet been detected. 1_B The event has been detected.
0	[31:16]	r	**Reserved;** Returns 0 if read; should be written with 0.

1) During the trap state, the selected outputs are set to the passive state. The logic level driven during the passive state is defined by the corresponding bit in register PSLR. Bits TRPS=1 and TRPF=0 can occur if the trap condition is no longer active but the selected synchronization has not yet taken place.

29.9.2.2 Interrupt Status Set Register

Register ISS contains individual interrupt request set bits to generate a CCU6 interrupt request by software. Writing a 1 sets the bit(s) in register IS at the corresponding bit position(s) and can generate an interrupt event (if available and enabled).
All bit positions read as 0.

ISS
Interrupt Status Set Register **($A4_H$)** **Reset Value: 0000 0000$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
S STR	S IDLE	S WHE	S CHE	S WHC	S TRPF	S T13PM	S T13CM	S T12PM	S T12OM	S CC62F	S CC62R	S CC61F	S CC61R	S CC60F	S CC60R
w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w

Field	Bits	Type	Description
SCC60R, SCC61R, SCC62R	0, 2, 4	w	**Set Capture, Compare-Match Rising Edge Flag** 0_B No action 1_B Bit CC6xR will be set.
SCC60F, SCC61F, SCC62F	1, 3, 5	w	**Set Capture, Compare-Match Falling Edge Flag** 0_B No action 1_B Bit CC6xF will be set.
ST12OM	6	w	**Set Timer T12 One-Match Flag** 0_B No action 1_B Bit T12OM will be set.
ST12PM	7	w	**Set Timer T12 Period-Match Flag** 0_B No action 1_B Bit T12PM will be set.
ST13CM	8	w	**Set Timer T13 Compare-Match Flag** 0_B No action 1_B Bit T13CM will be set.

Field	Bits	Type	Description
ST13PM	9	w	**Set Timer T13 Period-Match Flag** 0_B No action 1_B Bit T13PM will be set.
STRPF	10	w	**Set Trap Flag** 0_B No action 1_B Bits TRPF and TRPS will be set.
SWHC	11	w	**Software Hall Compare** 0_B No action 1_B The Hall compare action is triggered.
SCHE	12	w	**Set Correct Hall Event Flag** 0_B No action 1_B Bit CHE will be set.
SWHE	13	w	**Set Wrong Hall Event Flag** 0_B No action 1_B Bit WHE will be set.
SIDLE	14	w	**Set IDLE Flag** 0_B No action 1_B Bit IDLE will be set.
SSTR	15	w	**Set STR Flag** 0_B No action 1_B Bit STR will be set.
0	[31:16]	r	**Reserved;** Returns 0 if read; should be written with 0.

29.9.2.3 Status Reset Register

Register ISR contains bits to individually clear the interrupt event flags by software. Writing a 1 clears the bit(s) in register IS at the corresponding bit position(s).
All bit positions read as 0.

ISR
Interrupt Status Reset Register **($A8_H$)** **Reset Value: $0000\ 0000_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
R STR	R IDLE	R WHE	R CHE	0	R TRPF	R T13PM	R T13CM	R T12PM	R T12OM	R CC62F	R CC62R	R CC61F	R CC61R	R CC60F	R CC60R
w	w	w	w	r	w	w	w	w	w	w	w	w	w	w	w

Field	Bits	Type	Description
RCC60R, RCC61R, RCC62R	0, 2, 4	w	**Reset Capture, Compare-Match Rising Edge Flag** 0_B No action 1_B Bit CC6xR will be cleared.
RCC60F, RCC61F, RCC62F	1, 3, 5	w	**Reset Capture, Compare-Match Falling Edge Flag** 0_B No action 1_B Bit CC6xF will be cleared.
RT12OM	6	w	**Reset Timer T12 One-Match Flag** 0_B No action 1_B Bit T12OM will be cleared.
RT12PM	7	w	**Reset Timer T12 Period-Match Flag** 0_B No action 1_B Bit T12PM IS will be cleared.
RT13CM	8	w	**Reset Timer T13 Compare-Match Flag** 0_B No action 1_B Bit T13CM will be cleared.
RT13PM	9	w	**Reset Timer T13 Period-Match Flag** 0_B No action 1_B Bit T13PM will be cleared.

Field	Bits	Type	Description
RTRPF	10	w	**Reset Trap Flag** 0_B No action 1_B Bit TRPF will be cleared (not taken into account while input $\overline{\text{CTRAP}}$=0 and TRPPEN=1.
RCHE	12	w	**Reset Correct Hall Event Flag** 0_B No action 1_B Bit CHE will be cleared.
RWHE	13	w	**Reset Wrong Hall Event Flag** 1_B No action 0_B Bit WHE will be cleared.
RIDLE	14	w	**Reset IDLE Flag** 0_B No action 1_B Bit IDLE will be cleared.
RSTR	15	w	**Reset STR Flag** 0_B No action 1_B Bit STR will be cleared.
0	11, [31:16]	r	**Reserved;** Returns 0 if read; should be written with 0.

29.9.2.4 Interrupt Enable Register

Register IEN contains the interrupt enable bits and a control bit to enable the automatic idle function in the case of a wrong hall pattern.

IEN
Interrupt Enable Register **($B0_H$)** **Reset Value: 0000 0000$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ENSTR	ENIDLE	ENWHE	ENCHE	0	ENTRPF	ENT13PM	ENT13CM	ENT12PM	ENT12OM	ENCC62F	ENCC62R	ENCC61F	ENCC61R	ENCC60F	ENCC60R
rw	rw	rw	rw	r	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
ENCC60R, ENCC61R, ENCC62R	0, 2, 4	rw	**Capture, Compare-Match Rising Edge Interrupt Enable for Channel CC6x** 0_B No interrupt will be generated if the set condition for bit CC6xR in register IS occurs. 1_B An interrupt will be generated if the set condition for bit CC6xR in register IS occurs. The service request output that will be activated is selected by bit field INPCC6x.
ENCC60F, ENCC61F, ENCC62F	1, 3, 5	rw	**Capture, Compare-Match Falling Edge Interrupt Enable for Channel CC6x** 0_B No interrupt will be generated if the set condition for bit CC6xF in register IS occurs. 1_B An interrupt will be generated if the set condition for bit CC6xF in register IS occurs. The service request output that will be activated is selected by bit field INPCC6x.

Field	Bits	Type	Description
ENT12OM	6	rw	**Enable Interrupt for T12 One-Match** 0_B No interrupt will be generated if the set condition for bit T12OM in register IS occurs. 1_B An interrupt will be generated if the set condition for bit T12OM in register IS occurs. The service request output that will be activated is selected by bit field INPT12.
ENT12PM	7	rw	**Enable Interrupt for T12 Period-Match** 0_B No interrupt will be generated if the set condition for bit T12PM in register IS occurs. 1_B An interrupt will be generated if the set condition for bit T12PM in register IS occurs. The service request output that will be activated is selected by bit field INPT12.
ENT13CM	8	rw	**Enable Interrupt for T13 Compare-Match** 0_B No interrupt will be generated if the set condition for bit T13CM in register IS occurs. 1_B An interrupt will be generated if the set condition for bit T13CM in register IS occurs. The service request output that will be activated is selected by bit field INPT13.
ENT13PM	9	rw	**Enable Interrupt for T13 Period-Match** 0_B No interrupt will be generated if the set condition for bit T13PM in register IS occurs. 1_B An interrupt will be generated if the set condition for bit T13PM in register IS occurs. The service request output that will be activated is selected by bit field INPT13.
ENTRPF	10	rw	**Enable Interrupt for Trap Flag** 0_B No interrupt will be generated if the set condition for bit TRPF in register IS occurs. 1_B An interrupt will be generated if the set condition for bit TRPF in register IS occurs. The service request output that will be activated is selected by bit field INPERR.

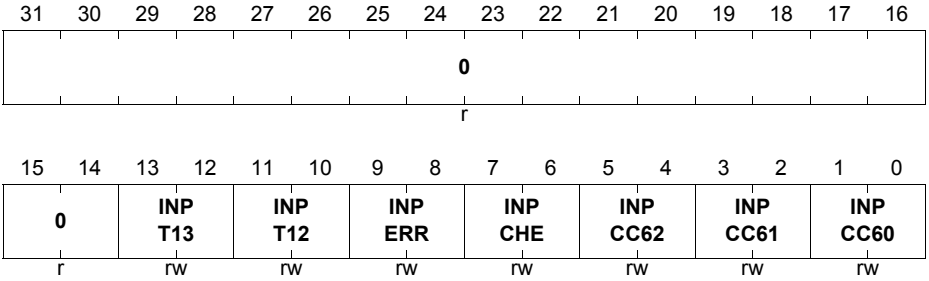
Field	Bits	Type	Description
ENCHE	12	rw	**Enable Interrupt for Correct Hall Event** 0_B No interrupt will be generated if the set condition for bit CHE in register IS occurs. 1_B An interrupt will be generated if the set condition for bit CHE in register IS occurs. The service request output that will be activated is selected by bit field INPCHE.
ENWHE	13	rw	**Enable Interrupt for Wrong Hall Event** 0_B No interrupt will be generated if the set condition for bit WHE in register IS occurs. 1_B An interrupt will be generated if the set condition for bit WHE in register IS occurs. The service request output that will be activated is selected by bit field INPERR.
ENIDLE	14	rw	**Enable Idle** This bit enables the automatic entering of the idle state (bit IDLE will be set) after a wrong hall event has been detected (bit WHE is set). During the idle state, the bit field MCMP is automatically cleared. 0_B The bit IDLE is not automatically set when a wrong hall event is detected. 1_B The bit IDLE is automatically set when a wrong hall event is detected.
ENSTR	15	rw	**Enable Multi-Channel Mode Shadow Transfer Interrupt** 0_B No interrupt will be generated if the set condition for bit STR in register IS occurs. 1_B An interrupt will be generated if the set condition for bit STR in register IS occurs. The service request output that will be activated is selected by bit field INPCHE.
0	11, [31:16]	r	**Reserved;** Returns 0 if read; should be written with 0.

29.9.2.5 Interrupt Node Pointer Register

Register INP contains the interrupt node pointers allowing a flexible interrupt handling. These bit fields define which service request output will be activated if the corresponding interrupt event occurs and the interrupt generation for this event is enabled.

INP

Interrupt Node Pointer Register **(AC_H)** **Reset Value: 0000 3940$_H$**



Field	Bits	Type	Description
INPCC60, INPCC61, INPCC62	[1:0], [3:2], [5:4]	rw	**Interrupt Node Pointer for Channel CC6x Interrupts** This bit field defines the service request output activated due to a set condition for bit CC6xR (if enabled by bit ENCC6xR) or for bit CC6xF (if enabled by bit ENCC6xF). 00_B Service request output SR0 is selected. 01_B Service request output SR1 is selected. 10_B Service request output SR2 is selected. 11_B Service request output SR3 is selected.
INPCHE	[7:6]	rw	**Interrupt Node Pointer for the CHE Interrupt** This bit field defines the service request output activated due to a set condition for bit CHE (if enabled by bit ENCHE) of for bit STR (if enabled by bit ENSTR). Coding see INPCC6x.
INPERR	[9:8]	rw	**Interrupt Node Pointer for Error Interrupts** This bit field defines the service request output activated due to a set condition for bit TRPF (if enabled by bit ENTRPF) or for bit WHE (if enabled by bit ENWHE). Coding see INPCC6x.
INPT12	[11:10]	rw	**Interrupt Node Pointer for Timer12 Interrupts** This bit field defines the service request output activated due to a set condition for bit T12OM (if enabled by bit ENT12OM) or for bit T12PM (if enabled by bit ENT12PM). Coding see INPCC6x.

Field	Bits	Type	Description
INPT13	[13:12]	rw	**Interrupt Node Pointer for Timer13 Interrupt** This bit field defines the service request output activated due to a set condition for bit T13CM (if enabled by bit ENT13CM) or for bit T13PM (if enabled by bit ENT13PM). Coding see INPCC6x.
0	[31:14]	r	**Reserved;** Returns 0 if read; should be written with 0.

29.9.3 Service Request Control Registers

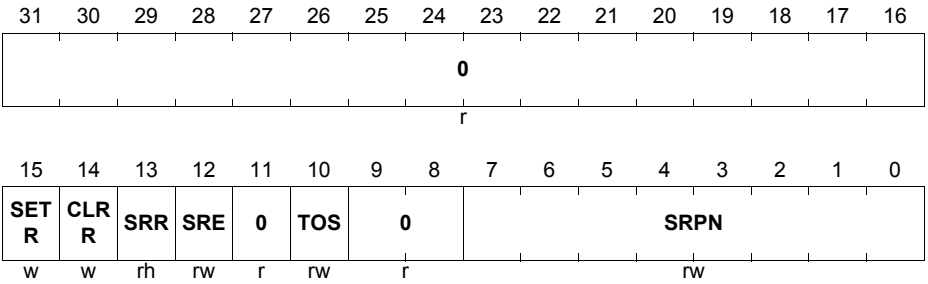
Each CC6x kernel has four service request outputs which are connected to four Service Request Nodes (SRN). Each SRN contains a Service Request Control Register.

CCU60_SRCx (x = 0-3)
CCU60 Service Request Control Register
(FC_H-x*4) **Reset Value: 0000 0000_H**

CCU61_SRCx (x = 0-3)
CCU61 Service Request Control Register
(FC_H-x*4) **Reset Value: 0000 0000_H**

CCU62_SRCx (x = 0-3)
CCU62 Service Request Control Register
(FC_H-x*4) **Reset Value: 0000 0000_H**

CCU63_SRCx (x = 0-3)
CCU63 Service Request Control Register
(FC_H-x*4) **Reset Value: 0000 0000_H**



Field	Bits	Type	Description
SRPN	[7:0]	rw	**Service Request Priority Number**
TOS	10	rw	**Type of Service Control**
SRE	12	rw	**Service Request Enable**
SRR	13	rh	**Service Request Flag**
CLRR	14	w	**Request Clear Bit**
SETR	15	w	**Request Set Bit**
0	[9:8], 11, [31:16]	r	**Reserved** Read as 0; should be written with 0.

29.10 General Module Operation

This section provides information about the:

- Configuration of the behavior of the different device operating modes (see mode control description in **Section 29.10.1**)
- Input selection (see **Section 29.10.2**)
- General register description (see **Section 29.10.4**)

29.10.1 Mode Control

The mode control concept for system control tasks, such as power saving, or suspend request for debugging, allows to program the module behavior under different device operating conditions. The behavior of a CCU6 kernel can be programmed for each of the device operating modes, that are requested by the global state control part of the SCU. Therefore, a CCU6 module provides a kernel state configuration register **KSCFG** defining the behavior in the following device operating modes:

- **Normal operation:**
  This operating mode is the default operating mode when neither a suspend request nor a clock-off request are pending. The module clock is not switched off and the CCU6 registers can be read or written. The kernel behavior is defined by KSCFG.NOMCFG.
- **Suspend mode:**
  This operating mode is requested when a suspend request (issued by a debugger through OCDS) is pending in the device. The module clock is not switched off and the CCU6 registers can be read or written. The kernel behavior is defined by KSCFG.SUMCFG.
- **Clock-off mode:**
  This operating mode is requested for power saving purposes. The module clock is switched off automatically when all kernels of the CCU6 module reached their specified state in a stop mode. In this case, CCU6 registers can not be accessed. The kernel behavior is defined by KSCFG.COMCFG. The clock-off mode is requested by a sleep request of the FPI bus.

The kernel distinguishes four different blocks (T12, T13, Hall logic, and trap logic). These blocks can be individually enabled for the request of stop mode 0 and stop mode 1 by the sensitivity bits **KSCSR**.SBx. If the request sensitivity is disabled, the block continues normal operation. If the request sensitivity is enabled, the block operates as specified for the selected stop mode.
The complete CCU6 acknowledge is given to the GSC when all four blocks have reached their defined end condition.

Table 29-12 CCU6 Functional Blocks

Block	Function	Sensitivity Bit
0	**Timer T12:** A functional enable is delivered until the specified stop condition is reached. Then, T12 stops counting and the CC6xIN input stages are frozen.	KSCSR.SB0
1	**Timer T13:** A functional enable is delivered until the specified stop condition is reached. Then, T13 stops counting.	KSCSR.SB1
2	**Hall Logic:** The hall logic is stopped immediately and the CCPOSx input stages are frozen.	KSCSR.SB2
3	**Trap Logic:** The trap logic is stopped immediately and the CTRAP input stage is frozen.	KSCSR.SB3

The behavior of the CCU6 kernel can be programmed for each of the device operating modes (normal operation and suspend mode). Therefore, it supports four kernel modes, as shown in **Table 29-13**.

Table 29-13 CCU6 Kernel Behavior

Kernel Mode	Kernel Behavior	Code
run mode 0	kernel operation as specified, no impact on CCU6 operation (same behavior for run mode 0 and run mode 1)	00_B
run mode 1		01_B

Table 29-13 CCU6 Kernel Behavior (cont'd)

Kernel Mode	Kernel Behavior	Code
stop mode 0	The sensitivity bits are taken into account for: **T12 block**: Timer T12 continues normal operation (if running) until they reach the end of the PWM period and then it stops (same stop condition as in single shot mode). When the timer stops, the CC6xIN inputs are frozen. **T13 block**: Timer T13 continues normal operation (if running) until they reach the end of the PWM period and then it stops (same stop condition as in single shot mode). **Hall logic block**: The CCPOSx input values are frozen. **Trap logic block**: The CTRAP input value is frozen.	10_B
stop mode 1	The output lines enabled for the trap condition are set to their passive values (similar to a trap state). The sensitivity bits are taken into account for: **T12 block**: Timer T12 stops immediately and CC6xIN inputs are frozen. **T13 block**: Timer T13 stops. **Hall logic block**: The CCPOSx input values are frozen. **Trap logic block**: The CTRAP input value is frozen.	11_B

Generally, bit field KSCFG.NOMCFG should be configured for run mode 0 as default setting for standard operation. If a CCU6 kernel should not react to a suspend request (and to continue operation as in normal mode), bit field KSCFG.SUMCFG has to be configured with the same value as KSCFG.NOMCFG. If a CCU6 kernel should show a different behavior and stop operation when a specific stop condition is reached, the code for stop mode 0 or stop mode 1 has to be written to KSCFG.SUMCFG.
A similar mechanism applies for the clock-off mode with the possibility to program the desired behavior by bit field KSCFG.COMCFG.

Note: The stop mode selection strongly depends on the application needs and it is very unlikely that different stop modes are required in parallel in the same application. As a result, only one stop mode type (either 0 or 1) should be used in the bit fields in register KSCFG. Do not mix stop mode 0 and stop mode 1 and avoid transitions from stop mode 0 to stop mode 1 (or vice versa) for the CCU6 module.

If the module clock is disabled by KSCFG.MODEN = 0 or in clock-off mode when the stop condition is reached (in stop mode 0 or 1), the module can not be accessed by read or write operations (except register KSCFG and KSCSR that can always be accessed). As a consequence, it can not be configured.
Please note that bit KSCFG.MODEN should only be set by SW while all configuration fields are configured for run mode 0.

29.10.2 Input Selection

Each CCU6 input signal can be selected from a vector of four or eight possible inputs by programming the port input select registers **PISEL0** and **PISEL2**. This permits to adapt the pin functionality of the device to the application requirements.
The output pins for the module output signals are chosen in the ports.

Naming convention:
The input vector CC60IN[D:A] for input signal CC60IN is composed of the signals CC60INA to CC60IND.

Note: All functional inputs of the CCU6 are synchronized to f_{CC6} before they affect the module internal logic. The resulting delay of $2/f_{CC6}$ and for asynchronous signals an additional uncertainty of $1/f_{CC6}$ have to be taken into account for precise timing calculation. An edge of an input signal can only be correctly detected if the high phase and the low phase of the input signal are both longer than $1/f_{CC6}$.

29.10.3 Input Monitoring

A selected event which occurs at each CCU6 input signal can be monitored through **IMON**.x. Every input signal can be included for the detection of a lost bit event (**IMON**.LBE) if enabled through its individual lost indicator enable bits (**LI**.yEN). The lost bit event occurs if a selected event occurs again with the previous event captured (IMON.x remains set) and its lost indicator is enabled for at least one of the monitored input signals. The lost bit event can be enabled (**LI**.LBEEN) for an interrupt to be generated at one of the SRx line, selected through **LI**.INPLBE. The LBE output signal of the kernel can be connected to a capture input to indicate when does the lost bit event happens. See **Section 29.12**.

The lost bit event can be used as a kind of interrupt or event watchdog to monitor if an action related to an event has been processed before a second event of the same type occurs. Like this, if a certain event is treated by an interrupt that should be monitored, the related indication flag has to be cleared by SW. If the SW has not yet cleared the flag and the event occurs again, the event is considered as being lost and another interrupt can be generated to inform the system about the loss. This can be also used to indicate that input events occur too often and the main task has not enough time to treat them.

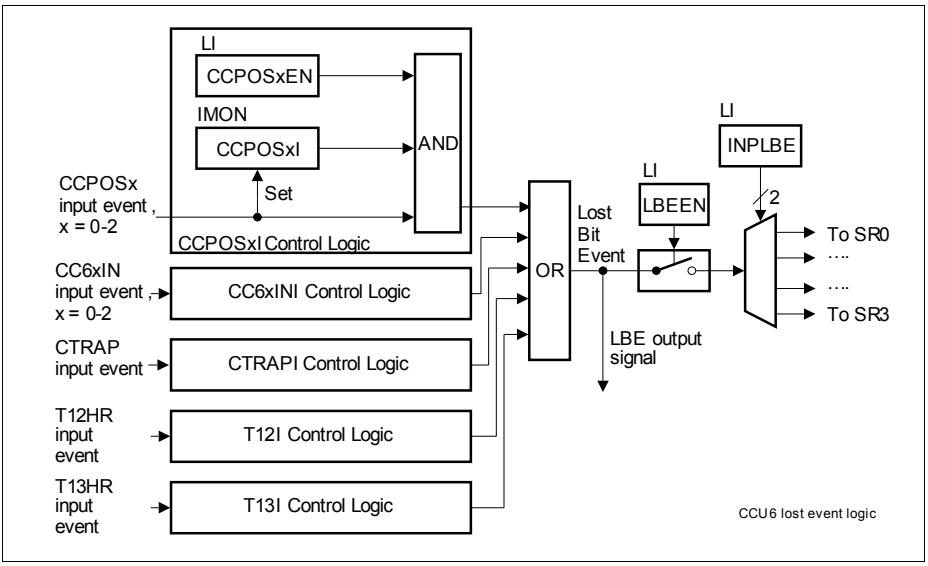


Figure 29-44 Lost Event Logic

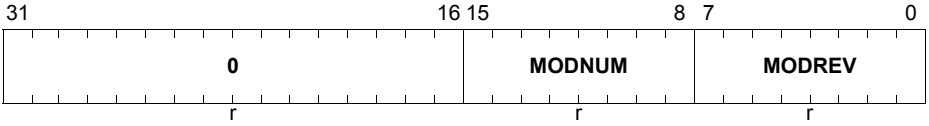
29.10.4 General Registers

29.10.4.1 ID Register

Reset value of the first version of ID register in TC1387 is 0000 5408$_H$.

The CCU6 Module Identification Register ID contains read-only information about the module identification number and its revision.

ID
Module Identification Register **(08_H)** **Reset Value: 0000 54XX$_H$**

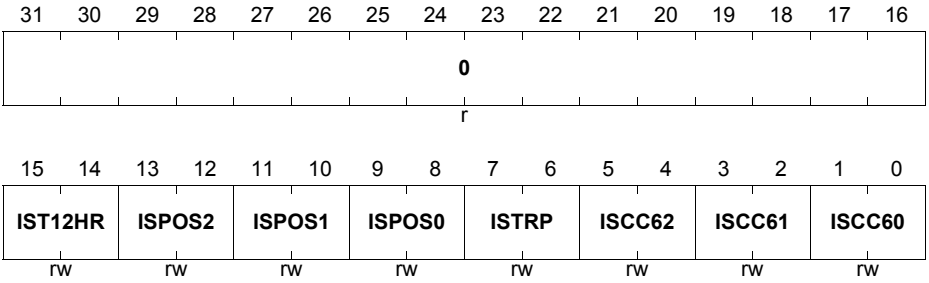


Field	Bits	Type	Description
MODREV	[7:0]	r	**Module Revision Number** MOD_REV defines the module revision number. The value of a module revision starts with 01_H (first revision), 02_H, 03_H, ... up to FF_H.
MODNUM	[15:8]	r	**Module Number Value** This bit field defines the module identification number for the CCU6: 54_H
0	[31:16]	r	**Reserved** Read as 0.

29.10.4.2 Port Input Select Registers

Registers PISEL0 and PISEL2 contain bit fields selecting the actual input signal for the module inputs.

PISEL0
Port Input Select Register 0 **(10_H)** **Reset Value: 0000 0000_H**



Field	Bits	Type	Description
ISCC60	[1:0]	rw	**Input Select for CC60** This bit field defines the input signal used as CC60 capture input. 00_B The signal CC60INA is selected. 01_B The signal CC60INB is selected. 10_B The signal CC60INC is selected. 11_B The signal CC60IND is selected.
ISCC61	[3:2]	rw	**Input Select for CC61** This bit field defines the input signal used as CC61 capture input. 00_B The signal CC61INA is selected. 01_B The signal CC61INB is selected. 10_B The signal CC61INC is selected. 11_B The signal CC61IND is selected.
ISCC62	[5:4]	rw	**Input Select for CC62** This bit field defines the input signal used as CC62 capture input. 00_B The signal CC62INA is selected. 01_B The signal CC62INB is selected. 10_B The signal CC62INC is selected. 11_B The signal CC62IND is selected.

Field	Bits	Type	Description
ISTRP	[7:6]	rw	**Input Select for CTRAP** This bit field defines the input signal used as CTRAP input. 00_B The signal CTRAPA is selected. 01_B The signal CTRAPB is selected. 10_B The signal CTRAPC is selected. 11_B The signal CTRAPD is selected.
ISPOS0	[9:8]	rw	**Input Select for CCPOS0** This bit field defines the input signal used as CCPOS0 input. 00_B The signal CCPOS0A is selected. 01_B The signal CCPOS0B is selected. 10_B The signal CCPOS0C is selected. 11_B The signal CCPOS0D is selected.
ISPOS1	[11:10]	rw	**Input Select for CCPOS1** This bit field defines the input signal used as CCPOS1 input. 00_B The signal CCPOS1A is selected. 01_B The signal CCPOS1B is selected. 10_B The signal CCPOS1C is selected. 11_B The signal CCPOS1D is selected.
ISPOS2	[13:12]	rw	**Input Select for CCPOS2** This bit field defines the input signal used as CCPOS2 input. 00_B The signal CCPOS2A is selected. 01_B The signal CCPOS2B is selected. 10_B The signal CCPOS2C is selected. 11_B The signal CCPOS2D is selected.

Field	Bits	Type	Description
IST12HR	[15:14]	rw	**Input Select for T12HR** This bit field defines the input signal used as T12HR input. 00_B Either signal T12HRA (if T12EXT = 0) or T12HRE (if T12EXT = 1) is selected. 01_B Either signal T12HRB (if T12EXT = 0) or T12HRF (if T12EXT = 1) is selected. 10_B Either signal T12HRC (if T12EXT = 0) or T12HRG (if T12EXT = 1) is selected. 11_B Either signal T12HRD (if T12EXT = 0) or T12HRH (if T12EXT = 1) is selected.
0	[31:16]	r	**Reserved** Returns 0 if read, should be written with 0.

PISEL2

Port Input Select Register 2 **(14_H)** **Reset Value: 0000 0000_H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0								**T13 EXT**	**T12 EXT**	**ISCNT13**		**ISCNT12**		**IST13HR**	
r								rw	rw	rw		rw		rw	

Field	Bits	Type	Description
IST13HR	[1:0]	rw	**Input Select for T13HR** This bit field defines the input signal used as T13HR input. 00_B Either signal T13HRA (if T13EXT = 0) or T13HRE (if T13EXT = 1) is selected. 01_B Either signal T13HRB (if T13EXT = 0) or T13HRF (if T13EXT = 1) is selected. 10_B Either signal T13HRC (if T13EXT = 0) or T13HRG (if T13EXT = 1) is selected. 11_B Either signal T13HRD (if T13EXT = 0) or T13HRH (if T13EXT = 1) is selected.
ISCNT12	[3:2]	rw	**Input Select for T12 Counting Input** This bit field defines the input event leading to a counting action of T12. 00_B The T12 prescaler generates the counting events. Bit TCTR4.T12CNT is not taken into account. 01_B Bit TCTR4.T12CNT written with 1 is a counting event. The T12 prescaler is not taken into account. 10_B The timer T12 is counting each rising edge detected in the selected T12HR signal. 11_B The timer T12 is counting each falling edge detected in the selected T12HR signal.
ISCNT13	[5:4]	rw	**Input Select for T13 Counting Input** This bit field defines the input event leading to a counting action of T13. 00_B The T13 prescaler generates the counting events. Bit TCTR4.T13CNT is not taken into account. 01_B Bit TCTR4.T13CNT written with 1 is a counting event. The T13 prescaler is not taken into account. 10_B The timer T13 is counting each rising edge detected in the selected T13HR signal. 11_B The timer T13 is counting each falling edge detected in the selected T13HR signal.
T12EXT	6	rw	**Extension for T12HR Inputs** This bit extends the 2-bit field IST12HR. 0_B One of the signals T12HR[D:A] is selected. 1_B One of the signals T12HR[H:E] is selected.

Field	Bits	Type	Description
T13EXT	7	rw	**Extension for T13HR Inputs** This bit extends the 2-bit field IST13HR. 0_B One of the signals T13HR[D:A] is selected. 1_B One of the signals T13HR[H:E] is selected.
0	[31:8]	r	**Reserved;** Returns 0 if read; should be written with 0.

29.10.4.3 Kernel State Configuration Register

The kernel state configuration register KSCFG allows the selection of the desired kernel modes for the different device operating modes.
Bit fields KSCFG.NOMCFG and KSCFG.COMCFG are reset by an application (class 3) reset. Bit field KSCFG.SUMCFG is reset by a debug (class 1) reset.

*Note: The coding of the bit fields NOMCFG, SUMCFG and COMCFG are described in **Table 29-13**.*

KSCFG
Kernel State Configuration Register

(18_H) **Reset Value: 0000 0000$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BP COM	0	COMCFG		BP SUM	0	SUMCFG		BP NOM	0	NOMCFG		SUS REQ	ACK	BP MOD EN	MOD EN
w	r	rw		w	r	rw		w	r	rw		rh	rh	w	rw

Field	Bits	Type	Description
MODEN	0	rw	**Module Enable** This bit enables the module kernel clock and the module functionality. 0_B The module is switched off immediately (without respecting a stop condition). It does not react on mode control actions and the module clock is switched off. The module does not react on read accesses and ignores write accesses (except to KSCFG). 1_B The module is switched on and can operate. After writing 1 to MODEN, it is recommended to read register KSCFG to avoid pipeline effects in the control block before accessing other CCU6 registers.
BPMODEN	1	w	**Bit Protection for MODEN** This bit enables the write access to the bit MODEN. It always reads 0. 0_B MODEN is not changed. 1_B MODEN is updated with the written value.
ACK	2	rh	**Module Acknowledge** This bit monitors the state of the CCU6 module's acknowledge on incoming requests. 0_B The acknowledge is not activated, because at least one of the module kernels is in a transition phase. 1_B The acknowledge is activated, because all module kernels have reached the requested state.
SUSREQ	3	rh	**Suspend Request** This bit monitors the state of the CCU6 module's suspend request input, requested through OCDS. The value is only valid when there is no sleep request. In the event that there is a sleep request, the value is ignored and COMCFG is considered as the kernel mode. 0_B A suspend mode is not requested and bit field NOMCFG defines the CCU6 kernel mode. 1_B A suspend mode is requested and bit field SUMCFG defines the CCU6 kernel mode.

Field	Bits	Type	Description
NOMCFG	[5:4]	rw	**Normal Operation Mode Configuration** This bit field defines the kernel mode applied in normal operation mode. 00_B Run mode 0 is selected. 01_B Run mode 1 is selected. 10_B Stop mode 0 is selected. 11_B Stop mode 1 is selected.
BPNOM	7	w	**Bit Protection for NOMCFG** This bit enables the write access to the bit field NOMCFG. It always reads 0. 0_B NOMCFG is not changed. 1_B NOMCFG is updated with the written value.
SUMCFG	[9:8]	rw	**Suspend Mode Configuration** This bit field defines the kernel mode applied in suspend mode. Coding like NOMCFG.
BPSUM	11	w	**Bit Protection for SUMCFG** This bit enables the write access to the bit field SUMCFG. It always reads 0. 0_B SUMCFG is not changed. 1_B SUMCFG is updated with the written value.
COMCFG	[13:12]	rw	**Clock Off Mode Configuration** This bit field defines the kernel mode applied in clock-off mode. Coding like NOMCFG.
BPCOM	15	w	**Bit Protection for COMCFG** This bit enables the write access to the bit field COMCFG. It always reads 0. 0_B COMCFG is not changed. 1_B COMCFG is updated with the written value.
0	6, 10, 14, [31:16]	r	**Reserved** Returns 0 if read; should be written with 0.

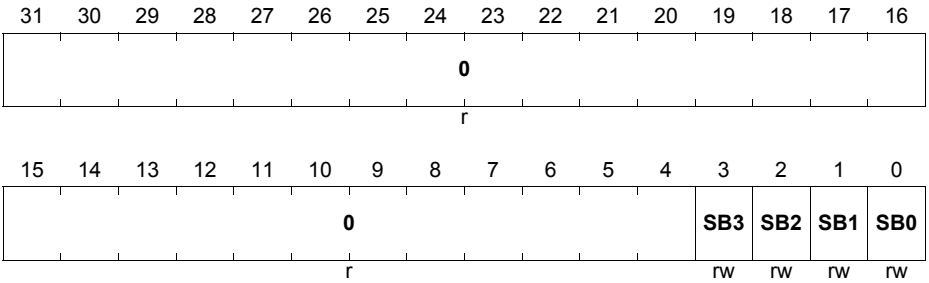
Note: The bit protection bits BPxxx allow partly modification of the configuration bits with a single write operation (without the need of a read-modify-write mechanism handled by the CPU).

29.10.4.4 Kernel State Sensitivity Control Register

The kernel state control sensitivity register bits define which internal block is effected by stop modes 0 and 1.

KSCSR
Kernel State Control Sensitivity Register

($1C_H$) **Reset Value: $0000\ 0000_H$**

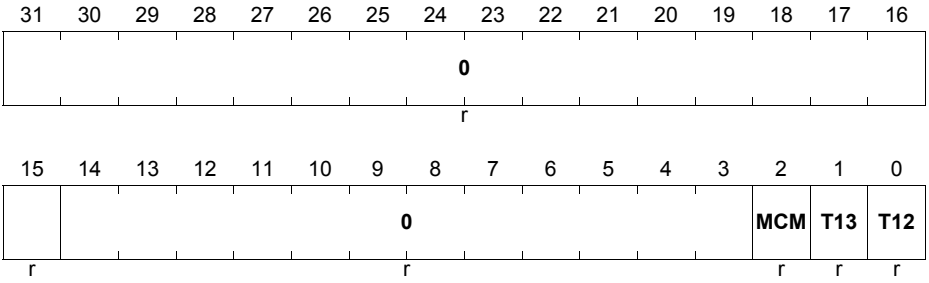


Field	Bits	Type	Description
SB0, **SB1,** **SB2,** **SB3**	0, 1, 2, 3	rw	**Sensitivity Block x** This bit defines if block x of the CCU6 kernel is sensitive to stop mode 0 or stop mode 1. The functional definition of the blocks is given in **Table 29-12**. 0_B Block x is not sensitive to stop mode 0 or stop mode 1 and behaves like in run mode 0. It continues normal operation without respecting the defined stop condition. 1_B Block x is sensitive to stop mode 0 or stop mode 1. It is respecting the defined stop condition.
0	[31:4]	r	**Reserved;** Returns 0 if read; should be written with 0.

29.10.4.5 Module Configuration Register

The module configuration register contains bits describing the functionality that is available in the CCU6 module.

MCFG
Module Configuration Register (04_H) Reset Value: 0000 0007_H



Field	Bits	Type	Description
T12	0	r	**T12 Available** This bit indicates if the T12 block is available. 0_B The T12 block is not available. A write access to T12PR is ignored. 1_B The T12 block is available. A write access to T12PR is executed.
T13	1	r	**T13 Available** This bit indicates if the T13 block is available. 0_B The T13 block is not available. A write access to T13PR is ignored. 1_B The T13 block is available. A write access to T13PR is executed.
MCM	2	r	**Multi-Channel Mode Available** This bit indicates if the multi-channel mode functionality is available. 0_B The multi-channel mode functionality is not available. A write access to MCMOUTS is ignored. 1_B The multi-channel mode functionality is available. A write access to MCMOUTS is executed.
0	[31:3]	r	**Reserved;** read as 0; should be written with 0.

Note: The MCFG register can be modified only if the signal which comes from the watchdog timer mechanism allows.

29.10.4.6 Input Monitoring Register

The input monitoring register monitors the occurence of a selected event for the input signals. If a hardware event triggers the setting of bit IMON.x and the same bit is written with 1 via software at the same time, then the corresponding bit is cleared (software overrules hardware). The lost bit event is indicated if an event is detected again at one or more input signals with its lost indicator enabled.

Note: The register is only applicable in capture modes if the edges are selected through T12MSEL.MSEL6x.

IMON
Input Monitoring Register **(98_H)** **Reset Value: 0000 0000$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0						T13HRI	T12HRI	CTRAPI	CC62INI	CC61INI	CC60INI	CCPOS2I	CCPOS1I	CCPOS0I	LBE
r						rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh

Field	Bits	Type	Description
LBE	0	rwh	**Lost Bit Event** This bit determines if a lost bit event has occured. A lost bit event occurs when a selected event occurs again with the previous event captured (IMON.x remains set) and its lost indicator is enabled, for at least one of the monitored input signals. The bit can be cleared by writing a 1 to the same bit position, while writing a 0 has no effect. 0_B The lost bit event has not occured. 1_B The lost bit event has occured.
CCPOSxI (x = 0 -2)	x + 1	rwh	**Event indication for input signal CCPOSx** The bit determines if the selected event has occured via an edge detection. The bit can be cleared by writing a 1 to the same bit position, while writing a 0 has no effect. 0_B A selected event has not occured. 1_B Edge detection indicates a selected event has occured. *Note: The dedicated edge is indicated for a selected event if Hysteretic-like Control or Capture modes are initialised in T12MSEL.MSEL6x. If these modes are not selected, then all edges will be indicated as an event for the inputs.*
CC6xINI (x = 0 -2)	x + 4	rwh	**Event indication for input signal CC6xIN** The bit determines if the selected event has occured via an edge detection. The bit can be cleared by writing a 1 to the same bit position, while writing a 0 has no effect. 0_B A selected event has not occured. 1_B Edge detection indicates a selected event has occured.
CTRAPI	7	rwh	**Event indication for input signal CTRAP** The bit determines if the selected event has occured via an edge detection. The bit can be cleared by writing a 1 to the same bit position, while writing a 0 has no effect. 0_B An event has not occured. 1_B Edge detection indicates an event has occured.

Field	Bits	Type	Description
T12HRI	8	rwh	**Event indication for input signal T12HR** The bit determines if the selected event has occured via an edge detection. The bit can be cleared by writing a 1 to the same bit position, while writing a 0 has no effect. 0_B An event has not occured. 1_B Edge detection indicates an event has occured.
T13HRI	9	rwh	**Event indication for input signal T13HR** The bit determines if the selected event has occured via an edge detection. The bit can be cleared by writing a 1 to the same bit position, while writing a 0 has no effect. 0_B An event has not occured. 1_B Edge detection indicates an event has occured.
0	[31:10]	r	**Reserved;** Returns 0 if read; should be written with 0.

29.10.4.7 Lost Indicator Register

The lost indicator register has the lost indicator enable bits for its detected event at the input signals. The lost bit event can then be enabled as an output signal through one of the service request lines.

LI

Lost Indicator Register **($9C_H$)** **Reset Value: $0000\ 0000_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INPLBE		LBEEN	0			T13HREN	T12HREN	CTRAPEN	CC62INEN	CC61INEN	CC60INEN	CCPOS2EN	CCPOS1EN	CCPOS0EN	0
rw		rw	r			rw	rw	rw	rw	rw	rw	rw	rw	rw	r

Field	Bits	Type	Description
CCPOSxEN (x = 0 -2)	x + 1	rw	**Lost Indicator Enable for input signal CCPOSx** This bit determines if the monitored event at the input signal is enabled for the detection of a lost bit event. 0_B Input signal is disabled for a lost bit event detection. 1_B Input signal is enabled for a lost bit event detection.
CC6xINEN (x = 0 -2)	x + 4	rw	**Lost Indicator Enable for input signal CC6xIN** This bit determines if the monitored event at the input signal is enabled for the detection of a lost bit event. 0_B Input signal is disabled for a lost bit event detection. 1_B Input signal is enabled for a lost bit event detection.

Field	Bits	Type	Description
CTRAPEN	7	rw	**Lost Indicator Enable for inputsignal CTRAP** This bit determines if the monitored event at the input signal is enabled for the detection of a lost bit event. 0_B Input signal is disabled for a lost bit event detection. 1_B Input signal is enabled for a lost bit event detection.
T12HREN	8	rw	**Lost Indicator Enable for input signal T12HR** This bit determines if the monitored event at the input signal is enabled for the detection of a lost bit event. 0_B Input signal is disabled for a lost bit event detection. 1_B Input signal is enabled for a lost bit event detection.
T13HREN	9	rw	**Lost Indicator Enable for input signal T13HR** This bit determines if the monitored event at the input signal is enabled for the detection of a lost bit event. 0_B Input signal is disabled for a lost bit event detection. 1_B Input signal is enabled for a lost bit event detection.
LBEEN	13	rw	**Interrupt Enable for Lost Bit Event** This bit determines if a SRx line is activated if lost bit event is detected. 0_B Lost bit event is disabled for the activation of a SRx line. 1_B Lost bit event is enabled for the activation of a SRx line.
INPLBE	[15:14]	rw	**Interrupt Node Pointer for lost bit event** This bit field defines which service request output line is selected to output an lost event alert for an enabled lost bit event. 00_B Service request output SR0 is selected. 01_B Service request output SR1 is selected. 10_B Service request output SR2 is selected. 11_B Service request output SR3 is selected.
0	0, [12:10], [31:16]	r	**Reserved;** Returns 0 if read; should be written with 0.

29.11 Implementation

This chapter describes the implementation of the CCU6 modules in the TC1798 device.

- Address map (see **Section 29.11.1**)
- Module output select (see **Section 29.11.2**)
- Synchronous start (see **Section 29.11.3**)
- Digital Connections (see **Section 29.12**)

29.11.1 Address Map

There are four CCU6 kernels in the TC1798, namely CCU60 to CCU63. The CCU6061 module consists of CCU60 and CCU61 kernels , while CCU6263 module consists of CCU62 and CCU63 kernels.

Table 29-14 Registers Address Space

Module	Base Address	End Address	Note
CCU60	F000 3000$_H$	F000 30FF$_H$	CCU6061 : consists of CCU60 and CCU61 kernels
CCU61	F000 3100$_H$	F000 31FF$_H$	CCU6061 : consists of CCU60 and CCU61 kernels
CCU62	F000 3200$_H$	F000 32FF$_H$	CCU6263 : consists of CCU62 and CCU63 kernels
CCU63	F000 3300$_H$	F000 33FF$_H$	CCU6263 : consists of CCU62 and CCU63 kernels

Table 29-15 Registers Overview - CCU6 Module Registers

Register Short Name	Register Long Name	Offset Addr.	Access Mode		Reset Value	Page
			Read	Write		
CCU6061 and CCU6263 Module Registers (only available in the address range of CCU60 and CCU62, respectively)						
CCU60_MOSEL	CCU60 Module Output Select Register	0C$_H$	U, SV	U, SV	0000 0000$_H$	29-136
CCU62_MOSEL	CCU62 Module Output Select Register	0C$_H$	U, SV	U, SV	0000 0000$_H$	29-138

29.11.1.1 Module Registers

Module Output Select Register

MOSEL contains bit fields to select the output signal from the CCU6061 or CCU6263 for the trigger signals to the ADCx modules.

CCU60_MOSEL
CCU60 Module Output Select Register($0C_H$) **Reset Value: $0000\ 0000_H$**

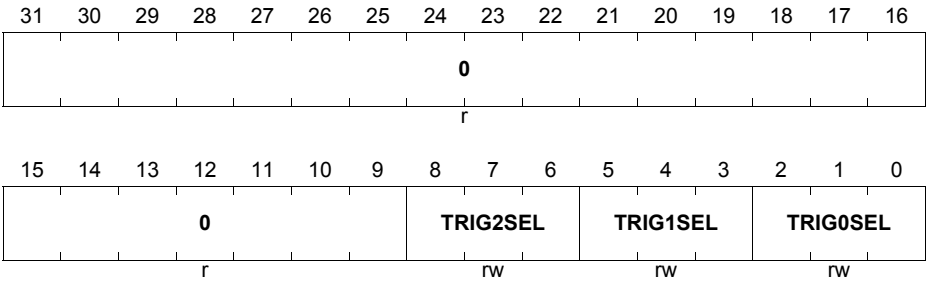
31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0							TRIG2SEL			TRIG1SEL			TRIG0SEL		
r							rw			rw			rw		

Field	Bits	Type	Description
TRIG0SEL	[2:0]	rw	**Output Trigger Select for CCU6061 TRIG0** This bit field defines the output signal from the module pair used as the trigger signal to ADCx inputs. 000_B The signal CCU60_COUT63 is selected. 001_B The signal CCU61_COUT63 is selected. 010_B The signal CCU60_CC60 is selected. 011_B The signal CCU61_CC60 is selected. 100_B The signal CCU60_SR1 is selected. 101_B The signal CCU61_SR1 is selected. 110_B The signal CCU60_SR3 is selected. 111_B The signal CCU61_SR3 is selected.
TRIG1SEL	[5:3]	rw	**Output Trigger Select for CCU6061 TRIG1** This bit field defines the output signal from the module pair used as the trigger signal to ADCx inputs. 000_B The signal CCU60_COUT63 is selected. 001_B The signal CCU61_COUT63 is selected. 010_B The signal CCU60_CC61 is selected. 011_B The signal CCU61_CC61 is selected. 100_B The signal CCU60_SR1 is selected. 101_B The signal CCU61_SR1 is selected. 110_B The signal CCU60_SR3 is selected. 111_B The signal CCU61_SR3 is selected.
TRIG2SEL	[8:6]	rw	**Output Trigger Select for CCU6061 TRIG2** This bit field defines the output signal from the module pair used as the trigger signal to ADCx inputs. 000_B The signal CCU60_COUT63 is selected. 001_B The signal CCU61_COUT63 is selected. 010_B The signal CCU60_CC62 is selected. 011_B The signal CCU61_CC62 is selected. 100_B The signal CCU60_SR1 is selected. 101_B The signal CCU61_SR1 is selected. 110_B The signal CCU60_SR3 is selected. 111_B The signal CCU61_SR3 is selected.
0	[31:9]	r	**Reserved** Returns 0 if read, should be written with 0.

CCU62_MOSEL

CCU62 Module Output Select Register($0C_H$) **Reset Value: $0000\ 0000_H$**



Field	Bits	Type	Description
TRIG0SEL	[2:0]	rw	**Output Trigger Select for CCU6263 TRIG0** This bit field defines the output signal from the module pair used as the trigger signal to ADCx inputs. 000_B The signal CCU62_COUT63 is selected. 001_B The signal CCU63_COUT63 is selected. 010_B The signal CCU62_CC60 is selected. 011_B The signal CCU63_CC60 is selected. 100_B The signal CCU62_SR1 is selected. 101_B The signal CCU63_SR1 is selected. 110_B The signal CCU62_SR3 is selected. 111_B The signal CCU63_SR3 is selected.
TRIG1SEL	[5:3]	rw	**Output Trigger Select for CCU6263 TRIG1** This bit field defines the output signal from the module pair used as the trigger signal to ADCx inputs. 000_B The signal CCU62_COUT63 is selected. 001_B The signal CCU63_COUT63 is selected. 010_B The signal CCU62_CC61 is selected. 011_B The signal CCU63_CC61 is selected. 100_B The signal CCU62_SR1 is selected. 101_B The signal CCU63_SR1 is selected. 110_B The signal CCU62_SR3 is selected. 111_B The signal CCU63_SR3 is selected.

Field	Bits	Type	Description
TRIG2SEL	[8:6]	rw	**Output Trigger Select for CCU6263 TRIG2** This bit field defines the output signal from the module pair used as the trigger signal to ADCx inputs. 000_B The signal CCU62_COUT63 is selected. 001_B The signal CCU63_COUT63 is selected. 010_B The signal CCU62_CC62 is selected. 011_B The signal CCU63_CC62 is selected. 100_B The signal CCU62_SR1 is selected. 101_B The signal CCU63_SR1 is selected. 110_B The signal CCU62_SR3 is selected. 111_B The signal CCU63_SR3 is selected.
0	[31:9]	r	**Reserved** Returns 0 if read, should be written with 0.

29.11.2 Module Output Select

For CCU6061 module, there are 3 trigger signals which are selectable from the output signals from CCU60 and CCU61 kernels. Similarly, CCU6263 module allows up to 3 output trigger signals from CCU62 and CCU63 kernels.

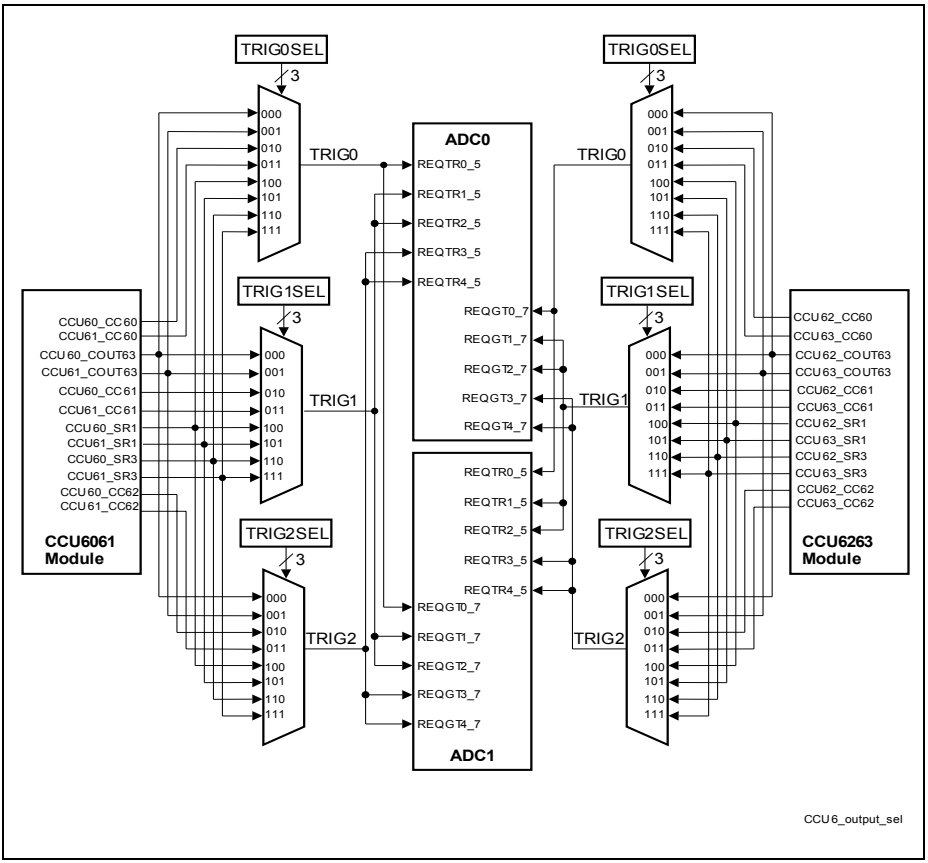


Figure 29-45 Output select trigger

29.11.3 Synchronous Start

Synchronous start of the capture/compare timers are supported by control bits SYSCON.CCTRIG0 and SYSCON.CCTRIG1 in the SCU module. Bit SYSCON.CCTRIG0 is connected to the T12HR and T13HR for CCU60 and CCU61 kernels while bit SYSCON.CCTRIG1 is connected to the T12HR and T13HR for CCU62 and CCU63 kernels.

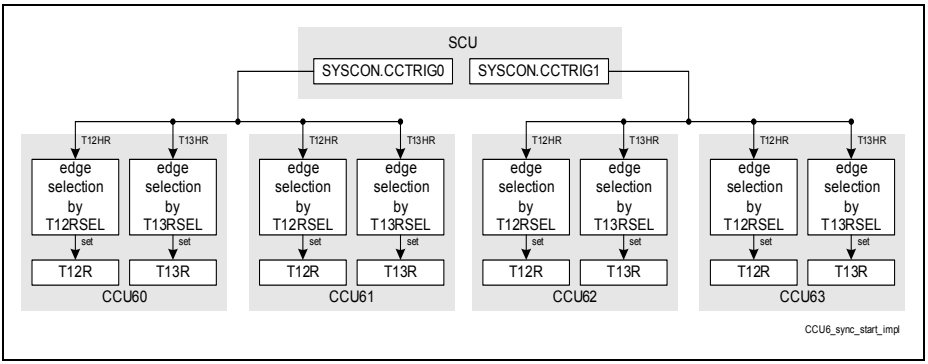


Figure 29-46 Synchronization Concept in TC1798

29.12 Digital Connections

The following tables show the digital connections of the CCU6x modules with other modules or pins in the TC1798 device.
Each input signal can be selected among 4 or 8 possible input lines, e.g. the input vector for input signal CC60IN is composed of CC60IN[D:A], whereas the input vectors for T12HR and T13HR are composed of T12HR[H:A] and T13HR[H:A]. The following sections refer to the interface signals.

Note: All functional inputs of the CCU6 are synchronized to f_{CC6} before they can affect the module internal logic. The resulting delay of $2/f_{CC6}$ and an uncertainty of $1/f_{CC6}$ have to be taken into account for precise timing calculation.
An edge of an input signal can only be correctly detected if both, the high phase and the low phase of the input signal are each longer than $1/f_{CC6}$.

29.12.1 Connections of CCU60

This table describes the module interconnections of CCU60.

Table 29-16 CCU60 Digital Connections in TC1798

Signal	from/to Module	I/O to CCU60	Can be used to/as
CC60INA	see port chapter	I	input signals for capture event on channel CC60
CC60INB	see port chapter	I	
CC60INC	see port chapter	I	
CC60IND	0	I	
CC61INA	see port chapter	I	input signals for capture event on channel CC61
CC61INB	see port chapter	I	
CC61INC	see port chapter	I	
CC61IND	0	I	

Table 29-16 CCU60 Digital Connections in TC1798 (cont'd)

Signal	from/to Module	I/O to CCU60	Can be used to/as
CC62INA	see port chapter	I	input signals for capture event on channel CC62
CC62INB	see port chapter	I	
CC62INC	0	I	
CC62IND	0	I	
CTRAPA	see port chapter	I	input signals for CTRAP
CTRAPB	see port chapter	I	
CTRAPC	CCU60_CTRAPA AND CCU60_CTRAPB	I	
CTRAPD	SCU_ERU_PDOUT 0	I	
CCPOS0A	see port chapter	I	input signals for CCPOS0
CCPOS0B	CCU61_SR2	I	
CCPOS0C	0	I	
CCPOS0D	0	I	edge detection off
CCPOS1A	see port chapter	I	input signals for CCPOS1
CCPOS1B	ADC_SR2	I	
CCPOS1C	0	I	
CCPOS1D	0	I	edge detection off

Table 29-16 CCU60 Digital Connections in TC1798 (cont'd)

Signal	from/to Module	I/O to CCU60	Can be used to/as
CCPOS2A	see port chapter	I	input signals for CCPOS2
CCPOS2B	0	I	
CCPOS2C	0	I	
CCPOS2D	0	I	edge detection off
T12HRA	CCTRIG0	I	input signals for T12HR
T12HRB	see port chapter	I	
T12HRC	see port chapter	I	
T12HRD	GPTA_TRIG00	I	
T12HRE	see port chapter	I	
T12HRF	GPT12_0_T6OFL	I	
T12HRG	CCU61_SR2	I	
T12HRH	0	I	
T13HRA	CCTRIG0	I	input signals for T13HR
T13HRB	see port chapter	I	
T13HRC	see port chapter	I	
T13HRD	GPTA_TRIG00	I	
T13HRE	see port chapter	I	
T13HRF	GPT12_0_T6OFL	I	
T13HRG	CCU61_SR2	I	
T13HRH	CCU60_SR1	I	

Table 29-16 CCU60 Digital Connections in TC1798 (cont'd)

Signal	from/to Module	I/O to CCU60	Can be used to/as
CC60	see port chapter	O	compare outputs of channel CC60
COUT60	see port chapter	O	
CC61	see port chapter	O	compare outputs of channel CC61
COUT61	see port chapter	O	
CC62	see port chapter	O	compare outputs of channel CC62
COUT62	see port chapter	O	
COUT63	see port chapter	O	compare output of channel CC63
LBE	CCU63_CC60IND	O	lost bit event output
T12_ZM	–	O	T12 zero match
T13_PM	–	O	T13 period match
MCM_ST	–	O	MCM shadow transfer
SR0	DMA CHm1_REQI13, m = 0, 1	O	DMA triggers
SR1	CCU60_T13HRH, ERU_OGU01	O	T13 count trigger, Output Gating Unit trigger
	ADC0_REQTRx_5, ADC1_REQGTx_7,x =0,1,2,3,4		ADC0 and ADC1 trigger capability, pls see **CCU60_MOSEL** for the respective trigger select to the request trigger/gating inputs of the ADC0/1.
SR2	CCU61_CCPOS0B, CCU61_T12HRG, CCU61_T13HRG	O	CCU61 triggers
SR3	ADC0_REQTRx_5, ADC1_REQGTx_7, x=0,1,2,3,4	O	ADC0 and ADC1 trigger capability, pls see **CCU60_MOSEL** for the respective trigger select to the request trigger/gating inputs of the ADC0/1.

29.12.2 Connections of CCU61

This table describes the module interconnections of CCU61.

Table 29-17 CCU61 Digital Connections in TC1798

Signal	from/to Module	I/O to CC61	Can be used to/as
CC60INA	see port chapter	I	input signals for capture event on channel CC60
CC60INB	see port chapter	I	
CC60INC	see port chapter	I	
CC60IND	CCU62_LBE	I	
CC61INA	see port chapter	I	input signals for capture event on channel CC61
CC61INB	see port chapter	I	
CC61INC	see port chapter	I	
CC61IND	CCU63_LBE	I	
CC62INA	see port chapter	I	input signals for capture event on channel CC62
CC62INB	see port chapter	I	
CC62INC	0	I	
CC62IND	GPT12_1_T6OFL	I	
CTRAPA	see port chapter	I	input signals for CTRAP
CTRAPB	see port chapter	I	
CTRAPC	CCU61_CTRAPA AND CCU61_CTRAPB	I	
CTRAPD	SCU_ERU_PDOUT1	I	

Table 29-17 CCU61 Digital Connections in TC1798 (cont'd)

Signal	from/to Module	I/O to CC61	Can be used to/as
CCPOS0A	see port chapter	I	input signals for CCPOS0
CCPOS0B	CCU60_SR2	I	
CCPOS0C	0	I	
CCPOS0D	0	I	edge detection off
CCPOS1A	see port chapter	I	input signals for CCPOS1
CCPOS1B	ADC_SR2	I	
CCPOS1C	0	I	edge detection off
CCPOS1D	0	I	
CCPOS2A	see port chapter	I	input signals for CCPOS2
CCPOS2B	0	I	
CCPOS2C	0	I	
CCPOS2D	0	I	edge detection off
T12HRA	CCTRIG0	I	input signals for T12HR
T12HRB	see port chapter	I	
T12HRC	see port chapter	I	
T12HRD	GPTA_TRIG00	I	
T12HRE	see port chapter	I	
T12HRF	GPT12_0_T6OFL	I	
T12HRG	CCU60_SR2	I	
T12HRH	0	I	

Table 29-17 CCU61 Digital Connections in TC1798 (cont'd)

Signal	from/to Module	I/O to CC61	Can be used to/as
T13HRA	CCTRIG0	I	input signals for T13HR
T13HRB	see port chapter	I	
T13HRC	see port chapter	I	
T13HRD	GPTA_TRIG00	I	
T13HRE	see port chapter	I	
T13HRF	GPT12_0_T6OFL	I	
T13HRG	CCU60_SR2	I	
T13HRH	CCU61_SR1	I	
CC60	see port chapter	O	compare outputs of channel CC60
COUT60	see port chapter	O	
CC61	see port chapter	O	compare outputs of channel CC61
COUT61	see port chapter	O	
CC62	see port chapter	O	compare outputs of channel CC62
COUT62	see port chapter	O	
COUT63	see port chapter	O	compare output of channel CC63
LBE	CCU63_CC61IND	O	lost bit event output
T12_ZM	–	O	T12 zero match
T13_PM	–	O	T13 period match
MCM_ST	–	O	MCM shadow transfer
SR0	DMA CHm5_REQI13, m = 0, 1	O	DMA triggers

Table 29-17 CCU61 Digital Connections in TC1798 (cont'd)

Signal	from/to Module	I/O to CC61	Can be used to/as
SR1	CCU61_T13HRH, ERU_OGU11	O	T13 count trigger, Output Gating Unit trigger
	ADC0_REQTRx_5, ADC1_REQGTx_7,x =0,1,2,3,4		ADC0 and ADC1 trigger capability, pls see **CCU60_MOSEL** for the respective trigger select to the request trigger/gating inputs of the ADC0/1.
SR2	CCU60_CCPOS0B, CCU60_T12HRG, CCU60_T13HRG	O	CCU60 triggers
SR3	ADC0_REQTRx_5, ADC1_REQGTx_7, x=0,1,2,3,4	O	ADC0 and ADC1 trigger capability, pls see **CCU60_MOSEL** for the respective trigger select to the request trigger/gating inputs of the ADC0/1.

29.12.3 Connections of CCU62

This table describes the module interconnections of CCU62.

Table 29-18 CCU62 Digital Connections in TC1798

Signal	from/to Module	I/O to CCU62	Can be used to/as
CC60INA	see port chapter	I	input signals for capture event on channel CC60
CC60INB	see port chapter	I	
CC60INC	see port chapter	I	
CC60IND	0	I	
CC61INA	see port chapter	I	input signals for capture event on channel CC61
CC61INB	see port chapter	I	
CC61INC	see port chapter	I	
CC61IND	0	I	
CC62INA	see port chapter	I	input signals for capture event on channel CC62
CC62INB	see port chapter	I	
CC62INC	0	I	
CC62IND	0	I	
CTRAPA	see port chapter	I	input signals for CTRAP
CTRAPB	see port chapter	I	
CTRAPC	CCU62_CTRAPA AND CCU62_CTRAPB	I	
CTRAPD	SCU_ERU_PDOUT2	I	

Table 29-18 CCU62 Digital Connections in TC1798 (cont'd)

Signal	from/to Module	I/O to CCU62	Can be used to/as
CCPOS0A	see port chapter	I	input signals for CCPOS0
CCPOS0B	CCU63_SR2	I	
CCPOS0C	0	I	
CCPOS0D	0	I	edge detection off
CCPOS1A	see port chapter	I	input signals for CCPOS1
CCPOS1B	ADC_SR2	I	
CCPOS1C	0	I	
CCPOS1D	0	I	edge detection off
CCPOS2A	see port chapter	I	input signals for CCPOS2
CCPOS2B	0	I	
CCPOS2C	0	I	
CCPOS2D	0	I	edge detection off
T12HRA	CCTRIG1	I	input signals for T12HR
T12HRB	see port chapter	I	
T12HRC	see port chapter	I	
T12HRD	GPTA_TRIG02	I	
T12HRE	see port chapter	I	
T12HRF	GPT12_1_T6OFL	I	
T12HRG	CCU63_SR2	I	
T12HRH	0	I	

Table 29-18 CCU62 Digital Connections in TC1798 (cont'd)

Signal	from/to Module	I/O to CCU62	Can be used to/as
T13HRA	CCTRIG1	I	input signals for T13HR
T13HRB	see port chapter	I	
T13HRC	see port chapter	I	
T13HRD	GPTA_TRIG02	I	
T13HRE	see port chapter	I	
T13HRF	GPT12_1_T6OFL	I	
T13HRG	CCU63_SR2	I	
T13HRH	CCU62_SR1	I	
CC60	see port chapter	O	compare outputs of channel CC60
COUT60	see port chapter	O	
CC61	see port chapter	O	compare outputs of channel CC61
COUT61	see port chapter	O	
CC62	see port chapter	O	compare outputs of channel CC62
COUT62	see port chapter	O	
COUT63	see port chapter	O	compare output of channel CC63
LBE	CCU61_CC60IND	O	lost bit event output
T12_ZM	–	O	T12 zero match
T13_PM	–	O	T13 period match
MCM_ST	–	O	MCM shadow transfer
SR0	DMA CHm6_REQI13, m = 0, 1 CCU62_T13HRH	O	DMA triggers

Table 29-18 CCU62 Digital Connections in TC1798 (cont'd)

Signal	from/to Module	I/O to CCU62	Can be used to/as
SR1	CCU62_T13HRH, ERU_OGU21	O	T13 count trigger, Output Gating Unit trigger
	ADC0_REQGTx_7, ADC1_REQTRx_5,x =0,1,2,3,4		ADC0 and ADC1 trigger capability, pls see **CCU62_MOSEL** for the respective trigger select to the request trigger/gating inputs of the ADC0/1.
SR2	CCU63_CCPOS0B, CCU63_T12HRG, CCU63_T13HRG	O	CCU63 triggers
SR3	ADC0_REQGTx_7, ADC1_REQTRx_5, x=0,1,2,3,4	O	ADC0 and ADC1 trigger capability, pls see **CCU62_MOSEL** for the respective trigger select to the request trigger/gating inputs of the ADC0/1.

29.12.4 Connections of CCU63

This table describes the module interconnections of CCU63.

Table 29-19 CCU63 Digital Connections in TC1798

Signal	from/to Module	I/O to CC63	Can be used to/as
CC60INA	see port chapter	I	input signals for capture event on channel CC60
CC60INB	see port chapter	I	
CC60INC	see port chapter	I	
CC60IND	CCU60_LBE	I	
CC61INA	see port chapter	I	input signals for capture event on channel CC61
CC61INB	see port chapter	I	
CC61INC	see port chapter	I	
CC61IND	CCU61_LBE	I	
CC62INA	see port chapter	I	input signals for capture event on channel CC62
CC62INB	see port chapter	I	
CC62INC	0	I	
CC62IND	GPT12_0_T6OFL	I	
CTRAPA	see port chapter	I	input signals for CTRAP
CTRAPB	see port chapter	I	
CTRAPC	CCU63_CTRAPA AND CCU63_CTRAPB	I	
CTRAPD	SCU_ERU_PDOUT3	I	

Table 29-19 CCU63 Digital Connections in TC1798 (cont'd)

Signal	from/to Module	I/O to CC63	Can be used to/as
CCPOS0A	see port chapter	I	input signals for CCPOS0
CCPOS0B	CCU62_SR2	I	
CCPOS0C	0	I	
CCPOS0D	0	I	edge detection off
CCPOS1A	see port chapter	I	input signals for CCPOS1
CCPOS1B	ADC_SR2	I	
CCPOS1C	0	I	
CCPOS1D	0	I	edge detection off
CCPOS2A	see port chapter	I	input signals for CCPOS2
CCPOS2B	0	I	
CCPOS2C	0	I	
CCPOS2D	0	I	edge detection off
T12HRA	CCTRIG1	I	input signals for T12HR
T12HRB	see port chapter	I	
T12HRC	see port chapter	I	
T12HRD	GPTA_TRIG02	I	
T12HRE	see port chapter4	I	
T12HRF	GPT12_1_T6OFL	I	
T12HRG	CCU62_SR2	I	
T12HRH	0	I	

Table 29-19 CCU63 Digital Connections in TC1798 (cont'd)

Signal	from/to Module	I/O to CC63	Can be used to/as
T13HRA	CCTRIG1	I	input signals for T13HR
T13HRB	see port chapter	I	
T13HRC	see port chapter	I	
T13HRD	GPTA_TRIG02	I	
T13HRE	see port chapter	I	
T13HRF	GPT12_1_T6OFL	I	
T13HRG	CCU62_SR2	I	
T13HRH	CCU63_SR1	I	
CC60	see port chapter	O	compare outputs of channel CC60
COUT60	see port chapter	O	
CC61	see port chapter	O	compare outputs of channel CC61
COUT61	see port chapter	O	
CC62	see port chapter	O	compare outputs of channel CC62
COUT62	see port chapter	O	
COUT63	see port chapter	O	compare output of channel CC63
LBE	CCU61_CC61IND	O	lost bit event output
T12_ZM	–	O	T12 zero match
T13_PM	–	O	T13 period match
MCM_ST	–	O	MCM shadow transfer
SR0	DMA CHm7_REQI13, m = 0, 1 CCU63_T13HRH	O	DMA triggers

Table 29-19 CCU63 Digital Connections in TC1798 (cont'd)

Signal	from/to Module	I/O to CC63	Can be used to/as
SR1	CCU63_T13HRH, ERU_OGU31	O	T13 count trigger, Output Gating Unit trigger
	ADC0_REQGTx_7, ADC1_REQTRx_5,x =0,1,2,3,4		ADC0 and ADC1 trigger capability, pls see **CCU62_MOSEL** for the respective trigger select to the request trigger/gating inputs of the ADC0/1.
SR2	CCU62_CCPOS0B, CCU62_T12HRG, CCU62_T13HRG	O	CCU62 triggers
SR3	ADC0_REQGTx_7, ADC1_REQTRx_5, x=0,1,2,3,4	O	ADC0 and ADC1 trigger capability, pls see **CCU62_MOSEL** for the respective trigger select to the request trigger/gating inputs of the ADC0/1.

30 The General Purpose Timer 12 (GPT12)

The General Purpose Timer 12 consist out of the blocks GPT1 and GPT2, that have a very flexible multifunctional timer structures which may be used for timing, event counting, pulse width measurement, pulse generation, frequency multiplication, and other purposes. They incorporate five 16-bit timers that are grouped into the two timer blocks GPT1 and GPT2. Each timer in each block may operate independently in a number of different modes such as Gated Timer or Counter Mode, or may be concatenated with another timer of the same block. Each block has alternate input/output functions and specific interrupts associated with it.

Note: Input signals can be selected from several sources by register PISEL.

Block GPT1 contains three timers/counters: The core timer T3 and the two auxiliary timers T2 and T4. The maximum resolution is $f_{GPT}/4$. The auxiliary timers of GPT1 may optionally be configured as reload or capture registers for the core timer. These registers are listed in **Section 30.1.6**.

- $f_{GPT}/4$ maximum resolution
- 3 independent timers/counters
- Timers/counters can be concatenated
- 4 operating modes:
  - Timer Mode
  - Gated Timer Mode
  - Counter Mode
  - Incremental Interface Mode
- Reload and Capture functionality
- Separate interrupts

Block GPT2 contains two timers/counters: The core timer T6 and the auxiliary timer T5. The maximum resolution is $f_{GPT}/2$. An additional Capture/Reload register (CAPREL) supports capture and reload operation with extended functionality. These registers are listed in **Section 30.2.7**.

The following list summarizes the features which are supported:

- $f_{GPT}/2$ maximum resolution
- 2 independent timers/counters
- Timers/counters can be concatenated
- 3 operating modes:
  - Timer Mode
  - Gated Timer Mode
  - Counter Mode
- Extended capture/reload functions via 16-bit capture/reload register CAPREL
- Separate interrupts

30.1 Timer Block GPT1

All three timers of block GPT1 (T2, T3, T4) can run in one of 4 basic modes: Timer Mode, Gated Timer Mode, Counter Mode, or Incremental Interface Mode. All timers can count up or down. Each timer of GPT1 is controlled by a separate control register TxCON.

Each timer has an input pin TxIN (alternate pin function) associated with it, which serves as the gate control in Gated Timer Mode, or as the count input in Counter Mode. The count direction (up/down) may be programmed via software or may be dynamically altered by a signal at the External Up/Down control input TxEUD (alternate pin function). An overflow/underflow of core timer T3 is indicated by the Output Toggle Latch T3OTL, whose state may be output on the associated pin T3OUT (alternate pin function). The auxiliary timers T2 and T4 may additionally be concatenated with the core timer T3 (through T3OTL) or may be used as capture or reload registers for the core timer T3.

The current contents of each timer can be read or modified by the CPU by accessing the corresponding timer count registers T2, T3, or T4. When any of the timer registers is written to by the CPU in the state immediately preceding a timer increment, decrement, reload, or capture operation, the CPU write operation has priority in order to guarantee correct results.

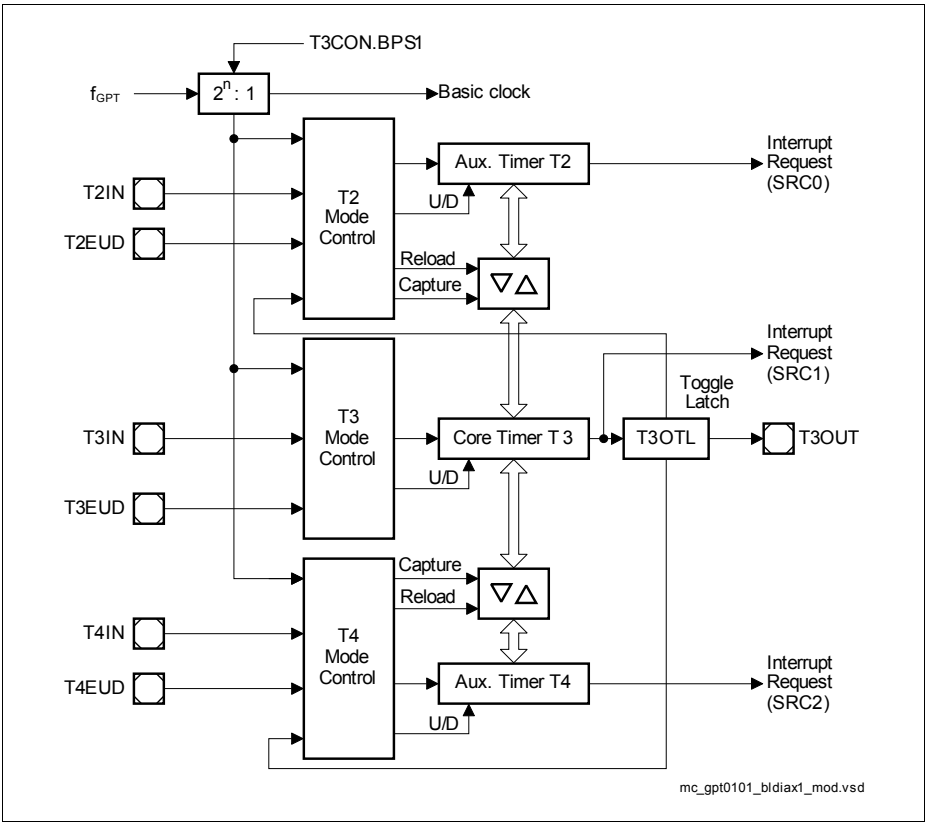


Figure 30-1 GPT1 Block Diagram

Note: The GPT1 block uses a finite state machine to control the actions. Since multiple interactions are possible between the timers (T2, T3, T4), these elements are processed sequentially. However, all actions are normally completed within one basic clock cycle. The GPT1 state machine has 8 states (4 states when BPS1 = 01_B) and processes the timers in the order T3 - T2 (all actions except capture) - T4 - T2 (capture).

30.1.1 GPT1 Core Timer T3 Control

The current contents of the core timer T3 are reflected by its count register T3. This register can also be written to by the CPU, for example, to set the initial start value.

T3CON
Timer 3 Control Register **(14_H)** **Reset Value: 0000 0000_H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
T3 R DIR	T3 CH DIR	T3E DGE	BPS1		T3 OTL	T3 OE	T3 UDE	T3 UD	T3 R	T3M			T3I		
rh	rwh	rwh	rw		rwh	rw	rw	rw	rw	rw			rw		

Field	Bits	Type	Description
T3I	[2:0]	rw	**Timer T3 Input Parameter Selection** Depends on the operating mode, see respective sections for encoding: **Table 30-8** for Timer Mode and Gated Timer Mode **Table 30-2** for Counter Mode **Table 30-3** for Incremental Interface Mode
T3M	[5:3]	rw	**Timer 3 Mode Control** 000_B Timer Mode 001_B Counter Mode 010_B Gated Timer Mode with gate active low 011_B Gated Timer Mode with gate active high 100_B Reserved. Do not use this combination 101_B Reserved. Do not use this combination 110_B Incremental Interface Mode (Rotation Detection Mode) 111_B Incremental Interface Mode (Edge Detection Mode)
T3R	6	rw	**Timer 3 Run Bit** 0_B Timer 3 stops 1_B Timer runs

Field	Bits	Type	Description
T3UD	7	rw	**Timer T3 Up/Down Control**[1)] 0_B Timer T3 counts up 1_B Timer T3 counts down
T3UDE	8	rw	**Timer T3 External Up/Down Enable**[1)] 0_B Input T3EUD is disconnected 1_B Direction influenced by input T3EUD
T3OE	9	rw	**Overflow/Underflow Output Enable** 0_B Alternate Output Function Disabled 1_B State of T3 toggle latch is output on pin T3OUT
T3OTL	10	rwh	**Timer T3 Overflow Toggle Latch** Toggles on each overflow/underflow of T3. Can be set or cleared by software (see separate description)
BPS1	[12:11]	rw	**GPT1 Block Prescaler Control** Selects the basic clock for block GPT1 (see also **Section 30.1.5**) 00_B $f_{GPT}/8$ 01_B $f_{GPT}/4$ 10_B $f_{GPT}/32$ 11_B $f_{GPT}/16$
T3EDGE	13	rwh	**Timer T3 Edge Detection Flag** The bit is set each time a count edge is detected. T3EDGE must be cleared by software. 0_B No count edge was detected 1_B A count edge was detected
T3CHDIR	14	rwh	**Timer T3 Count Direction Change Flag** This bit is set each time the count direction of timer T3 changes. T3CHDIR must be cleared by software. 0_B No change of count direction was detected 1_B A change of count direction was detected
T3RDIR	15	rh	**Timer T3 Rotation Direction Flag** 0_B Timer T3 counts up 1_B Timer T3 counts down
0	[31:16]	r	**Reserved** Read as 0; should be written with 0.

1) See **Table 30-1** for encoding of bits T3UD and T3UDE.

Timer T3 Run Control

The core timer T3 can be started or stopped by software through bit T3R (Timer T3 Run Bit). This bit is relevant in all operating modes of T3. Setting bit T3R will start the timer, clearing bit T3R stops the timer.

In Gated Timer Mode, the timer will only run if T3R = 1 and the gate is active (high or low, as programmed).

Note: When bit T2RC or T4RC in timer control register T2CON or T4CON is set, bit T3R will also control (start and stop) the auxiliary timer(s) T2 and/or T4.

Count Direction Control

The count direction of the GPT1 timers (core timer and auxiliary timers) can be controlled either by software or by the external input pin TxEUD (Timer Tx External Up/Down Control Input). These options are selected by bits TxUD and TxUDE in the respective control register TxCON. When the up/down control is provided by software (bit TxUDE = 0), the count direction can be altered by setting or clearing bit TxUD. When bit TxUDE = 1, pin TxEUD is selected to be the controlling source of the count direction. However, bit TxUD can still be used to reverse the actual count direction, as shown in **Table 30-1**. The count direction can be changed regardless of whether or not the timer is running.

Note: When pin TxEUD is used as external count direction control input, it must be configured as input (its corresponding direction control bit must be cleared).

Table 30-1 GPT1 Timer Count Direction Control

Pin TxEUD	Bit TxUDE	Bit TxUD	Count Direction	Bit TxRDIR
X	0	0	Count Up	0
X	0	1	Count Down	1
0	1	0	Count Up	0
1	1	0	Count Down	1
0	1	1	Count Down	1
1	1	1	Count Up	0

Timer 3 Output Toggle Latch

The overflow/underflow signal of timer T3 is connected to a block named ‘Toggle Latch’, shown in the timer mode diagrams. **Figure 30-2** illustrates the details of this block. An overflow or underflow of T3 will clock two latches: The first latch represents bit T3OTL in control register T3CON. The second latch is an internal latch toggled by T3OTL’s output. Both latch outputs are connected to the input control blocks of the auxiliary timers T2 and T4. The output level of the shadow latch will match the output level of T3OTL, but is delayed by one clock cycle. When the T3OTL value changes, this will result in a temporarily different output level from T3OTL and the shadow latch, which can trigger the selected count event in T2 and/or T4.

When software writes to T3OTL, both latches are set or cleared simultaneously. In this case, both signals to the auxiliary timers carry the same level and no edge will be detected. Bit T3OE (overflow/underflow output enable) in register T3CON enables the state of T3OTL to be monitored via an external pin T3OUT. When T3OTL is linked to an external port pin (must be configured as output), T3OUT can be used to control external HW. If T3OE = 1, pin T3OUT outputs the state of T3OTL. If T3OE = 0, pin T3OUT outputs a high level (as long as the T3OUT alternate function is selected for the port pin).

The trigger signals can serve as an input for the counter function or as a trigger source for the reload function of the auxiliary timers T2 and T4.

As can be seen from **Figure 30-2**, when latch T3OTL is modified by software to determine the state of the output line, also the internal shadow latch is set or cleared accordingly. Therefore, no trigger condition is detected by T2/T4 in this case.

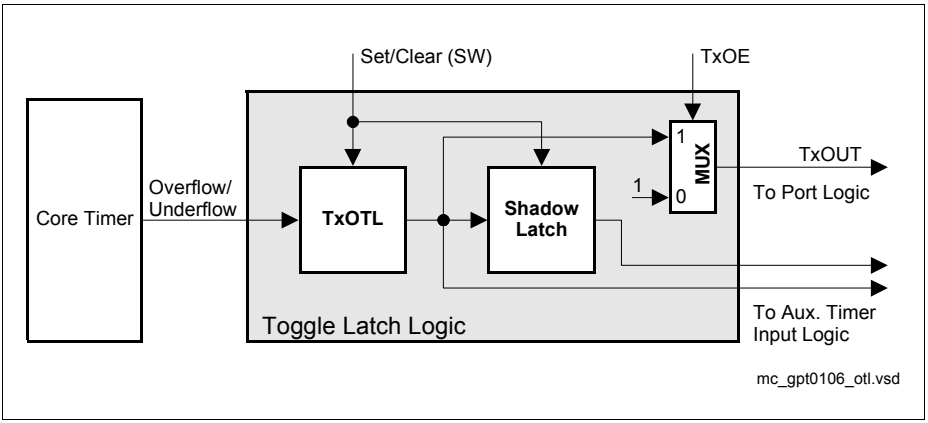


Figure 30-2 Block Diagram of the Toggle Latch Logic of Core Timer T3

30.1.2 GPT1 Core Timer T3 Operating Modes

Timer T3 can operate in one of several modes.

Timer 3 in Timer Mode

Timer Mode for the core timer T3 is selected by setting bitfield T3M in register T3CON to 000_B. In Timer Mode, T3 is clocked with the module's input clock f_{GPT} divided by two programmable prescalers controlled by bitfields BPS1 and T3I in register T3CON. Please see **Section 30.1.5** for details on the input clock options.

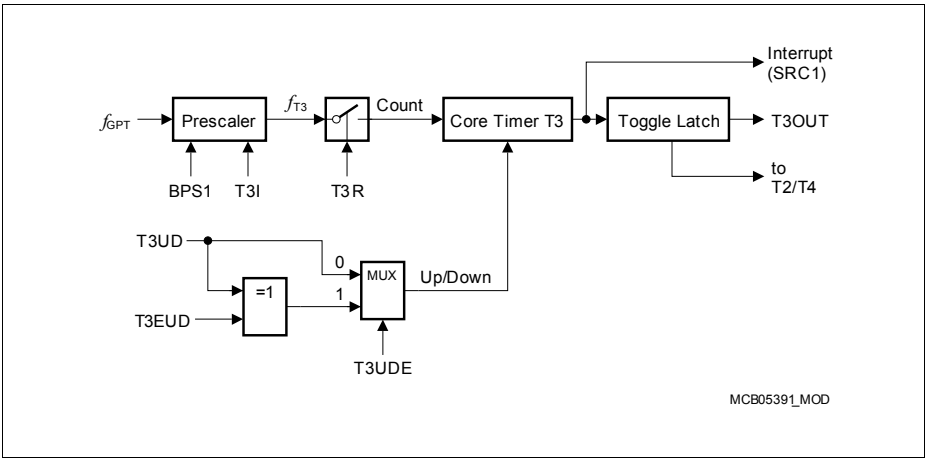


Figure 30-3 Block Diagram of Core Timer T3 in Timer Mode

Gated Timer Mode

Gated Timer Mode for the core timer T3 is selected by setting bitfield T3M in register T3CON to 010_B or 011_B. Bit T3M.0 (T3CON.3) selects the active level of the gate input. The same options for the input frequency are available in Gated Timer Mode as in Timer Mode (see **Section 30.1.5**). However, the input clock to the timer in this mode is gated by the external input pin T3IN (Timer T3 External Input).
To enable this operation, the associated pin T3IN must be configured as input, that is, the corresponding direction control bit must contain 0.

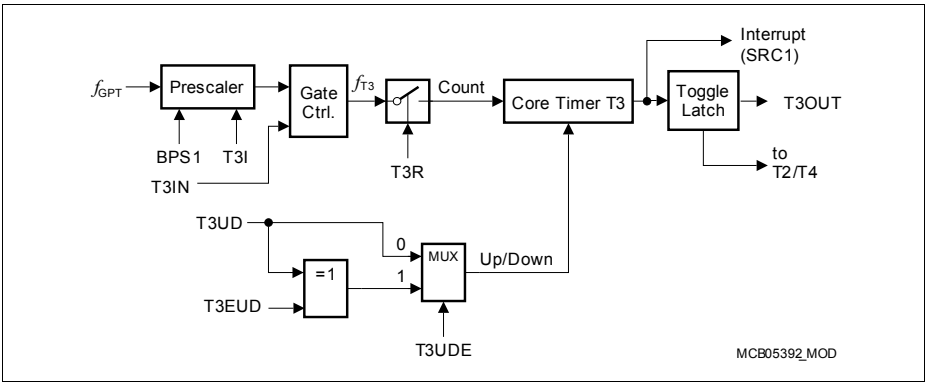


Figure 30-4 Block Diagram of Core Timer T3 in Gated Timer Mode

If T3M = 010_B, the timer is enabled when T3IN shows a low level. A high level at this line stops the timer. If T3M = 011_B, line T3IN must have a high level in order to enable the timer. Additionally, the timer can be turned on or off by software using bit T3R. The timer will only run if T3R is 1 and the gate is active. It will stop if either T3R is 0 or the gate is inactive.

Note: A transition of the gate signal at pin T3IN does not cause an interrupt request via SRC1.

Counter Mode

Counter Mode for the core timer T3 is selected by setting bitfield T3M in register T3CON to 001_B. In Counter Mode, timer T3 is clocked by a transition at the external input pin T3IN. The event causing an increment or decrement of the timer can be a positive, a negative, or both a positive and a negative transition at this line. Bitfield T3I in control register T3CON selects the triggering transition (see **Table 30-2**).

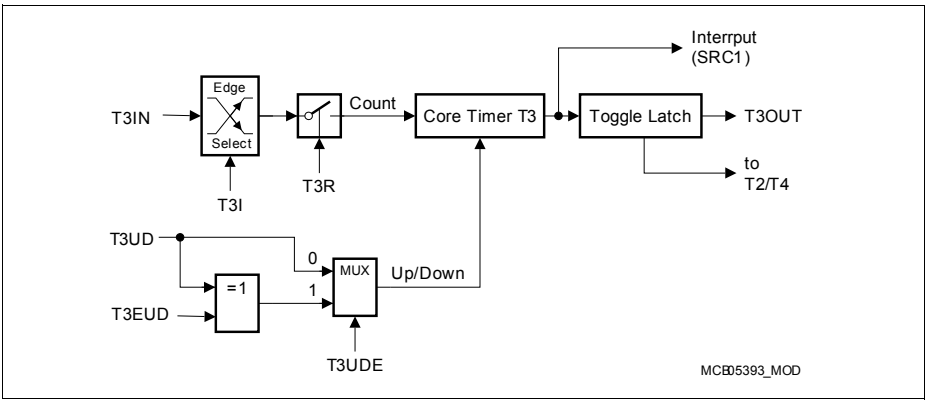


Figure 30-5 Block Diagram of Core Timer T3 in Counter Mode

Table 30-2 GPT1 Core Timer T3 (Counter Mode) Input Edge Selection

T3I	Triggering Edge for Counter Increment/Decrement
000_B	None. Counter T3 is disabled
001_B	Positive transition (rising edge) on T3IN
010_B	Negative transition (falling edge) on T3IN
011_B	Any transition (rising or falling edge) on T3IN
$1XX_B$	Reserved. Do not use this combination

For Counter Mode operation, pin T3IN must be configured as input (the respective direction control bit DPx.y must be 0). The maximum input frequency allowed in Counter Mode depends on the selected prescaler value. To ensure that a transition of the count input signal applied to T3IN is recognized correctly, its level must be held high or low for a minimum number of module clock cycles before it changes. This information can be found in **Section 30.1.5**.

Incremental Interface Mode

Incremental Interface Mode for the core timer T3 is selected by setting bitfield T3M in register T3CON to 110_B or 111_B. In Incremental Interface Mode, the two inputs associated with core timer T3 (T3IN, T3EUD) are used to interface to an incremental encoder. T3 is clocked by each transition on one or both of the external input pins to provide 2-fold or 4-fold resolution of the encoder input.

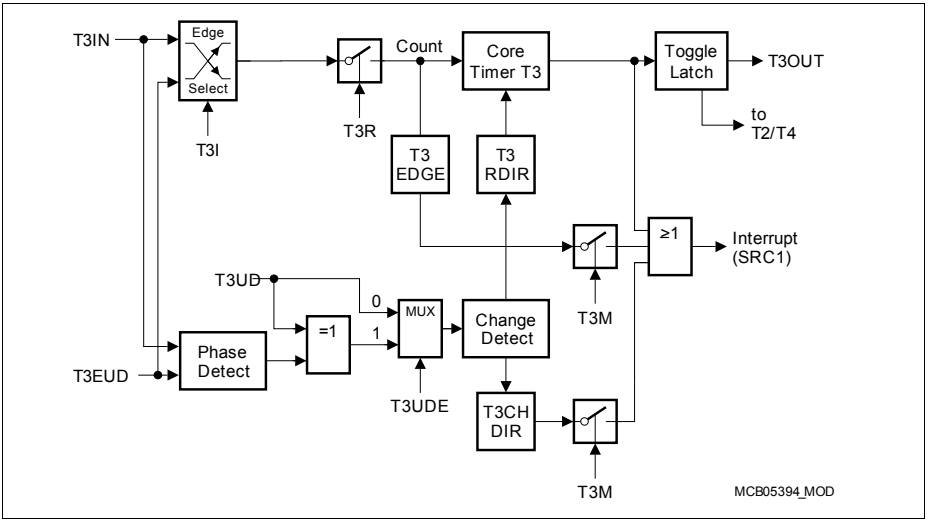


Figure 30-6 Block Diagram of Core Timer T3 in Incremental Interface Mode

Bitfield T3I in control register T3CON selects the triggering transitions (see **Table 30-3**). The sequence of the transitions of the two input signals is evaluated and generates count pulses as well as the direction signal. So T3 is modified automatically according to the speed and the direction of the incremental encoder and, therefore, its contents always represent the encoder's current position.

The interrupt request generation can be selected: In Rotation Detection Mode (T3M = 110_B), an interrupt request is generated each time the count direction of T3 changes. In Edge Detection Mode (T3M = 111_B), an interrupt request is generated each time a count edge for T3 is detected. Count direction, changes in the count direction, and count requests are monitored by status bits T3RDIR, T3CHDIR, and T3EDGE in register T3CON.

Table 30-3 Core Timer T3 (Incremental Interface Mode) Input Edge Selection

T3I	Triggering Edge for Counter Increment/Decrement
000_B	None. Counter T3 stops.
001_B	Any transition (rising or falling edge) on T3IN.
010_B	Any transition (rising or falling edge) on T3EUD.
011_B	Any transition (rising or falling edge) on any T3 input (T3IN or T3EUD).
$1XX_B$	Reserved. Do not use this combination.

The incremental encoder can be connected directly to the TC1798 without external interface logic. In a standard system, however, comparators will be employed to convert the encoder's differential outputs (such as A, $\overline{A}$) to digital signals (such as A). This greatly increases noise immunity.

Note: The third encoder output T0, that indicates the mechanical zero position, may be connected to an external interrupt input and trigger a reset of timer T3.
If input T4IN is available, T0 can be connected there and clear T3 automatically without requiring an interrupt.

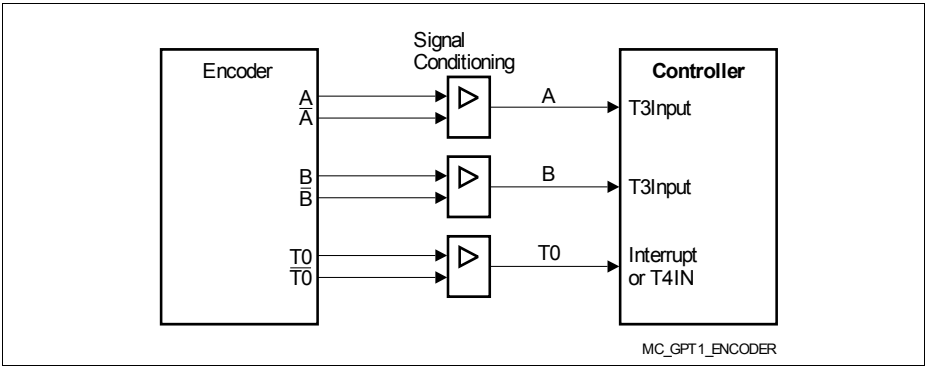


Figure 30-7 Connection of the Encoder to the TC1798

For Incremental Interface Mode operation, the following conditions must be met:

- Bitfield T3M must be 110_B or 111_B.
- Both pins T3IN and T3EUD must be configured as input.
- Pin T4IN must be configured as input, if used for T0.
- Bit T3UDE must be 1 to enable automatic external direction control.

The maximum count frequency allowed in Incremental Interface Mode depends on the selected prescaler value. To ensure that a transition of any input signal is recognized

correctly, its level must be held high or low for a minimum number of module clock cycles before it changes. This information can be found in **Section 30.1.5**.

As in Incremental Interface Mode two input signals with a 90° phase shift are evaluated, their maximum input frequency can be half the maximum count frequency.

In Incremental Interface Mode, the count direction is automatically derived from the sequence in which the input signals change, which corresponds to the rotation direction of the connected sensor. **Table 30-4** summarizes the possible combinations.

Table 30-4 GPT1 Core Timer T3 (Incremental Interface Mode) Count Direction

Level on Respective other Input	T3IN Input		T3EUD Input	
	Rising ↑	Falling ↓	Rising ↑	Falling ↓
High	Down	Up	Up	Down
Low	Up	Down	Down	Up

Figure 30-8 and **Figure 30-9** give examples of T3's operation, visualizing count signal generation and direction control. They also show how input jitter is compensated, which might occur if the sensor rests near to one of its switching points.

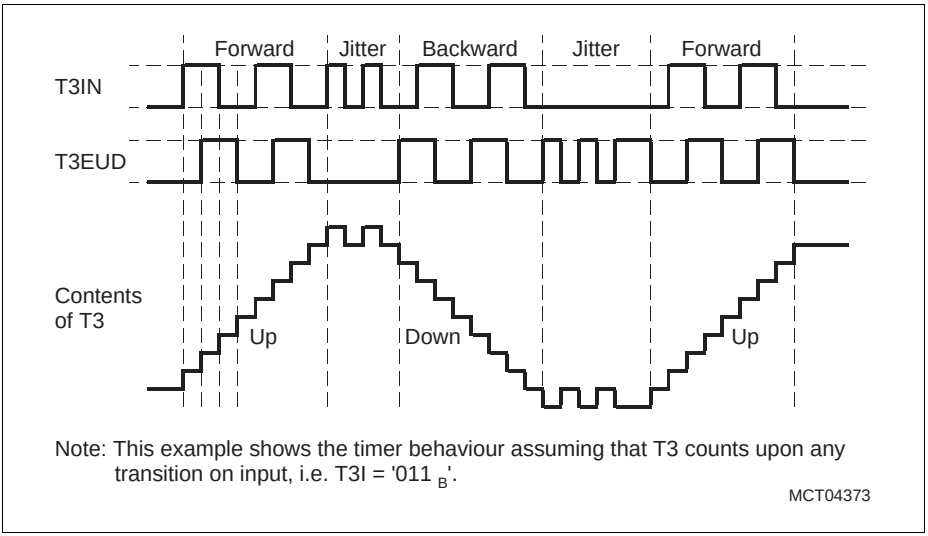


Figure 30-8 Evaluation of Incremental Encoder Signals, 2 Count Inputs

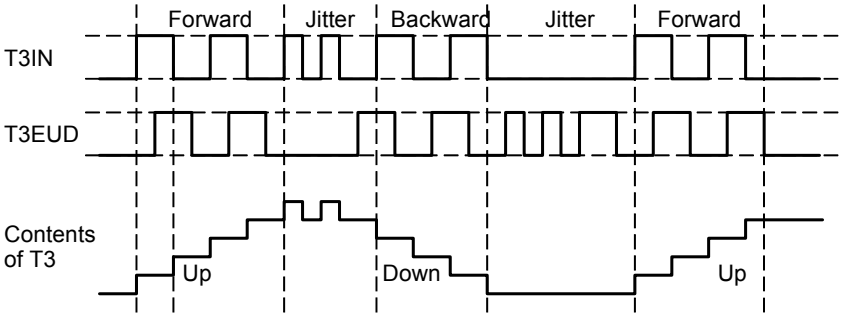


Figure 30-9 Evaluation of Incremental Encoder Signals, 1 Count Input

Note: Timer T3 operating in Incremental Interface Mode automatically provides information on the sensor's current position. Dynamic information (speed, acceleration, deceleration) may be obtained by measuring the incoming signal periods (see ***"Combined Capture Modes" on Page 30-59****).*

30.1.3 GPT1 Auxiliary Timers T2/T4 Control

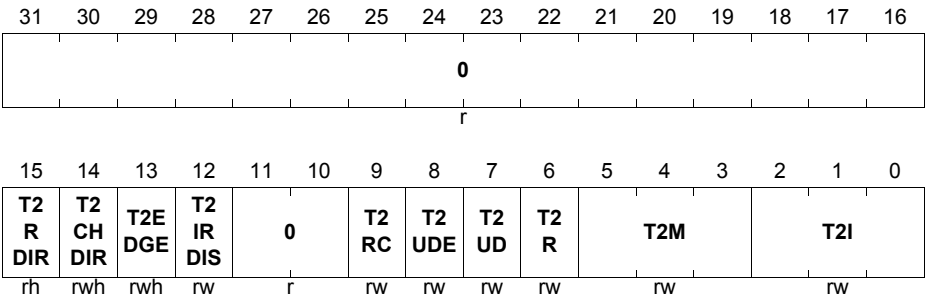
Auxiliary timers T2 and T4 have exactly the same functionality. They can be configured for Timer Mode, Gated Timer Mode, Counter Mode, or Incremental Interface Mode with the same options for the timer frequencies and the count signal as the core timer T3. In addition to these 4 counting modes, the auxiliary timers can be concatenated with the core timer, or they may be used as reload or capture registers in conjunction with the core timer. The start/stop function of the auxiliary timers can be remotely controlled by the T3 run control bit. Several timers may thus be controlled synchronously.

The current contents of an auxiliary timer are reflected by its count register T2 or T4, respectively. These registers can also be written to by the CPU, for example, to set the initial start value.

The individual configurations for timers T2 and T4 are determined by their control registers T2CON and T4CON, that are organized identically. Note that functions which are present in all 3 timers of block GPT1 are controlled in the same bit positions and in the same manner in each of the specific control registers.

Note: The auxiliary timers have no output toggle latch and no alternate output function.

T2CON
Timer 2 Control Register **(10_H)** **Reset Value: 0000 0000_H**



Field	Bits	Type	Description
T2I	[2:0]	rw	**Timer Tx Input Parameter Selection** Depends on the operating mode, see respective sections for encoding: **Table 30-8** for Timer Mode and Gated Timer Mode **Table 30-2** for Counter Mode **Table 30-3** for Incremental Interface Mode

Field	Bits	Type	Description
T2M	[5:3]	rw	**Timer 2 Mode Control (Basic Operating Mode)** 000_B Timer Mode 001_B Counter Mode 010_B Gated Timer Mode with gate active low 011_B Gated Timer Mode with gate active high 100_B Reload Mode 101_B Capture Mode 110_B Incremental Interface Mode (Rotation Detection Mode) 111_B Incremental Interface Mode (Edge Detection Mode)
T2R	6	rw	**Timer 2 Run Bit** 0_B Timer / Counter 2 stops 1_B Timer / Counter 2 runs
T2UD	7	rw	**Timer 2 Up/Down Control** (when T2UDE = ’0’) 0_B Counting ’Up’ 1_B Counting ’Down’
T2UDE	8	rw	**Timer 2 External Up/Down Enable** 0_B Counting direction is internally controlled by software 1_B Counting direction is externally controlled by line TxEUD
T2RC	9	rw	**Timer 2 Remote Control** 0_B Timer / Counter 2 is controlled by its own run bit T2R 1_B Timer / Counter 2 is controlled by the run bit of core timer 3
T2IRDIS	12	rw	**Timer 2 Interrupt Disable** 0_B Interrupt generation for T2CHDIR and T2EDGE interrupts in Incremental Interface Mode is enabled 1_B Interrupt generation for T2CHDIR and T2EDGE interrupts in Incremental Interface Mode is disabled

Field	Bits	Type	Description
T2EDGE	13	rwh	**Timer 2 Edge Detection** The bit is set on each successful edge detection. The bit has to be cleared by software. 0_B No count edge was detected 1_B A count edge was detected
T2CHDIR	14	rwh	**Timer 2 Count Direction Change** The bit is set on a change of the count direction of timer 2. The bit has to be cleared by software. 0_B No change in count direction was detected 1_B A change in count direction was detected
T2RDIR	15	rh	**Timer 2 Rotation Direction** 0_B Timer 2 counts up 1_B Timer 2 counts down
0	[11:10], [31:16]	r	**Reserved** Read as 0; should be written with 0.

T4CON
Timer 4 Control Register **(18_H)** **Reset Value: 0000 0000$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
T4 R DIR	**T4 CH DIR**	**T4E DGE**	**T4 IR DIS**	**CLR T3 EN**	**CLR T2 EN**	**T4 RC**	**T4 UDE**	**T4 UD**	**T4 R**	**T4M**			**T4I**		
rh	rwh	rwh	rw	rw	rw	rw	rw	rw	rw	rw			rw		

Field	Bits	Type	Description
T4I	[2:0]	rw	**Timer Tx Input Parameter Selection** Depends on the operating mode, see respective sections for encoding: **Table 30-8** for Timer Mode and Gated Timer Mode **Table 30-2** for Counter Mode **Table 30-3** for Incremental Interface Mode

Field	Bits	Type	Description
T4M	[5:3]	rw	**Timer 4 Mode Control (Basic Operating Mode)** 000_B Timer Mode 001_B Counter Mode 010_B Gated Timer Mode with gate active low 011_B Gated Timer Mode with gate active high 100_B Reload Mode 101_B Capture Mode 110_B Incremental Interface Mode (Rotation Detection Mode) 111_B Incremental Interface Mode (Edge Detection Mode)
T4R	6	rw	**Timer 4 Run Bit** 0_B Timer / Counter 4 stops 1_B Timer / Counter 4 runs
T4UD	7	rw	**Timer 4 Up/Down Control** (when T4UDE = '0') 0_B Counting 'Up' 1_B Counting 'Down'
T4UDE	8	rw	**Timer 4 External Up/Down Enable** 0_B Counting direction is internally controlled by software 1_B Counting direction is externally controlled by line T4EUD
T4RC	9	rw	**Timer 4 Remote Control** 0_B Timer / Counter 4 is controlled by its own run bit T4R 1_B Timer / Counter 4 is controlled by the run bit of core timer 3
CLRT2EN	10	rw	**Clear Timer 2 Enable** Enables the automatic clearing of T2 upon a falling edge of the selected T4EUD input. 0_B No effect of T4EUD on T2 1_B A falling edge on T4EUD clears timer T2
CLRT3EN	11	rw	**Clear Timer 3 Enable** Enables the automatic clearing of T3 upon a falling edge of the selected T4IN input. 0_B No effect of T4IN on T3 1_B A falling edge on T4IN clears timer T3

Field	Bits	Type	Description
T4IRDIS	12	rw	**Timer 4 Interrupt Disable** 0_B Interrupt generation for T4CHDIR and T4EDGE interrupts in Incremental Interface Mode is enabled 1_B Interrupt generation for T4CHDIR and T4EDGE interrupts in Incremental Interface Mode is disabled
T4EDGE	13	rwh	**Timer 4 Edge Detection** The bit is set on each successful edge detection. The bit has to be cleared by software. 0_B No count edge was detected 1_B A count edge was detected
T4CHDIR	14	rwh	**Timer 4 Count Direction Change** The bit is set on a change of the count direction of timer 4. The bit has to be cleared by software. 0_B No change in count direction was detected 1_B A change in count direction was detected
T4RDIR	15	rh	**Timer 4 Rotation Direction** 0_B Timer 4 counts up 1_B Timer 4 counts down
0	[31:16]	r	**Reserved** Read as 0; should be written with 0.

Timer T2/T4 Run Control

Each of the auxiliary timers T2 and T4 can be started or stopped by software in two different ways:

- Through the associated timer run bit (T2R or T4R). In this case it is required that the respective control bit TxRC = 0.
- Through the core timer's run bit (T3R). In this case the respective remote control bit must be set (TxRC = 1).

The selected run bit is relevant in all operating modes of T2/T4. Setting the bit will start the timer, clearing the bit stops the timer.

In Gated Timer Mode, the timer will only run if the selected run bit is set and the gate is active (high or low, as programmed).

Note: If remote control is selected T3R will start/stop timer T3 and the selected auxiliary timer(s) synchronously.

Count Direction Control

The count direction of the GPT1 timers (core timer and auxiliary timers) is controlled in the same way, either by software or by the external input pin TxEUD. Please refer to the description in **Table 30-1**.

Note: When pin TxEUD is used as external count direction control input, it must be configured as input (its corresponding direction control bit must be cleared).

30.1.4 GPT1 Auxiliary Timers T2/T4 Operating Modes

The operation of the auxiliary timers in the basic operating modes is almost identical with the core timer's operation, with very few exceptions. Additionally, some combined operating modes can be selected.

Timers T2 and T4 in Timer Mode

Timer Mode for an auxiliary timer Tx is selected by setting its bitfield TxM in register TxCON to 000_B.

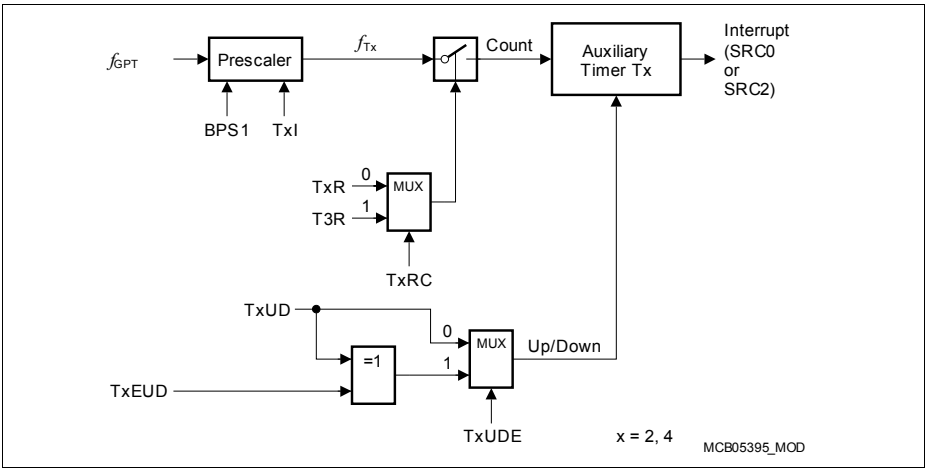


Figure 30-10 Block Diagram of an Auxiliary Timer in Timer Mode

Timers T2 and T4 in Gated Timer Mode

Gated Timer Mode for an auxiliary timer Tx is selected by setting bitfield TxM in register TxCON to 010_B or 011_B. Bit TxM.0 (TxCON.3) selects the active level of the gate input.

Note: A transition of the gate signal at TxIN does not cause an interrupt request. Interrupts of timer 2 are handled by register SRC0 and interrupts of timer 4 are handled by register SRC2.

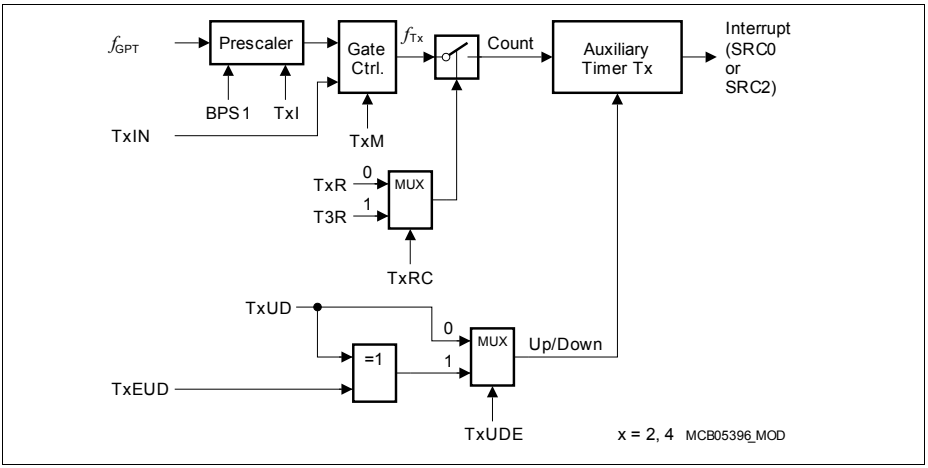


Figure 30-11 Block Diagram of an Auxiliary Timer in Gated Timer Mode

Note: There is no output toggle latch for T2 and T4.
Start/stop of an auxiliary timer can be controlled locally or remotely.

Timers T2 and T4 in Counter Mode

Counter Mode for an auxiliary timer Tx is selected by setting bitfield TxM in register TxCON to 001_B. In Counter Mode, an auxiliary timer can be clocked either by a transition at its external input line TxIN, or by a transition of timer T3's toggle latch T3OTL. The event causing an increment or decrement of a timer can be a positive, a negative, or both a positive and a negative transition at either the respective input pin or at the toggle latch. Bitfield TxI in control register TxCON selects the triggering transition (see **Table 30-5**).

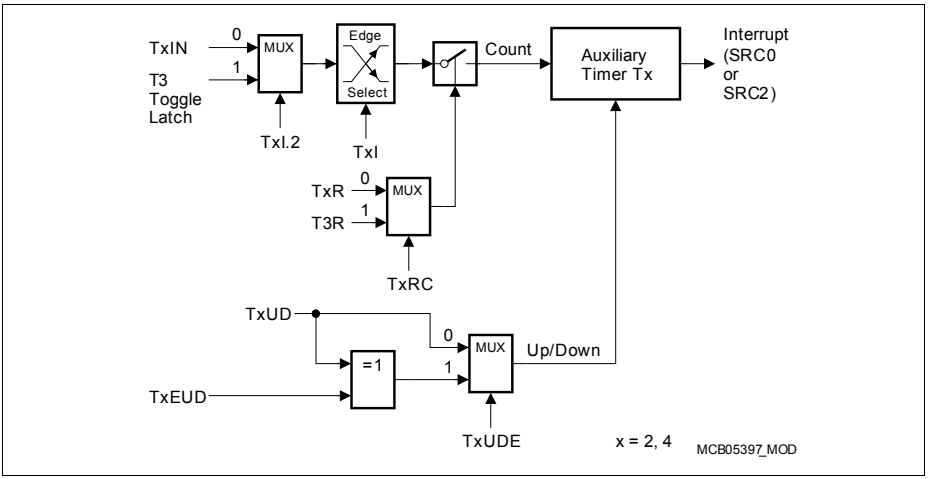


Figure 30-12 Block Diagram of an Auxiliary Timer in Counter Mode

Table 30-5 GPT1 Auxiliary Timer (Counter Mode) Input Edge Selection

T2I/T4I	Triggering Edge for Counter Increment/Decrement
$X00_B$	None. Counter Tx is disabled
001_B	Positive transition (rising edge) on TxIN
010_B	Negative transition (falling edge) on TxIN
011_B	Any transition (rising or falling edge) on TxIN
101_B	Positive transition (rising edge) of T3 toggle latch T3OTL
110_B	Negative transition (falling edge) of T3 toggle latch T3OTL
111_B	Any transition (rising or falling edge) of T3 toggle latch T3OTL

Note: Only state transitions of T3OTL which are caused by the overflows/underflows of T3 will trigger the counter function of T2/T4. Modifications of T3OTL via software will NOT trigger the counter function of T2/T4.

For counter operation, pin TxIN must be configured as input. The maximum input frequency allowed in Counter Mode depends on the selected prescaler value. To ensure that a transition of the count input signal applied to TxIN is recognized correctly, its level must be held high or low for a minimum number of module clock cycles before it changes. This information can be found in **Section 30.1.5**.

Timers T2 and T4 in Incremental Interface Mode

Incremental Interface Mode for an auxiliary timer Tx is selected by setting bitfield TxM in the respective register TxCON to 110_B or 111_B. In Incremental Interface Mode, the two inputs associated with an auxiliary timer Tx (TxIN, TxEUD) are used to interface to an incremental encoder. Tx is clocked by each transition on one or both of the external input pins to provide 2-fold or 4-fold resolution of the encoder input.

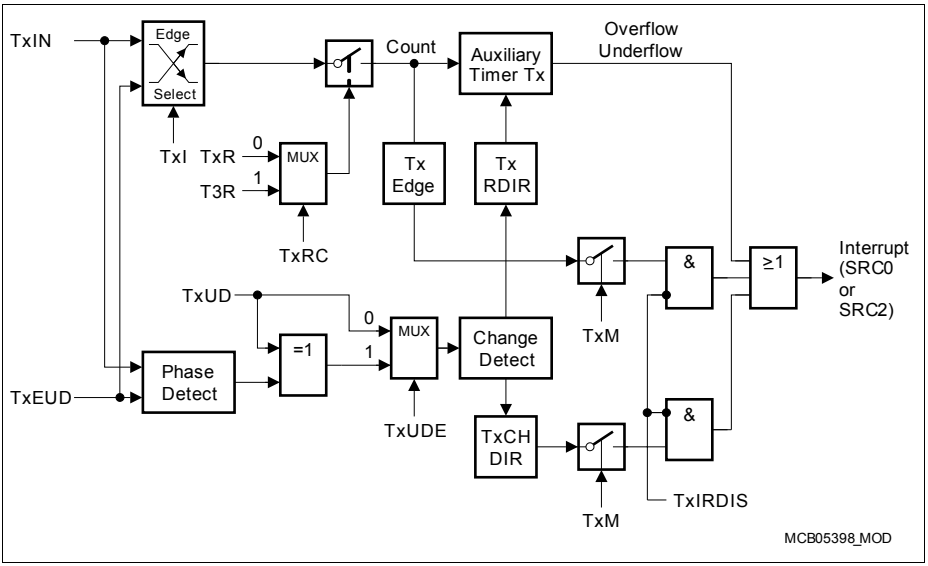


Figure 30-13 Block Diagram of an Auxiliary Timer in Incremental Interface Mode

The operation of the auxiliary timers T2 and T4 in Incremental Interface Mode and the interrupt generation are the same as described for the core timer T3. The descriptions, figures and tables apply accordingly.

*Note: Timers T2 and T4 operating in Incremental Interface Mode automatically provide information on the sensor's current position. For dynamic information (speed, acceleration, deceleration) see **"Combined Capture Modes" on Page 30-59**).*

Timer Concatenation

Using the toggle bit T3OTL as a clock source for an auxiliary timer in Counter Mode concatenates the core timer T3 with the respective auxiliary timer. This concatenation forms either a 32-bit or a 33-bit timer/counter, depending on which transition of T3OTL is selected to clock the auxiliary timer.

- **32-bit Timer/Counter:** If both a positive and a negative transition of T3OTL are used to clock the auxiliary timer, this timer is clocked on every overflow/underflow of the core timer T3. Thus, the two timers form a 32-bit timer.
- **33-bit Timer/Counter:** If either a positive or a negative transition of T3OTL is selected to clock the auxiliary timer, this timer is clocked on every second overflow/underflow of the core timer T3. This configuration forms a 33-bit timer (16-bit core timer + T3OTL + 16-bit auxiliary timer).
  As long as bit T3OTL is not modified by software, it represents the state of the internal toggle latch, and can be regarded as part of the 33-bit timer.

The count directions of the two concatenated timers are not required to be the same. This offers a wide variety of different configurations.

T3, which represents the low-order part of the concatenated timer, can operate in Timer Mode, Gated Timer Mode or Counter Mode in this case.

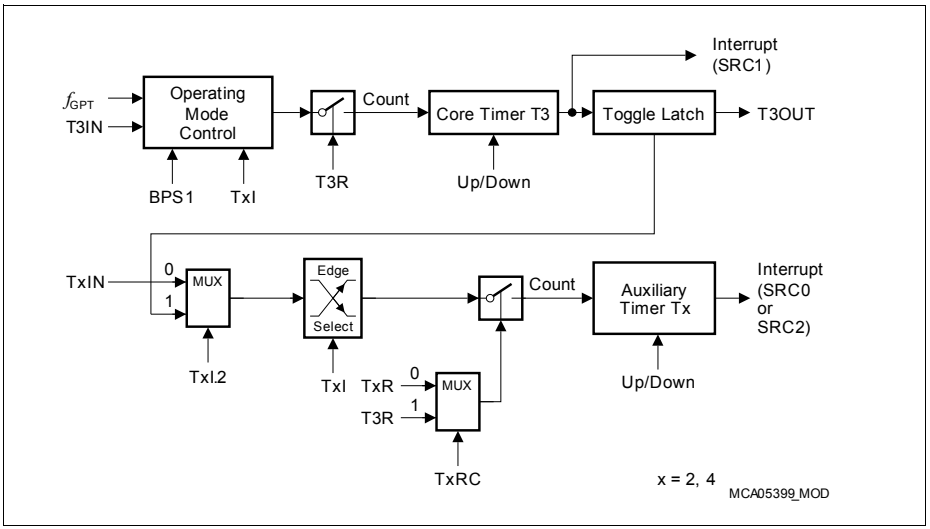


Figure 30-14 Concatenation of Core Timer T3 and an Auxiliary Timer

When reading the low and high parts of the concatenated timer, care must be taken to obtain consistent values in particular after a timer overflow/underflow (e.g. one part may already have considered an overflow, while the other has not).

Note: This is a general issue when reading multi-word results with consecutive instructions, and not necessarily unique to the GPT12 module architecture.

The following algorithm may be used to read concatenated GPT1 timers, represented by TIMER_HIGH (for auxiliary timer, here T2) and TIMER_LOW (for core timer T3). The high part is read twice, and reading of the low part is repeated if two different values were read for the high part:

- TIMER_HIGH_TMP = T2
- TIMER_LOW = T3
- Wait two basic clock cycles (to allow increment/decrement of auxiliary timer in case of core timer overflow/underflow) - see **Table 30-6**
- TIMER_HIGH = T2
- If TIMER_HIGH is not equal to TIMER_HIGH_TMP then TIMER_LOW = T3

After execution of this algorithm, TIMER_HIGH and TIMER_LOW represent a consistent time stamp of the concatenated timers.

The equivalent number of system clock cycles corresponding to two basic clock cycles is shown in **Table 30-6**.

Table 30-6 Number of System Clock Cycles to Wait for Two Basic Clock Cycles

Block Prescaler	BPS1 = 01_B	BPS1 = 00_B	BPS1 = 11_B	BPS1 = 10_B
Number of system clocks	8	16	32	64

In case the required timer resolution can be achieved with different combinations of the Block Prescaler BPS1 and the Individual Prescalers TxI, the variant with the smallest value for the Block Prescaler may be chosen to minimize the waiting time.

Auxiliary Timer in Reload Mode

Reload Mode for an auxiliary timer Tx is selected by setting bitfield TxM in the respective register TxCON to 100_B. In Reload Mode, the core timer T3 is reloaded with the contents of an auxiliary timer register, triggered by one of two different signals. The trigger signal is selected the same way as the clock source for Counter Mode (see **Table 30-5**), i.e. a transition of the auxiliary timer's input TxIN or the toggle latch T3OTL may trigger the reload.

Note: When programmed for Reload Mode, the respective auxiliary timer (T2 or T4) stops independently of its run flag T2R or T4R.
The timer input pin TxIN must be configured as input if it shall trigger a reload operation.

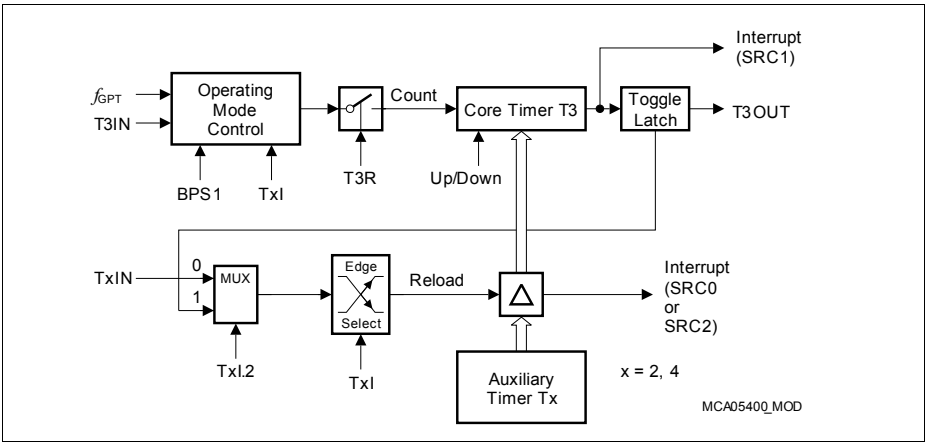


Figure 30-15 GPT1 Auxiliary Timer in Reload Mode

Upon a trigger signal, T3 is loaded with the contents of the respective timer register (T2 or T4) and the respective service request flag (SRR) is set.

Note: When a T3OTL transition is selected for the trigger signal, the service request flag will also be set upon a trigger, indicating T3's overflow or underflow. Modifications of T3OTL via software will NOT trigger the counter function of T2/T4.

To ensure that a transition of the reload input signal applied to TxIN is recognized correctly, its level must be held high or low for a minimum number of module clock cycles, detailed in **Section 30.1.5**.

The Reload Mode triggered by the T3 toggle latch can be used in a number of different configurations. The following functions can be performed, depending on the selected active transition:

- If both a positive and a negative transition of T3OTL are selected to trigger a reload, the core timer will be reloaded with the contents of the auxiliary timer each time it overflows or underflows. This is the standard Reload Mode (reload on overflow/underflow).
- If either a positive or a negative transition of T3OTL is selected to trigger a reload, the core timer will be reloaded with the contents of the auxiliary timer on every second overflow or underflow.
- Using this "single-transition" mode for both auxiliary timers allows to perform very flexible Pulse Width Modulation (PWM). One of the auxiliary timers is programmed to reload the core timer on a positive transition of T3OTL, the other is programmed for a reload on a negative transition of T3OTL. With this combination the core timer is alternately reloaded from the two auxiliary timers.

Figure 30-16 shows an example for the generation of a PWM signal using the “single-transition” reload mechanism. T2 defines the high time of the PWM signal (reloaded on positive transitions) and T4 defines the low time of the PWM signal (reloaded on negative transitions). The PWM signal can be output on pin T3OUT if T3OE = 1. With this method, the high and low time of the PWM signal can be varied in a wide range.

Note: The output toggle latch T3OTL is accessible via software and may be changed, if required, to modify the PWM signal.
However, this will NOT trigger the reloading of T3.

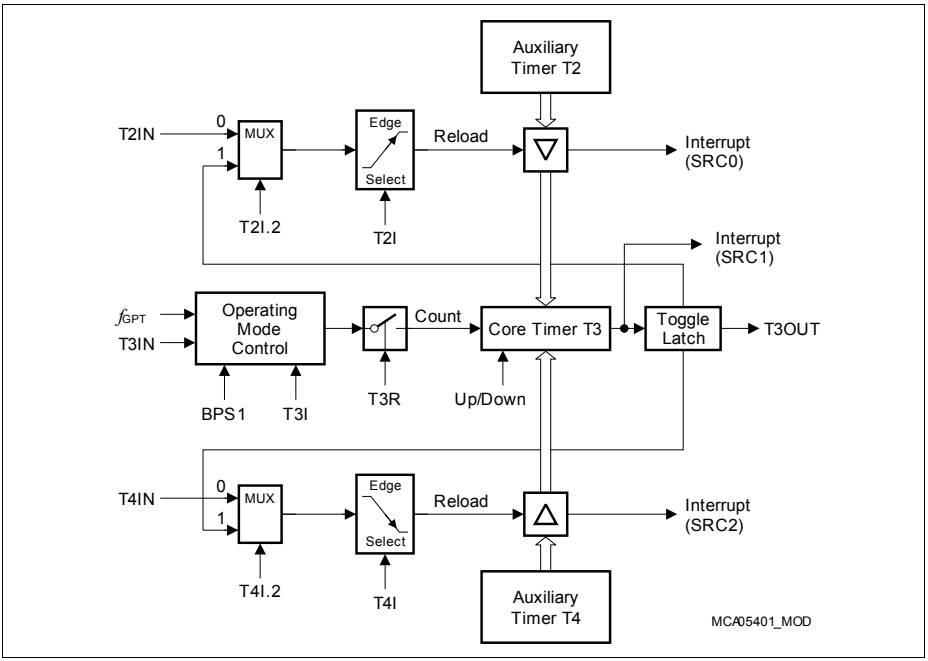


Figure 30-16 GPT1 Timer Reload Configuration for PWM Generation

Note: Although possible, selecting the same reload trigger event for both auxiliary timers should be avoided. In such a case, both reload registers would try to load the core timer at the same time. If this combination is selected, T2 is disregarded and the contents of T4 is reloaded.

The implementation of the GPT1 finite state machine may require special consideration in following applications:

- Reading T3 by Software with T2/T4 in Reload Mode
- Reload of T3 from T2 with setting BPS1 = 01_B and T3I = 000_B

When T2 or T4 are used to reload T3 on overflow/underflow, and T3 is read by software on the fly, the following unexpected values may be read from T3:

- When T3 is counting up, 0000_H or 0001_H may be read from T3 directly after an overflow, although the reload value in T2/T4 is higher (0001_H may be read in particular if BPS1 = 01_B and T3I = 000_B).
- When T3 is counting down, $FFFF_H$ or $FFFE_H$ may be read from T3 directly after an underflow, although the reload value in T2/T4 is lower ($FFFE_H$ may be read in particular if BPS1 = 01_B and T3I = 000_B).

Note: All timings derived from T3 in this configuration (e.g. distance between interrupt requests, PWM waveform on T3OUT, etc.) are accurate except for the specific case described below.

Workaround:

- When T3 counts up, and value_x < reload value is read from T3, value_x should be replaced with the reload value for further calculations.
- When T3 counts down, and value_x > reload value is read from T3, value_x should be replaced with the reload value for further calculations.

Alternatively, if the intention is to identify the overflow/underflow of T3, the T3 interrupt request may be used.

When T2 is used to reload T3 in the configuration with BPS1 = 01_B and T3I = 000_B (i.e. fastest configuration/highest resolution of T3), the reload of T3 is performed with a delay of one basic clock cycle.

Workaround 1:

To compensate the delay and achieve correct timing,

- increment the reload value in T2 by 1 when T3 is configured to count up,
- decrement the reload value in T2 by 1 when T3 is configured to count down.

Workaround 2:

Use T4 instead of T2 as reload register for T3. In this configuration the reload of T3 is not delayed, i.e. the effect described above does not occur with T4.

Auxiliary Timer in Capture Mode

Capture Mode for an auxiliary timer Tx is selected by setting bitfield TxM in the respective register TxCON to 101_B. In Capture Mode, the contents of the core timer T3 are latched into an auxiliary timer register in response to a signal transition at the respective auxiliary timer's external input pin TxIN. The capture trigger signal can be a positive, a negative, or both a positive and a negative transition.

The two least significant bits of bitfield TxI select the active transition (see **Table 30-5**). Bit 2 of TxI is irrelevant for Capture Mode and must be cleared (TxI.2 = 0).

Note: When programmed for Capture Mode, the respective auxiliary timer (T2 or T4) stops independently of its run flag T2R or T4R.

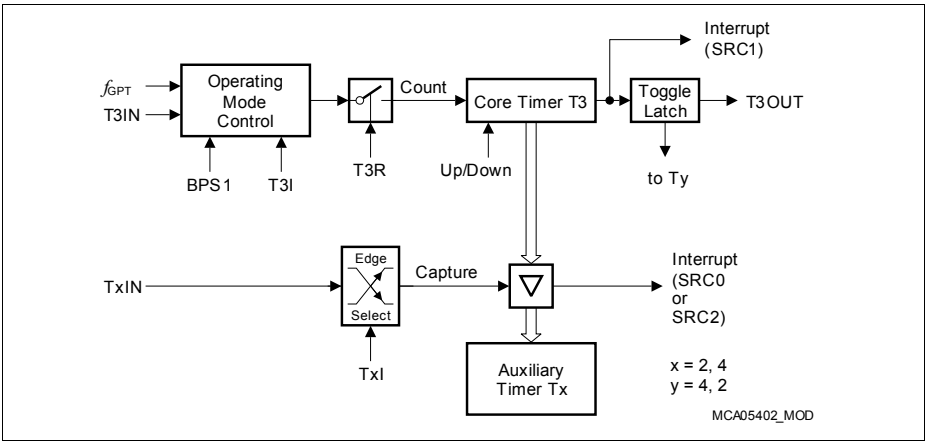


Figure 30-17 GPT1 Auxiliary Timer in Capture Mode

Upon a trigger (selected transition) at the corresponding input pin TxIN the contents of the core timer are loaded into the auxiliary timer register and the associated service request flag SRR will be set.

For Capture Mode operation, the respective timer input pin TxIN must be configured as input. To ensure that a transition of the capture input signal applied to TxIN is recognized correctly, its level must be held high or low for a minimum number of module clock cycles, detailed in **Section 30.1.5**.

30.1.5 GPT1 Clock Signal Control

All actions within the timer block GPT1 are triggered by transitions of its basic clock. This basic clock is derived from the system clock by a basic block prescaler, controlled by bitfield BPS1 in register T3CON (see **Figure 30-1**). The count clock can be generated in two different ways:

- **Internal count clock**, derived from GPT1's basic clock via a programmable prescaler, is used for (Gated) Timer Mode.
- **External count clock**, derived from the timer's input pin(s), is used for Counter Mode.

For both ways, the basic clock determines the maximum count frequency and the timer's resolution:

Table 30-7 Basic Clock Selection for Block GPT1

Block Prescaler[1]	BPS1 = 01_B	BPS1 = 00_B[2]	BPS1 = 11_B	BPS1 = 10_B
Prescaling Factor for GPT1: F(BPS1)	F(BPS1) = 4	F(BPS1) = 8	F(BPS1) = 16	F(BPS1) = 32
Maximum External Count Frequency	$f_{GPT}/8$	$f_{GPT}/16$	$f_{GPT}/32$	$f_{GPT}/64$
Input Signal Stable Time	$4 \times t_{GPT}$	$8 \times t_{GPT}$	$16 \times t_{GPT}$	$32 \times t_{GPT}$

1) Please note the non-linear encoding of bitfield BPS1.

2) Default after reset.

Internal Count Clock Generation

In Timer Mode and Gated Timer Mode, the count clock for each GPT1 timer is derived from the GPT1 basic clock by a programmable prescaler, controlled by bitfield TxI in the respective timer's control register TxCON.

The count frequency f_{Tx} for a timer Tx and its resolution r_{Tx} are scaled linearly with lower clock frequencies, as can be seen from the following formula:

$$f_{Tx} = \frac{f_{GPT}}{F(BPS1) \times 2^{<TxI>}} \qquad r_{Tx}[\mu s] = \frac{F(BPS1) \times 2^{<TxI>}}{f_{GPT}[MHz]} \tag{30.1}$$

The effective count frequency depends on the common module clock prescaler factor F(BPS1) as well as on the individual input prescaler factor $2^{<TxI>}$. **Table 30-8** summarizes the resulting overall divider factors for a GPT1 timer that result from these cascaded prescalers.

Table 30-8 GPT1 Overall Prescaler Factors for Internal Count Clock

Individual Prescaler for Tx	Common Prescaler for Module Clock[1]			
	$BPS1 = 01_B$	$BPS1 = 00_B$	$BPS1 = 11_B$	$BPS1 = 10_B$
$TxI = 000_B$	4	8	16	32
$TxI = 001_B$	8	16	32	64
$TxI = 010_B$	16	32	64	128
$TxI = 011_B$	32	64	128	256
$TxI = 100_B$	64	128	256	512
$TxI = 101_B$	128	256	512	1024
$TxI = 110_B$	256	512	1024	2048
$TxI = 111_B$	512	1024	2048	4096

1) Please note the non-linear encoding of bitfield BPS1.

External Count Clock Input

The external input signals of the GPT1 block are sampled with the GPT1 basic clock (see **Figure 30-1**). To ensure that a signal is recognized correctly, its current level (high or low) must be held active for at least one complete sampling period, before changing. A signal transition is recognized if two subsequent samples of the input signal represent different levels. Therefore, a minimum of two basic clock periods are required for the sampling of an external input signal. Thus, the maximum frequency of an input signal must not be higher than half the basic clock.

Table 30-9 summarizes the resulting requirements for external GPT1 input signals.

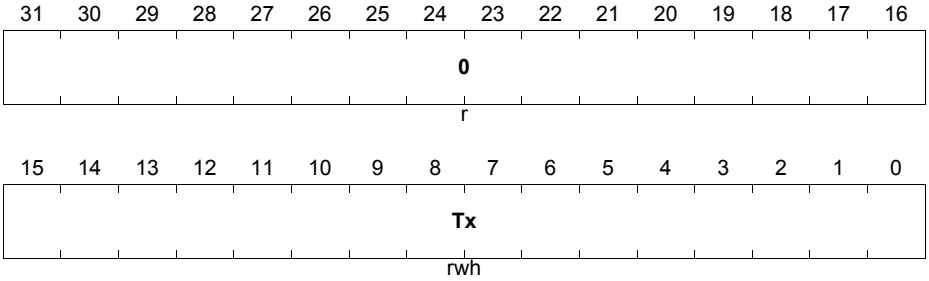
Table 30-9 GPT1 External Input Signal Limits

GPT1 Basic Clock = 10 MHz		Input Frequ. Factor	GPT1 Divider BPS1	Input Phase Duration	GPT1 Basic Clock = 40 MHz	
Max. Input Frequency	Min. Level Hold Time				Max. Input Frequency	Min. Level Hold Time
1.25 MHz	400 ns	$f_{GPT}/8$	01_B	$4 \times t_{GPT}$	5.0 MHz	100 ns
625.0 kHz	800 ns	$f_{GPT}/16$	00_B	$8 \times t_{GPT}$	2.5 MHz	200 ns
312.5 kHz	1.6 µs	$f_{GPT}/32$	11_B	$16 \times t_{GPT}$	1.25 MHz	400 ns
156.25 kHz	3.2 µs	$f_{GPT}/64$	10_B	$32 \times t_{GPT}$	625.0 kHz	800 ns

These limitations are valid for all external input signals to GPT1, including the external count signals in Counter Mode and Incremental Interface Mode, the gate input signals in Gated Timer Mode, and the external direction signals.

30.1.6 GPT1 Timer Registers

T2
Timer 2 Register **(34_H)** **Reset Value: 0000 0000_H**
T3
Timer 3 Register **(38_H)** **Reset Value: 0000 0000_H**
T4
Timer 4 Register **($3C_H$)** **Reset Value: 0000 0000_H**



Field	Bits	Type	Description
Tx	[15:0]	rwh	**Timer x** Contains the current value of Timer x.
0	[31:16]	r	**Reserved** Read as 0; should be written with 0.

30.1.7 Interrupt Control for GPT1 Timers

When a timer overflows from $FFFF_H$ to 0000_H (when counting up), or when it underflows from 0000_H to $FFFF_H$ (when counting down), its service request flag (SRR) in register SRCx will be set.

Interrupts of timer 2 are connected with register SRC0.

Interrupts of timer 3 are connected with register SRC1.

Interrupts of timer 4 are connected with register SRC2.

SRC0
Service Request Control 0 Register (FC_H) Reset Value: 0000 0000_H
SRC1
Service Request Control 1 Register ($F8_H$) Reset Value: 0000 0000_H
SRC2
Service Request Control 2 Register ($F4_H$) Reset Value: 0000 0000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SETR	CLRR	SRR	SRE	0	TOS	0		SRPN							
w	w	rh	rw	r	rw	r		rw							

Field	Bits	Type	Description
SRPN	[7:0]	rw	**Service Request Priority Number** 00_H Service request is never serviced 01_H Service request is on lowest priority ... FF_H Service request is on highest priority
TOS	10	rw	**Type of Service Control** 0_B CPU service is initiated 1_B PCP service is initiated
SRE	12	rw	**Service Request Enable** 0_B Service request is disabled 1_B Service request is enabled

Field	Bits	Type	Description
SRR	13	rh	**Service Request Flag** 0_B No service request is pending 1_B A service request is pending
CLRR	14	w	**Request Clear Bit** CLRR is required to clear SRR. 0_B No action 1_B Clear SRR; bit value is not stored; read always returns 0; no action if SETR is set also.
SETR	15	w	**Request Set Bit** SETR is required to set SRR. 0_B No action 1_B Set SRR; bit value is not stored; read always returns 0; no action if CLRR is set also.
0	[9:8], 11, [31:16]	r	**Reserved** Read as 0; should be written with 0.

30.2 Timer Block GPT2

Both timers of block GPT2 (T5, T6) can run in one of 3 basic modes: Timer Mode, Gated Timer Mode, or Counter Mode. All timers can count up or down. Each timer of GPT2 is controlled by a separate control register TxCON.

Each timer has an input pin TxIN (alternate pin function) associated with it, which serves as the gate control in Gated Timer Mode, or as the count input in Counter Mode. The count direction (up/down) may be programmed via software or may be dynamically altered by a signal at the External Up/Down control input TxEUD (alternate pin function). An overflow/underflow of core timer T6 is indicated by the Output Toggle Latch T6OTL, whose state may be output on the associated pin T6OUT (alternate pin function). The auxiliary timer T5 may additionally be concatenated with core timer T6 (through T6OTL).

The Capture/Reload register CAPREL can be used to capture the contents of timer T5, or to reload timer T6. A special mode facilitates the use of register CAPREL for both functions at the same time. This mode allows frequency multiplication. The capture function is triggered by the input pin CAPIN, or by GPT1 timer's T3 input lines T3IN and T3EUD. The reload function is triggered by an overflow or underflow of timer T6.

The current contents of each timer can be read or modified by the CPU by accessing the corresponding timer count registers T5 or T6. When any of the timer registers is written by the CPU in the state immediately preceding a timer increment, decrement, reload, or capture operation, the CPU write operation has priority in order to guarantee correct results.

The interrupts of GPT2 are controlled through the Service Request Control Registers SRC3, SRC4, and SRC5.

*Note: The timing requirements for external input signals can be found in **Section 30.2.6**, **Section 30.5** summarizes the module interface signals, including pins.*

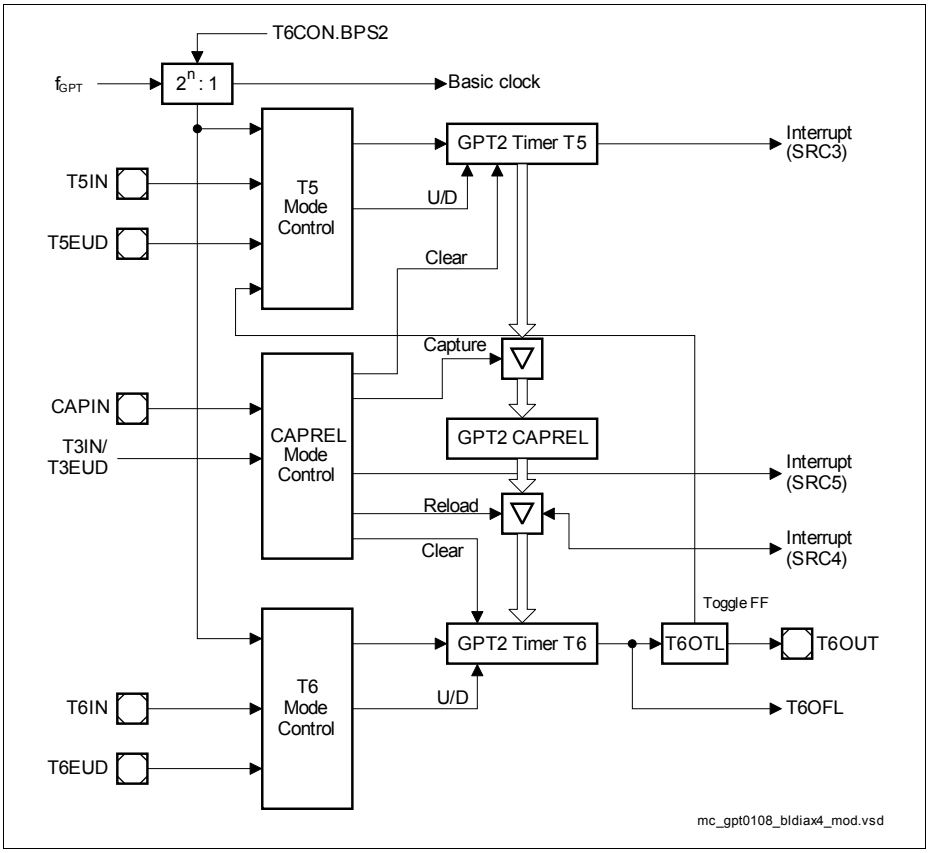


Figure 30-18 GPT2 Block Diagram

Note: The GPT2 module uses a finite state machine to control the actions. Since multiple interactions are possible between the timers (T5, T6) and register CAPREL, these elements are processed sequentially. However, all actions are normally completed within one basic clock cycle. The GPT2 state machine has 4 states (1 states when BPS1 = 01_B) and processes T6 before T5.

30.2.1 GPT2 Core Timer T6 Control

The current contents of the core timer T6 are reflected by its count register T6. This register can also be written to by the CPU, for example, to set the initial start value.

The core timer T6 is configured and controlled via its control register T6CON.

T6CON
Timer 6 Control Register **(20_H)** **Reset Value: 0000 0000_H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
T6 SR	T6 CLR	0	BPS2		T6 OTL	T6 OE	T6 UDE	T6 UD	T6 R	T6M			T6I		
rw	rw	r	rw		rwh	rw	rw	rw	rw	rw			rw		

Field	Bits	Type	Description
T6I	[2:0]	rw	**Timer T6 Input Parameter Selection** Depends on the operating mode, see respective sections for encoding: **Table 30-16** for Timer Mode and Gated Timer Mode **Table 30-11** for Counter Mode
T6M	[5:3]	rw	**Timer T6 Mode Control** (Basic Operating Mode) 000_B Timer Mode 001_B Counter Mode 010_B Gated Timer Mode with gate active low 011_B Gated Timer Mode with gate active high 100_B Reserved. Do not use this combination 101_B Reserved. Do not use this combination 110_B Reserved. Do not use this combination 111_B Reserved. Do not use this combination
T6R	6	rw	**Timer T6 Run Bit** 0_B Timer T6 stops 1_B Timer T3 runs

Field	Bits	Type	Description
T6UD	7	rw	**Timer 6 Up / Down Control**[1)] (when T6UDE = '0') 0_B Timer T6 counts up 1_B Timer T6 counts down
T6UDE	8	rw	**Timer T6 Up/Down Control**[1)] 0_B Timer T6 counts up 1_B Timer T6 counts down
T6OE	9	rw	**Overflow/Underflow Output Enable** 0_B Alternate Output Function Disabled 1_B State of T6 toggle latch is output on pin T6OUT
T6OTL	10	rwh	**Timer T6 Overflow Toggle Latch** Toggles on each overflow/underflow of T6. Can be set or cleared by software (see separate description)
BPS2	[12:11]	rw	**GPT2 Block Prescaler Control** Selects the basic clock for block GPT2 (see also **Section 30.2.6**) 00_B $f_{GPT}/4$ 01_B $f_{GPT}/2$ 10_B $f_{GPT}/16$ 11_B $f_{GPT}/8$
T6CLR	14	rw	**Timer T6 Clear Enable Bit** 0_B Timer T6 is not cleared on a capture event 1_B Timer T6 is cleared on a capture event
T6SR	15	rw	**Timer 6 Reload Mode Enable** 0_B Reload from register CAPREL Disabled 1_B Reload from register CAPREL Enabled
0	[31:16], 13	r	**Reserved** Read as 0; should be written with 0.

1) See **Table 30-10** for coding of bits T6UD and T6UDE

Timer T6 Run Control

The core timer T6 can be started or stopped by software through bit T6R (timer T6 run bit). This bit is relevant in all operating modes of T6. Setting bit T6R will start the timer, clearing bit T6R stops the timer.

In Gated Timer Mode, the timer will only run if T6R = 1 and the gate is active (high or low, as programmed).

Note: When bit T5RC in timer control register T5CON is set, bit T6R will also control (start and stop) the Auxiliary Timer T5.

Count Direction Control

The count direction of the GPT2 timers (core timer and auxiliary timer) can be controlled either by software or by the external input pin TxEUD (Timer Tx External Up/Down Control Input). These options are selected by bits TxUD and TxUDE in the respective control register TxCON. When the up/down control is provided by software (bit TxUDE = 0), the count direction can be altered by setting or clearing bit TxUD. When bit TxUDE = 1, pin TxEUD is selected to be the controlling source of the count direction. However, bit TxUD can still be used to reverse the actual count direction, as shown in **Table 30-10**. The count direction can be changed regardless of whether or not the timer is running.

Table 30-10 GPT2 Timer Count Direction Control

Pin TxEUD	Bit TxUDE	Bit TxUD	Count Direction
X	0	0	Count Up
X	0	1	Count Down
0	1	0	Count Up
1	1	0	Count Down
0	1	1	Count Down
1	1	1	Count Up

Timer 6 Output Toggle Latch

The overflow/underflow signal of timer T6 is connected to a block named ‘Toggle Latch’, shown in the timer mode diagrams. **Figure 30-19** illustrates the details of this block. An overflow or underflow of T6 will clock two latches: The first latch represents bit T6OTL in control register T6CON. The second latch is an internal latch toggled by T6OTL’s output. Both latch outputs are connected to the input control block of the auxiliary timer T5. The output level of the shadow latch will match the output level of T6OTL, but is delayed by one clock cycle. When the T6OTL value changes, this will result in a temporarily different output level from T6OTL and the shadow latch, which can trigger the selected count event in T5.

When software writes to T6OTL, both latches are set or cleared simultaneously. In this case, both signals to the auxiliary timers carry the same level and no edge will be detected. Bit T6OE (overflow/underflow output enable) in register T6CON enables the state of T6OTL to be monitored via an external pin T6OUT. When T6OTL is linked to an external port pin (must be configured as output), T6OUT can be used to control external HW. If T6OE = 1, pin T6OUT outputs the state of T6OTL. If T6OE = 0, pin T6OUT outputs a high level (while it selects the timer output signal).

As can be seen from **Figure 30-19**, when latch T6OTL is modified by software to determine the state of the output line, also the internal shadow latch is set or cleared accordingly. Therefore, no trigger condition is detected by T5 in this case.

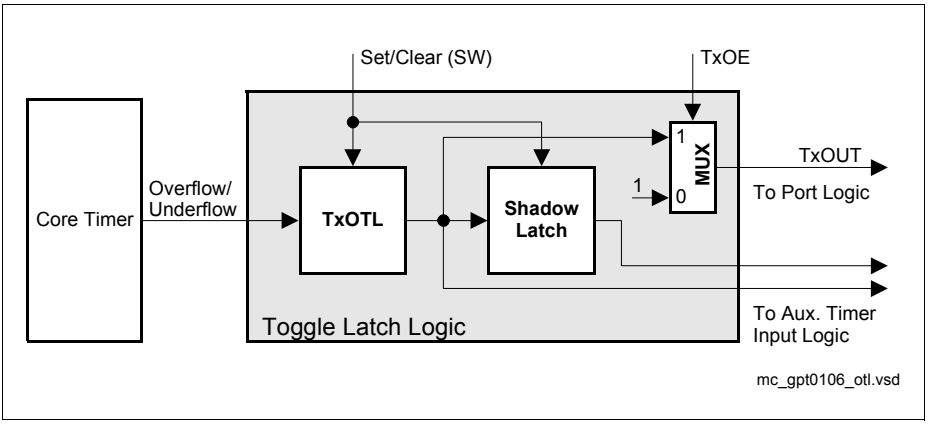


Figure 30-19 Block Diagram of the Toggle Latch Logic of Core Timer T6

30.2.2 GPT2 Core Timer T6 Operating Modes

Timer T6 can operate in one of several modes.

Timer 6 in Timer Mode

Timer Mode for the core timer T6 is selected by setting bitfield T6M in register T6CON to 000_B. In this mode, T6 is clocked with the module's input clock f_{GPT} divided by two programmable prescalers controlled by bitfields BPS2 and T6I in register T6CON. Please see **Section 30.2.6** for details on the input clock options.

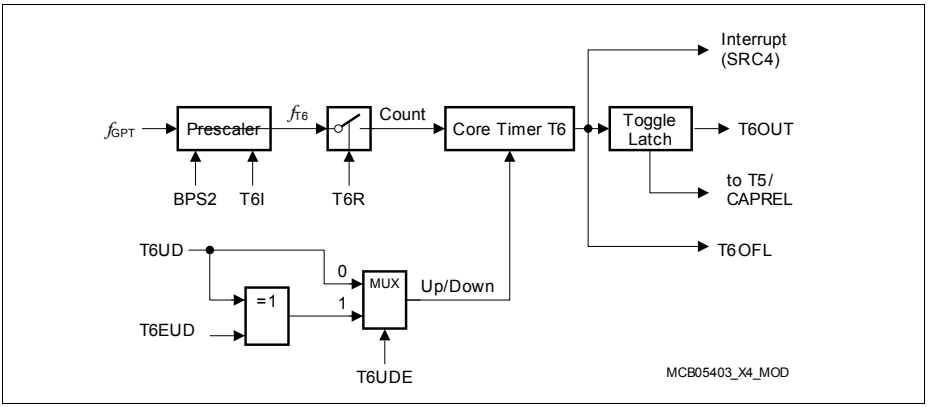


Figure 30-20 Block Diagram of Core Timer T6 in Timer Mode

Gated Timer Mode

Gated Timer Mode for the core timer T6 is selected by setting bitfield T6M in register T6CON to 010_B or 011_B. Bit T6M.0 (T6CON.3) selects the active level of the gate input. The same options for the input frequency are available in Gated Timer Mode as in Timer Mode (see **Section 30.2.6**). However, the input clock to the timer in this mode is gated by the external input pin T6IN (Timer T6 External Input).
To enable this operation, the associated pin T6IN must be configured as input (the corresponding direction control bit must contain 0).

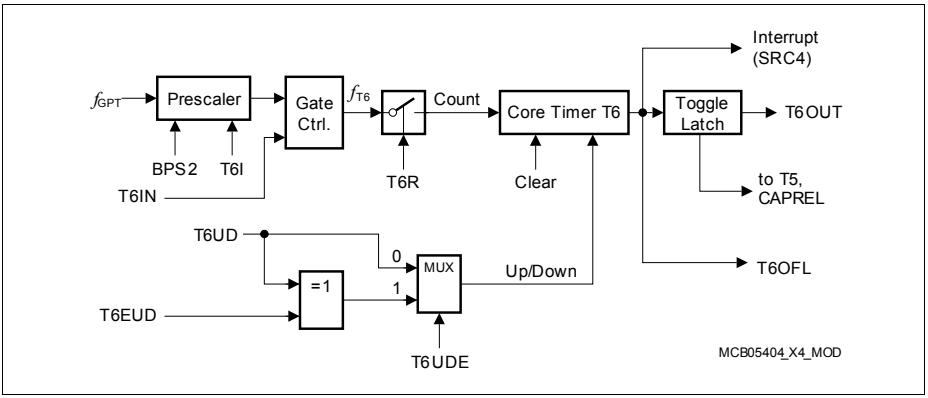


Figure 30-21 Block Diagram of Core Timer T6 in Gated Timer Mode

If T6M = 010_B, the timer is enabled when T6IN shows a low level. A high level at this line stops the timer. If T6M = 011_B, line T6IN must have a high level in order to enable the timer. Additionally, the timer can be turned on or off by software using bit T6R. The timer will only run if T6R is 1 and the gate is active. It will stop if either T6R is 0 or the gate is inactive.

Note: A transition of the gate signal at pin T6IN does not cause an interrupt request.

Counter Mode

Counter Mode for the core timer T6 is selected by setting bitfield T6M in register T6CON to 001_B. In Counter Mode, timer T6 is clocked by a transition at the external input pin T6IN. The event causing an increment or decrement of the timer can be a positive, a negative, or both a positive and a negative transition at this line. Bitfield T6I in control register T6CON selects the triggering transition (see **Table 30-11**).

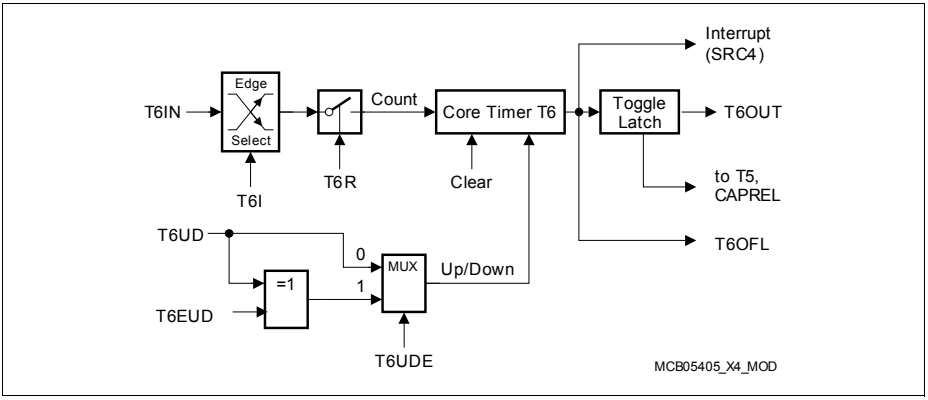


Figure 30-22 Block Diagram of Core Timer T6 in Counter Mode

Table 30-11 GPT2 Core Timer T6 (Counter Mode) Input Edge Selection

T6I	Triggering Edge for Counter Increment/Decrement
000_B	None. Counter T6 is disabled
001_B	Positive transition (rising edge) on T6IN
010_B	Negative transition (falling edge) on T6IN
011_B	Any transition (rising or falling edge) on T6IN
$1XX_B$	Reserved. Do not use this combination

For Counter Mode operation, pin T6IN must be configured as input. The maximum input frequency allowed in Counter Mode depends on the selected prescaler value. To ensure that a transition of the count input signal applied to T6IN is recognized correctly, its level must be held high or low for a minimum number of module clock cycles before it changes. This information can be found in **Section 30.2.6**.

30.2.3 GPT2 Auxiliary Timer T5 Control

Auxiliary timer T5 can be configured for Timer Mode, Gated Timer Mode, or Counter Mode with the same options for the timer frequencies and the count signal as the core timer T6. In addition to these 3 counting modes, the auxiliary timer can be concatenated with the core timer. The contents of T5 may be captured to register CAPREL upon an external or an internal trigger. The start/stop function of the auxiliary timers can be remotely controlled by the T6 run control bit. Several timers may thus be controlled synchronously.

The current contents of the auxiliary timer are reflected by its count register T5. This register can also be written to by the CPU, for example, to set the initial start value.

The individual configurations for timer T5 are determined by its control register T5CON. Some bits in this register also control the function of the CAPREL register. Note that functions which are present in all timers of block GPT2 are controlled in the same bit positions and in the same manner in each of the specific control registers.

Note: The auxiliary timer has no output toggle latch and no alternate output function.

T5CON
Timer 5 Control Register **($1C_H$)** **Reset Value: $0000\ 0000_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
T5 SC	T5 CLR	CI		0	CT3	T5 RC	T5 UDE	T5 UD	T5 R	T5M			T5I		
rw	rwh	rw		rw	rw	rw	rw	rw	rw	rw			rw		

Field	Bits	Type	Description
T5I	[2:0]	rw	**Timer T5 Input Parameter Selection** Depends on the operating mode, see respective sections for encoding: **Table 30-16** for Timer Mode and Gated Timer Mode **Table 30-11** for Counter Mode

Field	Bits	Type	Description
T5M	[5:3]	rw	**Timer T5 Mode Control** (Basic Operating Mode) 000_B Timer Mode 001_B Counter Mode 010_B Gated Timer Mode with gate active low 011_B Gated Timer Mode with gate active high $1xx_B$ Reserved. Do not use this combination
T5R	6	rw	**Timer T5 Run Bit** 0_B Timer T5 stops 1_B Timer T5 runs *Note: This bit only controls timer T5 if bit T5RC = 0.*
T5UD	7	rw	**Timer T5 Up/Down Control**[1)] 0_B Timer T5 counts up 1_B Timer T5 counts down
T5UDE	8	rw	**Timer T5 External Up/Down Enable**[1)] 0_B Input T5EUD is disconnected 1_B Direction influenced by input T5EUD
T5RC	9	rw	**Timer T5 Remote Control** 0_B Timer T5 is controlled by its own run bit T5R 1_B Timer T5 is controlled by the run bit T6R of core timer 6, not by bit T5R
CT3	10	rw	**Timer T3 Capture Trigger Enable** 0_B Capture trigger from input line CAPIN 1_B Capture trigger from T3 input lines T3IN and/or T3EUD
CI	[13:12]	rw	**Register CAPREL Capture Trigger Selection**[2)] 00_B Capture disabled 01_B Positive transition (rising edge) on CAPIN[3)] or any transition on T3IN 10_B Negative transition (falling edge) on CAPIN or any transition on T3EUD 11_B Any transition (rising or falling edge) on CAPIN or any transition on T3IN or T3EUD
T5CLR	14	rw	**Timer T5 Clear Enable Bit** 0_B Timer T5 is not cleared on a capture event 1_B Timer T5 is cleared on a capture event
T5SC	15	rw	**Timer 5 Capture Mode Enable** 0_B Capture into register CAPREL Disabled 1_B Capture into register CAPREL Enabled

Field	Bits	Type	Description
0	11	rw	**Reserved** Have be written with 0.
0	[31:16]	r	**Reserved** Read as 0; should be written with 0.

1) See **Table 30-10** for encoding of bits T5UD and T5UDE.

2) To define the respective trigger source signal, also bit CT3 must be regarded (see **Table 30-14**).

3) Rising edge must be selected if capturing is triggered by the internal GPT1 read signals (see register PISEL and **"Combined Capture Modes" on Page 30-59**).

Timer T5 Run Control

The auxiliary timer T5 can be started or stopped by software in two different ways:

- Through the associated timer run bit (T5R). In this case it is required that the respective control bit T5RC = 0.
- Through the core timer's run bit (T6R). In this case the respective remote control bit must be set (T5RC = 1).

The selected run bit is relevant in all operating modes of T5. Setting the bit will start the timer, clearing the bit stops the timer.

In Gated Timer Mode, the timer will only run if the selected run bit is set and the gate is active (high or low, as programmed).

Note: If remote control is selected T6R will start/stop timer T6 and the auxiliary timer T5 synchronously.

30.2.4 GPT2 Auxiliary Timer T5 Operating Modes

The operation of the auxiliary timer in the basic operating modes is almost identical with the core timer's operation, with very few exceptions. Additionally, some combined operating modes can be selected.

Timer T5 in Timer Mode

Timer Mode for the auxiliary timer T5 is selected by setting its bitfield T5M in register T5CON to 000_B.

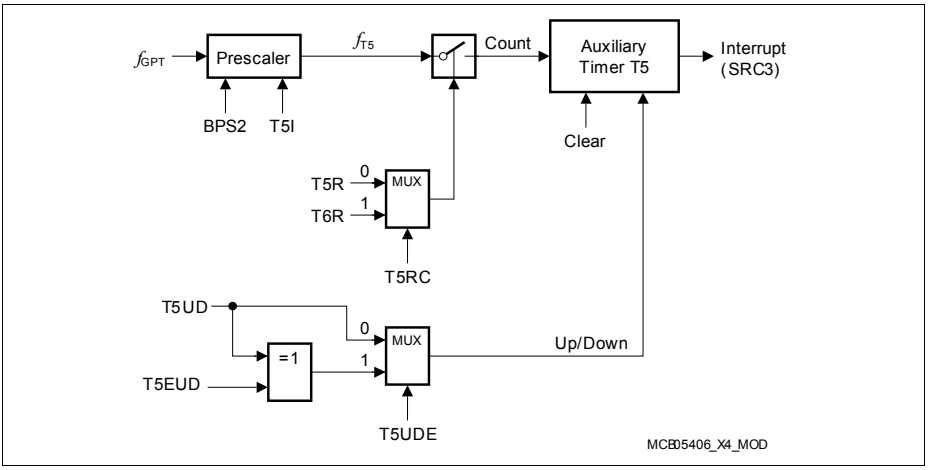


Figure 30-23 Block Diagram of Auxiliary Timer T5 in Timer Mode

Timer T5 in Gated Timer Mode

Gated Timer Mode for the auxiliary timer T5 is selected by setting bitfield T5M in register T5CON to 010_B or 011_B. Bit T5M.0 (T5CON.3) selects the active level of the gate input.

Note: A transition of the gate signal at line T5IN does not cause an interrupt request.

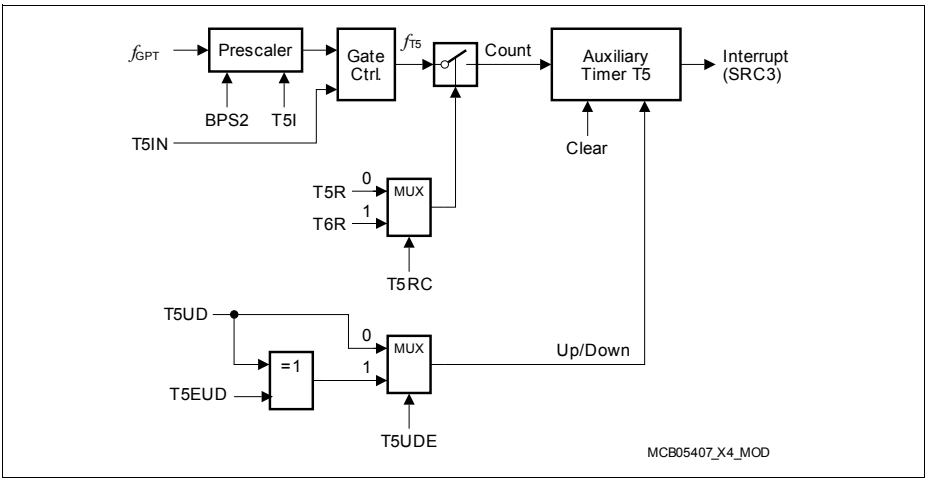


Figure 30-24 Block Diagram of Auxiliary Timer T5 in Gated Timer Mode

Note: There is no output toggle latch for T5.
Start/stop of the auxiliary timer can be controlled locally or remotely.

Timer T5 in Counter Mode

Counter Mode for auxiliary timer T5 is selected by setting bitfield T5M in register T5CON to 001_B. In Counter Mode, the auxiliary timer can be clocked either by a transition at its external input line T5IN, or by a transition of timer T6's toggle latch T6OTL. The event causing an increment or decrement of a timer can be a positive, a negative, or both a positive and a negative transition at either the respective input pin or at the toggle latch. Bitfield T5I in control register T5CON selects the triggering transition (see **Table 30-12**).

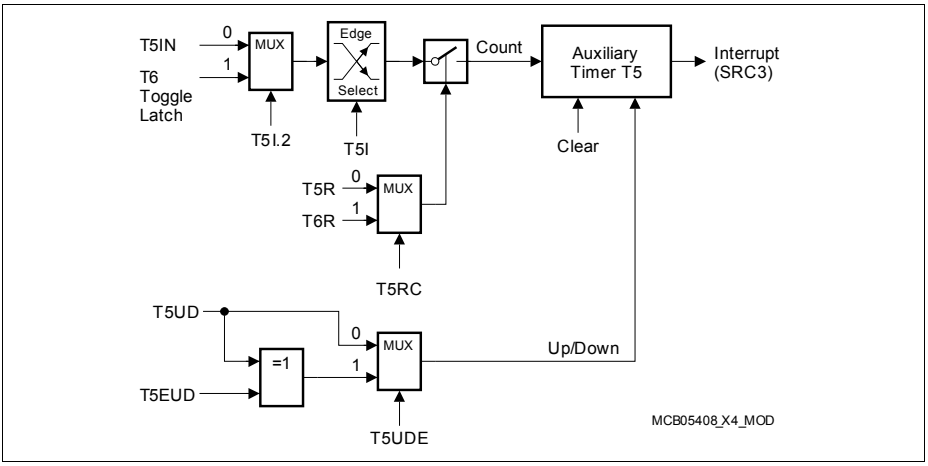


Figure 30-25 Block Diagram of Auxiliary Timer T5 in Counter Mode

Table 30-12 GPT2 Auxiliary Timer (Counter Mode) Input Edge Selection

T5I	Triggering Edge for Counter Increment/Decrement
$X00_B$	None. Counter T5 is disabled
001_B	Positive transition (rising edge) on T5IN
010_B	Negative transition (falling edge) on T5IN
011_B	Any transition (rising or falling edge) on T5IN
101_B	Positive transition (rising edge) of T6 toggle latch T6OTL
110_B	Negative transition (falling edge) of T6 toggle latch T6OTL
111_B	Any transition (rising or falling edge) of T6 toggle latch T6OTL

Note: Only state transitions of T6OTL which are caused by the overflows/underflows of T6 will trigger the counter function of T5. Modifications of T6OTL via software will NOT trigger the counter function of T5.

For counter operation, pin T5IN must be configured as input (the respective direction control bit DPx.y must be 0). The maximum input frequency allowed in Counter Mode depends on the selected prescaler value. To ensure that a transition of the count input signal applied to T5IN is recognized correctly, its level must be held high or low for a minimum number of module clock cycles before it changes. This information can be found in **Section 30.2.6**.

Timer Concatenation

Using the toggle bit T6OTL as a clock source for the auxiliary timer in Counter Mode concatenates the core timer T6 with the auxiliary timer T5. This concatenation forms either a 32-bit or a 33-bit timer/counter, depending on which transition of T6OTL is selected to clock the auxiliary timer.

- **32-bit Timer/Counter:** If both a positive and a negative transition of T6OTL are used to clock the auxiliary timer, this timer is clocked on every overflow/underflow of the core timer T6. Thus, the two timers form a 32-bit timer.
- **33-bit Timer/Counter:** If either a positive or a negative transition of T6OTL is selected to clock the auxiliary timer, this timer is clocked on every second overflow/underflow of the core timer T6. This configuration forms a 33-bit timer (16-bit core timer + T6OTL + 16-bit auxiliary timer).
  As long as bit T6OTL is not modified by software, it represents the state of the internal toggle latch, and can be regarded as part of the 33-bit timer.

The count directions of the two concatenated timers are not required to be the same. This offers a wide variety of different configurations.

T6, which represents the low-order part of the concatenated timer, can operate in Timer Mode, Gated Timer Mode or Counter Mode in this case.

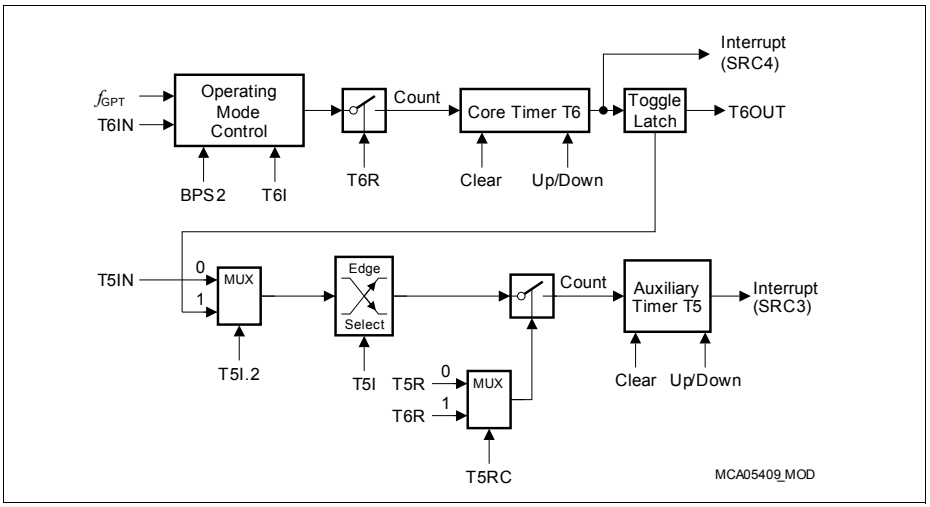


Figure 30-26 Concatenation of Core Timer T6 and Auxiliary Timer T5

When reading the low and high parts of the concatenated timer, care must be taken to obtain consistent values in particular after a timer overflow/underflow (e.g. one part may already have considered an overflow, while the other has not).

Note: This is a general issue when reading multi-word results with consecutive instructions, and not necessarily unique to the GPT12 module architecture.

The following algorithm may be used to read concatenated GPT1 timers, represented by TIMER_HIGH (for auxiliary timer, here T5) and TIMER_LOW (for core timer T6). The high part is read twice, and reading of the low part is repeated if two different values were read for the high part:

- TIMER_HIGH_TMP = T5
- TIMER_LOW = T6
- Wait two basic clock cycles (to allow increment/decrement of auxiliary timer in case of core timer overflow/underflow) - see **Table 30-13**
- TIMER_HIGH = T5
- If TIMER_HIGH is not equal to TIMER_HIGH_TMP then TIMER_LOW = T6

After execution of this algorithm, TIMER_HIGH and TIMER_LOW represent a consistent time stamp of the concatenated timers.

The equivalent number of system clock cycles corresponding to two basic clock cycles is shown in **Table 30-13**.

Table 30-13 Number of System Clock Cycles to Wait for Two Basic Clock Cycles

Block Prescaler	BPS2 = 01_B	BPS2 = 00_B	BPS2 = 11_B	BPS2 = 10_B
Number of system clocks	4	8	16	32

In case the required timer resolution can be achieved with different combinations of the Block Prescaler BPS2 and the Individual Prescalers TxI, the variant with the smallest value for the Block Prescaler may be chosen to minimize the waiting time. E.g. in order to run T6 at f_{FPI}/512, select BPS2 = 00_B, T6I = 111_B, and insert 8 NOPs (or other instructions) to ensure the required waiting time before reading TIMER_HIGH the second time.

30.2.5 GPT2 Register CAPREL Operating Modes

The Capture/Reload register CAPREL can be used to capture the contents of timer T5, or to reload timer T6. A special mode facilitates the use of register CAPREL for both functions at the same time. This mode allows frequency multiplication. The capture function is triggered by the input pin CAPIN, by GPT1 timer's T3 input lines T3IN and T3EUD, or by read accesses to GPT1 timers. The reload function is triggered by an overflow or underflow of timer T6.

In addition to the capture function, the capture trigger signal can also be used to clear the contents of timers T5 and T6 individually.

The functions of register CAPREL are controlled via several bit(field)s in the timer control registers T5CON and T6CON.

GPT2 Capture/Reload Register CAPREL in Capture Mode

Capture Mode for register CAPREL is selected by setting bit T5SC in control register T5CON (set bitfield CI in register T5CON to a non-zero value to select a trigger signal). In Capture Mode, the contents of the auxiliary timer T5 are latched into register CAPREL in response to a signal transition at the selected external input pin(s). Bit CT3 selects the external input line CAPIN or the input lines T3IN and/or T3EUD of GPT1 timer T3 as the source for a capture trigger. Either a positive, a negative, or both a positive and a negative transition at line CAPIN can be selected to trigger the capture function, or transitions on input T3IN or input T3EUD or both inputs, T3IN and T3EUD. The active edge is controlled by bitfield CI in register T5CON. **Table 30-14** summarizes these options.

Table 30-14 CAPREL Register Input Edge Selection

CT3	CI	Triggering Signal/Edge for Capture Mode
X	00_B	None. Capture Mode is disabled.
0	01_B	Positive transition (rising edge) on CAPIN.[1)]
0	10_B	Negative transition (falling edge) on CAPIN.
0	11_B	Any transition (rising or falling edge) on CAPIN.
1	01_B	Any transition (rising or falling edge) on T3IN.
1	10_B	Any transition (rising or falling edge) on T3EUD.
1	11_B	Any transition (rising or falling edge) on T3IN or T3EUD.

1) Rising edge must be selected if capturing is triggered by the internal GPT1 read signals (see register PISEL and **"Combined Capture Modes" on Page 30-59**).

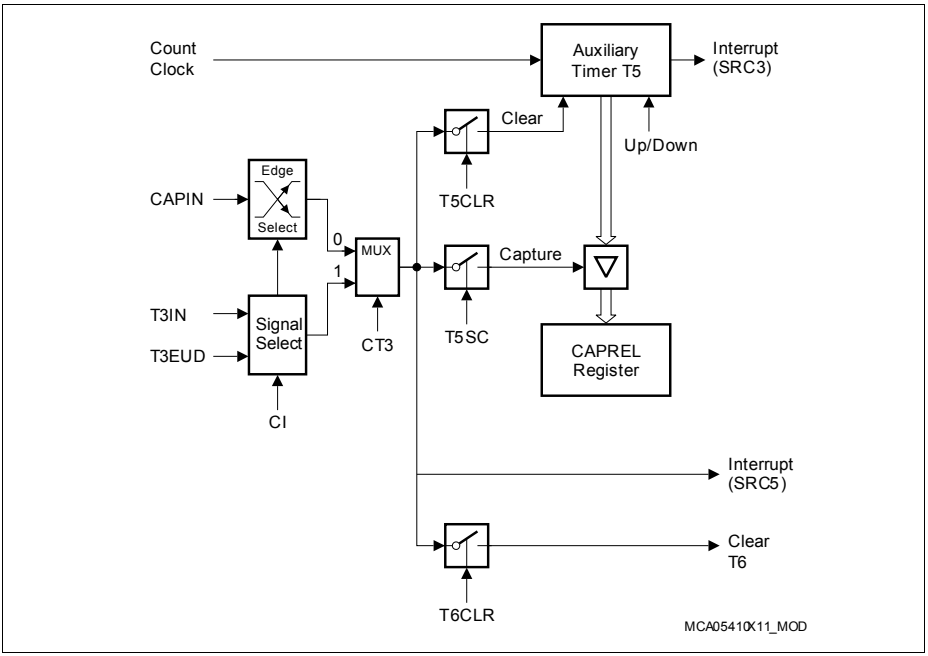


Figure 30-27 GPT2 Register CAPREL in Capture Mode

When a selected trigger is detected, the contents of the auxiliary timer T5 are latched into register CAPREL and the interrupt request is activated. The same event can optionally clear timer T5 and/or timer T6. This option is enabled by bit T5CLR in register T5CON and bit T6CLR in register T6CON, respectively. If TxCLR = 0 the contents of timer Tx is not affected by a capture. If TxCLR = 1 timer Tx is cleared after the current timer T5 value has been latched into register CAPREL.

Note: Bit T5SC only controls whether or not a capture is performed. If T5SC is cleared the external input pin(s) can still be used to clear timer T5 and/or T6, or as external interrupt input(s). This interrupt is controlled by the CAPREL interrupt control register SRC5.

When capture triggers T3IN or T3EUD are enabled (CT3 = 1), register CAPREL captures the contents of T5 upon transitions of the selected input(s). These values can be used to measure T3's input signals. This is useful, for example, when T3 operates in Incremental Interface Mode, in order to derive dynamic information (speed, acceleration) from the input signals.

For Capture Mode operation, the selected pins CAPIN, T3IN, or T3EUD must be configured as input. To ensure that a transition of a trigger input signal applied to one of

these inputs is recognized correctly, its level must be held high or low for a minimum number of module clock cycles, detailed in **Section 30.2.6**.

GPT2 Capture/Reload Register CAPREL in Reload Mode

Reload Mode for register CAPREL is selected by setting bit T6SR in control register T6CON. In Reload Mode, the core timer T6 is reloaded with the contents of register CAPREL, triggered by an overflow or underflow of T6. This will not activate the interrupt request SRC5.SRR associated with the CAPREL register. However, an interrupt request will be activated, indicating the overflow/underflow of T6.

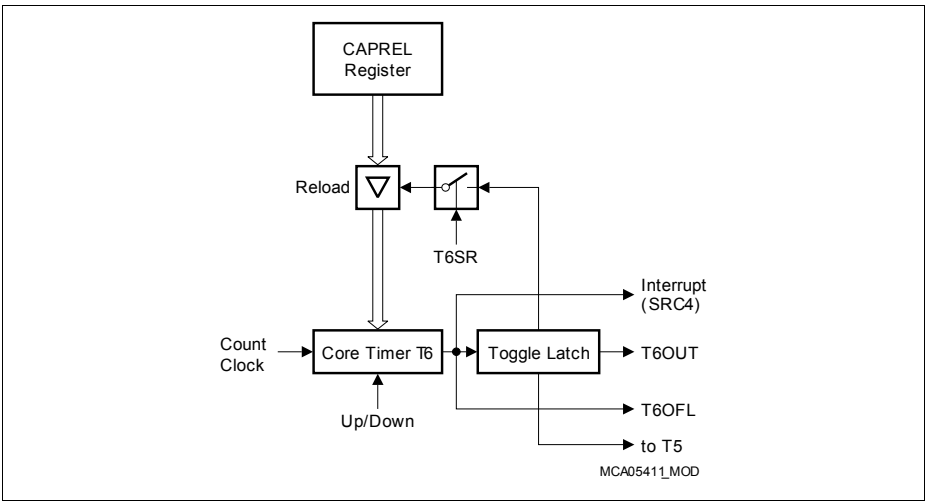


Figure 30-28 GPT2 Register CAPREL in Reload Mode

GPT2 Capture/Reload Register CAPREL in Capture-And-Reload Mode

Since the reload function and the capture function of register CAPREL can be enabled individually by bits T5SC and T6SR, the two functions can be enabled simultaneously by setting both bits. This feature can be used to generate an output frequency that is a multiple of the input frequency.

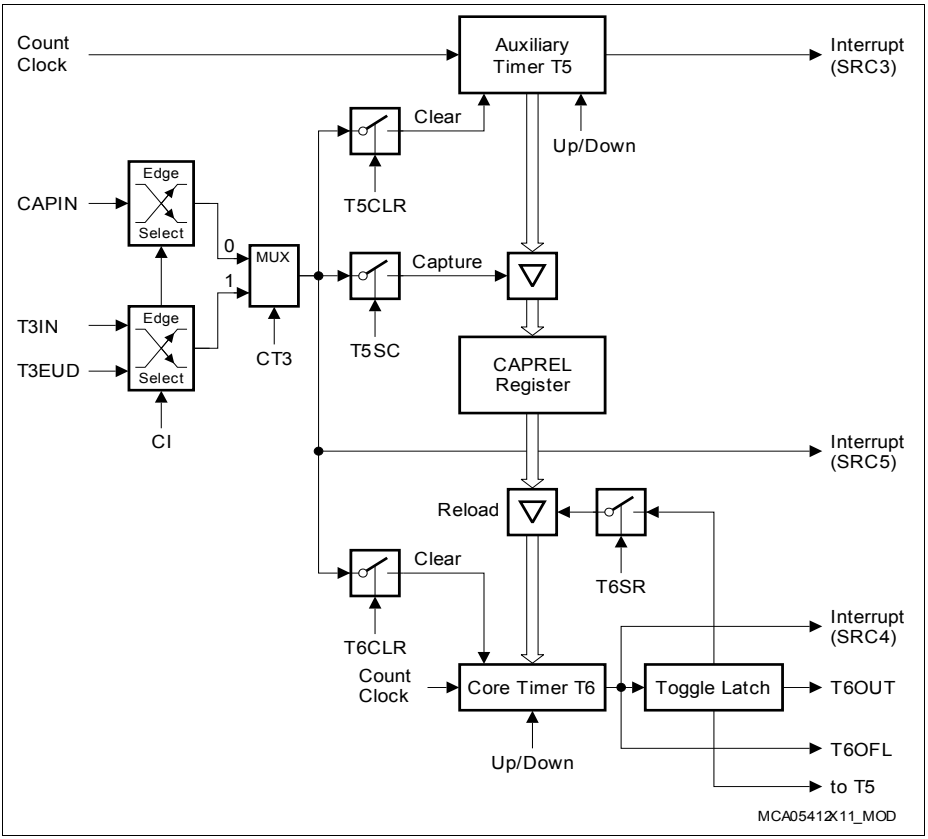


Figure 30-29 GPT2 Register CAPREL in Capture-And-Reload Mode

This combined mode can be used to detect consecutive external events which may occur aperiodically, but where a finer resolution, that means, more ‘ticks’ within the time between two external events is required.

For this purpose, the time between the external events is measured using timer T5 and the CAPREL register. Timer T5 runs in Timer Mode counting up with a frequency of e.g. $f_{GPT}/32$. The external events are applied to pin CAPIN. When an external event occurs,

the contents of timer T5 are latched into register CAPREL and timer T5 is cleared (T5CLR = 1). Thus, register CAPREL always contains the correct time between two events, measured in timer T5 increments. Timer T6, which runs in Timer Mode counting down with a frequency of e.g. $f_{GPT}/4$, uses the value in register CAPREL to perform a reload on underflow. This means, the value in register CAPREL represents the time between two underflows of timer T6, now measured in timer T6 increments. Since (in this example) timer T6 runs 8 times faster than timer T5, it will underflow 8 times within the time between two external events. Thus, the underflow signal of timer T6 generates 8 'ticks'. Upon each underflow, the interrupt request SRC4.SRR will be activated and bit T6OTL will be toggled. The state of T6OTL may be output on pin T6OUT. This signal has 8 times more transitions than the signal which is applied to pin CAPIN.

Capture Correction

A certain deviation of the output frequency is generated by the fact that timer T5 will count actual time units (e.g. T5 running at 1 MHz will count up to the value $64_H/100_D$ for a 10 kHz input signal), while T6OTL will only toggle upon an underflow of T6 (i.e. the transition from 0000_H to $FFFF_H$). In the above mentioned example, T6 would count down from 64_H, so the underflow would occur after 101 timing ticks of T6. The actual output frequency then is 79.2 kHz, instead of the expected 80 kHz.

Another possibility is to use T6 overflows. In this case, T5 counts down and T6 counts up. Upon a signal transition on pin CAPIN, the count value in T5 is captured into CAPREL and T5 is cleared to 0000_H. In its next clock cycle, T5 underflows to $FFFF_H$, and continues to count down with the following clocks. T6 is reloaded from CAPREL upon an overflow, and continues to count up with its following clock cycles (8 times faster in the above example). In this case, T5 and T6 count the same number of steps with their respective internal count frequency.

In the above example, T5 running at 1 MHz will count down to the value $FF9C_H/-100_D$ for a 10 kHz input signal applied at CAPIN, while T6 counts up from $FF9C_H$ through $FFFF_H$ to 0000_H. So the overflow occurs after 100 timing ticks of T6, and the actual output frequency at T6OUT then is the expected 80 kHz.

However, in this case CAPREL does not directly contain the time between two CAPIN events, but rather its 2's complement. Software will have to convert this value, if it is required for the operation.

Combined Capture Modes

For incremental interface applications in particular, several timer features can be combined to obtain dynamic information such as speed, acceleration, or deceleration. The current position itself can be obtained directly from the timer register (T2, T3, T4).

The time information to determine the dynamic parameters is generated by capturing the contents of the free-running timer T5 into register CAPREL. Two trigger sources for this event can be selected:

- Capture trigger on sensor signal transitions
- Capture trigger on position read operations

Capturing on sensor signal transitions is available for timer T3 inputs. This mode is selected by setting bit CT3 and selecting the intended signal(s) via bitfield CI in register T5CON. CAPREL then indicates the time between two selected transitions (measured in T5 counts).

Capturing on position read operations is available for timers T2, T3, and T4. This mode is selected by clearing bit CT3 and selecting the rising edge via bitfield CI in register T5CON. Bitfield ISCAPIN in register PISEL then selects either a read access from T3 or a read access from any of T2 or T3 or T4. CAPREL then indicates the time between two read accesses.

These operating modes directly support the measurement of position and rotational speed. Acceleration and deceleration can then be determined by evaluating subsequent speed measurements.

30.2.6 GPT2 Clock Signal Control

All actions within the timer block GPT2 are triggered by transitions of its basic clock. This basic clock is derived from the system clock by a basic block prescaler, controlled by bitfield BPS2 in register T6CON (see **Figure 30-18**). The count clock can be generated in two different ways:

- **Internal count clock**, derived from GPT2's basic clock via a programmable prescaler, is used for (Gated) Timer Mode.
- **External count clock**, derived from the timer's input pin(s), is used for Counter Mode.

For both ways, the basic clock determines the maximum count frequency and the timer's resolution:

Table 30-15 Basic Clock Selection for Block GPT2

Block Prescaler[1]	BPS2 = 01_B	BPS2 = 00_B[2]	BPS2 = 11_B	BPS2 = 10_B
Prescaling Factor for GPT2: F(BPS2)	F(BPS2) = 2	F(BPS2) = 4	F(BPS2) = 8	F(BPS2) = 16
Maximum External Count Frequency	$f_{GPT}/4$	$f_{GPT}/8$	$f_{GPT}/16$	$f_{GPT}/32$
Input Signal Stable Time	$2 \times t_{GPT}$	$4 \times t_{GPT}$	$8 \times t_{GPT}$	$16 \times t_{GPT}$

1) Please note the non-linear encoding of bitfield BPS2.

2) Default after reset.

Internal Count Clock Generation

In Timer Mode and Gated Timer Mode, the count clock for each GPT2 timer is derived from the GPT2 basic clock by a programmable prescaler, controlled by bitfield TxI in the respective timer's control register TxCON.

The count frequency f_{Tx} for a timer Tx and its resolution r_{Tx} are scaled linearly with lower clock frequencies, as can be seen from the following formula:

$$f_{Tx} = \frac{f_{GPT}}{F(BPS2) \times 2^{<TxI>}} \qquad r_{Tx}[\mu s] = \frac{F(BPS2) \times 2^{<TxI>}}{f_{GPT}[MHz]} \tag{30.2}$$

The effective count frequency depends on the common module clock prescaler factor F(BPS2) as well as on the individual input prescaler factor $2^{<TxI>}$. **Table 30-16** summarizes the resulting overall divider factors for a GPT2 timer that result from these cascaded prescalers.

Table 30-16 GPT2 Overall Prescaler Factors for Internal Count Clock

Individual Prescaler for Tx	Common Prescaler for Module Clock[1]			
	BPS2 = 01_B	BPS2 = 00_B	BPS2 = 11_B	BPS2 = 10_B
TxI = 000_B	2	4	8	16
TxI = 001_B	4	8	16	32
TxI = 010_B	8	16	32	64
TxI = 011_B	16	32	64	128
TxI = 100_B	32	64	128	256
TxI = 101_B	64	128	256	512
TxI = 110_B	128	256	512	1024
TxI = 111_B	256	512	1024	2048

1) Please note the non-linear encoding of bitfield BPS2.

Table 30-17 lists a timer's parameters (such as count frequency, resolution, and period) resulting from the selected overall prescaler factor and the applied system frequency. Note that some numbers may be rounded.

Table 30-17 GPT2 Timer Parameters

FPI_Bus Clock = 10 MHz			Overall Divider Factor	FPI_Bus Clock = 40 MHz		
Frequency	Resolution	Period		Frequency	Resolution	Period
5.0 MHz	200 ns	13.11 ms	2	20.0 MHz	50 ns	3.28 ms
2.5 MHz	400 ns	26.21 ms	4	10.0 MHz	100 ns	6.55 ms
1.25 MHz	800 ns	52.43 ms	8	5.0 MHz	200 ns	13.11 ms
625.0 kHz	1.6 µs	104.9 ms	16	2.5 MHz	400 ns	26.21 ms
312.5 kHz	3.2 µs	209.7 ms	32	1.25 MHz	800 ns	52.43 ms
156.25 kHz	6.4 µs	419.4 ms	64	625.0 kHz	1.6 µs	104.9 ms
78.125 kHz	12.8 µs	838.9 ms	128	312.5 kHz	3.2 µs	209.7 ms
39.06 kHz	25.6 µs	1.678 s	256	156.25 kHz	6.4 µs	419.4 ms
19.53 kHz	51.2 µs	3.355 s	512	78.125 kHz	12.8 µs	838.9 ms
9.77 kHz	102.4 µs	6.711 s	1024	39.06 kHz	25.6 µs	1.678 s
4.88 kHz	204.8 µs	13.42 s	2048	19.53 kHz	51.2 µs	3.355 s

External Count Clock Input

The external input signals of the GPT2 block are sampled with the GPT2 basic clock (see **Figure 30-18**). To ensure that a signal is recognized correctly, its current level (high or low) must be held active for at least one complete sampling period, before changing. A signal transition is recognized if two subsequent samples of the input signal represent different levels. Therefore, a minimum of two basic clock periods are required for the sampling of an external input signal. Thus, the maximum frequency of an input signal must not be higher than half the basic clock.

Table 30-18 summarizes the resulting requirements for external GPT2 input signals.

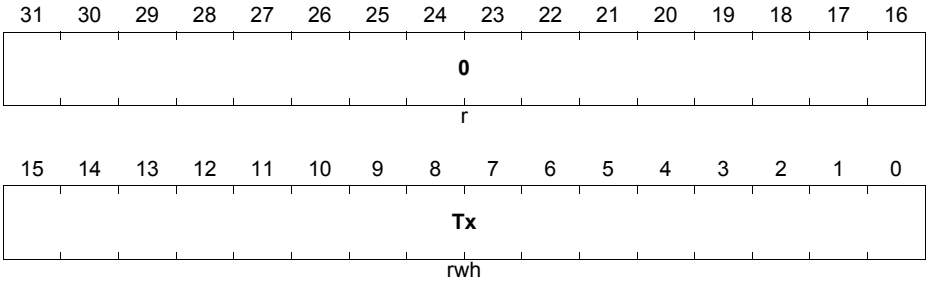
Table 30-18 GPT2 External Input Signal Limits

FPI_Bus Clock = 10 MHz		Input Frequ. Factor	GPT2 Divider BPS2	Input Phase Duration	FPI_Bus Clock = 40 MHz	
Max. Input Frequency	Min. Level Hold Time				Max. Input Frequency	Min. Level Hold Time
2.5 MHz	200 ns	$f_{GPT}/4$	01_B	$2 \times t_{GPT}$	10.0 MHz	50 ns
1.25 MHz	400 ns	$f_{GPT}/8$	00_B	$4 \times t_{GPT}$	5.0 MHz	100 ns
625.0 kHz	800 ns	$f_{GPT}/16$	11_B	$8 \times t_{GPT}$	2.5 MHz	200 ns
312.5 kHz	1.6 µs	$f_{GPT}/32$	10_B	$16 \times t_{GPT}$	1.25 MHz	400 ns

These limitations are valid for all external input signals to GPT2, including the external count signals in Counter Mode and the gate input signals in Gated Timer Mode.

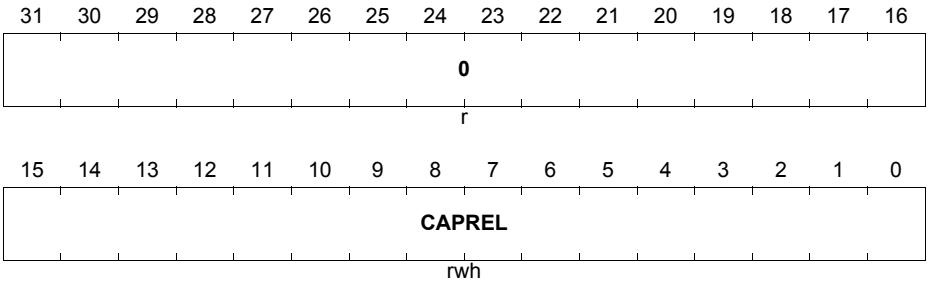
30.2.7 GPT2 Timer Registers

T5
Timer 5 Register **(40_H)** **Reset Value: 0000 0000$_H$**
T6
Timer 6 Register **(44_H)** **Reset Value: 0000 0000$_H$**



Field	Bits	Type	Description
Tx	[15:0]	rwh	**Timer x** Contains the current value of Timer x.
0	[31:16]	r	**Reserved** Read as 0; should be written with 0.

CAPREL
Capture and Reload Register **(30_H)** **Reset Value: 0000 0000$_H$**



Field	Bits	Type	Description
CAPREL	[15:0]	rwh	**Current reload value or Captured value**

Field	Bits	Type	Description
0	[31:16]	r	**Reserved** Read as 0; should be written with 0.

30.2.8 Interrupt Control for GPT2 Timers and CAPREL

When a timer overflows from $FFFF_H$ to 0000_H (when counting up), or when it underflows from 0000_H to $FFFF_H$ (when counting down), its service request flag (SRR) in register SRCx will be set. Whenever a transition according to the selection in bit field CI is detected at pin CAPIN, interrupt request flag SRR in register SRC5 is set.

Interrupts of timer 5 are connected with register SRC3.

Interrupts of timer 6 are connected with register SRC4.

Interrupts of the CAPREL function are connected with register SRC5.

SRC3
Service Request Control 3 Register ($F0_H$) Reset Value: 0000 0000_H

SRC4
Service Request Control 4Register (EC_H) Reset Value: 0000 0000_H

SRC5
Service Request Control 5 Register ($E8_H$) Reset Value: 0000 0000_H

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

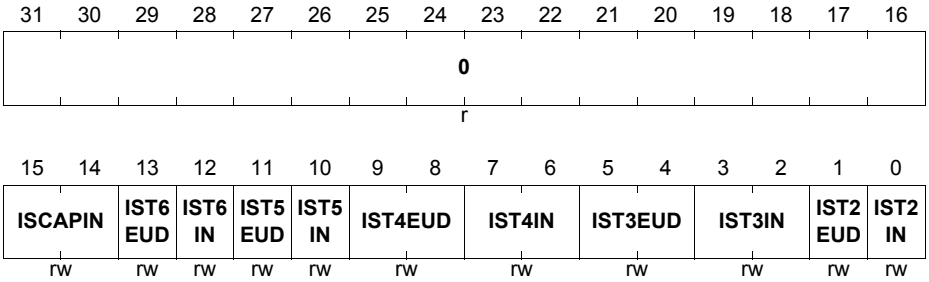
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SETR	CLRR	SRR	SRE	0	TOS	0		SRPN							
w	w	rh	rw	r	rw	r		rw							

Field	Bits	Type	Description
SRPN	[7:0]	rw	**Service Request Priority Number** 00_H Service request is never serviced 01_H Service request is on lowest priority ... FF_H Service request is on highest priority
TOS	10	rw	**Type of Service Control** 0_B CPU service is initiated 1_B PCP service is initiated
SRE	12	rw	**Service Request Enable** 0_B Service request is disabled 1_B Service request is enabled

Field	Bits	Type	Description
SRR	13	rh	**Service Request Flag** 0_B No service request is pending 1_B A service request is pending
CLRR	14	w	**Request Clear Bit** CLRR is required to clear SRR. 0_B No action 1_B Clear SRR; bit value is not stored; read always returns 0; no action if SETR is set also.
SETR	15	w	**Request Set Bit** SETR is required to set SRR. 0_B No action 1_B Set SRR; bit value is not stored; read always returns 0; no action if CLRR is set also.
0	[9:8], 11, [31:16]	r	**Reserved** Read as 0; should be written with 0.

30.3 Miscellaneous Registers

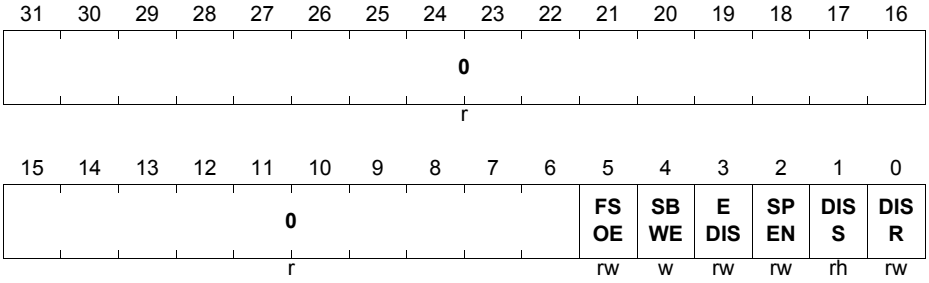
PISEL
Port Input Select Register **(04_H)** **Reset Value: 0000 0000_H**



Field	Bits	Type	Description
IST2IN	0	rw	**Input Select for T2IN** 0_B Signal T2INA is selected 1_B Signal T2INB is selected
IST2EUD	1	rw	**Input Select for T2EUD** 0_B Signal T2EUDA is selected 1_B Signal T2EUDB is selected
IST3IN	[3:2]	rw	**Input Select for T3IN** 00_B Signal T3INA is selected 01_B Signal T3INB is selected 10_B Signal T3INC is selected 11_B Signal T3IND is selected
IST3EUD	[5:4]	rw	**Input Select for T3EUD** 00_B Signal T3EUDA is selected 01_B Signal T3EUDB is selected 10_B Signal T3EUDC is selected 11_B Signal T3EUDD is selected
IST4IN	[7:6]	rw	**Input Select for T4IN** 00_B Signal T4INA is selected 01_B Signal T4INB is selected 10_B Signal T4INC is selected 11_B Signal T4IND is selected

Field	Bits	Type	Description
IST4EUD	[9:8]	rw	**Input Select for T4EUD** 00_B Signal T4EUDA is selected 01_B Signal T4EUDB is selected 10_B Signal T4EUDC is selected 11_B Signal T4EUDD is selected
IST5IN	10	rw	**Input Select for T5IN** 0_B Signal T5INA is selected 1_B Signal T5INB is selected
IST5EUD	11	rw	**Input Select for T5EUD** 0_B Signal T5EUDA is selected 1_B Signal T5EUDB is selected
IST6IN	12	rw	**Input Select for T6IN** 0_B Signal T6INA is selected 1_B Signal T6INB is selected
IST6EUD	13	rw	**Input Select for T6EUD** 0_B Signal T6EUDA is selected 1_B Signal T6EUDB is selected
ISCAPIN	[15:14]	rw	**Input Select for CAPIN** 00_B Signal CAPINA is selected 01_B Signal CAPINB is selected 10_B Signal CAPINC (Read trigger from T3) is selected 11_B Signal CAPIND (Read trigger from T2 or T3 or T4) is selected
0	[31:16]	r	**Reserved** Read as 0; should be written with 0.

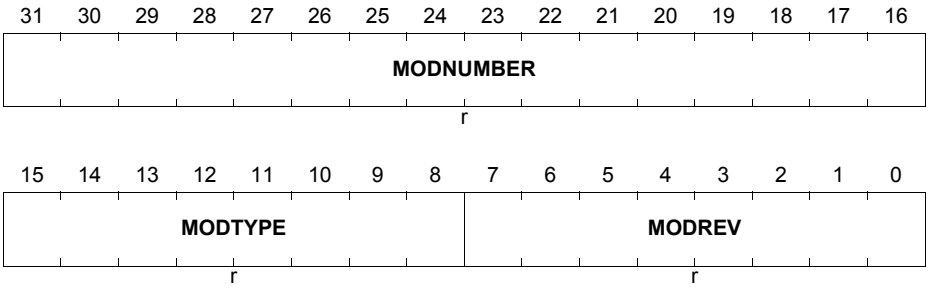
CLC
Clock Control Register **(00_H)** **Reset Value: 0000 0003$_H$**



Field	Bits	Type	Description
DISR	0	rw	**Module Disable Request Bit** Used for enable/disable control of the module. 0_B Module disable is not requested 1_B Module disable is requested
DISS	1	rh	**Module Disable Status Bit** Bit indicates the current status of the module 0_B Module is enabled 1_B Module is disabled If the RMC field is implemented and if it is 0, DISS is set automatically.
SPEN	2	rw	**Module Suspend Enable** Used for enabling the Suspend Mode. 0_B Module cannot be suspended (suspend is disabled) 1_B Module can be suspended (suspend is enabled) This bit can be written only if SBWE is set during the same write operation.
EDIS	3	rw	**Sleep Mode Enable Control** Used for module Sleep Mode control. 0_B Sleep Mode request is regarded. Module is enabled to go into Sleep Mode. 1_B Sleep Mode request is disregarded: Sleep Mode cannot be entered on a request.

Field	Bits	Type	Description
SBWE	4	w	**Module Suspend Bit Write Enable for OCDS** Determines whether SPEN and FSOE are write-protected. 0_B Bits SPEN and FSOE are write-protected 1_B Bits SPEN and FSOE are overwritten by respective value of SPEN or FSOE Reading this bit returns always 0.
FSOE	5	rw	**Fast Switch Off Enable** Used for fast clock switch-off in Suspend Mode. 0_B Clock switch-off in Suspend Mode via Disable Control Feature (Secure Clock Switch Off) selected 1_B Fast clock switch off in Suspend Mode selected This bit can be written only if SBWE is set during the same write operation.
0	[31:6]	r	**Reserved** Read as 0; should be written with 0.

ID
Identification Register **(08_H)** **Reset Value: 0068 C0XX$_H$**



Field	Bits	Type	Description
MODREV	[7:0]	r	**Module Revision Number** This bit field indicates the revision number of the TC1798 module (01_H = first revision).
MODTYPE	[15:8]	r	**Module Type** This bit field is $C0_H$. It defines a 32-bit module

Field	Bits	Type	Description
MODNUMBER	[31:16]	r	**Module Number** This bit field defines the module identification number.

30.4 GPT12 Kernel Register Overview

Table 30-19 Register Overview of GPT12

Short Name	Long Name	Offset Addr.[1)]	Access Mode		Reset	Description See
			Read	Write		
CLC	Clock Control Register	00_H	U, SV	SV, E	Application Reset	Page 30-70
PISEL	Port Input Select Register	04_H	U, SV	U, SV	Application Reset	Page 30-68
ID	Identification Register	08_H	U, SV	BE	Application Reset	Page 30-71
–	Reserved	$0C_H$	BE	BE	–	–
T2CON	Timer 2 Control Register	10_H	U, SV	U, SV	Application Reset	Page 30-15
T3CON	Timer 3 Control Register	14_H	U, SV	U, SV	Application Reset	Page 30-4
T4CON	Timer 4 Control Register	18_H	U, SV	U, SV	Application Reset	Page 30-17
T5CON	Timer 5 Control Register	1C	U, SV	U, SV	Application Reset	Page 30-46
T6CON	Timer 6 Control Register	20_H	U, SV	U, SV	Application Reset	Page 30-39
–	Reserved	24_H-$2C_H$	BE	BE	–	–
CAPREL	Capture and Reload Register	30_H	U, SV	U, SV	Application Reset	Page 30-64
T2	Timer 2 Register	34_H	U, SV	U, SV	Application Reset	Page 30-34
T3	Timer 3 Register	38_H	U, SV	U, SV	Application Reset	Page 30-34

Table 30-19 Register Overview of GPT12

Short Name	Long Name	Offset Addr.[1]	Access Mode		Reset	Description See
			Read	Write		
T4	Timer 4 Register	$3C_H$	U, SV	U, SV	Application Reset	Page 30-34
T5	Timer 5 Register	40_H	U, SV	U, SV	Application Reset	Page 30-64
T6	Timer 6 Register	44_H	U, SV	U, SV	Application Reset	Page 30-64
–	Reserved	48_H - $E4_H$	BE	BE	–	–
SRC5	Service Request Control Register 5	$E8_H$	U, SV	SV	Application Reset	Page 30-66
SRC4	Service Request Control Register 4	EC_H	U, SV	SV	Application Reset	Page 30-66
SRC3	Service Request Control Register 3	$F0_H$	U, SV	SV	Application Reset	Page 30-66
SRC2	Service Request Control Register 2	$F4_H$	U, SV	SV	Application Reset	Page 30-35
SRC1	Service Request Control Register 1	$F8_H$	U, SV	SV	Application Reset	Page 30-35
SRC0	Service Request Control Register 0	FC_H	U, SV	SV	Application Reset	Page 30-35

1) The absolute register address is calculated as follows:
Module Base Address + Offset Address (shown in this column)

30.5 Implementation of the GPT12 Modules

This chapter describes the implementation of the GPT12 modules in the TC1798 device.

30.5.1 Address Map

There are two GPT12 kernels in the TC1798, namely GPT120 and GPT121.

Table 30-20 Registers Address Space

Module	Base Address	End Address	Note
GPT120	$F000\ 3400_H$	$F000\ 34FF_H$	
GPT121	$F000\ 3500_H$	$F000\ 35FF_H$	

30.5.2 Module Connections

The following tables show the digital connections of the GPT12 modules with other modules or pins in the TC1798 device.
The GPT module is clocked with the FPI_Bus clock, so $f_{GPT} = f_{FPI}$.

Table 30-21 GPT120 Digital Connections in TC1798

Signal	from/to Module	I/O to GPT12	Can be used to/as
T2INA	P4.10	I	count input signals for timer T2
T2INB	P3.14	I	
T2EUDA	P4.12	I	direction input signals for timer T2
T2EUDB	P5.4	I	
T3INA	P2.14	I	count input signals for timer T3
T3INB	P3.8	I	
T3INC	P14.14	I	
T3IND	0	I	
T3EUDA	P4.8	I	direction input signals for timer T3
T3EUDB	P3.10	I	
T3EUDC	P14.15	I	
T3EUDD	0	I	
T3OUT	P1.7 P14.8	O	count output signal for timer T3

Table 30-21 GPT120 Digital Connections in TC1798 (cont'd)

Signal	from/to Module	I/O to GPT12	Can be used to/as
T4INA	P4.9	I	count input signals for timer T4
T4INB	P3.12	I	
T4INC	P15.0	I	
T4IND	0	I	
T4EUDA	P4.14	I	direction input signals for timer T4
T4EUDB	P5.5	I	
T4EUDC	P15.1	I	
T4EUDD	0	I	
T5INA	P3.0	I	count input signals for timer T5
T5INB	P0.11	I	
T5EUDA	P0.12	I	direction input signals for timer T5
T5EUDB	P0.13	I	
T6INA	P0.14	I	count input signals for timer T6
T6INB	P4.7	I	
T6EUDA	P5.0	I	direction input signals for timer T6
T6EUDB	P3.6	I	
T6OUT	P8.6 P14.10	O	count output signal for timer T6
T6OFL	P6.7 CCU60_T12HRF CCU60_T13HRF CCU61_T12HRF CCU61_T13HRF CCU63_CC62IND	O	over/under-flow signal from timer T6
CAPINA	P8.2	I	input capture signals
CAPINB	P6.8	I	

Table 30-22 GPT121 Digital Connections in TC1798

Signal	from/to Module	I/O to GPT12	Can be used to/as
T2INA	P3.14	I	count input signals for timer T2
T2INB	P4.10	I	
T2EUDA	P5.4	I	direction input signals for timer T2
T2EUDB	P4.12	I	
T3INA	P3.8	I	count input signals for timer T3
T3INB	P2.14	I	
T3INC	0	I	
T3IND	P14.14	I	
T3EUDA	P3.10	I	direction input signals for timer T3
T3EUDB	P4.8	I	
T3EUDC	0	I	
T3EUDD	P14.15	I	
T3OUT	P8.4 P14.9	O	count output signal for timer T3
T4INA	P3.12	I	count input signals for timer T4
T4INB	P4.9	I	
T4INC	0	I	
T4IND	P15.0	I	
T4EUDA	P5.5	I	direction input signals for timer T4
T4EUDB	P4.14	I	
T4EUDC	0	I	
T4EUDD	P15.1	I	
T5INA	P0.11	I	count input signals for timer T5
T5INB	P3.0	I	
T5EUDA	P0.13	I	direction input signals for timer T5
T5EUDB	P0.12	I	
T6INA	P4.7	I	count input signals for timer T6
T6INB	P0.14	I	

Table 30-22 GPT121 Digital Connections in TC1798 (cont'd)

Signal	from/to Module	I/O to GPT12	Can be used to/as
T6EUDA	P3.6	I	direction input signals for timer T6
T6EUDB	P5.0	I	
T6OUT	P8.7 P14.11	O	count output signal for timer T6
T6OFL	P6.9 CCU62_T12HRF CCU62_T13HRF CCU63_T12HRF CCU63_T13HRF CCU61_CC62IND	O	over/under-flow signal from timer T6
CAPINA	P6.8	I	input capture signals
CAPINB	P8.2	I	

31 Analog to Digital Converter (ADC)

The **A**nalog to **D**igital **C**onverter module (ADC) of the TC1798 allows the conversion of analog input values into discrete digital values based on the successive approximation method. With this method, the conversion result is elaborated bit by bit, starting with the most significant bit. As a consequence, an analog to digital conversion requires a certain number of clock cycles.

This chapter is structured as follows:

- Introduction (see **Section 31.1**)
- Operating the ADC (see **Section 31.2**)
- Module implementation in TC1798 (see **Section 31.3**)

31.1 Introduction

This section gives an overview about the feature set of the ADC module and introduces the general structure. It describes the:

- ADC block diagram (see **Section 31.1.1**)
- Feature set description (see **Section 31.1.2**)
- Abbreviations (see **Section 31.1.3**)
- Kernel overview (see **Section 31.1.4**)
- Conversion request handling (see **Section 31.1.5**)
- Conversion result handling (see **Section 31.1.6**)
- Interrupt structure (see **Section 31.1.7**)
- Electrical models (see **Section 31.1.8**)
- Transfer characteristics and error definitions (see **Section 31.1.9**)

31.1.1 ADC Block Diagram

The ADC module contains four independent kernels (ADC0, ADC1, ADC2, ADC3) that can operate autonomously or can be synchronized to each other. An ADC kernel is a unit used to convert an analog input signal into a digital value and provides means for triggering conversions, data handling and storage.
With this structure, parallel conversion of up to four analog input channels is supported.

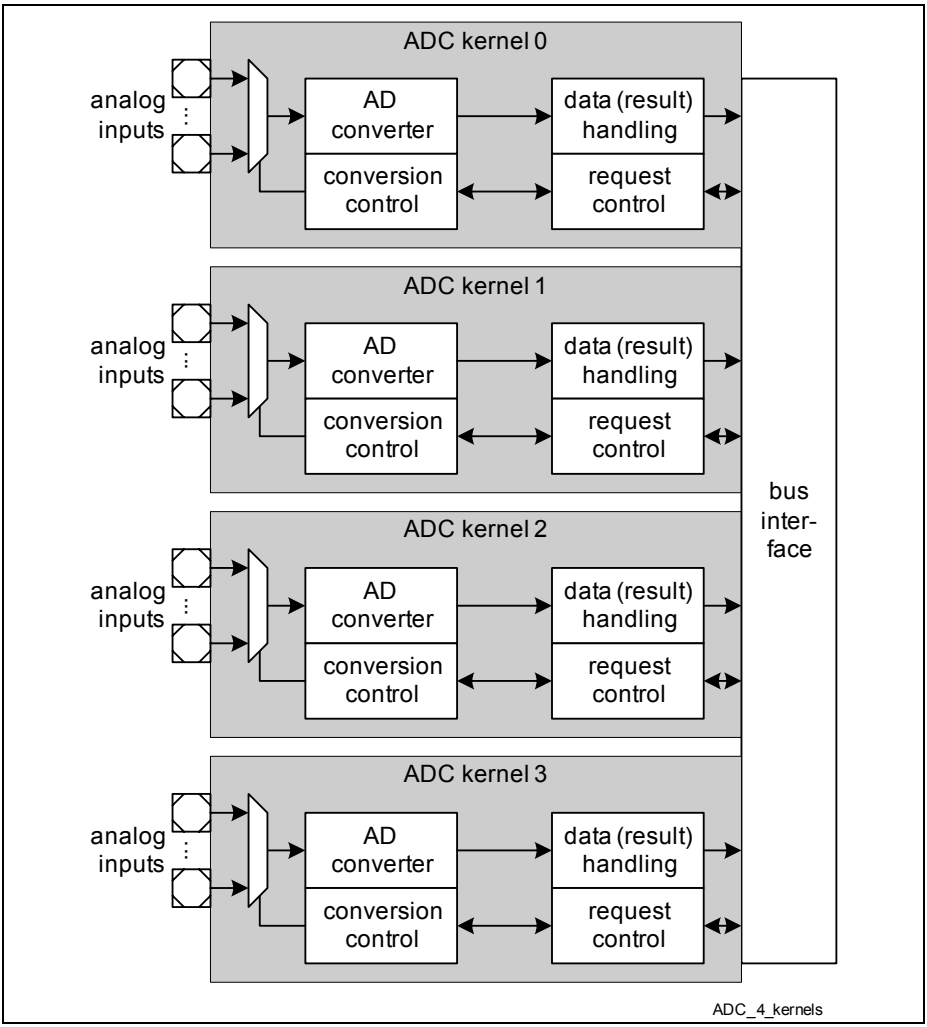


Figure 31-1 ADC Module Block Diagram

31.1.2 Feature Set

Features of each ADC kernel:

- Analog supply voltage range from 3.3 V (minimum) to 5 V (nominal) for V_{DDM}
- Input voltage range from 0 V to analog supply voltage V_{DDM}
- Input multiplexer for a maximum of 16 possible analog input channels
- One standard reference input (V_{AREF}) and one alternative reference input (CH0) available
- Broken wire detection support for each input channel
- Multiplexer test support for input channels with odd channel numbers
- 5 conversion request sources for external or timer-driven events, auto-scan, programmable sequences, SW-driven conversions, etc.
- Synchronization of the ADC kernels for concurrent conversion starts and parallel sampling and measuring of analog input signals, e.g. for phase current measurements in AC drives
- Control capability for an external analog multiplexer, respecting the additional set up time
- Adjustable sampling times to accommodate output impedance of different analog signal sources (sensors, etc.)
- Possibility to cancel running conversions on demand with automatic restart
- Flexible interrupt generation (possibility of DMA support)
- Limit checking to reduce interrupt load (e.g. for temperature measurements or overload detection, only values exceeding a programmable level lead to an interrupt)
- Programmable data reduction filter, e.g. for digital anti-aliasing filtering, by adding a programmable number of conversion results
- Independent result registers (16 independent registers)
- Programmable result data filter providing 3rd order FIR or 1st order IIR filter structure
- Support of conversion result FIFO mechanism to allow a longer interrupt latency
- Support of suspend and power saving modes
- Individually programmable reference selection for each channel, e.g. to allow measurements of 3.3 V and 5 V signals in the full measurement range with the same ADC kernel (with exception of dedicated channels always referring to V_{AREF})

31.1.3 Abbreviations

The following acronyms and terms are used in the ADC chapter:

Table 31-1 Abbreviations in ADC chapter

Abbreviation	Meaning
ADC	analog to digital converter
DMA	direct memory access mechanism
DNL	differential non-linearity error
FIFO	first-in-first-out data buffer mechanism
FIR	finite impulse resonse (digital filter)
INL	integral non-linearity error
IIR	infinite impulse resonse (digital filter)
LSB_n	finest granularity of the analog value in digital format, represented by one least significant bit of the conversion result with n bits resolution (measurement range divided in 2^n equally distributed steps)
SCU	system control unit of the device
TUE	total unadjusted error

31.1.4 ADC Kernel Overview

Each ADC kernel comprises:

- An **analog to digital converter** with a maximum of 16 analog inputs (CH0 - CH15). This block selects an input signal and translates the analog voltage into a digital value.
  Not all analog input channels are necessarily available in all packages, please refer to the implementation description in **Section 31.3**.
- A **conversion control** unit defining the conversion parameters like the length of the sample phase, the resolution and the reference for each conversion. The length of the sample phase and the resolution depend on the type of sensor (or other analog sources) connected to the ADC. These values are similar for several channels and, therefore, are grouped together to form the so-called input classes. Each channel can be individually assigned to an input class to define these parameters.
  The conversion control also handles the start conditions for the conversions, such as the immediate start (cancel-inject-repeat), overwrite of former results (wait-for-read), or synchronization of the ADC kernels (parallel conversions).
  Additionally, an external analog multiplexer can be controlled by the output signals EMUX[2:0] of dedicated ADC kernels.
- A **request control** unit defining which analog input channel has to be converted next. It contains 5 request sources that can trigger conversions depending on different events, such as edges of PWM or timer signals or events at port pins. Each request source can trigger either 1, up to 4, or up to 16 conversions in a sequence.
- A **result handling** unit providing 16 result registers for the conversion results. The conversion result of each analog input channel can be directed to one of the result registers to be stored there. The result handling block also supports data reduction (e.g. for digital anti-aliasing filtering) by automatically adding up to 4 conversion results before informing the CPU that new data is available.
  Additionally, the results registers can be concatenated to FIFO structures to provide storage capability for more than one conversion result without overwriting previous data. This feature also helps to handle CPU latency effects.
- An **interrupt generation** unit issuing interrupt requests to the CPU depending on ADC events. The interrupt generation in the ADC kernels support different mechanisms, e.g. some interrupts can be coupled to a value range of the conversion result (limit checking), some interrupts can be used to transport conversion data to locations in memory for further treatment, and other interrupts are generated after a complete sequence of conversions.

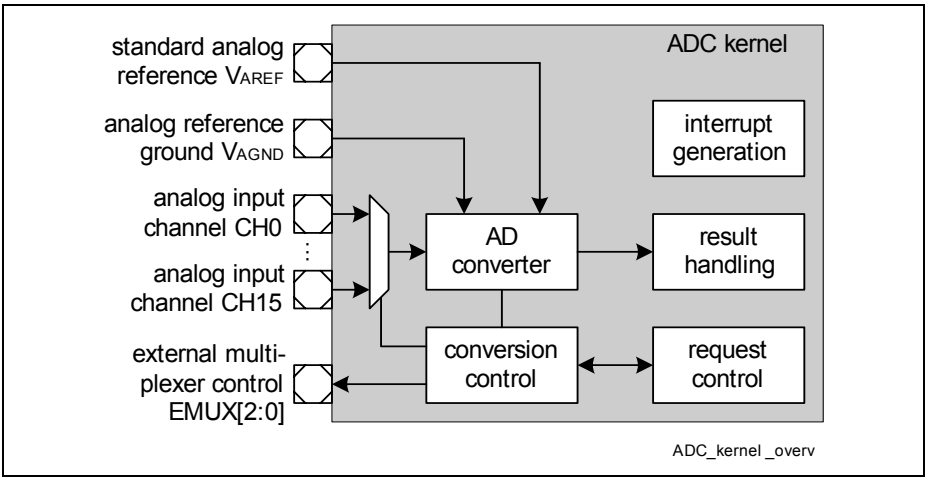


Figure 31-2 ADC Kernel Block Diagram

31.1.5 Conversion Request Unit

The conversion request unit of each ADC kernel autonomously handles the generation of conversion requests.
It contains 5 independent request sources that are connected to several modules to trigger the start of a conversion. A request source defines the analog input channel to be converted if a defined event occurs. For example, a trigger pulse from a timer unit generating a PWM signal can start the conversion of a single input channel or a programmed sequence of input channels.
Depending on the application, the request sources can be triggered by different events, either issued by other modules or under SW control. As a consequence, there can be two or more conversion requests pending at the same time. To allow the user to adapt the request source mechanism to the application needs, the trigger capability, the channel number(s) to be converted, and the priority can be individually programmed for each request source.
An arbiter block regularly scans the request sources for pending conversion requests and acts upon the conversion request with the highest priority. This conversion request is forwarded to the converter to start the conversion of the requested channel.

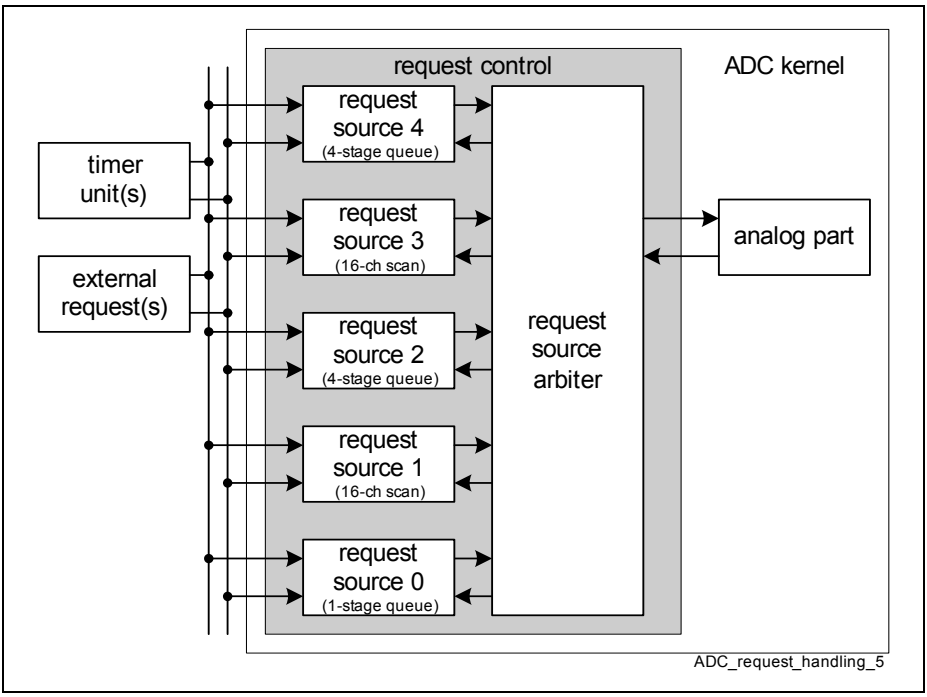


Figure 31-3 Conversion Request Unit

The functional characteristics of the request sources are adapted to the most common application requirements. In all request sources, a continuous operation or a single-shot operation can be selected. For continuous operation, the programmed sequence of conversions requests are continuously issued (once started), whereas in single-shot mode, each sequence of conversion requests has to be explicitly started. The trigger for a conversion request or a sequence can be handled under SW control or can be synchronized to ADC-external events, such as timer signals or port pins. For each request source, the user can select an input signal (from 8 possible signals REQTRx_[7:0]) as trigger input REQTRx and an input signal (from 8 possible signals REQGTx_[7:0]) as gating input REQGTx.

- **Request source 0** (1-stage sequential source) can issue a conversion request for a single input channel. The channel number can directly be programmed.
  This mechanism could be used for SW-controlled conversion requests or HW-triggered conversions of a single input channel. If programmed with a high priority, it can interrupt the sequences of the other request sources to inject a single conversion.
- **Request sources 1 and 3** (16-channel scan sources) can issue conversion requests for a sequence of up to 16 input channels. It can be programmed which channel takes part in this sequence. The sequence always starts with the highest enabled channel number and continues towards lower channel numbers (order defined by the channel number, each channel can be converted only once per sequence).
  This mechanism could be used to scan input channels permanently or on a regular time base. For example, if programmed with a low priority, some input channels can be scanned in a background task to update information that is not time-critical.
- **Request sources 2 and 4** (4-stage sequential sources) can issue a conversion request for a sequence of up to 4 input channels. The channel numbers can be freely programmed, especially multiple conversions of the same channel within the sequence are supported.
  This mechanism could be used to support application-specific conversion sequences that can not be covered by the scanning mechanism of request sources 1 or 3. Especially for timing-critical sequences containing multiple conversions of the same channel, one of these request sources should be used. For example, if programmed with a medium priority, some input channels can be converted when a specified event occurs (e.g. synchronized to a PWM) while the scan of other input channels of the background task (handled by request source 1) is interrupted.

31.1.6 Conversion Result Unit

The conversion result unit comprises for each ADC kernel:

- A set of **16 result registers** for storing the conversion results. A pointer mechanism for each analog input channel distributes the conversion results to the result registers. Especially for auto-scan applications, this feature simplifies DMA use (only one DMA channel needed to transfer a complete auto-scan sequence into the device memory).
- The result registers provide **valid flags** to indicate if new data has been stored since it has been read out (new data indication).
- A **result FIFO mechanism** for conversion results handling with a “relaxed” CPU timing. Result registers not directly used as target for a conversion result can be concatenated to form a result FIFO. This structure allows to store a sequence of conversion results before the CPU has to interact.
- A **digital anti-aliasing or data reduction filter**, accumulating a programmable number of conversion results before generating a result event interrupt.
  This feature can be used to avoid CPU intervention on each conversion result if a certain number of conversion results are added before further treatment, especially for fast conversions sequences and averaging of results.
- A **wait-for-read mechanism** can be enabled independently for each result register to delay conversions targeting a result register that has not yet been read out.
- A **flexible interrupt generation** based on result register events. A result register event occurs if a new valid data word becomes available in a result register and can be read out. Especially when using data reduction or digital anti-aliasing filtering, the result register event indicates that the final result is available.
- **Debugger support** for ADC result registers supporting read out of ADC conversion results without changing the result status (new data indication).

31.1.7 Interrupt Structure

Each ADC kernel provides 8 independent service request output signals (ADCx_SR[7:0]) used for interrupt handling. The interrupt generation inside the ADC kernel is based on three different types of events.

- **Channel events:**
  A channel event is detected if a conversion is finished and the conversion result is within a programmable value range.
  This type of event can be used to check if analog input values are inside or out of a nominal operating range, especially to reduce CPU load for background tasks. This allows the user to interrupt the CPU only if the specified conversion result range is met (or not met) instead of comparing each result by SW.
- **Result events:**
  A result event is detected if a new result is available in a result register and can be read out, e.g. to store the data in memory for further treatment by SW.
  This type of event can be used to trigger a read action by the CPU (or DMA). Especially when using data reduction or digital anti-aliasing filtering, not all finished conversion leads to a new result. Furthermore, when using a result FIFO, a result event decouples the CPU (DMA) read out from the channel events and tolerates a higher interrupt latency. The result register structure allows to use a single DMA channel for a complete auto-scan sequence by triggering the read out by a result event (if the conversion results of all channels taking part in the auto-scan sequence target the same result register, e.g. with FIFO mechanism or with a wait-for-read condition to avoid data loss).
- **Request source events:**
  A request source event is detected if a scan source has completely finished the requested conversion sequence. For a sequential source, the user can define where inside a conversion sequence a request source event is generated.
  This type of event can be used to inform the CPU that a conversion sequence has reached a defined state and SW can start the treatment of the related results in a block.

Each ADC event is indicated by a dedicated flag that can be cleared by SW. An interrupt can be generated (if enabled) for each event, independently from the status of the corresponding event indication flag. This structure ensures efficient DMA handling of ADC events (the ADC event can generate an interrupt without the need to clear the indication flag). A node pointer mechanism allows the user to group interrupts events by selecting which service request output signals SRx becomes activated by which event. Each ADC event can be individually directed to one of the service request output signals to adapt easily to application needs.

Note: A conversion can lead to three interrupts, one of each type. In this case, the ADC module first triggers the request source event interrupt, then the channel event interrupt, followed by the result event interrupt (all within a few f_{ADC} clock cycles).

31.1.8 Electrical Models

Each conversion of an analog input voltage into a digital value consists of two consecutive phases. During the sample phase, the input voltage is sampled and prepared for the following conversion phase. A simplified model for the sample phase describes the input signal path, whereas a second simplified model for the conversion phase is related to the reference voltage handling.

31.1.8.1 Input Signal Path

The ADC kernel in the TC1798 is based on one switched capacitor field for measurement with a total capacity represented by C_{AIN} and a small static capacitor at each input pin. During the sample phase, the capacitor field C_{AIN} is connected to one of the analog input CHx via an input multiplexer. The multiplexer is modeled by ideal switches and series resistors R_{AIN}. Only the switch to the selected analog input is closed during the sample phase. During the conversion phase or while no conversion is running (ADC is idle), all switches are open. The voltage at the analog input channel CHx is represented by V_{AINx}.

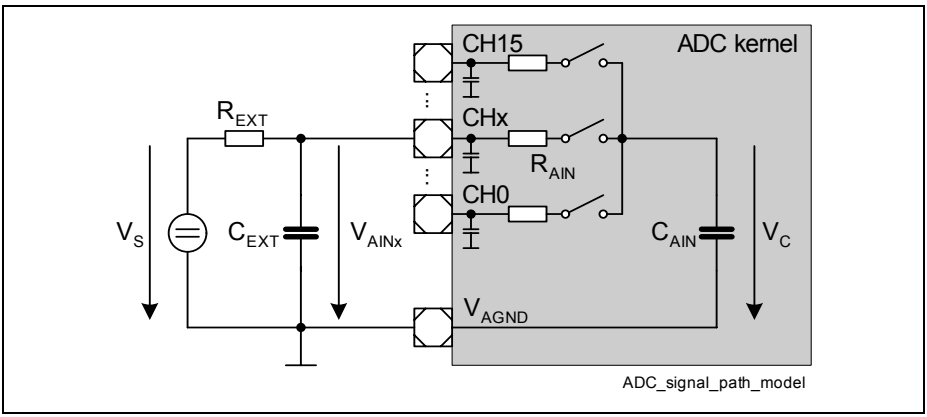


Figure 31-4 Signal Path Model

A simplified model for the analog input signal path is given in **Figure 31-4**. An analog voltage source (value V_S) with an internal impedance of R_{EXT} delivers the analog input that should be converted.

During the sample phase the corresponding switch is closed and the capacitor field C_{AIN} is charged. Due to the low-pass behavior of the resulting RC combination, the voltage V_C to be actually converted does not immediately follow V_S. The value R_{EXT} of the analog voltage source and the desired precision of the conversion strongly define the required length of the sample phase.

To reduce the influence of R_{EXT} and to filter input noise, it is recommended to introduce

a fast external blocking capacitor C_{EXT} at the analog input pin of the ADC. Like this, mainly C_{EXT} delivers the charge during the sample phase. This structure allows a significantly shorter sample phase than without a blocking capacitor, because the low-pass time constant defining the sample time is mainly given by the values of R_{AIN} and C_{AIN}.

Additionally, the capacitor C_{AIN} is automatically precharged to a voltage of approximately the half of the standard reference voltage V_{AREF} to minimize the average difference between V_{AINx} and V_C at the beginning of a sample phase. Due to varying parameters and parasitic effects, the precharge voltage of C_{AIN} is typically smaller than V_{AREF} / 2.

On the other hand, the charge redistribution between C_{EXT} and C_{AIN} leads to a voltage change of V_{AINx} during the sample phase. In order to keep this voltage change lower than 1 LSB_n, it is recommended to use an external blocking capacitor C_{EXT} in the range of at least $2^n \times C_{AIN}$.

The resulting low-pass filter of R_{EXT} and C_{EXT} should be dimensioned in a way to allow V_{AINx} to follow V_S between two sample phases of the same analog input channel.

Please note that, especially at high temperatures, the analog input structure of an ADC can lead to a leakage current and introduces an error due to a voltage drop over R_{EXT}. The ADC input leakage current increases if the input voltage level is close to the analog supply ground V_{SSM} or to the analog power supply V_{DDM}. It is recommended to use an operating range for the input voltage between approximately 3% and 97% of V_{DDM} to reduce input leakage values.

Furthermore, the leakage is influenced by an overload condition at adjacent analog inputs. During an overload condition, an input voltage exceeding the supply range is applied at an input and the built-in protection circuit limits the resulting input voltage. This leads to an overload current through the protection circuit that is translated (by a coupling factor) into an additional leakage at adjacent inputs.

31.1.8.2 Reference Path

During the conversion phase, parts of the capacitor field C_{AIN} are switched to a reference input or to V_{AGND}. The ADC kernel supports two possible reference inputs, V_{AREF} as standard reference and CH0 as alternative reference. The reference selection between both possibilities is handled individually for each analog input channel. For example, this structure allows conversions of 5 V and 3.3 V based analog input signals with the same ADC kernel.

A high accuracy of the conversion results requires a stable and noise-free reference voltage and analog supply voltages during the conversion phase. Instable voltages or noise on the supply or reference inputs lead to a reduced conversion accuracy. Please note that noise can also be introduced into the ADC module by other modules, e.g. by switching of neighboring pins. It is strongly recommended to carefully decouple analog from digital signal domains.

Due to the switching of parts of C_{AIN}, the ADC requires a dynamic current at the selected reference input. Thus, the impedance R_{AREF} of the reference voltage source V_R has to

be low enough to supply the reference current during the conversion phase. An external blocking capacitor C_{AREF} should be used to supply the peak currents and to minimize the current delivered by the reference source.

Due to the charge redistribution between C_{AREF} and parts of C_{AIN}, the voltage V_{AREF} decreases during the conversion phase. In order to limit the error introduced by this effect to 1/2 LSB_n, the external blocking capacitor C_{AREF} for the reference input should be at least $2^n \times C_{AIN}$.

The reference current I_{AREF} introduces a voltage drop at R_{AREF} that should not be neglected for the calculation of the overall accuracy. The average reference current during a conversion depends on the reference voltage level and the time t_{CONV} between two conversion starts.

$I_{AREF} = C_{AIN} \times V_{AREF} / t_{CONV}$

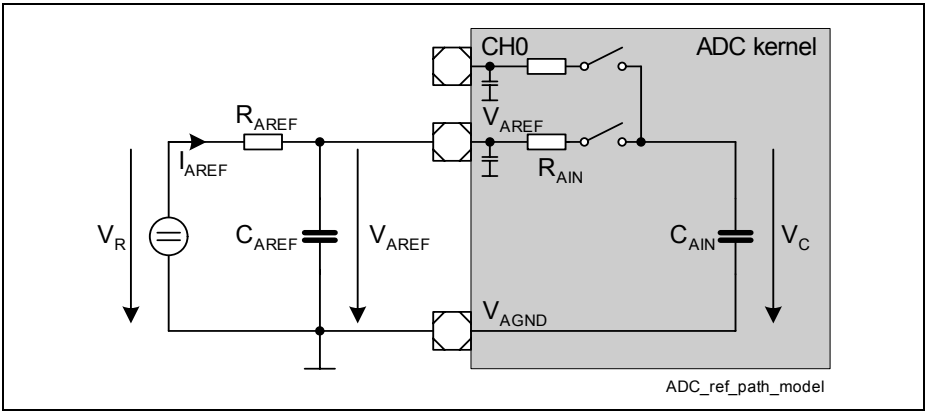


Figure 31-5 Reference Path Model

31.1.9 Transfer Characteristics and Error Definitions

The ideal transfer characteristic of the ADC translates a continuous analog input voltage into a discrete digital value out of a result range of 2^n steps for n bit resolution over a measurement range between 0 and a reference voltage. Each digital value in the available result range (from 0 to 2^n-1) represents an input voltage range that is defined by the reference voltage divided by 2^n. This range (called quantization step) represents the smallest granularity (called LSB_n) that can be handled by the ADC. Due to the discrete character of the digital result, each ADC conversion result has a system-inherent quantization uncertainty of ± 0.5 LSB_n. According to the ideal transfer characteristics, the first digital transition (between the digital values 0 and 1) takes place when the analog input reaches 0.5 LSB_n.
An analog input voltage above the reference voltage leads to a saturation of the digital result at 2^n-1.

Deviations of the conversion result from the ideal transfer characteristics can appear:

- An **offset error** is the deviation from the ideal transfer characteristics for an input voltage close to 0. It describes the difference between 0.5 LSB_n and the input voltage where the first digital transition (between the values of 0 and 1) occurs.
- A **gain error** is the deviation from the ideal transfer characteristics for an input voltage close to the reference voltage. It describes the difference between the reference voltage and the input voltage where the last digital transition (between the values of 2^n-2 and 2^n-1) occurs.
- A **differential non-linearity error** (DNL) describes the variations in the analog input voltage between two adjacent digital conversion results, over the full measurement range. If each step between the digital conversion results x and x+1 is exactly 1 LSB_n, the DNL value is zero. If the DNL value is lower than 1 LSB_n, the possibility of missing codes is excluded. A missing code occurs if not all values of the possible conversion result range can be reached.
- An **integral non-linearity error** (INL) describes the maximum difference between the transfer characteristics between the first and the last point of the measurement range and the real transfer characteristics (without quantization uncertainty, offset and gain errors).
- The **total unadjusted error** (TUE) describes the maximum deviation between a real conversion result and the ideal transfer characteristics over a given measurement range. Since some of these errors noted above can compensate each other, the TUE value generally is much less than the sum of the individual errors.
  The TUE also covers production process variations and internal noise effects (if switching noise is generated by the system, this generally leads to an increased TUE value).

31.2 Operating the ADC

This section describes the kernel functions and how to operate the kernel. It provides the functional descriptions and the associated register descriptions.

- Register overview (see **Section 31.2.1**)

General module, kernel and arbiter operation:

- Enabling the ADC module for configuration of the behavior for the different device operating modes (see mode control description in **Section 31.2.2**).
- Enabling the converter for operation or selecting the desired power saving mode (see **Section 31.2.3**)
- Selecting the appropriate frequency for the converter and for the request source arbiter (see **Section 31.2.4**).
- ADC module registers (see **Section 31.2.5**)
- General ADC kernel registers (see **Section 31.2.6**)
- Configuring the request source arbiter (see **Section 31.2.7**)
- Arbiter registers (see **Section 31.2.8**)

Request source operation:

- Scan request source handling (see **Section 31.2.9**)
- Scan request source registers (see **Section 31.2.10**)
- Sequential request source handling (see **Section 31.2.11**)
- Sequential request source registers (see **Section 31.2.12**)

Channel and result register operation:

- Configuring the channel-related functions (see **Section 31.2.13**)
- Channel-related registers (see **Section 31.2.14**)
- Conversion result handling (see **Section 31.2.15**)
- Conversion request handling (see **Section 31.2.16**)

Additional features:

- Multiplexer test support (see **Section 31.2.17**)
- External multiplexer control (see **Section 31.2.18**)
- Synchronization for parallel conversions (see **Section 31.2.19**)
- Equidistant sampling (see **Section 31.2.20**)
- Access protection (see **Section 31.2.21**)
- Broken-wire detection (see **Section 31.2.22**)
- Additional feature registers (see **Section 31.2.23**)

31.2.1 Register Overview

Table 31-2 shows all registers required for programming the ADC module. It summarizes the ADC kernel registers and defines their relative addresses and the reset values. The relative addresses have to be added to the base addresses for the ADC kernels (see Section 31.3) to obtain the absolute address for each register. Each ADC kernel is located in an address window of 4 * 256 bytes.
All registers can be accessed with 8 bit, 16 bit, or 32 bit wide accesses.

The prefix "**ADCx_**" has to be added to the register names in this table for each ADC kernel to distinguish registers of the different kernels. In this naming convention, x indicates the kernel number (e.g. ADC0_ for the ADC0 kernel and "ADC1_" for the ADC1 kernel).
The registers that are implemented only once in the ADC module are located in the address range of ADC0.

All ADC registers (including KSCFG.NOMCFG and KSCFG.COMCFG) are reset by an application reset (class 3), whereas bit field KSCFG.SUMCFG is reset by a debug reset (class 1).

Note: Register bits marked "w" always deliver 0 when read.

Access rights within the address range of an ADC kernel:

- Read or write access to defined register addresses: U, SV
- Accesses to empty addresses: reserved, BE

Table 31-2 Register Overview of ADC

Short Name	Description	Offset Addr.[1)]	Access Mode		Reset	Description See
			Read	Write		
ADC Module Registers (only available in the address range of ADC0)						
CLC	Clock Control Register	000_H	U, SV	SV, E	Class 3	Page 31-25
KSCFG	Kernel State Configuration Register	$00C_H$	U, SV	SV, E	Class 3	Page 31-26
SRCx x = 0 - 8	Service Request Control Registers	$3FC_H$ - x * 4_H	U, SV	U, SV	Class 3	Page 31-28
General Kernel Registers (available in the address range of each kernel)						
ID	Module Identification Register	008_H	U, SV	U, SV	Class 3	Page 31-32
RSIRx (x = 0 - 4)	Request Source x Input Register	010_H + x * 4	U, SV	U, SV	Class 3	Page 31-29

Table 31-2 Register Overview of ADC (cont'd)

Short Name	Description	Offset Addr.[1)]	Access Mode		Reset	Description See
			Read	Write		
INTR	Interrupt Activation Register	204_H	U, SV	U, SV	Class 3	Page 31-33
GLOBCTR	Global Control Register	030_H	U, SV	U, SV	Class 3	Page 31-34
GLOBCFG	Global Configuration Register	034_H	U, SV	U, SV	Class 3	Page 31-37
GLOBSTR	Global Status Register	038_H	U, SV	U, SV	Class 3	Page 31-39
Arbiter Registers (available in the address range of each kernel)						
ASENR	Arbitration Slot Enable Register	$03C_H$	U, SV	U, SV	Class 3	Page 31-47
RSPR0	Request Source Priority Register 0	040_H	U, SV	U, SV	Class 3	Page 31-48
RSPR4	Request Source Priority Register 4	044_H	U, SV	U, SV	Class 3	Page 31-49
Request Source 0 Registers (available in the address range of each kernel)						
QMR0	Queue 0 Mode Register	080_H	U, SV	U, SV	Class 3	Page 31-65
QSR0	Queue 0 Status Register	084_H	U, SV	U, SV	Class 3	Page 31-68
Q0R0	Queue 0 Register 0	088_H	U, SV	U, SV	Class 3	Page 31-70
QBUR0	Queue 0 Backup Register	$08C_H$	U, SV	U, SV	Class 3	Page 31-72
QINR0	Queue 0 Input Register	$08C_H$	U, SV	U, SV	Class 3	Page 31-74
Request Source 1 Registers (available in the address range of each kernel)						
CRCR1	Conversion Request 1 Control Register	090_H	U, SV	U, SV	Class 3	Page 31-54

Table 31-2 Register Overview of ADC (cont'd)

Short Name	Description	Offset Addr.[1)]	Access Mode		Reset	Description See
			Read	Write		
CRPR1	Conversion Request 1 Pending Register	094_H	U, SV	U, SV	Class 3	Page 31-56
CRMR1	Conversion Request 1 Mode Register	098_H	U, SV	U, SV	Class 3	Page 31-57
Request Source 2 Registers (available in the address range of each kernel)						
QMR2	Queue 2 Mode Register	$0A0_H$	U, SV	U, SV	Class 3	Page 31-65
QSR2	Queue 2 Status Register	$0A4_H$	U, SV	U, SV	Class 3	Page 31-68
Q0R2	Queue 2 Register 0	$0A8_H$	U, SV	U, SV	Class 3	Page 31-70
QBUR2	Queue 2 Backup Register	$0AC_H$	U, SV	U, SV	Class 3	Page 31-72
QINR2	Queue 2 Input Register	$0AC_H$	U, SV	U, SV	Class 3	Page 31-74
Request Source 3 Registers (available in the address range of each kernel)						
CRCR3	Conversion Request 3 Control Register	$0B0_H$	U, SV	U, SV	Class 3	Page 31-54
CRPR3	Conversion Request 3 Pending Register	$0B4_H$	U, SV	U, SV	Class 3	Page 31-56
CRMR3	Conversion Request 3 Mode Register	$0B8_H$	U, SV	U, SV	Class 3	Page 31-57
Request Source 4 Registers (available in the address range of each kernel)						
QMR4	Queue 4 Mode Register	$0C0_H$	U, SV	U, SV	Class 3	Page 31-65
QSR4	Queue 4 Status Register	$0C4_H$	U, SV	U, SV	Class 3	Page 31-68
Q0R4	Queue 4 Register 0	$0C8_H$	U, SV	U, SV	Class 3	Page 31-70

Table 31-2 Register Overview of ADC (cont'd)

Short Name	Description	Offset Addr.[1)]	Access Mode		Reset	Description See
			Read	Write		
QBUR4	Queue 4 Backup Register	$0CC_H$	U, SV	U, SV	Class 3	Page 31-72
QINR4	Queue 4 Input Register	$0CC_H$	U, SV	U, SV	Class 3	Page 31-74
Channel Registers (available in the address range of each kernel)						
CHCTRx (x = 0 -15)	Channel x Control Register	100_H + x * 4	U, SV	U, SV	Class 3	Page 31-81
INPCRx (x = 0 -3)	Input Class x Register	050_H + x * 4	U, SV	U, SV	Class 3	Page 31-83
ALR0	Alias Register 0	210_H	U, SV	U, SV	Class 3	Page 31-84
LCBRx (x = 0 - 3)	Limit Check Boundary Register x	$0F0_H$ + x * 4	U, SV	U, SV	Class 3	Page 31-85
CHFR	Channel Flag Register	060_H	U, SV	U, SV	Class 3	Page 31-86
CHFCR	Channel Flag Clear Register	064_H	U, SV	U, SV	Class 3	Page 31-87
CHENPR0	Channel Event Node Pointer Register 0	068_H	U, SV	U, SV	Class 3	Page 31-88
CHENPR8	Channel Event Node Pointer Register 8	$06C_H$	U, SV	U, SV	Class 3	Page 31-89
Result Registers (available in the address range of each kernel)						
RESR0	Result Register 0	180_H	U, SV	U, SV	Class 3	Page 31-100
RESRx (x = 1 - 15)	Result Register x	180_H + x * 4	U, SV	U, SV	Class 3	Page 31-102
RESRD0	Result Register 0 for Debugging	$1C0_H$	U, SV	U, SV	Class 3	Page 31-100
RESRDx (x = 1 - 15)	Result Register x for Debugging	$1C0_H$ + x * 4	U, SV	U, SV	Class 3	Page 31-102

Table 31-2 Register Overview of ADC (cont'd)

Short Name	Description	Offset Addr.[1]	Access Mode		Reset	Description See
			Read	Write		
VFR	Valid Flag Register	200_H	U, SV	U, SV	Class 3	Page 31-104
RCRx (x = 0 - 15)	Result Control Register x	140_H + x * 4	U, SV	U, SV	Class 3	Page 31-105
EVFR	Event Flag Register	070_H	U, SV	U, SV	Class 3	Page 31-107
EVFCR	Event Flag Clear Register	074_H	U, SV	U, SV	Class 3	Page 31-109
EVNPR	Source Event Node Pointer Register	078_H	U, SV	U, SV	Class 3	Page 31-110
RNPR0	Result Node Pointer Register 0	208_H	U, SV	U, SV	Class 3	Page 31-111
RNPR8	Result Node Pointer Register 8	$20C_H$	U, SV	U, SV	Class 3	Page 31-112
Additional Feature Registers (available in the address range of each kernel)						
APR	Access Protection Register	218_H	U, SV	SV, E	Class 3	Page 31-125
EMCTR	External Multiplexer Control Register	220_H	U, SV	U, SV	Class 3	Page 31-126
SYNCTR	Synchronization Control Register	048_H	U, SV	U, SV	Class 3	Page 31-130
BWDENR	Broken Wire Detection Enable Register	224_H	U, SV	U, SV	Class 3	Page 31-132
BWDCFGR	Broken Wire Detection Configuration Register	228_H	U, SV	U, SV	Class 3	Page 31-133

1) The absolute register address is calculated as follows:
Module Base Address + Offset Address (shown in this column)

31.2.2 Mode Control

The mode control concept for system control tasks, such as suspend request for debugging, allows to program the module behavior under different device operating conditions. The behavior of the ADC kernels can be programmed for each of the device operating modes. It is advantageous that the ADC kernels of an ADC module show an identical behavior regarding the device operating modes (e.g. to avoid that a non-suspended kernel waits for a suspended kernel to start a synchronized conversion). Therefore, the ADC module has a common associated register **ADC0_KSCFG** defining the behavior of all kernels of the module in the following device operating modes:

- **Normal operation:**
  This operating mode is the default operating mode when no suspend request is pending. The kernel behavior is defined by KSCFG.NOMCFG.
- **Suspend mode:**
  This operating mode is requested when a suspend request (issued by a debugger) is pending in the device. The kernel behavior is defined by KSCFG.SUMCFG.

For the ADC module, the following internal actions can be influenced by mode control:

- A current conversion of an analog value:
  If the request control unit has found a pending conversion request, the conversion can be started. This start has to be enabled by the mode control. If the current kernel mode allows the conversion start (run modes 0 and 1), it will be executed. If the kernel mode does not allow a start (stop modes 0 and 1), the conversion is not started. The start request is not cancelled, but frozen. A “frozen” conversion is started as programmed if the kernel mode is changed to a run mode again.
- An arbiter round:
  The start of a new arbiter round has to be enabled by the kernel modes. In stop mode 1, a new arbiter round will not start.

The behavior of the ADC kernels can be programmed for each of the device operating modes (normal operation, suspend mode). Therefore, the ADC kernels support four kernel modes, as shown in **Table 31-3**.

Table 31-3 ADC Kernel Behavior

Kernel Mode	Kernel Behavior	Code
run mode 0	kernel operation as specified, no impact on data transfer (same behavior for run mode 0 and run mode 1)	00_B
run mode 1		01_B

Table 31-3 ADC Kernel Behavior (cont'd)

Kernel Mode	Kernel Behavior	Code
stop mode 0	A currently running AD conversion is completely finished and the result is treated. Pending conversion request to start a new conversion are not taken into account (but not deleted). They start conversions after entering a run mode as programmed. The arbiter continues as programmed.	10_B
stop mode 1	Like stop mode 0, but the arbiter is stopped after it has finished its arbitration round.	11_B

Generally, bit field KSCFG.NOMCFG should be configured for run mode 0 as default setting for standard operation. If the ADC kernels should not react to a suspend request (and to continue operation as in normal mode), bit field KSCFG.SUMCFG has to be configured with the same value as KSCFG.NOMCFG. If the ADC kernels should show a different behavior and stop operation when a specific stop condition is reached, the code for stop mode 0 or stop mode 1 has to be written to KSCFG.SUMCFG.

Note: The stop mode selection strongly depends on the application needs and it is very unlikely that different stop modes are required in parallel in the same application. As a result, only one stop mode type (either 0 or 1) should be used in the bit fields in register KSCFG. Do not mix stop mode 0 and stop mode 1 and avoid transitions from stop mode 0 to stop mode 1 (or vice versa) for the ADC module.

31.2.3 Module Activation and Power Saving Modes

The converter of the ADC supports specific power down modes allowing an automatic reduction of the power consumption between two conversions. The following modes are determined by bit field **GLOBSTR**.ANON:

- ANON = 00_B: **Converter switched off** (default after reset)
  The complete converter is switched off and held in its reset state, conversions are not possible. To start a conversion, ANON has to be programmed to the desired mode. A maximum wake-up time of about 10 µs has to be respected before starting a conversion. Furthermore, digital logic blocks are set to their initial state.
- ANON = 01_B and 10_B: **Reserved**
  These modes are reserved and must not be selected.
- ANON = 11_B: **Normal operation**
  Conversions are always possible with the desired sample time. The converter stays active permanently.

31.2.4 Clocking Scheme

The different parts of an ADC kernel are driven by clock signals that are based on the clock f_{ADC} of the bus that is used to access the ADC module.

- The analog clock f_{ADCI} is used as internal clock for the converter and defines the conversion length and the sample time. It can be adjusted by programming bit field **GLOBCTR**.DIVA.
- The digital clock f_{ADCD} is used for the arbiter and defines the duration of an arbiter round. It can be adjusted by programming bit field **GLOBCTR**.DIVD.
- All other digital structures (such as interrupts, etc.) are directly driven by the module clock f_{ADC}.

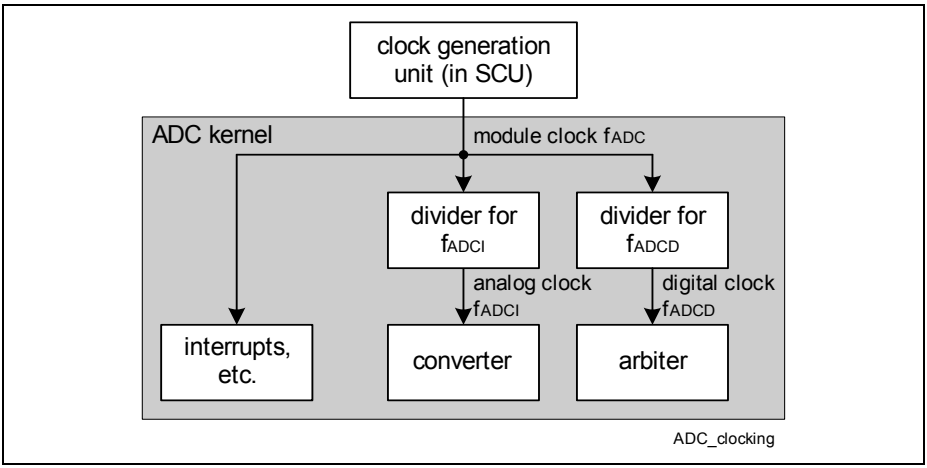


Figure 31-6 Clocking Scheme

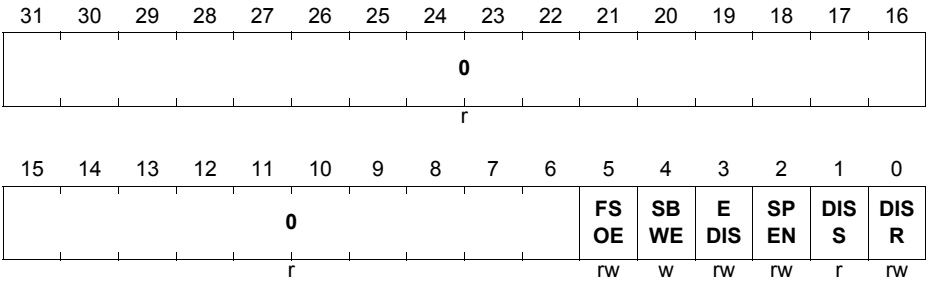
Note: If the clock generation for the converter of the ADC falls below a minimum value or is stopped during a running conversion, the conversion result can be corrupted. For correct ADC results, the frequency of f_{ADCI} must not exceed the range indicated in the electrical characteristics chapter.

31.2.5 ADC Module Registers

31.2.5.1 Clock Control Register

The clock control register allows the programmer to control (enable/disable) the clock signals to the ADC module.

ADC0_CLC
ADC Clock Control Register **(000_H)** **Reset Value: 0000 0003_H**



Field	Bits	Type	Description
DISR	0	rw	**Module Disable Request Bit** Used for enable/disable control of the module.
DISS	1	r	**Module Disable Status Bit** Bit indicates the current status of the module.
SPEN	2	rw	**Module Suspend Enable for OCDS** Used to enable the suspend mode
EDIS	3	rw	**Sleep Mode Enable Control** Used to control module's sleep mode.
SBWE	4	w	**Module Suspend Bit Write Enable for OCDS** Determines whether SPEN and FSOE are write-protected.
FSOE	5	rw	**Fast Switch Off Enable** Used to switch off fast clock in Suspend Mode.
0	[31:6]	r	**Reserved;** returns 0 if read; should be written with 0.

Note: After a hardware reset operation, the f_{CLC} and f_{ADC} clocks are switched off and the ADC module is disabled (DISS set).

31.2.5.2 Kernel State Configuration Register

The kernel state configuration register KSCFG allows the selection of the desired kernel modes. The ADC kernels are controlled by the same register ADC0_KSCFG.
All bits in KSCFG, except KSCFG.SUMCFG are reset by an application (class3) reset. Bit field KSCFG.SUMCFG is reset by the debug reset.
If a module should be switched off, SW can program a stop mode in bit field NOMCFG and check for ACK = 1 afterwards.

*Note: The coding of the bit fields NOMCFG, SUMCFG and COMCFG is described in **Table 31-3**.*

ADC0_KSCFG
Kernel State Configuration Register (00C$_H$) **Reset Value: 0000 0000$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0				BP SUM	0	SUMCFG		BP NOM	0	NOMCFG		SUS REQ	ACK	0	
r				w	r	rw		w	r	rw		rh	rh	r	

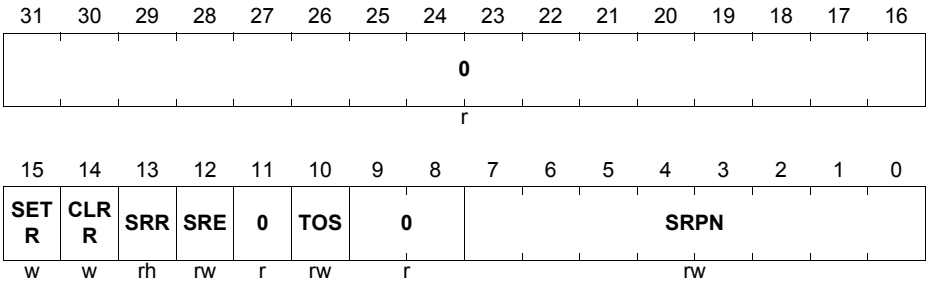
Field	Bits	Type	Description
ACK	2	rh	**Module Acknowledge** This bit monitors the state of the ADC module's acknowledge on incoming requests. 0_B The acknowledge is not activated, because at least one of the module kernels is in a transition phase. 1_B The acknowledge is activated, because all module kernels have reached the requested state.
SUSREQ	3	rh	**Suspend Request** This bit monitors the state of the ADC module's suspend request input. 0_B A suspend mode is not requested and bit field NOMCFG defines the ADC kernel mode. 1_B A suspend mode is requested and bit field SUMCFG defines the ADC kernel mode.

Field	Bits	Type	Description
NOMCFG	[5:4]	rw	**Normal Operation Mode Configuration** This bit field defines the kernel mode applied in normal operation mode. 00_B Run mode 0 is selected. 01_B Run mode 1 is selected. 10_B Stop mode 0 is selected. 11_B Stop mode 1 is selected.
BPNOM	7	w	**Bit Protection for NOMCFG** This bit enables the write access to the bit field NOMCFG. It always reads 0. 0_B The bit field NOMCFG is not changed. 1_B The bit field NOMCFG is updated with the written value.
SUMCFG	[9:8]	rw	**Suspend Mode Configuration** This bit field defines the kernel mode applied in suspend mode. Coding like NOMCFG.
BPSUM	11	w	**Bit Protection for SUMCFG** This bit enables the write access to the bit field SUMCFG. It always reads 0. 0_B The bit field SUMCFG is not changed. 1_B The bit field SUMCFG is updated with the written value.
0	[1:0], 6, 10, [31:12]	r	**Reserved** Read as 0; should be written with 0.

31.2.5.3 Service Request Control Registers

The service request control registers of the ADC module are located in the address range of ADC0.

ADC0_SRCx (x = 0-8)
ADC Service Request Control Register x
($3FC_H$ - x*4) **Reset Value: $0000\ 0000_H$**



Field	Bits	Type	Description
SRPN	[7:0]	rw	**Service Request Priority Number**
TOS	10	rw	**Type of Service Control**
SRE	12	rw	**Service Request Enable**
SRR	13	rh	**Service Request Flag**
CLRR	14	w	**Request Clear Bit**
SETR	15	w	**Request Set Bit**
0	[9:8], 11, [31:16]	r	**Reserved** Read as 0; should be written with 0.

Note: Additional details on service request nodes and the service request control registers are described in the TC1798 System Units part (Volume 1).

31.2.6 General ADC Kernel Registers

31.2.6.1 Request Source Input Registers

The setting of the request source input registers selects the desired input signal for the gating and trigger signals of the request sources. The status of the selected inputs is monitored. Additionally, the edge sensitivity for the trigger signal and the timer mode for equidistant sampling can be enabled/disabled.

The actual connections depending on the device implementation, please refer to the implementation description in **Section 31.3** for details.

Note: Signals from a synchronous domain can of course be connected to inputs with a synchronization stage. The additional synchronization delay of two ADC module clock cycles and an additional uncertainty of one ADC module clock cycle for asynchronous signals have to be taken into account when using a synchronization stage.

RSIRx (x = 0 - 4)

Request Source x Input Register (010_H + x * 4) **Reset Value: 0000 0000_H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

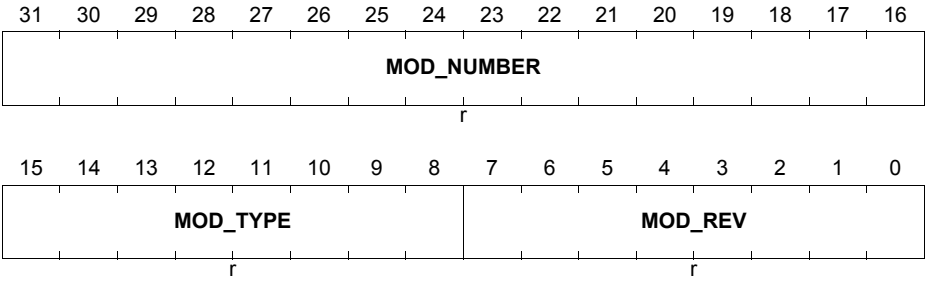
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TRI	0	R EN	F EN	0	TRSEL			GTI	0		TM EN	0	GTSEL		
rh	r	rw	rw	r	rw			rh	r		rw	r	rw		

Field	Bits	Type	Description
GTSEL	[2:0]	rw	**Input Selection for REQGT of Source x** This bit field defines the input signal used for request gating in request source x. The inputs selected by codes $0XX_H$ are considered as synchronous to the ADC module. The inputs selected by codes $1XX_H$ are considered as asynchronous to the ADC module. 000_B The input signal REQGTx_0 is selected. 001_B The input signal REQGTx_1 is selected. 010_B The input signal REQGTx_2 is selected. 011_B The input signal REQGTx_3 is selected. 100_B The input signal REQGTx_4 is selected. 101_B The input signal REQGTx_5 is selected. 110_B The input signal REQGTx_6 is selected. 111_B The input signal REQGTx_7 is selected.
TMEN	4	rw	**Timer Mode Enable of Source x** This bit enables the timer mode for equidistant sampling for request source x. 0_B The timer mode is disabled. The standard gating mechanism can be used. 1_B The timer mode for equidistant sampling is enabled. The standard gating mechanism has to be disabled.
GTI	7	rh	**Gating Input of Source x** This flag monitors the status of the selected gating signal REQGTx for request source x. 0_B The selected gating signal is 0. 1_B The selected gating signal is 1.

Field	Bits	Type	Description
TRSEL	[10:8]	rw	**Input Selection for REQTR of Source x** This bit field defines the input signal used for request triggering in request source x. The inputs selected by codes $0XX_H$ are considered as synchronous to the ADC module. The inputs selected by codes $1XX_H$ are considered as asynchronous to the ADC module. 000_B The input signal REQTRx_0 is selected. 001_B The input signal REQTRx_1 is selected. 010_B The input signal REQTRx_2 is selected. 011_B The input signal REQTRx_3 is selected. 100_B The input signal REQTRx_4 is selected. 101_B The input signal REQTRx_5 is selected. 110_B The input signal REQTRx_6 is selected. 111_B The input signal REQTRx_7 is selected.
FEN	12	rw	**Falling Edge Enable of Source x** This bit enables the request trigger for falling edges of the selected REQTRx signal for request source x. 0_B The request trigger with a falling edge is disabled. 1_B The request trigger with a falling edge is enabled.
REN	13	rw	**Rising Edge Enable of Source x** This bit enables the request trigger for rising edges of the selected REQTRx signal for request source x. 0_B The request trigger with a rising edge is disabled. 1_B The request trigger with a rising edge is enabled.
TRI	15	rh	**Trigger Input of Source x** This flag monitors the status of the selected trigger signal REQTRx for request source x. 0_B The selected trigger signal is 0. 1_B The selected trigger signal is 1.
0	3, [6:5], 11, 14, [31:16]	r	**Reserved** Read as 0; should be written with 0.

31.2.6.2 Module Identification Register

ID
Module Identification Register **(008_H)** **Reset Value: $005A\ C001_H$**



Field	Bits	Type	Description
MOD_REV	[7:0]	r	**Module Revision** This bit field indicates the revision number of the module implementation (depending on the design step). The given value of 00_H is a placeholder for the actual number. Bits [3:0] refer to the version of the digital part and bits [7:4] indicate the version of the analog part (anid).
MOD_TYPE	[15:8]	r	**Module Type**
MOD_NUMBER	[31:16]	r	**Module Number**

31.2.6.3 Interrupt Activation Register

The interrupt activation register contains bit locations allowing to activate one or more service request outputs SR[7:0] of the ADC kernel. Writing a 1 to a bit position x activates the corresponding SRx line. All bit positions read as 0.

INTR
Interrupt Activation Register (204_H) Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0								SISR7	SISR6	SISR5	SISR4	SISR3	SISR2	SISR1	SISR0
r								w	w	w	w	w	w	w	w

Field	Bits	Type	Description
SISRx (x = 0 - 7)	x	w	**Set Interrupt for SRx Line** Writing a 1 to a bit position sets an interrupt request at the SRx output of the ADC kernel (the activation is finished automatically). Writing a 0 has no effect. The read value is always 0. 0_B No action 1_B The service request output SRx of the ADC kernel becomes activated.
0	[31:8]	r	**Reserved** Read as 0; should be written with 0.

31.2.6.4 Global Control

The global control register contains bits to control the arbiter timing and the general enable function for the analog part.

GLOBCTR
Global Control Register **(030_H)** **Reset Value: 0000 00FF$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ARBM	0			ARBRND		ANON		DIVD		DIVA					
rw	rw			rw		rw		rw		rw					

Field	Bits	Type	Description
DIVA	[5:0]	rw	**Divider Factor for Analog Internal Clock** This bit field defines the number of f_{ADC} clock cycles to generate the f_{ADCI} clock for the converter (used as internal base for the conversions and the sample time calculation). The minimum divider is 4. 00_H $f_{ADCI} = f_{ADC} / 4$ 01_H $f_{ADCI} = f_{ADC} / 4$ 02_H $f_{ADCI} = f_{ADC} / 4$ 03_H $f_{ADCI} = f_{ADC} / 4$ 04_H $f_{ADCI} = f_{ADC} / 4$ 05_H $f_{ADCI} = f_{ADC} / 5$ 06_H $f_{ADCI} = f_{ADC} / 6$ 07_H $f_{ADCI} = f_{ADC} / 7$ ... $3F_H$ $f_{ADCI} = f_{ADC} / 63$

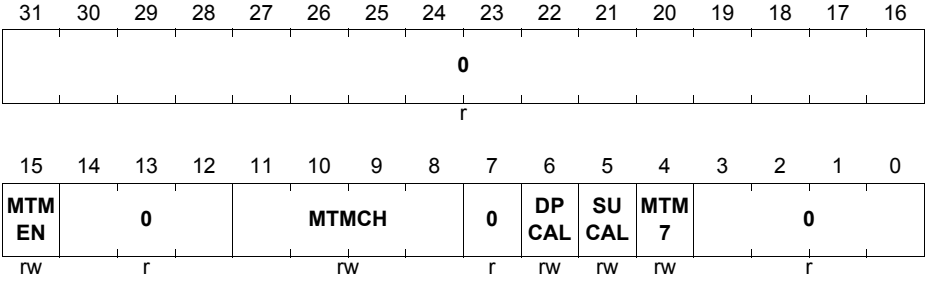
Field	Bits	Type	Description
DIVD	[7:6]	rw	**Divider Factor for Digital Arbiter Clock** This bit field defines the number of f_{ADC} clock cycles within each arbitration slot (each arbitration slots last one periods of f_{ADCD}). It is recommended to use the default setting 00_B to obtain the minimum arbiter reaction time. 00_B $f_{ADCD} = f_{ADC}$ 01_B $f_{ADCD} = f_{ADC} / 2$ 10_B $f_{ADCD} = f_{ADC} / 3$ 11_B $f_{ADCD} = f_{ADC} / 4$
ANON	[9:8]	rw	**Analog Part Switched On** This bit field defines the setting of bit field **GLOBSTR**.ANON (bit description see there) if this kernel is the synchronization master or without synchronization feature. For a synchronization slave, this bit field is not taken into account.
ARBRND	[11:10]	rw	**Arbitration Round Length** This bit field defines the number of arbitration slots per arbitration round (arbitration round length = t_{ARB}). 00_B An arbitration round contains 4 arbitration slots ($t_{ARB} = 4 / f_{ADCD}$). 01_B An arbitration round contains 8 arbitration slots ($t_{ARB} = 8 / f_{ADCD}$). 10_B An arbitration round contains 16 arbitration slots ($t_{ARB} = 16 / f_{ADCD}$). 11_B An arbitration round contains 20 arbitration slots ($t_{ARB} = 20 / f_{ADCD}$).

Field	Bits	Type	Description
ARBM	15	rw	**Arbitration Mode** This bit field defines whether the arbiter runs permanently or only while at least one conversion request is pending. 0_B The arbiter runs permanently. This setting has to be chosen in a synchronization slave (see **Section 31.2.19**) and for equidistant sampling using the signal ARBCNT (see **Section 31.2.20**). 1_B The arbiter only runs if at least one conversion request of an enabled request source is pending. This setting leads to a reproducible latency from an incoming request to the conversion start if the converter is idle. Synchronized conversions are not supported.
0	[14:12], [31:16]	r	**Reserved** Read as 0; should be written with 0.

31.2.6.5 Global Configuration

The global configuration register configures the general ADC kernel setting.

GLOBCFG
Global Configuration Register (034_H) Reset Value: $0000\ 0000_H$



Field	Bits	Type	Description
MTM7	4	rw	**Multiplexer Test Mode for Channel 7** This bit enables/disables the multiplexer test mode for the input channel 7, see **Section 31.2.17**. This feature is independent of the current mode of the ADC (ANON, selected channel for conversion). 0_B The multiplexer test mode is disabled. The analog input CH7 can be used for normal measurements. 1_B The multiplexer test mode is enabled. The analog input CH7 is internally connected to ground via voltage divider based on an additional resistor.[1)]
SUCAL	5	rw	**Start-Up Calibration** The transition from 0 to 1 of this bit starts the start-up calibration phase of the analog part. This should be done after reset before starting the first conversion to reduce analog errors. During the calibration phase (indicated by **GLOBSTR**.CAL = 1), conversions must not be started. It can take a few f_{ADC} clock cycles before bit CAL is set after a rising edge of SUCAL. 0_B Start-up calibration can be started. 1_B Start-up calibration has been started.

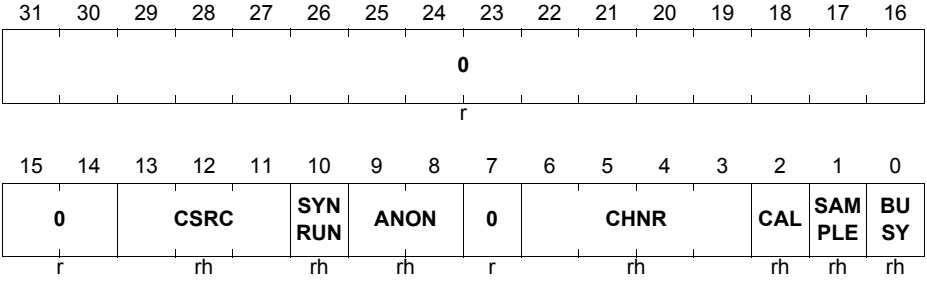
Field	Bits	Type	Description
DPCAL	6	rw	**Disable Post Calibration** This bit enables/disables the automatic post calibration of the analog part. 0_B The automatic post calibration is enabled. 1_B The automatic post calibration is disabled.
MTMCH	[11:8]	rw	**Multiplexer Test Mode Channel** This bit field defines the input channel number that can be enabled for multiplexer test mode in addition to channel CH7 (a value of 000001_B defines channel CH1, 000011_B channel CH3, 000101_B channel CH5, etc.). The multiplexer test mode is enabled for the selected input if MTMEN = 1.
MTMEN	15	rw	**Multiplexer Test Mode Enable** This bit enables the multiplexer test mode for the channel number selected by MTMCH. If an even channel number is selected, this bit is internally considered as 0. 0_B The multiplexer test mode for the selected input channel is disabled. This analog input can be used for normal measurements. 1_B The multiplexer test mode for the selected input channel is enabled. This analog input is internally connected to ground via voltage divider based on an additional resistor.[1)]
0	[3:0], 7, [14:12], [31:16]	r	**Reserved** Read as 0; should be written with 0.

1) Please refer to the AC/DC chapter for the value of the grounding resistor and its current capability.

31.2.6.6 Global Status

The status control register contains bits indicating the current status of a conversion.

GLOBSTR
Global Status Register **(038_H)** **Reset Value: $0000\ 0000_H$**



Field	Bits	Type	Description
BUSY	0	rh	**Analog Part Busy** This bit indicates that a conversion is currently active. 0_B The analog part is idle. 1_B A conversion is currently active.
SAMPLE	1	rh	**Sample Phase** This bit indicates that an analog input signal is currently sampled. 0_B The analog part is not in the sampling phase. 1_B The analog part is in the sampling phase.
CAL	2	rh	**Calibration Phase** This bit indicates that the analog part is in the startup calibration phase. 0_B The analog part is not in the calibration phase. 1_B The analog part is in the calibration phase.
CHNR	[6:3]	rh	**Channel Number** This bit field indicates which analog input channel is currently converted. This information is updated when a new conversion is started.

Field	Bits	Type	Description
ANON	[9:8]	rh	**Analog Part Switched On** This bit field defines the operation mode of the converter. It monitors either bit field GLOBCTR.ANON of the same ADC kernel (in master mode or without synchronization feature) or bit field GLOBCTR.ANON of the ADC kernel selected as synchronization master for this kernel (in slave mode). This ensures that all kernels of a synchronization group can be controlled with a single write operation to bit field GLOBCTR of the synchronization master. 00_B The analog part is switched off and conversions are not possible. To achieve a minimal power consumption, the internal analog circuitry is in its power-down state and the generation of f_{ADCI} and f_{ADCD} is stopped (counters set to an initial value). Furthermore, the arbiter finishes its current arbitration round (if running) and then remains in the idle state. 01_B reserved, do not use 10_B reserved, do not use 11_B The analog part of the ADC module is switched on and conversions are possible.
SYNRUN	10	rh	**Synchronous Conversion Running** This bit indicates that a synchronous (= parallel) conversion is currently running. 0_B There is no synchronous conversion running (either there is no conversion currently running or a parallel conversion has not been requested). A running conversion can be cancelled and repeated in case of a new incoming conversion request with higher priority. 1_B A synchronous conversion is running. This conversion can not be cancelled while running. Higher priority requests can trigger conversions only after the end of the currently running synchronous conversion.

Field	Bits	Type	Description
CSRC	[13:11]	rh	**Currently Converted Request Source** This bit field indicates the arbitration slot number of the current conversion (if BUSY = 1, a conversion is still running) or of the last conversion (if BUSY = 0, no conversion is running). This bit field is updated with each conversion start. 000_B The channel requested by the request source of arbitration slot 0 is (has been) converted. 001_B The channel requested by the request source of arbitration slot 1 is (has been) converted. ... 110_B The channel requested by the request source of arbitration slot 6 is (has been) converted. 111_B The channel requested by a synchronous injection is (has been) converted.
0	7, [31:14]	r	**Reserved** Read as 0; should be written with 0.

31.2.7 Request Source Arbiter

The request source arbiter evaluates which analog input channel has to be converted. Therefore, it regularly polls the request sources one after the other for pending conversion requests. The polling sequence is based on time slots with programmable length, called arbitration slots. If a request source is disabled or if no request source is available for an arbitration slot, the slot is considered as being empty and has no influence on the evaluation of the arbitration winner. After reset, all request sources are disabled and have to be enabled by bits in register **ASENR** to take part in the arbitration process.

The number of arbitration slots forming an arbitration round can be programmed to obtain a similar arbiter timing for different devices, even if the number of available request sources differs from one device to another. At the end of each arbitration round, the arbiter has determined the request source with the highest priority and a pending conversion request. This arbitration result is stored as arbitration winner for further actions. If a conversion is started in an arbitration round, this arbitration round does not deliver an arbitration winner.

In the TC1798, the following request sources are available:

- **Request source 0** in arbitration slot 0: **1-stage sequential source**
  This request source can issue a conversion request for a single input channel.
- **Request source 1** in arbitration slot 1: **16-channel scan source**
  This request source can issue a conversion request sequence of up to 16 input channels in a defined order.
- **Request source 2** in arbitration slot 2: **4-stage sequential source**
  This request source can issue a conversion request sequence of up to 4 input channels in a freely programmable order.
- **Request source 3** in arbitration slot 3: **16-channel scan source**
  This request source can issue a conversion request sequence of up to 16 input channels in a defined order.
- **Request source 4** in arbitration slot 4: **4-stage sequential source**
  This request source can issue a conversion request sequence of up to 4 input channels in a freely programmable order.
- Last arbitration slot of the arbitration round: **Synchronization source**
  In this slot, the arbiter checks for a synchronized request from another ADC kernel and does not evaluate any internal request source. A request for a synchronized conversion is always handled with the highest priority in a synchronization slave kernel (pending requests from other sources are not considered).

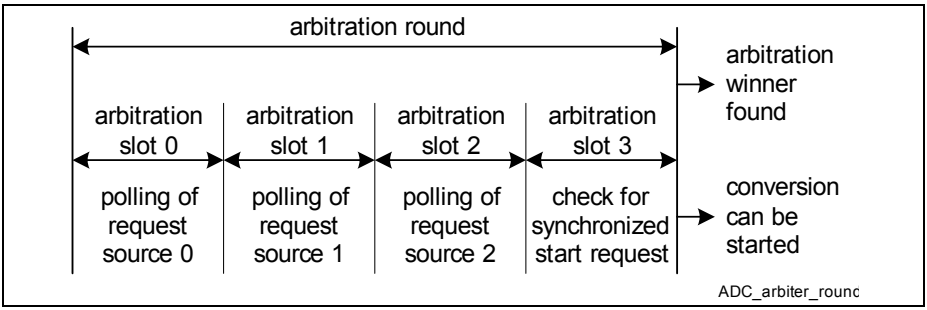


Figure 31-7 Arbitration Round with 4 Arbitration Slots

The period t_{ARB} of an arbitration round is given by:
$t_{ARB} = N \times (GLOBCTR.DIVD + 1) / f_{ADC}$
with N being 4, 8, 16, or 20 as defined by **GLOBCTR**.ARBRND

The period of the arbitration round introduces a timing granularity to detect an incoming conversion request signal and the earliest point to start the related conversion. This granularity can introduce a jitter of maximum one arbitration round. The jitter can be reduced by minimizing the period of an arbitration round (numbers of arbitration slots and their length).

To achieve a reproducible reaction time (constant delay without jitter) between the trigger event of a conversion request (e.g. by a timer unit or due to an external event) and the start of the related conversion, mainly the following two options exist. For both options, the converter has to be idle and other conversion requests must not be pending for at least one arbiter round before the trigger event occurs:

- If bit **GLOBCTR**.ARBM = 0, the **arbiter runs permanently**. In this mode, synchronized conversions of more than one ADC kernel are possible.
  The trigger for the conversion triggers has to be generated synchronously to the arbiter timing. Incoming triggers should have exactly n-times the granularity of the arbiter (n = 1, 2, 3, ...). In order to allow some flexibility, the duration of an arbitration slot can be programmed in cycles of f_{ADC}.
- If bit **GLOBCTR**.ARBM = 1, the **arbiter stops after an arbitration round** when no conversion request have been found pending any more. The arbiter is started again if at least one enabled request source indicates a pending conversion request. The trigger of a conversion request does need not to be synchronous to the arbiter timing. In this mode, parallel conversions are not possible for synchronization slave kernels.

31.2.7.1 Request Source Priority

Each request source has an individually programmable priority to be able to adapt to different applications (see registers **RSPR0**, **RSPR4**). The priorities define the order the request sources are handled by the arbiter if two or more request sources indicate

pending conversion requests at the same time.
Starting with request source 0, the arbiter checks if an enabled request source has a pending request for a conversion. The arbitration winner is the request source with a pending conversion request and the highest priority that has been found first in an arbitration round.

31.2.7.2 Conversion Start Modes

To start the requested conversion of the arbitration winner, the following aspects are automatically taken into consideration by the arbiter:

- If the converter is currently idle (no conversion running), the conversion of the arbitration winner is started immediately.
- If a conversion is currently running, the arbitration winner is compared to the priority of the currently running conversion. In the case that the current conversion has the same or a higher priority, it is completed. Then, the conversion of the arbitration winner is started.
- If a conversion is currently running, the arbitration winner is compared to the priority of the currently running conversion. In the case that the current conversion has the lower priority and the arbiter winner has been programmed for **wait-for-start mode**, the currently running conversion is completed. Then, the conversion of the arbitration winner is started.
  This mode can be used if the timing requirement for the higher priority conversions allow a jitter (between t3 and t4 in **Figure 31-8**) in the range of a running conversion.
- If a conversion is currently running, the arbitration winner is compared to the priority of the currently running conversion. In the case that the current conversion has the lower priority and the arbiter winner has been programmed for **cancel-inject-repeat mode**, the current conversion is aborted immediately if a new request with a higher priority has been found, unless both requests target the same result register with wait-for-read active (see **Section 31.2.15.2**). The conversion of the arbitration winner is started after the abort action. The aborted conversion request is restored in the request source that has requested the aborted conversion. As a consequence, it takes part again in the next arbitration round.
  Please note that the abort mechanism can take between 1 and 3 f_{ADCI} cycles, depending on the state of the current conversion.
  This mode can be used if higher priority conversions only tolerate a small jitter (between t8 and t9 in **Figure 31-8**).

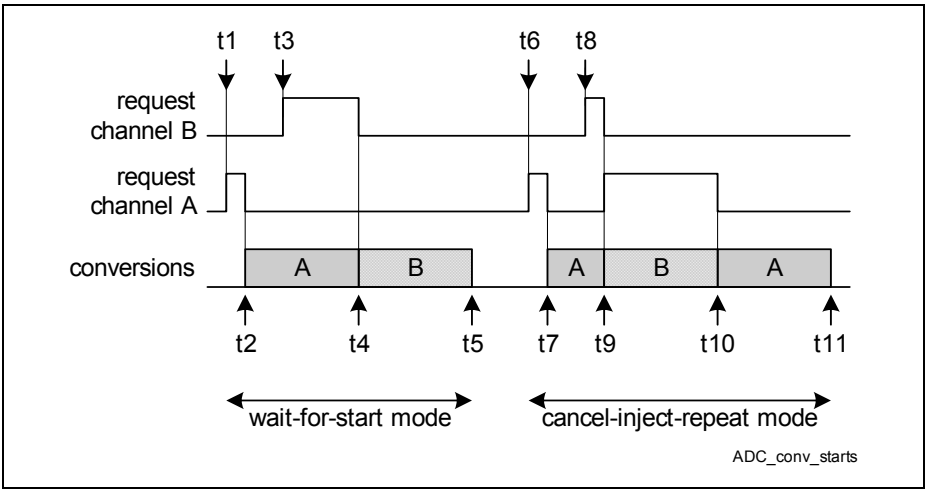


Figure 31-8 Conversion Start Modes

The conversion start mode can be individually programmed for each request source by bits in registers **RSPR0** and **RSPR4** and is applied to all channels requested by the source. **Figure 31-8** shows the influence of both conversion start modes on the conversion sequence if two request sources generate conversion requests. In this example, channel A is issued by a request source with a lower priority than the request source requesting the conversion of channel B.

- t1: The trigger event for channel A occurs and a conversion request is activated.
- t2: At the end of the arbitration round, channel A is determined as arbitration winner, the conversion of channel A is started. With the start of the conversion, the related conversion request is cleared.
- t3: The trigger event for channel B occurs and a conversion request is activated. In wait-for-read mode, the currently running conversion of channel A is finished normally.
- t4: After the conversion of channel A is finished, the conversion of channel B is started. With the start of the conversion, the related conversion request is cleared.
- t5: The conversion of channel B is finished.
- t6: The trigger event for channel A occurs and a conversion request is activated.
- t7: At the end of the arbitration round, channel A is determined as arbitration winner, the conversion of channel A is started. With the start of the conversion, the related conversion request is cleared.
- t8: The trigger event for channel B occurs and a conversion request is activated.
- t9: At the end of the arbitration round, channel B is determined as arbitration winner. In cancel-inject-repeat mode, the currently running conversion of channel A is aborted and the conversion of channel B is started. With the abort of the conversion,

the related conversion request is set again. With the start of the conversion, the related conversion request is cleared.

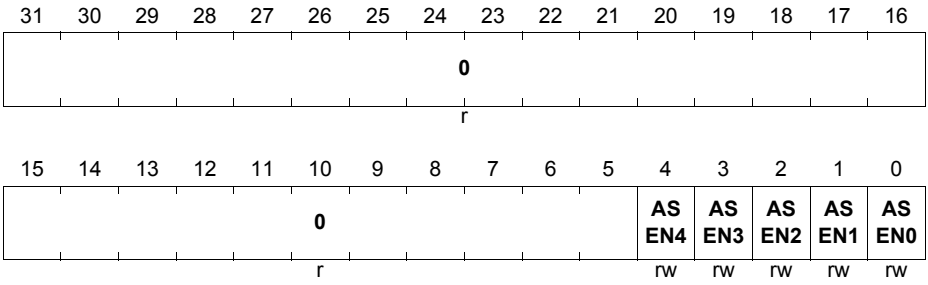
- t10: The conversion of channel B is finished. In the meantime, the pending request for channel A has been identified as arbitration winner and the conversion of channel A is started. With the start of the conversion, the related conversion request is cleared.
- t11: The conversion of channel A is finished.

31.2.8 Arbiter Registers

31.2.8.1 Arbitration Slot Enable Register

The arbitration slot enable register contains bits to enable/disable the conversion request treatment in the arbitration slots.

ASENR
Arbitration Slot Enable Register ($03C_H$) Reset Value: $0000\ 0000_H$



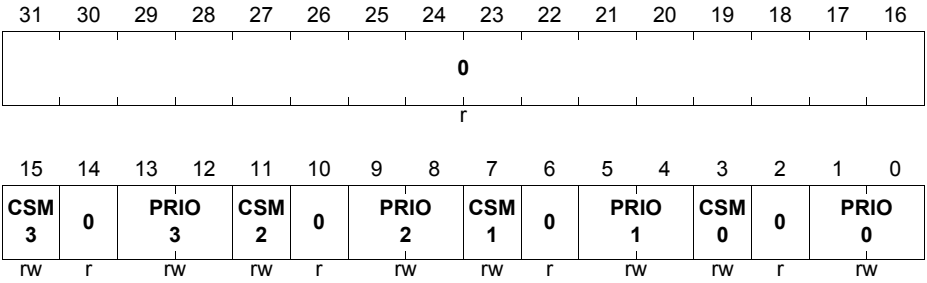
Field	Bits	Type	Description
ASENx (x = 0-4)	x	rw	**Arbitration Slot x Enable** Each bit enables an arbitration slot of the arbiter round. ASEN0 enables the arbitration slot 0, ASEN1 the slot 1, etc. If an arbitration slot is disabled, it is considered as being empty. The request bits of the request sources are not modified by write actions to ASENR. 0_B The corresponding arbitration slot is disabled and is not taken into account by the arbiter. Conversions are not requested, even for the request source(s) with pending request bit(s). 1_B The corresponding arbitration slot is enabled. Conversions are requested for the request source(s) with pending request bit(s).
0	[31:5]	r	**Reserved** Read as 0; should be written with 0.

31.2.8.2 Request Source Priority Register

The request source priority registers contain bits to define the request source priority and the conversion start mode.

RSPR0

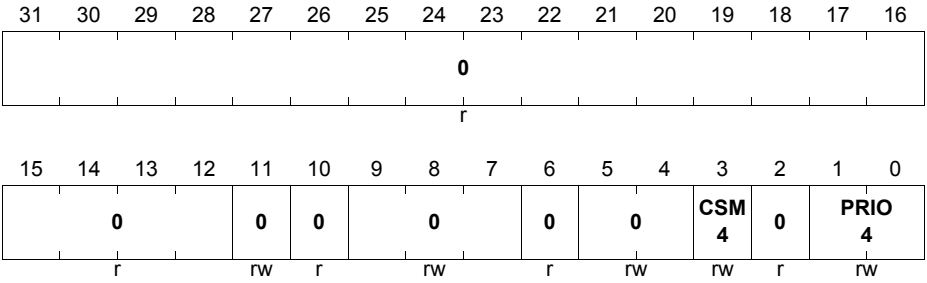
Request Source Priority Register 0 (040_H) **Reset Value: $0000\ 0000_H$**



Field	Bits	Type	Description
PRIO0, PRIO1, PRIO2, PRIO3	[1:0], [5:4], [9:8], [13:12]	rw	**Priority of Request Source x** This bit field defines the priority of the conversion request source x, located in arbitration slot x. 00_B Lowest priority is selected. ... 11_B Highest priority is selected.
CSM0, CSM1, CSM2, CSM3	3, 7, 11, 15	rw	**Conversion Start Mode of Request Source x** This bit defines the conversion start mode of the conversion request source x, located in arbitration slot x. 0_B The wait-for-start mode is selected. 1_B The cancel-inject-repeat mode is selected.
0	2, 6, 10, 14, [31:16]	r	**Reserved** Read as 0; should be written with 0.

RSPR4

Request Source Priority Register 4 (044_H) **Reset Value: $0000\ 0000_H$**



Field	Bits	Type	Description
PRIO4	[1:0]	rw	**Priority of Request Source 4** This bit field defines the priority of the conversion request source 4, located in arbitration slot 4. 00_B Lowest priority is selected. ... 11_B Highest priority is selected.
CSM4	3	rw	**Conversion Start Mode of Request Source 4** This bit defines the conversion start mode of the conversion request source 4, located in arbitration slot 4. 0_B The wait-for-start mode is selected. 1_B The cancel-inject-repeat mode is selected.
0	[5:4], [9:7], 11	rw	**Reserved** These bits are reserved for future use and have to be written with 000_B.
0	2, 6, 10, [31:12]	r	**Reserved** Read as 0; should be written with 0.

31.2.9 Scan Request Source Handling

A scan request source can issue conversion requests for a sequence of up to 16 input channels. It can be programmed individually for each input channel if it takes part in the scan sequence. The scan sequence always starts with the highest enabled channel number and continues towards lower channel numbers (order defined by the channel number, each channel can be converted only once per sequence).

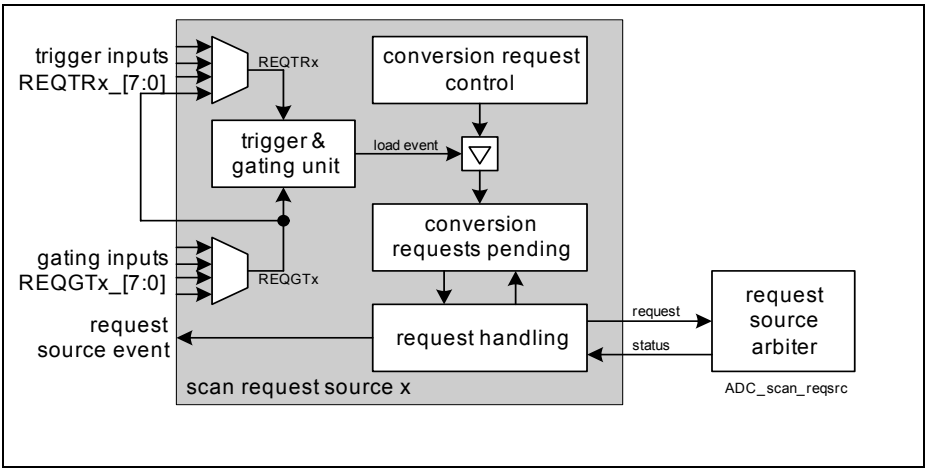


Figure 31-9 Scan Request Source

31.2.9.1 Overview

A scan request source performs the:

- Conversion request control:
  The conversion request control defines if an analog input channel takes part in the scan sequence (see bits in registers **CRCR1**, **CRCR3**). The programmed register value is kept unchanged by an ongoing scan sequence.
- Conversion request pending:
  The pending conversion requests indicate if an input channel has to be converted in an ongoing scan sequence (see bits in registers **CRPR1**, **CRPR3**). A conversion request can only be issued to the request source arbiter if at least one pending bit is set. With each conversion start that has been triggered by the scan request source, the corresponding pending bit is automatically cleared. The scan sequence is considered finished and a request source event is generated if the last conversion triggered by the scan source is finished and all pending bits have been cleared.
- Request handling:
  The request handling blocks interfaces with the request source arbiter. It requests conversion due to pending bits in the scan sequence and handles the conversion

status information. If a conversion triggered by the scan request source is aborted due to a conversion request from another request source with a higher priority, the corresponding pending bit is automatically set. This mechanism ensures that an aborted conversion takes part in the next arbitration round and does not get lost. The control of the scan sequence is done based on bits in registers **CRMR1**, **CRMR3**.

- Trigger and gating signal handling:
  The trigger and gating unit interfaces with signals and modules outside the ADC module that can request conversions. For example, a timer unit can issue a request signal to synchronize conversions to PWM events. A load event starts a scan sequence by modifying the request pending bits according to the request control bits.

31.2.9.2 Scan Sequence Operation

To **operate a scan request source**, the following aspects should be taken into account:

- The bits in register CRCRx have to be programmed to define the channels participating in the scan sequence.
- If a trigger or gating function by external signals is desired, the gating and trigger inputs have to be defined by bit fields in the related registers **RSIRx (x = 0 - 4)**, the value of x defines the number of the arbitration slot where the scan source is connected. Also the edge selection for the trigger event is done in these registers.
- The gating mechanism has to be defined by CRMRx.ENGT.
- The corresponding arbitration slot has to be enabled to accept conversion requests from the scan source (see register **ASENR**).
- The load event has to be defined by bits in CRMRx to start a scan sequence.
- If a load event occurs while CRMRx.LDM = 0, the content of CRCRx is copied to CRPRx (overwrite). This setting allows starting a new scan sequence and to “forget” remaining pending bits if a load event occurs while a scan sequence is running.
- If a load event occurs while CRMRx.LDM = 1, the content of CRCRx is bit-wisely logical OR-combined to CRPRx (no overwrite). This setting allows starting a new scan sequence without “forgetting” remaining pending bits if a load event occurs while a scan sequence is running.

To **start a scan sequence**, the following mechanisms are supported to generate a load event:

- An external trigger signal can be selected to start a scan sequence controlled by HW by an external module or signal, e.g. a timer unit or an input pin. The trigger feature is enabled by CRMRx.ENTR = 1. The load event is generated if the selected edge is detected at the selected trigger input REQTRx. The edge selection is done in register RSIRx.
- A load event is generated under SW control by writing CRMRx.LDEV = 1. This mechanism starts a scan sequence without modifying the bits in register CRCRx. A data write action to CRCRx does not lead to a load event (first prepare the channel control, then start the sequence).

- If SW writes data to register CRPRx, the written data is stored in register CRCRx and a load event is generated automatically. This mechanism starts a scan sequence with the channels defined by the written data (the sequence is defined and started with a single data write action, e.g. under DMA control).
- A load event is generated each time a scan sequence has finished and the request source event occurs if bit CRMRx.SCAN = 1. This setting leads to a permanent repetition of the scan sequence.

To **stop or abort an ongoing scan sequence**, the following mechanisms are supported:

- An external gating signal can be selected to stop and to continue a scan sequence at any point in time controlled by an external module or signal, e.g. a timer unit or an input pin. The gating feature can be enabled and the polarity of the gating signal REQGTx can be selected by CRMRx.ENGT. The gating mechanism does not modify the contents of the conversion pending bits, but only prevents the request handling block from issuing conversion requests to the arbiter.
- The arbiter can be disabled by SW for this arbiter slot by clearing the corresponding bit **ASENR**.ASENx. This mechanism does not modify the contents of the conversion pending bits, but only prevents the arbiter from accepting requests from the request handling block.
- The pending request bits can be cleared by writing bit CRMRx.CLRPND = 1. It is recommended to stop the scan sequence before clearing the pending bits.

31.2.9.3 Request Source Event and Interrupt

A request source event of a scan source occurs if the last conversion of a scan sequence is finished (all pending bits = 0). A request source event interrupt can be generated based on a request source event according to the structure shown in **Figure 31-10**. If a request source event is detected, it sets the corresponding indication flag in register **EVFR**. These flags can also be set by writing a 1 to the corresponding bit position, whereas writing 0 has no effect. Additionally, a gated event flag **EVFR**.GFSx indicates that a request source interrupt has been activated. The indication flags can be cleared by SW by writing a 1 to the corresponding bit position in register **EVFCR**.

The service request output ADCy_SRx that is selected by the request source event interrupt node pointer bit fields in register **EVNPR** becomes activated each time the related request source event is detected and the interrupt generation is enabled for this event in registers **CRCR1** (for request source 1) or **CRCR3** (for request source 3).
A service request output can be activated under SW control by writing **INTR**.SISRx.

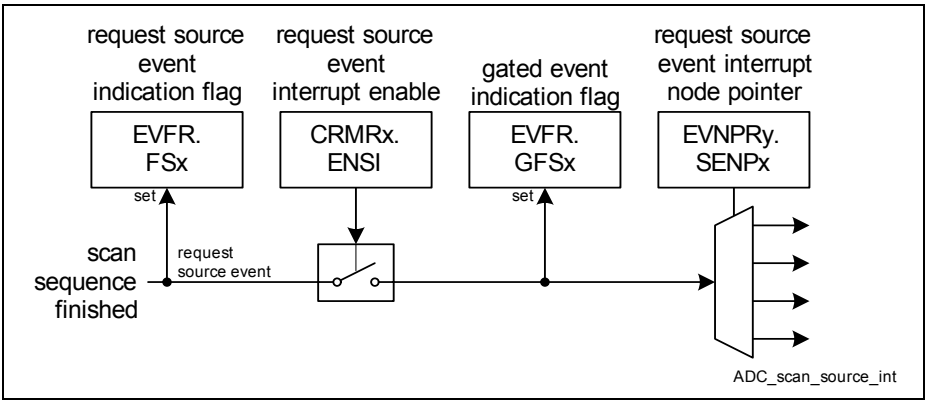


Figure 31-10 Interrupt Generation of a Scan Request Source

31.2.10 Scan Request Source Registers

31.2.10.1 Conversion Request Control Registers

These registers contain the control and status bits of a scan request source. In the TC1798, two scan sources are available (sources 1 and 3). The index describes the number of the arbitration slot where the request source is taking part in the arbitration.

The conversion request control register contains the bits that are copied to the pending register when the load event occurs. This register can be accessed at two different addresses. One address for read and write access is given for CRCRx (attribute “rw”), leading to a data write to the bits in CRCRx without an automatic load event. The second address only used for write actions is given for CRPRx (additional attribute “h”), leading to a data write to the bits in CRCRx with an automatic load event one clock cycle later.

CRCR1
Conversion Request 1 Control Register
(090_H) **Reset Value: 0000 0000$_H$**

CRCR3
Conversion Request 3 Control Register
($0B0_H$) **Reset Value: 0000 0000$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CH 15	CH 14	CH 13	CH 12	CH 11	CH 10	CH 9	CH 8	CH 7	CH 6	CH 5	CH 4	CH 3	CH 2	CH 1	CH 0
rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh

Field	Bits	Type	Description
CHx (x = 0-15)	x	rwh	**Channel Bit x** Each bit corresponds to one analog input channel, the channel number CHx is defined by the bit position x in this register. The corresponding bit x in the conversion request pending register will be overwritten by this bit (LDM = 0) or bit-wisely OR-combined with this bit (LDM = 1) when the load event occurs. 0_B The analog channel CHx will not be requested for conversion by this request source. 1_B The analog channel CHx will be requested for conversion by this request source.
0	[31:16]	r	**Reserved** Read as 0; should be written with 0.

31.2.10.2 Conversion Request Pending Registers

The conversion request pending register contains the bits that are requesting a conversion of the corresponding analog channel.
A read operation to CRPRx delivers the pending bits (attribute “rh”). A write operation to CRPRx leads to a data write to the bits in CRCRx with an automatic load event generation (additional attribute “w”).

CRPR1
Conversion Request 1 Pending Register
(094_H) **Reset Value: $0000\ 0000_H$**

CRPR3
Conversion Request 3 Pending Register
($0B4_H$) **Reset Value: $0000\ 0000_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CHP 15	CHP 14	CHP 13	CHP 12	CHP 11	CHP 10	CHP 9	CHP 8	CHP 7	CHP 6	CHP 5	CHP 4	CHP 3	CHP 2	CHP 1	CHP 0
rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh

Field	Bits	Type	Description
CHPx (x = 0-15)	x	rwh	**Channel Pending Bit x** Write view: A write to this address targets the bits in register **CRCR1** (for CRPR1) or **CRCR3** (for CRPR3). Read view: Each bit corresponds to one analog channel, the channel number CHx is defined by the bit position in the register. 0_B The analog channel CHx is not requested for conversion by this request source. 1_B The analog channel CHx is requested for conversion by this request source.
0	[31:16]	r	**Reserved** Read as 0; should be written with 0.

31.2.10.3 Conversion Request Mode Registers

The conversion request mode registers contain bits to configure the desired operating mode of the scan request sources.

CRMR1
Conversion Request 1 Mode Register
(098_H) **Reset Value: $0000\ 0000_H$**

CRMR3
Conversion Request 3 Mode Register
($0B8_H$) **Reset Value: $0000\ 0000_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0						LDEV	CLRPND	REQGT	0	LDM	SCAN	ENSI	ENTR	ENGT	
r						w	w	rh	r	rw	rw	rw	rw	rw	

Field	Bits	Type	Description
ENGT	[1:0]	rw	**Enable Gate** This bit field enables the gating functionality for the request source. 00_B The request source does not issue conversion requests. 01_B The request source issues conversion requests if at least one pending bit is set. 10_B The request source issues conversion requests if at least one pending bit is set and the selected gating signal REQGTx = 1. 11_B The request source issues conversion requests if at least one pending bit is set and the selected gating signal REQGTx = 0.

Field	Bits	Type	Description
ENTR	2	rw	**Enable External Trigger** This bit enables the external trigger possibility. If enabled, the load event takes place if the selected edge is detected at the external trigger input REQTRx. 0_B The external trigger is disabled. 1_B The external trigger is enabled.
ENSI	3	rw	**Enable Source Interrupt** This bit enables the request source interrupt generation if a request source event occurs (last pending conversion is finished). 0_B The request source interrupt is disabled. 1_B The request source interrupt is enabled.
SCAN	4	rw	**Autoscan Enable** This bit enables a permanent scan functionality. If enabled, the load event is automatically generated if a request source event occurs. 0_B The permanent scan functionality is disabled. 1_B The permanent scan functionality is enabled.
LDM	5	rw	**Load Event Mode** This bit defines the transfer mechanism triggered by the load event. 0_B With the load event, the value of register CRCRx is copied to the pending register CRPRx (overwrite). 1_B With the load event, the value of register CRCRx is bit-wisely logical OR combined to the pending register CRPRx.
REQGT	7	rh	**Request Gate Level** This bit monitors the level at the REQGTx input. 0_B The level is 0. 1_B The level is 1.
CLRPND	8	w	**Clear Pending Bits** 0_B No action. 1_B The bits in register CRPRx are cleared.
LDEV	9	w	**Generate Load Event** 0_B No action. 1_B A load event is generated.

Field	Bits	Type	Description
0	6, [31:10]	r	**Reserved** Read as 0; should be written with 0.

31.2.11 Sequential Request Source Handling

Sequential request sources have been introduced to allow short conversion sequences with freely programmable channel numbers (contrary to a scan request source with a fixed conversion order for the enabled channels). Two versions of the sequential sources are available in each ADC kernel:

- Request sources in arbitration slots 2 and 4:
  These request sources can handle a sequence of up to 4 input channels (4-stage queue for 4 entries). This mechanism could be used to support application-specific conversion sequences, especially for timing-critical sequences containing multiple conversions of the same channel.
- Request source in arbitration slot 0:
  This request source can handle a single input channel (1-stage queue for 1 entry). This mechanism could be used for SW-controlled conversion requests or HW-triggered conversions of a single input channel (to “inject” a single conversion into a running sequence).

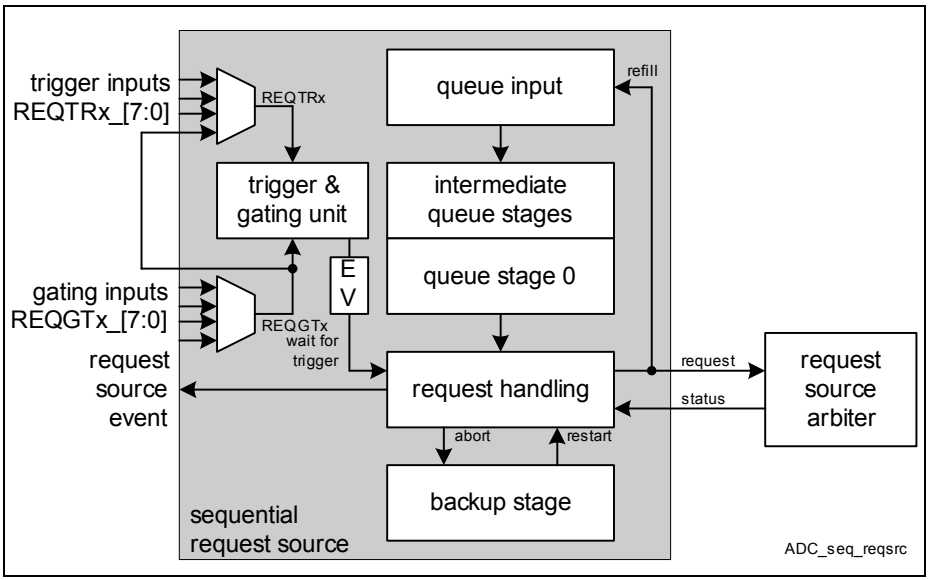


Figure 31-11 Sequential Request Source

The internal structure and the handling of the sequential sources is similar for both versions. The programmed sequence is stored in a queue buffer (based on a FIFO mechanism) with at least one queue stage (stage 0) and a backup stage for aborted conversions. The only difference between both versions is given by the number of intermediate queue stages for storing the sequence. The request source in arbitration

slot 0 does not provide intermediate queue stages (1-stage queue with only queue stage 0), whereas the ones in arbitration slots 2 and 4 provides 3 intermediate queue stages in additional to queue stage 0 (leading to a 4-stage queue each).

31.2.11.1 Overview

A sequential request source performs the:

- Queue input:
  The queue input represents the programming interface where the sequence is defined (see **QINR0**, **QINR2**, **QINR4**). It does not provide any buffer capability, but handles the filling of the queue buffer (queue stage 0 plus optional intermediate queue stages) by writing data to it. The contents of the queue stages can not be directly modified by program, except by the command for flushing the complete queue.
  The queue input also handles the refill mechanism, an automatic re-insertion of a started conversion from queue stage 0 (including the control parameters) as new queue input. This feature allows a single setup (by SW) of a conversion sequence and multiple repetitions of the same sequence without the need to re-program it each time. A conversion sequence is repeated if all queue entries of the sequence are setup for refill mode.
- Queue stage 0:
  The contents of this queue stage defines which channel will be requested next for a conversion (see **Q0R0**, **Q0R2**, **Q0R4**). It also defines if the request should be triggered by an external event or if the requested conversion should follow the previous one as soon as possible. It also enables the request source interrupt generation after the conversion.
  The contents of this queue stage is cleared when the requested conversion is started and the next queue entry can be handled (if available).
- Queue backup stage:
  The queue backup stage is used to store the request control parameters when a conversion requested by this request source is aborted. A validation bit indicates that the aborted conversion has to be requested next (before the current contents of queue stage 0) to maintain the original sequence (see **QBUR0**, **QBUR2**, **QBUR4**).
- Request handling:
  The request handling block interfaces with the request source arbiter. It requests a conversion due to a valid information in queue stage 0 and handles the conversion status information. The control of the queue sequence is done based on bits in registers **QMR0**, **QMR2**, and **QMR4** (for the arbitration slot x).
- Trigger and gating signal handling:
  The trigger and gating unit interfaces with signals and modules outside the ADC module that can request conversions. For example, a timer unit can issue a request signal to synchronize conversions to PWM events. A trigger event can start a conversion request for the entry in queue stage 0 (see **QMR0**, **QMR2**, **QMR4**). An

event flag QSRx.EV indicates that a trigger event has been detected (selected edge of selected trigger input signal REQTRx if enabled by QMRx.ENTR or write action with QMRx.TREV = 1). This bit is cleared with each conversion start requested by this source or by writing bits CEV = 1, FLUSH = 1, or CLRV = 1.

31.2.11.2 Sequential Source Operation

To **operate a sequential request source**, the following aspects should be taken into account:

- The sequence has to be initialized by writing to the queue input **QINR0** (for arbitration slot 0), **QINR2** (for arbitration slot 2), or **QINR4** (for arbitration slot 4) when using the refill mechanism. Each write access corresponds to one conversion request.
  The desired sequence should be completely initialized before enabling the request source, because with enabled refill feature, write accesses by SW to QINRx are not allowed.
- If a trigger or gating function by external signals is desired, the gating and trigger inputs have to be defined by bit fields in the related registers **RSIRx (x = 0 - 4)**, the value of x defines the number of the arbitration slot where the request source is connected. Also the edge selection for the trigger event is done in these registers.
- The gating mechanism has to be defined by QMRx.ENGT.
- The corresponding arbitration slot has to be enabled to accept conversion requests from the sequential source (see register **ASENR**).

To **start a sequence** of a sequential request source, the following mechanisms are supported:

- An external trigger signal can be selected to start a scan sequence controlled by HW by an external module or signal, e.g. a timer unit or an input pin. The trigger feature is enabled by QMRx.ENTR = 1. The trigger event is generated if the selected edge is detected at the selected trigger input.
- A trigger event is generated under SW control by writing QMRx.TREV = 1. This mechanism starts a request if queue stage 0 contains valid data (or the queue backup stage respectively).
- A write operation to a queue input leads to a (new) valid queue entry. If the queue is empty (no valid entry), the written data arrives in queue stage 0 and starts a conversion request (if enabled by QMRx.ENGT and without waiting for an external trigger). If the refill mechanism is used, the queue inputs must not be written while the queue is running. Write operations to a completely filled queue are ignored.

To **stop or abort an ongoing sequence** of a sequential request source, the following mechanisms are supported:

- An external gating signal can be selected to stop and to continue a sequence at any point in time controlled by an external module or signal, e.g. a timer unit or an input pin. The gating feature can be enabled and the polarity of the gating signal REQGTx can be selected by QMRx.ENGT. The gating mechanism does not modify the queue

entries, but only prevents the request handling block from issuing conversion requests to the arbiter.

- The arbiter can be disabled by SW for this arbiter slot by clearing the corresponding bit **ASENR**.ASENx. This mechanism does not modify the queue entries, but only prevents the arbiter from accepting requests from the request handling block.
- The next pending queue entry is cleared by writing bit QMRx.CLRV = 1. It is recommended to stop the sequence before clearing a queue entry (ENGT = 00_B). If the queue backup stage contains a valid entry, this one is cleared, otherwise a valid entry in queue register 0 is cleared.
- All queue entries are cleared by writing bit QMRx.FLUSH = 1. It is recommended to stop the sequence before clearing queue entries.

31.2.11.3 Request Source Event and Interrupt

A request source event occurs when a conversion that has been requested by this source is completely finished. The interrupt enable bits are located in the queue 0 register (if this has not been a repeated start after an abort) or in the queue backup register (if this has been a repeated start after an abort), e.g. see **Q0R0** for request source 0) or in the queue backup register (if this has been a repeated start after an abort, e.g. see **QBUR0** for request source 0).
A request source event interrupt can be generated based on a request source event according to the structure shown in **Figure 31-12**. If a request source event is detected, it sets the corresponding indication flag in register **EVFR**. These flags can also be set by writing a 1 to the corresponding bit position, whereas writing 0 has no effect. The indication flags can be cleared by SW by writing a 1 to the corresponding bit position in register **EVFCR**.

The service request output ADCy_SRx that is selected by the request source event interrupt node pointer bit fields in register **EVNPR** becomes activated each time the related request source event is detected.
A service request output can be activated under SW control by writing **INTR**.SISRx.

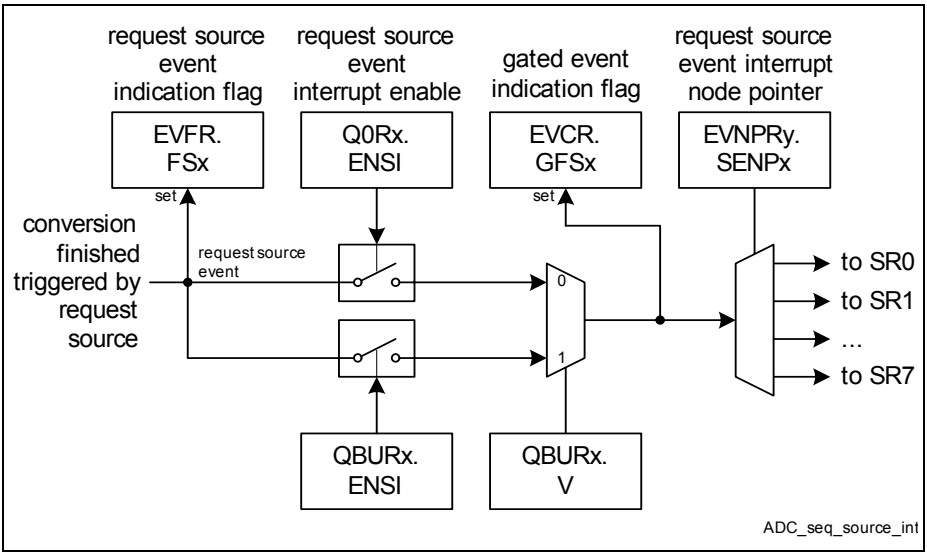


Figure 31-12 Interrupt Generation of a Sequential Request Source

31.2.12 Sequential Source Registers

31.2.12.1 Queue Mode Registers

These registers contain the control and status bits of a sequential source. The index describes the number of the arbitration slot where the request source is taking part in the arbitration.

*Note: Before SW modifies the queue content by QMRx.CLRV or QMRx.FLUSH, all HW actions related to this queue have to be finished. Therefore, the arbitration slot has to be disabled and SW has to wait for at least two arbitration rounds (to be sure that this request source can no longer be an arbitration winner). Then, it has to check **GLOBSTR**.CRSC and **GLOBSTR**.BUSY to be sure that a conversion triggered by this request source is no longer running. Then SW can read QBURx and Q0Rx and can start modification of the queue content.*

QMR0
Queue 0 Mode Register **(080_H)** **Reset Value: $0000\ 0000_H$**
QMR2
Queue 2 Mode Register **($0A0_H$)** **Reset Value: $0000\ 0000_H$**
QMR4
Queue 4 Mode Register **($0C0_H$)** **Reset Value: $0000\ 0000_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0				CEV	FLUSH	TREV	CLRV	0					ENTR	ENGT	
r				w	w	w	w	r					rw	rw	

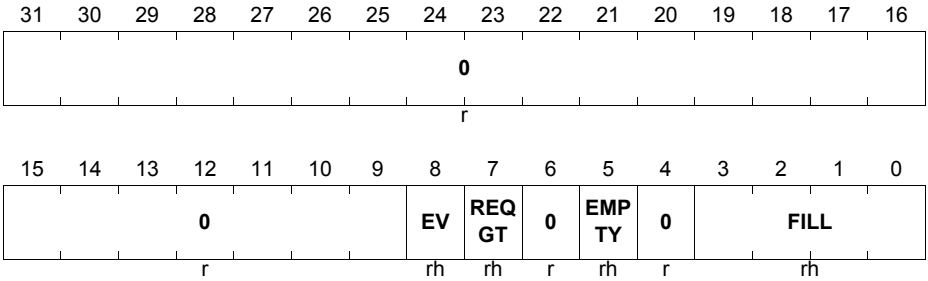
Field	Bits	Type	Description
ENGT	[1:0]	rw	**Enable Gate** This bit field enables the gating functionality for the request source. 00_B The request source does not issue conversion requests. 01_B The request source issues conversion requests if a valid conversion request is pending in the queue 0 register or in the backup register. 10_B The request source issues conversion requests if a valid conversion request is pending in the queue 0 register or in the backup register and the selected gating signal REQGTx = 1. 11_B The request source issues conversion requests if a valid conversion request is pending in the queue 0 register or in the backup register and the selected gating signal REQGTx = 0.
ENTR	2	rw	**Enable External Trigger** This bit enables the external trigger possibility. 0_B The external trigger is disabled and the trigger event is not generated. 1_B The external trigger is enabled and a trigger event is generated if the selected edge is detected at the selected trigger input signal for REQTRx.
CLRV	8	w	**Clear V Bit** 0_B No action. 1_B The next pending valid queue entry in the sequence and the event flag EV are cleared. If there is a valid entry in the queue backup register (QBURx.V = 1), this entry is cleared, otherwise the entry in queue register 0 is cleared.

Field	Bits	Type	Description
TREV	9	w	**Trigger Event** 0_B No action. 1_B A trigger event is generated by SW. If the a valid entry in the request source waits for a trigger event, a conversion request is started.
FLUSH	10	w	**Flush Queue** 0_B No action. 1_B All entries in the queue (including the backup stage) and the event flag EV are cleared. The queue contains no more valid entry.
CEV	11	w	**Clear Event Flag** 0_B No action. 1_B Bit EV is cleared.
0	[7:3], [31:12]	r	**Reserved** Read as 0; should be written with 0.

31.2.12.2 Queue Status Registers

The queue status registers contain bits indicating the status of the sequential source. The filling level and the empty information refer to the queue intermediate stages (if available) and to the queue register 0. An aborted conversion stored in the backup stage is not indicated by these bits (therefore, see QBURx.V).

QSR0
Queue 0 Status Register **(084_H)** **Reset Value: 0000 0020_H**
QSR2
Queue 2 Status Register **($0A4_H$)** **Reset Value: 0000 0020_H**
QSR4
Queue 4 Status Register **($0C4_H$)** **Reset Value: 0000 0020_H**



Field	Bits	Type	Description
FILL	[3:0]	rh	**Filling Level**[1)] This bit field indicates how many queue entries are valid in the sequential source. It is incremented each time a new entry is written to QINRx or by an enabled refill mechanism. It is decremented each time a requested conversion has been started. A new entry is ignored if the filling level has reached its maximum value. 00_B EMPTY = 1:There is no valid entry in the queue. EMPTY = 0:There is 1 valid entries in the queue. 01_B There are 2 valid entries in the queue. 10_B There are 3 valid entries in the queue. 11_B There are 4 valid entries in the queue.

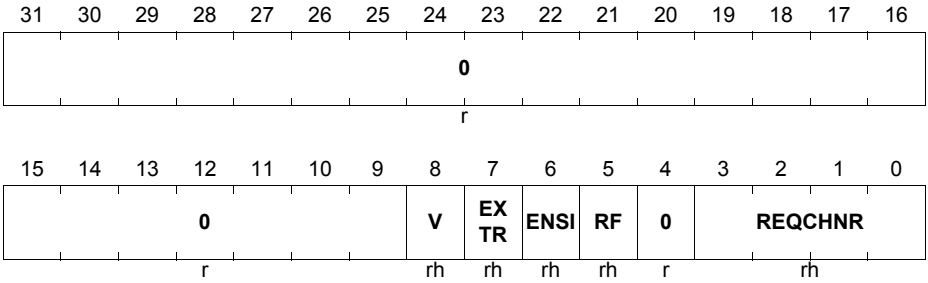
Field	Bits	Type	Description
EMPTY	5	rh	**Queue Empty** This bit indicates if the sequential source contains valid entries. 0_B There are FILL+1 valid entries in the queue. 1_B There are no valid entries (queue is empty).
REQGT	7	rh	**Request Gate Level** This bit monitors the level at the REQGTx input. 0_B The level is 0. 1_B The level is 1.
EV	8	rh	**Event Detected** This bit indicates that an event has been detected while at least one valid entry has been in the queue (queue register 0 or backup stage). Once set, this bit is cleared automatically when the requested conversion is started. 0_B A trigger event has not been detected. 1_B A trigger event has been detected.
0	4, 6, [31:9]	r	**Reserved** Read as 0; should be written with 0.

1) This bit field is always 00_B for the 1-stage queue in arbitration slot 0.

31.2.12.3 Queue 0 Registers

The queue x registers 0 monitor the status of the current sequential request (queue stage 0).

Q0R0
Queue 0 Register 0 **(088_H)** **Reset Value: 0000 0000$_H$**
Q0R2
Queue 2 Register 0 **($0A8_H$)** **Reset Value: 0000 0000$_H$**
Q0R4
Queue 4 Register 0 **($0C8_H$)** **Reset Value: 0000 0000$_H$**



Field	Bits	Type	Description
REQCHNR	[3:0]	rh	**Request Channel Number** This bit field indicates the channel number that will be or is currently requested.
RF	5	rh	**Refill** This bit indicates if the pending request is discarded after the conversion start or if it is automatically refilled into the queue input of the request queue. 0_B The request is discarded after the conversion start. 1_B The request is refilled into the queue after the conversion start.
ENSI	6	rh	**Enable Source Interrupt** This bit indicates if a request source interrupt is generated when the conversion is finished. 0_B The request source interrupt generation is disabled. 1_B The request source interrupt generation is enabled.

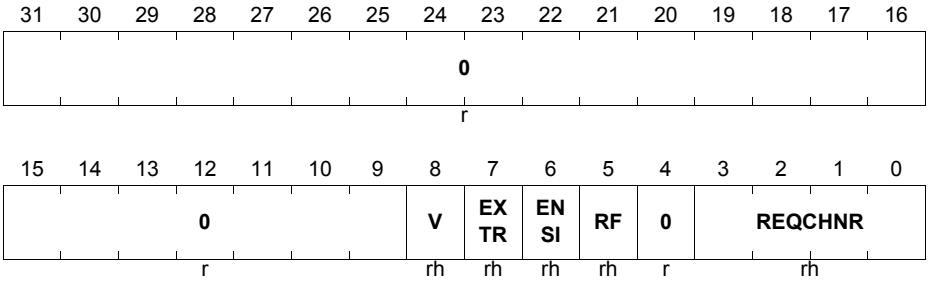
Field	Bits	Type	Description
EXTR	7	rh	**External Trigger** This bit indicates if a valid queue entry immediately leads to a conversion request or if the request handler waits for a trigger event. 0_B The request handler does not wait for a trigger event. 1_B The request handler waits for a trigger event.
V	8	rh	**Request Channel Number Valid** This bit indicates if the queue register 0 contains a valid queue entry. 0_B The queue entry is not valid and does not lead to a conversion request. 1_B The queue entry is valid and leads to a conversion request.
0	4, [31:9]	r	**Reserved** Read as 0; should be written with 0.

31.2.12.4 Queue Backup Registers

The queue backup registers monitor the status of an aborted sequential request.

The registers QBURx and QINRx share the same register address. A read operation at this register address will deliver the “rh” bits of register QBURx. A write operation to this address will target register QINRx.

QBUR0
Queue 0 Backup Register **($08C_H$)** **Reset Value: 0000 0000_H**
QBUR2
Queue 2 Backup Register **($0AC_H$)** **Reset Value: 0000 0000_H**
QBUR4
Queue 4 Backup Register **($0CC_H$)** **Reset Value: 0000 0000_H**



Field	Bits	Type	Description
REQCHNR	[3:0]	rh	**Request Channel Number** This bit field contains the channel number of an aborted conversion that has been requested by this request source.
RF	5	rh	**Refill** This bit contains the refill bit of an aborted conversion that has been requested by this request source.
ENSI	6	rh	**Enable Source Interrupt** This bit contains the request source event interrupt enable bit of an aborted conversion that has been requested by this request source.

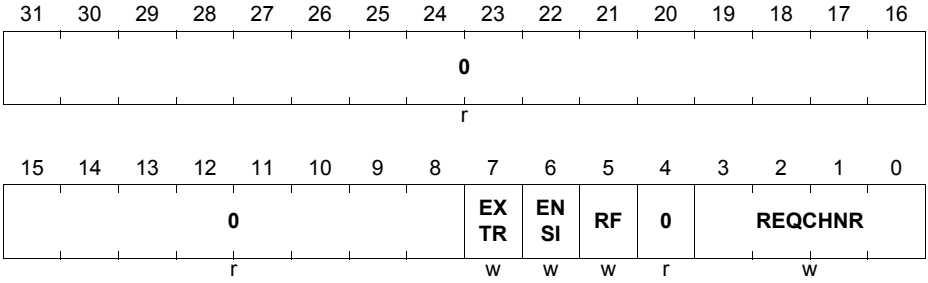
Field	Bits	Type	Description
EXTR	7	rh	**External Trigger** This bit contains the external trigger bit of an aborted conversion that has been requested by this request source.
V	8	rh	**Request Channel Number Valid** This bit indicates if the entry in the queue backup register is valid (REQCHNR, RF, TR and ENSI are valid). Bit V is set if a running conversion that has been requested by this request source is aborted. It is cleared when the repeated conversion is started. 0_B The backup register does not contain a valid entry. 1_B The backup register contains a valid entry. It will be requested before a valid entry in queue register 0 will be requested.
0	4, [31:9]	r	**Reserved** Read as 0; should be written with 0.

31.2.12.5 Queue Input Registers

The queue input registers are the entry registers for sequential requests for each sequential source (queue).

The registers QBURx and QINRx share the same register address. A read operation at this register address will deliver the “rh” bits of register QBURx. A write operation to this address will target the “w” bits in register QINRx.

QINR0
Queue 0 Input Register **($08C_H$)** **Reset Value: $0000\ 0000_H$**
QINR2
Queue 2 Input Register **($0AC_H$)** **Reset Value: $0000\ 0000_H$**
QINR4
Queue 4 Input Register **($0CC_H$)** **Reset Value: $0000\ 0000_H$**



Field	Bits	Type	Description
REQCHNR	[3:0]	w	**Request Channel Number** This bit field defines the requested channel number.
RF	5	w	**Refill** This bit defines the refill functionality for this queue entry. 0_B The content of this queue entry is not entered again in QINRx when the related conversion is started. 1_B The content of this queue entry is automatically entered again in QINRx when the related conversion is started.

Field	Bits	Type	Description
ENSI	6	w	**Enable Source Interrupt** This bit defines the request source event interrupt functionality. 0_B A request source event interrupt is not generated if the related conversion is finished. 1_B A request source event interrupt is generated if the related conversion is finished.
EXTR	7	w	**External Trigger** This bit defines the external trigger functionality. 0_B A valid queue entry immediately leads to a conversion request. 1_B A valid queue entry waits for a trigger event to occur before issuing a conversion request.
0	4, [31:8]	r	**Reserved** Read as 0; should be written with 0.

31.2.13 Channel-Related Functions

The channel control unit defines the conversion settings, that can be programmed individually for each analog input channel. Therefore, a channel control register **CHCTRx (x = 0 - 15)** is associated to each analog input channel CHx. After the arbiter has determined the channel to be converted, the defined settings are applied to the AD converter, comprising information about:

- **Conversion parameters:**
  Bit field ICLSEL defines which input class is taken into account for the conversion (see **Section 31.2.13.1**).
- **Reference selection:**
  Bit field REFSEL defines which reference input is used for the conversion (see **Section 31.2.13.2**)
- **Channel event handling:**
  Bit fields LCC, BNDASEL, and BNDBSEL define which boundaries are used for limit checking (see **Section 31.2.13.4**) and which channel event leads to a channel event interrupt (see **Section 31.2.13.5**).
- **Synchronous conversion request:**
  Bit SYNC defines if the channel triggers a synchronized conversion (see **Section 31.2.19**).
- **Alias feature:**
  In addition to the general channel control, the ADC kernel supports a mechanism (named alias feature, see **Section 31.2.13.3**) to redirect a conversion request to another channel number.

31.2.13.1 Input Classes

An input class defines the length of the sample phase and the resolution of the conversion. In most applications, the characteristics of the input circuitries (RC input low-pass filter and impedance of the signal source) are quite similar for several analog input signals, leading to similar timings for the sample phase of these channels. As a consequence, input channels with similar parameters can be grouped together to form an input class.
All channels with the same ICLSEL setting belong to the same input class and have the same sample phase length and resolution. In the TC1798, 4 input classes are supported. Registers **INPCRx (x = 0 - 3)** can be programmed to adjust the sample time and the resolution to the application requirements independently for each input class.
The default setting of these registers lead to the minimum sample phase length of 2 f_{ADCI} cycles and conversions with 10 bits resolution. If this default setting fits to the application requirements, bit fields **CHCTRx (x = 0 - 15)**.ICLSEL and registers **INPCRx (x = 0 - 3)** need not to be changed.

31.2.13.2 Reference Selection

The conversion result of the ADC is always referring to a reference voltage. The maximum digital result value (full scale) is obtained if the analog input voltage equals the reference voltage. In order to support more than one measurement range with full scale digital representation, the user can select between the standard reference input V_{AREF} and an alternative reference input at the analog input channel CH0 for each ADC kernel. The reference selection can be individually programmed for each input channel.
This feature can be used to connect 5 V based sensors and 3.3 V based sensors to the same ADC kernel. In this case, one set of input channels refers to the standard reference input, whereas the other one refers to the voltage level at input CH0.
Please note that the smallest granularity 1 LSB_n for n bit resolution refers to the selected reference voltage. The granularity becomes very small if a low reference voltage is applied, and as a consequence, the resulting TUE increases due to noise effects. Therefore it is recommended to avoid small reference voltages.

31.2.13.3 Alias Feature

The ADC kernel provides an alias feature, allowing a re-direction of conversion requests for channels CH0 or CH1 to other channel numbers. This feature can be used to measure the same input channel and to store the conversion results in two different result registers.

- The same signal can be measured twice without the need to read out the conversion result to avoid data loss. This allows triggering both conversions quickly one after the other and being independent from CPU interrupt latency.
- The sensor signal is connected to only one input channel (instead of two analog inputs). This saves input pins in low-cost applications and only the leakage of one input has to be considered in the error calculation.
- Even if the analog input CH0 is used as alternative reference (see **Figure 31-13**), the internal trigger and data handling features for channel CH0 can be used.
- The channel settings for both conversions can be different (boundary values, interrupts, etc.).
- If a sequential conversion request source has been set up, a conversion request for channels CH0 or CH1 can be easily directed to other input channels without flushing the queue.

In typical low-cost AC-drive applications, only one common current sensor is used to determine the phase currents. Depending on the applied PWM pattern, the measured value has different meanings and the sample points have to be precisely located in the PWM period. **Figure 31-13** shows an example where the sensor signal is connected to one input channel (CHx) but two conversions are triggered for two different channels (CHx and CH0). With the alias feature, a conversion request for CH0 leads to a conversion of the analog input CHx instead of CH0, but taking into account the settings for CH0. Although the same analog input (CHx) has been measured, the conversion

results can be stored and read out from the result registers RESRx (conversion triggered for CHx) and RESRy (conversion triggered for CH0). Additionally, different interrupts or limit boundaries can be selected, enabled or disabled.

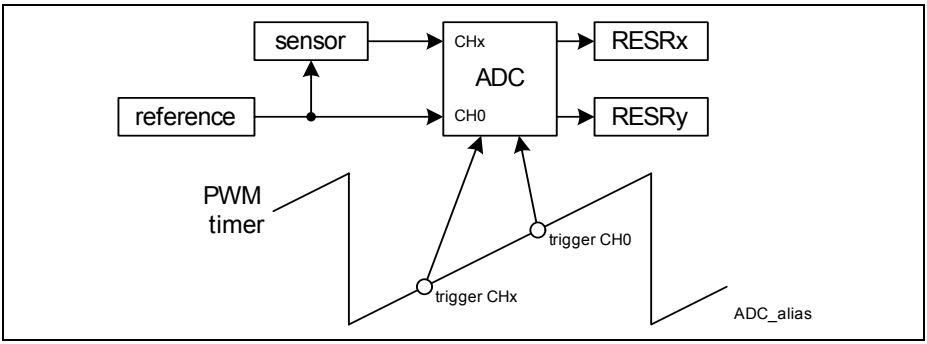


Figure 31-13 Alias Feature

31.2.13.4 Limit Checking

The limit checking mechanism automatically compares each conversion result to two boundary values (boundaries A and B). For each channel, the user can select these boundaries from a set of 4 programmable values (**LCBR0** to **LCBR3**).
With this structure, the conversion result range is split into three areas:

- Area I: The conversion result is below or equal to both boundaries.
- Area II: The conversion result is above one boundary and below or equal to the other boundary.
- Area III: The conversion result is above both boundaries.

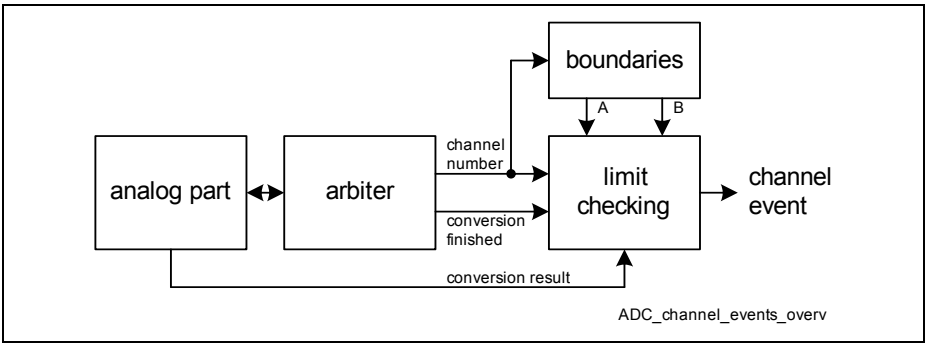


Figure 31-14 Channel Event Generation

Bit field LCC in the channel control register defines the condition to generate a channel event, leading to a channel event interrupt:

- LCC = 000_B: No trigger, the channel event generation is disabled.
- LCC = 001_B: A channel event is generated if the conversion result is not in area I.
- LCC = 010_B: A channel event is generated if the conversion result is not in area II.
- LCC = 011_B: A channel event is generated if the conversion result is not in area III.
- LCC = 100_B: A channel event is always generated (regardless of the boundaries).
- LCC = 101_B: A channel event is generated if the conversion result is in area I.
- LCC = 110_B: A channel event is generated if the conversion result is in area II.
- LCC = 111_B: A channel event is generated if the conversion result is in area III.

Figure 31-15 shows an example for limit checking where channel events are generated only if the conversion results are not in the normal operating range defined by area II (LCC = 010_B).

Typical applications for limit checking are temperature monitoring or overcurrent sensing. As long as the measured temperature value is below a boundary value, the CPU does not need to be informed. In this case, a channel event should be generated only if the conversion result is in area III (LCC = 111_B) to indicate an over-temperature condition. If the conversion of the analog temperature input signal is part of an auto-scan sequence autonomously triggered on a regular time base, the CPU load for the temperature monitoring is zero until the over-temperature condition is detected.

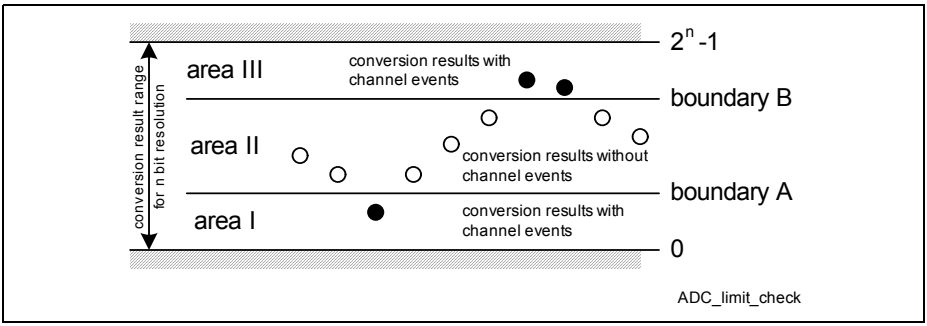


Figure 31-15 Limit Checking

Note: It is also possible to select the same boundary register for boundaries A and B. In this case, the conversion result range is split into two ranges (area II is empty).

31.2.13.5 Channel Event Interrupts

A channel event interrupt can be generated based on a channel event according to the structure shown in **Figure 31-16**. If a channel event is detected, it sets the corresponding indication flag FCx in register **CHFR**. These flags can also be set by writing a 1 to the corresponding bit position, whereas writing 0 has no effect. The indication flags can be cleared by SW by writing a 1 to the corresponding bit position in register **CHFCR**.

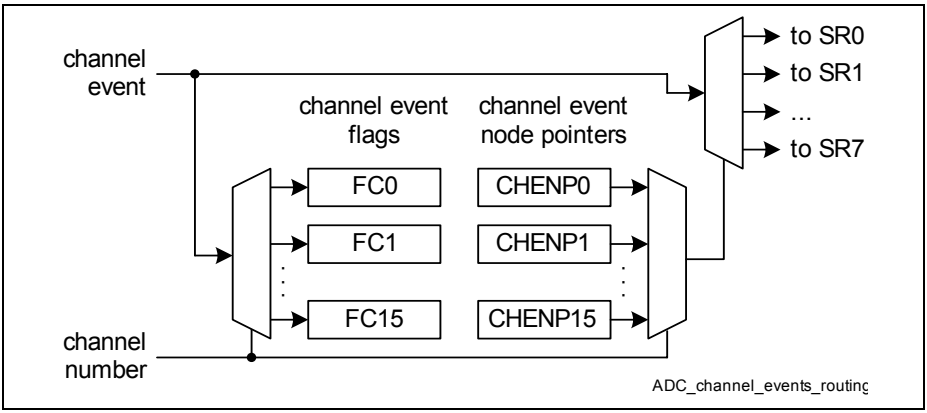


Figure 31-16 Channel Event Interrupt Generation

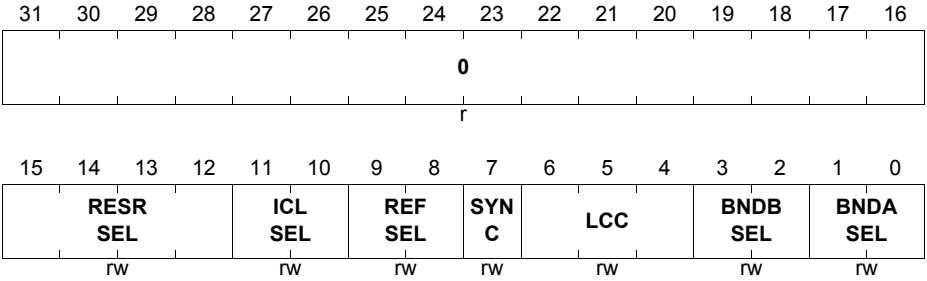
The service request output ADCy_SRx that is selected by the channel node pointer bit fields in registers **CHENPR0**, or **CHENPR8** is activated each time the related channel event is detected.
A service request output can be activated under SW control by writing **INTR**.SISRx.

31.2.14 Channel-Related Registers

31.2.14.1 Channel Control Registers

The channel control registers contain bits to select the targeted result register, to control the limit check mechanism and to select an input class.
The channel control register 0 defines the settings for the input channel 0, etc.

CHCTRx (x = 0 - 15)
Channel x Control Register **(100_H + x * 4)** **Reset Value: 0000 0000_H**



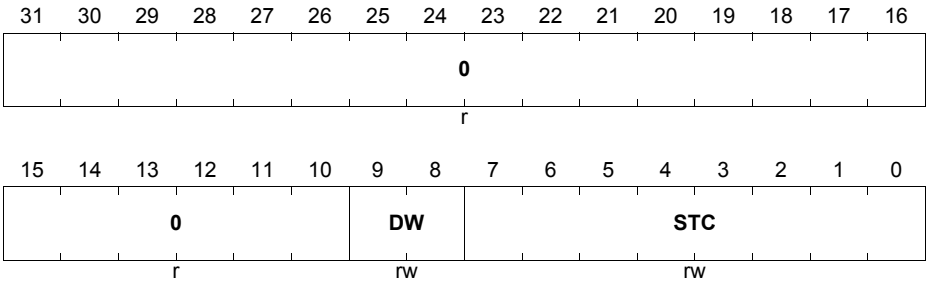
Field	Bits	Type	Description
BNDASEL	[1:0]	rw	**Boundary A Selection** This bit field defines which boundary will be taken as boundary A for the limit checking. 00_B The value given by LCBR0 is selected. 01_B The value given by LCBR1 is selected. 10_B The value given by LCBR2 is selected. 11_B The value given by LCBR3 is selected.
BNDBSEL	[3:2]	rw	**Boundary B Selection** This bit field defines which boundary will be taken as boundary B for the limit checking. 00_B The value given by LCBR0 is selected. 01_B The value given by LCBR1 is selected. 10_B The value given by LCBR2 is selected. 11_B The value given by LCBR3 is selected.
LCC	[6:4]	rw	**Limit Check Control** This bit field defines the behavior of the limit checking mechanism. Please refer to the coding in **Section 31.2.13.4** on **Page 31-78**.

Field	Bits	Type	Description
SYNC	7	rw	**Synchronization Request** This bit defines if a conversion request for this channel leads to a synchronized (parallel) conversion with other ADC kernels. This bit is only taken into account if the ADC kernel is a potential conversion master (**SYNCTR**.STSEL = 00), otherwise it is considered to be 0. 0_B This channel does not request a synchronized conversion. 1_B This channel requests a synchronized conversion if the ADC kernel is a potential synchronization master.
REFSEL	[9:8]	rw	**Reference Input Selection** This bit field defines the reference source for this channel. 00_B The standard reference input V_{AREF} is selected. 01_B The alternative reference input CH0 is selected. 10_B reserved, do not use 11_B reserved, do not use
ICLSEL	[11:10]	rw	**Input Class Selection** These bits are used to select the input class. 00_B The input class 0 is selected. 01_B The input class 1 is selected. 10_B The input class 2 is selected. 11_B The input class 3 is selected.
RESRSEL	[15:12]	rw	**Result Register Selection** This bit field defines which result register will be the target of a conversion of this channel. 0_H Result register 0 is selected. 1_H Result register 1 is selected. ... F_H Result register 15 is selected.
0	[31:16]	r	**Reserved** Read as 0; should be written with 0.

31.2.14.2 Input Class Registers

The input class registers contain bits to control the sample time and the resolution for each input class.
The input class register 0 defines the settings for the input class 0, etc.

INPCRx (x = 0 - 3)
Input Class Register x **(050_H + x * 4)** **Reset Value: 0000 0000_H**

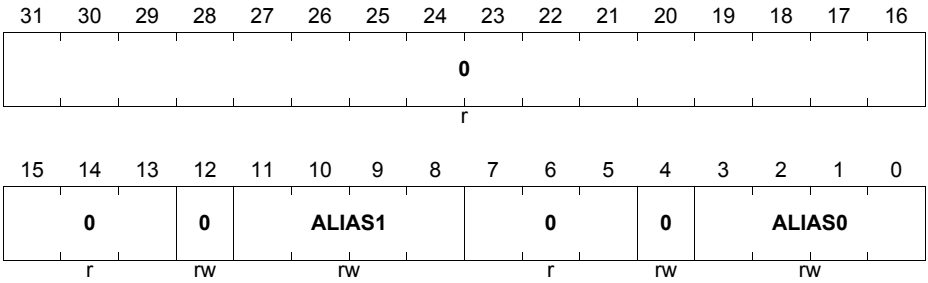


Field	Bits	Type	Description
STC	[7:0]	rw	**Sample Time Control** This bit field defines the additional length of the sample phase, given in analog clock cycles f_{ADCI}. A minimum sample phase of 2 analog clock cycles is extended by the programmed value. sample phase length = (2 + STC) / f_{ADCI}
DW	[9:8]	rw	**Data Width** This bit field defines how many bits are converted for the result. The MSBs of conversion results with different DW settings are left aligned in the result bit fields. Bit positions that are not converted are 0. 00_B The result is 10 bits wide. 01_B The result is 12 bits wide. 10_B The result is 8 bits wide. 11_B reserved
0	[31:10]	r	**Reserved** Read as 0; should be written with 0.

31.2.14.3 Alias Register

The alias register contains bits to change a requested channel number from CH0 and CH1 to another channel number, see also **Section 31.2.13.3**. The programmed alias channel number is replacing the internally requested number for analog input multiplexer (of the converter). The internally requested channel number is taken into account for all other internal actions and the synchronization request.

ALR0
Alias Register 0 **(210_H)** **Reset Value: $0000\ 0100_H$**

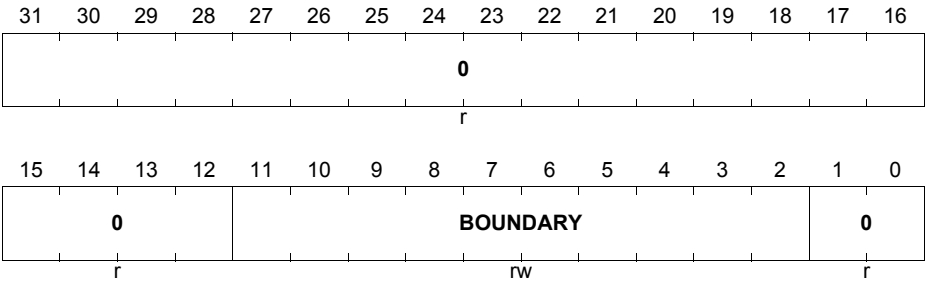


Field	Bits	Type	Description
ALIAS0	[3:0]	rw	**Alias Value for CH0 Conversion Requests** The channel indicated in this bit field is converted instead of channel CH0. The conversion is done with the settings defined for channel CH0.
ALIAS1	[11:8]	rw	**Alias Value for CH1 Conversion Requests** The channel indicated in this bit field is converted instead of channel CH1. The conversion is done with the settings defined for channel CH1.
0	4, 12	rw	**Reserved for Future Use** Bit is reserved for future use and has to be written with 0_B.
0	[7:5], [31:13]	r	**Reserved** Read as 0; should be written with 0.

31.2.14.4 Limit Check Boundary Registers

The bit fields in these registers define compare value (boundary) for the limit checking unit. The reset values of the boundaries are defined as 10%, 90%, 33% and 66% of the complete result range (the MSB located at bit position 11) of each conversion.

LCBR0
Limit Check Boundary Register 0 **($0F0_H$)** **Reset Value: $0000\ 0198_H$**
LCBR1
Limit Check Boundary Register 1 **($0F4_H$)** **Reset Value: $0000\ 0E64_H$**
LCBR2
Limit Check Boundary Register 2 **($0F8_H$)** **Reset Value: $0000\ 0554_H$**
LCBR3
Limit Check Boundary Register 3 **($0FC_H$)** **Reset Value: $0000\ 0AA8_H$**



Field	Bits	Type	Description
BOUNDARY	[11:2]	rw	**Boundary for Limit Checking** This bit field contains the value for the limit checking unit that is compared to the actual conversion result. The result of the limit check is used for the generation of the channel event, see **Section 31.2.13.4**.
0	[1:0], [31:12]	r	**Reserved** Read as 0; should be written with 0.

31.2.14.5 Channel Flag Register

The channel event indication flag register CHFR monitors the detected channel events.

CHFR
Channel Flag Register **(060_H)** **Reset Value: $0000\ 0000_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FC15	FC14	FC13	FC12	FC11	FC10	FC9	FC8	FC7	FC6	FC5	FC4	FC3	FC2	FC1	FC0
rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh

Field	Bits	Type	Description
FCx **(x = 0 - 15)**	x	rwh	**Event Flag for Channel x** Flag FCx indicates that a channel event for channel x has been detected. Writing a 0 has no effect, whereas writing a 1 sets the written bit position without generating an interrupt. Bit FCx is cleared by writing CHFCR.CFCx = 1. 0_B A channel x event has not occurred. 1_B A channel x event has occurred.
0	[31:16]	r	**Reserved** Read as 0; should be written with 0.

31.2.14.6 Channel Flag Clear Register

Writing a 1 to a bit position in register CHFCR clears the corresponding channel flag in register CHFR. If a hardware event triggers the setting of bit CHFR.x and software writes CHFCR.x = 1, bit CHFR.x is cleared (software overrules hardware).

CHFCR
Channel Flag Clear Register **(064_H)** **Reset Value: $0000\ 0000_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CF C15	CF C14	CF C13	CF C12	CF C11	CF C10	CF C9	CF C8	CF C7	CF C6	CF C5	CF C4	CF C3	CF C2	CF C1	CF C0
w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w

Field	Bits	Type	Description
CFCx (x = 0 - 15)	x	w	**Clear Event Flag for Channel x** 0_B No action. 1_B Bit CHFR.FCx is cleared.
0	[31:16]	r	**Reserved** Read as 0; should be written with 0.

31.2.14.7 Channel Event Node Pointer Registers

The bit fields in these registers define the service request output ADCy_SR[7:0] that is activated if a channel event occurs and the interrupt generation is enabled for this channel.

CHENPR0
Channel Event Node Pointer Register 0

(068_H) **Reset Value: $0000\ 0000_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	CHENP7			0	CHENP6			0	CHENP5			0	CHENP4		
r	rw			r	rw			r	rw			r	rw		

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	CHENP3			0	CHENP2			0	CHENP1			0	CHENP0		
r	rw			r	rw			r	rw			r	rw		

Field	Bits	Type	Description
CHENP0, CHENP1, CHENP2, CHENP3, CHENP4, CHENP5, CHENP6, CHENP7	[2:0], [6:4], [10:8], [14:12], [18:16], [22:20], [26:24], [30:28]	rw	**Node Pointer for Channel x** This bit field defines which service request output becomes activated if the channel x event of kernel ADCy occurs while enabled by **CHCTRx (x = 0 - 15)**.LCC. 000_B ADCy_SR0 is selected. 001_B ADCy_SR1 is selected. ... 111_B ADCy_SR7 is selected.
0	3, 7, 11, 15, 19, 23, 27, 31	r	**Reserved** Read as 0; should be written with 0.

CHENPR8
Channel Event Node Pointer Register 8

($06C_H$) **Reset Value: $0000\ 0000_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	CHENP15			0	CHENP14			0	CHENP13			0	CHENP12		
r	rw			r	rw			r	rw			r	rw		

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	CHENP11			0	CHENP10			0	CHENP9			0	CHENP8		
r	rw			r	rw			r	rw			r	rw		

Field	Bits	Type	Description
CHENP8, **CHENP9,** **CHENP10,** **CHENP11,** **CHENP12,** **CHENP13,** **CHENP14,** **CHENP15**	[2:0], [6:4], [10:8], [14:12], [18:16], [22:20], [26:24], [30:28]	rw	**Node Pointer for Channel x** This bit field defines which service request output becomes activated if the channel x event of kernel ADCy occurs while enabled by **CHCTRx (x = 0 - 15)**.LCC. 000_B ADCy_SR0 is selected. 001_B ADCy_SR1 is selected. ... 111_B ADCy_SR7 is selected.
0	3, 7, 11, 15, 19, 23, 27, 31	r	**Reserved** Read as 0; should be written with 0.

31.2.15 Conversion Result Handling

The result generation part handles the:

- Storage of the conversion results (see **Section 31.2.15.1**)
- Wait-for-read mode (see **Section 31.2.15.2**)
- Result event interrupts (see **Section 31.2.15.3**)
- Result FIFO buffer (see **Section 31.2.15.4**)
- Data reduction or anti-aliasing filtering (see **Section 31.2.15.5**)

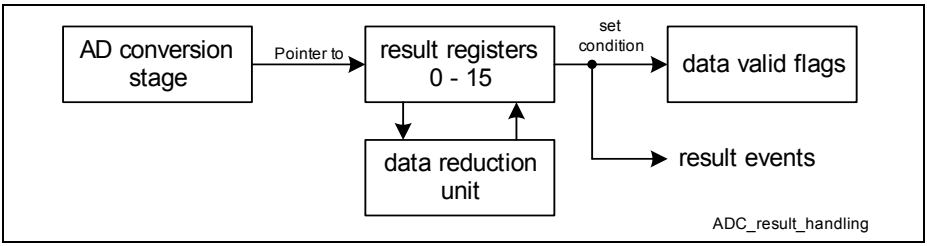


Figure 31-17 Conversion Result Handling

31.2.15.1 Storage of Conversion Results

For each analog input channel, the associated channel control register **CHCTRx (x = 0 - 15)** contains a pointer bit field (RESRSEL) defining the result register to store the conversion result of this channel. This structure allows the user to direct conversion results of different channels to one or more result registers. Depending on the application needs (data reduction, auto-scan, alias feature, result FIFO, etc.), the user can distribute the conversion results to minimize CPU load or to be more tolerant against interrupt latency.

An individual data valid flag **VFR**.VFx for each result register indicates that “new” valid data has been stored in the corresponding result register and can be read out.

Due to different result handling mechanisms, the conversion result can be represented in different ways:

- **Data reduction filter disabled:**
  The conversion result is maximum 12 bits wide with the MSB of the conversion result being always at bit position 11 and the remaining LSBs filled with 0.
  The data valid flag is set and a result event occurs each time a new conversion result is stored in the result register.
  It is possible to share a result register among several analog input channels.
- **Data reduction filter enabled:**
  The conversion result is maximum 12 bits wide with the MSB of the conversion result being always at bit position 11 and the remaining LSBs filled with 0. The additional bits [13:12] show the MSBs of the data accumulation.

The data valid flag is set and a result event occurs each time a data reduction sequence is finished and the final result is available in the result register.

In order to support a wait-for-read and FIFO buffer features, the valid flag has to be cleared automatically when SW does a read access or the result is transferred into another FIFO element (if result FIFO buffering is enabled).
This behavior is contradictory to debugging requirements. For debugging, it has to be possible to introduce read or write commands into the normal program flow, e.g. to monitor conversion results. If a debugger reads out a result register, it would change the status of the conversion result from valid = “new” (not yet read out) to “old” (already read out). This would have an undesired impact on the application.
Therefore, the read views with “D” deliver the same value as the read views without “D”, but without clearing the valid bit. As a result, a debugger using read views with “D” can monitor the conversion results without influencing their status for the application.

To allow debugger accesses without the risk of data sequence corruption, two different result register read views are supported. The read views refer to the same result register contents, but show a different behavior according to the address that has been read:

- Standard read view **RESR0** and **RESRx (x = 1 - 15)**:
  A read action clears the corresponding valid bit.
- Read view **RESRD0** and **RESRDx (x = 1 - 15)** for debugger:
  A read action does not clear the corresponding valid bit.

31.2.15.2 Wait-for-Read Mode

The wait-for-read mode is a feature of a result register allowing the CPU (or DMA) to treat each conversion result independently without the risk of data loss. Data loss could occur if the CPU does not read a conversion result from a result register before a new result overwrites the previous one.
Especially for auto-scan conversion sequences (or other sequences with “relaxed” timing requirements), the wait-for-read offers the possibility to request a conversion sequence according to an event (HW or SW), but to start a new conversion according to the CPU capability to read the formerly converted result.

If wait-for-read mode is enabled for a result register by setting bit WFR in register **RCRx (x = 0 - 15)**, a request source does not generate a conversion request while the targeted result register contains valid data (indicated by the valid flag VFx = 1) or if a currently running conversion targets the same result register.
A new conversion request is generated only after the targeted result register has been read out.
If two request sources target the same result register with wait-for-read selected, a lower priority request started before the higher priority source has requested its conversion can not be interrupted by the higher priority request. If a higher priority request targets a different result register, the lower priority conversion can be cancelled and repeated afterwards.

31.2.15.3 Result Event Interrupts

A result event interrupt can be generated based on a result event according to the structure shown in **Figure 31-18**. If a result event is detected, it sets the corresponding indication flag in register **EVFR**. These flags can also be set by writing a 1 to the corresponding bit position, whereas writing 0 has no effect. The indication flags can be cleared by SW by writing a 1 to the corresponding bit position in register **EVFCR**.

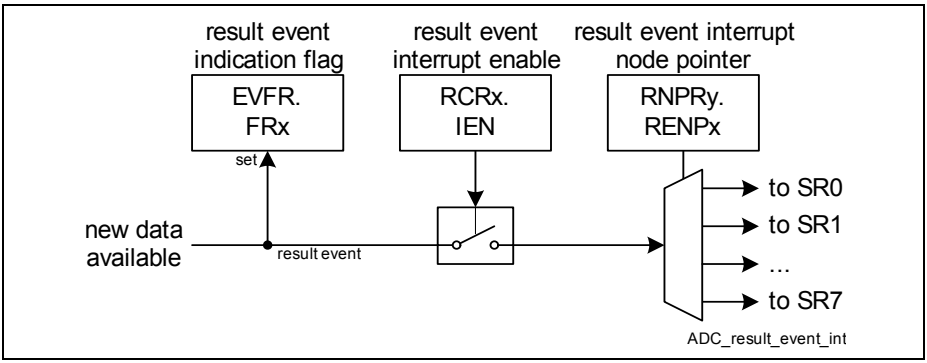


Figure 31-18 Result Event Interrupt Generation

The service request output ADCy_SRx that is selected by the result event interrupt node pointer bit fields in registers **RNPR0** or **RNPR8** issues an interrupt each time the related result event is detected.
A service request output can be activated under SW control by writing **INTR**.SISRx.

31.2.15.4 Result FIFO Buffer

If a result register is not used as direct target for a conversion result, it can be concatenated with other result registers of the same ADC kernel to form a result FIFO buffer (first-in-first-out buffer mechanism). This allows to store measurement results and to read them out later with a “relaxed” CPU access timing. It is possible to set up more than one FIFO buffer structure with the available result registers.
A FIFO structure can be built by at least two “neighbor” result registers with the indices x and z = x+1, where result register z represents the input and result register x represents the output of the FIFO buffer. The conversion result has to be delivered by the converter stage to the FIFO input, whereas the buffered data has to be read out from the FIFO output.
The FIFO buffer function can be enabled by setting bit FEN in registers **RCRx (x = 0 - 15)**.

In the example shown in **Figure 31-19**, the result registers have been configured to form two FIFO buffers with two buffer stages (result registers 0/1 and 6/7, respectively), one FIFO buffer with three buffer stages (result registers 2/3/4), whereas result register 5 is used as “normal” result register without additional FIFO buffer functionality.

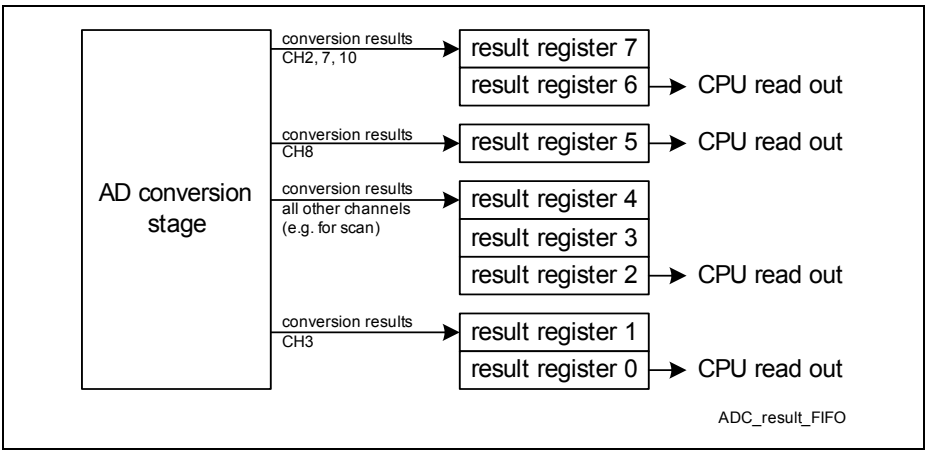


Figure 31-19 Result FIFO Buffers

If more than two result neighbor registers are concatenated to a FIFO buffer (from result register z to result register x, with z > x), the one with the highest index (z) is always the input and the one with the lowest index (x) is always the output. All intermediate result registers y (x < y < z) are used as intermediate FIFO stages without data input or data output functionality.

Result register features for each FIFO buffer:

- Result register z (**FIFO buffer input**):
  This result register can be enabled for data reduction. The wait-for-read mode is supported to avoid data loss if the FIFO is full. Result event interrupt generation is not supported. Must not be read at a read view modifying the valid bit.
- Result register y (**intermediate buffer stage**):
  This/these result register(s) must not be enabled neither for wait-for-read mode, nor for data reduction. Result event interrupt generation is not supported. Must not be read at a read view modifying the valid bit, nor be the target of a conversion result.
- Result register x (**FIFO buffer output**):
  This result register can be enabled for result event interrupt generation to inform the CPU that new data can be read out from this register location. Data reduction and wait-for-read are not supported and have to be disabled. Must not be the target of a conversion result.
  If enabled, a result interrupt is generated for each data word in the FIFO.

31.2.15.5 Data Reduction Filter

The data reduction filter can be used as digital filter for anti-aliasing or decimation purposes. It can accumulate a maximum of 4 conversion results to generate a final result.

Each result register can be individually enabled for data reduction. The feature is controlled by bit field DRCTR in registers **RCRx (x = 0 - 15)**. The actual status is given by bit field DRC (data reduction counter) in the related result register.
Conversion delivering results to other result registers do not influence the data reduction filter of result register x. As a consequence, other channels can be converted between two conversions targeting result register x.

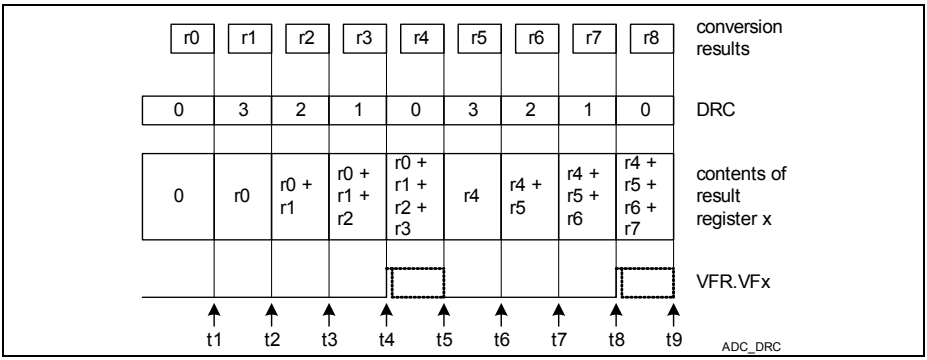


Figure 31-20 Data Reduction Filter

In the example given in **Figure 31-20**, a data reduction sequence of 4 accumulated conversion results is shown. The data reduction is based on three rules:

- Each time bit field DRC is 0 and a conversion targeting result register x is completed (t1, t5, t9), the contents of bit field RCRx.DRCTR is loaded into bit field DRC and the conversion result is stored in result register x.
- Each time bit field DRC is not 0 and a conversion targeting result register x is completed (t2, t3, t4 for the first final result and t6, t7, t8 for the next one), bit field DRC is decremented by 1 and the conversion result is added to the value already stored in result register x.
- Each time bit field DRC is 0 after decrementing or after loading it with RCRx.DRCTR = 0 (t4 for the first final result and t8 for the next one), the valid bit for the result register x becomes set and a result register event occurs.

The final result of a data reduction sequence has to be read out from result register x before the next data reduction sequence starts (interval between t4 and t5, or t8 and t9 respectively). With the read out of the final result from this register, the valid flag is automatically cleared.
If this interval is too short, it is recommended to associate a second result register z to

result register x by enabling the result FIFO mechanism for result register x, see **Figure 31-21** (z = x + 1). In this case, result register x is loaded with the final result elaborated by result register z when a data reduction sequence is finished. The final result has to be read out from result register x before the next data reduction sequence is finished (interval between t4 and t8).

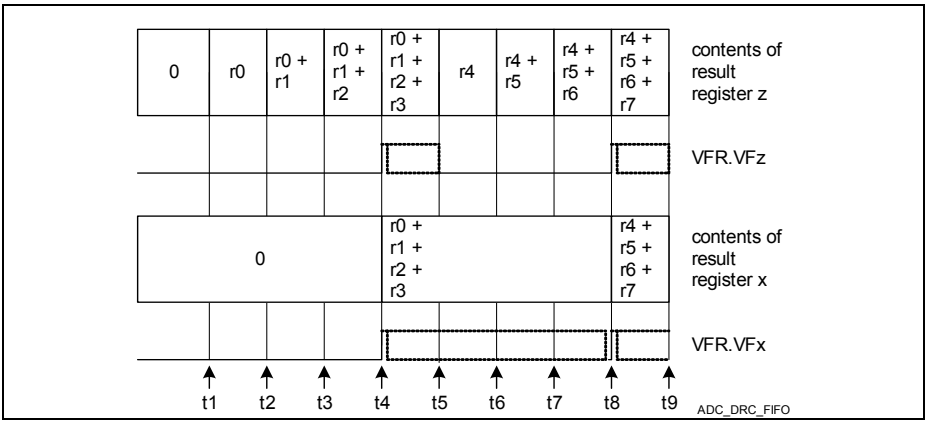


Figure 31-21 Data Reduction Filter with Result FIFO

31.2.15.6 Result Data Filter

A certain number of the result registers can be individually enabled for data filtering. As the result registers can be individually assigned to the channels, these filters can be selected for all channels within the same ADC kernel. Conversions delivering results to other result registers do not influence the value of this data filter activated at result register x. As a consequence, other channels can be converted between two conversions targeting result register x.

There are two different filter types implemented:

- A third order FIR filter with adjustable coefficients
- A first order IIR filter with adjustable coefficients

The result buffer are cleared as long as no result data filter is selected by parameter DRCTR in register **RCRx (x = 0 - 15)**. Only the output of this data filter can be used together with the result FIFO buffer function, described in **Section 31.2.15.4**.

FIR (finite impulse response) Filter

Each FIR filter contains three filter tab coefficients a, b and c and two result buffer (RB1 and RB2) for storing the intermediate values. **Figure 31-22** shows the structure of the filter.

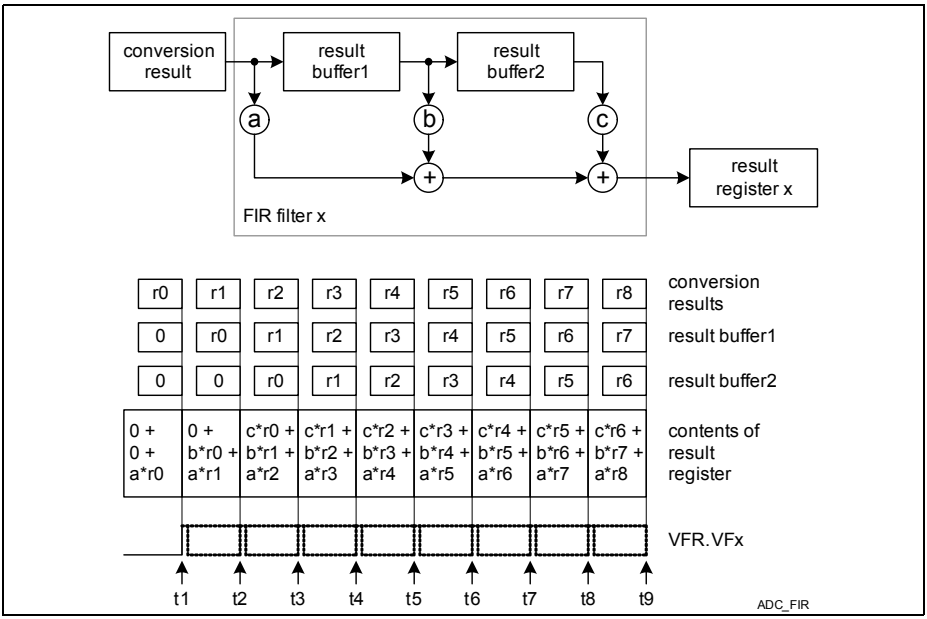


Figure 31-22 FIR Filter

The values from the result buffer and the conversion result are added to the result register according to their coefficients. There are predefined coefficients selectable in register **RCRx (x = 0 - 15)**, which cause a gain of 3 or 4 to the ADC result leading to a 14 bit value. The valid flag (**VFR**.VFx) indicates a valid result, at the first sample after activation and the result is valid for each sample.

IIR (infinite impulse response) Filter

The IIR filter contains two filter tab coefficients a and b. **Figure 31-23** shows the structure of the filter.

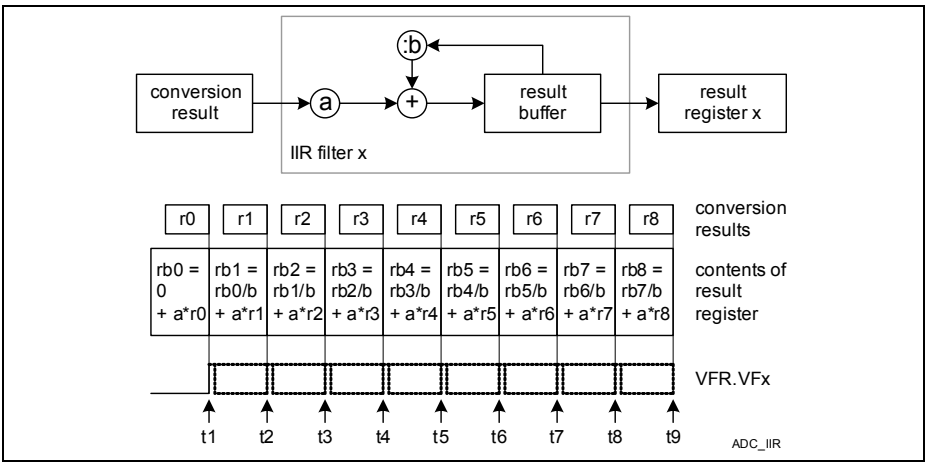


Figure 31-23 IIR Filter

This IIR filter represents a first order low pass filter. The conversion result is added a-times to the fractional (:b) amount of the previous value of the result buffer which is copied to the associated result register.

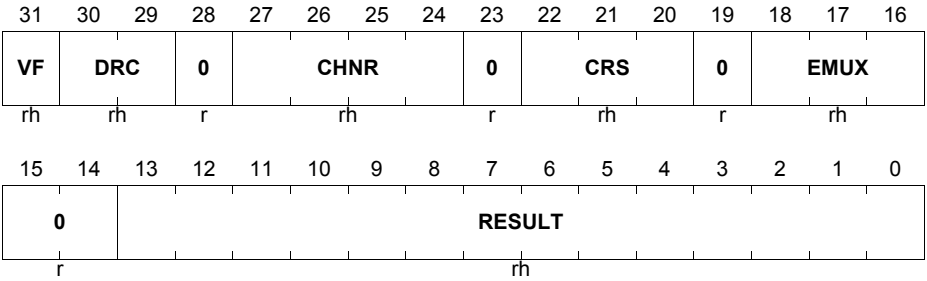
There are predefined coefficients selectable in register **RCRx (x = 0 - 15)**, which cause a gain of 4 to the ADC result leading to a 14 bit value. The valid flag (**VFR**.VFx) indicates a valid result, at the first sample after activation and the result is valid for each sample.

31.2.16 Conversion Result-Related Registers

31.2.16.1 Result Register 0

The result registers deliver the conversion results and associated information.
Additionally to this information, result register RESR0 also indicates the setting of an external analog multiplexer. The conversion results of the channel used with an external multiplexer have to be directed to RESR0 in order to indicate the multiplexer setting used during the conversion. If this information is not necessary, the conversion result can be directed to any other result register.
The valid flag VF indicates that a result register contains updated data and can be used to poll for new data. The valid flag of a result register is cleared automatically if at least the low byte of register RESR0 is read, whereas it is left unchanged when reading RESRD0.

RESR0
Result Register 0 **(180_H)** **Reset Value: 0000 0000_H**
RESRD0
Result Register 0 for Debugging **($1C0_H$)** **Reset Value: 0000 0000_H**



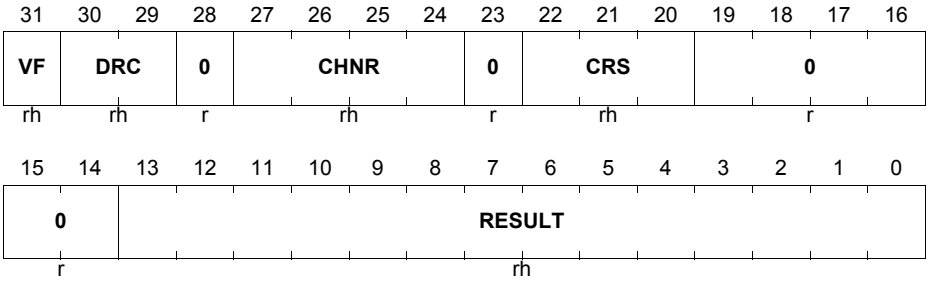
Field	Bits	Type	Description
RESULT	[13:0]	rh	**Conversion Result** This bit field contains the conversion result, or respectively, the result of the data reduction filter.
EMUX	[18:16]	rh	**External Multiplexer Setting** This bit field indicates the external multiplexer setting leading to the result stored in bit field RESULT.

Field	Bits	Type	Description
CRS	[22:20]	rh	**Converted Request Source** This bit field indicates the request source that has requested the conversion leading to the result stored in bit field RESULT. 000_B The conversion was requested by source 0. 001_B The conversion was requested by source 1. 010_B The conversion was requested by source 2. 011_B The conversion was requested by source 3. 100_B The conversion was requested by source 4. else reserved
CHNR	[27:24]	rh	**Channel Number** This bit field contains the channel number of the latest register update.
DRC	[30:29]	rh	**Data Reduction Counter** This bit field indicates how many conversion results have still to be accumulated to generate the final result for data reduction. The valid flag is automatically set when this bit field becomes 0. It can be cleared by SW by writing a 1 to the related bit position in register VFR. 00_B The final result is available in the result register. The valid flag is automatically set when this bit field is set to 0. 01_B 1 more conversion result has to be added to obtain the final result in the result register. 10_B 2 more conversion results have to be added to obtain the final result in the result register. 11_B 3 more conversion results have to be added to obtain the final result in the result register.
VF	31	rh	**Valid Flag** This bit indicates that bit field RESULT has been updated with valid data since it has been read out. It is another view of the corresponding bit in register VFR. 0_B The result register has not been updated. 1_B The result register has been updated.
0	[15:14], 19, 23, 28	r	**Reserved** Read as 0; should be written with 0.

31.2.16.2 Result Registers 1 to 15

The result registers deliver the conversion results and associated information.
The valid flag VF indicates that the result register contain updated data and can be used to poll for new data. The valid flag of a result register is cleared automatically if at least the low byte of register RESRx is read, whereas it is left unchanged when reading RESRDx.

RESRx (x = 1 - 15)
Result Register x **(180_H + x * 4)** **Reset Value: 0000 0000_H**
RESRDx (x = 1 - 15)
Result Register x for Debugging **($1C0_H$ + x * 4)** **Reset Value: 0000 0000_H**



Field	Bits	Type	Description
RESULT	[13:0]	rh	**Conversion Result** This bit field contains the conversion result, or respectively, the result of the data reduction filter.
CRS	[22:20]	rh	**Converted Request Source** This bit field indicates the request source that has requested the conversion leading to the result stored in bit field RESULT. 000_B The conversion was requested by source 0. 001_B The conversion was requested by source 1. 010_B The conversion was requested by source 2. 011_B The conversion was requested by source 3. 100_B The conversion was requested by source 4. else reserved
CHNR	[27:24]	rh	**Channel Number** This bit field contains the channel number of the latest register update.

Field	Bits	Type	Description
DRC	[30:29]	rh	**Data Reduction Counter** This bit field indicates how many conversion results have still to be accumulated to generate the final result for data reduction. The valid flag is automatically set and a result event is generated when this bit field becomes 0 (by decrementing or by reload). Bit field DRC is cleared by writing the related **VFR**.VFx = 1. 00_B The final result is available in the result register. 01_B 1 more conversion result has to be added to obtain the final result in the result register. 10_B 2 more conversion results have to be added to obtain the final result in the result register. 11_B 3 more conversion results have to be added to obtain the final result in the result register.
VF	31	rh	**Valid Flag** This bit indicates that bit field RESULT has been updated with valid data since it has been read out. It is another view of the corresponding bit in register VFR. 0_B The result register has not been updated. 1_B The result register has been updated.
0	[19:14], 23, 28	r	**Reserved** Read as 0; should be written with 0.

31.2.16.3 Valid Flag Register

The valid flag register contains the flags indicating that the corresponding result register contents are valid (valid = “new” = not read out).
These bits are another (condensed) view of the valid flags in the result registers.

VFR
Valid Flag Register **(200_H)** **Reset Value: $0000\ 0000_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

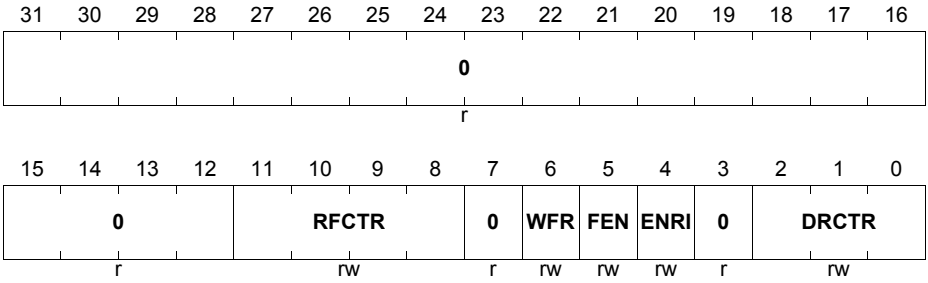
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VF 15	VF 14	VF 13	VF 12	VF 11	VF 10	VF 9	VF 8	VF 7	VF 6	VF 5	VF 4	VF 3	VF 2	VF 1	VF 0
rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh

Field	Bits	Type	Description
VFx **(x = 0 - 15)**	x	rwh	**Valid Flag for Result Register x** This bit indicates that the contents of the result register x is valid. Writing a 0 has no effect, whereas writing a 1 clears the written bit position and the bit field DRC in the related result register. If a hardware event triggers the setting of a bit VFx and SW writes a 1 to the same bit position, the bit VFx is cleared (software overrules hardware). 0_B The result register x does not contain valid data. Either this register has been read out or no data has been moved to it. 1_B The result register x contains valid data that has not yet been read out.
0	[31:16]	r	**Reserved** Read as 0; should be written with 0.

31.2.16.4 Result Control Registers

The result control registers contain bits to control the behavior of the result registers and to monitor their status. Result register x is controlled by result control register x.

RCRx (x = 0 - 15)
Result Control Register x **(140_H + x * 4)** **Reset Value: 0000 0000_H**



Field	Bits	Type	Description
DRCTR	[2:0]	rw	**Data Reduction and Filter Control** This bit field defines the processing of the result register (see **Section 31.2.15.5** and **Section 31.2.15.6**). It defines the reload value for bit field DRC. 000_B The data reduction filter is disabled. The reload value for DRC is 0, so no accumulation is done. 001_B The data reduction filter is enabled. The reload value for DRC is 1, so the accumulation is done over 2 conversions. 010_B The data reduction filter is enabled. The reload value for DRC is 2, so the accumulation is done over 3 conversions. 011_B The data reduction filter is enabled. The reload value for DRC is 3, so the accumulation is done over 4 conversions. 100_B The result data filter x is enabled. The filter coefficients are selected by RFCTR [11:8] in the same register.[1)] 101_B reserved, do not use 110_B reserved, do not use 111_B reserved, do not use

Field	Bits	Type	Description
ENRI	4	rw	**Enable Result Interrupt** This bit enables the result event interrupt if a result event is detected for result register x. 0_B The result event interrupt is disabled. 1_B The result event interrupt is enabled.
FEN	5	rw	**FIFO Enable** This bit enables the FIFO functionality for result register x, see **Section 31.2.15.4**. 0_B The FIFO functionality is disabled. 1_B The FIFO functionality is enabled.
WFR	6	rw	**Wait-for-Read Mode** This bit enables the wait-for-read mode for result register x. 0_B The wait-for-read mode is disabled. 1_B The wait-for-read mode is enabled.
RFCTR	[11:8]	rw	**Result Filter Control** [1)] This bit field defines the filter coefficients of the data filter. 0000_BFIR: a=2, b=1 c=0 0001_BFIR: a=1, b=2 c=0 0010_BFIR: a=2, b=0 c=1 0011_BFIR: a=1, b=1 c=1 0100_BFIR: a=1, b=0 c=2 0101_BFIR: a=3, b=1 c=0 0110_BFIR: a=2, b=2 c=0 0111_BFIR: a=1, b=3 c=0 1000_BFIR: a=3, b=0 c=1 1001_BFIR: a=2, b=1 c=1 1010_BFIR: a=1, b=2 c=1 1011_BFIR: a=2, b=0 c=2 1100_BFIR: a=1, b=1 c=2 1101_BFIR: a=1, b=0 c=3 1110_BIIR: a=2, b=2 1111_BIIR: a=3, b=4
0	3, 7, [31:12]	r	**Reserved** Read as 0; should be written with 0.

1) Availability of field RFCTR and selection DRCTR = 100b depends on implementation. Please refer to **Section 31.3.3**.

31.2.16.5 Event Flag Register

The event flag register contains flags related to request source events and result register events.

EVFR

Event Flag Register **(070_H)** **Reset Value: $0000\ 0000_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0			GFS4	GFS3	GFS2	GFS1	GFS0	0			FS4	FS3	FS2	FS1	FS0
r			rh	rh	rh	rh	rh	r			rwh	rwh	rwh	rwh	rwh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FR15	FR14	FR13	FR12	FR11	FR10	FR9	FR8	FR7	FR6	FR5	FR4	FR3	FR2	FR1	FR0
rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh	rwh

Field	Bits	Type	Description
FRx (x = 0 - 15)	x	rwh	**Event Flag for Result Register x** Flag FRx indicates that a result event of result register x has been detected. Writing a 0 has no effect, whereas writing a 1 sets the written bit position without generating an interrupt. Bit FRx is cleared by writing EVFCR.CFRx = 1. 0_B An event of result register x has not yet been detected. 1_B An event of result register x has been detected.
FSx (x = 0 - 4)	x + 16	rwh	**Event Flag for Request Source x** Flag FSx indicates that a request source event of request source x has been detected. Writing a 0 has no effect, whereas writing a 1 sets the written bit position without generating an interrupt. Bit FSx is cleared by writing EVFCR.CFSx = 1. 0_B An event of request source x has not yet been detected. 1_B An event of request source x has been detected.

Field	Bits	Type	Description
GFSx (x = 0 - 4)	x + 24	rh	**Gated Event Flag for Request Source x** Flag GFSx indicates that a request source event of request source x has been detected while the related interrupt was enabled. Writing to this bit position has no effect. Bit GFSx is cleared by writing EVFCR.CFSx = 1. 0_B An event of request source x has not yet been detected or the related interrupt was not enabled. 1_B An event of request source x has been detected while the related event interrupt was enabled.
0	[23:21], [31:29]	r	**Reserved** Read as 0; should be written with 0.

31.2.16.6 Event Flag Clear Register

Writing a 1 to a bit position in register EVFCR clears the corresponding event flag in register EVFR. If a hardware event triggers the setting of bit EVFR.x and software writes EVFCR.x = 1, bit EVFR.x is cleared (software overrules hardware).

EVFCR
Event Flag Clear Register **(074_H)** **Reset Value: 0000 0000_H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0											CFS4	CFS3	CFS2	CFS1	CFS0
r											w	w	w	w	w

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CFR15	CFR14	CFR13	CFR12	CFR11	CFR10	CFR9	CFR8	CFR7	CFR6	CFR5	CFR4	CFR3	CFR2	CFR1	CFR0
w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w

Field	Bits	Type	Description
CFRx (x = 0 - 15)	x	w	**Clear Event Flag for Result Register x** 0_B No action. 1_B Bit EVFR.FRx is cleared.
CFSx (x = 0 - 4)	x + 16	w	**Clear Event Flag for Source x** 0_B No action. 1_B Bits EVFR.FSx and EVFR.GFSx are cleared.
0	[31:21]	r	**Reserved** Read as 0; should be written with 0.

31.2.16.7 Event Node Pointer Registers

The bit fields in these registers define the service request output ADCy_SR[7:0] that is activated if a request source event or a result register event occurs and the interrupt generation is enabled for this event.

EVNPR
Event Node Pointer Register **(078_H)** **Reset Value: 0000 0000_H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0													SENP4		
r													rw		

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	SENP3			0	SENP2			0	SENP1			0	SENP0		
r	rw			r	rw			r	rw			r	rw		

Field	Bits	Type	Description
SENP0, SENP1, SENP2, SENP3, SENP4	[2:0], [6:4], [10:8], [14:12], [18:16]	rw	**Node Pointer for Request Source x** This bit field defines which service request output becomes activated if the request source x event of kernel ADCy occurs while the interrupt generation is enabled for this event. 000_B ADCy_SR0 is selected. 001_B ADCy_SR1 is selected. ... 111_B ADCy_SR7 is selected.
0	3, 7, 11, 15, [31:19]	r	**Reserved** Read as 0; should be written with 0.

RNPR0

Result Node Pointer Register 0 (208_H) Reset Value: 0000 0000$_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	**RENP7**			**0**	**RENP6**			**0**	**RENP5**			**0**	**RENP4**		
r	rw			r	rw			r	rw			r	rw		

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	**RENP3**			**0**	**RENP2**			**0**	**RENP1**			**0**	**RENP0**		
r	rw			r	rw			r	rw			r	rw		

Field	Bits	Type	Description
RENP0, **RENP1,** **RENP2,** **RENP3,** **RENP4,** **RENP5,** **RENP6,** **RENP7**	[2:0], [6:4], [10:8], [14:12], [18:16], [22:20], [26:24], [30:28]	rw	**Node Pointer for Result Register x** This bit field defines which service request output becomes activated if the result register x event of kernel ADCy occurs while the interrupt generation is enabled for this event. 000_B ADCy_SR0 is selected. 001_B ADCy_SR1 is selected. ... 111_B ADCy_SR7 is selected.
0	3, 7, 11, 15, 19, 23, 27, 31	r	**Reserved** Read as 0; should be written with 0.

RNPR8

Result Node Pointer Register 8 ($20C_H$) Reset Value: $0000\ 0000_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0	**RENP15**			**0**	**RENP14**			**0**	**RENP13**			**0**	**RENP12**		
r	rw			r	rw			r	rw			r	rw		

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	**RENP11**			**0**	**RENP10**			**0**	**RENP9**			**0**	**RENP8**		
r	rw			r	rw			r	rw			r	rw		

Field	Bits	Type	Description
RENP8, **RENP9,** **RENP10,** **RENP11,** **RENP12,** **RENP13,** **RENP14,** **RENP15**	[2:0], [6:4], [10:8], [14:12], [18:16], [22:20], [26:24], [30:28]	rw	**Node Pointer for Result Register x** This bit field defines which service request output becomes activated if the result register x event of kernel ADCy occurs while the interrupt generation is enabled for this event. 000_B ADCy_SR0 is selected. 001_B ADCy_SR1 is selected. ... 111_B ADCy_SR7 is selected.
0	3, 7, 11, 15, 19, 23, 27, 31	r	**Reserved** Read as 0; should be written with 0.

31.2.17 Multiplexer Test Support

A specific multiplexer test mode has been implemented for the analog input CH7 that can be enabled during run time by the user to check the connection to the sensor.

- **Multiplexer test mode disabled** (**GLOBCFG**.MTM7 = 0):
  The switch for the voltage divider and static load R_{MTM7} is open. The analog input CH7 can be used for normal measurements.
- **Multiplexer test mode enabled** (**GLOBCFG**.MTM7 = 1):
  The switch for the voltage divider and static load R_{MTM7} is closed. The analog input CH7 is loaded by a resulting resistance and the measured voltage is reduced by a voltage divider.
  Please refer to the AC/DC chapter for the value of the resulting grounding resistor and its current capability.

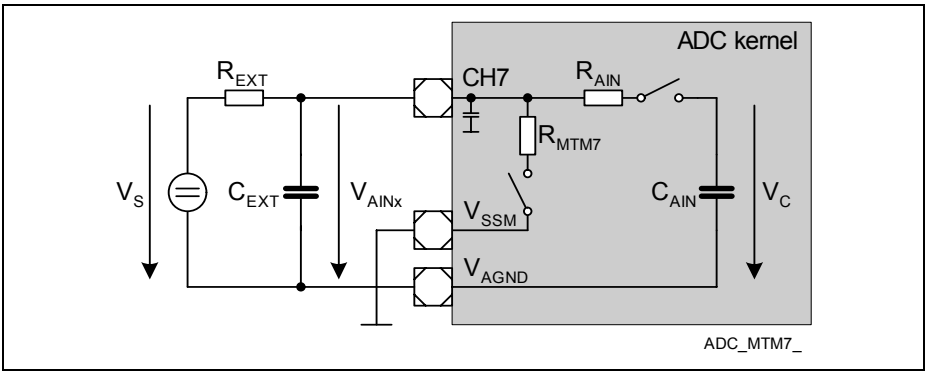


Figure 31-24 Multiplexer Test Mode for CH7

In addition to the multiplexer test support for channel CH7 based on bit MTM7, one of the input channels listed below can also be enabled for the same function. The additional channel number is selected by bit field GLOBCFG.MTMCH and the test mode becomes enabled for this channel if GLOBCFG.MTMEN = 1.

The following channels can be selected for the additional multiplexer test mode support: CH1, CH3, CH5, CH7, CH9, CH11, CH13, CH15

The channels with an even channel number do not support this test mode, even if their channel number is selected and MTMEN = 1.
The multiplexer test mode for input channel CH7 can be activated by both mechanisms.

31.2.18 External Multiplexer Control

If an application requires more analog inputs channels than available on the TC1798, the ADC kernel supports an extension of analog channels by adding an external analog multiplexer. Three output signals EMUX[2:0] are delivered by the ADC kernel to control the settings of an external analog multiplexer. They can be used to extend the number of analog input channels by adding an external 1-out-of-8 multiplexer.
The external multiplexer control behavior is defined by the bits in register **EMCTR**.
The current setting of EMUX[2:0] is given by bit field EMUX. If another extended input channel should be converted, bit field SETEMUX has to be programmed to the desired value or the scan function has to be enabled. The SETEMUX value is automatically applied with the start of the next conversion of the related analog ADC input channel.

In the example shown in **Figure 31-25** and in the description below, the analog input CH7 has been extended, leading to additional analog inputs named CH70 to CH77. The channel number where the external multiplexer is connected to is defined by bit field EMUXCHNR.

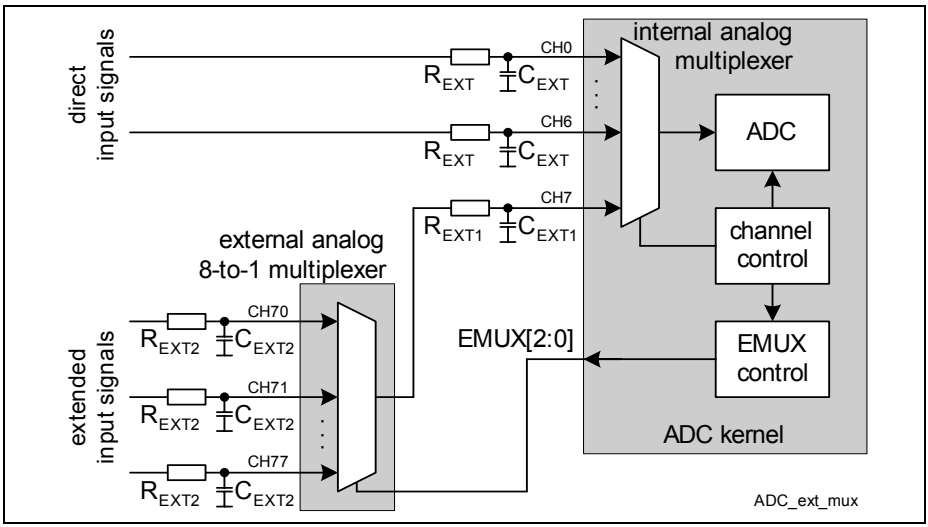


Figure 31-25 External Analog Multiplexer

If the external multiplexer is located far from the ADC analog input, it is recommended to introduce an RC filter R_{EXT1}-C_{EXT1} directly at the analog input CH7 of the ADC. If needed for signal filtering, local RC filters R_{EXT2}-C_{EXT2} can be optionally added at the inputs of the external analog multiplexer.
If the external multiplexer is located close to the analog ADC input, the components R_{EXT1} and C_{EXT1} are not necessarily needed. In this case it is strongly recommended to

introduce RC filters (R_{EXT2}, C_{EXT2}) at the multiplexer inputs.
Please note that each RC filter limits the bandwidth of the analog input signal.

The RC filters used with an external multiplexer may lead to another impedance “seen” by the ADC analog input CH7 than for the other (direct) analog inputs. The adaptation of the sample phase length can be done by using a different input class with a different value for the sample phase extension. This value can be adapted to execute conversions with an EMUX[2:0] setting that has changed a sufficiently long time before the conversion of CH7 starts. “A sufficiently long time before” signifies that signal transitions at the analog ADC input due to changing multiplexer setting are finished and the input signal is stable enough.
After changing the EMUX[2:0] setting of the external multiplexer, an additional settling time has to elapse before the switched analog signal is stable and can be measured. To compensate for this settling time, an alternative sample phase length (instead of the one given by the input class) is automatically applied for the first conversion of CH7 after EMUX[2:0] has changed. The alternative sample phase length can be programmed by bit field **EMCTR**.EMSAMPLE. If the first conversion of CH7 after the EMUX[2:0] setting has changed is aborted due to a higher priority request, the repeated conversion of CH7 also uses the value of EMSAMPLE. The settling time is considered to be finished after the complete conversion of CH7.

The external multiplexer control block supports different modes, that are programmed by the bits in register **EMCTR**:

- **SW control** without any HW interaction (EMUXEN = 0):
  The automatic control of the external multiplexer setting and of the sampling time is disabled. Bit field EMUX is permanently updated with the value of SETEMUX. The changes of EMUX are related to write actions to SETEMUX and not to conversion timing. The setting of EMSAMPLE is not taken into account. It is recommended to write the start value of the first scan sequence to SETEMUX while EMUXEN = 0.
- **HW control without scan** (EMUXEN = 1, SCANEN = 0):
  The update of EMUX with the value of SETEMUX happens with each conversion start of the channel selected by EMUXCHNR. For the first conversion with a new EMUX value, the setting of EMSAMPLE is applied.
- **HW control with single-input scan** (EMUXEN = 1, SCANEN = 1, TROEN = 0):
  The update of EMUX with a new value happens after each conversion of the channel selected by EMUXCHNR. For each update, EMUX is automatically decremented by 1. If EMUX = 0, it is reloaded with the value of SETEMUX for the next update. For each conversion of the selected channel, the setting of EMSAMPLE is applied.
  With this setting, an autoscan sequence requesting the conversion of the channel defined by EMUXCHNR leads to one conversion of the channel connected to the external multiplexer. As a result, for each completed auto scan sequence, another EMUX setting is applied.
  Assuming inputs 1, 2, 70, 71, and 72 being selected for scan, the following sequence will be executed: 1, 2, 72, 1, 2, 71, 1, 2, 70, 1, 2, 72, 1, 2, 71, 1, 2, 70, 1, 2, 72, ...

- **HW control with multi-input scan** (EMUXEN = 1, SCANEN = 1, TROEN = 1):
  The update of EMUX with a new value happens after each conversion of the channel selected by EMUXCHNR. For each update, EMUX is automatically decremented by 1. If EMUX = 0, it is reloaded with the value of SETEMUX for the next update. For each conversion of the selected channel, the setting of EMSAMPLE is applied.
  With enabled trigger option, the external multiplexer control block triggers a new conversion request each time a conversion is started of the channel defined by EMUXCHNR while EMUX > 0.
  In a scan request source, the corresponding pending bit becomes set, whereas in a sequential request source, the content of the backup stage becomes valid (V bit of backup stage becomes set).
  With this setting, all external multiplexer inputs are scanned during a single autoscan sequence, starting with the channel indicated by SETEMUX (same update rate of all channels of this sequence).
  Assuming inputs 1, 2, 70, 71, and 72 being selected for scan, the following sequence will be executed: 1, 2, 72, 71, 70, 1, 2, 72, 71, 70, 1, 2, 72, 71, 70, 1, 2, 72, ...

31.2.19 Synchronized Conversions for Parallel Sampling

The independent ADC kernels implemented in the TC1798 can be synchronized for simultaneous (parallel) measurements of analog input channels. While no parallel conversion is requested, the kernels can work independently.
The synchronization mechanism for parallel conversions ensures that the sample phases of the related channel start simultaneously. Different values for the resolution and the sample phase length of each kernel for a parallel conversion are supported.
A parallel conversion can be requested individually for each input channel (also several channels can be enabled for parallel conversions). In the example shown in the figure below, input channels CH3 of the ADC kernels ADC0 and ADC1 are converted synchronously, whereas other input channels do not lead to parallel conversions.

This leads to the following structure:

- A **synchronization master** ADC kernel can request a conversion of an analog channel. If this channel is selected for a synchronized conversion, it is also requested in the connected slave ADC kernel(s).
- A **synchronization slave** ADC kernel reacts to incoming synchronized conversion requests from its master. While no incoming master requests are active, the slave kernel can convert its own requests.
- All ADC kernels in an ADC module being similar, each kernel can be set up to be a synchronization master or a synchronization slave (depending on the application needs, such as trigger capability of request sources).
- A synchronization master can synchronize several slave kernels, whereas a slave kernel can only be synchronized to one master kernel.

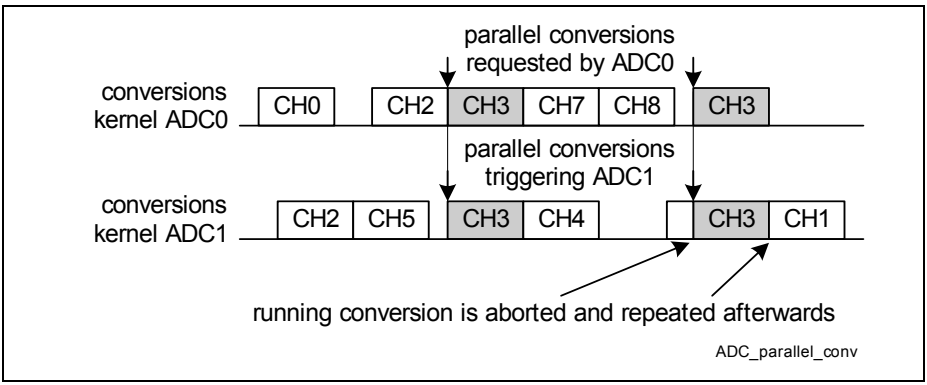


Figure 31-26 Parallel Conversions

The term “conversion group” has been introduced to define the kernel behavior allowing parallel sampling:

- Kernels in the same conversion group can execute parallel conversions.
- A conversion group contains at least 1 ADC kernel and can contain a maximum of all ADC kernels of the ADC module.
- Each conversion group contains exactly one synchronization master kernel that issues a parallel conversion request and defines the internal frequencies f_{ADCI} and f_{ADCD} and the channel number for a parallel conversion of the conversion group.
- All other kernels in a conversion group are synchronization slaves and have to be programmed with the same values of **GLOBCTR**.DIVA, DIVD and ARBRND as the synchronization master.
- If there is no need for parallel conversions, each kernel can be considered to form an own conversion group with only an ADC kernel as synchronization master, but without any synchronization slave.
- The channel number and the synchronization request are issued by the synchronization master to the kernels in the same synchronization group if a conversion is requested with **CHCTRx (x = 0 - 15)**.SYNC = 1 in the synchronization master kernel. Synchronization slaves can not issue synchronization requests.
- Once started, a parallel conversion can not be aborted.
- A parallel conversion request is always handled with highest priority and cancel-inject-repeat mode in a synchronization slave (see **Section 31.2.7.2**).
- Bit **GLOBCTR**.ARBM has to be 0 for synchronization slaves.
- The wait-for-read mode is supported for the master kernel, whereas the setting is ignored in the slave kernels (previous results may be overwritten).

The synchronization request issuing mechanism of the master to the slave kernels is based on bit field **GLOBSTR**.ANON. The information given by **GLOBCTR**.ANON is distributed by the synchronization master to all kernels in the conversion group (the bit fields **SYNCTR**.STSEL of all kernels must be programmed in a way that all kernels refer to the same information). In addition to the ANON information, the master delivers the requested channel number to the slave (not explicitly shown in **Figure 31-27**).
The start of the converters of all kernels of a conversion group is based on signals indicating when a kernel is ready and can start the sample phase of a parallel conversion. Bit **SYNCTR**.EVALRx defines if a kernel has to wait for the other kernel(s) (to allow parallel conversions) or can start without waiting (no parallel conversions possible). To support parallel conversions, all ready signals of the kernels of a conversion group have to be considered.

The alias feature is independent of synchronized conversions. All kernels of a conversion group request the same channel number (defined by the master), but can convert analog signals from different inputs. The requested channel number can be redirected by its alias setting. E.g., if the channel number requested in a conversion group is channel CH0, but for a kernel, an alternative reference is connected to this input,

the actually converted analog input can be changed to any value. This can be done by programming bit field ALIAS0 accordingly.

Note: A parallel conversion in a slave ADC should not target a result register that is already used for data reduction of other channels.

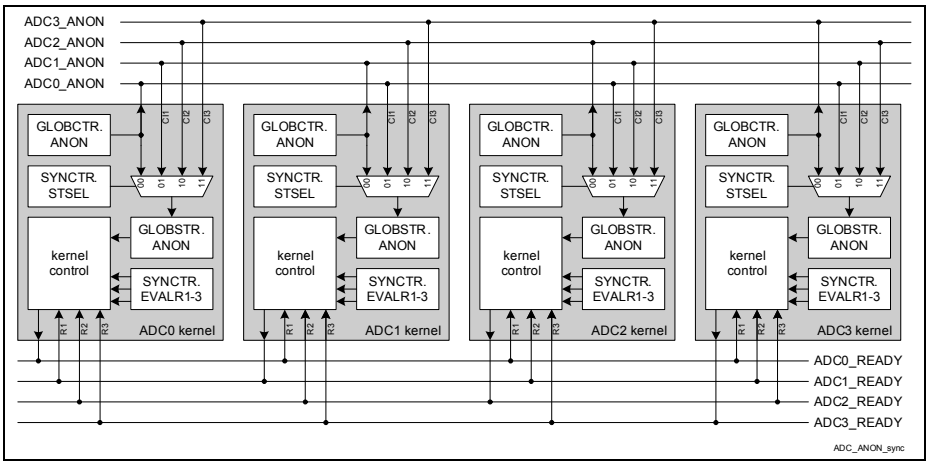


Figure 31-27 Synchronization via ANON and Ready Signals

The connections of the ADCx_ANON and ADCx_READY signals, as well as the programming hints for register EMCTR are described in the implementation chapter, see **Section 31.3**.

31.2.20 Equidistant Sampling

Each ADC kernel supports equidistant sampling of one (or more) analog input channels, e.g. for audio purposes or digital filters.

Therefore, each request source can be programmed to take part in the arbitration round and to win the arbitration (depending on the programmed priority levels), but without starting the conversion immediately. The exact start point of the conversion is given by a control signal (generated outside the ADC module, e.g. by a timer module) that is selected as trigger input REQTRx of request source x. Equidistant sampling is ensured if the REQTRx signal is generated synchronously to the arbiter timing, mainly for the arbiter. Each ADC kernel provides an output ARBCNT, that is activated once per arbitration round to count the arbiter cycles as timing base for the equidistant sampling by a timer located outside the ADC module.

A requested equidistant conversion can start its sampling phase if the converter is idle and the arbiter has decided which channel to convert. To ensure that the converter is idle, the arbiter decides which channel to convert (winner of the arbitration round), but it waits for the timer control signal to really start the measurement (preface time). If the request source selected for equidistant sampling has been programmed with the highest priority, no other request source can disturb the equidistant sampling.

The interpretation of the trigger signal REQTRx for equidistant sampling is enabled by selecting timer mode in the corresponding request source input register (RSIRx.TMEN = 1). The frequency of signal REQTRx defines the sampling rate and its high time defines the length of the preface time interval where the corresponding request source takes part in the arbitration. During the preface time, the currently running conversion can be finished. It has to be programmed to a value allowing the converter to become idle.

If signal ARBCNT is used as counting input signal for a timer, the arbiter has to be programmed to run permanently (GLOBCTR.ARBM = 0). If the timer has an independent time base, the arbiter can be stopped while no requests are pending. The preface time has to be longer than one arbitration round.

Depending on the request source requesting equidistant sampling, one or more channels can be converted one after the other. The order of the requested channels being fixed by the request source, the equidistant sampling is also supported for several channels. It is also possible to do equidistant sampling for more than one request source in parallel if the preface times and the equidistant conversions do not overlap.

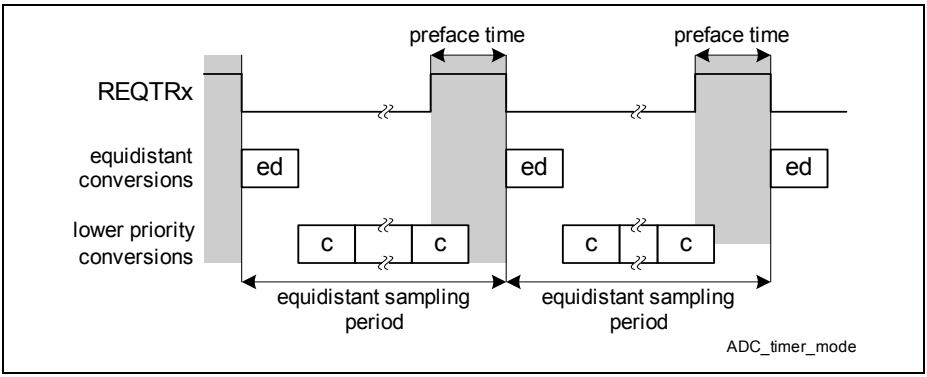


Figure 31-28 Timer Mode for Equidistant Sampling

31.2.21 Access Protection

An access protection scheme has been implemented to avoid unintended modification of some ADC control registers. It can be enabled by bits in register **APR** that itself is protected by the ENDINIT mechanism.
If the access protection is enabled for a group of registers and a write access occurs to one of them, the write access is discarded, the targeted register is not modified, the written data is ignored and the error flag ACCERR is set.
The protected ADC registers are located in one of the following register groups (registers not listed below can not be protected):

- Register group 0:
  GLOBCTR
- Register group 1:
  GLOBCFG, **EMCTR**, **RSIRx (x = 0 - 4)**, **ALR0**
- Register group 2:
  ASENR, **RSPR0**, **RSPR4**, **INPCRx (x = 0 - 3)**, **SYNCTR**
- Register group 3:
  CHCTRx (x = 0 - 15)
- Register group 4:
  RCRx (x = 0 - 15), **VFR**, **LCBR0**, **LCBR1**, **LCBR2**, **LCBR3**
- Register group 5:
  CHENPR0, **CHENPR8**, **EVNPR**, **RNPR0**, **RNPR8**, **INTR**, **CHFR**, **EVFR**

31.2.22 Broken Wire Detection

To support self-test in safety-critical applications, each ADC kernel provides a broken wire detection mechanism to check the connection of sensors or other voltage sources to the analog inputs of the ADC kernels.

This mechanism allows to prepare the capacitor field C_{AIN} before starting the sample phase and the conversion phase. A preparation phase is added to each conversion of an input channel with **BWDENR**.ENx = 1 (the broken wire detection can be individually enabled for each input channel CH0 to CH15).

An analog to digital conversion consists of the following phases:

- **Optional preparation phase:**
  If a channel is enabled for broken wire detection, the capacitor field C_{AIN} is connected to the analog input CHx defined by **BWDCFGR**.CHP before the sample phase starts. The preparation phase length is identical to the sample phase length for this conversion.
  If a channel is disabled for broken wire detection, the preparation phase is omitted (default setting).
- **Sample phase:**
  During this phase, the capacitor field C_{AIN} is connected to one of the analog inputs CHx via an input multiplexer (see **Section 31.1.8.1**). The request sources and the arbiter define which analog input has the highest priority.
- **Conversion phase:**
  During this phase, the capacitor field C_{AIN} is not connected to an analog input and the analog to digital conversion takes place. At the end of this phase, C_{AIN} is loaded to about $V_{AREF}/2$.

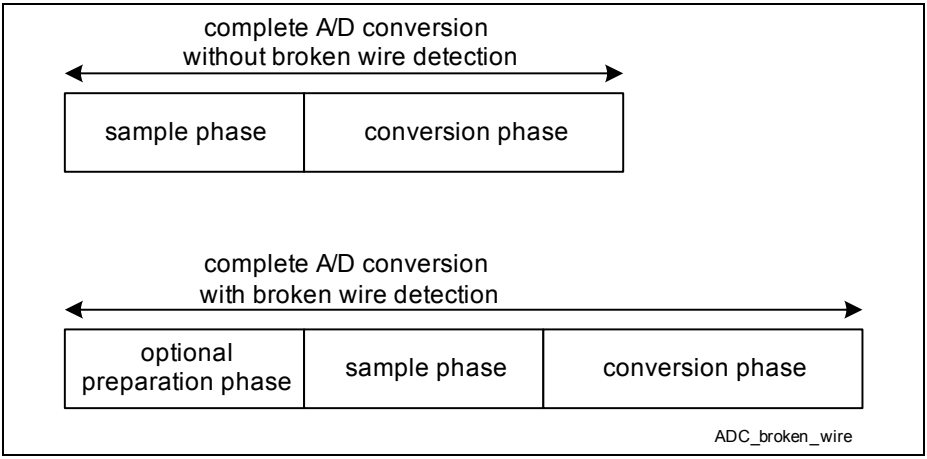


Figure 31-29 Broken Wire Detection

The broken wire detection mechanism allows to apply a voltage outside the expected measurement value range of the connected sensor. If the actual digital conversion result is located outside the expected measurement range (e.g. by using limit checking) with enabled broken wire detection, a defective connection has been detected. It is recommended to ensure enough margin between the voltage applied during the preparation phase and the sensors output range to minimize the effects of parasitics and leakage.

Input channels CH30 (V_{AGND}) and CH31 (V_{AREF}) have been especially introduced to allow the selection of the maximum or the minimum voltage of the measurement range.

Note: The length of the complete analog to digital conversion is increased by the length of the preparation phase if the broken wire detection is enabled. This influences the timing of conversion sequences.

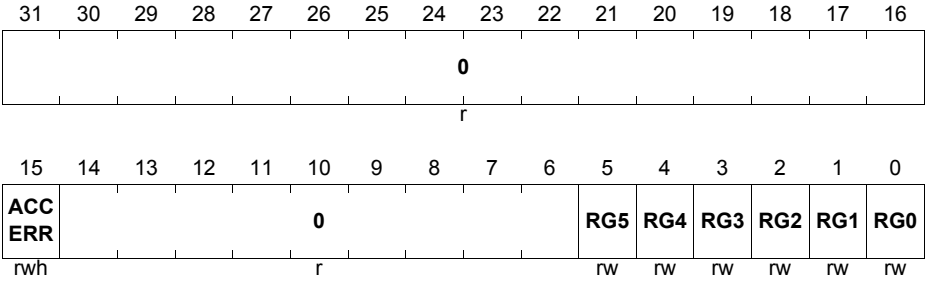
The preparation phase is introduced as additional presample phase (same behavior as the standard sampling phase, but with the possibility to select a different channel number). The analog part provides additional inputs for the channel number to be used during the presample phase and an enable line. The channel number is directly connected to BWDCFGR.CHP, whereas the enable line corresponds to the BWDENR.ENx bit for the arbitration winner CH x. The analog part expects these values at the beginning of the conversion (like all other signals) and automatically handles the insertion of the presample phase (handled like two consecutive sample phases with different channel numbers (but same length) before starting the conversion phase).

31.2.23 Additional Feature Registers

31.2.23.1 Access Protection Register

The access protection register APR contains bits to enable/disable modification of ADC control/configuration registers by write accesses. Register APR itself is protected by the ENDINIT mechanism.

APR
Access Protection Register **(218_H)** **Reset Value: 0000 0000_H**



Field	Bits	Type	Description
RGx (x = 0 - 5)	x	rw	**Register Group x** This bit enables/disables write accesses to registers of register group x. 0_B Write actions to register group x are enabled and can modify the register contents. 1_B Write actions to register group x are disabled and do not modify the register contents.
ACCERR	15	rwh	**Access Error** This flag indicates a violation of the access protection mechanism for the ADC kernel. It can be cleared by writing 1 to this bit position. Writing 0 has no effect. 0_B A write access to a protected register group has not been detected. 1_B A write access to a protected register group has been detected and discarded.
0	[31:16], [14:6]	r	**Reserved** Read as 0; should be written with 0.

31.2.23.2 External Multiplexer Control

The external multiplexer control register defines the settings of the external analog multiplexer.

EMCTR

External Multiplexer Control Register (220_H) **Reset Value: $0000\ 0000_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0								EMUXEN	SCANEN	TROEN	0	EMUXCHNR			
r								rw	rw	rw	r	rw			

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EMSAMPLE								0	EMUX			0	SETEMUX		
rw								r	rh			r	rw		

Field	Bits	Type	Description
SETEMUX	[2:0]	rw	**Setting of External Multiplexer** If the external multiplexer control is disabled, EMUX is loaded with the SETEMUX value. If enabled, the following two options are available: Scan Mode disabled: This bit field defines the input of the external multiplexer that will be selected for the next conversion of the channel selected by EMUXCHNR. Bit field EMUX will be updated by SETEMUX at the beginning of the next conversion of this channel. Scan Mode enabled: This bit field defines the start value of the scan of the external multiplexer inputs. The scan starts with the programmed input down to input 0. Bit field EMUX is updated by SETEMUX at the end of the conversion of this channel if EMUX = 0.

Field	Bits	Type	Description
EMUX	[6:4]	rh	**Current Setting for External Multiplexer** This bit field defines the input of the external multiplexer selected for conversion. Its value is available at the output lines EMUX[2:0]. If the external multiplexer control is disabled, EMUX is loaded with the SETEMUX value. If enabled, the following two options are available: Scan Mode disabled: This bit field becomes updated by SETEMUX at the beginning of the conversion of the channel selected by EMUXCHNR. Scan Mode enabled: This bit field is decremented by 1 at the end of the conversion of the channel selected by EMUXCHNR. After reaching 0, it is reloaded with the value of bit field SETEMUX.
EMSAMPLE	[15:8]	rw	**External Multiplexer Sampling Time** This bit field defines the alternative sample phase length in the case the external multiplexer setting has changed with the start of a conversion with enabled external multiplexer (the value given by the selected input class is not taken into account). A minimum sample phase of 2 analog clock cycles is extended by the programmed value. sample phase length = (2 + EMSAMPLE) / f_{ADCI}
EMUXCHNR	[19:16]	rw	**Channel Number for External Multiplexer** If external multiplexer control is enabled (EMUXEN = 1), this bit field defines the analog ADC input channel connected to the external analog multiplexer.

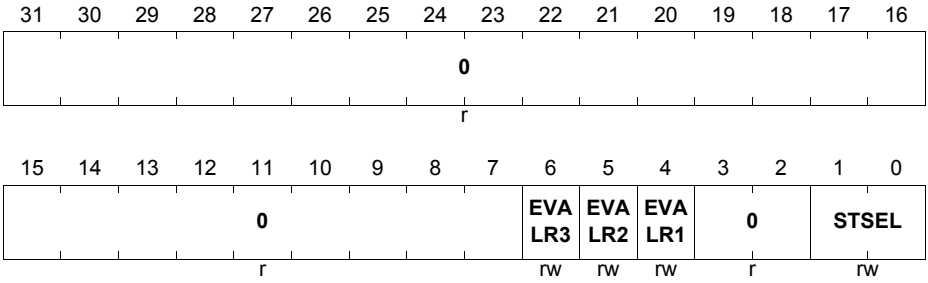
Field	Bits	Type	Description
TROEN	21	rw	**Trigger Option Enable** This bit selects the scan mode behavior of the external multiplexer (if enabled). Description see **Section 31.2.18**. 0_B Single-input scan is selected. The trigger option is disabled (no automatic trigger of more conversions of CHx). 1_B Multi-input scan is selected. The trigger option is enabled leading to an automatic scan through the externally connected multiplexer inputs by automatically triggering additional conversions of CHx until EMUX = 0.
SCANEN	22	rw	**Scan Enable** This bit enables/disables the automatic scan of the inputs of the external multiplexer for conversions of the channel selected by bit field EMUXCHNR (taken into account only if EMUXEN=1). 0_B The scan mode is disabled. Bit field EMUX is updated by bit field SETEMUX at the beginning of a conversion of the selected channel. If bit EMUX is changed, the value of EMSAMPLE is applied. 1_B The scan mode is enabled. Bit field EMUX is decremented by 1 for each conversion of the selected channel. After reaching 0, bit field EMUX is updated by bit field SETEMUX. The value of EMSAMPLE is always applied for the selected channel. It is recommended to write the start value of the first scan sequence to SETEMUX while EMUXEN=0.

Field	Bits	Type	Description
EMUXEN	23	rw	**External Multiplexer Control Enable** This bit enables/disables the automatic control of the external multiplexer. 0_B The external multiplexer control by HW is disabled. Bit field EMUX is immediately updated under SW control by writing to SETEMUX. The settings of SCANEN and TROEN are ignored. 1_B The external multiplexer control is enabled. The update of EMUX is under HW control respecting the conversion timings.
0	3, 7, 20, [31:24]	r	**Reserved** Read as 0; should be written with 0.

31.2.23.3 Synchronization Control Register

The synchronization control register contains bits controlling the synchronization between several kernels for parallel conversions. The programming of register SYNCTR in the kernels of a conversion group has to be done while the bit fields **GLOBCTR**.ANON = 00_B in all ADC kernels of the conversion group. Bit field **GLOBCTR**.ANON of the synchronization master can be set to 11_B afterwards.
The bits EVALRx are only taken into account if a synchronized, parallel conversion is requested by a master. This ensures that the conversions of the ADC kernels of the same synchronization group are started at the same time for parallel sampling (although a kernel might be idle, the master and all its connected slaves have to wait for all of them being ready).

SYNCTR
Synchronization Control Register (048_H) Reset Value: 0000 0000_H



Field	Bits	Type	Description
STSEL	[1:0]	rw	**Start Selection** This bit field controls the synchronization mechanism of the ADC kernel. 00_B The kernel is a synchronization master. The kernels own bit field GLOBCTR.ANON is taken into account. 01_B The kernel is a synchronization slave. The control information at input CI1 is taken into account instead. 10_B The kernel is a synchronization slave. The control information at input CI2 is taken into account instead. 11_B The kernel is a synchronization slave. The control information at input CI3 is taken into account instead.

Field	Bits	Type	Description
EVALR1	4	rw	**Evaluate Ready Input R1** This bit defines if a kernel is considered to be part of a synchronization group. Parallel conversions can only be started if the synchronization master and all slaves of the conversion group indicate that they are ready to start a parallel conversion. 0_B The ready input R1 is not considered for the start of a parallel conversion of this conversion group. 1_B The ready input R1 is considered for the start of a parallel conversion of this conversion group.
EVALR2	5	rw	**Evaluate Ready Input R2** This bit defines if a kernel is considered to be part of a synchronization group. Parallel conversions can only be started if the synchronization master and all slaves of the conversion group indicate that they are ready to start a parallel conversion. 0_B The ready input R2 is not considered for the start of a parallel conversion of this conversion group. 1_B The ready input R2 is considered for the start of a parallel conversion of this conversion group.
EVALR3	6	rw	**Evaluate Ready Input R3** This bit defines if a kernel is considered to be part of a synchronization group. Parallel conversions can only be started if the synchronization master and all slaves of the conversion group indicate that they are ready to start a parallel conversion. 0_B The ready input R3 is not considered for the start of a parallel conversion of this conversion group. 1_B The ready input R3 is considered for the start of a parallel conversion of this conversion group.
0	[3:2], [31:7]	r	**Reserved** Read as 0; should be written with 0.

31.2.23.4 Broken Wire Detection Enable Register

The broken wire detection enable register defines if a channel is enabled for broken wire detection by introducing an additional preparation phase to the sample phase (see **Section 31.2.22**). The channel number refers to the arbitration winner (can be directed to another input by the alias feature).

BWDENR
Broken Wire Detection Enable Register

(224_H) **Reset Value: 0000 0000$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

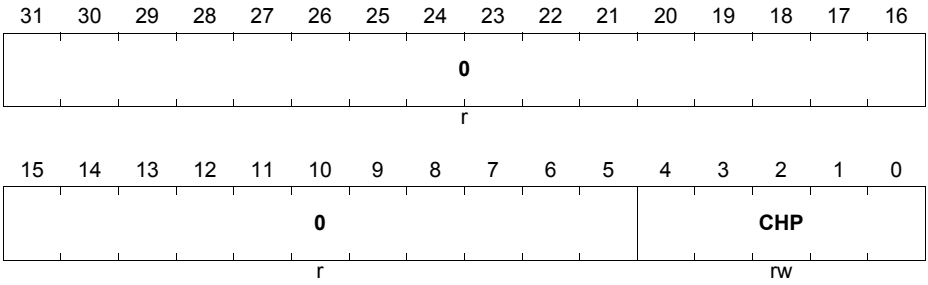
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
EN 15	**EN 14**	**EN 13**	**EN 12**	**EN 11**	**EN 10**	**EN 9**	**EN 8**	**EN 7**	**EN 6**	**EN 5**	**EN 4**	**EN 3**	**EN 2**	**EN 1**	**EN 0**
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Field	Bits	Type	Description
ENx (x=0-15)	x	rw	**Broken Wire Detection Enable for Channel CHx** This bit defines if the broken wire detection is enabled for CHx. 0_B The broken wire detection is disabled. 1_B The broken wire detection is enabled.
0	[31:16]	r	**Reserved** Read as 0; should be written with 0.

31.2.23.5 Broken Wire Detection Configuration Register

The broken wire detection configuration register defines which channel number is used for the additional preparation phase.

BWDCFGR
Broken Wire Detection Configuration Register
(228_H) **Reset Value: $0000\ 0000_H$**



Field	Bits	Type	Description
CHP	[4:0]	rw	**Channel Number for Preparation Phase** This bit field defines which input channel is used for the preparation phase for the broken wire detection.
0	[31:5]	r	**Reserved** returns 0 if read; should be written with 0;

31.3 Implementation

This chapter describes the implementation of the ADC kernels in the TC1798 device. It contains the following sections:

- Request sources (see **Section 31.3.1**)
- Address map (see **Section 31.3.2**)
- Result Data Filter (see **Section 31.3.3**)
- Connections to modules and pins (see **Section 31.3.4**)

31.3.1 Request Sources in TC1798

In each ADC kernel 5 request sources are implemented. They are numbered source 0 to source 4, with source x being evaluated in arbitration slot x. Each request source has the possibility to select one trigger input REQTRx out of a vector REQTRx_[7:0] and one gating input REQGTx out of a vector REQGTx_[7:0]. Each input vector contains 8 possible input signals, but not all of them are necessarily connected.

- Source 0: 1-stage sequential source
- Source 1: Parallel source for up to 16 channels
- Source 2: 4-stage sequential source
- Source 3: Parallel source for up to 16 channels
- Source 4: 4-stage sequential source

31.3.2 Address Map

The common KSCFG register of the ADC module can be accessed in the address range of kernel ADC0. The corresponding address in the range of kernel ADC1 to ADC3 is not used and delivers a dummy value when read.
The ADC kernels are available at the following base addresses:

Table 31-4 Registers Address Space

Module	Base Address	End Address	Note
ADC0	$F010\ 1000_H$	$F010\ 13FF_H$	
ADC1	$F010\ 1400_H$	$F010\ 17FF_H$	
ADC2	$F010\ 1800_H$	$F010\ 1BFF_H$	
ADC3	$F010\ 1C00_H$	$F010\ 1FFF_H$	

Table 31-5 Registers Overview

Register Short Name	Register Long Name	Offset Address	Page Number
please refer to register table in Section 31.2.1		H	

31.3.3 Result Data Filter

The implementation of the result data filter as part of the result handling is individual for each ADC kernel. The result register numbers providing a data filter have been chosen in order to allow the maximum number of FIFO stages (e.g. the filtered result of RESR15 can be FIFO-buffered in RESR14).
The result data filter are available at the following ADC kernels:

Table 31-6 Availability of Result Data Filter in the ADC Kernels

ADC Kernel	Number of Data Filter	Result Registers with Data Filter
ADC0	4	RESR3, RESR7, RESR11, RESR15
ADC1	4	RESR3, RESR7, RESR11, RESR15
ADC2	8	RESR1, RESR3, RESR5, RESR7, RESR9, RESR11 RESR13, RESR15
ADC3	0	-

31.3.4 ADC Module Connections

In addition to the standard signals of the interface between the analog and the digital parts, some side band signals have been introduced.
The ADC module consists of four ADC kernels. All kernels support the feature set listed above and share a common ADC0_KSCFG register. The kernels can be synchronized to each other for parallel sampling.

The channels CH4, CH5, CH6, and CH7 of ADC0 and the channels CH0 of all ADC kernels are always converted referring to the V_{AREF} input of the corresponding ADC kernel. For these channels, the programmed alternative reference selection is not taken into account. All other channels are converted with respect to the selected reference.

31.3.4.1 ADC0 Connections

Signals of the ADC module referring to the kernel of ADC0 are generally named with the prefix ADC0_.

The kernel ADC0 has its own reference inputs ADC0_V_{AGND} and ADC0_V_{AREF}. Depending on the package, these lines can be available as independent pins for high pin count packages or can be combined with the corresponding inputs of the other kernels for low pin count packages.
The respective voltage supply lines of all ADC analog parts are connected together.

Table 31-7 ADC0 Connections to Analog Part in TC1798

ADC0 Signal of Analog Part	from/to Module or Pin	Input or Output	Can be used to/as
V_{DDM}	V_{DDM}	I	analog power supply 3.3V - 5V
V_{DDA}	V_{DDMF}	I	analog power supply for comparator, connected to FADC 3.3V supply
V_{SSM}	V_{SSM}	I	analog power ground
V_{AREF}	V_{AREF}	I	positive analog reference
V_{AGND}	V_{AGND}	I	negative analog reference, combined with other kernels
CH0	AN0	I	analog input channel 0
CH1	AN1	I	analog input channel 1
CH2	AN2	I	analog input channel 2
CH3	AN3	I	analog input channel 3
CH4	AN4	I	analog input channel 4
CH5	AN5	I	analog input channel 5
CH6	AN6	I	analog input channel 6
CH7	AN7	I	analog input channel 7
CH8	AN8	I	analog input channel 8, overlaid with SENT
CH9	AN9	I	analog input channel 9, overlaid with SENT
CH10	AN10	I	analog input channel 10, overlaid with SENT
CH11	AN11	I	analog input channel 11, overlaid with SENT

Table 31-7 ADC0 Connections to Analog Part in TC1798 (cont'd)

ADC0 Signal of Analog Part	from/to Module or Pin	Input or Output	Can be used to/as
CH12	AN12	I	analog input channel 12, overlaid with SENT
CH13	AN13	I	analog input channel 13, overlaid with SENT
CH14	AN14	I	analog input channel 14, overlaid with SENT
CH15	AN15	I	analog input channel 15, overlaid with SENT

The following table shows the digital connections of the ADC0 kernel with other modules or pins in the TC1798 device. Signals of the ADC module referring to the kernel of ADC0 are named with the prefix ADC0_.

Table 31-8 ADC0 Connections of Digital Part in TC1798

ADC0 Signal of Digital Part	from/to Module or Pin	Input[1)] or Output	Can be used to/as
Kernel Signals			
ARBCNT	-	O	Counting signal for arbiter rounds
EMUXTR	-	O	Trigger output for scanning the external multiplexer inputs
EMUX0	P7.2	O	control of external analog multiplexer(s)
EMUX1	P7.3		
EMUX2	P7.1		
Request Source 0			
REQGT0_0	TRIG10	I	GPTA
REQGT0_1	TRIG12	I	GPTA
REQGT0_2	TRIG14	I	GPTA
REQGT0_3	PDOUT2	I	ERU
REQGT0_4	REQ0	I (s)	P1.0
REQGT0_5	IRQ1	I (s)	STM (do not use for gating, but for triggering)

Table 31-8 ADC0 Connections of Digital Part in TC1798 (cont'd)

ADC0 Signal of Digital Part	from/to Module or Pin	Input[1] or Output	Can be used to/as
REQGT0_6	0	I (s)	not (yet) connected
REQGT0_7	CCU6263_TRIG0	I (s)	CCU6263
REQTR0_0	TRIG00	I	GPTA
REQTR0_1	IOUT2	I	ERU
REQTR0_2	0	I	not (yet) connected
REQTR0_3	ADC_SR6	I	common service request output 6 of ADC module
REQTR0_4	REQ1	I (s)	P1.1
REQTR0_5	CCU6061_TRIG0	I (s)	CCU6061
REQTR0_6	ADC0_REQGT0	I (s)	extend input selection for triggering by using gating inputs (with ENGT = 0X)
REQTR0_7	ADC0_SR7	I (s)	service request output 7 of ADC0
REQTR0	-	O	selected trigger signal for source 0 (used as REQTRS for source 0)
REQGT0	ADC0_REQTR0_6	O	selected gating signal for source 0
Request Source 1			
REQGT1_0	TRIG10	I	GPTA
REQGT1_1	TRIG12	I	GPTA
REQGT1_2	TRIG14	I	GPTA
REQGT1_3	PDOUT3	I	ERU
REQGT1_4	REQ0	I (s)	P1.0
REQGT1_5	IRQ1	I (s)	STM (do not use for gating, but for triggering)
REQGT1_6	0	I (s)	not (yet) connected
REQGT1_7	CCU6263_TRIG1	I (s)	CCU6263
REQTR1_0	TRIG03	I	GPTA
REQTR1_1	IOUT3	I	ERU
REQTR1_2	TRIG16	I	GPTA
REQTR1_3	ADC_SR6	I	common service request output 6 of ADC module

Table 31-8 ADC0 Connections of Digital Part in TC1798 (cont'd)

ADC0 Signal of Digital Part	from/to Module or Pin	Input[1] or Output	Can be used to/as
REQTR1_4	REQ1	I (s)	P1.1
REQTR1_5	CCU6061_TRIG1	I (s)	CCU6061
REQTR1_6	ADC0_REQGT1	I (s)	extend input selection for triggering by using gating inputs (with ENGT = 0X)
REQTR1_7	ADC0_SR7	I (s)	service request output 7 of ADC0
REQTR1	-	O	selected trigger signal for source 1 (used as REQTRS for source 1)
REQGT1	ADC0_REQTR1_6	O	selected gating signal for source 1
Request Source 2			
REQGT2_0	TRIG10	I	GPTA
REQGT2_1	TRIG12	I	GPTA
REQGT2_2	TRIG14	I	GPTA
REQGT2_3	PDOUT3	I	ERU
REQGT2_4	REQ4	I (s)	P7.0
REQGT2_5	IRQ1	I (s)	STM (do not use for gating, but for triggering)
REQGT2_6	0	I (s)	not (yet) connected
REQGT2_7	CCU6263_TRIG1	I (s)	CCU6263
REQTR2_0	TRIG04	I	GPTA
REQTR2_1	IOUT3	I	ERU
REQTR2_2	TRIG16	I	GPTA
REQTR2_3	ADC_SR6	I	common service request output 6 of ADC module
REQTR2_4	REQ5	I (s)	P7.1
REQTR2_5	CCU6061_TRIG1	I (s)	CCU6061
REQTR2_6	ADC0_REQGT2	I (s)	extend input selection for triggering by using gating inputs (with ENGT = 0X)
REQTR2_7	ADC0_SR7	I (s)	service request output 7 of ADC0
REQTR2	-	O	selected trigger signal for source 2 (used as REQTRS for source 2)

Table 31-8 ADC0 Connections of Digital Part in TC1798 (cont'd)

ADC0 Signal of Digital Part	from/to Module or Pin	Input[1] or Output	Can be used to/as
REQGT2	ADC0_REQTR2_6	O	selected gating signal for source 2
Request Source 3			
REQGT3_0	TRIG10	I	GPTA
REQGT3_1	TRIG12	I	GPTA
REQGT3_2	TRIG14	I	GPTA
REQGT3_3	PDOUT2	I	ERU
REQGT3_4	REQ4	I (s)	P7.0
REQGT3_5	IRQ1	I (s)	STM (do not use for gating, but for triggering)
REQGT3_6	0	I (s)	not (yet) connected
REQGT3_7	CCU6263_TRIG2	I (s)	CCU6263
REQTR3_0	TRIG07	I	GPTA
REQTR3_1	IOUT2	I	ERU
REQTR3_2	TRIG16	I	GPTA
REQTR3_3	ADC_SR6	I	common service request output 6 of ADC module
REQTR3_4	REQ5	I (s)	P7.1
REQTR3_5	CCU6061_TRIG2	I (s)	CCU6061
REQTR3_6	ADC0_REQGT3	I (s)	extend input selection for triggering by using gating inputs (with ENGT = 0X)
REQTR3_7	ADC0_SR7	I (s)	service request output 7 of ADC0
REQTR3	-	O	selected trigger signal for source 3 (used as REQTRS for source 3)
REQGT3	ADC0_REQTR3_6	O	selected gating signal for source 3
Request Source 4			
REQGT4_0	TRIG10	I	GPTA
REQGT4_1	TRIG12	I	GPTA
REQGT4_2	TRIG14	I	GPTA
REQGT4_3	PDOUT2	I	ERU
REQGT4_4	REQ0	I (s)	P1.0

Table 31-8 ADC0 Connections of Digital Part in TC1798 (cont'd)

ADC0 Signal of Digital Part	from/to Module or Pin	Input[1] or Output	Can be used to/as
REQGT4_5	IRQ1	I (s)	STM (do not use for gating, but for triggering)
REQGT4_6	0	I (s)	not (yet) connected
REQGT4_7	CCU6263_TRIG2	I (s)	CCU6263
REQTR4_0	TRIG11	I	GPTA
REQTR4_1	IOUT2	I	ERU
REQTR4_2	0	I	not (yet) connected
REQTR4_3	ADC_SR6	I	common service request output 6 of ADC module
REQTR4_4		I (s)	P7.4
REQTR4_5	CCU6061_TRIG2	I (s)	CCU6061
REQTR4_6	ADC0_REQGT4	I (s)	extend input selection for triggering by using gating inputs (with ENGT = 0X)
REQTR4_7	ADC0_SR7	I (s)	service request output 7 of ADC0
REQTR4	-	O	selected trigger signal for source 4 (used as REQTRS for source 4)
REQGT4	ADC0_REQTR4_6	O	selected gating signal for source 4

1) In case of input signals, the lines marked "I" don't contain synchronization stages, whereas the lines marked "I (s)" contain synchronization stages (so they can directly handle asynchronous input signals). A signal connected to an input line marked "I" has to be delivered from a block located in the same clock domain as the ADC (the signal has to be synchronous to the ADC clock domain).

31.3.4.2 ADC1 Connections

Signals of the ADC module referring to the kernel of ADC1 are named with the prefix ADC1_.

The kernel ADC1 has its own reference inputs ADC1_V_{AGND} and ADC1_V_{AREF}. Depending on the package, these lines can be available as independent pins for high pin count packages or can be combined with the corresponding inputs of the other kernels for low pin count packages.
The respective voltage supply lines of the ADC analog parts are connected together.

Table 31-9 ADC1 Connections of Analog Part in TC1798

ADC1 Signal of Analog Part	from/to Module or Pin	Input or Output	Can be used to/as
V_{DDM}	V_{DDM}	I	analog power supply 3.3V - 5V
V_{DDA}	V_{DDMF}	I	analog power supply for comparator, taken from FADC 3.3V supply
V_{SSM}	V_{SSM}	I	analog power ground
V_{AREF}	V_{AREF}	I	positive analog reference
V_{AGND}	V_{AGND}	I	negative analog reference, combined with other kernels
CH0	AN16	I	analog input channel 16
CH1	AN17	I	analog input channel 17
CH2	AN18	I	analog input channel 18
CH3	AN19	I	analog input channel 19
CH4	AN20	I	analog input channel 20
CH5	AN21	I	analog input channel 21
CH6	AN22	I	analog input channel 22
CH7	AN23	I	analog input channel 23
CH8	AN24	I	analog input channel 24
CH9	AN25	I	analog input channel 25
CH10	AN26	I	analog input channel 26
CH11	AN27	I	analog input channel 27
CH12	AN28	I	analog input channel 28
CH13	AN29	I	analog input channel 29

Table 31-9 ADC1 Connections of Analog Part in TC1798 (cont'd)

ADC1 Signal of Analog Part	from/to Module or Pin	Input or Output	Can be used to/as
CH14	AN30	I	analog input channel 30
CH15	AN31	I	analog input channel 31

The following table shows the digital connections of the ADC1 kernel with other modules or pins in the TC1798 device. Output signals of the ADC module referring to the kernel of ADC1 are named with the prefix ADC1_.

Table 31-10 ADC1 Connections of Digital Part in TC1798

ADC1 Signal of Digital Part	from/to Module or Pin	Input [1] or Output	Can be used to/as
Kernel Signals			
ARBCNT	-	O	Counting signal for arbiter rounds
EMUXTR	-	O	Trigger output for scanning the external multiplexer inputs
EMUX0	P7.6	O	control of external analog multiplexer(s)
EMUX1	P7.7		
EMUX2	-		
Request Source 0			
REQGT0_0	TRIG10	I	GPTA
REQGT0_1	TRIG12	I	GPTA
REQGT0_2	TRIG14	I	GPTA
REQGT0_3	PDOUT2	I	ERU
REQGT0_4	REQ4	I (s)	P7.0
REQGT0_5	IRQ1	I (s)	STM (do not use for gating, but for triggering)
REQGT0_6	ADC0_SR7	I (s)	ADC1 trigger by ADC0
REQGT0_7	CCU6061_TRIG0	I (s)	CCU6061
REQTR0_0	TRIG00	I	GPTA
REQTR0_1	IOUT2	I	ERU
REQTR0_2	0	I	not (yet) connected

Table 31-10 ADC1 Connections of Digital Part in TC1798 (cont'd)

ADC1 Signal of Digital Part	from/to Module or Pin	Input [1] or Output	Can be used to/as
REQTR0_3	ADC_SR6	I	common service request output 6 of ADC module
REQTR0_4	REQ5	I (s)	P7.1
REQTR0_5	CCU6263_TRIG0	I (s)	CCU6263
REQTR0_6	ADC1_REQGT0	I (s)	extend input selection for triggering by using gating inputs (with ENGT = 0X)
REQTR0_7	ADC1_SR7	I (s)	service request output 7 of ADC1
REQTR0	-	O	selected trigger signal for source 0 (used as REQTRS for source 0)
REQGT0	ADC1_REQTR0_6	O	selected gating signal for source 0
Request Source 1			
REQGT1_0	TRIG10	I	GPTA
REQGT1_1	TRIG12	I	GPTA
REQGT1_2	TRIG14	I	GPTA
REQGT1_3	PDOUT3	I	ERU
REQGT1_4	REQ4	I (s)	P7.0
REQGT1_5	IRQ1	I (s)	STM (do not use for gating, but for triggering)
REQGT1_6	ADC0_SR7	I (s)	ADC1 trigger by ADC0
REQGT1_7	CCU6061_TRIG1	I (s)	CCU6061
REQTR1_0	TRIG05	I	GPTA
REQTR1_1	IOUT3	I	ERU
REQTR1_2	TRIG16	I	GPTA
REQTR1_3	ADC_SR6	I	common service request output 6 of ADC module
REQTR1_4	REQ5	I (s)	P7.1
REQTR1_5	CCU6263_TRIG1	I (s)	CCU6263
REQTR1_6	ADC1_REQGT1	I (s)	extend input selection for triggering by using gating inputs (with ENGT = 0X)
REQTR1_7	ADC1_SR7	I (s)	service request output 7 of ADC1

Table 31-10 ADC1 Connections of Digital Part in TC1798 (cont'd)

ADC1 Signal of Digital Part	from/to Module or Pin	Input [1] or Output	Can be used to/as
REQTR1	-	O	selected trigger signal for source 1 (used as REQTRS for source 1)
REQGT1	ADC1_REQTR1_6	O	selected gating signal for source 1
Request Source 2			
REQGT2_0	TRIG10	I	GPTA
REQGT2_1	TRIG12	I	GPTA
REQGT2_2	TRIG14	I	GPTA
REQGT2_3	PDOUT3	I	ERU
REQGT2_4	REQ0	I (s)	P1.0
REQGT2_5	IRQ1	I (s)	STM (do not use for gating, but for triggering)
REQGT2_6	ADC0_SR7	I (s)	ADC1 trigger by ADC0
REQGT2_7	CCU6061_TRIG1	I (s)	CCU6061
REQTR2_0	TRIG06	I	GPTA
REQTR2_1	IOUT3	I	ERU
REQTR2_2	TRIG16	I	GPTA
REQTR2_3	ADC_SR6	I	common service request output 6 of ADC module
REQTR2_4	REQ1	I (s)	P1.1
REQTR2_5	CCU6263_TRIG1	I (s)	CCU6263
REQTR2_6	ADC1_REQGT2	I (s)	extend input selection for triggering by using gating inputs (with ENGT = 0X)
REQTR2_7	ADC1_SR7	I (s)	service request output 7 of ADC1
REQTR2	-	O	selected trigger signal for source 2 (used as REQTRS for source 2)
REQGT2	ADC1_REQTR2_6	O	selected gating signal for source 2
Request Source 3			
REQGT3_0	TRIG10	I	GPTA
REQGT3_1	TRIG12	I	GPTA
REQGT3_2	TRIG14	I	GPTA

Table 31-10 ADC1 Connections of Digital Part in TC1798 (cont'd)

ADC1 Signal of Digital Part	from/to Module or Pin	Input [1] or Output	Can be used to/as
REQGT3_3	PDOUT2	I	ERU
REQGT3_4	REQ0	I (s)	P1.0
REQGT3_5	IRQ1	I (s)	STM (do not use for gating, but for triggering)
REQGT3_6	ADC0_SR7	I (s)	ADC1 trigger by ADC0
REQGT3_7	CCU6061_TRIG2	I (s)	CCU6061
REQTR3_0	TRIG01	I	GPTA
REQTR3_1	IOUT2	I	ERU
REQTR3_2	TRIG16	I	GPTA
REQTR3_3	ADC_SR6	I	common service request output 6 of ADC module
REQTR3_4	REQ1	I (s)	P1.1
REQTR3_5	CCU6263_TRIG2	I (s)	CCU6263
REQTR3_6	ADC1_REQGT3	I (s)	extend input selection for triggering by using gating inputs (with ENGT = 0X)
REQTR3_7	ADC1_SR7	I (s)	service request output 7 of ADC1
REQTR3	-	O	selected trigger signal for source 3 (used as REQTRS for source 3)
REQGT3	ADC1_REQTR3_6	O	selected gating signal for source 3
Request Source 4			
REQGT4_0	TRIG10	I	GPTA
REQGT4_1	TRIG12	I	GPTA
REQGT4_2	TRIG14	I	GPTA
REQGT4_3	PDOUT3	I	ERU
REQGT4_4	REQ0	I (s)	P1.0
REQGT4_5	IRQ1	I (s)	STM (do not use for gating, but for triggering)
REQGT4_6	ADC0_SR7	I (s)	ADC1 trigger by ADC0
REQGT4_7	CCU6061_TRIG2	I (s)	CCU6061
REQTR4_0	TRIG13	I	GPTA

Table 31-10 ADC1 Connections of Digital Part in TC1798 (cont'd)

ADC1 Signal of Digital Part	from/to Module or Pin	Input [1] or Output	Can be used to/as
REQTR4_1	IOUT3	I	ERU
REQTR4_2	0	I	not (yet) connected
REQTR4_3	ADC_SR6	I	common service request output 6 of ADC module
REQTR4_4		I (s)	P7.5
REQTR4_5	CCU6263_TRIG2	I (s)	CCU6263
REQTR4_6	ADC1_REQGT4	I (s)	extend input selection for triggering by using gating inputs (with ENGT = 0X)
REQTR4_7	ADC1_SR7	I (s)	service request output 7 of ADC1
REQTR4	-	O	selected trigger signal for source 4 (used as REQTRS for source 4)
REQGT4	ADC1_REQTR4_6	O	selected gating signal for source 4

1) In case of input signals, the lines marked "I" don't contain synchronization stages, whereas the lines marked "I (s)" contain synchronization stages (so they can directly handle asynchronous input signals). A signal connected to an input line marked "I" has to be delivered from a block located in the same clock domain as the ADC (the signal has to be synchronous to the ADC clock domain).

31.3.4.3 ADC2 Connections

Signals of the ADC module referring to the kernel of ADC2 are generally named with the prefix ADC2_.

The kernel ADC2 has its own reference inputs ADC2_V_{AGND} and ADC2_V_{AREF}. Depending on the package, these lines can be available as independent pins for high pin count packages or can be combined with the corresponding inputs of the other kernels for low pin count packages.
The respective voltage supply lines of all ADC analog parts are connected together.

Table 31-11 ADC2 Connections to Analog Part in TC1798

ADC2 Signal of Analog Part	from/to Module or Pin	Input or Output	Can be used to/as
V_{DDM}	V_{DDM}	I	analog power supply 3.3V - 5V
V_{DDA}	V_{DDMF}	I	analog power supply for comparator, connected to FADC 3.3V supply
V_{SSM}	V_{SSM}	I	analog power ground
V_{AREF}	V_{AREF}	I	positive analog reference, independent from other kernels
V_{AGND}	V_{AGND}	I	negative analog reference, combined with other kernels
CH0	AN32	I	analog input channel 0
CH1	AN33	I	analog input channel 1
CH2	AN34	I	analog input channel 2
CH3	AN35	I	analog input channel 3
CH4	AN36	I	analog input channel 4, overlaid with SENT
CH5	AN37	I	analog input channel 5, overlaid with SENT
CH6	AN38	I	analog input channel 6, overlaid with SENT
CH7	AN39	I	analog input channel 7, overlaid with SENT
CH8	AN40	I	analog input channel 8, overlaid with SENT
CH9	AN41	I	analog input channel 9, overlaid with SENT

Table 31-11 ADC2 Connections to Analog Part in TC1798 (cont'd)

ADC2 Signal of Analog Part	from/to Module or Pin	Input or Output	Can be used to/as
CH10	AN42	I	analog input channel 10, overlaid with SENT
CH11	AN43	I	analog input channel 11, overlaid with SENT
CH12	AN44	I	analog input channel 12
CH13	AN45	I	analog input channel 13
CH14	AN46	I	analog input channel 14
CH15	AN47	I	analog input channel 15

The following table shows the digital connections of the ADC2 kernel with other modules or pins in the TC1798 device. Signals of the ADC module referring to the kernel of ADC2 are named with the prefix ADC2_.

Table 31-12 ADC2 Connections of Digital Part in TC1798

ADC2 Signal of Digital Part	from/to Module or Pin	Input[1] or Output	Can be used to/as
Kernel Signals			
ARBCNT	-	O	Counting signal for arbiter rounds
EMUXTR	-	O	Trigger output for scanning the external multiplexer inputs
EMUX0	P7.4	O	control of external analog multiplexer(s)
EMUX1	P7.5		
EMUX2	P7.0		
Request Source 0			
REQGT0_0	TRIG10	I	GPTA
REQGT0_1	TRIG12	I	GPTA
REQGT0_2	TRIG14	I	GPTA
REQGT0_3	PDOUT2	I	ERU
REQGT0_4	REQ6	I (s)	P7.4
REQGT0_5	IRQ1	I (s)	STM (do not use for gating, but for triggering)

Table 31-12 ADC2 Connections of Digital Part in TC1798 (cont'd)

ADC2 Signal of Digital Part	from/to Module or Pin	Input[1] or Output	Can be used to/as
REQGT0_6	ADC1_SR7	I (s)	ADC2 trigger by ADC1
REQGT0_7	0	I (s)	not (yet) connected
REQTR0_0	TRIG00	I	GPTA
REQTR0_1	IOUT2	I	ERU
REQTR0_2	0	I	not (yet) connected
REQTR0_3	ADC_SR6	I	common service request output 6 of ADC module
REQTR0_4	REQ7	I (s)	P7.5
REQTR0_5	0	I (s)	not (yet) connected
REQTR0_6	ADC2_REQGT0	I (s)	extend input selection for triggering by using gating inputs (with ENGT = 0X)
REQTR0_7	ADC2_SR7	I (s)	service request output 7 of ADC2
REQTR0	-	O	selected trigger signal for source 0 (used as REQTRS for source 0)
REQGT0	ADC0_REQTR0_6	O	selected gating signal for source 0
Request Source 1			
REQGT1_0	TRIG10	I	GPTA
REQGT1_1	TRIG12	I	GPTA
REQGT1_2	TRIG14	I	GPTA
REQGT1_3	PDOUT3	I	ERU
REQGT1_4	REQ7	I (s)	P7.5
REQGT1_5	IRQ1	I (s)	STM (do not use for gating, but for triggering)
REQGT1_6	ADC1_SR7	I (s)	ADC2 trigger by ADC1
REQGT1_7	0	I (s)	not (yet) connected
REQTR1_0	TRIG14	I	GPTA
REQTR1_1	IOUT3	I	ERU
REQTR1_2	TRIG16	I	GPTA
REQTR1_3	ADC_SR6	I	common service request output 6 of ADC module

Table 31-12 ADC2 Connections of Digital Part in TC1798 (cont'd)

ADC2 Signal of Digital Part	from/to Module or Pin	Input[1] or Output	Can be used to/as
REQTR1_4	REQ6	I (s)	P7.4
REQTR1_5	0	I (s)	not (yet) connected
REQTR1_6	ADC2_REQGT1	I (s)	extend input selection for triggering by using gating inputs (with ENGT = 0X)
REQTR1_7	ADC2_SR7	I (s)	service request output 7 of ADC2
REQTR1	-	O	selected trigger signal for source 1 (used as REQTRS for source 1)
REQGT1	ADC2_REQTR1_6	O	selected gating signal for source 1
Request Source 2			
REQGT2_0	TRIG10	I	GPTA
REQGT2_1	TRIG12	I	GPTA
REQGT2_2	TRIG14	I	GPTA
REQGT2_3	PDOUT3	I	ERU
REQGT2_4	REQ7	I (s)	P7.5
REQGT2_5	IRQ1	I (s)	STM (do not use for gating, but for triggering)
REQGT2_6	ADC1_SR7	I (s)	ADC2 trigger by ADC1
REQGT2_7	0	I (s)	not (yet) connected
REQTR2_0	TRIG14	I	GPTA
REQTR2_1	IOUT3	I	ERU
REQTR2_2	TRIG16	I	GPTA
REQTR2_3	ADC_SR6	I	common service request output 6 of ADC module
REQTR2_4	REQ6	I (s)	P7.4
REQTR2_5	0	I (s)	not (yet) connected
REQTR2_6	ADC2_REQGT2	I (s)	extend input selection for triggering by using gating inputs (with ENGT = 0X)
REQTR2_7	ADC2_SR7	I (s)	service request output 7 of ADC2
REQTR2	-	O	selected trigger signal for source 2
REQGT2	ADC2_REQTR2_6	O	selected gating signal for source 2

Table 31-12 ADC2 Connections of Digital Part in TC1798 (cont'd)

ADC2 Signal of Digital Part	from/to Module or Pin	Input[1] or Output	Can be used to/as
Request Source 3			
REQGT3_0	TRIG10	I	GPTA
REQGT3_1	TRIG12	I	GPTA
REQGT3_2	TRIG14	I	GPTA
REQGT3_3	PDOUT2	I	ERU
REQGT3_4	REQ6	I (s)	P7.4
REQGT3_5	IRQ1	I (s)	STM (do not use for gating, but for triggering)
REQGT3_6	ADC1_SR7	I (s)	ADC2 trigger by ADC1
REQGT3_7	0	I (s)	not (yet) connected
REQTR3_0	TRIG15	I	GPTA
REQTR3_1	IOUT2	I	ERU
REQTR3_2	TRIG16	I	GPTA
REQTR3_3	ADC_SR6	I	common service request output 6 of ADC module
REQTR3_4	REQ7	I (s)	P7.5
REQTR3_5	0	I (s)	not (yet) connected
REQTR3_6	ADC2_REQGT3	I (s)	extend input selection for triggering by using gating inputs (with ENGT = 0X)
REQTR3_7	ADC2_SR7	I (s)	service request output 7 of ADC2
REQTR3	-	O	selected trigger signal for source 3 (used as REQTRS for source 3)
REQGT3	ADC2_REQTR3_6	O	selected gating signal for source 3
Request Source 4			
REQGT4_0	TRIG10	I	GPTA
REQGT4_1	TRIG12	I	GPTA
REQGT4_2	TRIG14	I	GPTA
REQGT4_3	PDOUT2	I	ERU
REQGT4_4	REQ6	I (s)	P7.4

Table 31-12 ADC2 Connections of Digital Part in TC1798 (cont'd)

ADC2 Signal of Digital Part	from/to Module or Pin	Input[1] or Output	Can be used to/as
REQGT4_5	IRQ1	I (s)	STM (do not use for gating, but for triggering)
REQGT4_6	ADC1_SR7	I (s)	ADC2 trigger by ADC1
REQGT4_7	0	I (s)	not (yet) connected
REQTR4_0	TRIG15	I	GPTA
REQTR4_1	IOUT2	I	ERU
REQTR4_2	0	I	not (yet) connected
REQTR4_3	ADC_SR6	I	common service request output 6 of ADC module
REQTR4_4	REQ7	I (s)	P7.5
REQTR4_5	0	I (s)	not (yet) connected
REQTR4_6	ADC2_REQGT4	I (s)	extend input selection for triggering by using gating inputs (with ENGT = 0X)
REQTR4_7	ADC2_SR7	I (s)	service request output 7 of ADC2
REQTR4	-	O	selected trigger signal for source 4 (used as REQTRS for source 4)
REQGT4	ADC2_REQTR4_6	O	selected gating signal for source 4

1) In case of input signals, the lines marked "I" don't contain synchronization stages, whereas the lines marked "I (s)" contain synchronization stages (so they can directly handle asynchronous input signals). A signal connected to an input line marked "I"has to be delivered from a block located in the same clock domain as the ADC (the signal has to be synchronous to the ADC clock domain).

31.3.4.4 ADC3 Connections

Signals of the ADC module referring to the kernel of ADC3 are generally named with the prefix ADC3_.

The kernel ADC3 has its own reference inputs ADC4_V_{AGND} and ADC4_V_{AREF}. Depending on the package, these lines can be available as independent pins for high pin count packages or can be combined with the corresponding inputs of the other kernels for low pin count packages.
The respective voltage supply lines of all ADC analog parts are connected together.

Table 31-13 ADC3 Connections to Analog Part in TC1798

ADC3 Signal of Analog Part	from/to Module or Pin	Input or Output	Can be used to/as
V_{DDM}	V_{DDM}	I	analog power supply 3.3V - 5V
V_{DDA}	V_{DDMF}	I	analog power supply for comparator, connected to FADC 3.3V supply
V_{SSM}	V_{SSM}	I	analog power ground
V_{AREF}	V_{AREF}	I	positive analog reference, independent from other kernels
V_{AGND}	V_{AGND}	I	negative analog reference, combined with other kernels
CH0	AN48	I	analog input channel 0
CH1	AN49	I	analog input channel 1
CH2	AN50	I	analog input channel 2
CH3	AN51	I	analog input channel 3
CH4	AN52	I	analog input channel 4
CH5	AN53	I	analog input channel 5
CH6	AN54	I	analog input channel 6
CH7	AN55	I	analog input channel 7
CH8	AN56	I	analog input channel 8
CH9	AN57	I	analog input channel 9
CH10	AN58	I	analog input channel 10
CH11	AN59	I	analog input channel 11
CH12	AN60	I	analog input channel 12
CH13	AN61	I	analog input channel 13

Table 31-13 ADC3 Connections to Analog Part in TC1798 (cont'd)

ADC3 Signal of Analog Part	from/to Module or Pin	Input or Output	Can be used to/as
CH14	AN62	I	analog input channel 14
CH15	AN63	I	analog input channel 15

The following table shows the digital connections of the ADC3 kernel with other modules or pins in the TC1798 device. Signals of the ADC module referring to the kernel of ADC3 are named with the prefix ADC3_.

Table 31-14 ADC3 Connections of Digital Part in TC1798

ADC3 Signal of Digital Part	from/to Module or Pin	Input[1] or Output	Can be used to/as
Kernel Signals			
ARBCNT	-	O	Counting signal for arbiter rounds
EMUXTR	-	O	Trigger output for scanning the external multiplexer inputs
EMUX0	-	O	control of external analog multiplexer(s)
EMUX1	-		
EMUX2	-		
Request Source 0			
REQGT0_0	TRIG10	I	GPTA
REQGT0_1	TRIG12	I	GPTA
REQGT0_2	TRIG14	I	GPTA
REQGT0_3	PDOUT2	I	ERU
REQGT0_4	REQ6	I (s)	P7.4
REQGT0_5	IRQ1	I (s)	STM (do not use for gating, but for triggering)
REQGT0_6	ADC2_SR7	I (s)	ADC3 trigger by ADC2
REQGT0_7	0	I (s)	not (yet) connected
REQTR0_0	TRIG00	I	GPTA
REQTR0_1	IOUT2	I	ERU
REQTR0_2	0	I	not (yet) connected

Table 31-14 ADC3 Connections of Digital Part in TC1798 (cont'd)

ADC3 Signal of Digital Part	from/to Module or Pin	Input[1] or Output	Can be used to/as
REQTR0_3	ADC_SR6	I	common service request output 6 of ADC module
REQTR0_4	REQ7	I (s)	P7.5
REQTR0_5	0	I (s)	not (yet) connected
REQTR0_6	ADC3_REQGT0	I (s)	extend input selection for triggering by using gating inputs (with ENGT = 0X)
REQTR0_7	ADC3_SR7	I (s)	service request output 7 of ADC3
REQTR0	-	O	selected trigger signal for source 0 (used as REQTRS for source 0)
REQGT0	ADC0_REQTR0_6	O	selected gating signal for source 0
Request Source 1			
REQGT1_0	TRIG10	I	GPTA
REQGT1_1	TRIG12	I	GPTA
REQGT1_2	TRIG14	I	GPTA
REQGT1_3	PDOUT3	I	ERU
REQGT1_4	REQ7	I (s)	P7.5
REQGT1_5	IRQ1	I (s)	STM (do not use for gating, but for triggering)
REQGT1_6	ADC2_SR7	I (s)	ADC3 trigger by ADC2
REQGT1_7	0	I (s)	not (yet) connected
REQTR1_0	TRIG14	I	GPTA
REQTR1_1	IOUT3	I	ERU
REQTR1_2	TRIG16	I	GPTA
REQTR1_3	ADC_SR6	I	common service request output 6 of ADC module
REQTR1_4	REQ6	I (s)	P7.4
REQTR1_5	0	I (s)	not (yet) connected
REQTR1_6	ADC3_REQGT1	I (s)	extend input selection for triggering by using gating inputs (with ENGT = 0X)
REQTR1_7	ADC3_SR7	I (s)	service request output 7 of ADC2

Table 31-14 ADC3 Connections of Digital Part in TC1798 (cont'd)

ADC3 Signal of Digital Part	from/to Module or Pin	Input[1] or Output	Can be used to/as
REQTR1	-	O	selected trigger signal for source 1 (used as REQTRS for source 1)
REQGT1	ADC3_REQTR1_6	O	selected gating signal for source 1
Request Source 2			
REQGT2_0	TRIG10	I	GPTA
REQGT2_1	TRIG12	I	GPTA
REQGT2_2	TRIG14	I	GPTA
REQGT2_3	PDOUT3	I	ERU
REQGT2_4	REQ7	I (s)	P7.5
REQGT2_5	IRQ1	I (s)	STM (do not use for gating, but for triggering)
REQGT2_6	ADC2_SR7	I (s)	ADC3 trigger by ADC2
REQGT2_7	0	I (s)	not (yet) connected
REQTR2_0	TRIG14	I	GPTA
REQTR2_1	IOUT3	I	ERU
REQTR2_2	TRIG16	I	GPTA
REQTR2_3	ADC_SR6	I	common service request output 6 of ADC module
REQTR2_4	REQ6	I (s)	P7.4
REQTR2_5	0	I (s)	not (yet) connected
REQTR2_6	ADC3_REQGT2	I (s)	extend input selection for triggering by using gating inputs (with ENGT = 0X)
REQTR2_7	ADC3_SR7	I (s)	service request output 7 of ADC3
REQTR2	-	O	selected trigger signal for source 2
REQGT2	ADC3_REQTR2_6	O	selected gating signal for source 2
Request Source 3			
REQGT3_0	TRIG10	I	GPTA
REQGT3_1	TRIG12	I	GPTA
REQGT3_2	TRIG14	I	GPTA
REQGT3_3	PDOUT2	I	ERU

Table 31-14 ADC3 Connections of Digital Part in TC1798 (cont'd)

ADC3 Signal of Digital Part	from/to Module or Pin	Input[1] or Output	Can be used to/as
REQGT3_4	REQ6	I (s)	P7.4
REQGT3_5	IRQ1	I (s)	STM (do not use for gating, but for triggering)
REQGT3_6	ADC2_SR7	I (s)	ADC3 trigger by ADC2
REQGT3_7	0	I (s)	not (yet) connected
REQTR3_0	TRIG15	I	GPTA
REQTR3_1	IOUT2	I	ERU
REQTR3_2	TRIG16	I	GPTA
REQTR3_3	ADC_SR6	I	common service request output 6 of ADC module
REQTR3_4	REQ7	I (s)	P7.5
REQTR3_5	0	I (s)	not (yet) connected
REQTR3_6	ADC3_REQGT3	I (s)	extend input selection for triggering by using gating inputs (with ENGT = 0X)
REQTR3_7	ADC3_SR7	I (s)	service request output 7 of ADC3
REQTR3	-	O	selected trigger signal for source 3 (used as REQTRS for source 3)
REQGT3	ADC3_REQTR3_6	O	selected gating signal for source 3
Request Source 4			
REQGT4_0	TRIG10	I	GPTA
REQGT4_1	TRIG12	I	GPTA
REQGT4_2	TRIG14	I	GPTA
REQGT4_3	PDOUT2	I	ERU
REQGT4_4	REQ6	I (s)	P7.4
REQGT4_5	IRQ1	I (s)	STM (do not use for gating, but for triggering)
REQGT4_6	ADC3_SR7	I (s)	ADC3 trigger by ADC2
REQGT4_7	0	I (s)	not (yet) connected
REQTR4_0	TRIG15	I	GPTA
REQTR4_1	IOUT2	I	ERU

Table 31-14 ADC3 Connections of Digital Part in TC1798 (cont'd)

ADC3 Signal of Digital Part	from/to Module or Pin	Input[1] or Output	Can be used to/as
REQTR4_2	0	I	not (yet) connected
REQTR4_3	ADC_SR6	I	common service request output 6 of ADC module
REQTR4_4	REQ7	I (s)	P7.5
REQTR4_5	0	I (s)	not (yet) connected
REQTR4_6	ADC3_REQGT4	I (s)	extend input selection for triggering by using gating inputs (with ENGT = 0X)
REQTR4_7	ADC3_SR7	I (s)	service request output 7 of ADC3
REQTR4	-	O	selected trigger signal for source 4 (used as REQTRS for source 4)
REQGT4	ADC3_REQTR4_6	O	selected gating signal for source 4

1) In case of input signals, the lines marked "I" don't contain synchronization stages, whereas the lines marked "I (s)" contain synchronization stages (so they can directly handle asynchronous input signals). A signal connected to an input line marked "I"has to be delivered from a block located in the same clock domain as the ADC (the signal has to be synchronous to the ADC clock domain).

31.3.4.5 Service Request Connections

Each ADC kernel provides the service request output lines ADCy_SR[7:0]. The ADC module's service request outputs ADC_SR[11:0] are generated based on these lines according to the following table. If a line ADCy_SRx can be activated by more than one ADC kernel, the corresponding request lines of the ADC kernels are logical OR-combinations of the kernel outputs.
The wiring of the ADC_SRx signals to the DMA channels is given in the DMA chapter.
The signal ADCy_SR7 of each ADC kernel is available as input for the request sources for this kernel. Additionally, ADC0_SR7 is connected to ADC1 inputs, ADC1_SR7 is connected to ADC2 and ADC2_SR7 is connected to ADC3 inputs.
The common signal ADC_SR6 is available as input for the request sources of all kernels.

Table 31-15 ADC Module Service Request Generation

Module Service Request Output	from ADC0 Kernel	from ADC1 Kernel	from ADC2 Kernel	from ADC3 Kernel	Service Request Node
ADC_SR0	ADC0_SR0	ADC1_SR0	-	-	ADC0_SRC0
ADC_SR1	ADC0_SR1	ADC1_SR1	-	-	ADC0_SRC1
ADC_SR2	ADC0_SR2	ADC1_SR2	-	-	ADC0_SRC2
ADC_SR3	ADC0_SR3	ADC1_SR3	-	-	ADC0_SRC3
ADC_SR4	ADC0_SR4	ADC1_SR4	ADC2_SR4	ADC3_SR4	ADC0_SRC4
ADC_SR5	ADC0_SR5	ADC1_SR5	ADC2_SR5	ADC3_SR5	ADC0_SRC5
ADC_SR6	ADC0_SR6	ADC1_SR6	ADC2_SR6	ADC3_SR6	-
ADC_SR7	ADC0_SR7	ADC1_SR7	ADC2_SR7	ADC3_SR7	-
ADC_SR8	-	-	ADC2_SR0	ADC3_SR0	ADC0_SRC6
ADC_SR9	-	-	ADC2_SR1	ADC3_SR1	ADC0_SRC7
ADC_SR10	-	-	ADC2_SR2	ADC3_SR2	ADC0_SRC8
ADC_SR11	-	-	ADC2_SR3	ADC3_SR3	-

31.3.4.6 Kernel Synchronization

The independent ADC kernels of the ADC module can be synchronized to each other by selecting the corresponding connections. The table below shows the setting of the bits in the synchronization control registers in the ADC to allow synchronization. A kernel can operate completely autonomously if it is configured as master ADC. A slave ADC can be synchronized by the selected master ADC.

Note: A master ADC can synchronize several slave ADCs, whereas a slave ADC can only be synchronized by one master ADC.

Table 31-16 SYNCTR Setting for Kernel Synchronization

Operating Mode	SYNCTR. EVALR3	SYNCTR. EVALR2	SYNCTR. EVALR1	SYNCTR. STSEL
ADC0 Kernel (values to be programmed to ADC0_SYNCTR)				
no sync	0	0	0	00_B
master of only ADC1	0	0	1	00_B
master of only ADC2	0	1	0	00_B
master of only ADC3	1	0	0	00_B
master of ADC1 and ADC2	0	1	1	00_B
master of ADC1 and ADC3	1	0	1	00_B
master of ADC2 and ADC3	1	1	0	00_B
master of ADC1, ADC2 and ADC3	1	1	1	00_B
single slave of ADC1	0	0	1	01_B
ADC0 and ADC2 are slaves of ADC1	0	1	1	01_B

Table 31-16 SYNCTR Setting for Kernel Synchronization (cont'd)

Operating Mode	SYNCTR. EVALR3	SYNCTR. EVALR2	SYNCTR. EVALR1	SYNCTR. STSEL
ADC0 and ADC3 are slaves of ADC1	1	0	1	01_B
ADC0, ADC2 and ADC3 are slaves of ADC1	1	1	1	01_B
single slave of ADC2	0	1	0	10_B
ADC0 and ADC1 are slaves of ADC2	0	1	1	10_B
ADC0 and ADC3 are slaves of ADC2	1	1	0	10_B
ADC0, ADC1 and ADC3 are slaves of ADC2	1	1	1	10_B
single slave of ADC3	1	0	0	11_B
ADC0 and ADC1 are slaves of ADC3	1	0	1	11_B
ADC0 and ADC2 are slaves of ADC3	1	1	0	11_B
ADC0, ADC1 and ADC2 are slaves of ADC3	1	1	1	11_B

ADC1 Kernel (values to be programmed to ADC1_SYNCTR)

no sync	0	0	0	00_B
master of only ADC0	0	0	1	00_B
master of only ADC2	0	1	0	00_B

Table 31-16 SYNCTR Setting for Kernel Synchronization (cont'd)

Operating Mode	SYNCTR. EVALR3	SYNCTR. EVALR2	SYNCTR. EVALR1	SYNCTR. STSEL
master of only ADC3	1	0	0	00_B
master of ADC0 and ADC2	0	1	1	00_B
master of ADC1 and ADC3	1	0	1	00_B
master of ADC2 and ADC3	1	1	0	00_B
master of ADC1, ADC2 and ADC3	1	1	1	00_B
single slave of ADC0	0	0	1	01_B
ADC1 and ADC2 are slaves of ADC0	0	1	1	01_B
ADC1 and ADC3 are slaves of ADC0	1	0	1	01_B
ADC1, ADC2 and ADC3 are slaves of ADC0	1	1	1	01_B
single slave of ADC2	0	1	0	10_B
ADC0 and ADC1 are slaves of ADC2	0	1	1	10_B
ADC1 and ADC3 are slaves of ADC2	1	1	0	10_B
ADC0, ADC1 and ADC3 are slaves of ADC2	1	1	1	10_B
single slave of ADC3	1	0	0	11_B

Table 31-16 SYNCTR Setting for Kernel Synchronization (cont'd)

Operating Mode	SYNCTR. EVALR3	SYNCTR. EVALR2	SYNCTR. EVALR1	SYNCTR. STSEL
ADC0 and ADC1 are slaves of ADC3	1	0	1	11_B
ADC1 and ADC2 are slaves of ADC3	1	1	0	11_B
ADC0, ADC1 and ADC2 are slaves of ADC3	1	1	1	11_B
ADC2 Kernel (values to be programmed to ADC2_SYNCTR)				
no sync	0	0	0	00_B
master of only ADC0	0	0	1	00_B
master of only ADC1	0	1	0	00_B
master of only ADC3	1	0	0	00_B
master of ADC0 and ADC1	0	1	1	00_B
master of ADC0 and ADC3	1	0	1	00_B
master of ADC1 and ADC3	1	1	0	00_B
master of ADC0, ADC1 and ADC3	1	1	1	00_B
single slave of ADC0	0	0	1	01_B
ADC1 and ADC2 are slaves of ADC0	0	1	1	01_B

Table 31-16 SYNCTR Setting for Kernel Synchronization (cont'd)

Operating Mode	SYNCTR. EVALR3	SYNCTR. EVALR2	SYNCTR. EVALR1	SYNCTR. STSEL
ADC2 and ADC3 are slaves of ADC0	1	0	1	01_B
ADC1, ADC2 and ADC3 are slaves of ADC0	1	1	1	01_B
single slave of ADC1	0	1	0	10_B
ADC0 and ADC2 are slaves of ADC1	0	1	1	10_B
ADC2 and ADC3 are slaves of ADC1	1	1	0	10_B
ADC0, ADC2 and ADC3 are slaves of ADC1	1	1	1	10_B
single slave of ADC3	1	0	0	11_B
ADC0 and ADC2 are slaves of ADC3	1	0	1	11_B
ADC1 and ADC2 are slaves of ADC3	1	1	0	11_B
ADC0, ADC1 and ADC2 are slaves of ADC3	1	1	1	11_B

ADC3 Kernel (values to be programmed to ADC2_SYNCTR)

no sync	0	0	0	00_B
master of only ADC0	0	0	1	00_B
master of only ADC1	0	1	0	00_B

Table 31-16 SYNCTR Setting for Kernel Synchronization (cont'd)

Operating Mode	SYNCTR. EVALR3	SYNCTR. EVALR2	SYNCTR. EVALR1	SYNCTR. STSEL
master of only ADC2	1	0	0	00_B
master of ADC0 and ADC1	0	1	1	00_B
master of ADC0 and ADC2	1	0	1	00_B
master of ADC1 and ADC2	1	1	0	00_B
master of ADC0, ADC1 and ADC2	1	1	1	00_B
single slave of ADC0	0	0	1	01_B
ADC1 and ADC3 are slaves of ADC0	0	1	1	01_B
ADC2 and ADC3 are slaves of ADC0	1	0	1	01_B
ADC1, ADC2 and ADC3 are slaves of ADC0	1	1	1	01_B
single slave of ADC1	0	1	0	10_B
ADC0 and ADC3 are slaves of ADC1	0	1	1	10_B
ADC2 and ADC3 are slaves of ADC1	1	1	0	10_B
ADC0, ADC2 and ADC3 are slaves of ADC1	1	1	1	10_B
single slave of ADC2	1	0	0	11_B

Table 31-16 SYNCTR Setting for Kernel Synchronization (cont'd)

Operating Mode	SYNCTR. EVALR3	SYNCTR. EVALR2	SYNCTR. EVALR1	SYNCTR. STSEL
ADC0 and ADC3 are slaves of ADC2	1	0	1	11_B
ADC1 and ADC3 are slaves of ADC2	1	1	0	11_B
ADC0, ADC1 and ADC2 are slaves of ADC2	1	1	1	11_B

•

32 Fast Analog to Digital Converter (FADC)

The TC1798 contains a fast analog to digital converter (FADC) with differential input channels, thus allowing sampling of high frequency signals. For slow and mid-range frequency signals, an anti-aliasing filter by data reduction is implemented to avoid expensive external filters.

- Functional description of the FADC Kernel (see **Section 32.2**)
- FADC kernel register descriptions (see **Section 32.3**)
- TC1798 implementation-specific details and registers of the FADC module, including on-chip interconnections, service request control, address decoding, and clock control (see **Section 32.4**)

*Note: The FADC Kernel register names described in **Section 32.3** are referenced in the TC1798 User´s Manual by the module name prefix "FADC_" for the FADC interface.*

32.1 FADC Short Description

General Features

- Extreme fast conversion, 21 cycles of f_{FADC} clock (262.5 ns @ f_{FADC} = 80 MHz)
- 10-bit A/D conversion (higher resolution can be achieved by averaging of consecutive conversions in digital data reduction filter)
- Successive approximation conversion method
- Each differential input channel can also be used as single-ended input
- Offset calibration support for each channel
- Programmable gain of 1, 2, 4, or 8 for each channel
- Free-running (Channel Timers) or triggered conversion modes
- Trigger and gating control for external signals
- Built-in Channel Timers for internal triggering
- Channel timer request periods independently selectable for each channel
- Selectable, programmable digital anti-aliasing and data reduction filter block with four independent filter units

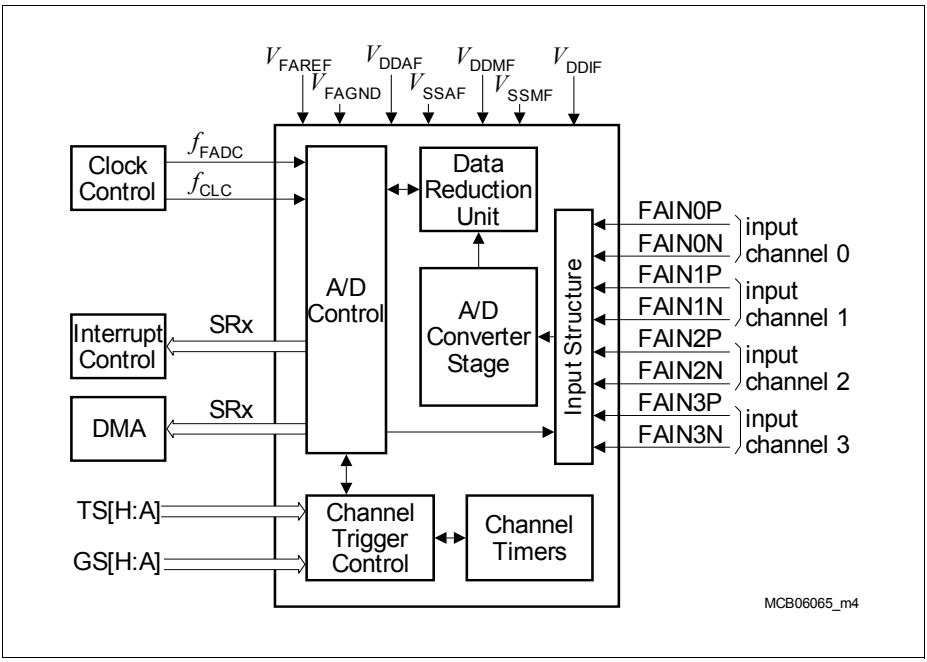


Figure 32-1 Block Diagram of the FADC Module with 4 Input Channels

As shown in **Figure 32-1**, the main FADC functional blocks are:

- An Input Structure containing the differential inputs and impedance control.
- An A/D Converter Stage responsible for the analog-to-digital conversion including an input multiplexer to select between the channel amplifiers
- A Data Reduction Unit containing programmable anti-aliasing and data reduction filters
- A Channel Trigger Control block determining the trigger and gating conditions for the FADC channels
- A Channel Timer for each channel to independently trigger the conversions
- An A/D Control block responsible for the overall FADC functionality

The analog block of the FADC in the TC1798 contains:

- A differential analog input stage for each input channel to select the input impedance (differential or single-ended measurement) and to decouple the FADC input signal from the pins. It is supplied by V_{DDIF} / V_{SSMF} (3.3 V - 5 V).
  The V_{DDIF} supply does not appear as supply pin in the pin list, because it is internally connected to the V_{DDM} supply of the ADC that is sharing the FADC input pins.
- A channel amplifier with a settling time of about 5µs if its configuration is changed by SW (changing between unused, differential, single-ended N, or single-ended P mode). It is supplied by V_{DDMF} / V_{SSMF} (3.3 V) .
- A 10-bit analog converter stage supplied by V_{DDAF} / V_{SSAF} (1.2 V)externally. The inputs for the FADC reference voltage (3.3 V max.) and the FADC reference ground V_{FAREF} / V_{FAGND} are connected to pins.

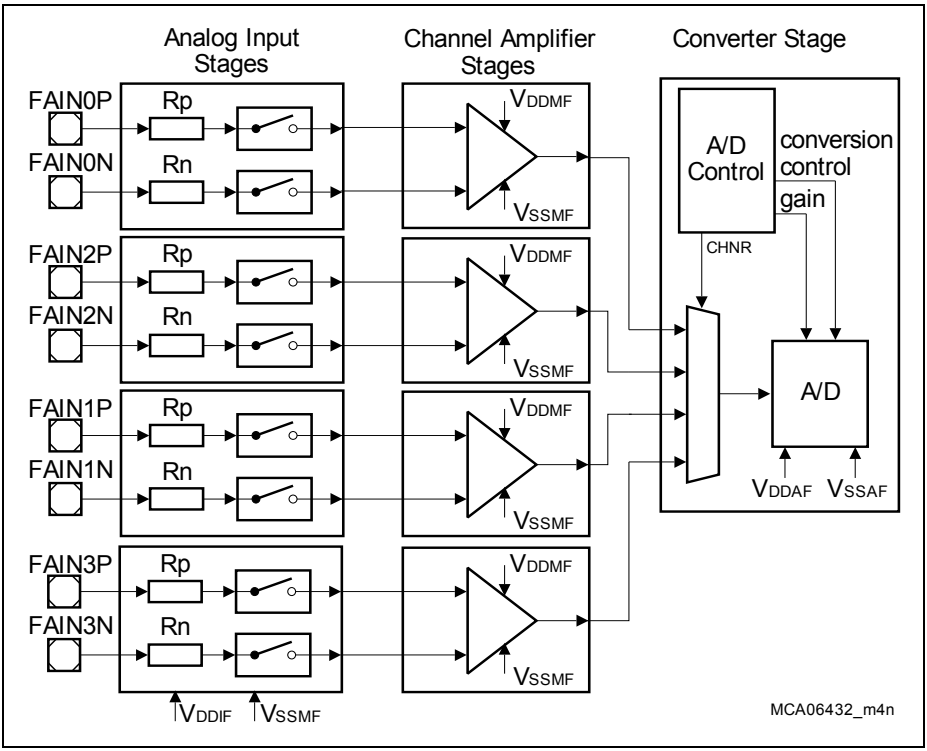


Figure 32-2 FADC Input Structure in TC1798

Note: The analog voltages of the FADC have to be stable and noise-free to ensure a high quality of the conversions.

32.2 FADC Kernel Description

The FADC kernel description covers the following items:

- Analog input stage configurations (see **Section 32.2.1**)
- Conversion timing (see **Section 32.2.3**)
- Channel triggers (see **Section 32.2.4**)
- Channel timers (see **Section 32.2.5**)
- Conversion control (see **Section 32.2.6**)
- Data reduction unit (see **Section 32.2.7**)
- Neighbor channel trigger (see **Section 32.2.8**)
- Offset calibration (see **Section 32.2.9**)
- Interrupt generation (see **Section 32.2.10**)

32.2.1 Analog Input Stage Configurations

The analog input stage makes it possible to control the input impedance by selecting different configurations independently for each FADC channel x. These combinations are shown in **Figure 32-3**.

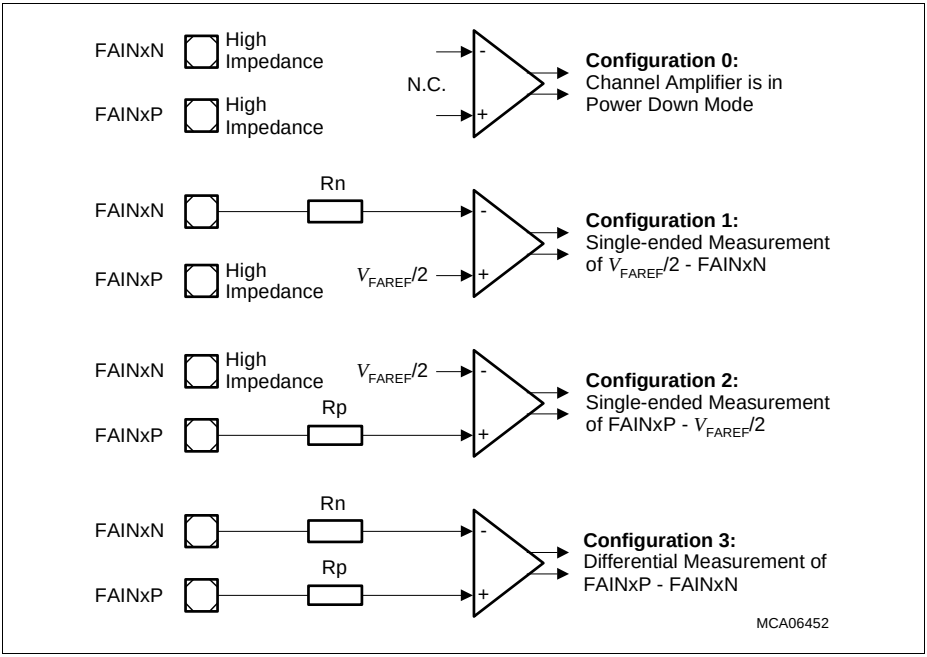


Figure 32-3 Analog Input Stage Configurations

Note: Due to the temperature characteristics of offset and gain of the internal amplifiers a TUE (total unadjusted error) cannot be specified. The input impedance for R_p and R_n is defined in the TC1798 Data Sheet.

Note: The analog input lines of the FADC can also be used as input lines for other ADCs. If both (regular ADC and FADC) are connected to the same pin at the same time, the input impedances of the analog inputs must be taken into account in order to minimize signal distortions and measurement errors.

Configuration 0: Channel Not Used (ACRx.ENP = ACRx.ENN = 0)

FADC channel x inputs FAINxP and FAINxN are in a high impedance state. The channel amplifier of the analog input stage is in power-down mode if both connected input channels are switched off for measurements.

Configuration 1: Single-ended of FAINxN (ACRx.ENP = 0 and ACRx.ENN = 1)

This configuration enables the single-ended measurement mode for $V_{VAREF}/2$ - FAINxN: The positive analog input FAINxP is disconnected is in a high impedance state. The negative analog input FAINxN is connected to the channel amplifier (input impedance is determined by R_n). The positive input of the channel amplifier is connected to $V_{FAREF}/2$ (1.65 V with V_{FAREF} = 3.3 V). If the voltage at the negative input FAINxN varies, the FADC will deliver conversion results as follows (gain = 1 selected by ACRx.GAIN = 00_B):

- FAINxN = 0 V: FADC conversion result is 768
- FAINxN = 3.3 V: FADC conversion result is 256

To cover the full range of the measurement result in this single-ended measurement mode, a gain of 2 must be selected (ACRx.GAIN = 01_B). With gain = 2, the FADC will deliver conversion results as follows:

- FAINxN = 0 V: FADC conversion result is 1023
- FAINxN = 3.3 V: FADC conversion result is 0

The voltage at the disconnected positive analog input FAINxP has no influence on the conversion result.

Configuration 2: Single-ended of FAINxP (ACRx.ENP = 1 and ACRx.ENN = 0)

This configuration enables the single-ended measurement mode for FAINxP - $V_{VAREF}/2$. The negative analog input FAINxN is disconnected and in a high impedance state. The positive analog input FAINxP is connected to the channel amplifier (input impedance is determined by R_p). The negative input of the channel amplifier is connected to $V_{FAREF}/2$ (1.65 V with V_{FAREF} = 3.3 V). If the voltage at the positive input FAINxP varies, the FADC will deliver conversion results as follows (gain = 1 selected by ACRx.GAIN = 00_B):

- FAINxP = 0 V: FADC conversion result is 256
- FAINxP = 3.3 V: FADC conversion result is 768

To cover the full range of the measurement result in this single-ended measurement mode, a gain of 2 must be selected (ACRx.GAIN = 01_B). With gain = 2, the FADC will deliver conversion results as follows:

- FAINxP = 0 V: FADC conversion result is 0
- FAINxP = 3.3 V: FADC conversion result is 1023

The voltage at the disconnected negative analog input FAINxN has no influence on the conversion result.

Configuration 3: Differential Measurement (ACRx.ENP = ACRx.ENN = 1)

This configuration enables the differential measurement mode for FAINxP - FAINxN. Both analog inputs, FAINx.N and FAINxP, are connected to the channel amplifier inputs. Their impedances are determined by R_n and R_p. The full measurement range is available.

32.2.2 Result Representation

The conversion result for FADC channel x is given by the following equations:

$$\text{Conversion Result } V_{Mx} = \text{GAIN}_x \times ((V_{FAINxP} - V_{FAREFM}) + (V_{FAREFM} - V_{FAINxN})) \quad (32.1)$$

$$\text{with } V_{FAREFM} = V_{FAGND} + (V_{FAREF} - V_{FAGND})/2$$

The absolute value of the result V_{Mx} is limited to V_{FAREF}. The mapping of the conversion result V_{Mx} to the result RCHx.ADRES is as follows:

$V_{Mx} = -V_{FAREF}$	leads to RCHx.ADRES = 0
$V_{Mx} = 0$	leads to RCHx.ADRES = 512
$V_{Mx} = +V_{FAREF}$	leads to RCHx.ADRES = 1023

For single-ended measurements, the following values are taken into account:

- if ENP_x = 0 then $V_{FAINxP} = V_{FAREFM}$
- if ENN_x = 0 then $V_{FAINxN} = V_{FAREFM}$

Note: In Multiplexer Test Mode (GCR.MUXTM = 1), the channel amplifiers are disconnected from the converter stage. The measured conversion result in multiplexer test mode is 512 plus/minus the offset of the converter stage.

32.2.3 Conversion Timing

The conversion time of the FADC is determined by the frequency of clock f_{FADC}. The conversion time including sampling, converting, and storing of the conversion result takes 21 periods of f_{FADC}.

32.2.4 Channel Triggers

As shown **Figure 32-4**, the trigger behavior of an FADC channel x is determined by its channel x trigger control logic. An FADC channel x can be triggered by three trigger sources:

- External trigger source input signal, selectable from an input vector TS[H:A]
- Internal channel x timer trigger signal
- Internal neighbor channel trigger signal

If one of these trigger sources is selected, becomes active, and the gating logic is programmed to enable trigger signals (signal ECHTIMx set), the conversion request flag CRFx becomes set indicating a valid request for FADC channel x.
The gating source input and gating mode selection logic generate an enable signal for channel x timer that determines whether any of the three conversion trigger signal sources is allowed to set the channel x conversion request flag CRFx. It can select an input signal from the input vector GS[H:A].
The control logic does the following tasks, independently in each of the FADC channels:

- Gating source input selection (CFGRx.GSEL)
- Gating mode selection (CFGRx.GM)
- Trigger source input selection (CFGRx.TSEL)
- Trigger mode selection (CFGRx.TM)
- Channel timer request generation
- Conversion request flag set/clear

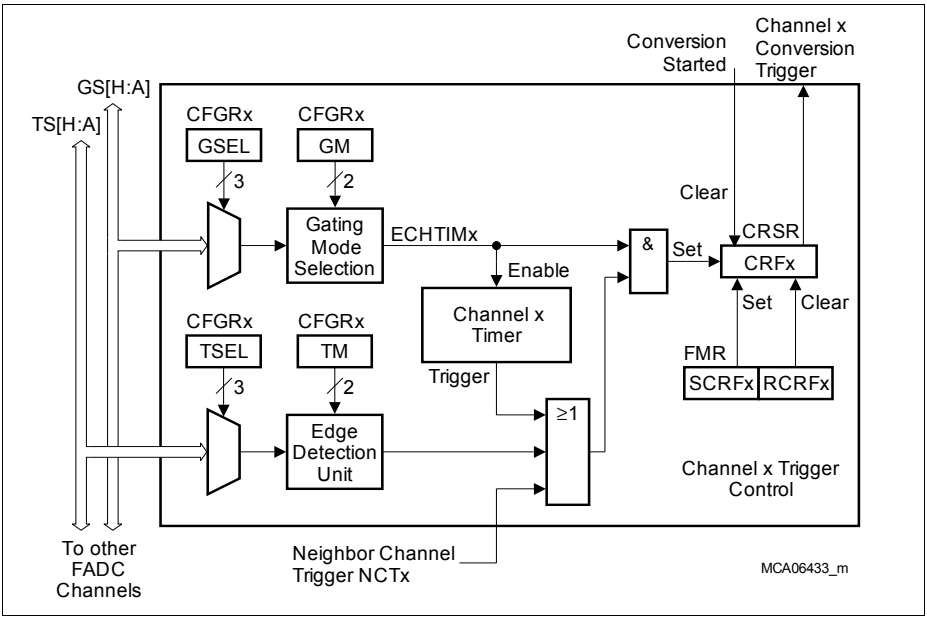


Figure 32-4 Channel Trigger Control Logic

Table 32-1 describes the possible gating modes (enabled, disabled, active gating source input polarity) of an FADC channel.

Table 32-1 Gating Modes

CFGRx.GM	Gating Mode
00_B	Conversion requests are disabled and Channel Timer is stopped. Bit CRSR.CRFx never becomes set (by hardware).
01_B	Conversion requests and Channel Timer are always enabled. Bit CRSR.CRFx becomes set by hardware with each active trigger signal.
10_B	When gating source input GSn = 1 (as selected by CFGRx.GSEL), the Channel Timer is enabled and the conversion request bit CRSR.CRFx becomes set by hardware with each active trigger signal.
11_B	When gating source input GSn = 0 (as selected by CFGRx.GSEL), the Channel Timer is enabled and the conversion request bit CRSR.CRFx becomes set by hardware with each active trigger signal.

An edge detection unit determines which edge of the trigger source input signal (as selected by CFGRx.TSEL) is generating a conversion request trigger signal. Rising, falling or both edges can be selected for trigger signal generation.

Table 32-2 Trigger Modes

CFGRx.TM	Trigger Mode
00_B	No trigger signal generated.
01_B	A conversion request trigger signal is generated on a rising edge of trigger source input TSn (selected by CFGRx.TSEL).
10_B	A conversion request trigger signal is generated on a falling edge of trigger source input TSn (selected by CFGRx.TSEL).
11_B	A conversion request trigger signal is generated on a rising or falling edge of trigger source input TSn (selected by CFGRx.TSEL).

The Conversion Request Flag CRSR.CRFx is cleared by hardware when the conversion of channel x is started. Bit CRFx can be also set or cleared by software via bits in the Flag Modification Register FMR. Writing a 1 to FMR.SCRF sets CRFx. Writing a 1 to FMR.RCRF clears CRFx (independently of FMR.SCRF).

32.2.5 Channel Timer

Each of the FADC channels contains an 8-bit Channel Timer that can be used to generate periodic conversion requests. The Channel Timer is built up by a decrementing counter that is reloaded with a programmable value. When the Channel Timer reaches zero while running, a Channel Timer trigger event is generated and the Channel Timer is reloaded with the reload value CFGRx.CTREL when the requested conversion is started. With the start of the A/D conversion, request bit CRSR.CRFx is cleared. Note that the request flag is set by a timer trigger event only if the gating condition is met (signal ECHTIMx in **Figure 32-4** set).

A clock divider, fed by the module clock f_{FADC} and common for all Channel Timers, generates several clock signals with different periods. Bit field CFGRx.CTF selects whether or not the channel x timer clock f_{CTx} is enabled and, if enabled, determines the frequency of channel x timer input clock f_{CTx}.

While the Channel Timer is disabled (CFGRx.CTM = 00_B) or if the gating condition is not met (gating line ECHTIMx delivers 0), the channel x timer value is set to 04_H. This value ensures a fast conversion trigger after the gating becomes enabled, but prevents unintended conversion starts in case of short pulses (bouncing) at the gating input.

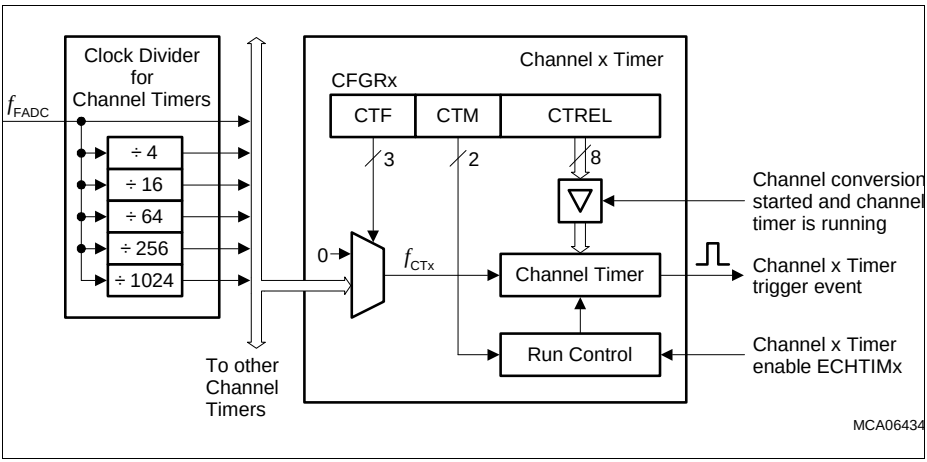


Figure 32-5 Channel Timer Block Diagram

Due to the common divider, the first event at the trigger output of CHTIMx after the start has a maximum jitter of one clock cycle of the selected channel x timer clock f_{CTx}.

A Channel x Timer input clock pulse at f_{CTx} is ignored if it occurs in the f_{FADC} clock cycle directly after the Channel x Timer has reached 0. If there is at least one f_{FADC} clock cycle between two Channel x Timer input clock pulses, all Channel x Timer input clock pulses

are taken into account. This leads to a Channel x Timer reload value (CFGRx.CTREL) whose definition depends on the ratio of f_{FADC} / f_{CTx}:

$f_{FADC} / f_{CTx} = 1$	Channel x timer divide factor = CTREL + 2
$1 < f_{FADC} / f_{CTx} < 2$	Not recommended to be used!
$2 \leq f_{FADC} / f_{CTx}$	Channel x timer divide factor = CTREL + 1

In case of a f_{FADC} / f_{CTx} ratio between 1 and 2, a mixture of both divide factor definitions occurs depending on the divider ratio as programmed by the fractional divider value. Therefore, it is recommended that this ratio should not be used.

32.2.6 Conversion Control

A conversion is started when at least one of the CRSR.CRFx bits is set. A running conversion cannot be aborted and is indicated by the busy flag CRSR.BSYx set. The corresponding bit CRSR.CRFx is reset by hardware when the conversion starts.

32.2.6.1 Static Channel Priority

If more than one conversion request flag CRSR.CRFx (x = 0-3) is set, the channels are converted according to a priority scheme as defined by the bit field GCR.CRPRIO (without respecting the status of the current filter sequences).

Table 32-3 Static Channel Request Priority

Priority	GCR.CRPRIO			
	00_B	01_B	10_B	11_B
High	Channel 0	Channel 1	Channel 2	Channel 3
	Channel 1	Channel 2	Channel 3	Channel 0
	Channel 2	Channel 3	Channel 0	Channel 1
Low	Channel 3	Channel 0	Channel 1	Channel 2

32.2.6.2 Dynamic Priority Assignment

If dynamic priority assignment is enabled (GCR.DPAEN = 1), a channel that has the only active gate signal (signal ECHTIMx in **Figure 32-4**) among the four channels gets the highest priority (GCR.CRPRIO is set to the number of the channel). If more than one channel gating signal is active, GCR.CRPRIO is not changed automatically. In this case, it can be changed by software.

32.2.6.3 Clock Generation

The FADC module is provided with two clock signals: f_{CLC} and f_{FADC}. Clock f_{CLC} is used inside the FADC kernel for control purposes such as clocking of control logic, register operations, trigger detection, or filter calculation.
The clock rate of f_{FADC} is programmable. It is used inside the FADC kernel for the Channel Timers and other internal timings.

32.2.6.4 Suspend Mode Behavior

When a suspend/idle mode request is generated for the FADC module via the fractional divider, a currently running conversion is completely finished (not aborted) and, if selected, a filter calculation still takes place. Thereafter, no new conversion will be started and the state of the FADC module is frozen until the suspend/idle mode request is released again. If enabled, the related interrupts are signaled.
If suspend mode is needed, it is recommended to use to the suspend control by the fractional divider and not by the CLC register.

32.2.6.5 Alias Feature

The alias feature is mainly meant for emulation purposes and does not need to be used in standard applications. It allows a reassignment of the channel to be converted with respect to the channel number that has been requested for conversion. This feature can be used to redirect conversion requests to other input channels without changing the request SW. For example, a SW from TC1766 (with only the two input channels 0 and 1), can be adapted to either channels 0 and 1 (compatibility to older products) or to channels 2 and 3 instead. Especially when emulating several different devices with a common emulation chip, the channel reassignment allows compatible SW usage with different channel wiring to pins.

The setting of the input stages (incl. calibration information) is defined by register ACRx of the input channel that is requested (no alias-mapping). I.e. the ACRx register of the actually converted channel is used as it is permanently conntected to its channel. The result handling (incl. interrupts) also refers to the requested channel number. The alias feature is only taken into account as channel number for the conversion start.

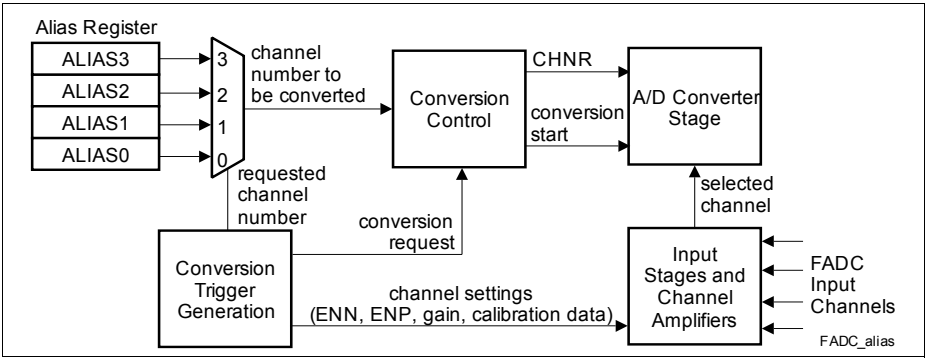


Figure 32-6 Alias Feature

32.2.7 Data Reduction Unit

A Data Reduction Unit is implemented in the FADC that operates as anti-aliasing filter. This unit allows the number of conversion data requests that are issued to the CPU or other bus masters to be reduced by adding multiple conversion results according to a certain algorithm and presenting it to the CPU or other bus masters with a reduced conversion request rate.

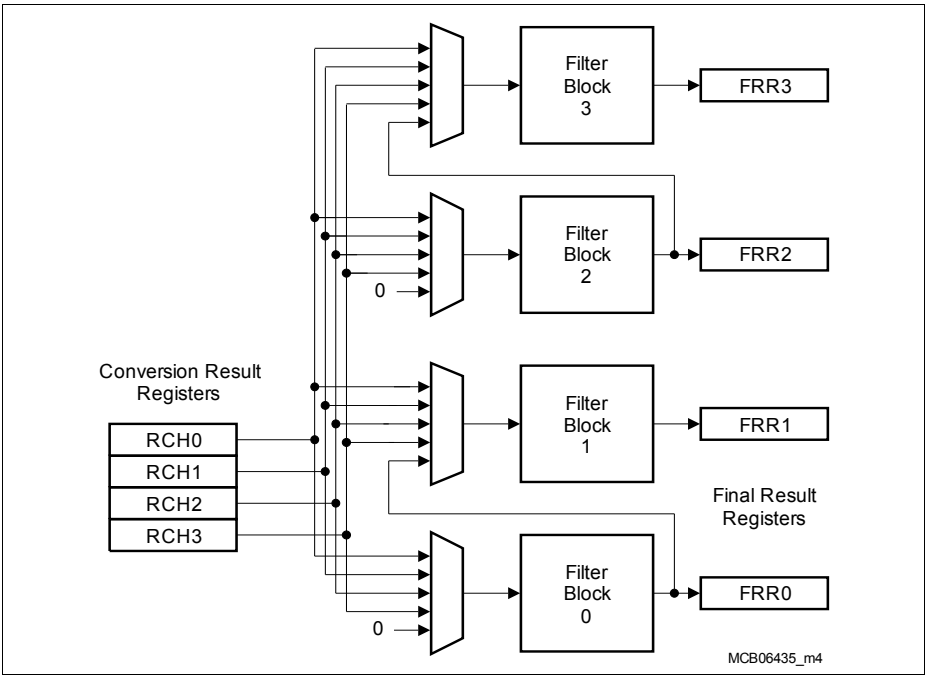


Figure 32-7 TC1798 FADC Filter Blocks

The Data Reduction Unit contains four filter blocks. Each filter block allows selection of its input data source. The input data sources are the conversion result registers of the four A/D converter channels.

Filter blocks can also be concatenated (block 0 and block 1 can be concatenated, same for block 2 and block 3). When the result of a filter operation is stored in one of the final result registers, a service request can be generated. Each filter block basically contains adder logic and intermediate storage registers that allow support for typical digital filter operations such as moving average calculations with intermediate results.

32.2.7.1 Filter Block Structure

The filter block consists of an adder and several result registers for calculating filter output data from the filter input data. For filter n, the Current Result Register CRRn is used for adding up conversion results. After a programmable number of conversion results have been added, the contents of CRRn are stored as intermediate result in the Intermediate Result Register IRR1n. The three intermediate result registers operate like a pipeline. Before IRR1n is overwritten, IRR2n is transferred to IRR3n, and IRR1n is transferred to IRR2n. The Final Result Register FRRn stores the sum that is built by the contents of the current result register and the intermediate result registers.

All result registers of the filter block can be read at any time. Please note that only one intermediate result register is available in filter block 1 (IRR11) and in filter block 3 (IRR13).

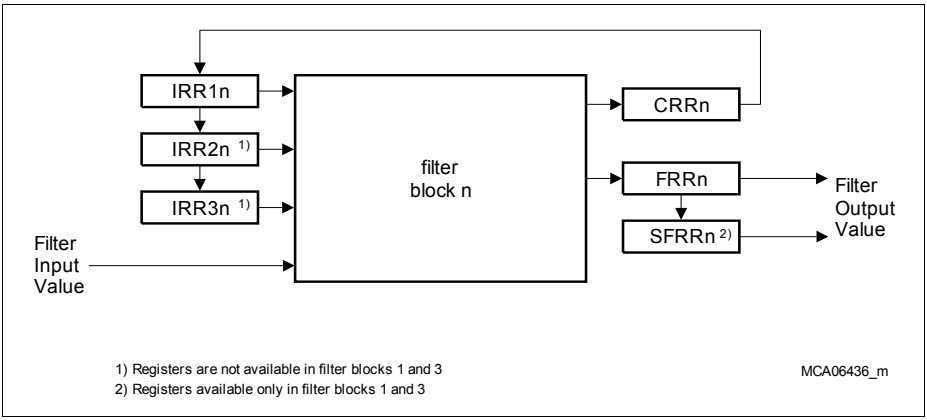


Figure 32-8 Filter Block Structure

32.2.7.2 Filter Block Operation

A filter block can be used for data-reduction or anti-aliasing filtering of the conversion results (n indicates the number of the filter block). It performs a combination of data reduction by adding and a moving average operation.

- A continuous A/D conversion is running on channel x.
- The filter input selection is set to channel x (FCRn.INSEL = 100_B + x).
- The addition length is controlled by FCRn.ADDL defining how many conversion results are added to build one intermediate result (intermediate cycle).

- The moving average length is controlled by FCRn.MAVL defining how many intermediate results are taken into account for a moving average to build the final result (final result cycle).

Intermediate Result Calculation

Each incoming conversion result is added to the content of CRRn until the programmed number of conversion results have been summed up in CRRn. At that point, CRRn contains a new intermediate result and the calculation of the next final result value by moving average is started. Then CRRn is cleared automatically after the final result cycle to be prepared for the first conversion result for the next intermediate cycle.
Before the filter operation of continuous conversion results of channel x is started, the filter block n has to be cleared (writing GCR.RSTFn = 1) after programming the filter control bit fields.

Final Result Calculation

The calculation of a final result is started when an intermediate cycle has been finished. The new intermediate result (stored in CRRn) and the contents of the intermediate registers IRRnx are added to build the final result in FRRn. The number of intermediate results taking part in the moving average operation to build the final result is programmable, the maximum is given by:

- Filter block 0: FRR0 := CRR0 + IRR10 + IRR20 + IRR30
- Filter block 1: FRR1 := CRR1 + IRR11
- Filter block 2: FRR2 := CRR2 + IRR12 + IRR22 + IRR32
- Filter block 3: FRR3 := CRR3 + IRR13

At the end of the final result cycle, the contents of IRR2n are transferred into IRR3n, then the contents of IRR1n into IRR2n, then the contents of CRRn into IRR10 (for filter blocks 0 and 2). The former contents of IRR3n are lost.
Bit field FCRn.MAVL determines the number of intermediate results that are used for the final result calculation. For filter blocks 1 and 3, only two bit combinations are valid and the intermediate result registers IRR2n and 3n are not available and handled as if they were 0.

Each update of a result register FRRn with a new final result value generates a filter block n service request.

32.2.7.3 Filter Concatenation

Filter block 1 and 3 allow filter concatenation to support more filter stages. Filter 1 can be programmed to use the result value of filter 0, similar for filter blocks 2 and 3.

Filter blocks 0 and 2 operate with the following parameters:

- Intermediate results are calculated based on the conversion results of one of the input channels (FCRn.INSEL = $1XX_B$).

- An intermediate cycle can contain a maximum of 8 conversion results.
- A final result cycle can contain a maximum of 4 intermediate results.

Filter blocks 1 and 3 operate with the following parameters:

- Intermediate results are based on the final results of filter block 0 (for filter block 1) and of filter block 2 (for filter block 3). Filter block concatenation is enabled by FCRn.INSEL = 010_B.
- An intermediate cycle can contain a maximum of 8 conversion results.
- A final result cycle can contain a maximum of 2 intermediate results.

32.2.7.4 Width of Result Registers

The additions executed in filter 0 and filter 1 together with the possible maximum values of the filter parameters determine the width of the current, intermediate, and final result registers (same for filter blocks 2 and 3).

In addition to the final result registers FRR1 and FRR3 with 20 bit width, another view is available that is shifted by 5 bit positions to the right, given by registers SFRR1 and SFRR3. This allows a representation of the data within a 16 bit word for further digital data handling.

Table 32-4 Data Width of Result Registers

Register Long Name	Register Short Name	Result Width
Filter 0 Current Result Register	CRR0	13-bit
Filter 0 Intermediate Result Register 1	IRR10	
Filter 0 Intermediate Result Register 2	IRR20	
Filter 0 Intermediate Result Register 3	IRR30	
Filter 0 Final Result Register	FRR0	15-bit
Filter 1 Current Result Register	CRR1	18-bit
Filter 1 Intermediate Result Register 1	IRR11	
Filter 1 Final Result Register	FRR1	20-bit
Filter 1 Shifted Final Result Register	SFRR1	15-bit
Filter 2 Current Result Register	CRR2	13-bit
Filter 2 Intermediate Result Register 1	IRR12	
Filter 2 Intermediate Result Register 2	IRR22	
Filter 2 Intermediate Result Register 3	IRR32	
Filter 2 Final Result Register	FRR2	15-bit
Filter 3 Current Result Register	CRR3	18-bit
Filter 3 Intermediate Result Register 1	IRR13	
Filter 3 Final Result Register	FRR3	20-bit
Filter 3 Shifted Final Result Register	SFRR3	15-bit

32.2.8 Neighbor Channel Trigger

The neighbor channel trigger feature allows the concatenation of channel conversions. This means that the start of a conversion for one channel can generate multiple channel trigger requests for the other three channels. A channel conversion request flag of a neighbor channel becomes only set by a neighbor channel trigger request if the gating condition (gating mode selection output at high level in **Figure 32-4**) in the corresponding neighbor channel is valid.

All neighbor channel trigger enable bits ENxy are located in the Neighbor Channel Trigger Register NCTR. Index “x” indicates the number of the channel that starts a neighbor channel trigger. Index “y” is the number of the neighbor channel to be triggered.

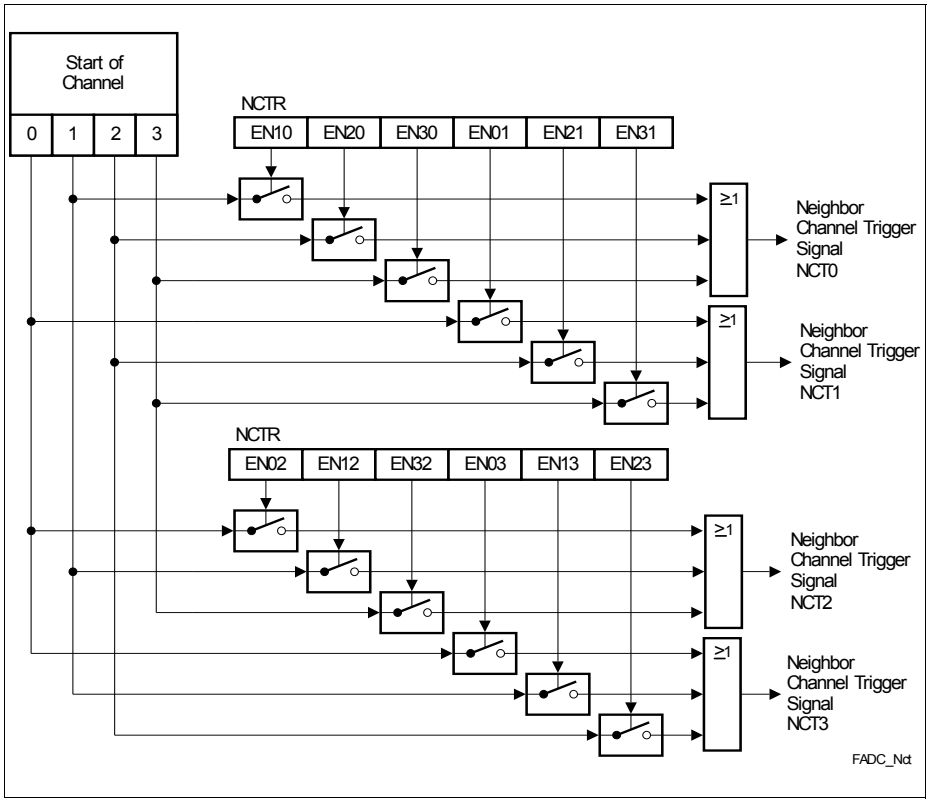


Figure 32-9 Neighbor Channel Trigger

32.2.9 Calibration

The calibration is used to minimize the error of the FADC conversion results independently for each channel. The output of each channel amplifier can be adjusted to deliver a minimum offset value for zero input voltage difference. The channel which is calibrated is selected by GCR.CALCH. The calibration mode is selected by GCR.CALMODE. During the calibration process of a channel, the other channels can be used in normal conversion mode without restrictions.

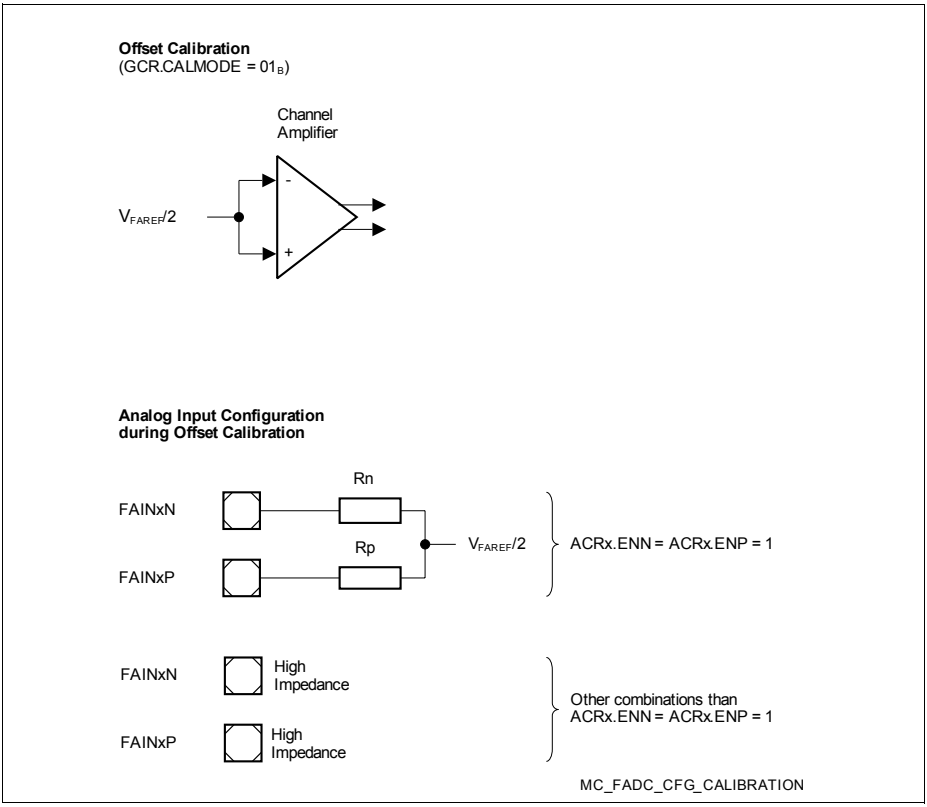


Figure 32-10 Analog Input and Channel Amplifier Configuration at Calibration

Figure 32-10 shows the channel amplifier configuration as well as the analog input pin configurations that are selected during offset and gain calibration. Note that in the calibration modes, the impedance of the analog inputs depends on the settings of the ENN and ENP bits of the corresponding Channel x Analog Control Register ACRx.

32.2.9.1 Offset Calibration

When offset calibration is selected (GCR.CALMODE = 01_B), the channel amplifier inputs of the selected channel are both connected to $V_{FAREF}/2$. After enabling a channel amplifier for offset calibration, a delay of minimum 5 µs must be respected before starting a conversion for this channel. The conversion result must be compared by software with the tolerated offset value (a conversion result with zero offset is equal to 512). If the conversion result exceeds the tolerated range, bit field ACRx.CALOFF (with x specifying the calibrated channel) can be adjusted and a new conversion can be started. The calibration process is finished when the conversion result is in the tolerated offset range. After switching back to normal mode for channel x, a delay of minimum 5 µs must be respected before starting a new conversion for this channel.

32.2.10 Interrupt Generation

A flexible service request control structure is implemented in the FADC. The FADC provides the channel conversion request sources and the filter block request sources, that can be programmed to generate one of four service request output signals SR[3:0]. The service request compressor also makes it possible to assign more than one service request source to one service request output.

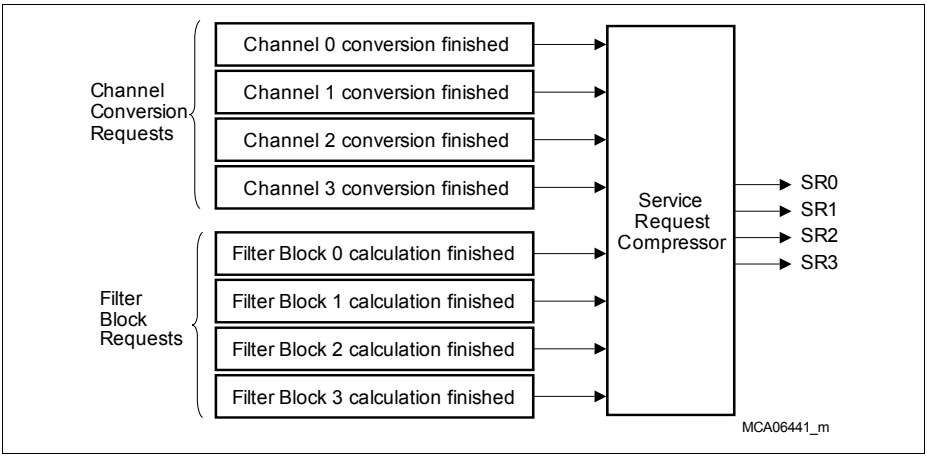


Figure 32-11 Service Request Configuration

All service requests are controlled by an identical control logic. This control logic as shown in **Figure 32-12** provides the following functionality:

- Service Request Flag
- Set/Clear Request Flag Control Bits
- Service Request Enable Bit
- Service Request Node Pointer

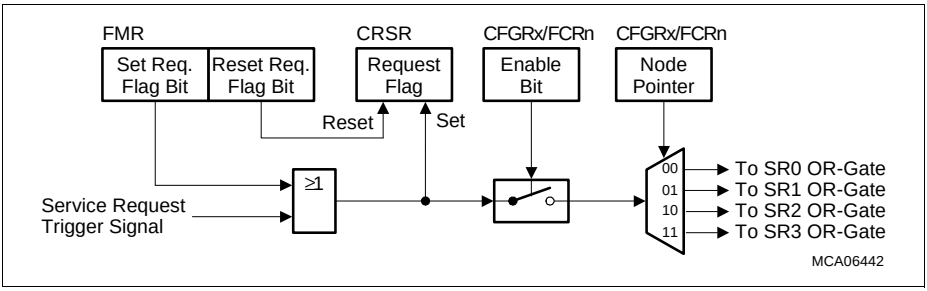


Figure 32-12 Service Request Control Logic

The request flag is always set by hardware when the corresponding request event occurs. It can also be set or cleared by software when writing a 1 to the corresponding set/clear request flag bit in the Flag Modification Register FMR. Finally, a service request event is directed to one of the four service request output lines SR[3:0] when the corresponding service request enable bit IEN is set. The service request node pointer determines which of the service request output lines SR[3:0] becomes activated.

Table 32-5 lists the six service request sources of the FADC Module with its related control and status flags/bits.

Table 32-5 Service Request Control/Status Bits/Flags

Service Request Source	Request Flag	Enable Bit	Set Request Bit / Clear Request Bit	Service Request Node Pointer
Channel x Conversion Request (x = 0-3)	CRSR.IRQx	CFGRx.IEN	FMR.SIRQx / FMR.RIRQx	CFGRx.INP
Filter Block n Request (n = 0-3)	CRSR.IRQFn	FCRn.IEN	FMR.SIRQFn / FMR.RIRQFn	FCRn.INP

In the service request compressor logic shown in **Figure 32-13**, the inputs of one SRx OR-gate are connected to all demultiplexer outputs with identical INP node pointer value. Therefore, one service request event can be only assigned to one of the four service request outputs, but one service request output can be used by multiple service request events.

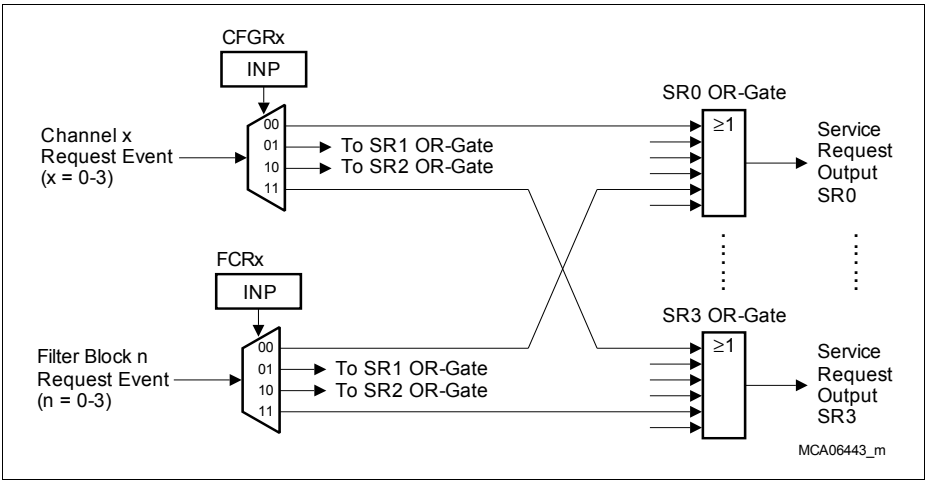


Figure 32-13 Service Request Compressor Logic

Depending on the implementation of the FADC Module in a specific micro controller, the service request output signals SR[3:0] can either be connected to an interrupt node (controlled by a service request control register) or can be used as DMA request input of a DMA controller unit. The TC1798 specific request output connections are described in the FADC implementation chapter.

32.3 FADC Register Description

This section describes the kernel registers of the FADC module. All FADC kernel register names described in this section will be referenced in other parts of the TC1798 User´s Manual by the module name prefix “FADC_”.

All registers can accessed with 8-bit, 16-bit, or 32-bit read or write operations.

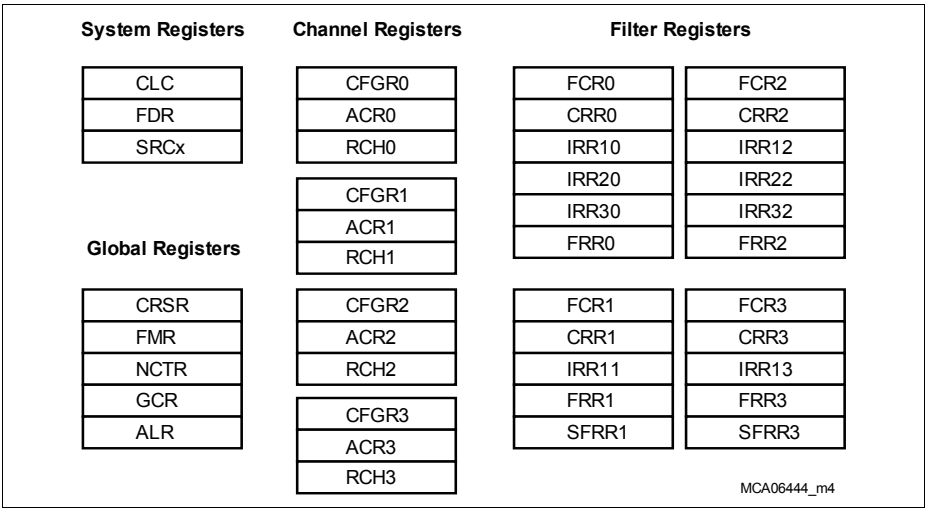


Figure 32-14 FADC Kernel Registers

Access rights within the address range of an FADC kernel:

- Read access to defined register addresses: U, SV
- Write access to defined register addresses: U, SV
- Accesses to empty addresses: reserved, BE

Table 32-6 Register Overview of FADC

Short Name	Description	Offset Addr.[1)]	Access Mode		Reset	Description See
			Read	Write		
FADC Module Registers						
CLC	Clock Control Register	000_H	U, SV	SV, E	Class 3	Page 32-30
FDR	Fractional Divider Register	$00C_H$	U, SV	SV, E	Class 3	Page 32-31

Table 32-6 Register Overview of FADC

Short Name	Description	Offset Addr.[1]	Access Mode		Reset	Description See
			Read	Write		
ID	Module Identification Register	008_H	U, SV	U, SV	Class 3	Page 32-33
SRCx x = 0 - 3	Service Request Control Registers	$0FC_H$ - x * 4_H	U, SV	U, SV	Class 3	Page 32-34
Global Registers						
CRSR	Conversion Request Status Register	010_H	U, SV	U, SV	Class 3	Page 32-35
FMR	Flag Modification Register	014_H	U, SV	U, SV	Class 3	Page 32-37
NCTR	Neighbor Channel Trigger Register	018_H	U, SV	U, SV	Class 3	Page 32-39
GCR	Global Control Register	$01C_H$	U, SV	U, SV	Class 3	Page 32-42
reserved	no BE, has to be written with 0	050_H				
ALR	Alias Register	054_H	U, SV	SV, E	Class 3	Page 32-46
Channel Registers						
CFGRx	Channel x Configuration Register (x = 0-3)	020_H + (x × 4)	U, SV	U, SV	Class 3	Page 32-48
ACRx	Channel x Analog Control Reg. (x = 0-3)	030_H + (x × 4)	U, SV	U, SV	Class 3	Page 32-52
RCHx	Channel x Conversion Result Register (x = 0-3)	040_H + (x × 4)	U, SV	U, SV	Class 3	Page 32-54
Filter 0 Registers						
FCR0	Filter 0 Control Register	060_H	U, SV	U, SV	Class 3	Page 32-55
CRR0	Filter 0 Current Result Register	064_H	U, SV	U, SV	Class 3	Page 32-58

Table 32-6 Register Overview of FADC

Short Name	Description	Offset Addr.[1]	Access Mode		Reset	Description See
			Read	Write		
IRR10	Filter 0 Intermediate Result Register 1	068_H	U, SV	U, SV	Class 3	Page 32-60
IRR20	Filter 0 Intermediate Result Register 2	$06C_H$	U, SV	U, SV	Class 3	Page 32-60
IRR30	Filter 0 Intermediate Result Register 3	070_H	U, SV	U, SV	Class 3	Page 32-60
FRR0	Filter 0 Final Result Register	074_H	U, SV	U, SV	Class 3	Page 32-62
Filter 1 Registers						
FCR1	Filter 1 Control Register	080_H	U, SV	U, SV	Class 3	Page 32-55
CRR1	Filter 1 Current Result Register	084_H	U, SV	U, SV	Class 3	Page 32-58
IRR11	Filter 1 Intermediate Result Register 1	088_H	U, SV	U, SV	Class 3	Page 32-60
FRR1	Filter 1 Final Result Register	094_H	U, SV	U, SV	Class 3	Page 32-62
SFRR1	Filter 1 Shifted Final Result Register	098_H	U, SV	U, SV	Class 3	Page 32-63
Filter 2 Registers						
FCR2	Filter 2 Control Register	$0A0_H$	U, SV	U, SV	Class 3	Page 32-55
CRR2	Filter 2 Current Result Register	$0A4_H$	U, SV	U, SV	Class 3	Page 32-58
IRR12	Filter 2 Intermediate Result Register 1	$0A8_H$	U, SV	U, SV	Class 3	Page 32-60
IRR22	Filter 2 Intermediate Result Register 2	$0AC_H$	U, SV	U, SV	Class 3	Page 32-60
IRR32	Filter 2 Intermediate Result Register 3	$0B0_H$	U, SV	U, SV	Class 3	Page 32-60

Table 32-6 Register Overview of FADC

Short Name	Description	Offset Addr.[1]	Access Mode		Reset	Description See
			Read	Write		
FRR2	Filter 2 Final Result Register	$0B4_H$	U, SV	U, SV	Class 3	Page 32-62
Filter 3 Registers						
FCR3	Filter 3 Control Register	$0C0_H$	U, SV	U, SV	Class 3	Page 32-55
CRR3	Filter 3 Current Result Register	$0C4_H$	U, SV	U, SV	Class 3	Page 32-58
IRR13	Filter 3 Intermediate Result Register 1	$0C8_H$	U, SV	U, SV	Class 3	Page 32-60
FRR3	Filter 3 Final Result Register	$0D4_H$	U, SV	U, SV	Class 3	Page 32-62
SFRR3	Filter 3 Shifted Final Result Register	$0D8_H$	U, SV	U, SV	Class 3	Page 32-63

1) The absolute register address is calculated as follows:
Module Base Address + Offset Address (shown in this column)

32.3.1 System Registers

32.3.1.1 Clock Control Register

The Clock Control Register allows the programmer to control (enable/disable) the clock signal f_{CLC} under certain conditions. After a reset operation, the FADC module is disabled and its module clock signal f_{CLC} is switched off.

CLC
Clock Control Register (000_H) Reset Value: 0000 0003$_H$

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

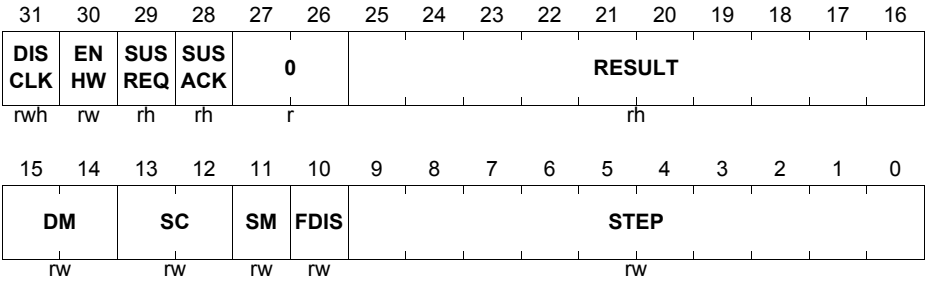
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0										FSOE	SBWE	EDIS	SPEN	DISS	DISR

Field	Bits	Type	Description
DISR	0	rw	**Module Disable Request Bit** Used for enable/disable control of the module.
DISS	1	r	**Module Disable Status Bit** Bit indicates the current status of the module.
SPEN	2	rw	**Module Suspend Enable for OCDS** Used to enable the suspend mode.
EDIS	3	rw	**Sleep Mode Enable Control** Used to control module's sleep mode.
SBWE	4	w	**Module Suspend Bit Write Enable for OCDS** Determines whether SPEN and FSOE are write-protected.
FSOE	5	rw	**Fast Switch Off Enable** Used for fast clock switch off in Suspend Mode.
0	[31:6]	r	**Reserved** Read as 0. Should be written with 0.

32.3.1.2 Fractional Divider Register

The Fractional Divider Register allows the programmer to control the clock rate of the module clock f_{FADC}.

FDR
Fractional Divider Register **($00C_H$)** **Reset Value: $0000\ 0000_H$**



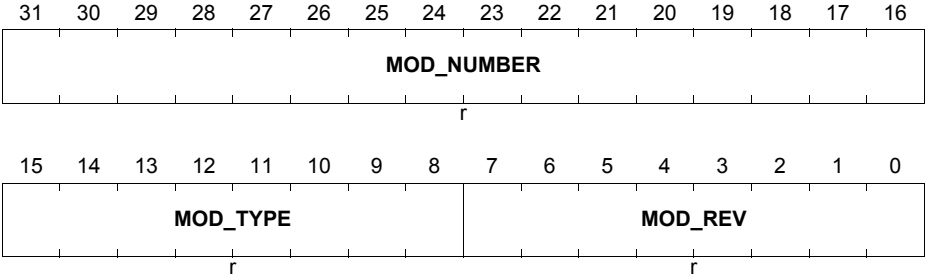
Field	Bits	Type	Description
STEP	[9:0]	rw	**Step Value** Reload or addition value for RESULT.
FDIS	10	rw	**Freeze Disable** This bit controls the freeze function for this module. 0_B Module operates on corrected clock, with reduced modulation jitter 1_B Module operates on uncorrected clock with full modulation jitter
SM	11	rw	**Suspend Mode** SM selects between granted or immediate suspend mode.
SC	[13:12]	rw	**Suspend Control** This bit field determines the behavior of the fractional divider in suspend mode.
DM	[15:14]	rw	**Divider Mode** This bit field selects normal divider mode, fractional divider mode, and off-state.
RESULT	[25:16]	rh	**Result Value** Bit field for the addition result.
SUSACK	28	rh	**Suspend Mode Acknowledge** Indicates state of SPNDACK signal.

Field	Bits	Type	Description
SUSREQ	29	rh	**Suspend Mode Request** Indicates state of SPND signal.
ENHW	30	rw	**Enable Hardware Clock Control** Controls operation of ECEN input and DISCLK bit. Should be always written with 0.
DISCLK	31	rwh	**Disable Clock** Hardware controlled disable for f_{FADC} signal.
0	10, [27:26]	r	**Reserved** Read as 0. Should be written with 0.

32.3.1.3 Module Identification Register

The register table can be found on **Page 32-26**.

ID
Module Identification Register **(008_H)** **Reset Value: $0027\ C000_H$**



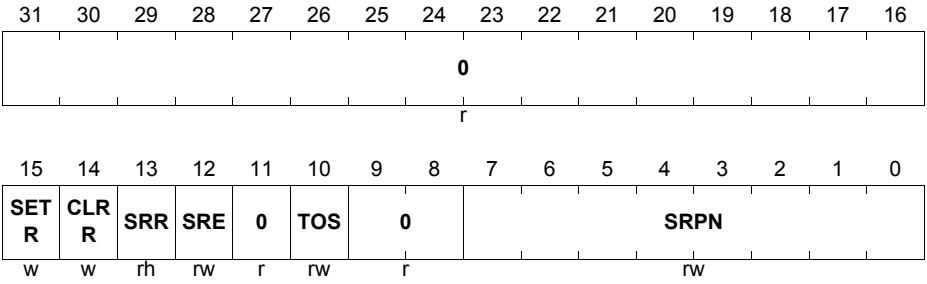
Field	Bits	Type	Description
MOD_REV	[7:0]	r	**Module Revision** This bit field indicates the revision number of the module implementation (depending on the design step). The given value of 00_H is a placeholder for the actual number. Bits [3:0] refer to the version of the digital part and bits [7:4] indicate the version of the analog part (anid).
MOD_TYPE	[15:8]	r	**Module Type**
MOD_NUMBER	[31:16]	r	**Module Number**

32.3.1.4 Service Request Control Registers

Each of the interrupts of the FADC is controlled by a service request control register.

SRCx (x = 0-3)
Service Request Control Register x

($0FC_H$ - x*4_H) **Reset Value: $0000\ 0000_H$**



Field	Bits	Type	Description
SRPN	[7:0]	rw	**Service Request Priority Number**
TOS	10	rw	**Type of Service Control**
SRE	12	rw	**Service Request Enable**
SRR	13	rh	**Service Request Flag**
CLRR	14	w	**Request Clear Bit**
SETR	15	w	**Request Set Bit**
0	[9:8], 11, [31:16]	r	**Reserved** Read as 0. Should be written with 0.

32.3.2 Global Registers

32.3.2.1 Conversion Request Status Register

The Conversion Request Status Register CRSR contains the flags for monitoring the state of pending conversions and the interrupt request flags.

CRSR
Conversion Request Status Register (010_H) **Reset Value: $0000\ 0000_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0								IRQF3	IRQF2	IRQF1	IRQF0	IRQ3	IRQ2	IRQ1	IRQ0
r								rh	rh	rh	rh	rh	rh	rh	rh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0				BSY3	BSY2	BSY1	BSY0	0				CRF3	CRF2	CRF1	CRF0
r				rh	rh	rh	rh	r				rh	rh	rh	rh

Field	Bits	Type	Description
CRFx (x = 0-3)	x	rh	**Conversion Request Flag** This bit monitors whether a conversion request is pending for channel x. CRFx is set by hardware when a trigger event is detected while the gating condition delivers 1. CRFx is automatically cleared by hardware when a conversion of the channel x is started. 0_B A conversion of channel x has not been requested. 1_B A conversion of channel x has been requested. Bits CRFx can be set/cleared by software via bits FMR.RCRFx and FMR.SCRFx. If a set and a clear condition for CRFx occur simultaneously (generated by hardware and/or software), the clear condition always wins.

Field	Bits	Type	Description
BSYx (x = 0-3)	8 + x	rh	**Busy Flag** This bit indicates if a conversion is currently running for channel x. 0_B A conversion is not running. 1_B A conversion is running.
IRQx (x = 0-3)	16 + x	rh	**Interrupt Request Flag** This bit indicates that a conversion of channel x has been finished since it has been cleared by software. Interrupt requests can also be generated while IRQx is still set. An interrupt can only be generated when CFGRx.IEN = 1. 0_B A conversion has not been finished. 1_B A conversion has been finished. Bits IRQx can be set/cleared by software via bits FMR.SIRQx and FMR.RIRQx.
IRQFn (n = 0-3)	20 + n	rh	**Interrupt Request Flag for Filter n** This bit indicates that a filter sequence of filter n has been finished (new final result is available) since it has been cleared by software. Interrupt requests can also be generated while IRQ is still set. An interrupt can only be generated when FCRn.IEN = 1. 0_B A filter sequence has not been finished. 1_B A filter sequence has been finished. Bits IRQFn can be set/cleared by software via bits FMR.SIRQFn and FMR.RIRQFn.
0	[7:4], [15:12], 24[31:24]	r	**Reserved** Read as 0. Should be written with 0.

32.3.2.2 Flag Modification Register

The bits of the Flag Modification Register FMR allow the flags of the conversion request status register to be set/cleared by software.
If a clear and set request are issued at the same time, the target flag is cleared. It is recommended to avoid writing both bit positions (for set and for clear) of the same target bit with 1 within the same write operation.

FMR
Flag Modification Register **(014_H)** **Reset Value: 0000 0000$_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
S IRQ F3	S IRQ F2	S IRQ F1	S IRQ F0	S IRQ 3	S IRQ 2	S IRQ 1	S IRQ 0	R IRQ F3	R IRQ F2	R IRQ F1	R IRQ F0	R IRQ 3	R IRQ 2	R IRQ 1	R IRQ 0
w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0				S CRF 3	S CRF 2	S CRF 1	S CRF 0	0				R CRF 3	R CRF 2	R CRF 1	R CRF 0
r				w	w	w	w	r				w	w	w	w

Field	Bits	Type	Description
RCRFx (x = 0-3)	x	w	**Clear Conversion Request Flag** This bit allows bit CRSR.CRFx to be cleared by software. 0_B No operation 1_B Bit CRSR.CRFx is cleared.
SCRFx (x = 0-3)	8 + x	w	**Set Conversion Request Flag** This bit allows bit CRSR.CRFx to be set by software. 0_B No operation 1_B Bit CRSR.CRFx is set.
RIRQx (x = 0-3)	16 + x	w	**Clear Interrupt Request Flag** This bit allows bit CRSR.IRQx to be cleared by software. 0_B No operation 1_B Bit CRSR.IRQx is cleared.

Field	Bits	Type	Description
RIRQFn (n = 0-3)	20 + n	w	**Clear Interrupt Request Flag for Filter n** This bit allows bit CRSR.IRQFn to be cleared by software. 0_B No operation 1_B Bit CRSR.IRQFn is cleared.
SIRQx (x = 0-3)	24 + x	w	**Set Interrupt Request Flag** This bit allows bit CRSR.IRQx to be set by software. 0_B No operation 1_B Bit CRSR.IRQx is set and an interrupt is generated if CFGRx.IEN = 1.
SIRQFn (n = 0-3)	28 + n	w	**Set Interrupt Request Flag for Filter n** This bit allows bit CRSR.IRQFn to be set by software. 0_B No operation 1_B Bit CRSR.IRQFn is set and an interrupt is generated if FCRn.IEN = 1.
0	[7:4], [15:12]1 212121 2	r	**Reserved** Read as 0. Should be written with 0.

32.3.2.3 Neighbor Channel Trigger Register

The Neighbor Channel Trigger Register NCTR contains the enable bits for the neighbor channel trigger signal (NCTx) generation (see Page 32-20).

NCTR

Neighbor Channel Trigger Register (018_H) **Reset Value: $0000\ 0000_H$**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0					EN32	EN31	EN30	0				EN23	0	EN21	EN20
r					rw	rw	rw	r							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0				EN13	EN12	0	EN10	0				EN03	EN02	EN01	0
r							rw	r						rw	r

Field	Bits	Type	Description
EN01	1	rw	**Enable Neighbor Channel Trigger 01** This bit enables the neighbor channel trigger for channel 1 when a conversion of channel 0 is started. 0_B No action. 1_B A trigger will be generated.
EN02	2	rw	**Enable Neighbor Channel Trigger 02** This bit enables the neighbor channel trigger for channel 2 when a conversion of channel 0 is started. 0_B No action. 1_B A trigger will be generated.
EN03	3	rw	**Enable Neighbor Channel Trigger 03** This bit enables the neighbor channel trigger for channel 3 when a conversion of channel 0 is started. 0_B No action. 1_B A trigger will be generated.
EN10	8	rw	**Enable Neighbor Channel Trigger 10** This bit enables the neighbor channel trigger for channel 0 when a conversion of channel 1 is started. 0_B No action. 1_B A trigger will be generated.

Field	Bits	Type	Description
EN12	10	rw	**Enable Neighbor Channel Trigger 12** This bit enables the neighbor channel trigger for channel 2 when a conversion of channel 1 is started. 0_B No action. 1_B A trigger will be generated.
EN13	11	rw	**Enable Neighbor Channel Trigger 13** This bit enables the neighbor channel trigger for channel 3 when a conversion of channel 1 is started. 0_B No action. 1_B A trigger will be generated.
EN20	16	rw	**Enable Neighbor Channel Trigger 20** This bit enables the neighbor channel trigger for channel 0 when a conversion of channel 2 is started. 0_B No action. 1_B A trigger will be generated.
EN21	17	rw	**Enable Neighbor Channel Trigger 21** This bit enables the neighbor channel trigger for channel 1 when a conversion of channel 2 is started. 0_B No action. 1_B A trigger will be generated.
EN23	19	rw	**Enable Neighbor Channel Trigger 23** This bit enables the neighbor channel trigger for channel 3 when a conversion of channel 2 is started. 0_B No action. 1_B A trigger will be generated.
EN30	24	rw	**Enable Neighbor Channel Trigger 30** This bit enables the neighbor channel trigger for channel 0 when a conversion of channel 3 is started. 0_B No action. 1_B A trigger will be generated.
EN31	25	rw	**Enable Neighbor Channel Trigger 31** This bit enables the neighbor channel trigger for channel 1 when a conversion of channel 3 is started. 0_B No action. 1_B A trigger will be generated.

Field	Bits	Type	Description
EN32	26	rw	**Enable Neighbor Channel Trigger 32** This bit enables the neighbor channel trigger for channel 2 when a conversion of channel 3 is started. 0_B No action. 1_B A trigger will be generated.
0	0, [7:4], 9, [15:12], 18, [23:20], [31:27]	r	**Reserved** Read as 0. Should be written with 0.

Note: The hardware does not check whether the enable bits are set in such a way as to describe a loop of conversion requests (e.g. 0 triggers 2, 2 triggers 3 and 3 triggers 0, etc.). It is in the responsibility of the user to set these bits in an appropriate way.

32.3.2.4 Global Control Register

The Global Control Register GCR contains bits used to reset the Channel Timers, the filters and to control global FADC settings.

GCR
Global Control Register **($01C_H$)** **Reset Value: 0000 0000_H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0				CALCH		CALMODE		0		ANON	MUXTM	RESWEN	DPAEN	CRPRIO	
r				rw		rw		r		rw	rw	rw	rw	rwh	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0			RSTF3	RSTF2	RSTF1	RSTF0	RCD	0				RCT3	RCT2	RCT1	RCT0
r			w	w	w	w	w	r				w	w	w	w

Field	Bits	Type	Description
RCTx (x = 0-3)	x	w	**Reload Channel Timer** 0_B Channel x Timer will not be changed. 1_B Channel x Timer will be loaded with its reload value.
RCD	8	w	**Reset Common Divider** 0_B The common divider will not be changed. 1_B The common divider will be cleared.
RSTFn (n = 0-3)	9 + n	w	**Reset Filter n** 0_B The contents of filter n will not be changed. 1_B The contents of filter n will be cleared. The values of the bits in the filter registers will be cleared, except bit field CRRn.AC that is loaded with the value of FCRn.ADDL.

Field	Bits	Type	Description
CRPRIO	[17:16]	rwh	**Conversion Request Priority** This bit field determines the priority of the conversion requests if more than one channel is requested. If the dynamic priority assignment is enabled, the priority is automatically changed as a function of the gating inputs. The priority of the channels is: 00_B Channel 0 before channel 1 before channel 2 before channel 3 01_B Channel 1 before channel 2 before channel 3 before channel 0 10_B Channel 2 before channel 3 before channel 0 before channel 1 11_B Channel 3 before channel 0 before channel 1 before channel 2
DPAEN	18	rw	**Dynamic Priority Assignment Enable** If the dynamic priority assignment is enabled, the priority bit field CRPRIO is automatically changed as a function of the gating input signals. In this case, the channel that is active while the other three channels are not active gets the highest priority. 0_B The dynamic priority assignment is disabled. 1_B The dynamic priority assignment is enabled.
RESWEN	19	rw	**Result Write Enable** This bit enables a write action to the result registers RCHx (x = 0-3) of the FADC. 0_B Write accesses to the result registers are not taken into account. The written data is discarded. 1_B Write accesses to the result registers are taken into account. The former value of the written result register is overwritten by the write data. If a filter is sensitive to the written result register, the written value is taken as new filter input value.

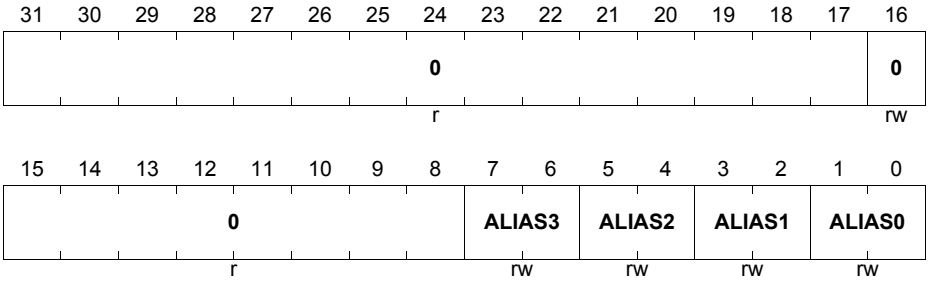
Field	Bits	Type	Description
MUXTM	20	rw	**Multiplexer Test Mode** The input multiplexer to select a channel for the conversion can be tested by opening all multiplexer inputs. In multiplexer test mode, the channel amplifiers are not connected to the converter stage. 0_B The multiplexer test mode is disabled. 1_B The multiplexer test mode is enabled.
ANON	21	rw	**Analog Part ON** This bit enables the analog part of the FADC. This bit must be set to convert the analog input signal to a digital value. 0_B The complete analog part is in power-down mode, the amplifiers and comparators are switched off. Conversions are not possible. 1_B The analog part is enabled.
CALMODE	[25:24]	rw	**Calibration Mode** This bit field enables the calibration for offset and gain for the channel selected by CALCH. 00_B No calibration process is running. All channels are in normal mode (default after reset). 01_B The analog channel selected by CALCH is in offset calibration mode. The other channels are in normal mode. 10_B Reserved 11_B Reserved
CALCH	[27:26]	rw	**Calibration Channel** This bit field selects the channel for the calibration process determined by CALMODE. The setting of CALCH is only taken into account while a calibration process is running. 00_B The analog input channel 0 is selected for a calibration process. 01_B The analog input channel 1 is selected for a calibration process. 10_B The analog input channel 2 is selected for a calibration process. 11_B The analog input channel 3 is selected for a calibration process.

Field	Bits	Type	Description
0	[7:4], [15:13], [23:22], [31:28]	r	**Reserved** Read as 0. Should be written with 0.

32.3.2.5 Alias Register

The Alias Register contains bit fields allowing a re-assignment of the requested channel number to the actually converted channel.

ALR
Alias Register **(054_H)** **Reset Value: 0000 00E4$_H$**



Field	Bits	Type	Description
ALIAS0	[1:0]	rw	**Alias of Channel 0** This bit field defines which channel is converted if a trigger for channel 0 occurs. 00_B Channel 0 will be converted (default). 01_B Channel 1 will be converted. 10_B Channel 2 will be converted. 11_B Channel 3 will be converted.
ALIAS1	[3:2]	rw	**Alias of Channel 1** This bit field defines which channel is converted if a trigger for channel 1 occurs. 00_B Channel 0 will be converted. 01_B Channel 1 will be converted (default). 10_B Channel 2 will be converted. 11_B Channel 3 will be converted.
ALIAS2	[5:4]	rw	**Alias of Channel 2** This bit field defines which channel is converted if a trigger for channel 2 occurs. 00_B Channel 0 will be converted. 01_B Channel 1 will be converted. 10_B Channel 2 will be converted (default). 11_B Channel 3 will be converted.

Field	Bits	Type	Description
ALIAS3	[7:6]	rw	**Alias of Channel 3** This bit field defines which channel is converted if a trigger for channel 3 occurs. 00_B Channel 0 will be converted. 01_B Channel 1 will be converted. 10_B Channel 2 will be converted. 11_B Channel 3 will be converted (default).
0	16	rw	**Placeholder Bit** This bit position is a placeholder for further extensions and should be written with 0.
0	[31:17], [15:8]	r	**Reserved** Read as 0. Should be written with 0.

32.3.3 Channel Registers

32.3.3.1 Channel Configuration Registers

The Channel x Configuration Register CFGRx contains the bits for the selection of the trigger source, the gating source, and other channel settings of channel x.

CFGRx (x = 0-3)
Channel x Configuration Register (020_H+x*4_H) **Reset Value: 0000 0000_H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
IEN	0	INP		0				CTREL							
rw	r	rw		r				rw							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	CTF			CTM		TM		GM		TSEL			GSEL		
r	rw			rw		rw		rw		rw			rw		

Field	Bits	Type	Description
GSEL	[2:0]	rw	**Gating Selection** This bit field selects the gating source input signal for channel x. 000_B Gating source input signal GSA selected 001_B Gating source input signal GSB selected 010_B Gating source input signal GSC selected 011_B Gating source input signal GSD selected 100_B Gating source input signal GSE selected 101_B Gating source input signal GSF selected 110_B Gating source input signal GSG selected 111_B Gating source input signal GSH selected

Field	Bits	Type	Description
TSEL	[5:3]	rw	**Trigger Selection** This bit field selects the trigger source input signal for channel x. 000_B Trigger source input signal TSA selected 001_B Trigger source input signal TSB selected 010_B Trigger source input signal TSC selected 011_B Trigger source input signal TSD selected 100_B Trigger source input signal TSE selected 101_B Trigger source input signal TSF selected 110_B Trigger source input signal TSG selected 111_B Trigger source input signal TSH selected
GM	[7:6]	rw	**Gating Mode** This bit field determines the functionality of the gating (enable) signal. It determines whether and under which condition the generation of conversion requests by trigger signals is possible. 00_B Conversion requests are disabled and the Channel Timer is stopped. CRFx never becomes set (by hardware). 01_B Conversion requests and the Channel Timer are always enabled. CRFx becomes set by hardware with each active trigger signal. 10_B Conversion requests and the Channel Timer are enabled only if the gating source input (as selected by CFGRx.GSEL) is at high level. 11_B Conversion requests and the Channel Timer are enabled only if the gating source input (as selected by CFGRx.GSEL) is at low level.

Field	Bits	Type	Description
TM	[9:8]	rw	**Trigger Mode** This bit field enables the triggering and determines the edge of the trigger source input signal that generates a conversion trigger signal. 00_B No conversion trigger signals are generated. Edge detection unit is switched off. 01_B A conversion request is generated (if gating enabled) on a rising edge of a trigger source input (as selected by CFGRx.TSEL). 10_B A conversion request is generated (if gating enabled) on a falling edge of a trigger source input (as selected by CFGRx.TSEL). 11_B A conversion request is generated (if gating enabled) on both, rising and falling, edges of a trigger source input (as selected by CFGRx.TSEL).
CTM	[11:10]	rw	**Channel Timer Mode** This bit determines the operating mode of channel x timer. 00_B Channel x timer is switched off. 01_B Channel timer is permanently running. 10_B Channel timer is running only if ECHTIMx = 1. 11_B Reserved A Channel Timer trigger event is generated each time the channel x timer value reaches 00_H. While the Channel Timer is not running (CTM = 00_B or signal ECHTIMx = 0), the Channel Timer is loaded with 04_H.
CTF	[14:12]	rw	**Channel Timer Frequency** This bit field controls the channel x timer input clock f_{CT} (enable control and frequency selection). 000_B f_{CTx} is disabled. 001_B f_{CTx} is enabled with frequency f_{FADC}. 010_B f_{CTx} is enabled with frequency f_{FADC} / 4. 011_B f_{CTx} is enabled with frequency f_{FADC} / 16. 100_B f_{CTx} is enabled with frequency f_{FADC} / 64. 101_B f_{CTx} is enabled with frequency f_{FADC} / 256. 110_B f_{CTx} is enabled with frequency f_{FADC} / 1024. 111_B Reserved; do not use this combination.

Field	Bits	Type	Description
CTREL	[23:16]	rw	**Channel Timer Reload Value** This bit field determines the reload value of the Channel Timer CHTIMx, see **Section 32.2.5**. If CTREL = 0, no trigger event is generated.
INP	[29:28]	rw	**Interrupt Node Pointer** This bit field selects which service request output line will be activated when a conversion of channel x is finished while CFGRx.IEN is set. 00_B Service request output SR0 is selected. 01_B Service request output SR1 is selected. 10_B Service request output SR2 is selected. 11_B Service request output SR3 is selected.
IEN	31	rw	**Interrupt Enable** This bit enables the generation of a service request when a conversion of channel x is finished. 0_B Channel x conversion service request generation is disabled. 1_B Channel x conversion service request generation is enabled.
0	15, [27:24], 30	r	**Reserved** Read as 0. Should be written with 0.

32.3.3.2 Analog Control Registers

The Channel x Analog Control Register ACRx contains the bits that control the analog input stage.

ACRx (x = 0-3)
Channel x Analog Control Register

(030_H+x*4_H) **Reset Value: 0000 0000_H**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0															
r															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0		CALOFF3	0	CALOFF[2:0]			0				ENN	ENP	GAIN	
r	rw		rw	r	rw			r				rw	rw	rw	

Field	Bits	Type	Description
GAIN	[1:0]	rw	**Amplifier Gain** This bit field determines the amplifier gain for channel x. 00_B The selected amplifier gain is 1. 01_B The selected amplifier gain is 2. 10_B The selected amplifier gain is 4. 11_B The selected amplifier gain is 8.
ENP	2	rw	**Enable Positive Input** This bit enables the voltage measurement on the FAINxP analog input. 0_B Analog input FAINxP is high-impedance. The upper half of the measuring range is not available. 1_B Analog input FAINxP line is connected to the channel amplifier. The upper half of the measuring range is available.

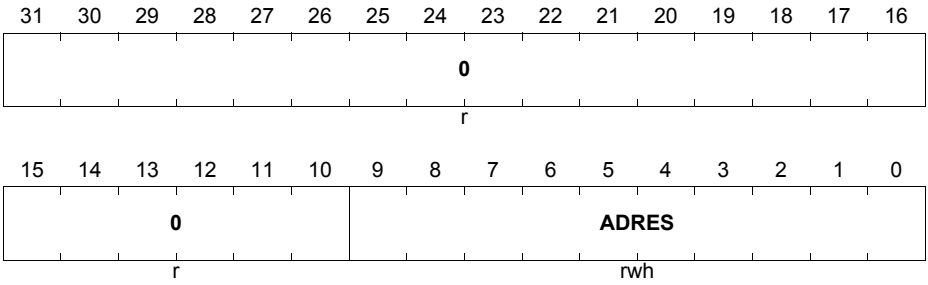
Field	Bits	Type	Description
ENN	3	rw	**Enable Negative Input** This bit enables the voltage measurement on the FAINxN analog input. 0_B Analog input FAINxN is high-impedance. The lower half of the measuring range is not available. 1_B Analog input FAINxN line is connected to the channel amplifier. The lower half of the measuring range is available.
CALOFF[2:0]	[10:8]	rw	**Calibrate Offset** This bit field determines the value applied for the offset calibration for channel x. The calibrate offset value is composed by the most significant bit CALOFF3 and bit field CALOFF[2:0], resulting in a 4-bit bit field CALOFF[3:0].
CALOFF3	12	rw	
0	[7:4], 11, [14:13], [31:15]	r	**Reserved** Read as 0. Should be written with 0.

32.3.3.3 Conversion Result Registers

The Channel x Conversion Result Register RCHx contains the conversion result of channel x.

RCHx (x = 0-3)
Channel x Conversion Result Register

(040_H+x*4_H) **Reset Value: 0000 0000_H**



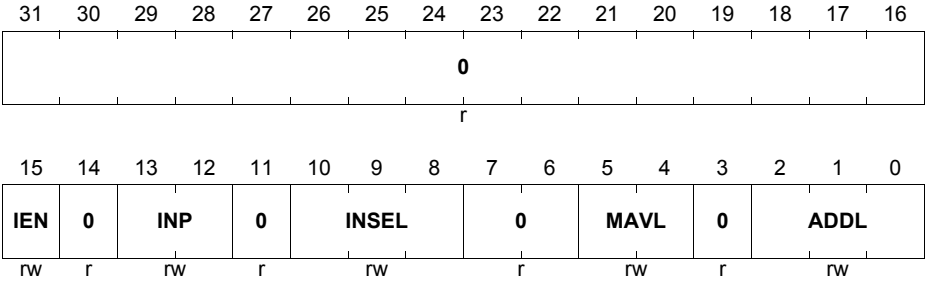
Field	Bits	Type	Description
ADRES	[9:0]	rwh	**AD Conversion Result** This bit field contains the conversion result of channel x. ADRES can only be overwritten by software if GCR.RESWEN = 1.
0	[31:10]	r	**Reserved** Read as 0. Should be written with 0.

32.3.4 Filter Registers

32.3.4.1 Filter Control Registers

Filter blocks are controlled by bits in the Filter n Control Registers FCRn.

FCRn (n = 0-3)
Filter n Control Register **(060_H+n*20_H)** **Reset Value: 0000 0000_H**



Field	Bits	Type	Description
ADDL	[2:0]	rw	**Addition Length** This bit field determines the number of filter input values that are added to obtain one intermediate result. 000_B Each filter input value is considered as intermediate result. 001_B 2 filter input values are added up. 010_B 3 filter input values are added up. 011_B 4 filter input values are added up. 100_B 5 filter input values are added up. 101_B 6 filter input values are added up. 110_B 7 filter input values are added up. 111_B 8 filter input values are added up.

Field	Bits	Type	Description
MAVL	[5:4]	rw	**Moving Average Length** This bit field determines the number of intermediate results that are added up for a final result. 00_B No moving average is selected. Each intermediate result is considered as final result value: FRRn.FR = CRRn.CR 01_B A moving average of 2 values is selected. The final result is calculated by 2 values: FRRn.FR = CRRn.CR + IRR1n.IR 10_B A moving average of 3 values is selected. The final result is calculated by 3 values: FRRn.FR = CRRn.CR + IRR1n.IR + IRR2n.IR 11_B A moving average of 4 values is selected. The final result is calculated by 4 values: FRRn.FR = CRRn.CR + IRR1n.IR + IRR2n.IR + IRR3n.IR Bit combinations 10_B and 11_B are not available in filter blocks 1 and 3 and must not be selected there.

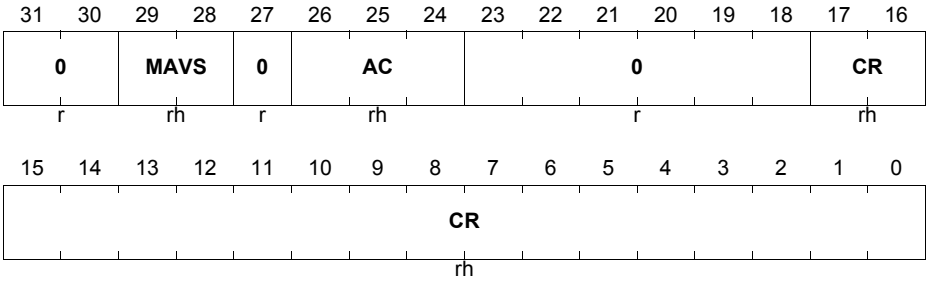
Field	Bits	Type	Description
INSEL	[10:8]	rw	**Input Selection** This bit field enables the filter block and determines which input value is taken for filter block n. For the settings 010_B, set FORM = 00_B. 000_B The filter block is disabled. Intermediate and final sum calculations are not executed. The filter register values are not changed (except by a filter block reset). 001_B Any conversion result of any channel is taken as new filter input value. 010_B Filter block 0: filter is stopped (as 000_B). Filter block 1: filter input value is the output value (final result) of filter block 0. Filter block 2: filter is stopped (as 000_B). Filter block 3: filter input value is the output value (final result) of filter block 2. 011_B Reserved 100_B Channel 0 conversion result is taken as filter input value. 101_B Channel 1 conversion result is taken as filter input value. 110_B Channel 2 conversion result is taken as filter input value. 111_B Channel 3 conversion result is taken as filter input value. *Note: Channel 2/3 is only applicable for FADC modules having 4 channels*
INP	[13:12]	rw	**Interrupt Node Pointer** This bit field selects which service request output line will be activated when a final result of filter block n is available while bit IEN is set. 00_B Service request output SR0 selected 01_B Service request output SR1 selected 10_B Service request output SR2 selected 11_B Service request output SR3 selected
IEN	15	rw	**Interrupt Enable** This bit enables the generation of a new final result service request of filter block n. 0_B Service request generation disabled 1_B Service request generation enabled

Field	Bits	Type	Description
0	3, [7:6], 11, 14, [31:16]	r	**Reserved** Read as 0. Should be written with 0.

32.3.4.2 Current Result Registers

The Current Result Registers CRRn store the current result of filter n. Further, status information of filter block n can be read from CRRn.

CRRn (n = 0-3)
Filter n Current Result Register (064_H + n * 20_H) **Reset Value: 0000 0000_H**



Field	Bits	Type	Description
CR	[17:0]	rh	**Current Result** This bit field (significant bits [12:0] for filter 0 and 2, [17:0] for filter 1 and 3) contains the right-aligned current result value of filter 0. CR is cleared when writing GCR.RSTFn = 1.
AC	[26:24]	rh	**Addition Count** This bit field indicates the number of additions of filter input values with remain to be executed before the next intermediate result register transfer occurs. AC is loaded with the value of FCRn.ADDL for a new addition sequence, also when writing GCR.RSTFn = 1.

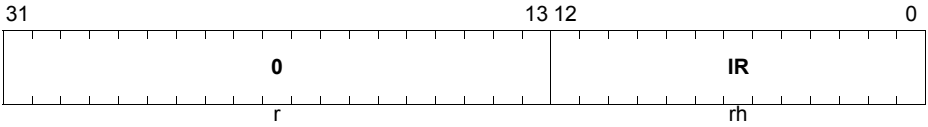
Field	Bits	Type	Description
MAVS	[29:28]	rh	**Moving Average State** This bit field indicates how many intermediate registers transfers remain to be executed for the generation of the next final result. MAVS = 0 indicates the end of a filter calculation operation. Since the filter calculation is executed very fast in comparison to a conversion, MAVS > 0 can be interpreted only as a kind of calculation busy flag. Therefore, it is recommended to read a valid filter result from register FRRn only when the corresponding interrupt request flag CRSR.IRQFn is set. MAVS is reset when writing GCR.RSTFn = 1.
0	[23:18], 27, [31:30]	r	**Reserved** Read as 0. Should be written with 0.

32.3.4.3 Intermediate Result Registers

The Intermediate Result Registers IRRmn hold the intermediate results y of filter n.

IRRy0 (y = 1-3)
Filter 0 Intermediate Result Register y
(064_H+y*4_H) **Reset Value: 0000 0000_H**

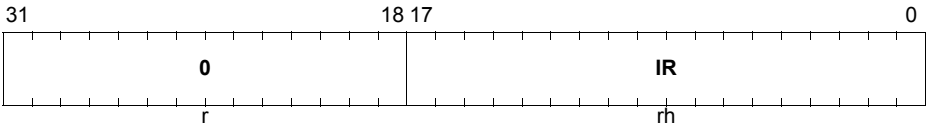
IRRy2 (y = 1-3)
Filter 2 Intermediate Result Register y
($0A4_H$+y*4_H) **Reset Value: 0000 0000_H**



Field	Bits	Type	Description
IR	[12:0]	rh	**Intermediate Result** This bit field contains the right-aligned intermediate result. IR is cleared when writing GCR.RSTFn = 1.
0	[31:13]	rh	**Reserved** Read as 0. Should be written with 0.

IRR11
Filter 1 Intermediate Result Register 1
(088_H) **Reset Value: 0000 0000_H**

IRR13
Filter 3 Intermediate Result Register 1
($0C8_H$) **Reset Value: 0000 0000_H**

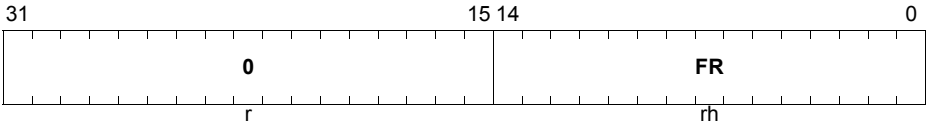


Field	Bits	Type	Description
IR	[17:0]	rh	**Intermediate Result** This bit field contains the right-aligned intermediate result. IR is reset when writing GCR.RSTFn = 1.
0	[31:18]	rh	**Reserved** Read as 0. Should be written with 0.

32.3.4.4 Final Result Registers

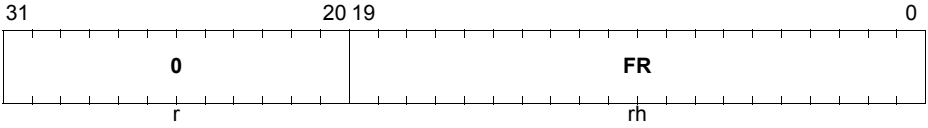
The Final Result Registers FRRn hold the final results of filter block n. The data width being different for the filter block 0 and 2 from the one from data blocks 1 and 3, two different register layouts are necessary.

FRR0
Filter 0 Final Result Register **(074_H)** **Reset Value: 0000 0000_H**
FRR2
Filter 2 Final Result Register **($0B4_H$)** **Reset Value: 0000 0000_H**



Field	Bits	Type	Description
FR	[14:0]	rh	**Final Result** This bit field contains the right-aligned final result. FR is cleared when writing GCR.RSTFn = 1.
0	[31:15]	rh	**Reserved** Read as 0. Should be written with 0.

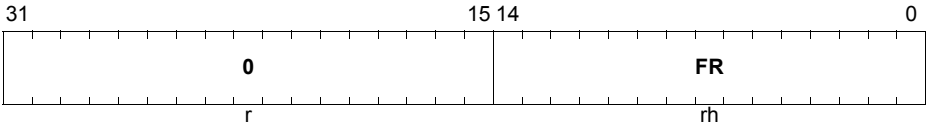
FRR1
Filter 1 Final Result Register **(094_H)** **Reset Value: 0000 0000_H**
FRR3
Filter 3 Final Result Register **($0D4_H$)** **Reset Value: 0000 0000_H**



Field	Bits	Type	Description
FR	[19:0]	rh	**Final Result** This bit field contains the right-aligned final result. FR is cleared when writing GCR.RSTFn = 1.
0	[31:20]	rh	**Reserved** Read as 0. Should be written with 0.

The Shifted Final Result Registers SFRRn hold the final results of filter blocks 1 and 3 that are shifted right by 5 bit positions. The data representation allows the use of 16-bit data operations for further treatment.

SFRR1
Filter 1 Shifted Final Result Register (098_H) **Reset Value: $0000\ 0000_H$**
SFRR3
Filter 3 Shifted Final Result Register ($0D8_H$) **Reset Value: $0000\ 0000_H$**



Field	Bits	Type	Description
FR	[14:0]	rh	**Final Result** This bit field contains the right-aligned final result from the corresponding final result register FRRn shifted right by 5 bit positions. FR is cleared when writing GCR.RSTFn = 1.
0	[31:15]	rh	**Reserved** Read as 0. Should be written with 0.

32.4 Implementation of FADC

This section describes the implementation of the FADC module in the TC1798.

32.4.1 Register Overview

All FADC kernel register names described in this section are referenced in other parts of the TC1798 User´s Manual by the module name prefix “FADC_”.

Table 32-7 Registers Address Space - FADC Module

Module	Base Address	End Address	Note
FADC	$F010\ 0400_H$	$F010\ 05FF_H$	-

Table 32-8 Registers Overview

Register Short Name	Register Long Name	Offset Address	Page Number
intentionally left blank, please refer to register table in Section 32.3		H	

32.4.2 FADC Connections

The following table shows the analog connections of the FADC kernel with other modules or pins in the TC1798 device.

Table 32-9 Connections to FADC Analog Part in TC1798

FADC Signal of Analog Part	from/to Module or Pin	Input or Output	Can be used to/as
V_{DDIF}	V_{DDM}	I	analog power supply 3 V - 5.5 V of input stage, connected to the power supply of the ADC
V_{DDMF}	V_{DDA}	I	analog power supply 3.3 V
V_{SSMF}	V_{SSMF}	I	analog power ground
V_{DDAF}	V_{DDAF}	I	analog power supply 1.2 V
V_{SSAF}	V_{SSM}	I	analog power ground
V_{FAREF}	V_{FAREF}	I	positive analog reference,
V_{FAGND}	V_{FAGND}	I	negative analog reference,
FAIN0P	AN64	I	analog input P channel 0
FAIN0N	AN65	I	analog input N channel 0
FAIN1P	AN66	I	analog input P channel 1
FAIN1N	AN67	I	analog input N channel 1
FAIN2P	AN68	I	analog input P channel 2
FAIN2N	AN69	I	analog input N channel 2
FAIN3P	AN70	I	analog input P channel 3
FAIN3N	AN71	I	analog input N channel 3

The following table shows the digital connections of the FADC kernel with other modules or pins in the TC1798 device.

Table 32-10 Connections of FADC Digital Part in TC1798

FADC Signal of Digital Part	from/to Module or Pin	Input or Output	Can be used to/as
Gating Inputs			
GSA	REQ0	I	P1.0P1.0P1.0P1.0

Table 32-10 Connections of FADC Digital Part in TC1798 (cont'd)

FADC Signal of Digital Part	from/to Module or Pin	Input or Output	Can be used to/as
GSB	REQ4	I	P7.0
GSC	PDOUT2	I	ERU
GSD	PDOUT3	I	ERU
GSE	TRIG11	I	GPTA
GSF	TRIG13	I	GPTA
GSG	TRIG15	I	GPTA
GSH	TRIG17	I	GPTA
Trigger Inputs			
TSA	REQ1	I	P1.1
TSB	REQ5	I	P7.1
TSC	IOUT2	I	ERU
TSD	IOUT3	I	ERU
TSE	TRIG00	I	GPTA
TSF	TRIG02	I	GPTA
TSG	TRIG04	I	GPTA
TSH	TRIG06	I	GPTA
Others			
FADC_ SR[3:0]	interrupt controller, DMA	O	service request output lines of FADC (service request)

32.4.3 Service Request Connections

The FADC kernel provides 4 service request output lines FADC_SR[3:0]. All 4 lines are connected to the DMA (for more details, refer to DMA chapter).

Table 32-11 FADC Service Request Connections in TC1798

Service Request Signal	Connected to Service Request Node
FADC_SR[0]	FADC_SRC0
FADC_SR[1]	FADC_SRC1
FADC_SR[2]	FADC_SRC2
FADC_SR[3]	FADC_SRC3

32.4.4 Clock Control

The FADC module is provided with two clock signals:

- f_{CLC}
  This is the module clock that is used inside the FADC kernel for control purposes such as clocking of control logic and register operations. The frequency of f_{CLC} is always identical to the system clock frequency f_{FPI}. The clock control register FADC_CLC makes it possible to enable/disable f_{CLC}.
- f_{FADC}
  This clock is the module clock that is used in the FADC as the clock for the channel timer and other internal timings, such as the conversion timing. The fractional divider registers FADC_FDR controls the frequency of f_{FADC} and allows it to be enabled/disabled independently of f_{CLC}.

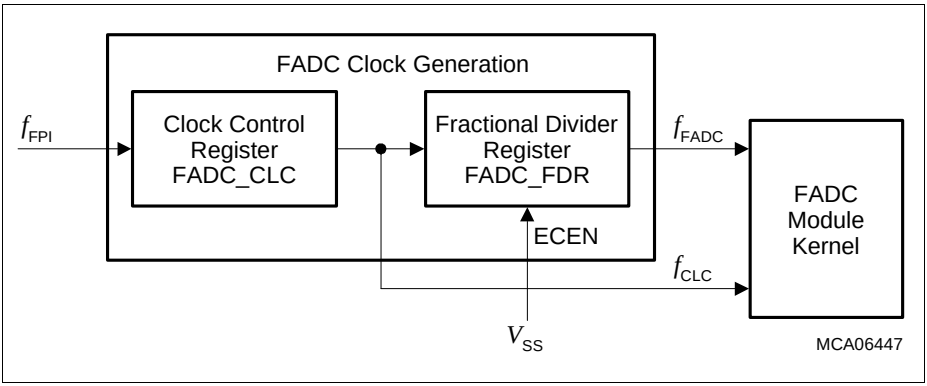


Figure 32-15 FADC Clock Generation

The following formulas define the frequency of f_{FADC}:

$$f_{FADC} = f_{FPI} \times \frac{1}{n} \quad \text{with n = 1024 - FDR.STEP} \tag{32.2}$$

$$f_{FADC} = f_{FPI} \times \frac{n}{1024} \quad \text{with n = 0-1023} \tag{32.3}$$

Equation (32.2) is valid for FADC_FDR.DM = 01_B (normal divider mode).

Equation (32.3) is valid for FADC_FDR.DM = 10_B (fractional divider mode).

Keyword Index

A

Abbreviations 1-4
Access mode definitions 1-3
ADC
- ADC0 Connections **31-137**
- ADC1 Connections **31-143**
- ADC2 Connections **31-149**, **31-155**
- Equidistant Sampling **31-120**
- Registers
  - ALR0 **31-84**
  - APR **31-125**
  - ASENR **31-47**
  - BWDCFGR **31-133**
  - BWDENR **31-132**
  - CHCTRx **31-81**
  - CHENPRx **31-88**
  - CHFCR **31-87**
  - CHFR **31-86**
  - CLC **31-25**
  - CRCRx **31-54**
  - CRMRx **31-57**
  - CRPRx **31-56**
  - EMCTR **31-126**
  - EVFCR **31-109**
  - EVFR **31-107**
  - EVNPR **31-110**
  - GLOBCFG **31-37**
  - GLOBCTR **31-34**
  - GLOBSTR **31-39**
  - ID **31-32**
  - INPCRx **31-83**
  - INTR **31-33**
  - KSCFG **31-26**
  - LCBRx **31-85**
  - Q0Rx **31-70**
  - QBURx **31-72**
  - QINRx **31-74**
  - QMRx **31-65**
  - QSRx **31-68**
  - RCRx **31-105**
  - RESR0 **31-100**
  - RESRD0 **31-100**
  - RESRDx **31-102**
  - RESRx **31-102**
  - RNPRx **31-111**
  - RSIRx **31-29**
  - RSPRx **31-48**
  - SRCx **31-28**
  - SYNCTR **31-130**
  - VFR **31-104**

ASC
- Asynchronous mode 20-4–20-8
  - Data frames 20-5
- Baud rate generation 20-12–20-16
  - Asynchronous modes 20-13
  - Synchronous mode 20-16
- Block diagram
  - Asynchronous modes 20-4
  - Synchronous mode 20-9
- DMA request outputs 20-40
- Error detection 20-17
- Features 20-2
- Implementation
  - Address map 20-42
- Interrupt generation 20-17
- Module implementation
  - DMA request outputs 20-40
  - Input/output function selection 20-37
  - Interrupt registers 20-39
  - Module clock control 20-33
  - Peripheral input select 20-35
- Registers 20-19
  - BG **20-27**
  - CON **20-22**
  - FDV **20-27**
  - ID **20-21**
  - Offset addresses 20-19
  - Overview **20-19**
  - PISEL **20-20**
  - RBUF **20-29**

TBUF **20-28**
WHBCON **20-25**
Synchronous mode 20-9–20-11
Timings 20-11
ASI
Field in MMU_ASI Register 2-25

B

Basic operation 10-3
BCU
SBCU 4-70
Bus agents and priorities 4-70
Bus arbitration 4-70
Bus error handling 4-72
Starvation prevention 4-72
BMU
Registers
CLC **18-30**
CTL **18-33**
FMCTL **18-43**
FMSTS **18-43**
FMTH **18-44**
FULLNESS **18-35**
ID **18-32**
MIECON **18-47**
MIECON2 **18-47**
PSET0 **18-36**
PSET1 **18-39**
PTR **18-34**
SMACON **18-46**
SRC **18-49**
TID **18-42**
BootROM 5-5

C

CAN
Address map 24-214
Basics 24-2
Addressing and arbitration 24-2
Basic-/Full-CAN 24-10
Error detection and handling 24-9
Frame formats 24-3
Nominal bit time 24-8
Block diagram 24-14
DMA requests 24-209
Module implementation 24-202–24-213
External registers 24-203
I/O line control 24-208
Input/output function selection 24-208
Interfaces 24-202
Interrupt control 24-211
Module clock generation 24-204
MultiCAN
Bit timing 24-26
Block diagram 24-18
Clock generation 24-21, 24-22
Interrupt structure 24-20
Message acceptance filtering 24-39
Message object data handling 24-46
Message object FIFO 24-53
Message object functionality 24-52
Message object interrupts 24-42
Message object lists 24-31
Node control 24-25
Node interrupts 24-29
Suspend mode 24-23
MultiCAN module features 24-15
MultiCAN registers
Address ranges 24-214
LISTi **24-71**
MCR **24-69**
MITR **24-70**
MOAMRn **24-110**
MOARn **24-112**
MOCTRn **24-94**
MODATAHn **24-116**
MODATALn **24-115**
MOFCRn **24-104**
MOFGPRn **24-109**
MOIPRn **24-102**
MOSTATn **24-97**
MSIDk **24-74**

MSIMASK **24-75**
MSPNDk **24-73**
NBTRx **24-87**
NCRx **24-76**
NECNTx **24-89**
NFCRx **24-90**
NIPRx **24-84**
NPCRx **24-86**
NSRx **24-80**
Overview 24-60
PANCTR **24-65**
Registers
Offset addresses 24-61
TTCAN 24-117
Application watchdog 24-153
Automatic TUR adjust 24-118
Configuration 24-151
Cycle time 24-118
Error handling 24-153
Interrupt control 24-155
Local offset and global time 24-121
Local time generation 24-117
Master reference mark 24-120
MSC handling 24-154
Reference message 24-123
Scheduler 24-126
Scheduler entry setup 24-145
Scheduler entry types 24-128
ARBE 24-134
BCE 24-143
EOS 24-144
ICE 24-132
RCE 24-139, 24-141
TCE 24-136, 24-129
Scheduler instruction sequence 24-148
Scheduler memory 24-127
Transmit enable window 24-120
Transmit trigger 24-122
TTCAN extension features 24-17
TTCAN Basics 24-11
Basic cycle 24-11
Global system time 24-12
Network time unit 24-13
System matrix 24-12
Time reference 24-11
TTCAN extension registers 24-157
Address map 24-159
AWDR **24-171**
CYCTMR **24-166**
GMR **24-169**
LGMR **24-170**
LOR **24-167**
LREFMR **24-165**
LTR **24-162**
Offset addresses 24-157
Overview 24-157
REFMR **24-164**
SISR **24-198**
STPTR0 **24-195**
STSRH **24-197**
STSRL **24-196**
SYNMR **24-163**
TTCFGR **24-176**
TTCR **24-172**
TTFMR **24-183**
TTIER **24-189**
TTINPR **24-193**
TTIRR **24-185**
TTSR **24-178**
TURR **24-160**
CAPCOM6 1-47
Capture Mode
GPT1 30-29
GPT2 (CAPREL) 30-55
Capture/Compare Unit 6 1-47
Chip select outputs 15-53
CLC register 3-54
Implementation in the modules 3-57
Clock
output signal 3-30
Clock System
Oscillator run detection 3-9
Clock system

Clock source 3-8, 3-17
Clock tree diagram 3-3
Features 3-2
Module clock generation 3-53
CLC register 3-54
Fractional divider 3-58
Oscillator run detection 3-6
Overview 3-2
PLL, see “PLL”
Concatenation of Timers 30-25, 30-53
Count direction 30-6, 30-41
Counter 30-23, 30-51
Counter Mode (GPT1) 30-10, 30-45
CPU
Registers **2-59**
COMPAT **2-29**
CPU_ID **2-26**
CPU_SBSRC **2-61**
CPU_SRCn **2-60**
DIEAR **2-53**
DIETR **2-51**
FPU_ID **2-39**
ICR **2-23**
MIECON **2-42**, **2-44**
MMU_CON **2-24**
PIEAR **2-49**
PIETR **2-47**
PSW **2-22**
SMACON **2-55**
see also Processor subsystem
CSCOMB control 15-53

D

Direction
count 30-6, 30-41
DMA 12-2
Access protection 12-44
Access protection assignment 12-111
Block diagram 12-2, 13-2
Bridge Functionality 12-26
Bus switch 12-21, 13-21
Bus Switch Priorities 12-23
Bus Switch Priorities of DMA Move Engines 12-23
Channel operation 12-6, 13-6
Channel operation modes 12-11, 13-11
Channel request control 12-10, 13-10
Channel reset operation 12-16, 13-16
Circular buffer 12-19, 13-19
Control Registers Offset addresses 12-48
Debug capabilities 12-27, 13-23
Definition of terms 12-4, 13-4
DMA Principle 12-5
Error conditions 12-15, 13-15
Features 12-3, 13-3
Implementation diagram 12-100, 13-84
Interrupts 12-30, 13-26
Channel interrupts 12-30, 13-26
Interrupt request compressor 12-36, 13-31
Move engine interrupts 12-33, 13-29
Transaction lost interrupts 12-32, 13-28
Wrap buffer interrupts 12-35, 13-30
Memory Checker Control Registers Offset addresses 12-132
On Chip Bus Access Rights, RMW support 12-24, 13-21
On Chip Bus Master Interfaces 12-25, 13-21
Pattern detection 12-37, 13-32
Priorities on On Chip Busses 12-24
Registers
ADRCR0x **12-92**
ADRCR1x **12-92**
Block address map 12-129, 13-95
CHCR0x **12-85**
CHCR1x **12-85**
CHICR0x **12-90**
CHICR1x **12-90**
CHRSTR **12-59**
CHSR0x **12-89**
CHSR1x **12-89**

CLRE **12-71**
DADR0x **12-98**
DADR1x **12-98**
DMA_MLI0SRCx **12-127**
DMA_MLI1SRCy **12-127**
DMA_SRCx **12-126**
EER **12-65**
ERRSR **12-68**
GINTR **12-58**
HTREQ **12-63**
ID **12-53**
INTCR **12-77**
INTSR **12-73**
ME0AENR0 **12-81**
ME0AENR1 **12-81**
ME0ARR0 **12-83**
ME0ARR1 **12-83**
ME0PR **12-80**
ME0R **12-80**
ME1AENR0 **12-81**
ME1AENR1 **12-81**
ME1ARR **12-83**
ME1ARR0 **12-83**
ME1PR **12-80**
ME1R **12-80**
MESR **12-78**
OCDSR **12-54**
Overview **12-47**, **13-40**
SADR0x **12-97**
SADR1x **12-97**
SHADR0x **12-99**
SHADR1x **12-99**
STREQ **12-62**
SUSPMR **12-56**
TRSR **12-60**
WRPSR **12-75**
Request wiring matrix 12-101, 13-84
Transaction control 12-20, 13-20
DMI
Features 2-88
Overlay Control 7-1
DMI Data Memory Interface 2-88
Document
Structure 1-1
Terminology and abbreviations 1-3
Textual conventions 1-1

E

EBU 15-1
Access phases 15-62
Address phase 15-63
Burst phase 15-65
Command delay phase 15-64
Command phase 15-64
Data hold phase 15-65
Recovery phase 15-67
Address region selection 15-49
Asynchronous accesses
Signals 15-69
Wait control 15-76
Boot operation 15-41
Boot read access cycle 15-43
Configuration word 15-44
External boot mode 15-41
External bus arbitration 15-28
Arbitration modes 15-30
Arbitration signals 15-28
Arbitration timing 15-32
EBU as participant 15-35
EBU as sole master 15-30
Locking external bus 15-39
Modes 15-28
Memory regions 15-45
Registers
ADDRSELx **15-163**
BUSRAPx **15-172**
BUSRCONx **15-165**
BUSWAPx **15-175**
BUSWCONx **15-169**
CLC **15-156**
DDRNCON **15-190**
DDRNMOD **15-192**
DDRNMOD2 **15-194**
DDRNPRLD **15-197**
DDRNSRR **15-196**
DDRNTAGx **15-198**

EXTBOOT **15-161**
MODCON **15-158**
Overview 15-153
SDRMCON **15-178**
SDRMOD **15-180**
SDRMREF **15-183**
SDRSTAT **15-185**
USERCON **15-199**
EBU Control Register
Offset Addresses 15-153
EBU_ADDRSEL0 **15-163**
EBU, see “External bus interface unit”
Emergency stop output control 3-155
Register SCU_EMSR **3-157**
Entering Sleep Mode 3-122
E-Ray
Block diagram 1-33, 26-1, 26-263
Channel protocol controller 26-4
Clock
Minimum 26-243
Communication controller
Commands 26-92, 26-95
FIFO 26-230
Message RAM 26-248
POC 26-116
Protocol operation control 26-116
Restrictions 26-262
Service requests 26-259
Customer host interface 26-3
Frame processing 26-5
Generic host interface 26-3
Global time unit 26-5
Input buffer 26-4
Interrupt control 26-6
Kernel
Clock minimum 26-243
RAM test 26-30
Release coding 26-167
Service request 26-41, 26-87
Test registers 26-23
Kernel block diagram 26-3
Kernel description 1-33, 26-1
Message buffer pointer 26-140
Message handler 26-4
Message RAM 26-4
Module implementations 26-263
On-chip connections 26-266
Service request 26-269
Module registers 26-8
Network management 26-5
Output Buffer 26-4
Overview 1-34, 26-2
Protocol
Clock 26-199
Communication cycle 26-196
Network management 26-222
Register offsets 26-8–??
Registers 26-8–??, 26-16
ACS **26-130**
CCEV **26-120**
CCSV **26-115**
CLC **26-268**
Communication controller control 26-88, 26-113
Communication controller status 26-115–26-137
CREL **26-166**
CUST1 **26-17**
CUST3 **26-20**
Customer registers 26-16
EIER **26-65**
EIES **26-60**
EILS **26-52**
EIR **26-41**
ENDN **26-168**
ESIDnn (nn = 01-015) **26-133**
FCM **26-144**
FRF **26-141**
FRFM **26-143**
FSR **26-149**
GTUC01 **26-103**
GTUC02 **26-104**
GTUC03 **26-105**
GTUC04 **26-106**
GTUC05 **26-107**
GTUC06 **26-108**

GTUC07 **26-109**
GTUC08 **26-110**
GTUC09 **26-111**
GTUC10 **26-112**
GTUC11 **26-113**
IBCM **26-175**
IBCR **26-177**
ID **26-16**
Identification 26-166–26-168
ILE **26-80**
Input buffer 26-168–26-177
INT0SRC **26-279**
INT1SRC **26-279**
LCK **26-39**
LDTS **26-148**
MBS **26-186**
MBSC0SRC **26-279**
MBSC1 **26-162**
MBSC10SRC **26-279**
MBSC2 **26-163**
MBSC3 **26-164**
MBSC4 **26-165**
Message buffer control 26-138–26-144
Message buffer status 26-145–26-165
MHDC **26-102**
MHDF **26-151**
MHDS **26-145**
MRC 26-138
MSIC1 **26-274**
MSIC2 **26-275**
MSIC3 **26-276**
MSIC4 **26-277**
MTCCV **26-122**
NDAT0SRC **26-279**
NDAT1 **26-158**
NDAT1SRC **26-279**
NDAT2 **26-159**
NDAT3 **26-160**
NDAT4 **26-161**
NDIC1 **26-270**
NDIC2 **26-271**
NDIC3 **26-272**
NDIC4 **26-273**
NEMC **26-98**
NMVx (x = 1-3) **26-137**
OBCM **26-191**
OBCR **26-194**
OCV **26-124**
OSIDnn (nn = 01-15) **26-135**
Output buffer 26-179–26-193
PRT2 **26-101**
PRTC1 **26-99**
RCV **26-123**
RDDSnn (nn = 01-64) **26-179**
RDHS1 **26-180**
RDHS2 **26-182**
RDHS3 **26-184**
SCV **26-121**
Service request 26-41, 26-87
Service request nodes 26-269
SFS **26-125**
SIER **26-75**
SIES **26-70**
SILS **26-56**
SIR **26-47**
STPW1 **26-85**
STPW2 **26-87**
SUCC1 **26-88**
SUCC2 **26-96**
SUCC3 **26-97**
SWINIT **26-127**
T1C **26-83**
Test registers 26-23
TEST1 **26-23**
TEST2 **26-28**, **26-31**, **26-33**, **26-35**, **26-37**, **26-38**
TINT0SRC **26-279**
TINT1SRC **26-279**
TOC **26-81**
TXRQ1 **26-154**
TXRQ2 **26-155**
TXRQ3 **26-156**
TXRQ4 **26-157**
WRDSnn (nn = 01-64) **26-169**

WRHS **26-170**
WRHS2 **26-173**
WRHS3 **26-174**
Symbol processing 26-5
System universal control 26-5
Transient buffer 26-4
ESR
Registers
ESRCFG0 **3-84**
ESRCFG1 **3-84**
SCU_IOCR **3-85**
External bus interface unit, see “EBU”
External request unit
Registers 3-104
EICR0 **3-105**
EICR1 **3-108**
EIFR **3-112**
FMR **3-112**
IGCR0 **3-114**
IGCR1 **3-117**
PDDR **3-113**

F

FADC
Calibration 32-21
Channel timers 32-11
Channel triggers 32-8
Clock generation 32-13
Conversion priority 32-12
Data reduction filter 32-15
Filter block structure 32-16
Filter concatenation 32-17
Gating modes 32-9
Interrupts 32-23
Module implementation
Module clock control 32-67
Neighbor channel triggers 32-20
Registers
ACRx **32-52**
ALR **32-46**
CFGRx **32-48**
CLC **32-30**
CRRn **32-58**
CRSR **32-35**
FCRn **32-55**
FDR **32-31**
FMR **32-37**
FRRn **32-62**
GCR **32-42**
ID **32-33**
IRRyn **32-60**
NCTR **32-39**
Overview **32-26**
RCHx **32-54**
SFRRn **32-63**
SRCn **32-34**
Trigger modes 32-10
FCE
Block diagram 14-4
Block Diagram CRC Kernels 14-5
Control Registers Offset addresses 14-15
Features 14-3
Programming Guide 14-28
Registers
CFGm **14-22**
CHECKm **14-25**
CLC **14-17**
CRCm **14-26**
CTRm **14-27**
ID **14-20**
IRm **14-21**
LENGTHm **14-25**
Overview **14-14**
Register Map **14-15**
RESm **14-21**
STSm **14-24**
Related Documents 14-2
FDR register 3-51, 3-64
Features
Instruction set 1-10
On-chip memory 1-10
Flash 5-6
ALSE 5-78
Application Hints 5-64
Command sequences 5-13

Clear Status 5-18
Disable Read Protection 5-17
Disable Sector Write Protection 5-17
Enter Page Mode 5-14
Erase Physical Sector 5-16
Erase Sector 5-15
Erase User Configuration Block 5-16
Load Page 5-14
Reset to Read 5-13
Resume Protection 5-18
Write Page 5-15
Write User Configuration Page 5-15
Concurrent operations 5-18
Configuration Sector 5-7
ECC 5-23, 5-79
Endurance 5-6
Erasing 5-6
Flash Bank 5-7
Flash Module 5-7
Flash Structure 5-7
Interrupts and traps 5-25
KeyFlash 5-7
Logical Sector 5-7
Margin checks 5-24
Operations 5-10
Page 5-7
Physical Sector 5-7
Power reduction 5-26
Programming 5-6
Protection 5-19
Read Buffers 5-9
Registers
ECCR 5-61
ECCW 5-60
FCON 5-41
FSR 5-32
ID 5-47
MARD 5-51
MARP 5-50
PROCON0 5-52
PROCON1 5-55
PROCON2 5-58
RDBCFG0 5-46
RDBCFG1 5-46
RDBCFG2 5-46
SEMA 5-49
SHEBOOT0-2 5-62
XFSR 5-39
Reset 5-25
Resets during Flash operation 5-76
Retention 5-6
Sector 5-7
UCB 5-7, 5-21
User Configuration Block 5-7
Word-Line 5-7
FPI Bus 4-65
Basic operations 4-68
Overview 4-65
Transaction types 4-67
Fractional divider 3-58
Block diagram 3-28
FDR register 3-51, 3-64
Implementation in the modules 3-61
Operating modes 3-29
Frequency
output signal 3-30

G

Gated timer mode (GPT1) 30-9
Gated timer mode (GPT2) 30-44
GPT1 30-2
GPT2 30-37
GPTA
Address ranges 28-308
Block diagram 28-8
Clock generation cells (CGC) 28-10
Clock distribution module 28-35
Digital phase locked loop cell 28-30
Duty cycle measurement cell 28-26
Filter and prescaler cell 28-12
Phase discrimination logic 28-21
Features of GPTA0 28-5
Features of GPTA0/GPTA1 1-44

Features of GPTA1 28-5
Input IN1 control 3-181
Interrupt processing and control 28-123, 28-248
Module implementations 28-274
Block diagram 28-275
Cascading limits 28-306
External registers 28-276
Input/output function selection 28-279
Module clock generation 28-296
On-chip connections 28-286
Port control and connections 28-276
Overview 28-4
Programming hints 28-158
Pseudo-code description 28-126–28-155
Registers
Address ranges 28-308
Signal generation cells (SGC)
Global timer cell 28-55
Global timers 28-38
Local timer cell 28-67
GPTA0
Registers
CKBCTR **28-185**
CLC **28-300**
DBGCTR **28-305**
DCMCAVk **28-175**
DCMCOVk **28-176**
DCMCTRk **28-173**
DCMTIMk **28-175**
EDCTR **28-303**
FDR **28-301**
FPCCTRk **28-168**
FPCSTAT **28-167**
FPCTIMk **28-170**
GIMCRHg **28-217**
GIMCRLg **28-215**
GTCCTRk **28-187**, **28-189**
GTCTRk **28-182**
GTCXRk **28-191**
GTREVk **28-184**
GTTIMk **28-183**
LIMCRHg **28-221**
LIMCRLg **28-219**
LTCCTR63 **28-204**
LTCCTRk **28-192**, **28-195**
LTCXR63 **28-206**
LTCXRk **28-205**
MMXCTR00 **28-291**
MMXCTR01 **28-291**
MMXCTR10 **28-292**
MMXCTR11 **28-293**
MRACTL **28-207**
MRADIN **28-208**
MRADOUT **28-209**
Offset addresses 28-161
OMCRHg **28-212**, **28-307**
OMCRLg **28-210**
OTMCRLg **28-214**
Overview 28-160
PDLCTR **28-171**
PLLCNT **28-179**
PLLCTR **28-177**
PLLDTR **28-181**
PLLMTI **28-178**
PLLREV **28-180**
PLLSTP **28-179**
SRNR **28-232**
SRSC0 **28-223**
SRSC1 **28-226**
SRSC2 **28-228**
SRSC3 **28-230**
SRSS0 **28-225**
SRSS1 **28-227**
SRSS2 **28-229**
SRSS3 **28-231**
GPTA1
Registers
CKBCTR **28-185**
DCMCAVk **28-175**
DCMCOVk **28-176**
DCMCTRk **28-173**
DCMTIMk **28-175**

FPCCTRk **28-168**
FPCSTAT **28-167**
FPCTIMk **28-170**
GIMCRHg **28-217**
GIMCRLg **28-215**
GTCCTRk **28-187**, **28-189**
GTCTRk **28-182**
GTCXRk **28-191**
GTREVk **28-184**
GTTIMk **28-183**
LIMCRHg **28-221**
LIMCRLg **28-219**
LTCCTR63 **28-204**
LTCCTRk **28-192**, **28-195**
LTCXR63 **28-206**
LTCXRk **28-205**
MRACTL **28-207**
MRADIN **28-208**
MRADOUT **28-209**
Offset addresses 28-161
OMCRHg **28-212**
OMCRLg **28-210**
OTMCRg **28-214**
Overview 28-160
PDLCTR **28-171**
PLLCNT **28-179**
PLLCTR **28-177**
PLLDTR **28-181**
PLLMTI **28-178**
PLLREV **28-180**
PLLSTP **28-179**
SRCk **28-307**
SRNR **28-232**
SRSC0 **28-223**
SRSC1 **28-226**
SRSC2 **28-228**
SRSC3 **28-230**
SRSS0 **28-225**
SRSS1 **28-227**
SRSS2 **28-229**
SRSS3 **28-231**

I

Idle mode 3-121
Incremental Interface Mode (GPT1) 30-11
Interrupt system
- Arbitration cycles 16-12
- Arbitration process 16-12
- Block diagram 16-2
- Control register ICR 16-8
- External interrupts 16-22
- Hints for applications 16-18–16-22
- Interrupt control unit 16-8
- Interrupt vector table 16-15
- Overview 16-1
- Priorities 16-19
- Service request control register 16-3
- Service request node table 16-23
- Service request nodes 16-3
- Service routine entering 16-13
- Service routine exiting 16-14
- Software initiated interrupts 16-22

L

LMU
- Register
  - CLC **6-5**
  - ID **6-9**
  - MEMCON **6-6**

LTCA2
- Registers
  - LIMCRHg **28-272**
  - LIMCRLg **28-271**
  - LTCCTR31 **28-261**
  - LTCCTRk **28-252**
  - LTCXR31 **28-263**
  - LTCXRk **28-263**
  - MRACTL **28-264**
  - MRADIN **28-266**
  - MRADOUT **28-266**
  - Offset addresses 28-250
  - OMCRHg **28-269**
  - OMCRLg **28-268**
  - Overview 28-250

SRCk **28-307**
SRSC2 **28-228**
SRSC3 **28-230**
SRSS2 **28-229**
SRSS3 **28-231**

M

Memory Checker 12-130
Functionality 12-130
Registers
MCHK_ID **12-133**
MCHK_IRx **12-135**
MCHK_RRx **12-135**, **12-136**
MCHK_WR **12-136**
Memory maps 9-1
Access restrictions 9-21, 9-22
Segment 0 to 14 from SPB 9-8
Segment 15 from SPB 9-13
Segment contents 9-6
Memory protection system
Registers 2-33
MLI
Access protection 27-49
Block diagram 27-51
Communication principles 27-6
Frames 27-10
Answer frame 27-18
Command frame 27-17
Copy base address frame 27-12
Layout 27-11
Optimized read frame 27-16
Optimized write frame 27-14
Write offset and data frame 27-13
Handshake signalling 27-19
Interrupts 27-57
Receiver interrupts 27-62
Transmitter interrupts 27-59
Kernel registers 27-77
Module implementation 27-127
Clock generation 27-131
Input/output function selection 27-133
MLI0 block diagram 27-128, 27-129
On-chip connections 27-136
Transfer window map 27-138
Naming conventions 27-4
Receiver
I/O line control 27-53
Registers
AER **27-90**
AER1 **27-90**
ARR0 **27-91**
ARR1 **27-91**
FDR **27-79**
GINTR **27-83**
Offset addresses 27-78
OICR **27-86**
Overview 27-77
RADRR **27-118**
RCR **27-113**
RDATAR **27-119**
RIER **27-120**
RINPR **27-125**
RISR **27-123**
RPxBAR **27-117**
RPxSTATR **27-116**
SCR **27-84**
TCBAR **27-106**
TCR **27-92**
TDRAR **27-104**
TIER **27-107**
TINPR **27-111**
TISR **27-109**
TPxAOFR **27-103**
TPxBAR **27-105**
TPxDATAR **27-104**
TPxSTATR **27-97**
TRSTATR **27-101**
TSTATR **27-95**, **27-99**
Transaction flow diagrams
Command frame 27-41
Copy base address 27-28
Read frame 27-35
Write frame 27-30
Transmitter
Description of frame transmission

27-28
I/O line control 27-53
Typical application 27-2
MMU_ASI
Address Space Identifier Register Definition 2-25
Module clock generation 3-53
MSC
Applications 23-2
Downstream channel 23-5
Baud rate 23-20
Block diagram 23-5
Command frames 23-7
Data frames 23-9
Data repetition mode 23-15
Downstream counter 23-19
Frame formats 23-6
Output control 23-27
Passive time frames 23-11
Shift register operation 23-12
Transmission mode 23-14
Triggered mode 23-14
Features 23-4
I/O control 23-27
Interrupts 23-31
Command frame interrupt 23-32
Data frame interrupt 23-32
Interrupt request compressor 23-35
Receive data interrupt 23-34
Time frame finished interrupt 23-33
Kernel block diagram 23-3
Module implementation
Input/output function selection 23-69
Module clock control 23-65
Overview 23-3
Registers
DC **23-59**
DD **23-59**
DSC **23-41**
DSDSH **23-47**
DSDSL **23-46**
DSS **23-44**
ESR **23-48**
ICR **23-49**
ID **23-38**, **27-82**
ISC **23-54**
ISR **23-52**
OCR **23-56**
Offset addresses 23-37
Overview 23-36
UDx **23-60**
USR **23-39**
Upstream channel 23-21
Baud rate 23-25
Block diagram 23-21
Data frame protocol 23-22
Data reception 23-23, 23-24
Input control 23-30
Parity checking 23-22
Sampling 23-26

O

OCDS
Cerberus 19-10
Communication mode 19-11
Features 19-10
Multi-core break switch 19-11
Registers 19-14
RW mode 19-10
Triggered transfers 19-11
Components 19-4
JTAG interface 19-13
Registers 19-14
OCDS level 1 19-5
Debug actions 19-8
Debug event generation 19-7
of BCU 19-9
of CPU 19-6
of DMA 19-9
of PCP 19-9
Registers 19-8
OCDS level 3 19-1
Overview 19-1
System block diagram 19-3
Operational 14-4

OVC
Access performance 7-6
Data access overlay control 7-1
Data access redirection 7-2
Emulation memory overlay 7-6
External memory overlay 7-6
Overlay Memory Control Registers 7-7
Offset addresses 7-7
Overview 7-7
Overlay Registers
OCON 7-14, 7-16
OMASKx **7-12**
OTARx **7-11**
RABRx **7-9**
Overlay Control 7-1

P

PCON 2-85
PCP 11-1
Accessing from FPI bus 11-57
Architecture 11-3
Channel programs 11-27
Context models 11-13
Control and interrupt registers 11-62, 11-66
Debugging 11-60
Error handling 11-44
General purpose registers 11-8
Instruction set details 11-98
Instruction set overview 11-49
Instruction times 11-138
Instruction timing 11-135
Interrupt operation 11-34
Overview 11-2
Programming 11-145
Programming model 11-8
Programming tips 11-151
Registers
PCP_CLC **11-67**
PCP_CS **11-69**
PCP_ES **11-71**
PCP_ICON **11-77**
PCP_ICR **11-74**
PCP_ID **11-68**
PCP_ITR **11-76**
PCP_SMACON **11-81**, **11-82**, **11-83**, **11-84**, **11-85**, **11-86**, **11-87**, **11-91**
PCP_SRC0 **11-92**
PCP_SRC1 **11-92**
PCP_SRC10 **11-96**
PCP_SRC11 **11-96**
PCP_SRC2 **11-94**
PCP_SRC3 **11-94**
PCP_SRC4 **11-95**
PCP_SRC5 **11-95**
PCP_SRC6 **11-95**
PCP_SRC7 **11-95**
PCP_SRC8 **11-95**
PCP_SRC9 **11-96**
PCP_SSR **11-79**
Peripheral control processor, see PCP
PLL **3-7**, **3-16**
Features 3-7, 3-16
Functionality 3-7, 3-16
PMI
Features 2-79
Registers 2-82
PMI_CON0 **2-83**
PMI_CON1 **2-84**
PMI Program memory interface 2-79
PMU
Block diagram 5-2
BootROM 5-5
Changes to Audo-NG and Audo-F 5-64
Configuration 5-2
Data access overlay operation 1-23
Flash 5-6
Registers
ID 5-28
Tuning Protection 5-5
Port
Temperature compensation 3-136
Ports
Emergency stop control 3-155
Function table 10-5

General port structure 10-3
I/O functions 10-5
Output register Pn_OUT 3-87
Pad driver control 10-16, 10-20
Pad driver mode selection 10-16
Port 0 10-27
Function table 10-28, 10-102, 10-142
Register overview 10-32, 10-144, 10-155
Port 1 10-33
Function table 10-34, 10-153
Register overview 10-37
Port 10 10-96
Function table 10-96
Register overview 10-98
Port 11 10-101
Function table 10-102
Register overview 10-106
Port 12 10-107
Function table 10-108
Register overview 10-109
Port 13 10-111
Function table 10-112
Register overview 10-117
Port 14 10-118
Function table 10-119
Register overview 10-124
Port 15 10-125
Function table 10-126
Register overview 10-131
Port 16 10-132
Function table 10-133
Register overview 10-137
Port 17 10-141
Port 18 10-152
Port 2 10-39
Function table 10-39
Register overview 10-44
Port 3 10-48
Function table 10-48
Register overview 10-54
Port 4 10-55
Function table 10-55
Register overview 10-60
Port 5 10-62
Function table 10-64
Register overview 10-69
Port 6 10-70
Function table 10-71
Register overview 10-75
Port 7 10-77
Function table 10-78
Register overview 10-80
Port 8 10-81
Function table 10-82, 10-96
Register overview 10-85
Port 9 10-86
Function table 10-87
Register overview 10-92
Port control coding 10-14
Registers 10-7, 10-63
Emergency stop register 10-24
Input register 10-25
Input/output control registers 3-84, 10-11, 10-145
Output modification register 10-22
Output register 10-21
Pad driver mode register 10-16, 10-20
Power Management
Register PMCSR **3-122**
Power management 3-120
Idle mode 3-121
Mode definitions 3-120
Sleep mode 3-122
Processor subsystem
Core debug registers 2-62
CPU
Block diagram 2-4
CSFRs 2-20
Execution unit 2-6
Features 2-2, 2-8
General purpose register file 2-7
Implementation-specific features 2-2

Instruction fetch unit 2-5
Registers 2-19
Data cache 2-17
Data side memories 2-16
Data tag 2-17
Error handling 2-13
General purpose registers 2-30
Implementation-specific features 2-10
Instruction cache 2-15
Instruction timing 2-66
Interrupt system 2-12
Local data RAM 2-16
Memory protection registers 2-33
PMI block diagram 2-79
Program side memories 2-14
Program tag 2-15
Scratchpad RAM 2-14
see also CPU
Subsystem block diagram 2-1

R

Register
MMU_ASI 2-25
PCON 2-85
Reset 3-68
Module behavior 3-69
Registers
RSTCNTCON **3-78**
SCU_ARSTDIS **3-80**
SCU_RSTCON **3-78**
SCU_RSTSTAT **3-75**
SWRSTCON **3-81**

S

SBCU
Registers
SBCU_CON **4-83**
SBCU_DBADR! **4-93**
SBCU_DBADR2 **4-93**
SBCU_DBADRT **4-97**
SBCU_DBBOS **4-94**
SBCU_DBBOST **4-98**
SBCU_DBCNTL **4-88**
SBCU_DBDAT **4-100**
SBCU_DBGRNT **4-91**
SBCU_DGNTT **4-95**
SBCU_EADD **4-86**
SBCU_ECON **4-84**
SBCU_EDAT **4-87**
SBCU_ID **4-82**
SBCU_SRC **4-102**
SBCU Control Registers Offset addresses 4-80
SCU
Miscellaneous registers
SCU_CHIPID **3-183**
SCU_ID **3-184**
SCU_MANID **3-185**
SCU_RTID **3-185**
Registers
SCU_DTSCON **3-137**
SCU_DTSSTAT **3-138**
SDMA 13-2
Control Registers Offset addresses 13-41
Registers
ADRCR0x **13-72**
CHCR0x **13-65**
CHICR0x **13-70**
CHRSTR **13-51**
CHSR0x **13-69**
CLRE **13-59**
DADR0x **13-78**
DAMAX0x **13-81**
DAMIN0x **13-81**
EER **13-55**
ERRSR **13-57**
GINTR **13-50**
HTREQ **13-54**
ID **13-46**
INTSR **13-60**
ME0PR **13-64**
ME0R **13-64**
MESR **13-63**
OCDSR **13-47**
RDCRC0x **13-83**

SADR0x **13-77**
SAMAX0x **13-80**
SAMIN0x **13-80**
SCRC0x **13-82**
SDCRC0x **13-82**
SDMA_SRCx **13-94**
SHADR0x **13-79**
STREQ **13-53**
SUSPMR **13-49**
TRSR **13-52**
WRPSR **13-61**
SDMA Principle 13-5
SFI bridge 4-64
Sleep mode 3-122
SRI
Terms **4-4**
SSC
Baud rate generation 21-14, 21-48, 22-34
Baud rate generation formulas 21-50, 22-35
Block diagram 21-4
Chip select generation 21-17
Continuous transfer 21-10
DMA request outputs 21-46
Error detection 21-20
Full-duplex operation 21-6
Half-duplex operation 21-9
Interrupts 21-20
Module implementation 21-43, 22-30
DMA request outputs 21-46
Interrupt registers 21-58, 22-39
Module clock control 21-48, 22-34
Port control 21-53
Parity Mode 21-11
Registers 3-187, 21-27, 22-8
Address map 21-59, 22-40
BR **21-41**, **22-23**
CON **21-31**, **22-13**
EFM **21-36**, **22-18**
ID **21-28**
Offset addresses 21-28, 22-9
Overview 21-27, 22-8, 22-40
PISEL **21-29**, **22-11**
RB **21-42**, **22-24**, **22-26**
SSOC **21-38**, **22-20**
STAT **21-34**, **22-16**, **22-27**, **22-28**, **22-29**
TB **21-42**, **22-24**, **22-25**
Slave select input operation 21-16
Slave select output operation 21-17
SSCG
Registers
ID **22-10**
STM, see “System timer” 17-1
System Peripheral Bus 4-65
System timer
Block diagram 1-16, 17-3
Compare register operation 17-5
Implementation details 17-21
Interrupt control 17-6
On-chip interconnections 17-21
Operation 17-1
Overview 17-1
Registers
Address map 17-21
Offset addresses 17-8
Overview 17-7
STM_CAP **17-14**
STM_CLC **17-9**
STM_CMCON **17-15**
STM_CMPx **17-14**
STM_ICR **17-17**
STM_ID **17-10**
STM_ISRR **17-19**
STM_SRCx **17-20**
STM_TIM0 **17-11**
STM_TIM1 **17-11**
STM_TIM2 **17-12**
STM_TIM3 **17-12**
STM_TIM4 **17-12**
STM_TIM5 **17-13**
STM_TIM6 **17-13**
Resolutions and ranges 17-4

T

temperature measurement 3-136
Timer 30-2, 30-37
  Auxiliary Timer 30-15, 30-46
  Concatenation 30-25, 30-53
  Core Timer 30-4, 30-39
  Counter Mode (GPT1) 30-10, 30-45
  Gated Mode (GPT1) 30-9
  Gated Mode (GPT2) 30-44
  Incremental Interface Mode (GPT1) 30-11
  Mode (GPT1) 30-8
  Mode (GPT2) 30-43
TTCAN, see “CAN”
Tuning Protection 5-5

W

Watchdog Timer
  Period calculation 3-145
Watchdog timer 3-139–3-154
  During power-saving modes 3-148
  Endinit function 3-140
  Features 3-139
  Modify access to WDT_CON0 3-143
  Operating modes
    Disable mode 3-146
    Normal mode 3-146
    Prewarning mode 3-146
    Time-out mode 3-145
  Overview 3-139
  Registers 3-149
    WDT_CON0 **3-149**
    WDT_CON1 **3-151**
    WDT_SR **3-152**
  Servicing 3-147
WDT
  Operating Modes 3-145
WDT, see “Watchdog timer”

X

XBAR_SRI
  Registers
    XBAR_ARBCON **4-42**
    XBAR_DBADD **4-55**
    XBAR_DBCON **4-52**
    XBAR_DBMADD **4-59**
    XBAR_DBSAT **4-35**
    XBAR_DMADD **4-59**
    XBAR_ERR **4-51**
    XBAR_ERRADDR **4-50**
    XBAR_EXTCON **4-40**
    XBAR_ID **4-34**
    XBAR_IDINTEN **4-39**
    XBAR_IDINTSAT **4-37**
    XBAR_INTSAT **4-36**
    XBAR_PRIOH **4-44**
    XBAR_PRIOL **4-44**
    XBAR_SRC **4-63**
XBAR_SRI Control Registers Offset addresses 4-28

Register Index

A

A0 2-31
A1 2-31
A10 2-32
A11 2-32
A12 2-32
A13 2-32
A14 2-32
A15 2-32
A2 2-31
A3 2-31
A4 2-31
A5 2-32
A6 2-32
A7 2-32
A8 2-32
A9 2-32
ADC_ALR0 31-84
ADC_APR 31-125
ADC_ASENR 31-47
ADC_BWDCFGR 31-133
ADC_BWDENR 31-132
ADC_CHCTRx 31-81
ADC_CHENPRx 31-88
ADC_CHFCR 31-87
ADC_CHFR 31-86
ADC_CRCRx 31-54
ADC_CRMRx 31-57
ADC_CRPRx 31-56
ADC_EMCTR 31-126
ADC_EVFCR 31-109
ADC_EVFR 31-107
ADC_EVNPR 31-110
ADC_GLOBCFG 31-37
ADC_GLOBCTR 31-34
ADC_GLOBSTR 31-39
ADC_ID 31-32
ADC_INPRx 31-83
ADC_INTR 31-33
ADC_LCBRx 31-85
ADC_Q0Rx 31-70
ADC_QBURx 31-72
ADC_QINRx 31-74
ADC_QMRx 31-65
ADC_QSRx 31-68
ADC_RCRx 31-105
ADC_RESR0 31-100
ADC_RESRD0 31-100
ADC_RESRDx 31-102
ADC_RESRx 31-102
ADC_RNPRx 31-111
ADC_RSIRx 31-29
ADC_RSPRx 31-48
ADC_SYNCTR 31-130
ADC_VFR 31-104
ADC0_CLC 31-25
ADC0_KSCFG 31-26
ADC0_SRCx 31-28
ASC module registers 20-19
ASC0 register address map 20-42
ASC0_BG 20-27, 20-42
ASC0_CLC 20-33, 20-42
ASC0_CON 20-22, 20-42
ASC0_ESRC 20-39, 20-43
ASC0_FDV 20-27, 20-42
ASC0_ID 20-21, 20-42
ASC0_PISEL 20-36, 20-42
ASC0_RBUF 20-29, 20-42
ASC0_RSRC 20-39, 20-42
ASC0_TBSRC 20-39, 20-43
ASC0_TBUF 20-28, 20-42
ASC0_TSRC 20-39, 20-42
ASC0_WHBCON 20-25, 20-42
ASC1 register address map 20-43
ASC1_BG 20-27, 20-43
ASC1_CON 20-22, 20-43
ASC1_ESRC 20-39, 20-44
ASC1_FDV 20-27, 20-43
ASC1_ID 20-21, 20-43
ASC1_PISEL 20-36, 20-43
ASC1_RBUF 20-29, 20-43

ASC1_RSRC 20-39, 20-43
ASC1_TBSRC 20-39, 20-44
ASC1_TBUF 20-28, 20-43
ASC1_TSRC 20-39, 20-43
ASC1_WHBCON 20-25, 20-43

B

BIV 2-20
BMU_CLC 18-30
BMU_CTL 18-33
BMU_FMCTL 18-43
BMU_FMSTS 18-43
BMU_FMTH 18-44
BMU_FULLNESS 18-35
BMU_ID 18-32
BMU_MIECON 18-47
BMU_MIECON2 18-47
BMU_PSET0 18-36
BMU_PSET1 18-39
BMU_PTR 18-34
BMU_SMACON 18-46
BMU_SRC 18-49
BMU_TID 18-42
BTV 2-20

C

CAN_AWDR 24-171
CAN_CLC 24-205
CAN_CYCTMR 24-166
CAN_FDR 24-206
CAN_GMR 24-169
CAN_LGMR 24-170
CAN_LISTi 24-71
CAN_LOR 24-167
CAN_LREFMR 24-165
CAN_LTR 24-162
CAN_MCR 24-69
CAN_MITR 24-70
CAN_MOAMRn 24-110
CAN_MOARn 24-112
CAN_MOCTRn 24-94
CAN_MODATAHn 24-116
CAN_MODATALn 24-115
CAN_module registers 24-61
CAN_MOFCRn 24-104
CAN_MOFGPRn 24-109
CAN_MOIPRn 24-102
CAN_MOSTATn 24-97
CAN_MSIDk 24-74
CAN_MSIMASK 24-75
CAN_MSPNDk 24-73
CAN_NBTRx 24-87
CAN_NCRx 24-76
CAN_NECNTx 24-89
CAN_NFCRx 24-90
CAN_NIPRx 24-84
CAN_NPCRx 24-86
CAN_NSRx 24-80
CAN_PANCTR 24-65
CAN_REFMR 24-164
CAN_SISR 24-198
CAN_SRCm 24-213
CAN_STPTR0 24-195
CAN_STSRH 24-197
CAN_STSRL 24-196
CAN_SYNMR 24-163
CAN_TTCFGR 24-176
CAN_TTCR 24-172
CAN_TTFMR 24-183
CAN_TTIER 24-189
CAN_TTINPR 24-193
CAN_TTIRR 24-185
CAN_TTSR 24-178
CAN_TURR 24-160
CBS_COMDATA 19-16
CBS_ICTSA 19-16
CBS_ICTTA 19-16
CBS_INTMOD 19-16
CBS_IOSR 19-16
CBS_JDPID 19-16
CBS_MCDBBS 19-16
CBS_MCDBBSS 19-16
CBS_MCDSSG 19-16
CBS_MCDSSGC 19-16
CBS_OCNTRL 19-16
CBS_OEC 19-16

CBS_OSTATE 19-16
CBS_SRC 19-16
CCDIER 2-40
CCPIER 2-40
COMPAT 2-21, 2-29
CPM0 2-36
CPM1 2-36
CPM2 2-36
CPM3 2-36
CPU_ID 2-20, 2-26
CPU_SBSRC 2-59, 2-61
CPU_SRC0 2-59
CPU_SRC1 2-59
CPU_SRC2 2-59
CPU_SRC3 2-59
CPU_SRCn 2-60

D

D0 2-30
D1 2-30
D10 2-31
D11 2-31
D12 2-31
D13 2-31
D14 2-31
D15 2-31
D2 2-30
D3 2-30
D4 2-30
D5 2-31
D6 2-31
D7 2-31
D8 2-31
D9 2-31
DIEAR 2-40, 2-53
DIETR 2-41, 2-51
DMA control registers 12-48
DMA_ADRCR0x 12-92
DMA_ADRCR1x 12-92
DMA_CHCR0x 12-85
DMA_CHCR1x 12-85
DMA_CHICR0x 12-90
DMA_CHICR1x 12-90
DMA_CHRSTR 12-59
DMA_CHSR0x 12-89
DMA_CHSR1x 12-89
DMA_CLC 12-125
DMA_CLRE 12-71
DMA_DADR0x 12-98
DMA_DADR1x 12-98
DMA_EER 12-65
DMA_ERRSR 12-68
DMA_GINTR 12-58
DMA_HTREQ 12-63
DMA_ID 12-53
DMA_INTCR 12-77
DMA_INTSR 12-73
DMA_ME0AENR0 12-81
DMA_ME0AENR1 12-81
DMA_ME0ARR0 12-83
DMA_ME0ARR1 12-83
DMA_ME0PR 12-80
DMA_ME0R 12-80
DMA_ME1AENR0 12-81
DMA_ME1AENR1 12-81
DMA_ME1ARR0 12-83
DMA_ME1ARR1 12-83
DMA_ME1PR 12-80
DMA_ME1R 12-80
DMA_MESR 12-78
DMA_MLI0SRC0 12-51, 12-127
DMA_MLI0SRC1 12-51, 12-127
DMA_MLI0SRC2 12-51, 12-127
DMA_MLI0SRC3 12-51, 12-127
DMA_MLI1SRC0 12-51, 12-127
DMA_MLI1SRC1 12-51, 12-127
DMA_OCDSR 12-54
DMA_SADR0x 12-97
DMA_SADR1x 12-97
DMA_SHADR0x 12-99
DMA_SHADR1x 12-99
DMA_SRC0 12-52, 12-126
DMA_SRC1 12-52, 12-126
DMA_SRC2 12-52, 12-126
DMA_SRC3 12-52, 12-126
DMA_SRC4 12-52, 12-126

DMA_SRC5 12-52, 12-126
DMA_SRC6 12-52, 12-126
DMA_SRC7 12-52, 12-126
DMA_STREQ 12-62
DMA_SUSPMR 12-56
DMA_TRSR 12-60
DMA_WRPSR 12-75
DMI_ATR 2-93
DMI_CON 2-93
DMI_STR 2-93
DPM0 2-36
DPM1 2-36
DPM2 2-36
DPM3 2-36

E

EBU Registers 15-153
EBU_ADDRSEL0 15-163
EBU_ADDRSEL1 15-163
EBU_ADDRSEL2 15-163
EBU_ADDRSEL3 15-163
EBU_BUSRAP0 15-172
EBU_BUSRAP1 15-172
EBU_BUSRAP2 15-172
EBU_BUSRAP3 15-172
EBU_BUSRCON0 15-165
EBU_BUSRCON1 15-165
EBU_BUSRCON2 15-165
EBU_BUSRCON3 15-165
EBU_BUSWAP0 15-175
EBU_BUSWAP1 15-175
EBU_BUSWAP2 15-175
EBU_BUSWAP3 15-175
EBU_BUSWCON0 15-169
EBU_BUSWCON1 15-169
EBU_BUSWCON2 15-169
EBU_BUSWCON3 15-169
EBU_CLC 15-156
EBU_DDRNCON 15-190
EBU_DDRNMOD 15-192
EBU_DDRNMOD2 15-194
EBU_DDRNPRLD 15-197
EBU_DDRNSRR 15-196
EBU_DDRNTAG0 15-198
EBU_DDRNTAG1 15-198
EBU_DDRNTAG2 15-198
EBU_DDRNTAG3 15-198
EBU_EXTBOOT 15-161
EBU_ID 15-200
EBU_MODCON 15-158
EBU_SDRMCON 15-178
EBU_SDRMOD 15-180
EBU_SDRMREF 15-183
EBU_SDRSTAT 15-185
EBU_USERCON 15-199
EICR0 3-105
EICR1 3-108
EIFR 3-112
ERAY_ACS 26-11, 26-130
ERAY_CCEV 26-10, 26-120
ERAY_CCSV 26-10, 26-115
ERAY_CLC 26-8, 26-268
ERAY_CREL 26-14, 26-166
ERAY_CUST1 26-8, 26-17
ERAY_CUST3 26-8, 26-20
ERAY_DATA_READ 26-37
ERAY_DATA_WRITE 26-38
ERAY_DED_CON 26-35
ERAY_DEDCON 26-15
ERAY_ECCR 26-15
ERAY_ECCW 26-15
ERAY_EIER 26-9, 26-65
ERAY_EIES 26-9, 26-60
ERAY_EILS 26-8, 26-52
ERAY_EIR 26-8, 26-41
ERAY_ENDN 26-14, 26-168
ERAY_ESIDnn (nn = 01-15) 26-11, 26-133
ERAY_FCL 26-11
ERAY_FCM 26-144
ERAY_FRF 26-11, 26-141
ERAY_FRFM 26-11, 26-143
ERAY_FSR 26-12, 26-149
ERAY_GTUC01 26-10, 26-103
ERAY_GTUC02 26-10, 26-104
ERAY_GTUC03 26-10, 26-105

ERAY_GTUC04 26-10, 26-106
ERAY_GTUC05 26-10, 26-107
ERAY_GTUC06 26-10, 26-108
ERAY_GTUC07 26-10, 26-109
ERAY_GTUC08 26-10, 26-110
ERAY_GTUC09 26-10, 26-111
ERAY_GTUC10 26-10, 26-112
ERAY_GTUC11 26-10, 26-113
ERAY_IBCM 26-14, 26-175
ERAY_IBCR 26-14, 26-177
ERAY_IBUSYSRC 26-13, 26-279
ERAY_ID 26-8, 26-16
ERAY_ILE 26-9, 26-80
ERAY_INT0SRC 26-14, 26-279
ERAY_INT1SRC 26-14, 26-279
ERAY_LCK 26-8, 26-39
ERAY_LDTS 26-11, 26-148
ERAY_MBS 26-14, 26-186
ERAY_MBSC0SRC 26-13, 26-279
ERAY_MBSC1 26-12, 26-162
ERAY_MBSC1SRC 26-13, 26-279
ERAY_MBSC2 26-12, 26-163
ERAY_MBSC3 26-12, 26-164
ERAY_MBSC4 26-12, 26-165
ERAY_MHDC 26-9, 26-102
ERAY_MHDF 26-12, 26-151
ERAY_MHDS 26-11, 26-145
ERAY_MRC 26-11, 26-138
ERAY_MSIC1 26-13, 26-274
ERAY_MSIC2 26-13, 26-275
ERAY_MSIC3 26-13, 26-276
ERAY_MSIC4 26-13, 26-277
ERAY_MTCCV 26-11, 26-122
ERAY_NDAT0SRC 26-13, 26-279
ERAY_NDAT1 26-12, 26-158
ERAY_NDAT1SRC 26-13, 26-279
ERAY_NDAT2 26-12, 26-159
ERAY_NDAT3 26-12, 26-160
ERAY_NDAT4 26-12, 26-161
ERAY_NDIC1 26-12, 26-270
ERAY_NDIC2 26-12, 26-271
ERAY_NDIC3 26-12, 26-272
ERAY_NDIC4 26-13, 26-273
ERAY_NEMC 26-9, 26-98
ERAY_NMVx (x = 1-3) 26-11, 26-137
ERAY_OBCM 26-14, 26-191
ERAY_OBCR 26-15, 26-194
ERAY_OBUSYSRC 26-13, 26-279
ERAY_OCV 26-11, 26-124
ERAY_OSIDnn (nn = 01-15) 26-11, 26-135
ERAY_PRTC1 26-9, 26-99
ERAY_PRTC2 26-9, 26-101
ERAY_RCV 26-11, 26-123
ERAY_RDDSnn (nn = 01-64) 26-14, 26-179
ERAY_RDHS1 26-14, 26-180
ERAY_RDHS2 26-14, 26-182
ERAY_RDHS3 26-14, 26-184
ERAY_SCV 26-10, 26-121
ERAY_SEC_CON 26-31
ERAY_SECCON 26-15
ERAY_SED_CON 26-33
ERAY_SEDCON 26-15
ERAY_SFS 26-11, 26-125
ERAY_SIER 26-9, 26-75
ERAY_SIES 26-9, 26-70
ERAY_SILS 26-56
ERAY_SIR 26-8, 26-47
ERAY_STPW1 26-9, 26-85
ERAY_STPW2 26-9, 26-87
ERAY_SUCC1 26-9, 26-88
ERAY_SUCC2 26-9, 26-96
ERAY_SUCC3 26-9, 26-97
ERAY_SWINIT 26-127
ERAY_SWNIT 26-11
ERAY_T0C 26-9, 26-81
ERAY_T1C 26-9, 26-83
ERAY_TEST1 26-8, 26-23
ERAY_TEST2 26-8, 26-28
ERAY_TINT0SRC 26-13, 26-279
ERAY_TINT1SRC 26-13, 26-279
ERAY_TXRQ1 26-12, 26-154
ERAY_TXRQ2 26-12, 26-155
ERAY_TXRQ3 26-12, 26-156
ERAY_TXRQ4 26-12, 26-157

ERAY_WRDSnn (nn = 01-64) 26-14, 26-169
ERAY_WRHS1 26-14, 26-170
ERAY_WRHS2 26-14, 26-173
ERAY_WRHS3 26-14, 26-174
ESRCFG0 3-84
ESRCFG1 3-84

F

FADC_ACRx 32-52
FADC_ALR 32-46
FADC_CFGRx 32-48
FADC_CLC 32-30
FADC_CRR0 32-58
FADC_CRRn 32-58
FADC_CRSR 32-35
FADC_FCR0 32-55
FADC_FCR1 32-55
FADC_FCRn 32-55
FADC_FDR 32-31
FADC_FMR 32-37
FADC_FRRn 32-62
FADC_GCR 32-42
FADC_ID 32-33
FADC_IRR10 32-60, 32-62, 32-63
FADC_IRR20 32-60, 32-62, 32-63
FADC_IRR30 32-60, 32-62, 32-63
FADC_IRRyn 32-60
FADC_NCTR 32-39
FADC_RCH0 32-54
FADC_RCH1 32-54
FADC_RCH2 32-54
FADC_RCH3 32-54
FADC_RCHx 32-54
FADC_SFRRn 32-63
FADC_SRCn 32-34
FCE control registers 14-15
FCE_CFGm 14-22
FCE_CHECKm 14-25
FCE_CLC 14-17
FCE_CRCm 14-26
FCE_CTRm 14-27
FCE_ID 14-20
FCE_IRm 14-21
FCE_LENGTHm 14-25
FCE_RESm 14-21
FCE_SRC 14-18
FCE_STSm 14-24
FCX 2-21
Flash module registers 5-30
FLASH0_ID 5-47
FLASH1_ID 5-48
FLASHx_ECCR 5-61
FLASHx_ECCW 5-60
FLASHx_FCON 5-41
FLASHx_FSR 5-32
FLASHx_MARD 5-51
FLASHx_MARP 5-50
FLASHx_PROCON0 5-52
FLASHx_PROCON1 5-55
FLASHx_PROCON2 5-58
FLASHx_RDBCFG0 5-46
FLASHx_RDBCFG1 5-46
FLASHx_RDBCFG2 5-46
FLASHx_SEMA 5-49
FLASHx_SHEBOOT0-2 5-62
FLASHx_XFSR 5-39
FMR 3-112
FPU_ID 2-38, 2-39
FPU_TRAP_CON 2-38
FPU_TRAP_OPC 2-38
FPU_TRAP_PC 2-38
FPU_TRAP_SRC1 2-38
FPU_TRAP_SRC2 2-38
FPU_TRAP_SRC3 2-38

G

GPT12E_CAPREL 30-64
GPT12E_ID 30-71
GPT12E_PISEL 30-68
GPT12E_SRC0 30-35
GPT12E_SRC1 30-35
GPT12E_SRC2 30-35
GPT12E_SRC3 30-66
GPT12E_SRC4 30-66
GPT12E_SRC5 30-66

GPT12E_T2 30-34
GPT12E_T2CON 30-15, 30-17
GPT12E_T3 30-34
GPT12E_T3CON 30-4
GPT12E_T4 30-34
GPT12E_T5 30-64
GPT12E_T5CON 30-46
GPT12E_T6 30-64
GPT12E_T6CON 30-39
GPTA0_CKBCTR 28-185
GPTA0_CLC 28-300
GPTA0_DBGCTR 28-305
GPTA0_DCMCAVk 28-175
GPTA0_DCMCOVk 28-176
GPTA0_DCMCTRk 28-173
GPTA0_DCMTIMk 28-175
GPTA0_EDCTR 28-303
GPTA0_FDR 28-301
GPTA0_FPCCTRk 28-168
GPTA0_FPCSTAT 28-167
GPTA0_FPCTIMk 28-170
GPTA0_GIMCRH 28-217
GPTA0_GIMCRL 28-215
GPTA0_GTCCTRk 28-187, 28-189
GPTA0_GTCTRk 28-182
GPTA0_GTCXRk 28-191
GPTA0_GTREVk 28-184
GPTA0_GTTIMk 28-183
GPTA0_LIMCRH 28-221
GPTA0_LIMCRL 28-219
GPTA0_LTCCTR63 28-204
GPTA0_LTCCTRk 28-192, 28-195
GPTA0_LTCXR63 28-206
GPTA0_LTCXRk 28-205
GPTA0_MMXCTR00 28-291
GPTA0_MMXCTR01 28-291
GPTA0_MMXCTR10 28-292
GPTA0_MMXCTR11 28-293
GPTA0_MRACTL 28-207
GPTA0_MRADIN 28-208
GPTA0_MRADOUT 28-209
GPTA0_OMCRH 28-212
GPTA0_OMCRL 28-210
GPTA0_OTMCR 28-214
GPTA0_PDLCTR 28-171
GPTA0_PLLCNT 28-179
GPTA0_PLLCTR 28-177
GPTA0_PLLDTR 28-181
GPTA0_PLLMTI 28-178
GPTA0_PLLREV 28-180
GPTA0_PLLSTP 28-179
GPTA0_SRCk 28-307
GPTA0_SRNR 28-232
GPTA0_SRSC0 28-223
GPTA0_SRSC1 28-226
GPTA0_SRSC2 28-228
GPTA0_SRSC3 28-230
GPTA0_SRSS0 28-225
GPTA0_SRSS1 28-227
GPTA0_SRSS2 28-229
GPTA0_SRSS3 28-231
GPTA1_CKBCTR 28-185
GPTA1_DCMCAVk 28-175
GPTA1_DCMCOVk 28-176
GPTA1_DCMCTRk 28-173
GPTA1_DCMTIMk 28-175
GPTA1_FPCCTRk 28-168
GPTA1_FPCSTAT 28-167
GPTA1_FPCTIMk 28-170
GPTA1_GIMCRH 28-217
GPTA1_GIMCRL 28-215
GPTA1_GTCCTRk 28-187, 28-189
GPTA1_GTCTRk 28-182
GPTA1_GTCXRk 28-191
GPTA1_GTREVk 28-184
GPTA1_GTTIMk 28-183
GPTA1_LIMCRH 28-221
GPTA1_LIMCRL 28-219
GPTA1_LTCCTR63 28-204
GPTA1_LTCCTRk 28-192, 28-195
GPTA1_LTCXR63 28-206
GPTA1_LTCXRk 28-205
GPTA1_MRACTL 28-207
GPTA1_MRADIN 28-208
GPTA1_MRADOUT 28-209
GPTA1_OMCRH 28-212

GPTA1_OMCRL 28-210
GPTA1_OTMCR 28-214
GPTA1_PDLCTR 28-171
GPTA1_PLLCNT 28-179
GPTA1_PLLCTR 28-177
GPTA1_PLLDTR 28-181
GPTA1_PLLMTI 28-178
GPTA1_PLLREV 28-180
GPTA1_PLLSTP 28-179
GPTA1_SRCk 28-307
GPTA1_SRNR 28-232
GPTA1_SRSC0 28-223
GPTA1_SRSC1 28-226
GPTA1_SRSC2 28-228
GPTA1_SRSC3 28-230
GPTA1_SRSS0 28-225
GPTA1_SRSS1 28-227
GPTA1_SRSS2 28-229
GPTA1_SRSS3 28-231

I

ICR 2-21, 2-23, 16-8
IGCR0 3-114
IGCR1 3-117
ISP 2-21

L

LCX 2-21
LMU_CLC 6-5
LMU_MEMCON 6-6
LMU_MODID 6-9
LTCA2_LIMCRH 28-272
LTCA2_LIMCRL 28-271
LTCA2_LTCCTR31 28-261
LTCA2_LTCCTRk 28-252
LTCA2_LTCXR31 28-263
LTCA2_LTCXRk 28-263
LTCA2_MRACTL 28-264
LTCA2_MRADIN 28-266
LTCA2_MRADOUT 28-266
LTCA2_OMCRH 28-269
LTCA2_OMCRL 28-268
LTCA2_SRCk 28-307
LTCA2_SRSC2 28-228
LTCA2_SRSC3 28-230
LTCA2_SRSS2 28-229
LTCA2_SRSS3 28-231

M

MCHK_CRCx 12-136
MCHK_ID 12-133
MCHK_IRx 12-135
MCHK_RRx 12-135
MCHK_WR 12-136
Memory Checker Control Registers 12-132
MIECON 2-40, 2-42, 2-44
MLI module registers 27-78
MLI0 register address map 27-139
MLI0_AER0 27-90, 27-141
MLI0_AER1 27-90, 27-142
MLI0_ARR0 27-91, 27-142
MLI0_ARR1 27-91, 27-142
MLI0_FDR 27-79, 27-139
MLI0_GINTR 27-83, 27-141
MLI0_ID 27-139
MLI0_OICR 27-86, 27-141
MLI0_RADRR 27-118, 27-141
MLI0_RCR 27-113, 27-140
MLI0_RDATAR 27-119, 27-141
MLI0_RIER 27-120, 27-141
MLI0_RINPR 27-125, 27-141
MLI0_RISR 27-123, 27-141
MLI0_RP0BAR 27-117, 27-140
MLI0_RP0STATR 27-116, 27-141
MLI0_RP1BAR 27-117, 27-140
MLI0_RP1STATR 27-116, 27-141
MLI0_RP2BAR 27-117, 27-140
MLI0_RP2STATR 27-116, 27-141
MLI0_RP3BAR 27-117, 27-140
MLI0_RP3STATR 27-116, 27-141
MLI0_SCR 27-84, 27-141
MLI0_TCBAR 27-106, 27-140
MLI0_TCMDR 27-99, 27-139
MLI0_TCR 27-92, 27-139
MLI0_TDRAR 27-104, 27-140

MLI0_TIER 27-107, 27-141
MLI0_TINPR 27-111, 27-141
MLI0_TISR 27-109, 27-141
MLI0_TP0AOFR 27-103, 27-139
MLI0_TP0BAR 27-105, 27-140
MLI0_TP0DATAR 27-104, 27-140
MLI0_TP0STATR 27-97, 27-139
MLI0_TP1AOFR 27-103, 27-139
MLI0_TP1BAR 27-105, 27-140
MLI0_TP1DATAR 27-104, 27-140
MLI0_TP1STATR 27-97, 27-139
MLI0_TP2AOFR 27-103, 27-139
MLI0_TP2BAR 27-105, 27-140
MLI0_TP2DATAR 27-104, 27-140
MLI0_TP2STATR 27-97, 27-139
MLI0_TP3AOFR 27-103, 27-140
MLI0_TP3BAR 27-105, 27-140
MLI0_TP3DATAR 27-104, 27-140
MLI0_TP3STATR 27-97, 27-139
MLI0_TRSTATR 27-101, 27-139
MLI0_TSTATR 27-95, 27-139
MLI1 register address map 27-142
MLI1_AER0 27-90, 27-145
MLI1_AER1 27-90, 27-145
MLI1_ARR0 27-91, 27-145
MLI1_ARR1 27-91, 27-145
MLI1_FDR 27-79, 27-142
MLI1_GINTR 27-83, 27-144
MLI1_ID 27-142
MLI1_OICR 27-86, 27-145
MLI1_RADRR 27-118, 27-144
MLI1_RCR 27-113, 27-143
MLI1_RDATAR 27-119, 27-144
MLI1_RIER 27-120, 27-144
MLI1_RINPR 27-125, 27-144
MLI1_RISR 27-123, 27-144
MLI1_RP0BAR 27-117, 27-143
MLI1_RP0STATR 27-116, 27-144
MLI1_RP1BAR 27-117, 27-143
MLI1_RP1STATR 27-116, 27-144
MLI1_RP2BAR 27-117, 27-144
MLI1_RP2STATR 27-116, 27-144
MLI1_RP3BAR 27-117, 27-144
MLI1_RP3STATR 27-116, 27-144
MLI1_SCR 27-84, 27-144
MLI1_TCBAR 27-106, 27-143
MLI1_TCMDR 27-99, 27-142
MLI1_TCR 27-92, 27-142
MLI1_TDRAR 27-104, 27-143
MLI1_TIER 27-107, 27-144
MLI1_TINPR 27-111, 27-144
MLI1_TISR 27-109, 27-144
MLI1_TP0AOFR 27-103, 27-142
MLI1_TP0BAR 27-105, 27-143
MLI1_TP0DATAR 27-104, 27-143
MLI1_TP0STATR 27-97, 27-142
MLI1_TP1AOFR 27-103, 27-143
MLI1_TP1BAR 27-105, 27-143
MLI1_TP1DATAR 27-104, 27-143
MLI1_TP1STATR 27-97, 27-142
MLI1_TP2AOFR 27-103, 27-143
MLI1_TP2BAR 27-105, 27-143
MLI1_TP2DATAR 27-104, 27-143
MLI1_TP2STATR 27-97, 27-142
MLI1_TP3AOFR 27-103, 27-143
MLI1_TP3BAR 27-105, 27-143
MLI1_TP3DATAR 27-104, 27-143
MLI1_TP3STATR 27-97, 27-142
MLI1_TRSTATR 27-101, 27-142
MLI1_TSTATR 27-95, 27-142
MMU_CON 2-20, 2-24
MSC module registers 23-37
MSC0 register address map 23-75
MSC0_CLC 23-67, 23-75
MSC0_DC 23-59, 23-75
MSC0_DD 23-59, 23-75
MSC0_DSC 23-41, 23-75
MSC0_DSDSH 23-47, 23-75
MSC0_DSDSL 23-46, 23-75
MSC0_DSS 23-44, 23-75
MSC0_ESR 23-48, 23-75
MSC0_FDR 23-68, 23-75
MSC0_ICR 23-49, 23-76
MSC0_ID 23-38, 23-75, 27-82
MSC0_ISC 23-54, 23-76
MSC0_ISR 23-52, 23-76

MSC0_OCR 23-56, 23-76
MSC0_SRC0 23-74, 23-76
MSC0_SRC1 23-74, 23-76
MSC0_UD0 23-60, 23-75
MSC0_UD1 23-60, 23-75
MSC0_UD2 23-60, 23-76
MSC0_UD3 23-60, 23-76
MSC0_USR 23-39, 23-75
MSC1 register address map 23-76
MSC1_CLC 23-67, 23-76
MSC1_DC 23-59, 23-77
MSC1_DD 23-59, 23-77
MSC1_DSC 23-41, 23-76
MSC1_DSDSH 23-47, 23-77
MSC1_DSDSL 23-46, 23-77
MSC1_DSS 23-44, 23-77
MSC1_ESR 23-48, 23-77
MSC1_FDR 23-68, 23-76
MSC1_ICR 23-49, 23-77
MSC1_ID 23-38, 23-76, 27-82
MSC1_ISC 23-54, 23-77
MSC1_ISR 23-52, 23-77
MSC1_OCR 23-56, 23-77
MSC1_SRC0 23-74, 23-78
MSC1_SRC1 23-74, 23-78
MSC1_UD0 23-60, 23-77
MSC1_UD1 23-60, 23-77
MSC1_UD2 23-60, 23-77
MSC1_UD3 23-60, 23-77
MSC1_USR 23-39, 23-76

O

OVC_OCON 7-14, 7-16
OVC_OMASKx 7-12
OVC_OTARx 7-11
OVC_RABRx 7-9
Overlay memory control registers 7-7

P

P0_ESR 10-24
P0_IN 10-25, 10-148
P0_IOCR0 10-11, 10-145
P0_IOCR12 10-14, 10-147
P0_IOCR4 10-12, 10-146
P0_IOCR8 10-13, 10-146
P0_OMR 10-22
P0_OUT 10-21
P0_PDR0 10-18
P0_PDR1 10-19
P1_ESR 10-24
P1_IN 10-25, 10-148
P1_IOCR0 10-11, 10-145
P1_IOCR12 10-14, 10-147
P1_IOCR4 10-12, 10-146
P1_IOCR8 10-13, 10-146
P1_OMR 10-22
P1_OUT 10-21
P1_PDR0 10-18
P1_PDR1 10-19
P10_IN 10-25, 10-148
P10_IOCR0 10-11
P10_IOCR4 10-12, 10-146
P10_OMR 10-22
P10_OUT 10-21
P10_PDR0 10-100
P11_IN 10-25, 10-148
P11_IOCR0 10-11
P11_IOCR12 10-14
P11_IOCR4 10-12, 10-146
P11_IOCR8 10-13
P11_OMR 10-22
P11_OUT 10-21
P11_PDR0 10-18
P11_PDR1 10-19
P12_IN 10-25
P12_IOCR0 10-11
P12_IOCR4 10-12
P12_OMR 10-22
P12_OUT 10-21
P12_PDR0 10-18
P13_ESR 10-24
P13_IN 10-25
P13_IOCR0 10-11
P13_IOCR12 10-14
P13_IOCR4 10-12
P13_IOCR8 10-13

P13_OMR 10-22
P13_OUT 10-21
P13_PDR0 10-18
P13_PDR1 10-19
P14_ESR 10-24
P14_IN 10-25
P14_IOCR0 10-11
P14_IOCR12 10-14
P14_IOCR4 10-12
P14_IOCR8 10-13
P14_OMR 10-22
P14_OUT 10-21
P14_PDR0 10-18
P14_PDR1 10-19
P15_IN 10-25
P15_IOCR0 10-11
P15_IOCR12 10-14
P15_IOCR4 10-12
P15_IOCR8 10-13
P15_OMR 10-22
P15_OUT 10-21
P15_PDR0 10-18
P15_PDR1 10-19
P16_IN 10-25
P16_IOCR0 10-11
P16_IOCR12 10-138
P16_IOCR4 10-12
P16_IOCR8 10-13
P16_OMR 10-22
P16_OUT 10-21
P16_PDR0 10-18
P16_PDR1 10-140
P17_IN 10-25
P18_IN 10-25
P18_IOCR0 10-11
P18_IOCR4 10-12
P18_OMR 10-22
P18_OUT 10-21
P18_PDR0 10-18
P2_ESR 10-24
P2_IN 10-25, 10-148
P2_IOCR0 10-45, 10-99
P2_IOCR12 10-14, 10-147
P2_IOCR4 10-12, 10-146
P2_IOCR8 10-13, 10-146
P2_OMR 10-22
P2_OUT 10-21
P2_PDR0 10-46
P2_PDR1 10-19
P3_ESR 10-24
P3_IN 10-25, 10-148
P3_IOCR0 10-11
P3_IOCR12 10-14, 10-147
P3_IOCR4 10-12, 10-146
P3_IOCR8 10-13, 10-146
P3_OMR 10-22
P3_OUT 10-21
P3_PDR0 10-18
P3_PDR1 10-19
P4_ESR 10-24
P4_IN 10-25, 10-148
P4_IOCR0 10-11
P4_IOCR12 10-14, 10-147
P4_IOCR4 10-12, 10-146
P4_IOCR8 10-13, 10-146
P4_OMR 10-22
P4_OUT 10-21
P4_PDR0 10-18
P4_PDR1 10-19
P5_ESR 10-24
P5_IN 10-25, 10-148
P5_IOCR0 10-11
P5_IOCR4 10-12, 10-146
P5_IOCR8 10-13, 10-146
P5_OMR 10-22
P5_OUT 10-21
P5_PDR0 10-18
P5_PDR1 10-19
P6_IN 10-25, 10-148
P6_IOCR0 10-11
P6_IOCR12 10-14, 10-147
P6_IOCR4 10-12, 10-146
P6_IOCR8 10-13, 10-146
P6_OMR 10-22
P6_OUT 10-21
P6_PDR0 10-76

P6_PDR1 10-19
P7_IN 10-25, 10-148
P7_IOCR0 10-11
P7_IOCR4 10-12, 10-146
P7_OMR 10-22
P7_OUT 10-21
P7_PDR0 10-18
P8_ESR 10-24
P8_IN 10-25, 10-148
P8_IOCR0 10-11
P8_IOCR4 10-12, 10-146
P8_OMR 10-22
P8_OUT 10-21
P8_PDR0 10-18
P8_PDR1 10-19
P9_ESR 10-24
P9_IN 10-25, 10-148
P9_IOCR0 10-11
P9_IOCR4 10-12, 10-146
P9_IOCR8 10-13, 10-93
P9_OMR 10-22
P9_OUT 10-21
P9_PDR0 10-18
P9_PDR1 10-95
PC 2-20
PCP_CLC 11-67
PCP_CS 11-69
PCP_ES 11-71
PCP_ICON 11-77
PCP_ICR 11-74
PCP_ID 11-68
PCP_ITR 11-76
PCP_SMACON 11-81, 11-82, 11-83, 11-84, 11-85, 11-86, 11-87, 11-91
PCP_SRC0 11-92
PCP_SRC1 11-92
PCP_SRC10 11-96
PCP_SRC11 11-96
PCP_SRC2 11-94
PCP_SRC3 11-94
PCP_SRC4 11-95
PCP_SRC5 11-95
PCP_SRC6 11-95
PCP_SRC7 11-95
PCP_SRC8 11-95
PCP_SRC9 11-96
PCP_SSR 11-79
PCXI 2-20
PDRR 3-113
PIEAR 2-40, 2-49
PIETR 2-40, 2-47
PMI_CON0 2-82, 2-83
PMI_CON1 2-82, 2-84
PMI_CON2 2-82
PMI_STR 2-82
PMU module registers 5-27
PMU0_ID 5-28
PMU1_ID 5-29
PSW 2-20, 2-22

R

RSTCNTCON 3-78

S

SBCU control registers 4-80
SBCU_CON 4-80, 4-83
SBCU_DBADR1 4-81, 4-93
SBCU_DBADR2 4-81, 4-93
SBCU_DBADRT 4-81, 4-97
SBCU_DBBOS 4-81, 4-94
SBCU_DBBOST 4-81, 4-98
SBCU_DBCNTL 4-81, 4-88
SBCU_DBDAT 4-81, 4-100
SBCU_DBGNTT 4-81, 4-95
SBCU_DBGRNT 4-81, 4-91
SBCU_EADD 4-81, 4-86
SBCU_ECON 4-81, 4-84
SBCU_EDAT 4-81, 4-87
SBCU_ID 4-80, 4-82
SBCU_SRC 4-81, 4-102
SCU_ARSTDIS 3-80
SCU_CCUCON0 3-42
SCU_CCUCON1 3-45
SCU_CCUCON2 3-47
SCU_CHIPID 3-183

SCU_DTSCON 3-137
SCU_DTSSTAT 3-138
SCU_ECCCLR 3-134
SCU_ECCCON 3-130
SCU_ECCSTAT 3-132
SCU_EMSR 3-157
SCU_EXTCON 3-49
SCU_FDR 3-51
SCU_ID 3-184
SCU_IN 3-90
SCU_INTCLR 3-164
SCU_INTDIS 3-165
SCU_INTNP 3-167
SCU_INTSET 3-162
SCU_INTSTAT 3-160
SCU_IOCR 3-85
SCU_MANID 3-185
SCU_MEMTEST 3-187
SCU_OMR 3-89
SCU_OSCCON 3-31
SCU_OUT 3-88
SCU_PLLCON0 3-35, 3-40
SCU_PLLCON1 3-37, 3-42
SCU_PLLCON2 3-38
SCU_PLLSTAT 3-33, 3-38
SCU_PMCSR 3-123
SCU_RSTCON 3-78
SCU_RSTSTAT 3-75
SCU_RTID 3-185
SCU_SRC0 3-169, 25-71
SCU_SRC1 3-169, 25-71
SCU_SRC2 3-169, 25-71
SCU_SRC3 3-169, 25-71
SCU_STCON 3-128
SCU_STSTAT 3-126
SCU_SYSCON 3-182
SCU_TRAPCLR 3-177
SCU_TRAPDIS 3-179
SCU_TRAPSET 3-175
SCU_TRAPSTAT 3-172
SDMA
  Registers
    INTCR 13-62
SDMA control registers 13-41
SDMA_ADRCR0x 13-72
SDMA_CHCR0x 13-65
SDMA_CHICR0x 13-70
SDMA_CHRSTR 13-51
SDMA_CHSR0x 13-69
SDMA_CLC 13-92
SDMA_CLRE 13-59
SDMA_DADR0x 13-78
SDMA_DAMAX0x 13-81
SDMA_DAMIN0x 13-81
SDMA_DCRC0x 13-82
SDMA_EER 13-55
SDMA_ERRSR 13-57
SDMA_GINTR 13-50
SDMA_HTREQ 13-54
SDMA_ID 13-46
SDMA_INTCR 13-62
SDMA_INTSR 13-60
SDMA_ME0PR 13-64
SDMA_ME0R 13-64
SDMA_MESR 13-63
SDMA_OCDSR 13-47
SDMA_RDCRC0x 13-83
SDMA_SADR0x 13-77
SDMA_SAMAX0x 13-80
SDMA_SAMIN0x 13-80
SDMA_SCRC0x 13-82
SDMA_SHADR0x 13-79
SDMA_SRC0 13-45, 13-94
SDMA_SRC1 13-45, 13-94
SDMA_SRC2 13-44, 13-94
SDMA_SRC3 13-44, 13-94
SDMA_SRC4 13-44, 13-94
SDMA_SRC5 13-44, 13-94
SDMA_SRC6 13-44, 13-94
SDMA_SRC7 13-44, 13-94
SDMA_STREQ 13-53
SDMA_SUSPMR 13-49
SDMA_TRSR 13-52
SDMA_WRPSR 13-61
SMACON 2-41, 2-55
SSC

Registers
SSOTC 21-39, 22-21
SSC module registers 21-28, 22-9
SSC0 register address map 21-59
SSC0_BR 21-41, 21-59, 22-23
SSC0_CLC 21-51, 21-59, 22-36
SSC0_CON 21-31, 21-59, 22-13
SSC0_EFM 21-36, 21-59, 22-18
SSC0_ESRC 21-58, 21-60
SSC0_FDR 21-52, 21-59, 22-37
SSC0_ID 21-28, 21-59
SSC0_PISEL 21-29, 21-59, 22-11
SSC0_RB 21-42, 21-59, 22-24, 22-26
SSC0_RSRC 21-58, 21-60
SSC0_SSOC 21-38, 22-20
SSC0_SSOTC 21-39, 21-59, 22-21
SSC0_STAT 21-34, 21-59, 22-16, 22-27, 22-28, 22-29
SSC0_TB 21-42, 21-59, 22-24, 22-25
SSC0_TSRC 21-58, 21-59, 22-39
SSC1 register address map 21-60
SSC1_BR 21-41, 21-60, 22-23
SSC1_CLC 21-51, 21-60
SSC1_CON 21-31, 21-60, 22-13
SSC1_EFM 21-36, 21-60, 22-18
SSC1_ESRC 21-58, 21-61
SSC1_FDR 21-52, 21-60
SSC1_ID 21-28, 21-60
SSC1_PISEL 21-29, 21-60, 22-11
SSC1_RB 21-42, 21-60, 22-24, 22-26
SSC1_RSRC 21-58, 21-60
SSC1_SSOC 21-38, 21-60, 22-20
SSC1_SSOTC 21-39, 21-60, 22-21
SSC1_STAT 21-34, 21-60, 22-16, 22-27, 22-28, 22-29
SSC1_TB 21-42, 21-60, 22-24, 22-25
SSC1_TSRC 21-58, 21-60, 22-39
SSC2 register address map 21-61, 21-62
SSC2_BR 21-61
SSC2_CLC 21-51, 21-61
SSC2_CON 21-61
SSC2_EFM 21-61
SSC2_ESRC 21-58, 21-61
SSC2_FDR 21-52, 21-61
SSC2_ID 21-61
SSC2_PISEL 21-61
SSC2_RB 21-61
SSC2_RSRC 21-58, 21-61
SSC2_SSOC 21-61
SSC2_SSOTC 21-61
SSC2_STAT 21-61
SSC2_TB 21-61
SSC2_TSRC 21-58, 21-61
SSC3_BR 21-62
SSC3_CLC 21-51, 21-62
SSC3_CON 21-62
SSC3_EFM 21-62
SSC3_ESRC 21-62
SSC3_FDR 21-52, 21-62
SSC3_ID 21-62
SSC3_PISEL 21-62
SSC3_RB 21-62
SSC3_RSRC 21-62
SSC3_SSOC 21-62
SSC3_SSOTC 21-62
SSC3_STAT 21-62
SSC3_TB 21-62
SSC3_TSRC 21-62
SSCGx_BR 22-41
SSCGx_CLC 22-41
SSCGx_CON 22-41
SSCGx_EFM 22-41
SSCGx_FDR 22-41
SSCGx_GEFM 22-41
SSCGx_GEN 22-41
SSCGx_GSRC 22-41
SSCGx_GSTAT 22-41
SSCGx_ID 22-41
SSCGx_PISEL 22-41
SSCGx_RB 22-41
SSCGx_RBSNAP 22-41
SSCGx_SSOTC 22-41
SSCGx_STAT 22-41
SSCGx_TB 22-41
SSCGx_TB1 22-41
SSCGx_TB1SNAP 22-41

STM register address map 17-22
STM_CAP 17-14, 17-22
STM_CLC 17-9, 17-22
STM_CMCON 17-15, 17-22
STM_CMP0 17-14, 17-22
STM_CMP1 17-14, 17-22
STM_ICR 17-17, 17-22
STM_ID 17-10, 17-22
STM_ISRR 17-19, 17-22
STM_SRC0 17-20, 17-22
STM_SRC1 17-20, 17-22
STM_TIM0 17-11, 17-22
STM_TIM1 17-11, 17-22
STM_TIM2 17-12, 17-22
STM_TIM3 17-12, 17-22
STM_TIM4 17-12, 17-22
STM_TIM5 17-13, 17-22
STM_TIM6 17-13, 17-22
SWRSTCON 3-81
SYSCON 2-20

W

WDT_CON0 3-149
WDT_CON1 3-151
WDT_SR 3-152

X

XBAR_ARBCON 4-42
XBAR_DBADD 4-55
XBAR_DBCON 4-52
XBAR_DBMADD 4-59
XBAR_DBSAT 4-35
XBAR_ERR 4-51
XBAR_ERRADDR 4-50
XBAR_EXTCON 4-40
XBAR_ID 4-34
XBAR_IDINTEN 4-39
XBAR_IDINTSAT 4-37
XBAR_INTSAT 4-36
XBAR_PRIOH 4-44
XBAR_SRC 4-63
XBAR_SRI control registers 4-28

www.infineon.com

Published by Infineon Technologies AG

Doc_Number