(V) Preliminary Specifications
(   ) Final Specifications

Module	12.1" WXGA Color TFT-LCD
Model Name	B121EW07 V0 (HW:0A)

Customer	**Date**

Checked & Approved by

Note: This Specification is subject to change without notice.

Approved by	**Date**

2006/10/15

Prepared by

2006/10/15

MDBU Marketing Division /
AU Optronics corporation

Contents

2. General Description

B121EW07 V0 is a Color Active Matrix Liquid Crystal Display composed of a TFT LCD panel, a driver circuit, and backlight system. The screen format is intended to support the WXGA (1280(H) x 800(V)) screen and 262k colors (RGB 6-bits data driver). All input signals are LVDS interface compatible. Inverter card of backlight is not included.

B121EW07 V0 is designed for a display unit of notebook style personal computer and industrial machine.

2.1 Display Characteristics

The following items are characteristics summary on the table under 25 ℃ condition:

| Items	Unit	Specifications
Screen Diagonal	[mm]	307.9 (12.1W")
Active Area	[mm]	261.12(H) X 163.2(V)
Pixels H x V		1280x3(RGB) x 800
Pixel Pitch	[mm]	0.204X0.204
Pixel Arrangement		R.G.B. Vertical Stripe
Display Mode		Normally White
Typical White Luminance	[cd/m^2]	200 typ. (5 points average) 170 min. (5 points average) (Note1)
Luminance Uniformity		1.25 max. (5 points)
Contrast Ratio		400 min.
Optical Rise Time/Fall Time	[msec]	10/15 typ.
Nominal Input Voltage VDD	[Volt]	+3.3 typ.
Typical Power Consumption	[Watt]	4.0W max.
Weight (without inverter)	[Grams]	215g typ. 230g max
Physical Size	[mm]	275.82x 179.4 x 5.1 max.
Electrical Interface		1 channel LVDS
Surface Treatment		AG, Hardness 3H,
Support Color		Native 262K colors (RGB 6-bit data driver)

Product Specification

Temperature Range			
Operating	[°C]	0 to +50	
Storage (Non-Operating)	[°C]	-40 to +60	
RoHS Compliance		RoHS Compliance	

## 2.2 Optical Characteristics

The optical characteristics are measured under stable conditions at 25℃ (Room Temperature):

Item	Unit	Conditions	Min.	Typ.	Max.	Note
White Luminance LED 20.0mA	[cd/m2]	5 points average	170	200	-	1,2,3
Viewing Angle	[degree] [degree]	Horizontal (Right) CR = 10 (Left)	- -	40 40	- -	2,7
	[degree] [degree]	Vertical (Upper) CR = 10 (Lower)	- -	20 40	- -	
Uniformity		5 Points			1.25	1
Uniformity		13 Points			1.6	
CR: Contrast Ratio			400	-	-	6
Cross talk	%				4	4
Response Time	[msec]	Rising	-	10	15	5
	[msec]	Falling	-	15	20	
	[msec]	Raising + Falling		25	35	
Color / Chromaticity Coordinates (CIE 1931)		Red x	0.560	0.580	0.600	2,7
		Red y	0.320	0.340	0.360	
		Green x	0.290	0.310	0.330	
		Green y	0.530	0.550	0.570	
		Blue x	0.135	0.155	0.175	
		Blue y	0.135	0.155	0.175	
		White x	0.283	0.313	0.343	
		White y	0.299	0.329	0.359	

Note 1: 5 points position (Display area : 261.12mm x 163.2mm)
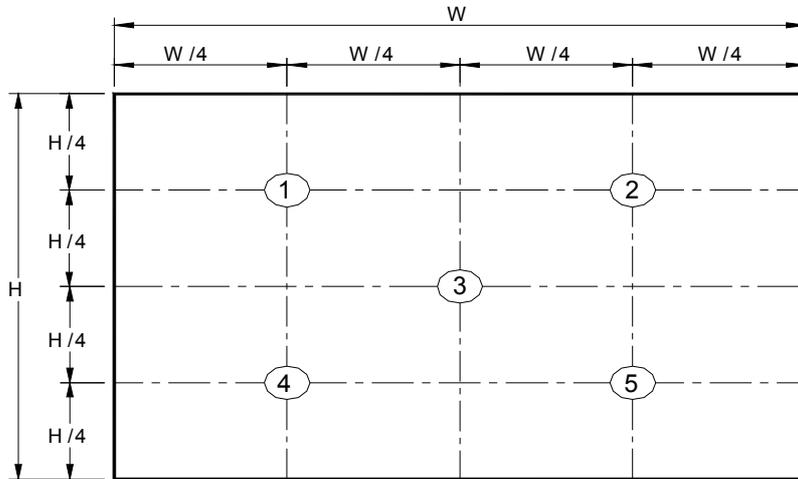

Note 2: 13 points position
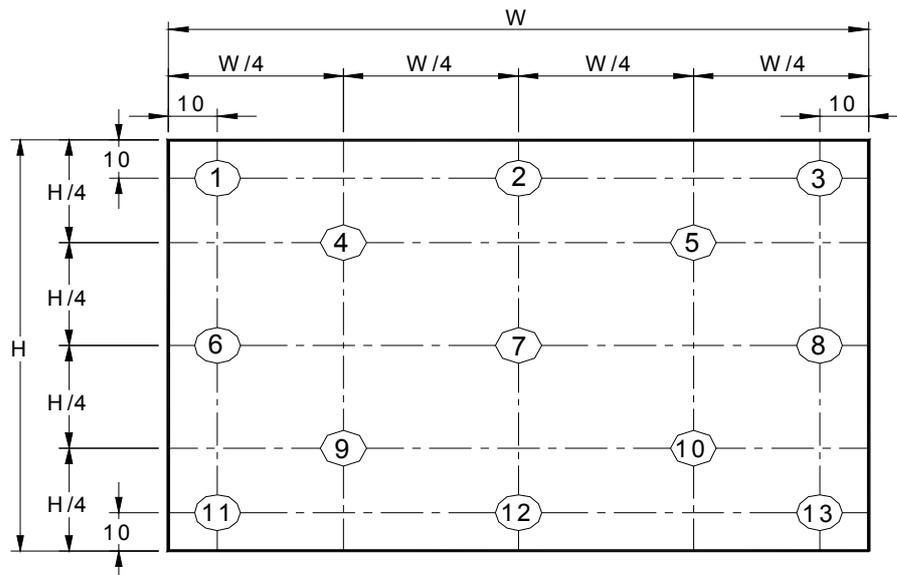
Note 3: The luminance uniformity of 5 and 13 points is defined by dividing the maximum luminance values by the minimum test point luminance

$$\delta_{W5} = \frac{\text{Maximum Brightness of five points}}{\text{Minimum Brightness of five points}}$$

$$\delta_{W13} = \frac{\text{Maximum Brightness of thirteen points}}{\text{Minimum Brightness of thirteen points}}$$

Note 4: Measurement method

The LCD module should be stabilized at given temperature for 30 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 30 minutes in a stable, windless and dark room.
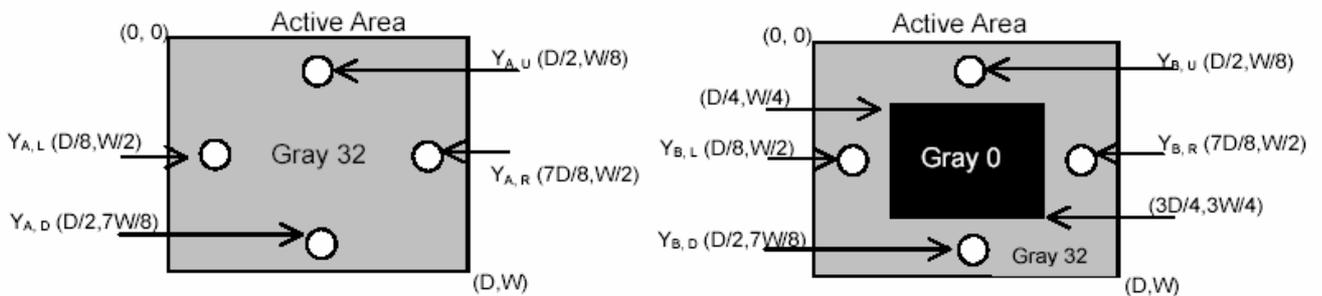
Photo detector

Field=2°

50 cm

LCD Panel

TFT-LCD

Center of the screen
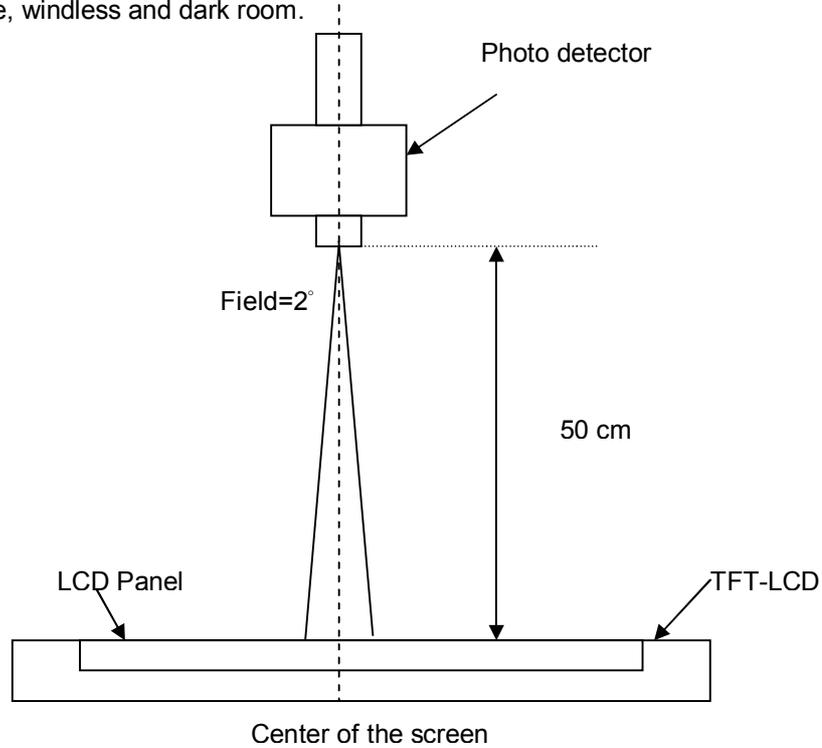
Note 5： Definition of Cross Talk (CT)

$CT = | Y_B - Y_A | / Y_A \times 100$ (%)

Where

Y_A = Luminance of measured location without gray level 0 pattern (cd/m2)

Y_B = Luminance of measured location with gray level 0 pattern (cd/m2)

Note 6: Definition of response time:

The output signals of BM-7 or equivalent are measured when the input signals are changed from "Black" to "White" (falling time) and from "White" to "Black" (rising time), respectively. The response time interval between the 10% and 90% of amplitudes. Refer to figure as below.
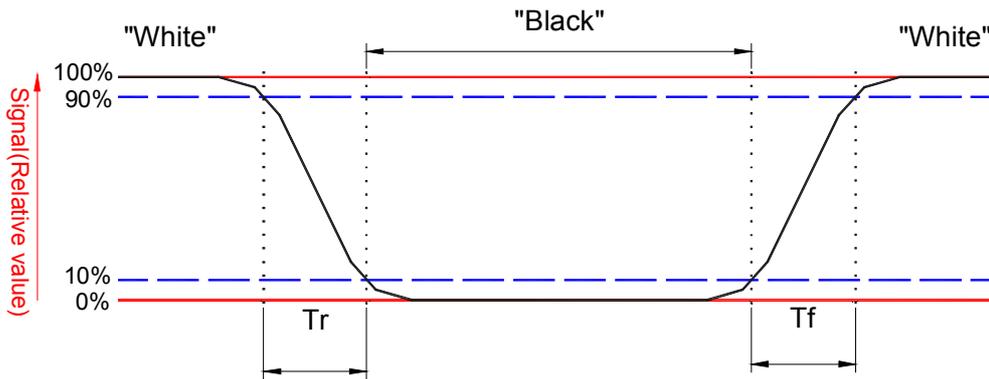
Note 7. Definition of viewing angle

Viewing angle is the measurement of contrast ratio ≥ 10, at the screen center, over a 180° horizontal and 180° vertical range (off-normal viewing angles). The 180° viewing angle range is broken down as follows; 90° (θ) horizontal left and right and 90° (Φ) vertical, high (up) and low (down). The measurement direction is typically perpendicular to the display surface with the screen rotated about its center to develop the desired measurement viewing angle.
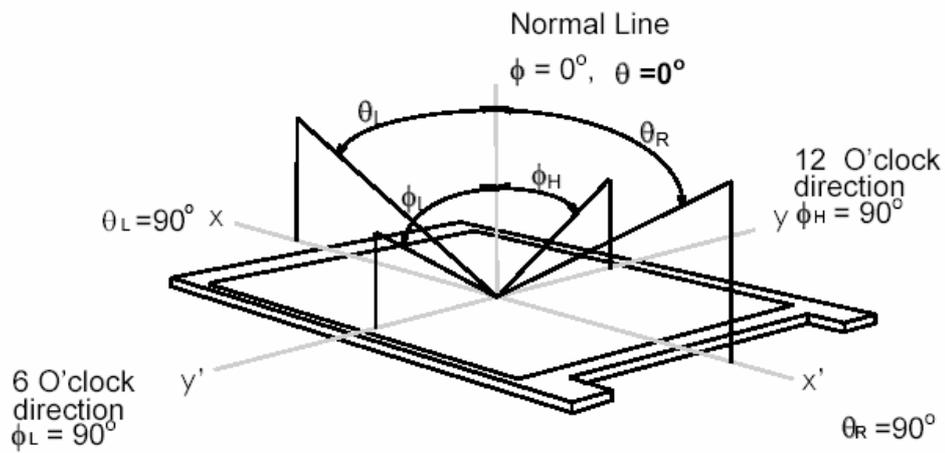
3. Functional Block Diagram

The following diagram shows the functional block of the 12.1 inches wide Color TFT/LCD Module:
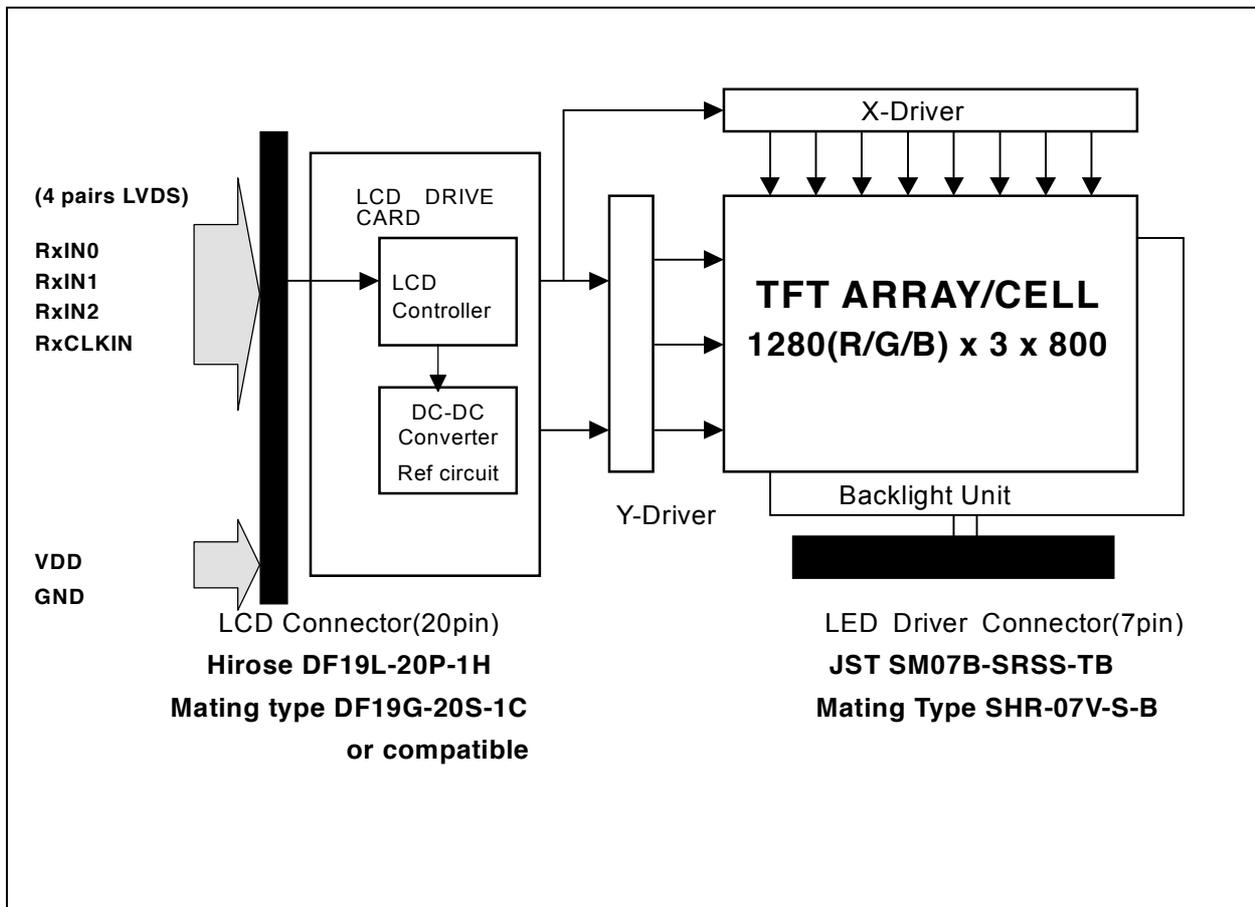
4. Absolute Maximum Ratings

Absolute maximum ratings of the module is as following:

4.1 Absolute Ratings of TFT LCD Module

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive	Vin	-0.3	+4.0	[Volt]	Note 1,2

4.2 Absolute Ratings of Backlight Unit

Item	Symbol	Min	Max	Unit	Conditions
LED current	Id	-	20	[mA] rms	Note 1,2

4.3 Absolute Ratings of Environment

Item	Symbol	Min	Max	Unit	Conditions
Operating Temperature	TOP	0	+50	[^{o}C]	Note 3
Operation Humidity	HOP	5	95	[%RH]	Note 3
Storage Temperature	TST	-40	+60	[^{o}C]	Note 3
Storage Humidity	HST	5	95	[%RH]	Note 3

Note 1: With in Ta (25℃)

Note 2: Permanent damage to the device may occur if exceed maximum values

Note 3: For quality performance, please refer to AUO IIS(Incoming Inspection Standard).
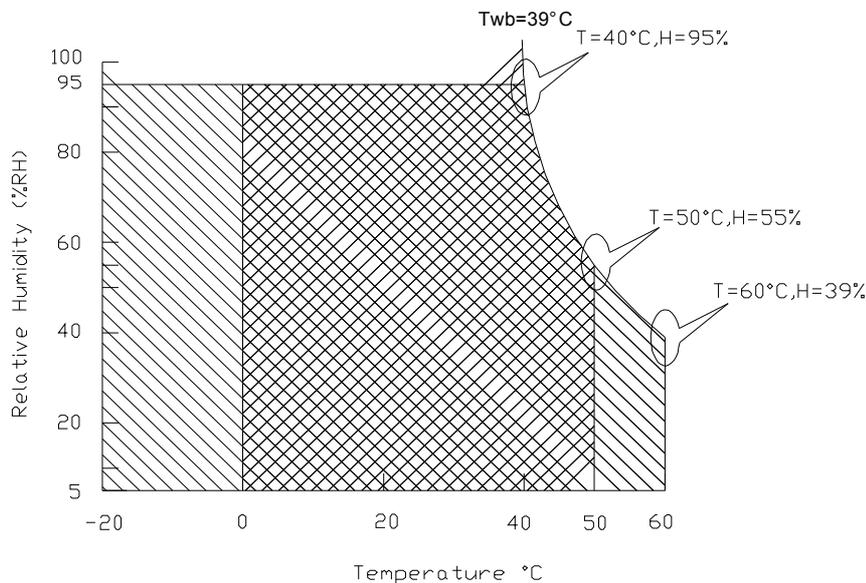
Operating Range [XXXXX] Storage Range [XXXXX + \\\\\]
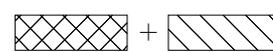
5. Electrical characteristics

5.1 TFT LCD Module

5.1.1 Power Specification

Input power specifications are as follows;

Symble	Parameter	Min	Typ	Max	Units	Condition
VDD	Logic/LCD Drive Voltage	3.0	3.3	3.6	[Volt]	Load Capacitance 20uF
PDD	VDD Power		1.0	1.2	[Watt]	Max:All Black Pattern
IDD	IDD Current		300	360	mA	Max:All Black Pattern
IRush	Inrush Current			1500	mA	
VDDrp	Allowable Logic/LCD Drive Ripple Voltage			100	[mV] p-p	

Note 1 : Measurement conditions:
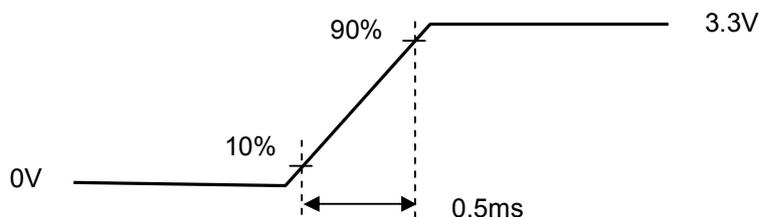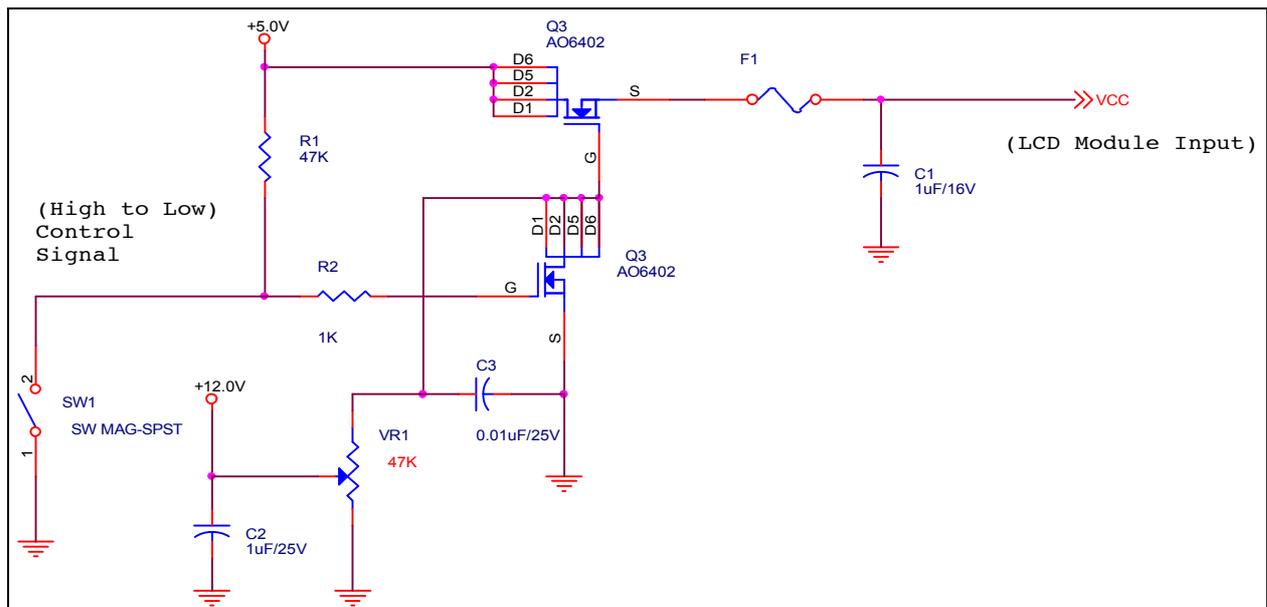
Vin rising time

5.1.2 Signal Electrical Characteristics

Input signals shall be low or Hi-Z state when VDD is off.

It is recommended to refer the specifications of THC63LVDF84A (Thine Electronics Inc.) in detail.

Signal electrical characteristics are as follows;

Parameter	Condition	Min	Max	Unit
V_{th}	Differential Input High Threshold (Vcm=+1.2V)		100	[mV]
V_{tl}	Differential Input Low Threshold (Vcm=+1.2V)	-100		[mV]

Note: LVDS Signal Waveform
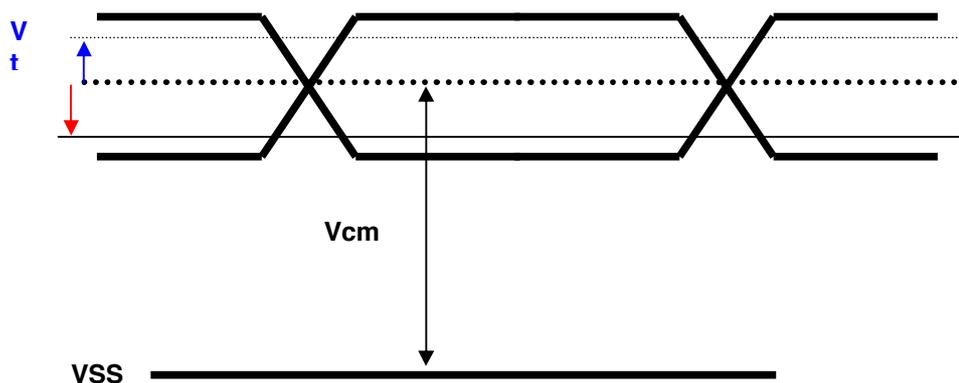
5.2 Backlight Unit

The backlight system is an edge-lighting type with LED (Light Emitting Diode).

The characteristics of the LED are shown in the following table.

Symbol	Parameter	Min.	Typ.	Max.	Unit	Remark
IL	System Input Current	480	280	160	MA	
VL	System Input Voltage	7	12	21	Vdc	
VF	LED Float Voltage	3.0	3.2	3.4	Vdc	
Vtotal	LED total forward voltage	21	22.4	23.8	Vdc	
ILed	LED operate current	120	120	120	mA	
PL	LED Power Consumption	2.5	2.7	2.9	W	
FL1	Input PWM frequency	17	17.5	18	KHz	
FL2	LED dimming frequency	190	200	210	Hz	

6. Signal Characteristic

6.1 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.

6.2 The input data format

| Signal Name	Description	
RED5 RED4 RED3 RED2 RED1 RED0	Red Data 5 (MSB) Red Data 4 Red Data 3 Red Data 2 Red Data 1 Red Data 0 (LSB) Red-pixel Data	Red-pixel Data Each red pixel's brightness data consists of these 6 bits pixel data.
GREEN 5 GREEN 4 GREEN 3 GREEN 2 GREEN 1 GREEN 0	Green Data 5 (MSB) Green Data 4 Green Data 3 Green Data 2 Green Data 1 Green Data 0 (LSB) Green-pixel Data	Green-pixel Data Each green pixel's brightness data consists of these 6 bits pixel data.
BLUE 5 BLUE 4 BLUE 3 BLUE 2 BLUE 1 BLUE 0	Blue Data 5 (MSB) Blue Data 4 Blue Data 3 Blue Data 2 Blue Data 1 Blue Data 0 (LSB) Blue-pixel Data	Blue-pixel Data Each blue pixel's brightness data consists of these 6 bits pixel data.
DTCLK	Data Clock	The typical frequency is 68.9 MHZ.. The signal is used to strobe the pixel data and DSPTMG signals. All pixel data shall be valid at the falling edge when the DSPTMG signal is high.
DSPTMG	Display Timing	This signal is strobed at the falling edge of -DTCLK. When the signal is high, the pixel data shall be valid to be displayed.
VSYNC	Vertical Sync	The signal is synchronized to -DTCLK .
HSYNC	Horizontal Sync	The signal is synchronized to -DTCLK .

Note: Output signals from any system shall be low or Hi-Z state when VDD is off.

6.3 Signal Description

Signal Name	Description
RxIN0N, RxIN0P	LVDS differential data input (Red0-Red5, Green0)
RxIN1N, RxIN1P	LVDS differential data input (Green1-Green5, Blue0-Blue1)
RxIN2N, RxIN2P	LVDS differential data input (Blue2-Blue5, Hsync, Vsync, DSPTMG)
RxCLKINN, RxCLKIN0P	LVDS differential clock input
VDD	+3.3V Power Supply
GND	Ground

Connector

20

NC

1

GND
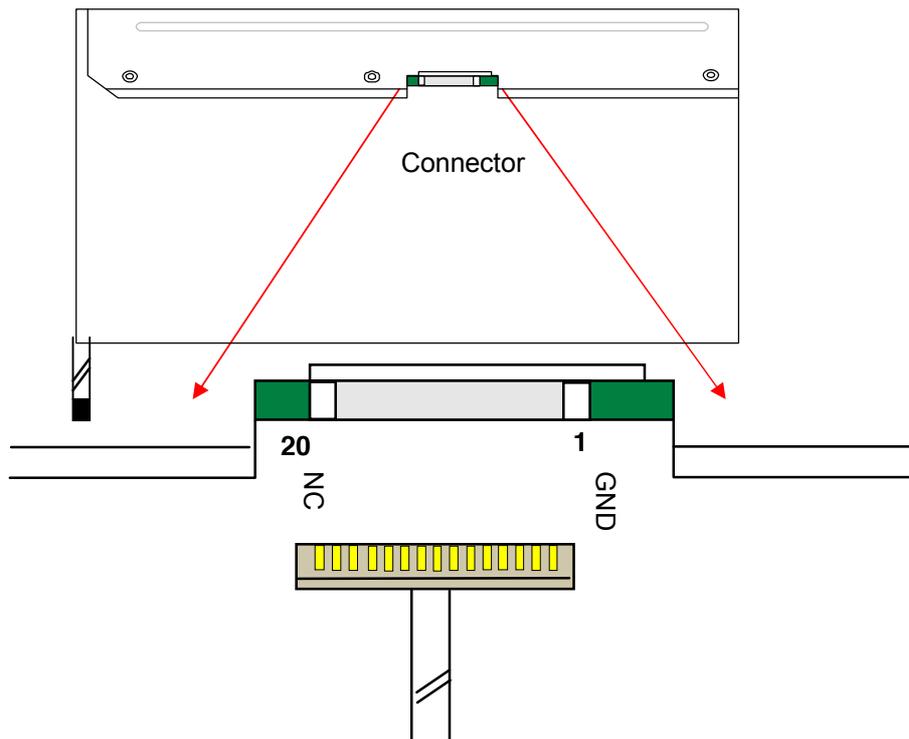
The module uses a 100ohm resistor between positive and negative data lines of each receiver input
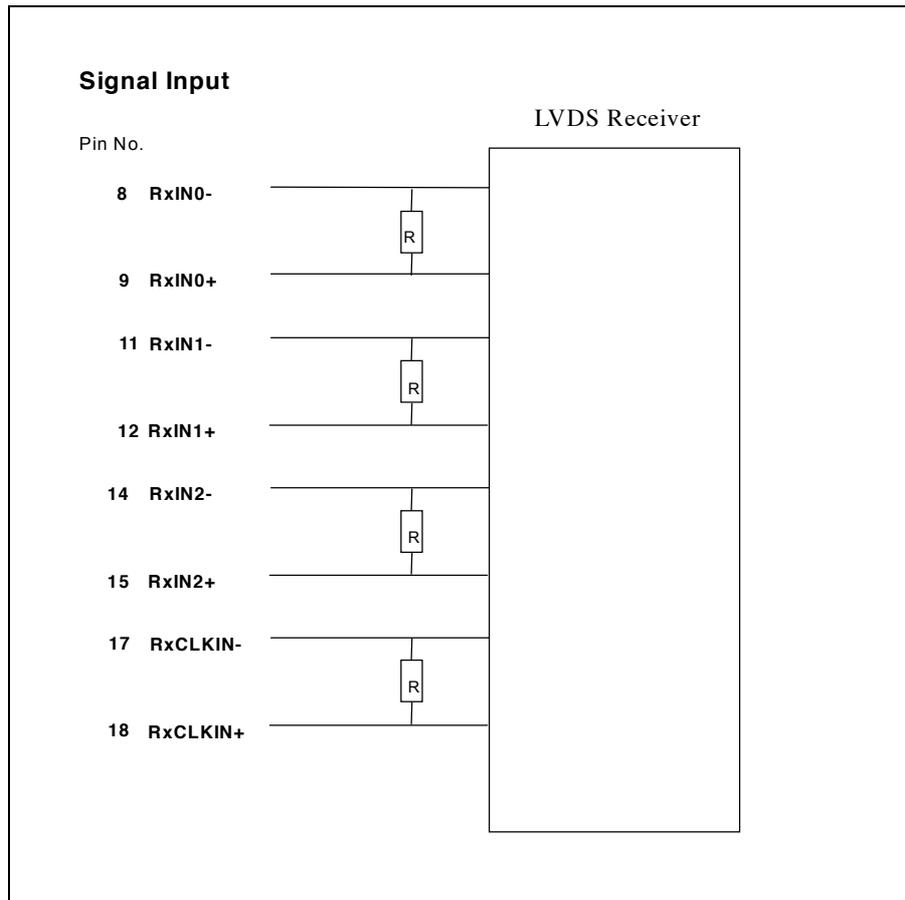
6.4 Interface Timing

6.4.1 Timing Characteristics

Basically, interface timings should match the 1280x800 /60Hz   manufacturing guide line timing.

Parameter		Symbol	Min.	Typ.	Max.	Unit
Frame Rate		-	50	60	-	Hz
Clock frequency		$1/T_{Clock}$	62	68.9	72	MHz
Vertical Section	Period	T_V	803	816	832	T_{Line}
	Active	T_{VD}	800	800	800	
	Blanking	T_{VB}	3	16	32	
Horizontal Section	Period	T_H	1302	1408	1700	T_{Clock}
	Active	T_{HD}	-	1280	-	
	Blanking	T_{HB}	22	128	420	
End-frame checking period		tEF	2			T_{Line}
DE checking period		tDE	6400			T_{Line}

Note : DE mode only

6.4.2 Timing diagram

Input Timing Definition (DE Mode)
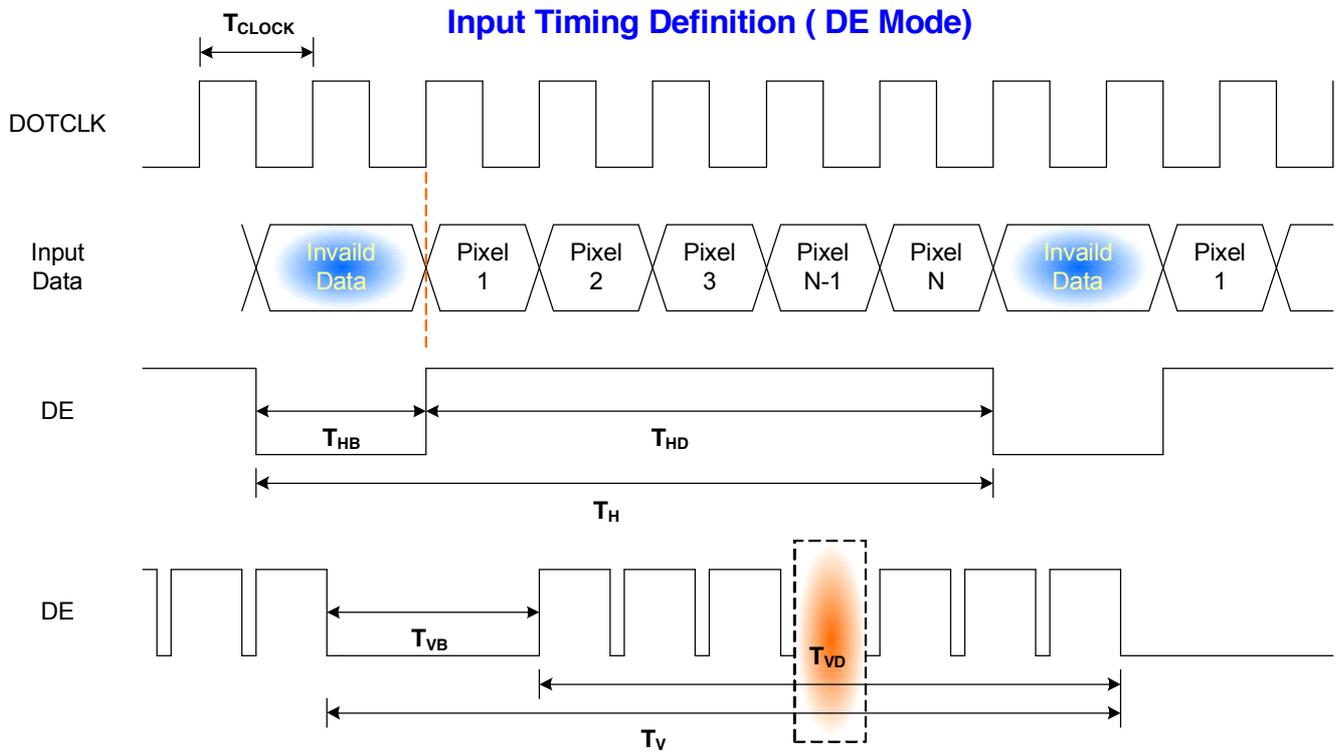
6.5 Power ON/OFF Sequence

VDD power and lamp on/off sequence is as follows. Interface signals are also shown in the chart. Signals from any system shall be Hi-Z state or low level when VDD is off.
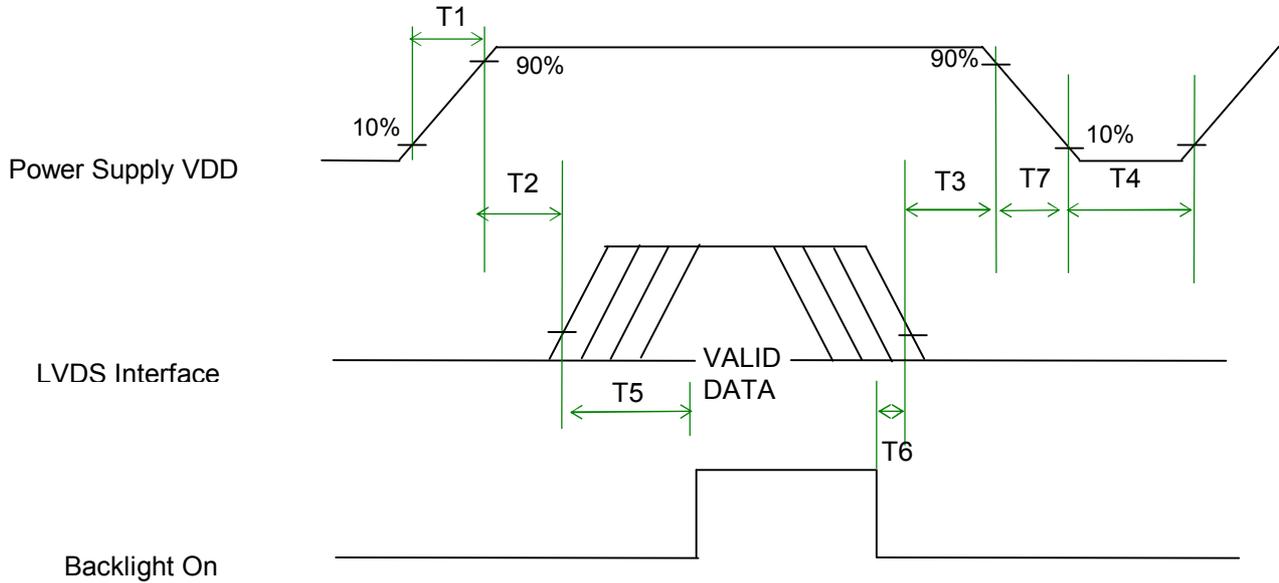
Power Sequence Timing

Parameter	Value			Units
	Min.	**Typ.**	**Max.**	
T1	0.5	-	10	(ms)
T2	0	-	50	(ms)
T3	0	-	50	(ms)
T4	500	-	-	(ms)
T5	200	-	-	(ms)
T6	200	-	-	(ms)
T7	0	-	10	(ms)

7. Connector & Pin Assignment

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

7.1 TFT LCD Module

(A) CONNECTOR

Connector Name / Designation	For Signal Connector
Manufacturer	Hirose
Type / Part Number	DF19L-20P-1H
Mating Housing/Part Number	DF19G-20S-1C or compatible

(B) Signal Pin

LVDS is a differential signal technology for LCD interface and high speed data transfer device.

PIN#	Signal Name	Description
1	GND	Ground
2	VDD	+3.3V Power Supply
3	VDD	+3.3V Power Supply
4	V_{EDID}	+3.3V EDID Power
5	NC	No Connection (Bist Enable)
6	CLK_{EDID}	EDID Clock Input
7	$DATA_{EDID}$	EDID Data Input
8	RxIN0-	LVDS differential data input(R0-R5, G0)
9	RxIN0+	LVDS differential data input(R0-R5, G0)
10	GND	Ground
11	RxIN1-	LVDS differential data input(G1-G5, B0-B1)
12	RxIN1+	LVDS differential data input(G1-G5, B0-B1)
13	GND	Ground
14	RxIN2-	LVDS differential data input(B2-B5, HS, VS, DE)
15	RxIN2+	LVDS differential data input(B2-B5, HS, VS, DE)
16	GND	Ground
17	RxCLKIN-	LVDS differential clock input
18	RxCLKIN+	LVDS differential clock input
19	GND	Ground
20	NC	No connection

7.2 Backlight Unit

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

(A) CONNECTOR

Connector Name / Designation	For Lamp Connector
Manufacturer	JST
Type / Part Number	SM07B-SRSS-TB
Mating Type / Part Number	SHR-07V-S-B

7.3 Signal for LED Driver Board

LVDS is a differential signal technology for LCD interface and high speed data transfer device.

PIN#	Signal Name	Description
1	ALSEN	Ambient light sensor control signal (Enable:5V, disable:0V)
2	PWM	high: 3.3V, low: 0V, frequency 17.5KHz
3	Logic Power	+5V Power Supply for ALS, Controller, enable pin of LED driver
4	GND	Power Ground
5	GND	Power Ground
6	VIN	+7~21V Power Supply
7	VIN	+7~21V Power Supply

8 Vibration and Shock Test

8.1 Vibration Test

Test Spec:

Test method:	Non-Operation
Acceleration:	1.5G
Frequency:	26 - 500Hz Random
Sweep:	30 Minutes each Axis (X, Y, Z)

8.2 Shock Test Spec:

Test Spec:

Test method:	Non-Operation
Acceleration:	180 G , Half sine wave
Active time:	2 ms
Pulse:	X,Y,Z .one time for each side

9. Reliability

Items	Required Condition	Note
Temperature Humidity Bias	40℃/95%,250Hr	
High Temperature Operation	50℃/Dry,250Hr	
Low Temperature Operation	0℃,250Hr	
On/Off Test	ON/30 sec. OFF/30sec., 30,000 cycles.	
Hot Storage	65℃/20% RH ,250 hours	
Cold Storage	-40℃/50% RH ,250 hours	
Thermal Shock Test	-40℃/20 min ,65℃/20 min 300cycles	
Hot Start Test	50℃/1 Hr min.　power on/off per 5 minutes, 5 times	
Cold Start Test	0℃/1 Hr min.　power on/off per 5 minutes, 5 times	
Shock Test (Non-Operating)	180G, 2ms, Half-sine wave	
Vibration Test (Non-Operating)	Random vibration, 1.5 G zero-to-peak, 26 to 500 Hz, 30 mins in each of three mutually perpendicular axes.	
ESD	Contact :　±8KV/ operation Air :　　　±15KV / operation	Note 1
Room temperature Test	25℃, 2000hours, Operating with loop pattern	

Note1: According to EN61000-4-2 , ESD class B: Some performance degradation allowed. No data lost

　　. Self-recoverable. No hardware failures.

Note2: LED Life time: 10,000 hours minimum under 20 mA driving current / normal module usage.

10. Mechanical Characteristics

10.1 LCM Outline Dimension

Shipping label

BLU bar code

107 ±1

32.7 ±1

176 ±1

76.2 ±1
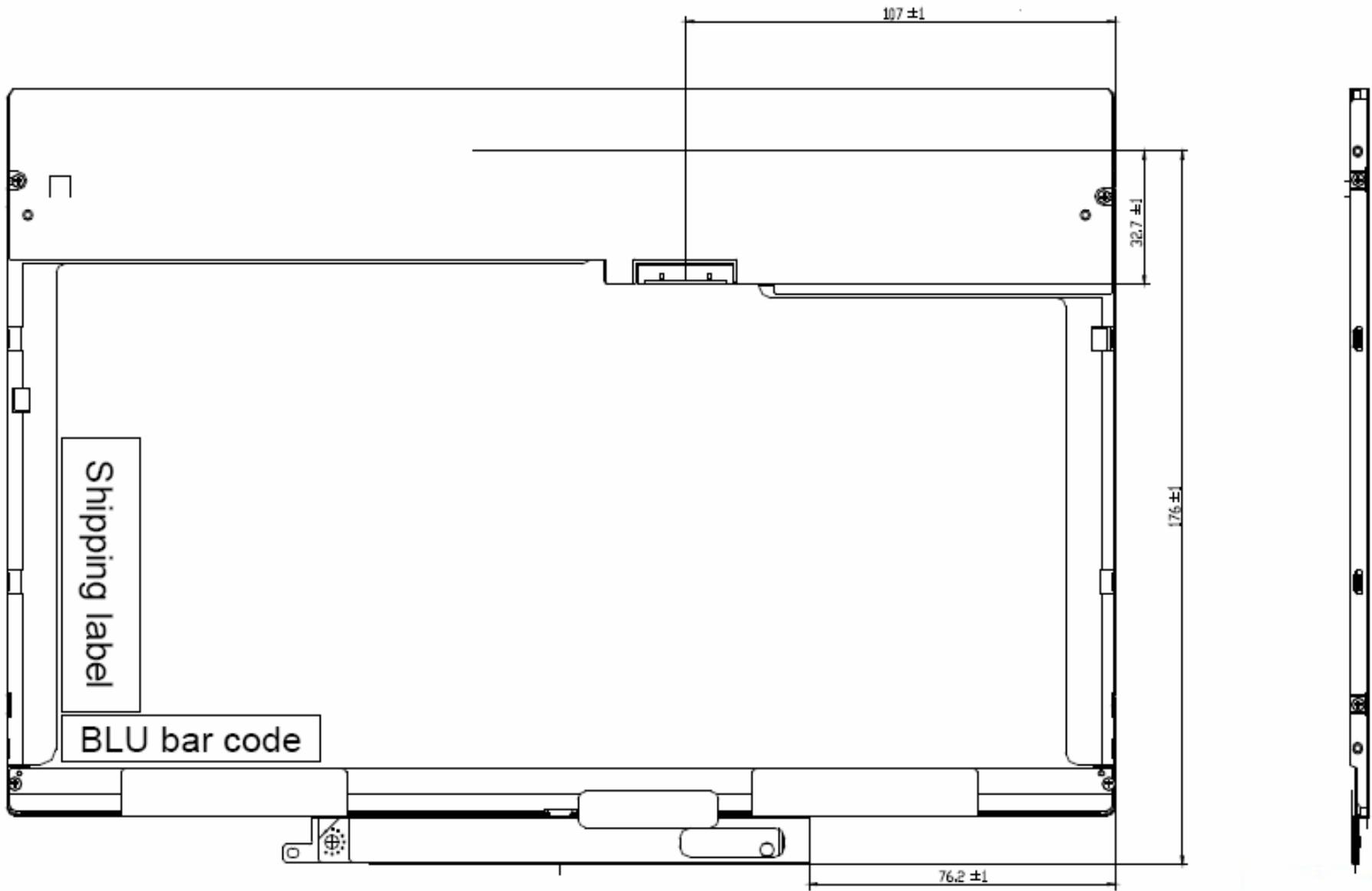
10.2 Screw Hole Depth and Center Position

Screw hole minimum depth, from side surface =2.85 mm (See drawing)

Screw hole center location, from front surface = 328 ± 0.2mm (See drawing)
Screw Torque: Maximum 2.2 kgf-cm
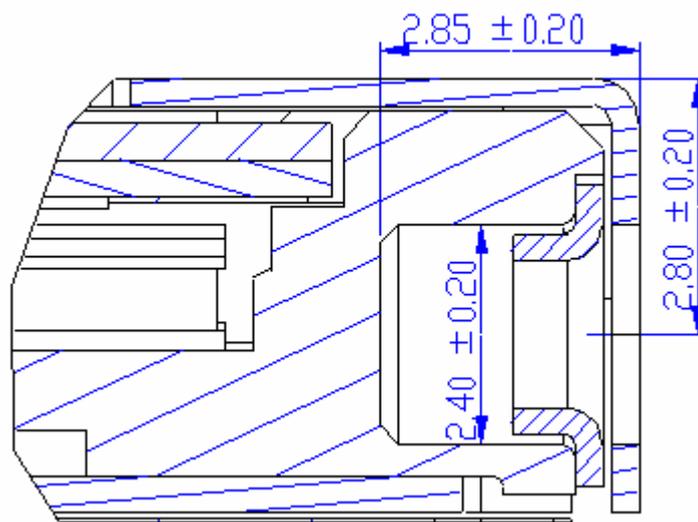
11. Shipping and Package

11.1 Shipping Label Format
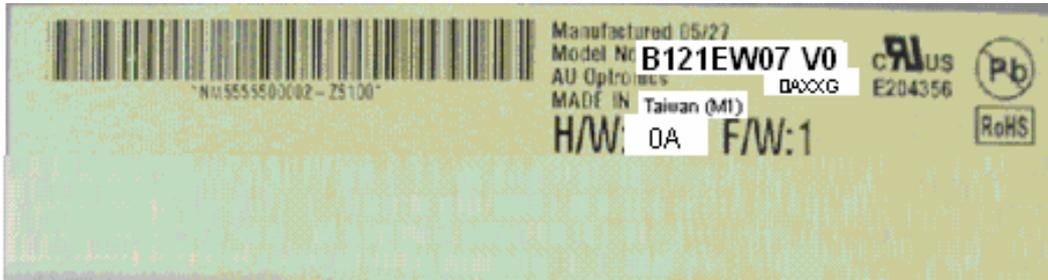
Note 1:

IC Combination	Control Code	H/W
First source IC	0AXXX	0A

11.2. Carton package

The outside dimension of carton is 486 (L)mm x 286 (W)mm x 360 (H)mm
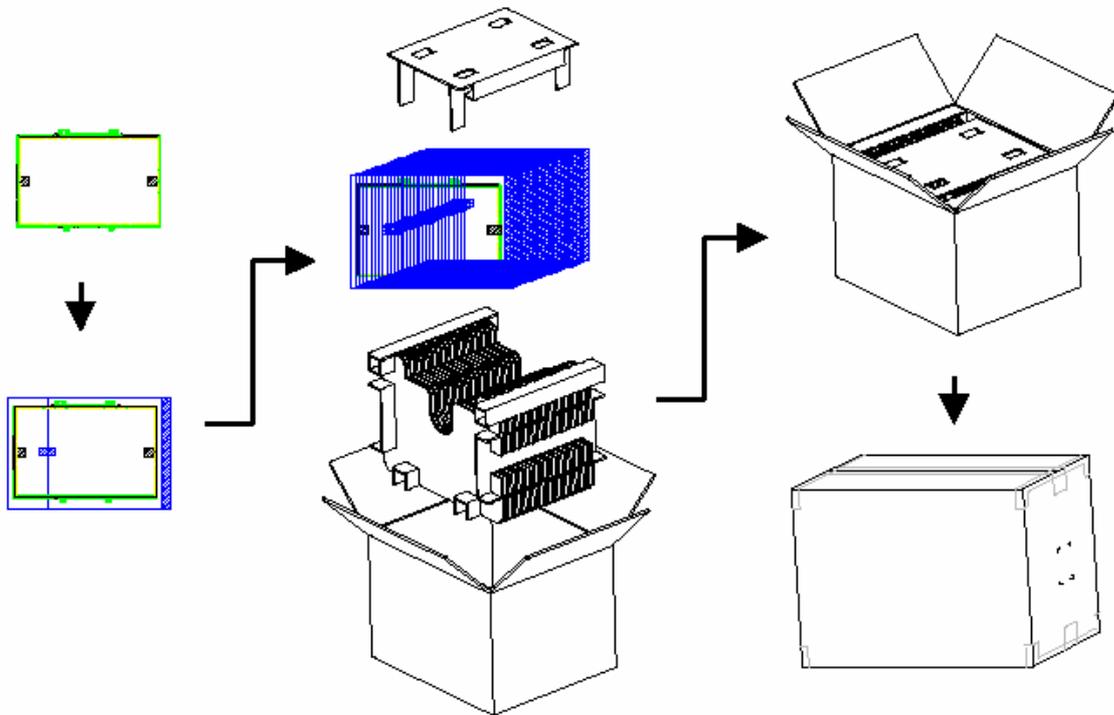
11.3 Shipping package of palletizing sequence

Top cardboard

Bottom cardboard

Wooden pallet

Corner angle

PE band

Stretch film

Note : Limit of box palletizing = Max 3 layers(ship and stock conditions)

12. Appendix: EDID description

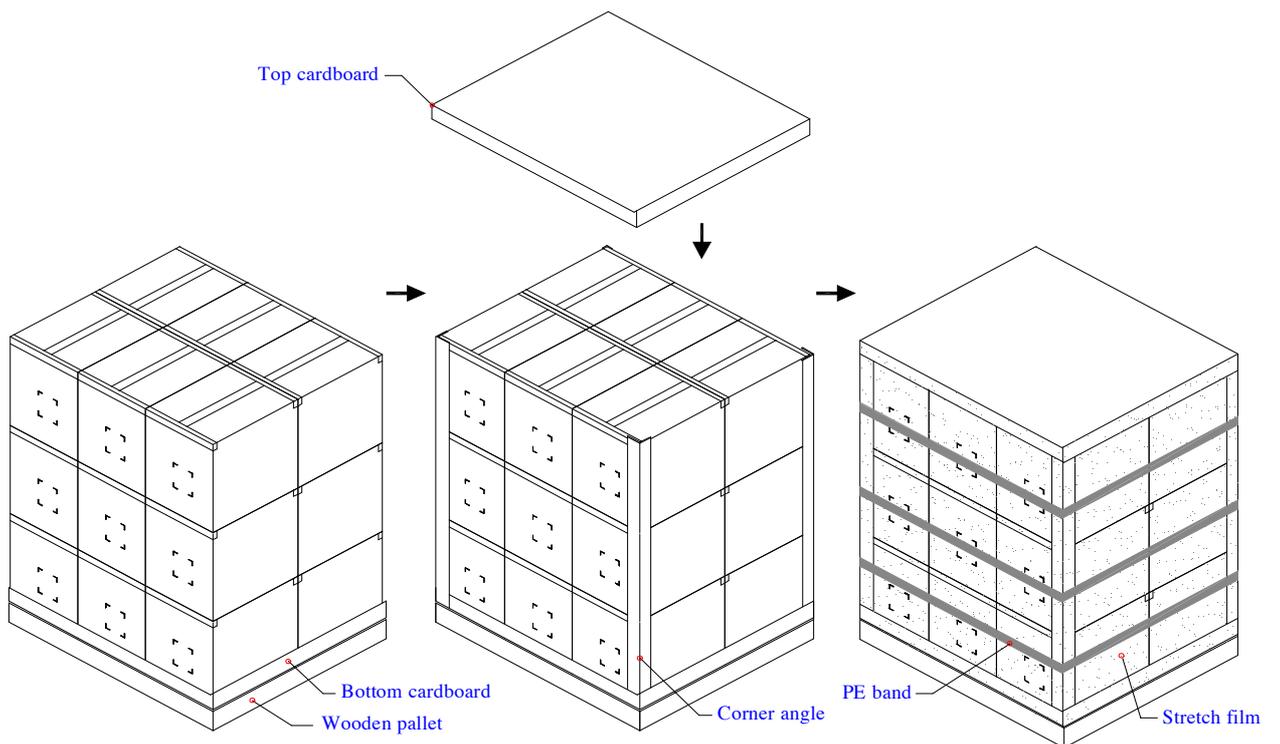| Address	FUNCTION	Value	Value	Value	Note
HEX		HEX	BIN	DEC	
00	Header	00	00000000	0	
01		FF	11111111	255	
02		FF	11111111	255	
03		FF	11111111	255	
04		FF	11111111	255	
05		FF	11111111	255	
06		FF	11111111	255	
07		00	00000000	0	
08	EISA Manuf. Code LSB	06	00000110	6	
09	Compressed ASCII	AF	10101111	175	
0A	Product Code	14	00010100	20	
0B	hex, LSB first	70	01110000	112	
0C	32-bit ser #	00	00000000	0	
0D		00	00000000	0	
0E		00	00000000	0	
0F		00	00000000	0	
10	Week of manufacture	01	00000001	1	
11	Year of manufacture	11	00010001	17	
12	EDID Structure Ver.	01	00000001	1	
13	EDID revision #	03	00000011	3	
14	**Video input def.** *(digital I/P, non-TMDS, CRGB)*	80	10000000	128	
15	**Max H image size** *(rounded to cm)*	1A	00011010	26	
16	**Max V image size** *(rounded to cm)*	10	00010000	16	
17	**Display Gamma** *(=(gamma*100)-100)*	78	01111000	120	
18	**Feature support** *(no DPMS, Active OFF, RGB, tmg Blk#1)*	0A	00001010	10	
19	Red/green low bits **(Lower 2:2:2:2 bits)**	87	10000111	135	
1A	Blue/white low bits **(Lower 2:2:2:2 bits)**	FE	11111110	254	
1B	Red x **(Upper 8 bits)**	94	10010100	148	
1C	Red y/ highER 8 bits	57	01010111	87	
1D	Green x	4F	01001111	79	
1E	Green y	8C	10001100	140	
1F	Blue x	27	00100111	39	
20	Blue y	27	00100111	39	
21	White x	50	01010000	80	
22	White y	54	01010100	84	
23	Established timing 1	00	00000000	0	
24	Established timing 2	00	00000000	0	
25	Established timing 3	00	00000000	0	
26	Standard timing #1	01	00000001	1	
27		01	00000001	1	
28	Standard timing #2	01	00000001	1	
29		01	00000001	1	
2A	Standard timing #3	01	00000001	1	
2B		01	00000001	1	
2C	Standard timing #4	01	00000001	1	

Address	Description	Hex	Binary	Decimal	
2D		01	00000001	1	
2E	Standard timing #5	01	00000001	1	
2F		01	00000001	1	
30	Standard timing #6	01	00000001	1	
31		01	00000001	1	
32	Standard timing #7	01	00000001	1	
33		01	00000001	1	
34	Standard timing #8	01	00000001	1	
35		01	00000001	1	
36	Pixel Clock/10000 LSB	EA	11101010	234	
37	Pixel Clock/10000 USB	1A	00011010	26	
38	Horz active **Lower 8bits**	00	00000000	0	
39	Horz blanking **Lower 8bits**	80	10000000	128	
3A	HorzAct:HorzBlnk **Upper 4:4 bits**	50	01010000	80	
3B	Vertical Active **Lower 8bits**	20	00100000	32	
3C	Vertical Blanking **Lower 8bits**	10	00010000	16	
3D	Vert Act : Vertical Blanking **(upper 4:4 bit)**	30	00110000	48	
3E	HorzSync. Offset	30	00110000	48	
3F	HorzSync.Width	20	00100000	32	
40	VertSync.Offset : VertSync.Width	36	00110110	54	
41	Horz&Vert Sync Offset/Width **Upper 2bits**	00	00000000	0	
42	Horizontal Image Size **Lower 8bits**	05	00000101	5	
43	Vertical Image Size **Lower 8bits**	A3	10100011	163	
44	Horizontal & Vertical Image Size **(upper 4:4 bits)**	10	00010000	16	
45	Horizontal Border *(zero for internal LCD)*	00	00000000	0	
46	Vertical Border *(zero for internal LCD)*	00	00000000	0	
47	Signal *(non-intr, norm, no stero, sep sync, neg pol)*	18	00011000	24	
48	Detailed timing/monitor	00	00000000	0	
49	descriptor #2	00	00000000	0	
4A		00	00000000	0	
4B		0F	00001111	15	
4C		00	00000000	0	
4D		00	00000000	0	
4E		00	00000000	0	
4F		00	00000000	0	
50		00	00000000	0	
51		00	00000000	0	
52		00	00000000	0	
53		00	00000000	0	
54		00	00000000	0	
55		00	00000000	0	
56		00	00000000	0	
57		00	00000000	0	
58		00	00000000	0	
59		20	00100000	32	
5A	Detailed timing/monitor	00	00000000	0	
5B	descriptor #3	00	00000000	0	
5C		00	00000000	0	
5D		FE	11111110	254	

5E		00	00000000	0	
5F	Manufacture	41	01000001	65	A
60	Manufacture	55	01010101	85	U
61	Manufacture	4F	01001111	79	O
62		0A	00001010	10	
63		20	00100000	32	
64		20	00100000	32	
65		20	00100000	32	
66		20	00100000	32	
67		20	00100000	32	
68		20	00100000	32	
69		20	00100000	32	
6A		20	00100000	32	
6B		20	00100000	32	
6C	Detailed timing/monitor	00	00000000	0	
6D	descriptor #4	00	00000000	0	
6E		00	00000000	0	
6F		FE	11111110	254	
70		00	00000000	0	
71	Manufacture P/N	42	01000010	66	B
72	Manufacture P/N	31	00110001	49	1
73	Manufacture P/N	32	00110010	50	2
74	Manufacture P/N	31	00110001	49	1
75	Manufacture P/N	45	01000101	69	E
76	Manufacture P/N	57	01010111	87	W
77	Manufacture P/N	30	00110000	48	0
78	Manufacture P/N	37	00110111	55	7
79	Manufacture P/N	20	00100000	32	
7A	Manufacture P/N	56	01010110	86	V
7B	Manufacture P/N	30	00110000	48	0
7C		20	00100000	32	
7D		0A	00001010	10	
7E	Extension Flag	00	00000000	0	
7F	Checksum	D1	11010001	209	
		SUM		6144	
		SUM to HEX		1800	