



Preliminary Specification  
 Final Specification

<b>Module</b>	24.0" WUXGA Color TFT-LCD
<b>Model Name</b>	M240UW01 V1

<b>Customer</b>	<b>Date</b>
_____	_____
<b>Approved by</b>	
_____	_____

Note: This Specification is subject to change without notice.

<b>Prepared by</b>	<b>Date</b>
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<b>Approved by</b>	
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Desktop Display Business Group /  
AU Optronics corporation

## 2.0 General Description

This specification applies to the 24.0 inch Color a-Si TFT-LCD Module M240UW01.

The display supports the WUXGA (1920(H) x 1200(V)) screen format and 16.7M colors (RGB 8-bits data).

All input signals are 2 channel LVDS interface compatible.

This module doesn't contain an inverter board for backlight.

## 2.1 Display Characteristics

The following items are characteristics summary on the table under 25 °C condition:

ITEMS	Unit	SPECIFICATIONS
Screen Diagonal	[mm]	611.32(24")
Active Area	[mm]	518.4 (H) x 324 (V)
Pixels H x V		1920(x3) x 1200
Pixel Pitch	[mm]	0.270 (per one triad) x 0.270
Pixel Arrangement		R.G.B. Vertical Stripe
Display Mode		Normally Black
White Luminance ( Center )	[cd/m <sup>2</sup> ]	500 cd/m <sup>2</sup> @ I <sub>L</sub> =6mA (Typ.)
Contrast Ratio		1000 : 1 (Typ.)
Optical Response Time	[msec]	12ms(Typ., on/off); 8ms(Typ., GTG)
Nominal Input Voltage VDD	[Volt]	+5.0 V
Power Consumption (VDD line + CCFL line)	[Watt]	74 W (Typ.) (without inverter)
Weight	[Grams]	3250 (Max)
Physical Size	[mm]	546.4(W) x 352(H) x 35.8(D) (Typ.)
Electrical Interface		Even/Odd R/G/B data, clock LVDS
Support Color		16.7M colors (RGB 8-bit data )
Surface Treatment		Glare type ,Hard coating (2H)
Temperature Range		
Operating	[°C]	0 to +50
Storage (Shipping)	[°C]	-20 to +60
RoHS Compliance		RoHS Compliance

## 2.2 Optical Characteristics

The optical characteristics are measured under stable conditions at 25°C:

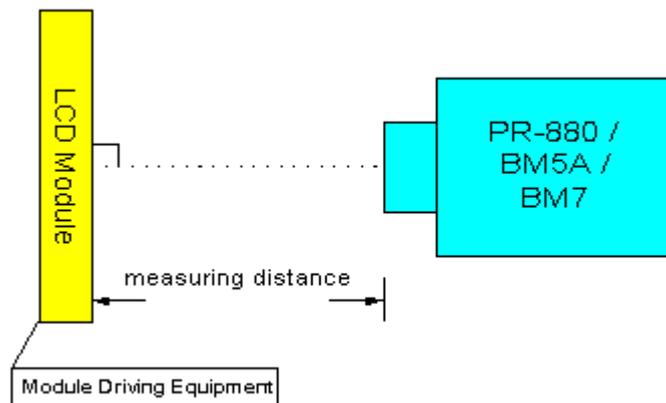
Item	Unit	Conditions	Min.	Typ.	Max.	Note
Viewing Angle	[degree] [degree]	Horizontal (Right)	75	89	-	
		CR = 10 (Left)	75	89	-	
	[degree] [degree]	Vertical (Up)	75	89	-	
		CR = 10 (Down)	75	89	-	
Contrast ratio		Normal Direction	700	1000	-	
Response Time	[msec]	Raising Time	-	7		<b>Note 1</b>
	[msec]	Falling Time	-	5		<b>Note 1</b>
	[msec]	Raising + Falling	-	12		<b>Note 1</b>
	[msec]	Gray to Gray	-	8	-	<b>Note 2</b>
Color / Chromaticity Coordinates (CIE)		Red x	0.623	0.653	0.683	
		Red y	0.307	0.337	0.367	
		Green x	0.265	0.295	0.325	
		Green y	0.577	0.607	0.637	
		Blue x	0.114	0.144	0.174	
		Blue y	0.045	0.075	0.105	
Color Coordinates (CIE) White		White x	0.283	0.313	0.343	
		White y	0.299	0.329	0.359	
Central Luminance ( $I_L=6mA$ )	[cd/m <sup>2</sup> ]		400	500	-	
Luminance Uniformity	[%]		75	80	-	<b>Note 3</b>
Crosstalk (in60Hz)	[%]				1.5	<b>Note 4</b>
Flicker	dB				-20	<b>Note 5</b>

Equipment Pattern Generator, Power Supply, Digital Voltmeter, Luminance meter (PR 880, BM-5A , BM 7 ,CS-1000, & EZContrast\* )

Aperture 1° with 100cm VD or 2° with 50cm viewing distance

Test Point Center (VESA point 9)

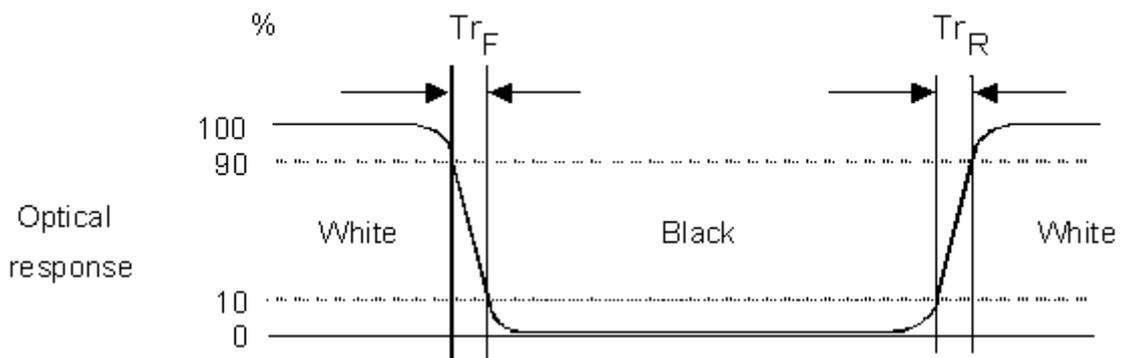
Environment < 1 lux



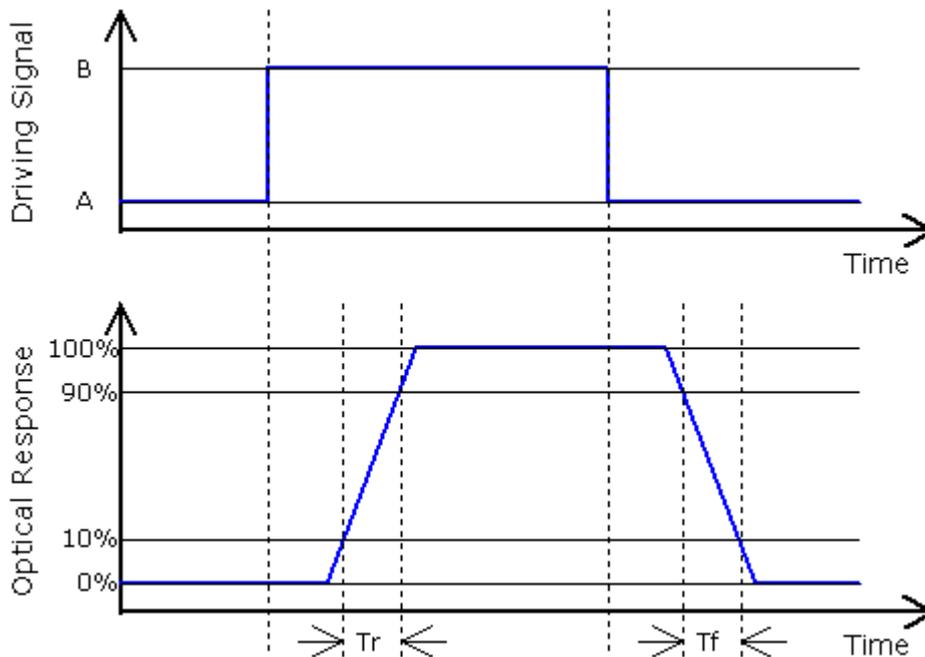
\* EZ Contrast is different measurement tool with very close viewing distance.

**Note 1: Definition of Response time**

The output signals of photodetector are measured when the input signals are changed from “Black” to “White” (rising time), and from “White” to “Black ”(falling time), respectively. The response time is interval between the 10% and 90% of amplitudes.



**Note 2: Over-Drive and Response time:**

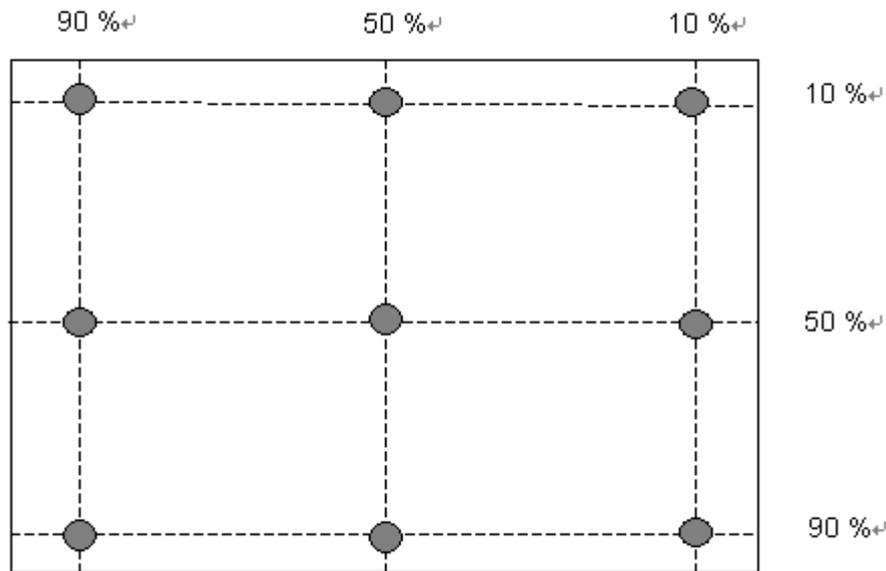


Algorithm:

$| \text{Level A} - \text{Level B} | \geq 16$  then the average of Grey-to-Grey response time is 8 ms. ( F = 60 Hz).

$Tr$  (rising time; from “Black” to “White”) +  $Tf$  (Falling time; from “White” to “Black”) = 12 ms(typ).

**Note 3:** Luminance uniformity of these 9 points is defined as below



$$\text{Uniformity} = \frac{\text{Minimum Luminance in 9 points (1 - 9)}}{\text{Maximum Luminance in 9 Points (1 - 9)}}$$

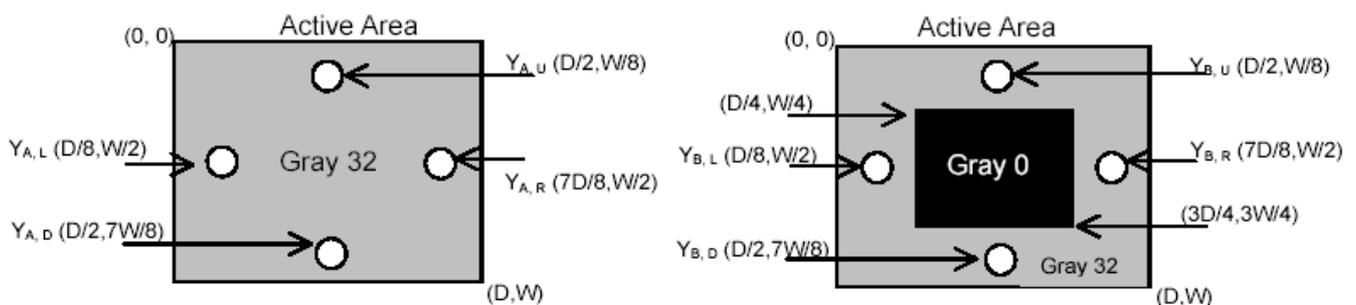
**Note 4:** Crosstalk is defined as below :

$$\text{CT} = |Y_B - Y_A| / Y_A \times 100 (\%)$$

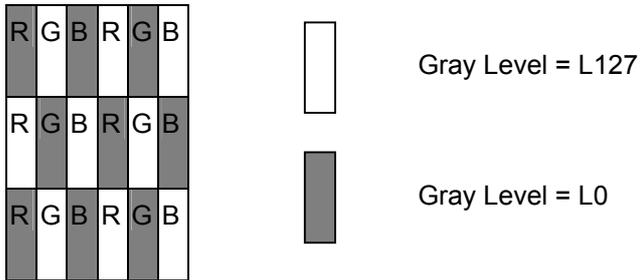
Where

YA = Luminance of measured location without gray level 0 pattern (cd/m<sup>2</sup>)

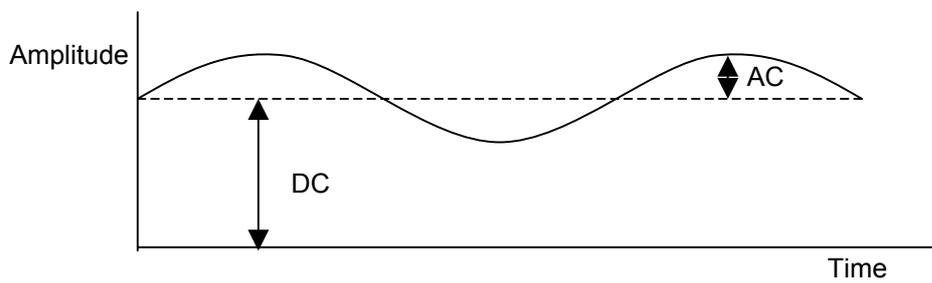
YB = Luminance of measured location with gray level 0 pattern (cd/m<sup>2</sup>)



**Note 5:** Test Patern: Subchecker Pattern



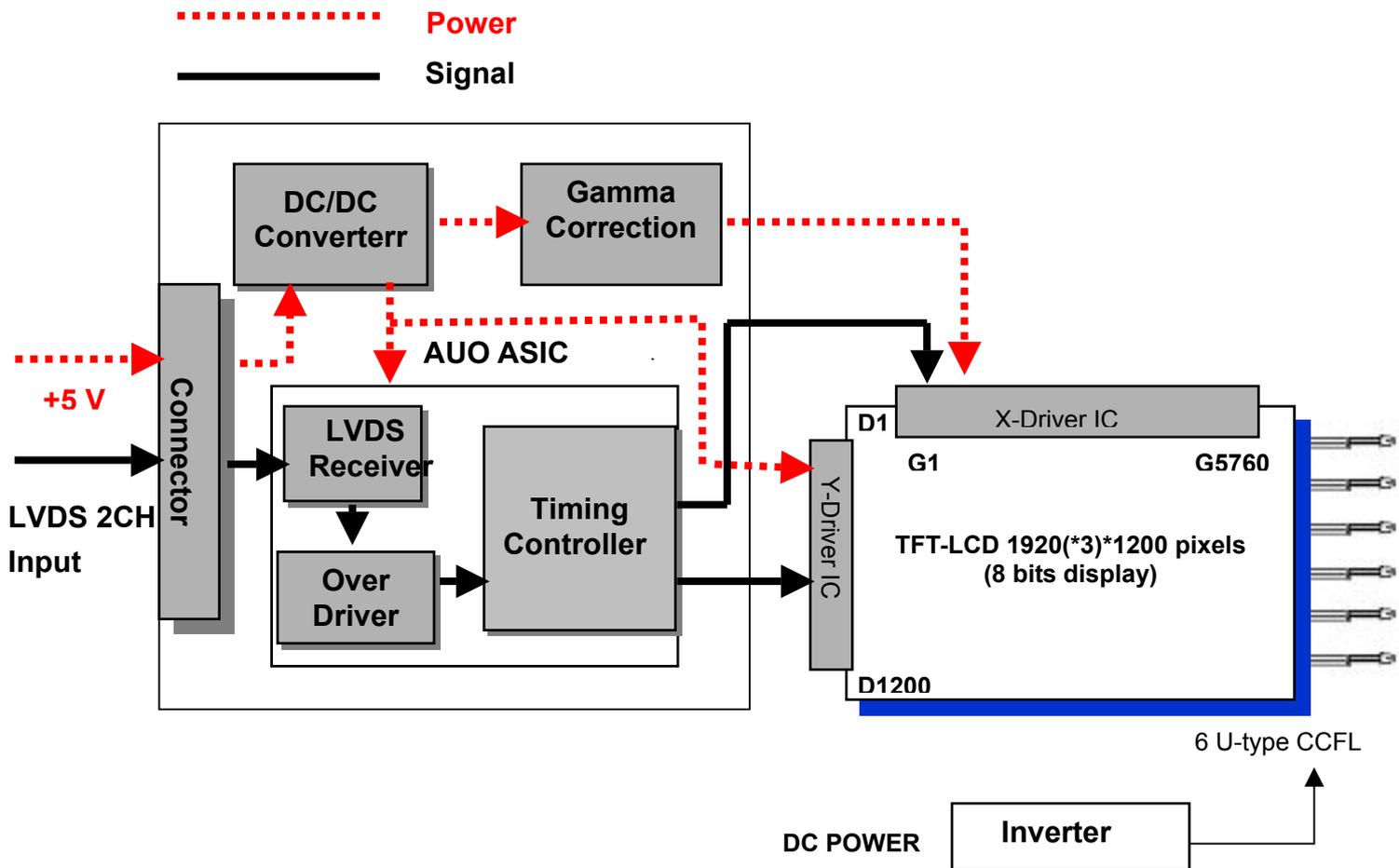
Method: Record dBV & DC value with (WESTAR)TRD-100



$$\text{Flicker (dB)} = 20 \log \frac{\text{AC Level(at 30 Hz)}}{\text{DC Level}}$$

## 3.0 Functional Block Diagram

The following diagram shows the functional block of the 24.0 inch Color TFT-LCD Module:



### I/F PCB Interface:

JAE FI-XB30SSL-HF15 or compatible

### Mating Type:

FI-X30HL-T (Locked Type)

FI-X30S-H (Unlocked Type)

## 4.0 Absolute Maximum Ratings

Absolute maximum ratings of the module is as following:

### 4.1 TFT LCD Module

Item	Symbol	Min	Max	Unit	Conditions
Logic/LCD Drive	VIN	4.5	5.5	[Volt]	Note 1,2

### 4.2 Backlight Unit

Item	Symbol	Min	Max	Unit	Conditions
CCFL Current	ICFL	2.0	8.0	[mA] rms	Note 1,2

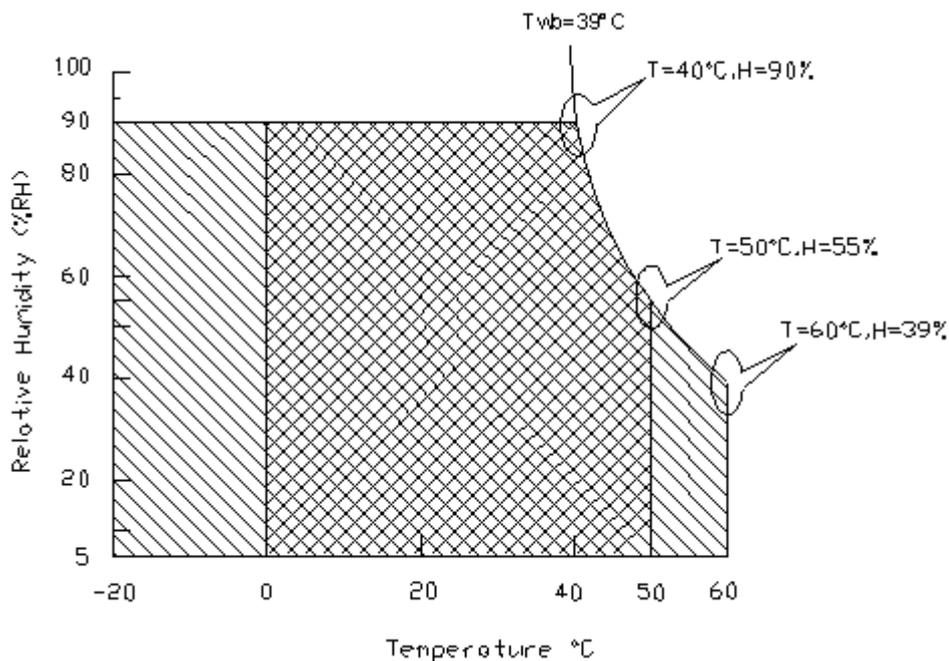
### 4.3 Absolute Ratings of Environment

Item	Symbol	Min.	Max.	Unit	Conditions
Operating Temperature	TOP	0	+50	[°C]	Note 3
Operation Humidity	HOP	5	90	[%RH]	
Storage Temperature	TST	-20	+60	[°C]	
Storage Humidity	HST	5	90	[%RH]	

**Note 1:** With in Ta (25°C )

**Note 2:** Permanent damage to the device may occur if exceed maximum values

**Note 3:** For quality performance, please refer to AUO IIS(Incoming Inspection Standard).



Operating Range



Storage Range





## 5.1.2 Signal Electrical Characteristics

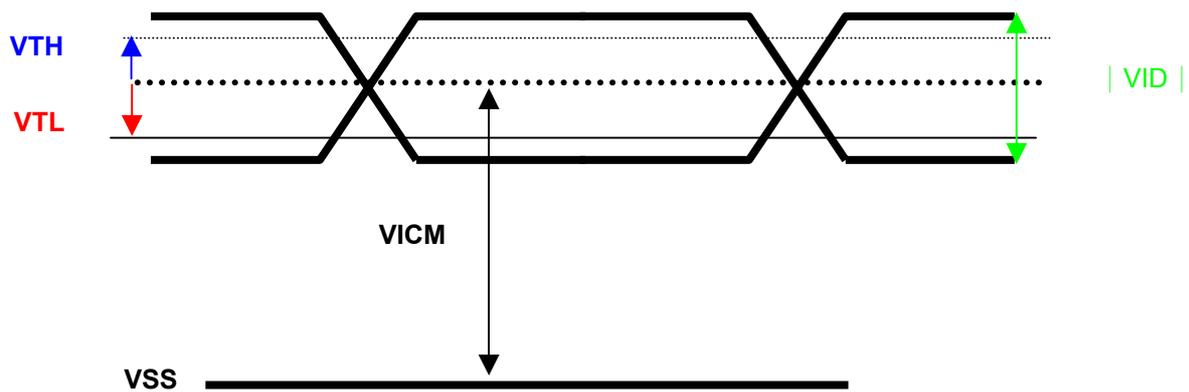
Input signals shall be low or Hi-Z state when Vin is off

It is recommended to refer the specifications of SN75LVDS82DGG (Texas Instruments) in detail.

Each signal characteristics are as follows;

Symbol	Parameter	Min	Typ	Max	Units	Condition
VTH	Differential Input High Threshold	-	+50	+100	[mV]	VICM = 1.2V <b>Note</b>
VTL	Differential Input Low Threshold	-100	-50	-	[mV]	VICM = 1.2V <b>Note</b>
VID	Input Differential Voltage	100	-	600	[mV]	<b>Note</b>
VICM	Differential Input Common Mode Voltage	+1.0	+1.2	+1.5	[V]	VTH-VTL = 200mV <b>Note</b>

**Note:** LVDS Signal Waveform



## 5.2 Backlight Unit

Parameter guideline for CCFL Inverter is under stable conditions at 25°C (Room Temperature):

Parameter	Min.	Typ.	Max.	Unit	Condition
CCFL Operation Current(IRCFL)	2.0	6.0	8.0	[mA] rms	Note 2
CCFL Frequency(FCFL)	48	53	58	[KHz]	Note 3,4
CCFL Ignition Voltage(ViCFL, Ta= 0°C)	2850	-	-	[Volt] rms	Note 5
CCFL Ignition Voltage(ViCF, Ta= 25°C)	2280	-	-	[Volt] rms	
CCFL Operation Voltage (VCFL)	-	1800 (@ 6mA)	-	[Volt] rms	Note 6
CCFL Power Consumption(PCFL)	-	64.8	-	[Watt]	Note 6
CCFL Life Time(LTCFL)	40,000	50,000	-	[Hour]	Note 7

Note 1: Typ. are AUO recommended design points.

- \*1 All of characteristics listed are measured under the condition using the AUO test inverter.
- \*2 In case of using an inverter other than listed, it is recommended to check the inverter carefully. Sometimes, interfering noise stripes appear on the screen, and substandard luminance or flicker at low power may happen.
- \*3 In designing an inverter, it is suggested to check safety circuit very carefully. Impedance of CCFL, for instance, becomes more than 1 [M ohm] when CCFL is damaged.
- \*4 Generally, CCFL has some amount of delay time after applying kick-off voltage. It is recommended to keep on applying kick-off voltage for 1 [Sec] until discharge.
- \*5 Reducing CCFL current increases CCFL discharge voltage and generally increases CCFL discharge frequency. So all the parameters of an inverter should be carefully designed so as not to produce too much leakage current from high-voltage output of the inverter.

Note 2: CCFL standard current is measured at 25±2°C.

Note 3: CCFL discharge frequency should be carefully determined to avoid interference between inverter and TFT LCD.

Note 4: The frequency range will not affect to lamp life and reliability characteristics.

Note 5: CCFL inverter should be able to give out a power that has a generating capacity of over 2850 voltage. Lamp units need 2850 voltage minimum for ignition.

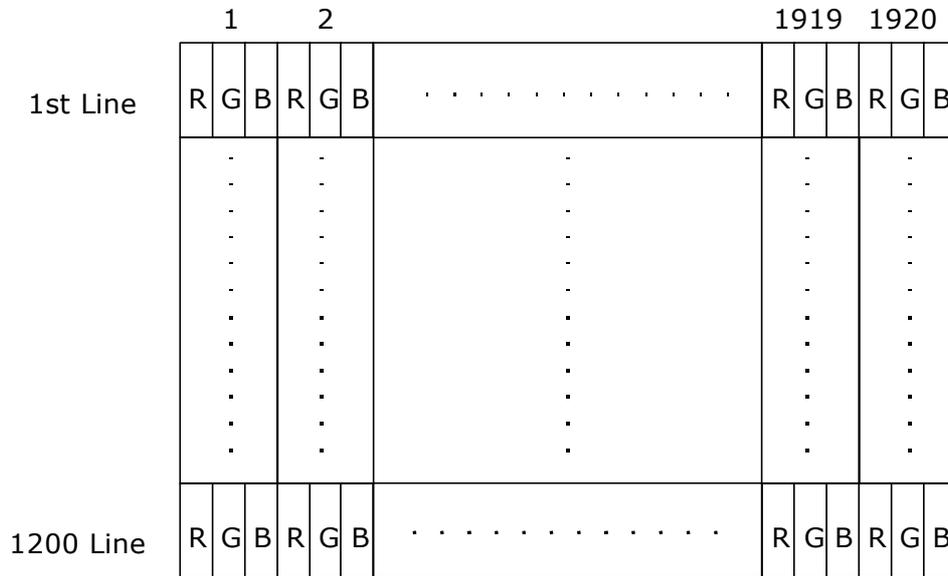
Note 6: The variance of CCFL power consumption is ±10%. Calculator value for reference (IRCFL × VCFL × 6 = PCFL)

Note 7: Definition of life: brightness becomes 50% or less than the minimum luminance value of CCFL. The typical life time of CCFL is on the condition at 6 mA lamp current.

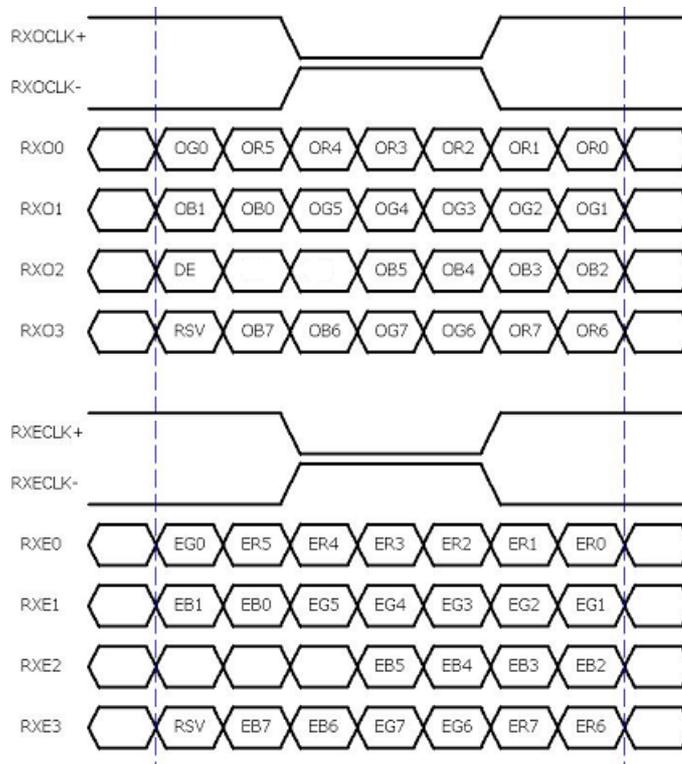
## 6.0 Signal Characteristic

### 6.1 Pixel Format Image

Following figure shows the relationship of the input signals and LCD pixel format.



### 6.2 The input data format



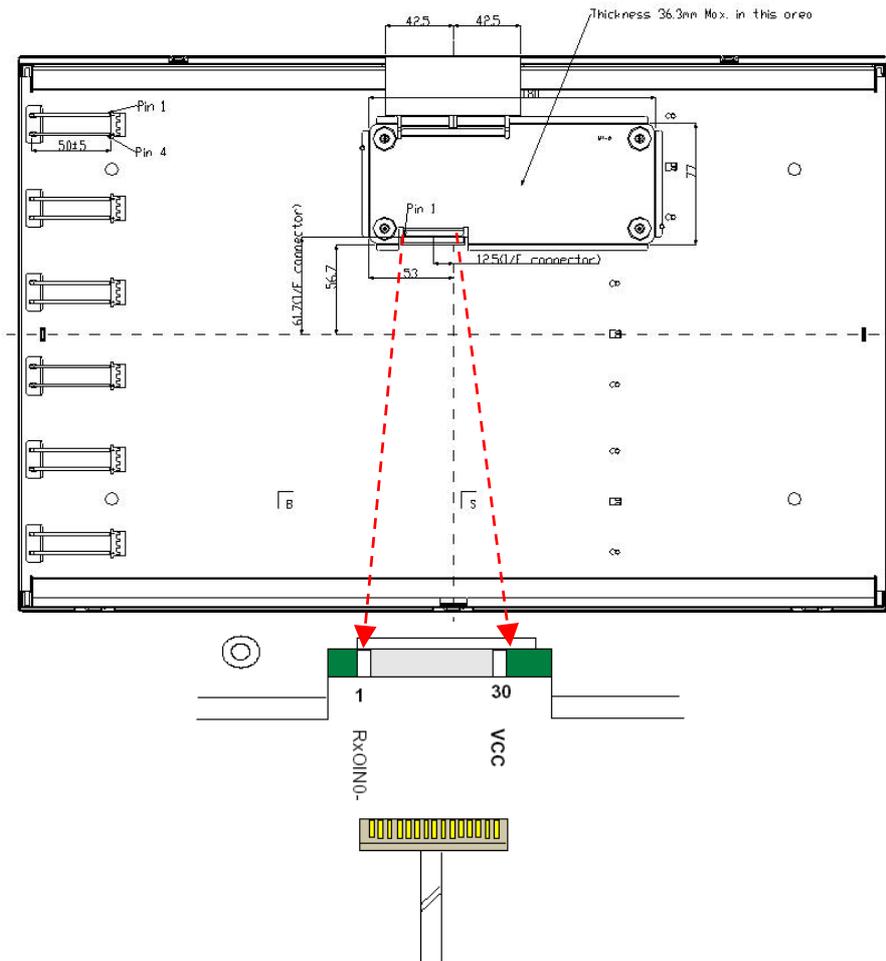
**Note 1:** R/G/B data 7:MSB, R/G/B data 0:LSB  
O = "First Pixel Data"  
E = "Second Pixel Data"

## 6.3 Signal Description

The module using one LVDS receiver SN75LVDS82(Texas Instruments) or compatible. LVDS is a differential signal technology for LCD interface and high speed data transfer device. Transmitter shall be SN75LVDS83(negative edge sampling) or compatible. The first LVDS port(RxOxxx) transmits odd pixels while the second LVDS port(RxExxx) transmits even pixels.

PIN #	SIGNAL NAME	DESCRIPTION
1	RxOIN0-	Negative LVDS differential data input (Odd data)
2	RxOIN0+	Positive LVDS differential data input (Odd data)
3	RxOIN1-	Negative LVDS differential data input (Odd data)
4	RxOIN1+	Positive LVDS differential data input (Odd data)
5	RxOIN2-	Negative LVDS differential data input (Odd data, DSPTMG)
6	RxOIN2+	Positive LVDS differential data input (Odd data, DSPTMG)
7	GND	Power Ground
8	RxOCLK-	Negative LVDS differential clock input (Odd clock)
9	RxOCLK+	Positive LVDS differential clock input (Odd clock)
10	RxOIN3-	Negative LVDS differential data input (Odd data)
11	RxOIN3+	Positive LVDS differential data input (Odd data)
12	RxEIN0-	Negative LVDS differential data input (Even data)
13	RxEIN0+	Positive LVDS differential data input (Even data)
14	GND	Power Ground
15	RxEIN1-	Positive LVDS differential data input (Even data)
16	RxEIN1+	Negative LVDS differential data input (Even data)
17	GND	Power Ground
18	RxEIN2-	Negative LVDS differential data input (Even data)
19	RxEIN2+	Positive LVDS differential data input (Even data)
20	RxECLK-	Negative LVDS differential clock input (Even clock)
21	RxECLK+	Positive LVDS differential clock input (Even clock)
22	RxEIN3-	Negative LVDS differential data input (Even data)
23	RxEIN3+	Positive LVDS differential data input (Even data)
24	GND	Power Ground
25	NC	No connection
26	NC	No connection
27	VDD	Power +5V
28	VDD	Power +5V
29	VDD	Power +5V
30	VDD	Power +5V

Note1: Start from left side



**Note2:** Input signals of odd and even clock shall be the same timing.

## 6.4 Timing Characteristics

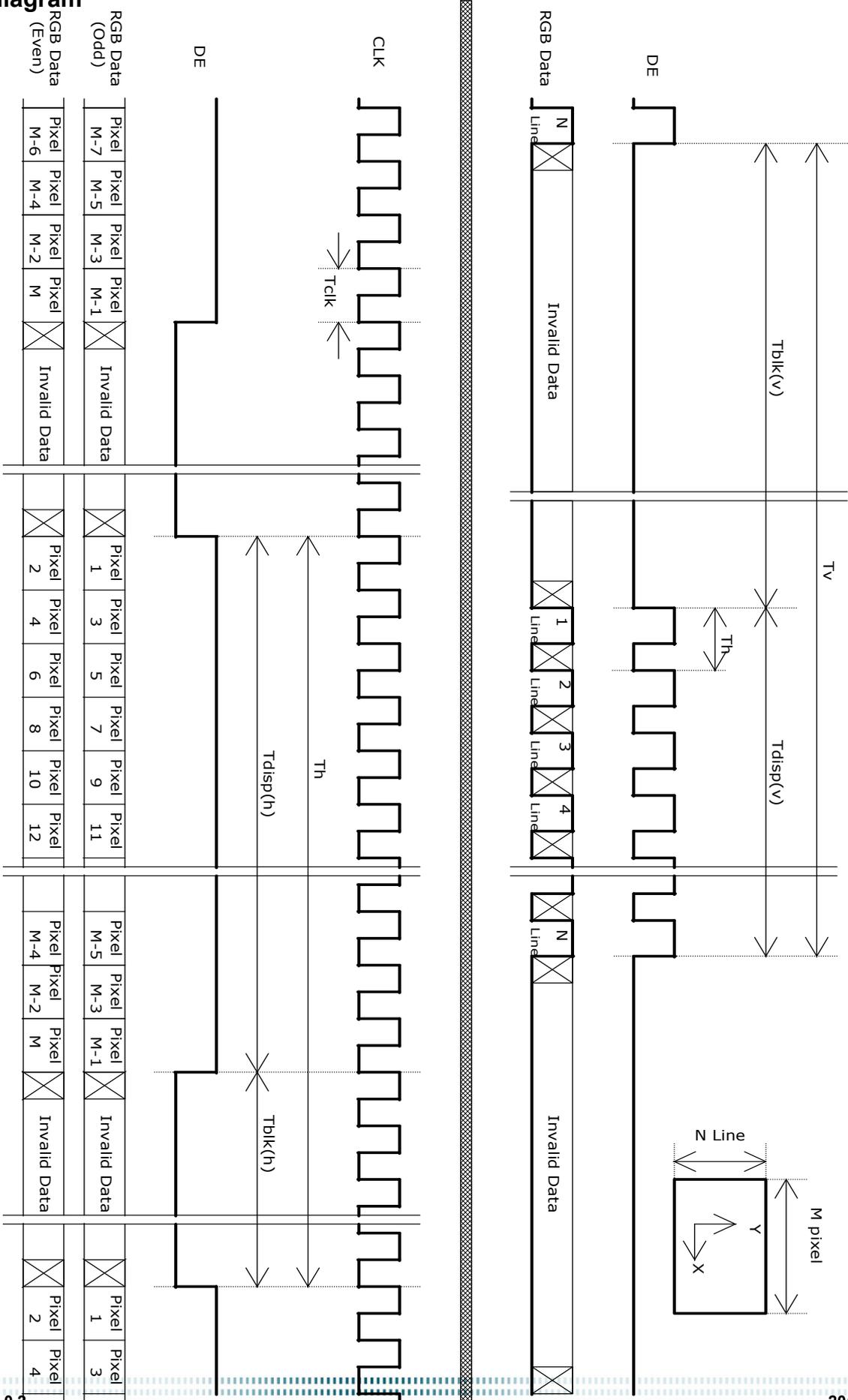
Basically, interface timings described here is not actual input timing of LCD module but output timing of SN75LVDS82DGG (Texas Instruments) or equivalent.

**Note:** Typical value refer to VESA STANDARD

Signal	Item	Symbol	Min	Typ	Max	Unit
Vertical Section	Period	Tv	1211	1212	2048	Th
	Active	Tdisp(v)	1200	1200	1200	Th
	Blanking	Tblk(v)	11	12	-	Th
Horizontal Section	Period	Th	1040	1072	2048	Tclk
	Active	Tdisp(h)	960	960	960	Tclk
	Blanking	Tblk(h)	80	112	-	Tclk
Clock	Period	Tclk	11.76	-	-	ns
	Frequency	Freq	-	-	85	MHz
Frame Rate	Frequency	Vsync	47	60	65	Hz

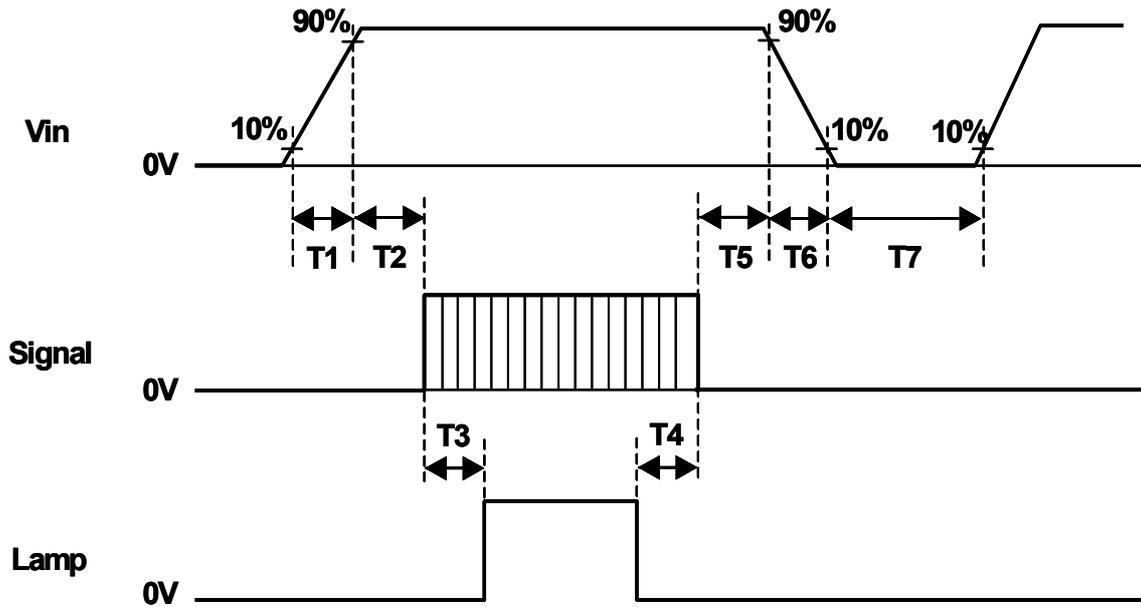
Note : DE mode only

## 6.5 Timing diagram



## 6.6 Power ON/OFF Sequence

Vin power and lamp on/off sequence is as follows. Interface signals are also shown in the chart. Signals from any system shall be Hi-Z state or low level when Vin is off.



Symbol	Values			Unit
	Min	Typ	Max	
T1	0.3	-	10	[ms]
T2	0.5	40	50	[ms]
T3	300	-	-	[ms]
T4	300	-	-	[ms]
T5	0.5	16	50	[ms]
T6	0.5	-	60	[ms]
T7	1000	-	-	[ms]

## 7.0 Connector & Pin Assignment

Physical interface is described as for the connector on module.

These connectors are capable of accommodating the following signals and will be following components.

### 7.1 TFT LCD Module

Connector Name / Designation	Interface Connector / Interface card
Manufacturer	JAE or compatible
Type Part Number	FI-XB30SSL-HF15
Mating Housing Part Number	FI-X30HL-T (Locked Type)
	FI-X30S-H (Unlocked Type)

#### 7.1.1 Pin Assignment

Pin#	Signal Name	Pin#	Signal Name
1	RxOIN0-	2	RxOIN0+
3	RxOIN1-	4	RxOIN1+
5	RxOIN2-	6	RxOIN2+
7	GND	8	RxOCLKIN-
9	RxOCLKIN+	10	RxOIN3-
11	RxOIN3+	12	RxEIN0-
13	RxEIN0+	14	GND
15	RxEIN1-	16	RxEIN1+
17	GND	18	RxEIN2-
19	RxEIN2+	20	RxECLKIN-
21	RxECLKIN+	22	RxEIN3-
23	RxEIN3+	24	GND
25	NV	26	NC
27	VDD	28	VDD
29	VDD	30	VDD

## 7.2 Backlight Unit

Physical interface is described as for the connector on module. These connectors are capable of accommodating the following signals and will be following components.

Connector Name / Designation	Lamp Connector / Backlight lamp
Manufacturer	JST
Type Part Number	BHR-04VS-1
Mating Type Part Number	SM02(12)B-BH

### 7.2.1 Signal for Lamp connector

Connector	Pin No.	Input	Color	Function
CN1	1	Hot	Pink	High Voltage
	4	Hot	White	High Voltage
CN2	1	Hot	Pink	High Voltage
	4	Hot	White	High Voltage
CN3	1	Hot	Pink	High Voltage
	4	Hot	White	High Voltage
CN4	1	Hot	Pink	High Voltage
	4	Hot	White	High Voltage
CN5	1	Hot	Pink	High Voltage
	4	Hot	White	High Voltage
CN6	1	Hot	Pink	High Voltage
	4	Hot	White	High Voltage

## 8.0 Reliability Test

Environment test conditions are listed as following table.

Items	Required Condition	Note
Temperature Humidity Bias (THB)	Ta= 50°C , 80%RH, 300hours	
High Temperature Operation (HTO)	Ta= 50°C , 50%RH, 300hours	
Low Temperature Operation (LTO)	Ta= 0°C , 300hours	
High Temperature Storage (HTS)	Ta= 60°C , 300hours	
Low Temperature Storage (LTS)	Ta= -20°C , 300hours	
Vibration Test (Non-operation)	Acceleration: 1.5 G Wave: Random Frequency: 10 - 200 - 10 Hz Sweep: 30 Minutes each Axis (X, Y, Z)	
Shock Test (Non-operation)	Acceleration: 50 G Wave: Half-sine Active Time: 20 ms Direction: ±X, ±Y, ±Z (one time for each Axis)	
Drop Test	Height: 60 cm, package test	
Thermal Shock Test (TST)	-20°C/30min, 60°C/30min, 100 cycles	1
On/Off Test	On/10sec, Off/10sec, 30,000 cycles	
ESD (ElectroStatic Discharge)	Contact Discharge: ± 8KV, 150pF(330Ω ) 1sec, 8 points, 25 times/ point.	2
	Air Discharge: ± 15KV, 150pF(330Ω ) 1sec 8 points, 25 times/ point.	
Altitude Test	Operation:10,000 ft Non-Operation:30,000 ft	

Note 1: The TFT-LCD module will not sustain damage after being subjected to 100 cycles of rapid temperature change. A cycle of rapid temperature change consists of varying the temperature from -20°C to 60°C, and back again. Power is not applied during the test. After temperature cycling, the unit is placed in normal room ambient for at least 4 hours before power on.

Note 2: According to EN61000-4-2 , ESD class B: Some performance degradation allowed. No data lost. Self-recoverable. No hardware failures.

## 9.0 Shipping Label

The label is on the panel as shown below:





