

# DATA SHEET

## **SSTL16877**

14-bit SSTL\_2 registered driver with  
differential clock inputs

Product specification  
Supersedes data of 2000 Apr 11

2000 Apr 20

# 14-bit SSTL\_2 registered driver with differential clock inputs

## SSTL16877

### FEATURES

- Stub-series terminated logic for 2.5 V VDDQ (SSTL\_2)
- Optimized for DDR (Double Data Rate) SDRAM applications
- Supports SSTL\_2 signal inputs and outputs
- Flow-through architecture optimizes PCB layout
- Meets SSTL\_2 class I and class II specifications
- Latch-up protection exceeds 500mA per JEDEC Std 17
- ESD protection exceeds 2000 V per MIL STD 833 Method 3015 and 200 V per Machine Model
- Full DDR solution provided when used with PCK877 and CBT3867

### DESCRIPTION

The SSTL16877 is a 14-bit SSTL\_2 registered driver with differential clock inputs, designed to operate between 2.3 V and 2.7 V. V<sub>DDQ</sub> must not exceed V<sub>CC</sub>. Inputs are SSTL\_2 type with V<sub>REF</sub> normally at 0.5\*V<sub>DDQ</sub>. The outputs support class I which can be used for standard stub-series applications or capacitive loads. Master reset (RESET) asynchronously resets all registers to zero.

The SSTL16877 is intended to be incorporated into standard DIMM (Dual In-Line Memory Module) designs defined by JEDEC, such as DDR (Double Data Rate) SDRAM or SDRAM II Memory Modules. Different from traditional SDRAM, DDR SDRAM transfers data on both clock edges (rising and falling), thus doubling the peak bus bandwidth. A DDR DRAM rated at 166 MHz will have a burst rate of 333 MHz. The modules require between 23 and 27 registered control and address lines, so two 14-bit wide devices will be used on each module. The SSTL16877 is intended to be used for SSTL\_2 input and output signals.

The device data inputs consist of differential receivers. One differential input is tied to the input pin while the other is tied to a reference input pad, which is shared by all inputs.

The clock input is fully differential to be compatible with DRAM devices that are installed on the DIMM. However, since the control inputs to the SDRAM change at only half the data rate, the device must only change state on the positive transition of the CLK signal. In order to be able to provide defined outputs from the device even before a stable clock has been supplied, the device must support an asynchronous input pin (reset), which when held to the LOW state will assume that all registers are reset to the LOW state and all outputs drive a LOW signal as well.

### QUICK REFERENCE DATA

GND = 0 V; T<sub>amb</sub> = 25°C; t<sub>r</sub> = t<sub>f</sub> ≤ 2.5 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t <sub>PHL</sub> /t <sub>PLH</sub>	Propagation delay; CLK to Qn	C <sub>L</sub> = 30 pF; V <sub>DDQ</sub> = 2.5 V	2.4	ns
C <sub>I</sub>	Input capacitance	V <sub>CC</sub> = 2.5 V	2.9	pF

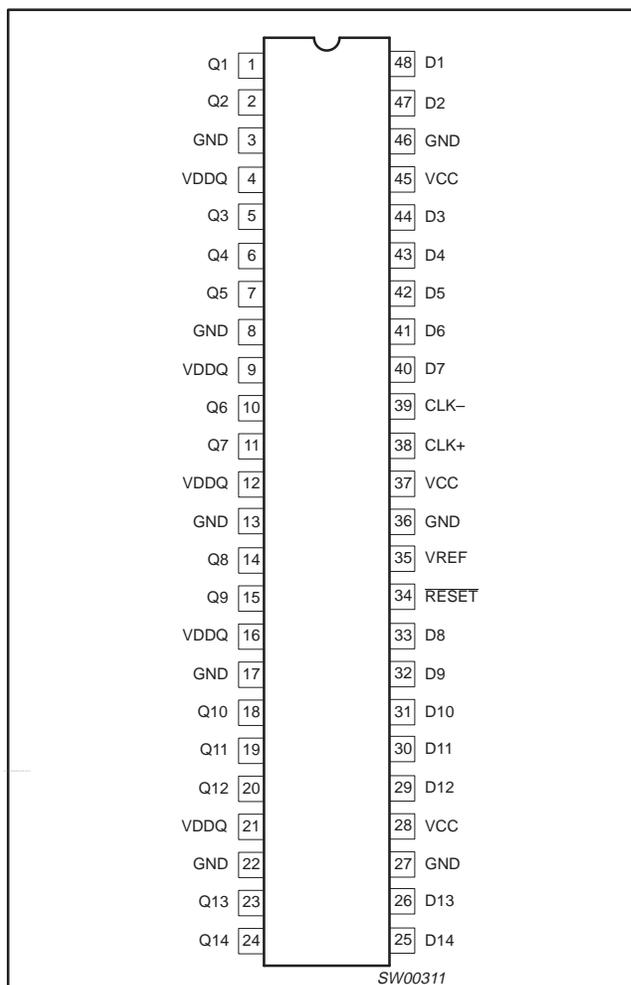
#### NOTES:

1. C<sub>PD</sub> is used to determine the dynamic power dissipation (P<sub>D</sub> in μW) P<sub>D</sub> = C<sub>PD</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>i</sub> + ∑ (C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) where:  
f<sub>i</sub> = input frequency in MHz; C<sub>L</sub> = output load capacity in pF; f<sub>o</sub> = output frequency in MHz; V<sub>CC</sub> = supply voltage in V;  
∑ (C<sub>L</sub> × V<sub>CC</sub><sup>2</sup> × f<sub>o</sub>) = sum of the outputs.

### ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	ORDER CODE	DWG NUMBER
48-Pin Plastic TSSOP Type I	0°C to +70°C	SSTL16877 DGG	SOT362-1

### PIN CONFIGURATION



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## PIN DESCRIPTION

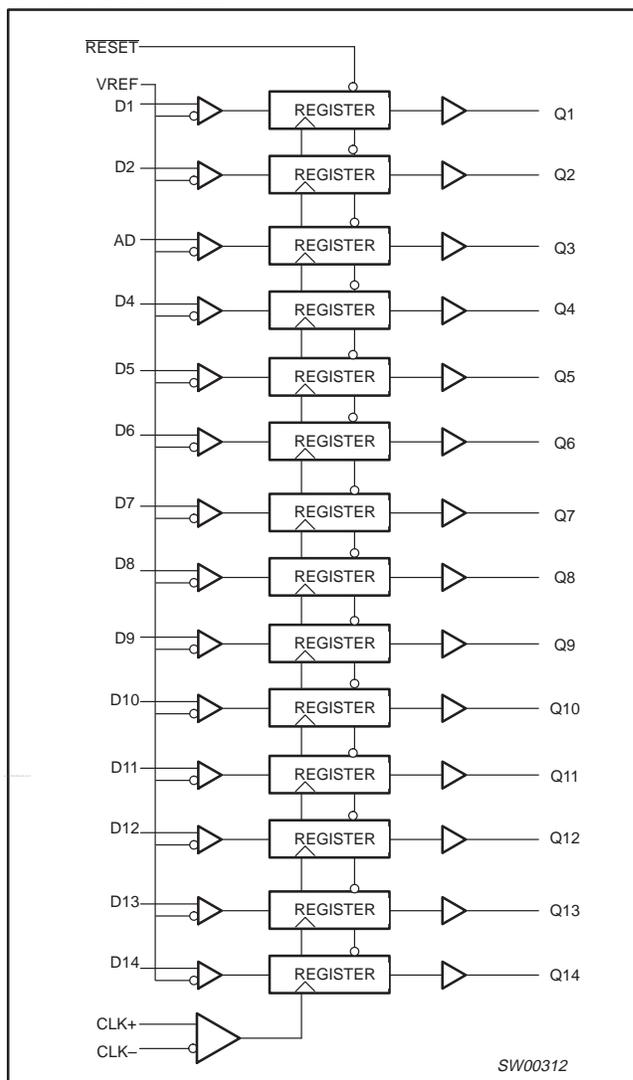
PIN NUMBER	SYMBOL	NAME AND FUNCTION
34	RESET	LVC MOS asynchronous master reset (Active LOW)
48, 47, 44, 43, 42, 41, 40, 33, 32, 31, 30, 29, 26, 25	D1 – D14	SSTL_2 data inputs
1, 2, 5, 6, 7, 10, 11, 14, 15, 18, 19, 20, 23, 24	Q1 – Q14	SSTL_2 data outputs
35	VREF	SSTL_2 input reference level
3, 8, 13, 17, 22, 27, 36, 46	GND	Ground (0 V)
28, 37, 45	V <sub>CC</sub>	Positive supply voltage
4, 9, 12, 16, 21	V <sub>DDQ</sub>	Output supply voltage
38 39	CLK+ CLK-	Differential clock inputs

## FUNCTION TABLE

INPUTS				OUTPUT
RESET	CLK	CLK	D	Q
L	X	X	X	L
H	↓	↑	H	H
H	↓	↑	L	L
H	L or H	L or H	X	Q <sub>0</sub>

H = High voltage level  
 L = Low voltage level  
 ↓ = High-to-Low transition  
 ↑ = Low-to-High transition  
 X = Don't care

## LOGIC DIAGRAM



## ABSOLUTE MAXIMUM RATINGS<sup>1, 2</sup>

SYMBOL	PARAMETER	CONDITION	LIMITS		UNIT
			MIN	MAX	
V <sub>CC</sub>	DC supply voltage		-0.5	+4.6	V
I <sub>IK</sub>	DC input diode current	V <sub>I</sub> < 0		-50	mA
V <sub>I</sub>	DC input voltage <sup>3</sup>		-0.5	V <sub>DDQ</sub> + 0.5	V
I <sub>OK</sub>	DC output diode current	V <sub>O</sub> < 0		-50	mA
V <sub>OUT</sub>	DC output voltage <sup>3</sup>	Note 3	-0.5	V <sub>DDQ</sub> + 0.5	V
I <sub>OUT</sub>	DC output current	V <sub>O</sub> = 0 to V <sub>DDQ</sub>		±50	mA
	Continuous current <sup>4</sup>	V <sub>CC</sub> , V <sub>DDQ</sub> , or GND		±100	
T <sub>STG</sub>	Storage temperature range		-65	+150	°C

### NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
- The continuous current at V<sub>CC</sub>, V<sub>DDQ</sub>, or GND should not exceed ±100 mA.

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## RECOMMENDED OPERATING CONDITIONS<sup>1</sup>

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V <sub>CC</sub>	Supply voltage		2.3	2.5	2.7	V
V <sub>DDQ</sub>	Output supply voltage		2.3	2.5	2.7	V
V <sub>REF</sub>	Reference voltage (V <sub>REF</sub> = 0.5 x V <sub>DDQ</sub> )		1.15	1.25	1.35	V
V <sub>TT</sub>	Termination voltage		V <sub>REF</sub> - 40 mV	V <sub>REF</sub>	V <sub>REF</sub> + 40 mV	V
V <sub>I</sub>	Input voltage		0		V <sub>CC</sub>	V
V <sub>IH</sub>	AC HIGH-level input voltage	All inputs	V <sub>REF</sub> + 350 mV			V
V <sub>IL</sub>	AC LOW-level input voltage	All inputs			V <sub>REF</sub> - 350 mV	V
V <sub>IH</sub>	DC HIGH-level input voltage	All inputs	V <sub>REF</sub> + 180 mV		V <sub>DDQ</sub> + 0.5 V	V
V <sub>IL</sub>	DC LOW-level input voltage	All inputs	V <sub>SS</sub> - 0.5 V		V <sub>REF</sub> - 180 mV	V
I <sub>OH</sub>	HIGH-level output current				-20	mA
I <sub>OL</sub>	LOW-level output current				20	mA
T <sub>amb</sub>	Operating free-air temperature range		0		70	°C

### NOTE:

- Unused control inputs must be held HIGH or LOW to prevent them from floating.

## DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT	
			Temp = 0°C to +70°C				
			MIN	TYP <sup>2</sup>	MAX		
V <sub>IK</sub>	I/O supply voltage	V <sub>CC</sub> = 2.3 V; I <sub>I</sub> = -18 mA			-1.2	V	
V <sub>OH</sub>	HIGH level output voltage	V <sub>CC</sub> = 2.3 V to 2.7 V; I <sub>OH</sub> = -100 μA	V <sub>CC</sub> - 0.2	2.3			
		V <sub>CC</sub> = 2.3 V; I <sub>OH</sub> = -8 mA	1.95	2.2			
		V <sub>CC</sub> = 2.3 V; I <sub>OH</sub> = -16 mA	1.95	2.1			
V <sub>OL</sub>	LOW level output voltage	V <sub>CC</sub> = 2.3 V to 2.7 V; I <sub>OL</sub> = -100 μA		0.002	0.2	V	
		V <sub>CC</sub> = 2.3 V; I <sub>OL</sub> = -8 mA		0.14	0.35		
		V <sub>CC</sub> = 2.3 V; I <sub>OL</sub> = -16 mA		0.30	0.35		
V <sub>CMR</sub>	CLK, $\overline{\text{CLK}}$	Common mode range for reliable performance	0.97		1.53	V	
V <sub>PP</sub>	CLK, $\overline{\text{CLK}}$	Minimum peak-to-peak input to ensure logic state	360			mV	
I <sub>I</sub>	Data inputs, RESET	V <sub>CC</sub> = 2.7 V; V <sub>I</sub> = 1.7 V or 0.8 V	V <sub>REF</sub> = 1.15V or 1.35V		0.01	±5	μA
		V <sub>CC</sub> = 2.7 V; V <sub>I</sub> = 2.7 V or 0 V			0.01	±5	
	CLK, $\overline{\text{CLK}}$	V <sub>CC</sub> = 2.7 V; V <sub>I</sub> = 1.7 V or 0.8 V	V <sub>REF</sub> = 1.15V or 1.35V		0.05	±5	μA
		V <sub>CC</sub> = 2.7 V; V <sub>I</sub> = 2.7 V or 0 V			0.05	±5	
I <sub>CC</sub>	Quiescent supply current CLK and $\overline{\text{CLK}}$ in opposite state <sup>1</sup>	V <sub>CC</sub> = 2.7 V; V <sub>I</sub> = 1.7 V or 0.8 V			12	25	mA
		V <sub>CC</sub> = 2.7 V; V <sub>I</sub> = 2.7 V or 0 V			10	25	

### NOTES:

- When CLK and  $\overline{\text{CLK}}$  are HIGH, typical I<sub>CC</sub> = 25 mA.
- All typical values are at V<sub>CC</sub> = 3.3 V and T<sub>amb</sub> = 25°C (unless otherwise specified).

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## TIMING REQUIREMENTS

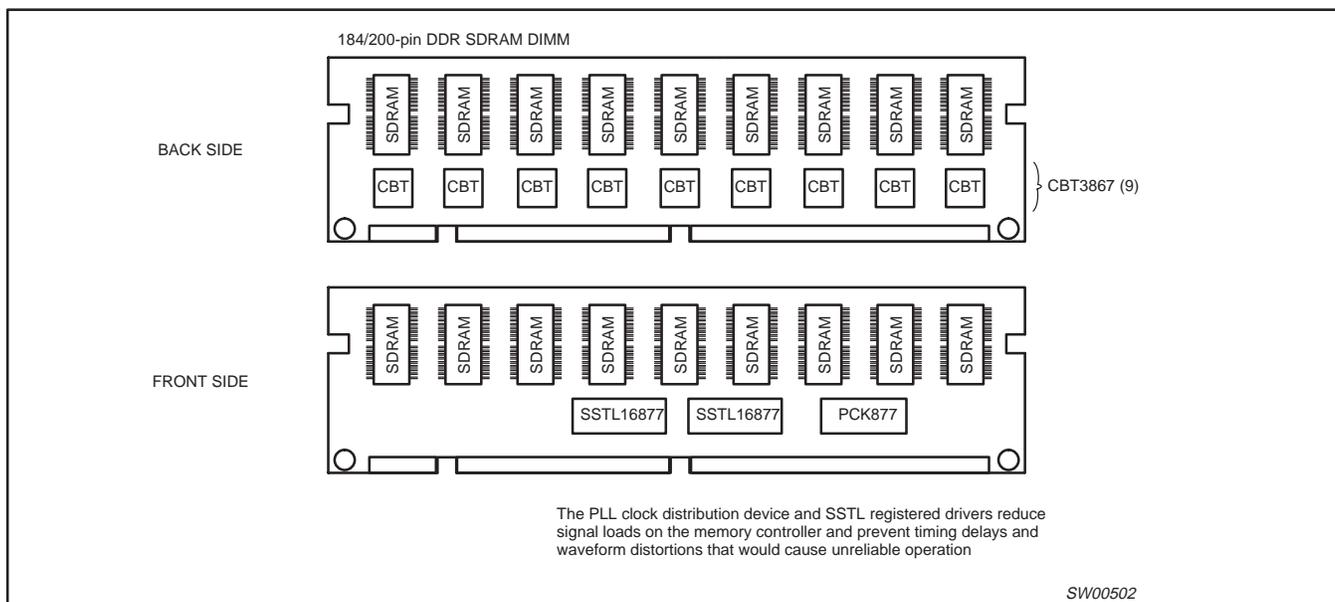
Over recommended operating conditions;  $T_{amb} = 0^{\circ}\text{C}$  to  $+70^{\circ}\text{C}$  (unless otherwise noted) (see Figure 1)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS		UNIT
			$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$		
			MIN	MAX	
$f_{\text{clock}}$	Clock frequency			200	MHz
$t_w$	Pulse duration, CLK, $\overline{\text{CLK}}$ HIGH or LOW		1.0		ns
$t_{\text{su}}$	Setup time	Data before $\text{CLK}\uparrow$ , $\text{CLK}\downarrow$	0.2		ns
		$\overline{\text{RESET}}$ HIGH before $\text{CLK}\uparrow$ , $\text{CLK}\downarrow$	0.8		
$t_h$	Hold time		1.2		ns

## SWITCHING CHARACTERISTICS

Over recommended operating conditions;  $T_{amb} = 0^{\circ}\text{C}$  to  $+70^{\circ}\text{C}$ ;  $V_{DDQ} = 2.3 - 2.7\text{ V}$  and  $V_{DDQ}$  does not exceed  $V_{CC}$ . Class I,  $V_{REF} = V_{TT} = V_{DDQ} \times 0.5$  and  $C_L = 10\text{ pF}$  (unless otherwise noted) (see Figure 1)

SYMBOL	FROM (INPUT)	TO (OUTPUT)	LIMITS		UNIT
			$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$		
			MIN	MAX	
$f_{\text{max}}$	Maximum clock frequency		200		MHz
$t_{\text{PLH}}/t_{\text{PHL}}$	CLK and $\overline{\text{CLK}}$	Q	1.0	3.5	ns
$t_{\text{PHL}}$	RESET	Q	2.0	4.0	ns

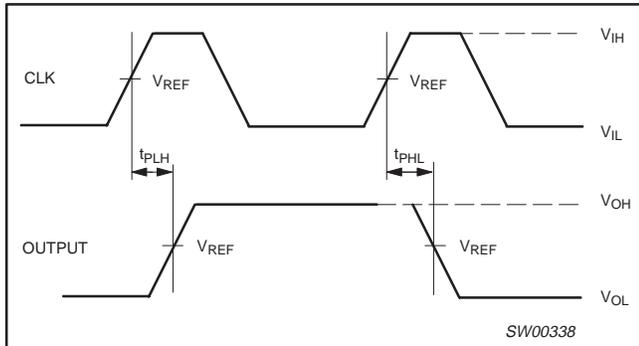


# 14-bit SSTL\_2 registered driver with differential clock inputs

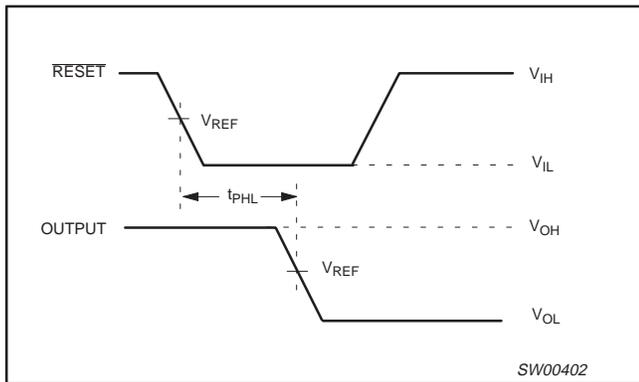
SSTL16877

## PARAMETER MEASUREMENT INFORMATION

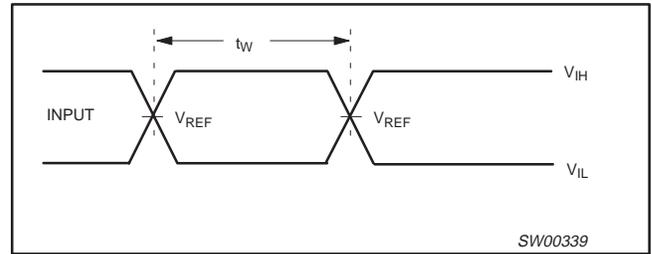
### AC WAVEFORMS



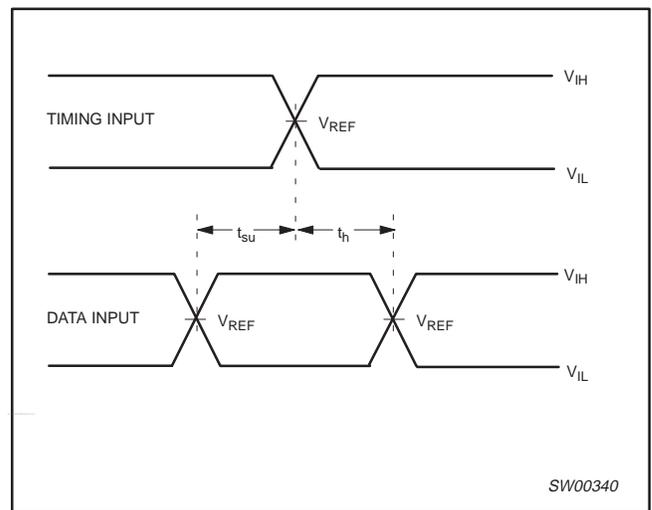
Waveform 1. Propagation delay times inverting and non-inverting outputs



Waveform 2. Propagation delay  $\overline{\text{RESET}}$  to output.



Waveform 3. Pulse duration



Waveform 4. Setup and hold times

### TEST CIRCUIT

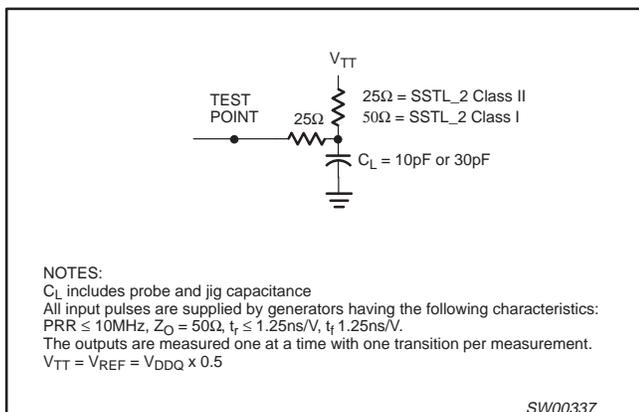


Figure 1. Load circuitry

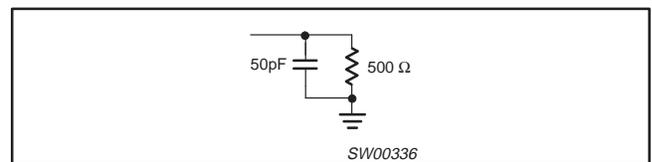


Figure 2.

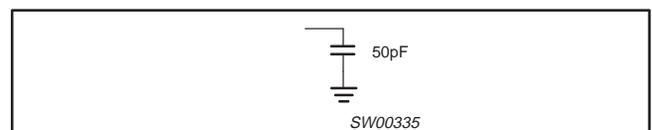


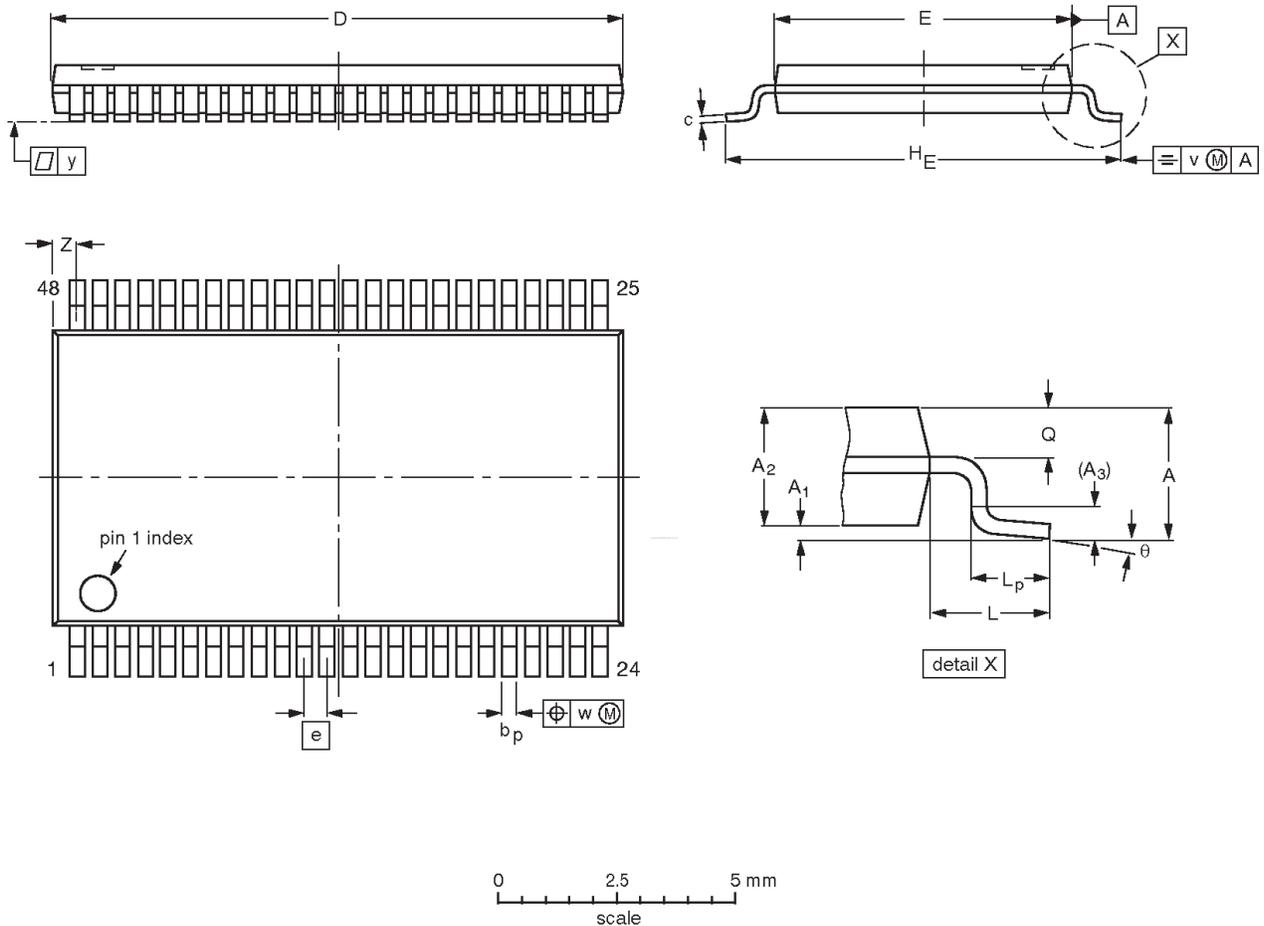
Figure 3.

# 14-bit SSTL\_2 registered driver with differential clock inputs

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**TSSOP48:** plastic thin shrink small outline package; 48 leads; body width 6.1 mm

**SOT362-1**



**DIMENSIONS (mm are the original dimensions).**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(2)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z	θ
mm	1.2	0.15 0.05	1.05 0.85	0.25	0.28 0.17	0.2 0.1	12.6 12.4	6.2 6.0	0.5	8.3 7.9	1	0.8 0.4	0.50 0.35	0.25	0.08	0.1	0.8 0.4	8° 0°

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT362-1		MO-153				-95-02-10 99-12-27

# 14-bit SSTL\_2 registered driver with differential clock inputs

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## Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued datasheet before initiating or completing a design.

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