

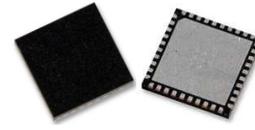
TAT6281

FTTH Variable Gain Receiver



Applications

- High Gain, low noise FTTH Receiver
- TIA, Multi-Dwelling Unit

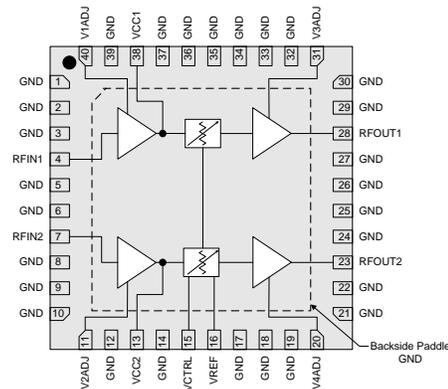


40 Pin 6x6 mm leadless SMT Package

Product Features

- 45-1003 MHz bandwidth
- Compact 6x6 mm integrated package
- 5v, 300 mA bias
- Variable gain attenuator: 20 dB typical range
- Max gain setting: 33 dB typical
- 17 dB typical return loss across gain range
- 3.8 dB pA/rtHz typical EIN
- -8 to +1 dBm optical input range
- 19 dBmV typical RF Output

Functional Block Diagram



General Description

The TAT6281 FTTP SFU Video Receiver provides a low noise analog interface to optical triplexers. The TAT6281 is intended for use in single family unit (SFU) analog video fiber to the premise (FTTP) applications.

The TAT6281 exhibits low input noise and distortion that provides performance margin critical to meeting stringent FTTP link requirements. It runs on a single 5 volt supply, eliminating the need for an extra ONT power supply.

The TAT6281 provides integrated automatic gain control (AGC) to maintain a constant 19 dBmV output to insure a consistent video quality and ease of design.

The TAT6281 is fabricated using 6-inch GaAs pHEMT technology to optimize performance and cost.

Pin Configuration

Pin #	Symbol
1-3, 5-6, 8-10, 12, 14, 17-19, 21-22, 24-27, 29-30, 32-37, 39	GND
4 / 7	RFIN1 / RFIN2
11	V2ADJ
40	V1ADJ
13 / 38	VCC2 / VCC1
15	VCTRL
16	VREF
20	V4ADJ
23 / 28	RFOUT2 / RFOUT1
31	V3ADJ
Backside Paddle	GND

Ordering Information

Part No.	Description
TAT6281	FTTH Variable Gain Receiver
TAT6281-PCB	45-1003 MHz Evaluation Board

Standard T/R size = TBD pieces on a TBD" reel

Specifications

Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	-55 to 150 °C
RF Input Power, CW, 75 Ω, T=25°C	-
V _{CC} (pins 13, 23, 28, 38)	+10 V
V _{REF} and V _{CTRL}	+10 V

Operation of this device outside the parameter ranges given above may cause permanent damage.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
V _{SUPPLY}	4.75	5.0	5.25	V
T _{CASE}	-40		+85	°C
T _j (for >10 ⁶ hours MTTF)			+150	°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

Test conditions unless otherwise noted: V_{CC}=+5 V, I_{CC} = 300 mA, T_{CASE} = +25 °C, 75 Ω system

Parameter	Conditions	Min	Typical	Max	Units
Operational Frequency Range		45		1003	MHz
Gain	At 1003 MHz, min. AGC attenuation		33		dB
Gain Flatness	See Note 1.		± 1.25		dB
Tilt			7		dB
Output Return Loss	45-1003 MHz		17		dB
Attenuation Range			20		dB
Equivalent Input Noise			3.8		pA/rtHz
Composite Second Order (see note 2.)	80 Channels, 3.3% OMI, 6 MHz spaced, +1 dbm optical input power		-64		dBc
Composite Triple Beat (see note 2.)	80 Channels, 3.3% OMI, 6 MHz spaced, +1 dbm optical input power		-64		dBc
Thermal Resistance (jnc to case) θ _{jc}				-	°C/W

Notes:

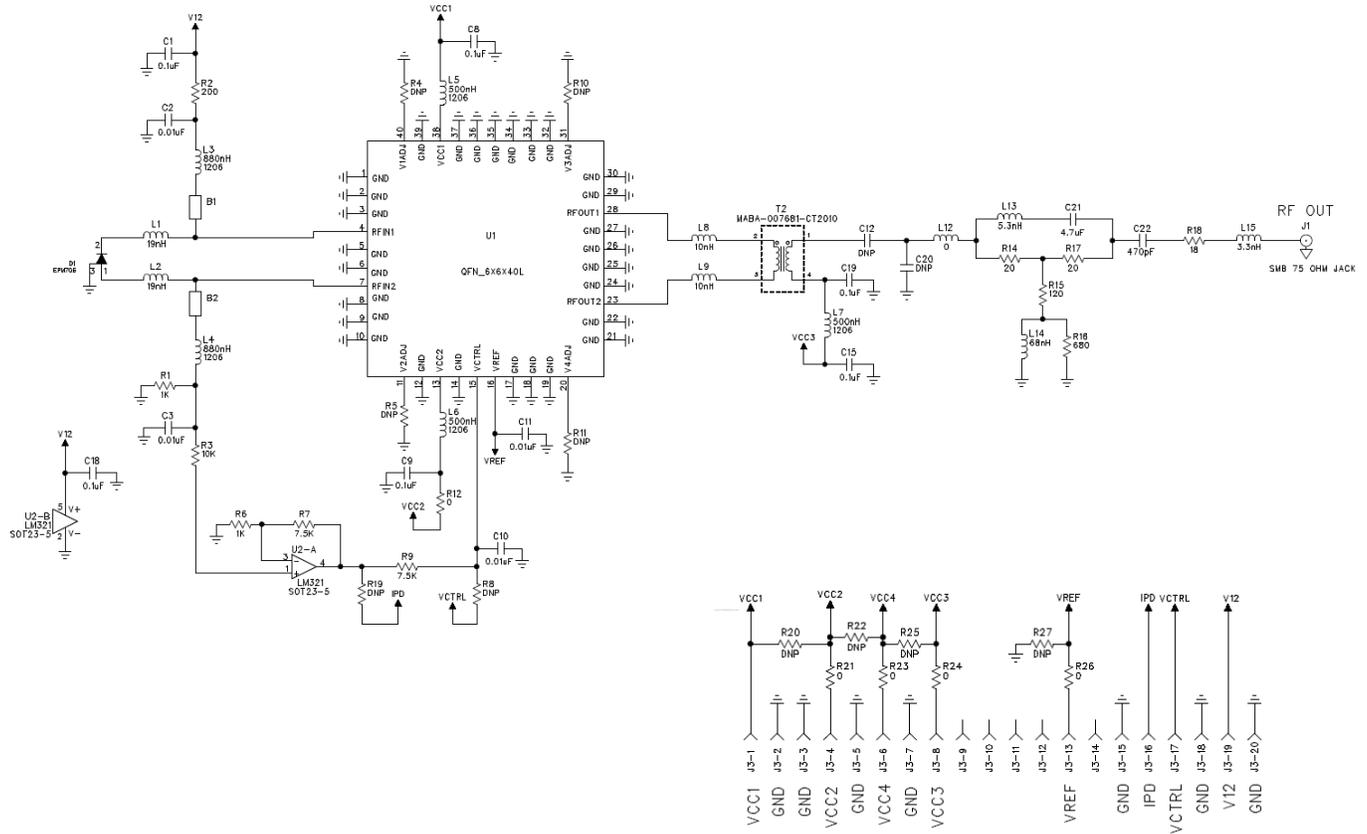
1. Calculated using the least mean squares method.
2. Data presented includes non-linearity contribution from laser transmitter.

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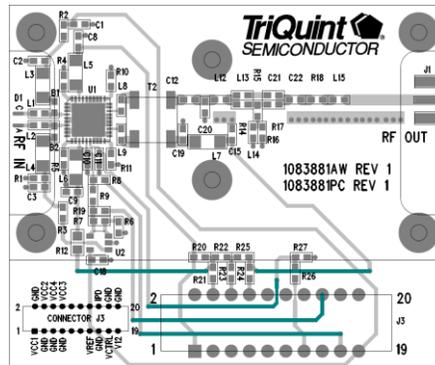
Application Circuit – TAT6281-PCB



TAT6281

FTTH Variable Gain Receiver

Application Circuit – TAT6281-PCB



Bill of Material: TAT6281-PCB

Reference Des.	Value	Description	Manuf.	Part Number
U1	n/a		TQNT	TAT6281
D1	n/a	Photo Diode	JDSU	EPM705 SC/APC
T2	n/a	2:1 Transformer	M/A COM	MABA-007681-CT-2010
L1, L2	16 nH	Wire-wound Inductor 603	Coil craft	0603CT-16NXJLU
L3,L4,L5,L6,L7	880 nH	Ind 1206 Ferrite Core Wirewound	Murata	LQH31HNR88K
L13	7.5 nH	Wirewound Inductor 603	Coil craft	0603CS-7N5XJLU
L14	10 nH	Wirewound Inductor 603	Coil craft	0603CS-10NXJLU
C1,C2,C3,C8,C9, C10,C11, C15,C19	1 uF	Cap Chip Ceramic 0603	Murata	GRM188C81E105KAADD
C12	0.1 uF	Cap Chip Ceramic 0603	Murata	GRM188R72A104KA35D
C21	4 pF	Cap Chip Ceramic 0603	Murata	GRM1885C1H4R0CZ01D
B1,B2	0 ohm	Res Chip 0603	Panasonic	ERJ-3GEY0R00V
R1,R27	1 Kohm	Res Chip 0603	Panasonic	ERJ-3EKF1001V
R2	200 ohm	Res Chip 0603	Panasonic	ERJ-3EKF2000V
R4,R5	8.2 Kohm	Res Chip 0603	Panasonic	ERJ-3EKF8201V
R10, R11	2.2 Kohm	Res Chip 0603	Panasonic	ERJ-3EKF2201V
R14,R17	27 ohm	Res Chip 0603	Panasonic	ERJ-3EKF27R0V
R15	75 ohm	Res Chip 0603	Panasonic	ERJ-3EKF75R0V
R16	510 ohm	Res Chip 0603	Panasonic	ERJ-3EKF5100V
R26	270 ohm	Res Chip 0603	Panasonic	ERJ-3EKF2700V
C22,L8,L9,L12,L15,R8,R1 2,R18,R21,R23,R24	0 ohm	Res Chip 0603	Panasonic	ERJ-3GEY0R00V
U2,C18,C20,R3,R6,R7, R9,R19,R20,R22,R25	n/a	DNP	n/a	n/a

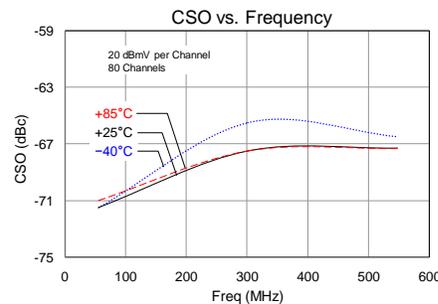
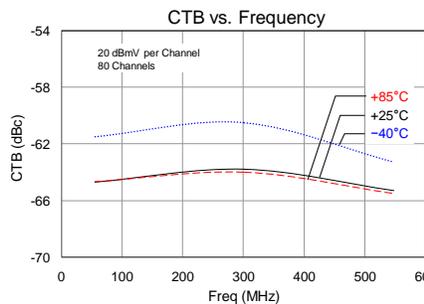
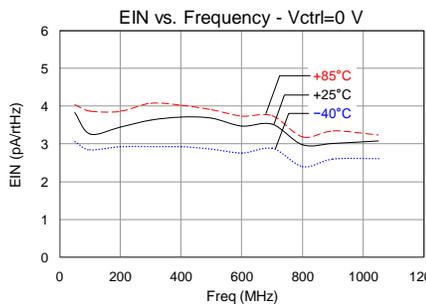
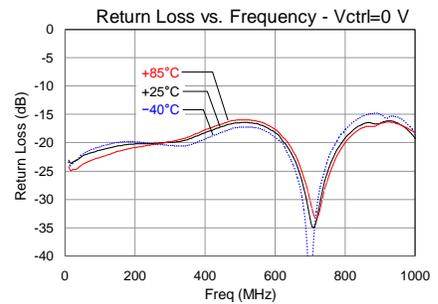
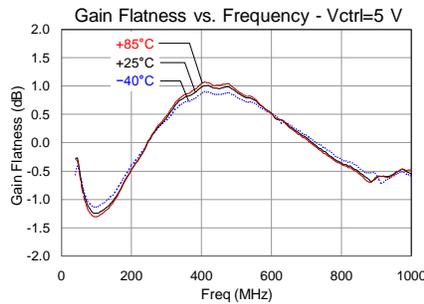
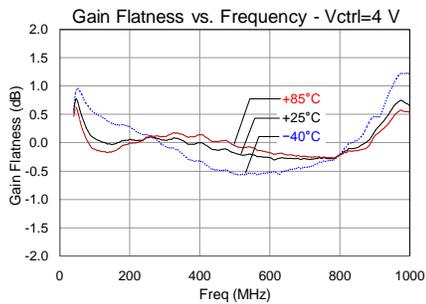
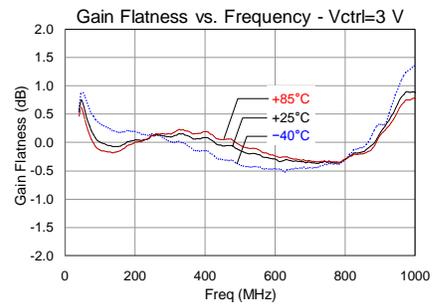
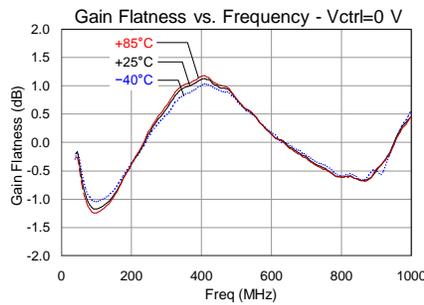
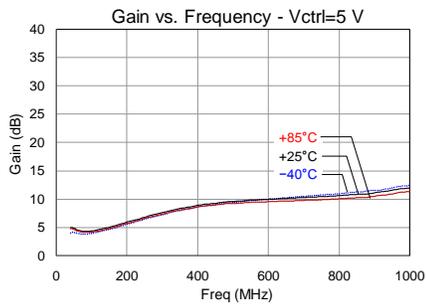
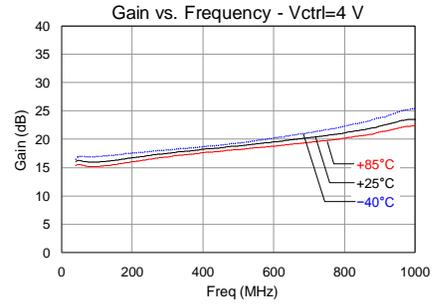
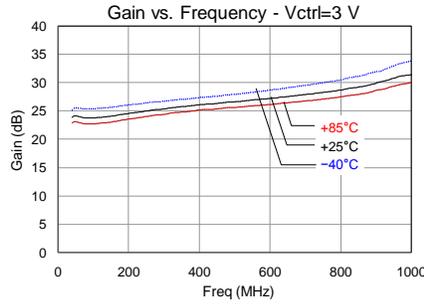
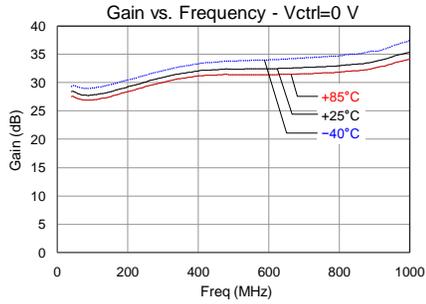
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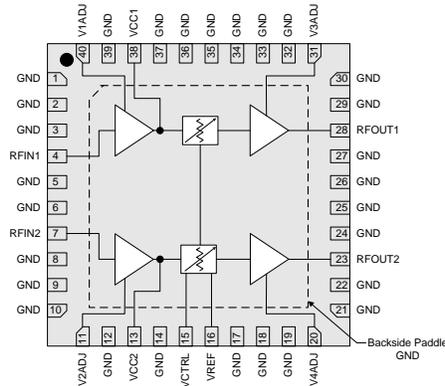


Performance Plots

Test conditions unless otherwise noted: $V_{CC}=+5\text{ V}$, $I_{CC} = 300\text{ mA}$, $T_{CASE} = +25^\circ\text{C}$, $75\ \Omega$ system



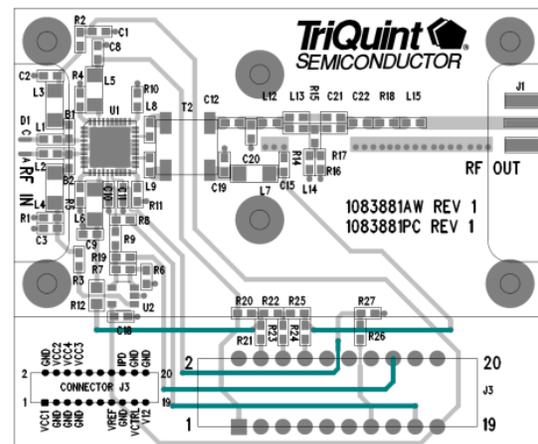
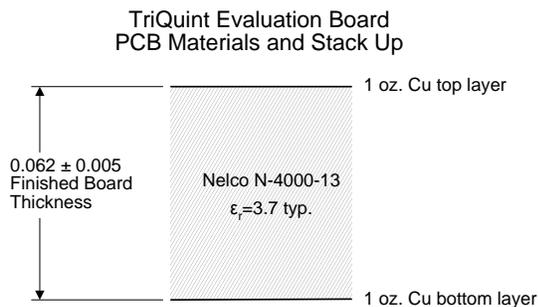
Pin Description



Pin	Symbol	Description
1-3, 5-6, 8-10, 12, 14, 17-19, 21-22, 24-27, 29-30, 32-37, 39	GND (Ground)	RF/DC Ground
4 / 7	RFIN1 / RFIN2	RF input 1 / RF input 2. Impedance matching required
11 / 40	V2ADJ / V1ADJ	Input amp 2 bias adjust / Input amp 1 bias adjust
13 / 38	VCC2 / VCC1	Amp 2 / Amp 1 DC supply. Bias choke and dropping resistor required.
15	VCTRL	Attenuation (Gain) control
16	VREF	Attenuator DC supply
20 / 31	V4ADJ / V3ADJ	Output amp 2 bias adjust / Output amp 1 bias adjust
23	RFOUT2	RF output / DC supply. Impedance matching, DC block and bias choke required.
28	RFOUT1	RF output / DC supply. Impedance matching, DC block and bias choke required.
Backside Paddle	GND (Ground)	RF/DC Ground. Use multiple PCB vias to minimize inductance and thermal resistance; see PCB mounting pattern in Mechanical Information section.

Applications Information

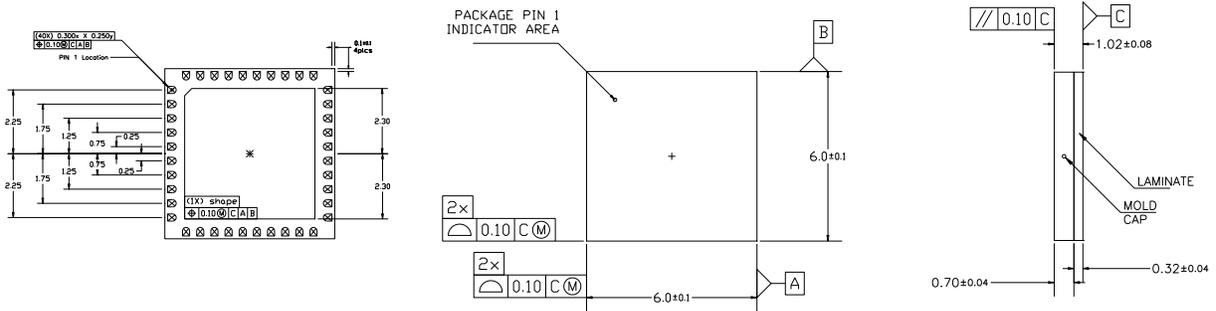
PC Board Layout



Mechanical Information

Package Information and Dimensions

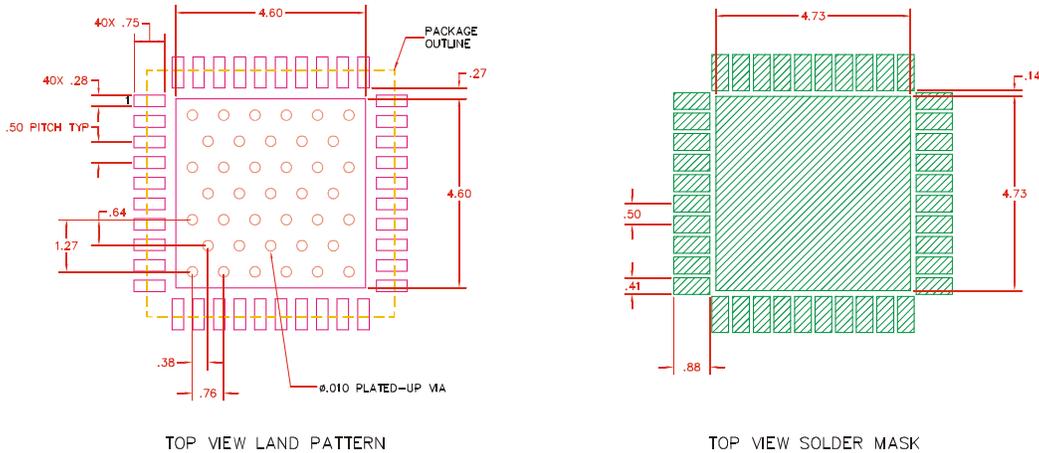
Marking: TriQuint Logo
 Product Number – TAT6281
 Year/Week/Country Code -YYWW CCCC
 Assembly Code - AaXXXX



All dimensions are in millimeters (inches). Angles are in degrees.

PCB Mounting Pattern

All dimensions are in millimeters (inches). Angles are in degrees.



- Notes:
1. Ground / thermal vias are critical for the proper performance of this device. Vias should use a .35mm (#80 / .0135") diameter drill and have a final plated thru diameter of .25 mm (.010").
 2. Use 1 oz. Copper minimum.

Product Compliance Information

ESD Information



Caution! ESD-Sensitive Device

ESD Rating: Class TBD
Value: Passes \geq TBD V to $<$ TBD V
Test: Human Body Model (HBM)
Standard: JEDEC Standard JESD22-A114

ESD Rating: Class TBD
Value: Passes \geq TBD V
Test: Charged Device Model (CDM)
Standard: JEDEC Standard JESD22-C101

MSL Rating

Moisture Sensitivity Level 3 at 260°C per JEDEC standard IPC/JEDEC J-STD-020.

Solderability

Package lead plating: NiPdAu

Compatible with both lead-free (260°C max. reflow temperature) and tin/lead (245°C max. reflow temperature) soldering processes.

RoHS Compliance

This part is compliant with EU 2002/95/EC RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).

This product also has the following attributes:

- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A (C₁₅H₁₂Br₄O₂) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations, and information about TriQuint:

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