Holtek 32-bit Microcontroller with ARM® Cortex™-M3 Core

HT32F1755/HT32F1765/HT32F2755
Datasheet

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1 General Description

The Holtek HT32F1755/1765/2755 devices are high performance and low power consumption 32-bit microcontrollers based around an ARM® Cortex™-M3 processor core. The Cortex™-M3 is a next-generation processor core which is tightly coupled with Nested Vectored Interrupt Controller (NVIC), SysTick timer, and including advanced debug support.

The HT32F1755/1765/2755 devices operate at a frequency of up to 72MHz with a Flash accelerator to obtain maximum efficiency. It provides 128KB of embedded Flash memory for code/data storage and up to 64KB of embedded SRAM memory for system operation and application program usage. A variety of peripherals, such as ADC, I²C, USART, SPI, PDMA, GPTM, MCTM, SCI, CSIF, USB2.0 FS, SWJ-DP (Serial Wire and JTAG Debug Port), etc., are also implemented in the device series. Several power saving modes provide the flexibility for maximum optimisation between wakeup latency and power consumption, an especially important consideration in low power applications.

The above features ensure that the HT32F1755/1765/2755 devices are suitable for use in a wide range of applications, especially in areas such as white goods application control, power monitors, alarm systems, consumer products, handheld equipment, data logging applications, motor control, fingerprint recognition and so on.

2 Features

Core

- 32-bit ARM® Cortex™-M3 processor core
- Up to 72MHz operation frequency
- 1.25 DMIPS/MHz (Dhrystone 2.1)
- Single-cycle multiplication and hardware division
- Integrated Nested Vectored Interrupt Controller (NVIC)
- 24-bit SysTick timer

The Cortex™-M3 processor is a general-purpose 32-bit processor core especially suitable for products requiring high performance and low power consumption microcontrollers. It offers many new features such as a Thumb-2 instruction set, hardware divider, low latency interrupt respond time, atomic bit-banding access and multiple buses for simultaneous accesses. The Cortex™-M3 processor is based on the ARMv7 architecture and supports both Thumb and Thumb-2 instruction sets.

On-chip Memory

- 128KB on-chip Flash memory for instruction/data and options storage
- up to 64KB on-chip SRAM
- Supports multiple boot modes

The ARM® Cortex™-M3 processor is structured using a Harvard architecture which uses separate busses to fetch instructions and load/store data. The instruction code and data are both located in the same memory address space but in different address ranges. The maximum address range of the Cortex™-M3 is 4GB due to its 32-bit bus address width. Additionally, a pre-defined memory map is provided by the Cortex™-M3 processor to reduce the software complexity of repeated implementation for different device vendors. However, some regions are used by the ARM® Cortex™-M3 system peripherals. Refer to the ARM® Cortex™-M3 Technical Reference Manual for more information. The Figure 2. shows the memory map of the HT32F1755/1765/2755 series of devices, including Code, SRAM, peripheral, and other pre-defined regions.

Flash Memory Controller

- Flash accelerator for maximum efficiency
- 32-bit word programming with In System Programming Interface (ISP) and In Application Programming (IAP)
- Flash protection capability to prevent illegal access

The Flash Memory Controller, FMC, provides all the necessary functions and pre-fetch buffer for the embedded on-chip Flash Memory. Since the access speed of the Flash Memory is slower than the CPU, a wide access interface with a pre-fetch buffer is provided for the Flash Memory in order to reduce the CPU waiting time which will cause CPU instruction execution delays. Flash Memory word program/page erase functions are also provided.

Reset Control Unit

- Supply supervisor:
  - Power-on Reset – POR
  - Brown-out Detector – BOD
  - Programmable Low Voltage Detector – LVD

The Reset Control Unit (RSTCU) has three kinds of reset, the power on reset, system reset and an APB unit reset. The power on reset, known as a cold reset, resets the full system during power up. A system reset resets the processor core and peripheral IP components with the exception of the SWJ-DP controller. The resets can be triggered by an external signal, internal events and the reset generators.

Clock Control Unit

- External 4 to 16MHz crystal oscillator
- External 32,768Hz crystal oscillator
- Internal 8MHz RC oscillator trimmed to ±2% accuracy at 3.3V operating voltage and 25°C operating temperature
- Internal 32kHz RC oscillator
- Integrated system clock PLL
- Independent clock gating bits for peripheral clock sources

The Clock Control unit, CKCU, provides a range of oscillator and clock functions. These include a High Speed Internal RC oscillator (HSI), a High Speed External crystal oscillator (HSE), a Low Speed Internal RC oscillator (LSI), a Low Speed External crystal oscillator (LSE), a Phase Lock Loop (PLL), a HSE clock monitor, clock prescalers, clock multiplexers and clock gating circuitry. The clocks of the AHB, APB and Cortex™-M3 are derived from the system clock (CK_SYS) which can come from the HSI, HSE or PLL. The Watchdog Timer and Real Time Clock (RTC) use either the LSI or LSE as their clock source. The maximum operating frequency of the system core clock (CK_AHB) can be up to 72MHz.

Power Management

- Single 3.3V power supply: 2.7V to 3.6V
- Integrated 1.8V LDO regulator for core and peripheral power supply
- V_{BAT} battery power supply for RTC and backup registers
- Three power domains: 3.3V, 1.8V and Backup
- Four power saving modes: Sleep, Deep-Sleep1, Deep-Sleep2, Power-Down

The Power consumption can be regarded as one of the most important issues for many embedded system applications. Accordingly the Power Control Unit, PWRCU, in these devices provides many types of power saving modes such as Sleep, Deep-Sleep1, Deep-Sleep2 and Power-Down mode. These operating modes reduce the power consumption and allow the application to achieve the best trade-off between the conflicting demands of CPU operating time, speed and power consumption.

Analog to Digital Converter

- 12-bit SAR ADC engine
- Up to 1Msps conversion rate – 1μs at 56MHz, 1.17μs at 72MHz
- 8 external analog input channels
- Supply voltage range: 2.7V ~ 3.6V
- Conversion range: V_{REF+} ~ V_{REF-}

A 12-bit multi-channel ADC is integrated in the device. There are a total of 10 multiplexed channels, which include 8 external channels on which the external analog signals can be measured, and 2 internal channels. If the input voltage is required to remain within a specific threshold window, an Analog Watchdog function will monitor and detect these signals. An interrupt will then be generated to inform the device that the input voltage is not within the preset threshold levels. There are three conversion modes to convert an analog signal to digital data. The ADC can be operated in one shot, continuous and discontinuous conversion modes.

Analog Operational Amplifier/Comparator

- Two Operational Amplifiers or Comparator functions which are software configurable
- Supply voltage range: 2.7V ~ 3.6V

Two Operational Amplifiers/Comparators (OPA/CMP) are implemented within the devices. They can be configured either as Operational Amplifiers or as Analog Comparators. When configured as comparators, they are capable of generating interrupts to the NVIC.

I/O Ports

- Up to 80 GPIOs
- Port A, B, C, D, E are mapped as 16 external interrupts – EXTI
- Almost all I/O pins are 5V-tolerant except for pins shared with analog inputs

There are up to 80 General Purpose I/O pins, (GPIO), named PA0 ~ PA15 to PE0 ~ PE15 for the implementation of logic input/output functions. Each of the GPIO ports has a series of related control and configuration registers to maximise flexibility and to meet the requirements of a wide range of applications.

The GPIO ports are pin-shared with other alternative functions to obtain maximum functional flexibility on the package pins. The GPIO pins can be used as alternative functional pins by configuring the corresponding registers regardless of the input or output pins.

The external interrupts on the GPIO pins of the device have related control and configuration registers in the External Interrupt Control Unit, EXTI.

PWM Generation and Capture Timers – GPTM

- Two 16-bit General-Purpose Timers – GPTM
- Up to 4-channel PWM Compare Output or Input Capture function for each GPTM
- External trigger input

The General-Purpose Timers, known as GPTM0 and GPTM1, consist of one 16-bit up/down-counter, four 16-bit Capture/Compare Registers (CCRs), one 16-bit Counter-Reload Register (CRR) and several control/status registers. They can be used for a variety of purposes including general time measurement, input signal pulse width measurement, output waveform generation such as single pulse generation, or PWM output generation. The GPTM supports an Encoder Interface using a decoder with two inputs.

Motor Control Timer – MCTM

- Single 16-bit up, down, up/down auto-reload counter
- 16-bit programmable prescaler allowing dividing the counter clock frequency by any factor between 1 and 65536
- Input Capture function
- Compare Match Output
- PWM waveform generation with Edge and Centre-aligned Modes
- Single Pulse Mode Output
- Complementary Outputs with programmable dead-time insertion
- Encoder interface controller with two inputs using quadrature decoder
- Support 3-phase motor control and hall sensor interface
- Brake input to force the timer's output signals into a reset or fixed condition

The Motor Control Timer consists of a single 16-bit up/down counter, four 16-bit CCRs (Capture/Compare Registers), single one 16-bit counter-reload register (CRR), single 8-bit repetition counter and several control/status registers. It can be used for a variety of purposes including measuring the pulse widths of input signals or generating output waveforms such as compare match outputs, PWM outputs or complementary PWM outputs with dead-time insertion. The MCTM supports an Encoder interface controller to an incremental encoder with two inputs. The MCTM is capable of offering full functional support for motor control, hall sensor interfacing and brake input.

Basic Function Timer – BFTM

- Two 32-bit compare/match count-up counters – no I/O control features
- One shot mode – counting stops after a match condition
- Repetitive mode – restart counter after a match condition

The Basic Function Timer is a simple count-up 32-bit counter designed to measure time intervals and generate a one shot or repetitive interrupts. The BFTM operates in two functional modes, repetitive or one shot mode. In the repetitive mode the BFTM restarts the counter when a compare match event occurs. The BFTM also supports a one shot mode which forces the counter to stop counting when a compare match event occurs.

Watchdog Timer

- 12-bit down counter with 3-bit prescaler
- Interrupt or reset event for the system
- Programmable watchdog timer window function
- Registers write protection function

The Watchdog Timer is a hardware timing circuit that can be used to detect system failures due to software malfunctions. It includes a 12-bit count-down counter, a prescaler, a WDT counter value register, a WDT delta value register, interrupt related circuits, WDT operation control circuitry and a WDT protection mechanism. The Watchdog Timer can be operated in an interrupt mode or a reset mode. The Watchdog Timer will generate an interrupt or a reset when the counter counts down and reaches a zero value. If the software does not reload the counter value before a Watchdog Timer underflow occurs, an interrupt or a reset will be generated when the counter underflows. In addition, an interrupt or reset is also generated if the software reloads the counter when the counter value is greater than or equal to the WDT delta value. This means the counter must be reloaded within a limited timing window using a specific method. The Watchdog Timer counter can be stopped while the processor is in the debug mode. There is a register write protect function which can be enabled to prevent it from changing the Watchdog Timer configuration unexpectedly.

Real Time Clock

- 32-bit up-counter with a programmable prescaler
- Alarm function
- Interrupt and Wake-up event

The Real Time Clock, RTC, circuitry includes the APB interface, a 32-bit count-up counter, a control register, a prescaler, a compare register and a status register. Most of the RTC circuits are located in the Backup Domain except for the APB interface. The APB interface is located in the V_{DD18} power domain. Therefore, it is necessary to be isolated from the ISO signal that comes from the power control unit when the V_{DD18} power domain is powered off, that is when the device enters the Power-Down mode. The RTC counter is used as a wakeup timer to generate a system resume signal from the Power-Down mode.

Inter-integrated Circuit – I²C

- Support both master and slave mode with a frequency of up to 1MHz
- Provide an arbitration function and clock synchronization
- Supports 7-bit and 10-bit addressing mode and general call addressing
- Supports slave multi-addressing mode with maskable address

The I²C Module is an internal circuit allowing communication with an external I²C interface which is an industry standard two line serial interface used for connection to external hardware. These two serial lines are known as a serial data line, SDA, and a serial clock line, SCL. The I²C module provides three data transfer rates: (1). 100kHz in the Standard mode, (2). 400kHz in the Fast mode and, (3). 1MHz in the Fast mode plus. The SCL period generation register is used to setup different kinds of duty cycle implementation for the SCL pulse.

The SDA line which is connected directly to the I²C bus is a bi-directional data line between the master and slave devices and is used for data transmission and reception. The I²C module also has an arbitration detect function and clock synchronization to prevent situations where more than one master attempts to transmit data to the I²C bus at the same time.

Serial Peripheral Interface – SPI

- Supports both master and slave mode
- Frequency of up to 36MHz for master mode and 18MHz for slave mode
- FIFO Depth: 8 levels
- Multi-master and multi-slave operation

The Serial Peripheral Interface, SPI, provides an SPI protocol data transmit and receive function in both master and slave mode. The SPI interface uses 4 pins, which are the serial data input and output lines MISO and MOSI, the clock line, SCK, and the slave select line, SEL. One SPI device acts as a master device which controls the data flow using the SEL and SCK signals to indicate the start of data communication and the data sampling rate. To receive a data byte, the streamed data bits are latched on a specific clock edge and stored in the data register or in the RX FIFO. Data transmission is carried in a similar way but with a reverse sequence. The mode fault detection provides a capability for multi-master applications.

Universal Synchronous Asynchronous Receiver Transmitter – USART

- Operating frequency up to 4.5MHz
- Supports both asynchronous and clocked synchronous serial communication modes
- IrDA SIR encoder and decoder
- RS485 mode with output enable control
- Full Modem function for USART0
- Auto hardware flow control mode – RTS, CTS
- FIFO Depth: 16×9 bits for both receiver and transmitter

The Universal Synchronous Asynchronous Receiver Transceiver, USART, provides a flexible full duplex data exchange using synchronous or asynchronous transfer. The USART is used to translate data between parallel and serial interfaces, and is also commonly used for RS232 standard communication. The USART peripheral function supports five types of interrupt including Line Status Interrupt, Transmitter FIFO Empty Interrupt, Receiver Threshold Level Reaching Interrupt, Time Out Interrupt and MODEM Status Interrupt. The USART module includes a 16-byte transmitter FIFO (TX_FIFO) and a 16-byte receiver FIFO (RX_FIFO). The software can detect a USART error status by reading the Line Status Register, LSR. The status includes the type and the condition of transfer operations as well as several error conditions resulting from Parity, Overrun, Framing and Break events.

The USART includes a programmable baud rate generator which is capable of dividing the CK_AHB to produce a clock for the USART transmitter and receiver.

Smart Card Interface – SCI

- Support ISO 7816-3 standard
- Character mode
- Single transmit buffer and single receive buffer
- 11-bit ETU (Elementary Time Unit) counter
- 9-bit guard time counter
- 24-bit general purpose waiting time counter
- Parity generation and checking
- Automatic character retry on parity error detection in transmission and reception modes

The Smart Card Interface is compatible with the ISO 7816-3 standard. This interface includes Card Insertion/Removal detection, SCI data transfer control logic and data buffers, internal Timer Counters and corresponding control logic circuits to perform all the necessary Smart Card operations. The Smart Card interface acts as a Smart Card Reader to facilitate communication with the external Smart Card. The overall functions of the Smart Card interface are controlled by a series of registers including control and status registers together with several corresponding interrupts which are generated to get the attention of the microcontroller for SCI transfer status.

Peripheral Direct Memory Access – PDMA

- 12 channels with trigger source grouping
- Supports Single and block transfer mode
- 8/16/32-bit width data transfer
- Supports Address increment, decrement or fixed mode
- 4-level programmable channel priority
- Auto reload mode
- Supports trigger source: CSIF, ADC, SPI, USART, I²C, GPTM, MCTM, SCI and software

The Peripheral Direct Memory Access controller, PDMA, moves data between the peripherals (USART, SPI, ADC, GPTM, MCTM, CSIF, I²C and SCI, CPU for software mode) and the system memory on the AHB bus. Each PDMA channel has a source address, destination address, block length and transfer count. The PDMA can exclude the CPU intervention and avoid interrupt service routine execution. It improves system performance as the software does not need to join each data movement operation.

Universal Serial Bus Device Controller – USB

- Complies with USB 2.0 full-speed (12Mbps) specification
- On-chip USB full-speed transceiver
- 1 control endpoint (EP0) for control transfer
- 3 single-buffered endpoints for bulk and interrupt transfer
- 4 double-buffered endpoints for bulk, interrupt and isochronous transfer
- 1024 bytes EP-SRAM used as the endpoint data buffers

The USB device controller is compliant with USB 2.0 full-speed specification. There is one control endpoint known as Endpoint 0 and seven configurable endpoints. A 1024-byte SRAM is used as the endpoint buffers. Each endpoint buffer size is programmable using corresponding registers, which provides maximum flexibility for various applications. The integrated USB full-speed transceiver helps to minimise the overall system complexity and cost. The USB functional block also contains the resume and suspend features to meet the requirements of low-power consumption.

CMOS Sensor Interface – CSIF (HT32F2755 only)

- Up to 2048×2048 input resolution
- Supports 8-bit YUV422 and Raw RGB formats
- Up to 24MHz input pixel clock frequency
- Multi VSYNC and HSYNC settings for image capture
- Hardware window capture function
- Fractional hardware sub-sample function
- Dual FIFOs each with a capacity of 8×32 bits which can be read by the PDMA or CPU

The CMOS Sensor Interface, otherwise known as the CSIF, provides an interface for image capture from CMOS sensors. The device can be connected to the CMOS sensor directly using its CMOS Sensor Interface. The CSIF supports both Vertical SYNC and Horizontal SYNC modes for image capture implementation. The CSIF consists of window capture and sub-sampling functions together with dual FIFOs, each with a capacity of 8×32 bits, to store data which can be moved to the internal SRAM via the Peripheral Direct Memory Access circuitry, PDMA. The CSIF does not support image data conversion or decode but rather transfers the image data received from the CMOS sensor to the internal SRAM transparently.

Debug Support

- Serial Wire or JTAG Debug Port SWJ-DP
- 6 instruction comparators and 2 literal comparators for hardware breakpoint or code/literal patch
- 4 comparators for hardware watchpoints
- 1-bit asynchronous trace – TRACESWO

Package and Operation Temperature

- 48/64/100-pin LQFP packages
- Operation temperature range: -40°C to +85°C

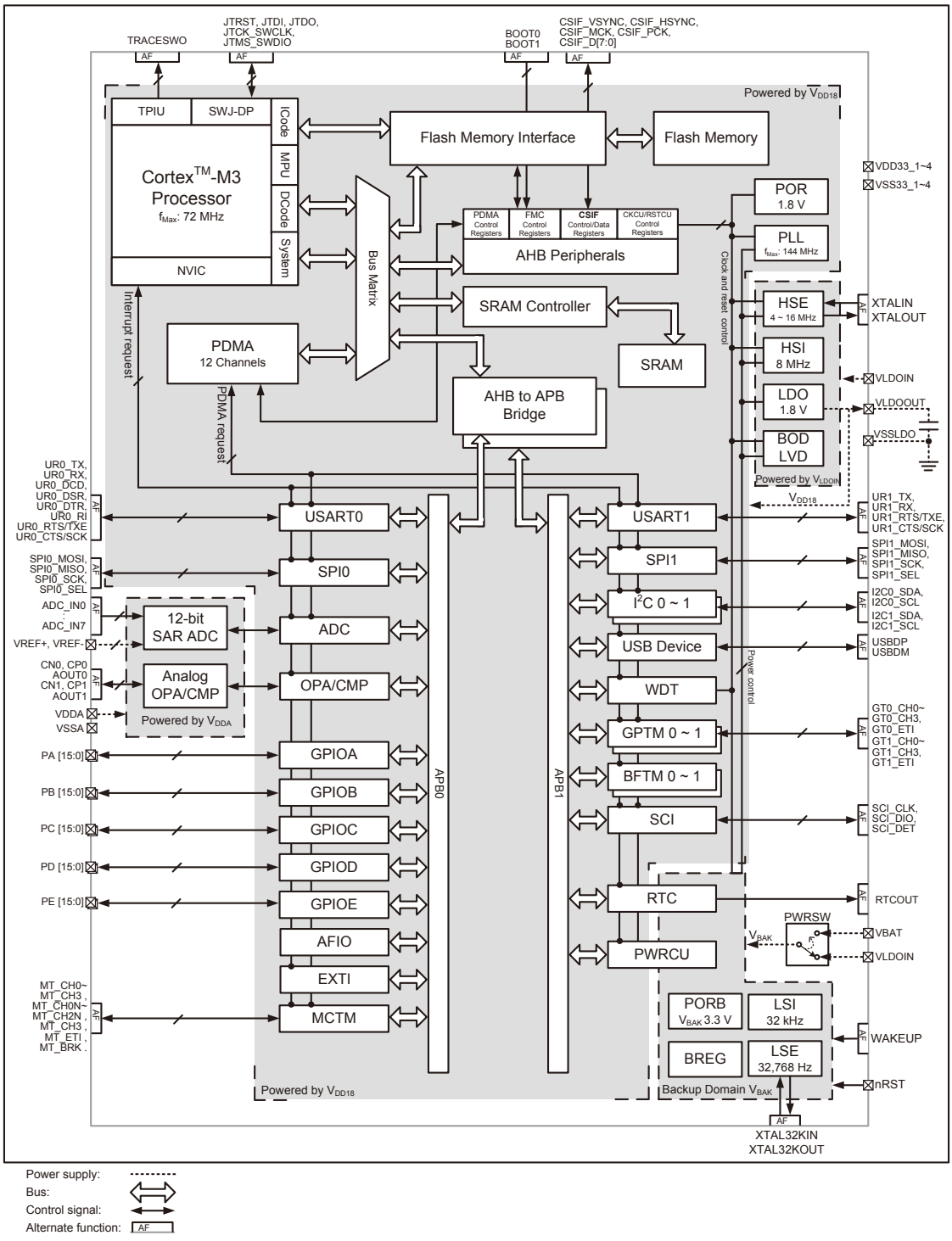
3 Overview

Device Information

Table 1. HT32F1755/1765/2755 Series Features and Peripheral List

Peripherals		HT32F1755	HT32F1765	HT32F2755
Main Flash (KB)		127	127	127
Option Bytes Flash (KB)		1	1	1
SRAM (KB)		32	64	64
Timers	MCTM	1		
	GPTM	2		
	BFTM	2		
	RTC	1		
	WDT	1		
Communication	CSIF	—	—	1
	USB	1		
	SCI	1		
	USART	2		
	SPI	2		
	I^2C	2		
GPIO		Up to 80		
EXTI		16		
12-bit ADC Number of channels		1 8 Channels		
OPA/Comparator		2		
CPU frequency		Up to 72MHz		
Operating voltage		2.7V ~ 3.6V		
Operating temperature		-40°C ~ +85°C		
Package		48/64/100-pin LQFP		

Block Diagram



NOTE: The AHB peripheral function, CSIF, is only available in the HT32F2755 device.

Figure 1. HT32F1755/1765/2755 Block Diagram

Memory Map

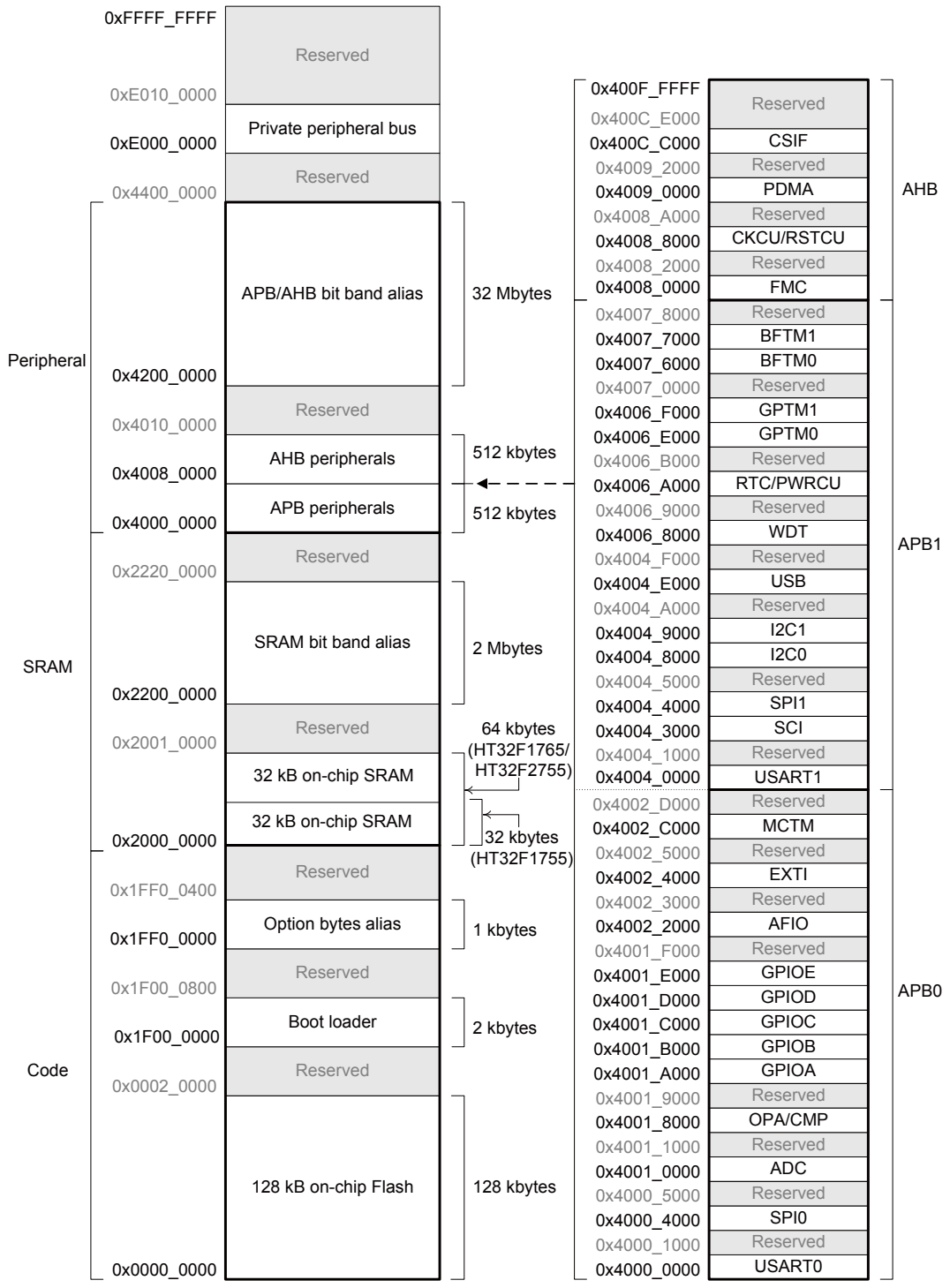


Figure 2. HT32F1755/1765/2755 Memory Map

Clock Structure

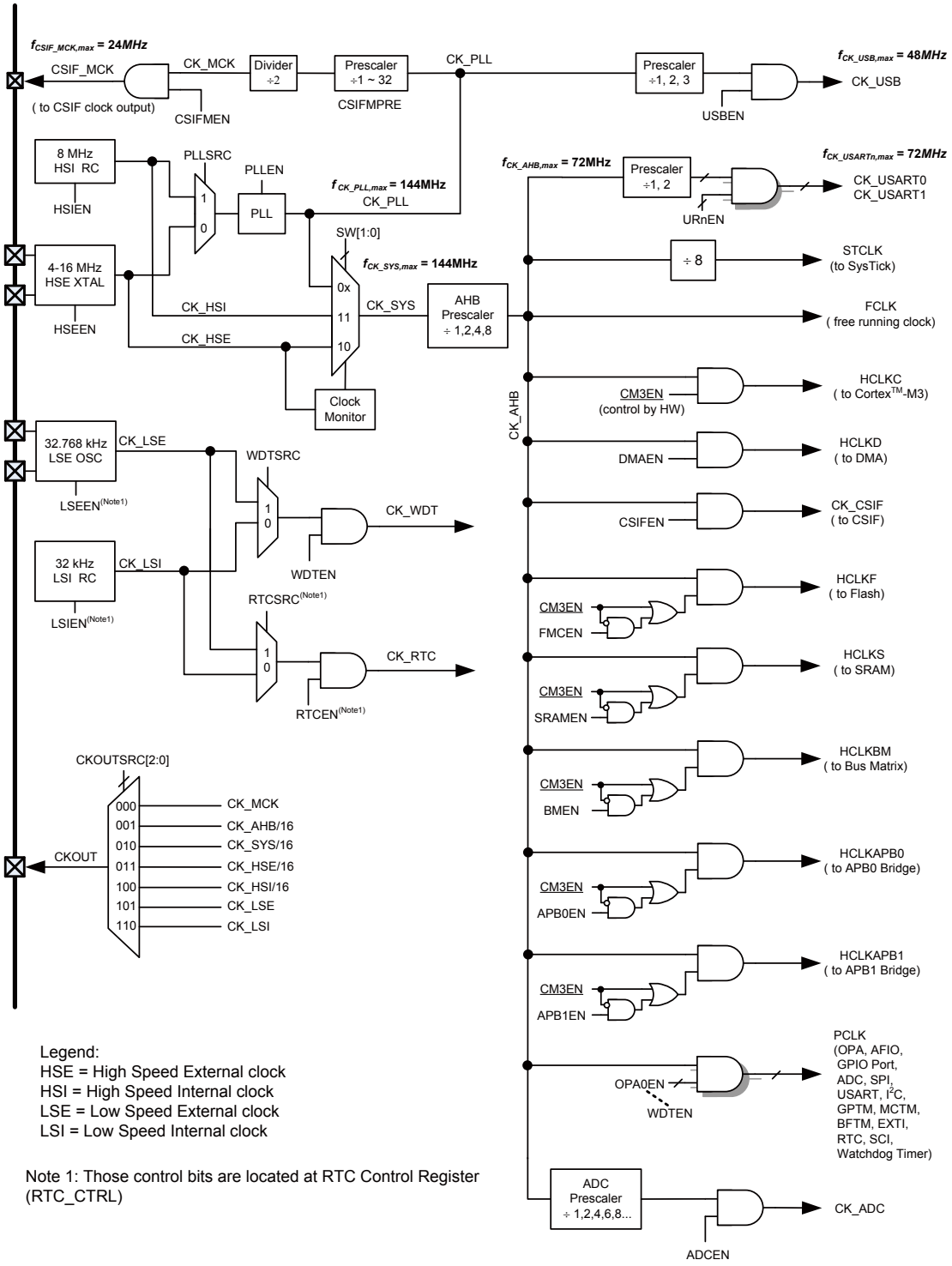


Figure 3. HT32F1755/1765/2755 Clock Structure

Pin Assignment

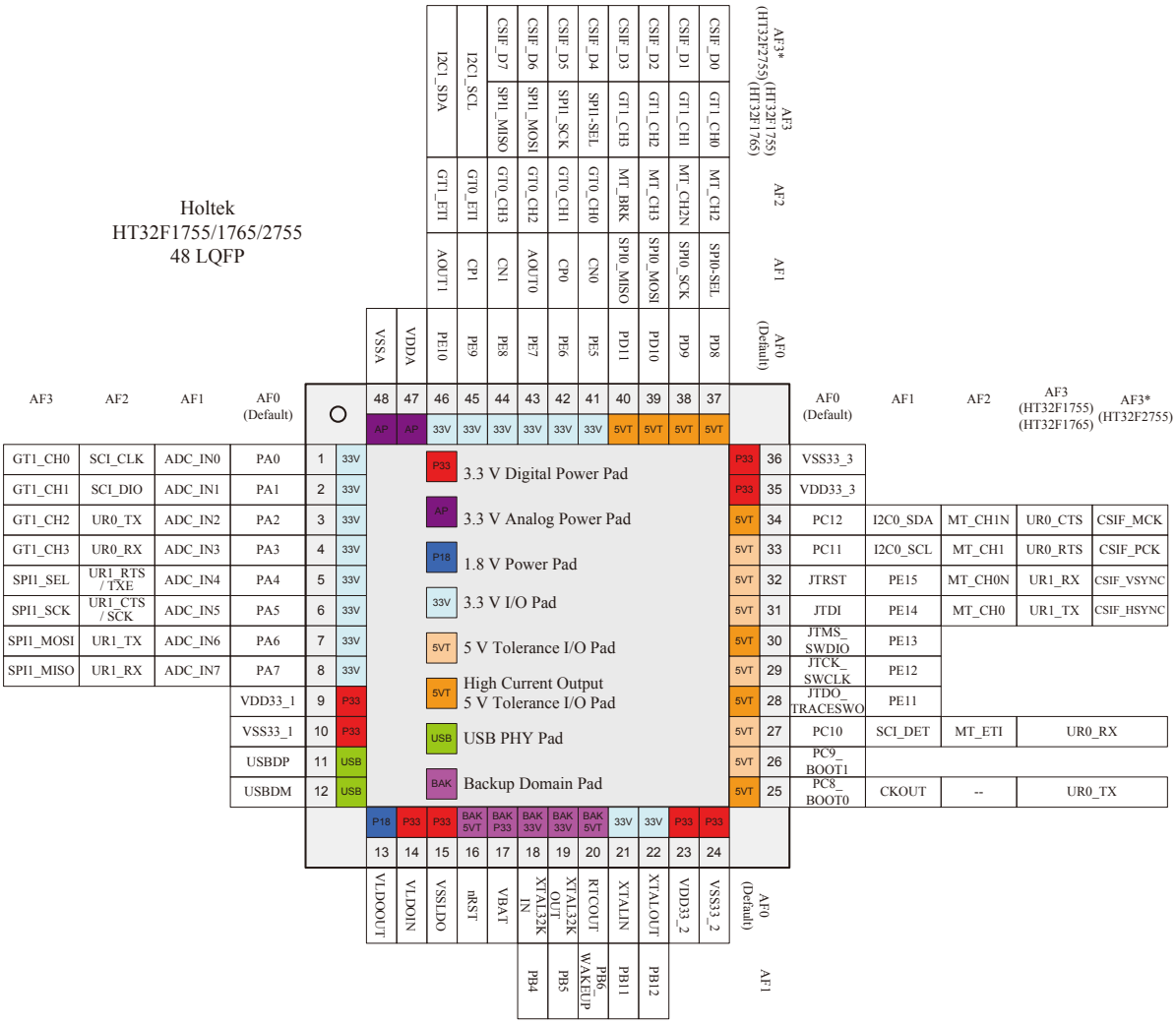


Figure 4. HT32F1755/1765/2755 48-LQFP Pin Assignment

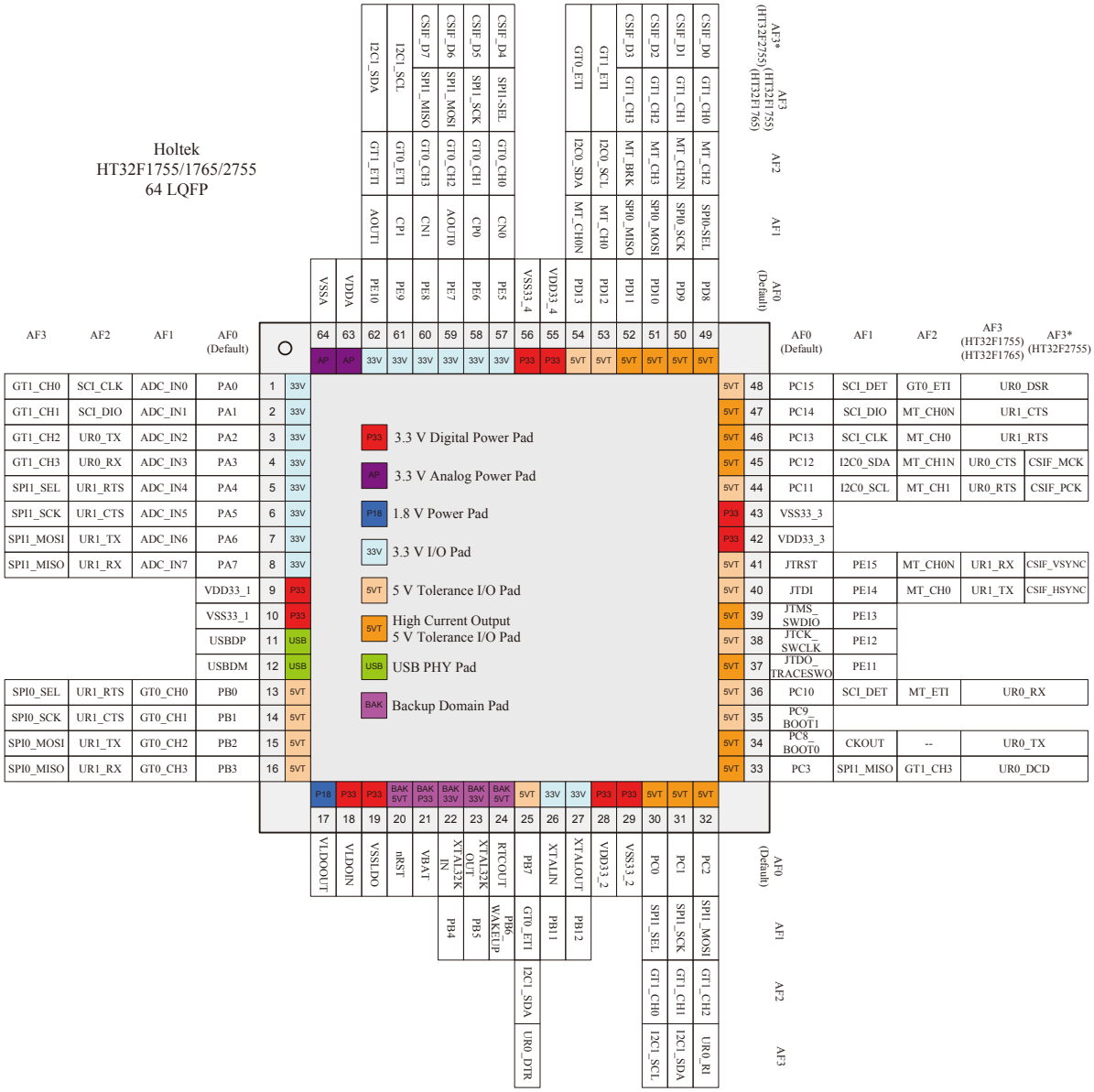


Figure 5. HT32F1755/1765/2755 64-LQFP Pin Assignment

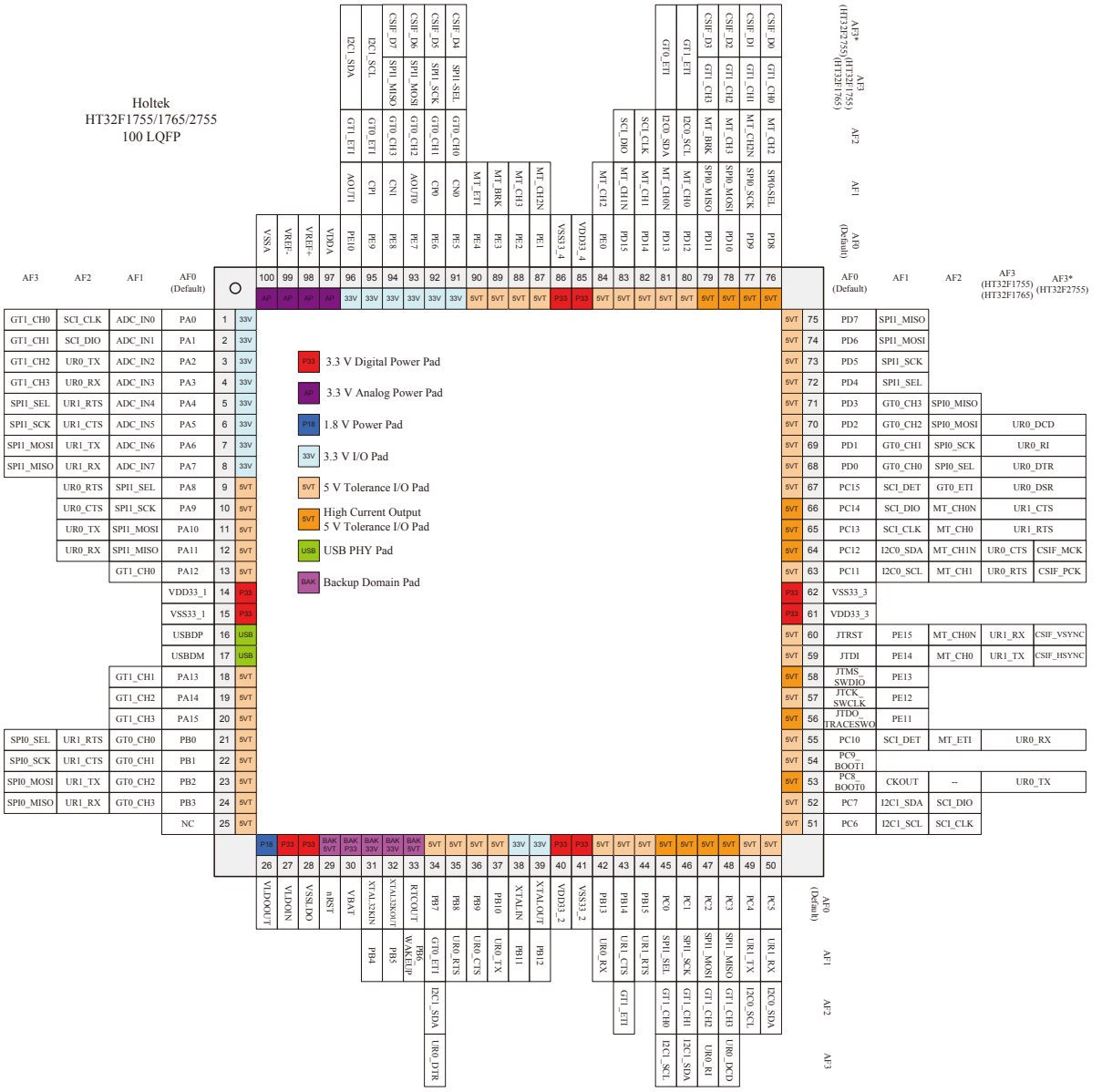


Figure 6. HT32F1755/1765/2755 100-LQFP Pin Assignment

Table 2. HT32F1755/1765/2755 Pin Descriptions

Pin Name	Pins			Type (Note1)	IO Level (Note2)	Description				
	48 LQFP	64 LQFP	100 LQFP			Main function (AF0)	AF1	AF2	AF3 (HT32F1755) (HT32F1765)	AF3 (HT32F2755)
PA0	1	1	1	AI/O	—	PA0	ADC_IN0	SCI_CLK	GT1_CH0	GT1_CH0
PA1	2	2	2	AI/O	—	PA1	ADC_IN1	SCI_DIO	GT1_CH1	GT1_CH1
PA2	3	3	3	AI/O	—	PA2	ADC_IN2	UR0_TX	GT1_CH2	GT1_CH2
PA3	4	4	4	AI/O	—	PA3	ADC_IN3	UR0_RX	GT1_CH3	GT1_CH3
PA4	5	5	5	AI/O	—	PA4	ADC_IN4	UR1_RTS /TXE	SPI1_SEL	SPI1_SEL
PA5	6	6	6	AI/O	—	PA5	ADC_IN5	UR1_CTS /SCK	SPI1_SCK	SPI1_SCK
PA6	7	7	7	AI/O	—	PA6	ADC_IN6	UR1_TX	SPI1_MOSI	SPI1_MOSI
PA7	8	8	8	AI/O	—	PA7	ADC_IN7	UR1_RX	SPI1_MISO	SPI1_MISO
PA8	—	—	9	I/O	5V-T	PA8	SPI1_SEL	UR0_RTS /TXE	—	—
PA9	—	—	10	I/O	5V-T	PA9	SPI1_SCK	UR0_CTS /SCK	—	—
PA10	—	—	11	I/O	5V-T	PA10	SPI1_MOSI	UR0_TX	—	—
PA11	—	—	12	I/O	5V-T	PA11	SPI1_MISO	UR0_RX	—	—
PA12	—	—	13	I/O	5V-T	PA12	GT1_CH0	—	—	—
VDD33_1	9	9	14	P	—	3.3V voltage for digital I/O				
VSS33_1	10	10	15	P	—	Ground reference for digital I/O				
USBDP	11	11	16	AI/O	—	USB Differential data bus conforming to the Universal Serial Bus standard				
USBDM	12	12	17	AI/O	—	USB Differential data bus conforming to the Universal Serial Bus standard				
PA13	—	—	18	I/O	5V-T	PA13	GT1_CH1	—	—	—
PA14	—	—	19	I/O	5V-T	PA14	GT1_CH2	—	—	—
PA15	—	—	20	I/O	5V-T	PA15	GT1_CH3	—	—	—
PB0	—	13	21	I/O	5V-T	PB0	GT0_CH0	UR1_RTS /TXE	SPI0_SEL	SPI0_SEL
PB1	—	14	22	I/O	5V-T	PB1	GT0_CH1	UR1_CTS /SCK	SPI0_SCK	SPI0_SCK
PB2	—	15	23	I/O	5V-T	PB2	GT0_CH2	UR1_TX	SPI0_MOSI	SPI0_MOSI
PB3	—	16	24	I/O	5V-T	PB3	GT0_CH3	UR1_RX	SPI0_MISO	SPI0_MISO
NC	—	—	25	—	—	No connection				
VLDOOUT	13	17	26	P	—	LDO 1.8V output It is recommended to connect a capacitor, denoted as C_{LDO}, as close as possible between this pin and VSSLDO				
VLDOIN	14	18	27	P	—	LDO 3.3V power input Connected to the power switch circuitry for the internal backup domain				
VSSLDO	15	19	28	P	—	LDO ground reference				
nRST	16	20	29	I (BK)	5V-T_PU	External reset pin and external wakeup pin in Power-Down mode				
VBAT	17	21	30	P	—	VDD 3.3V for backup domain				

Pin Name	Pins			Type (Note1)	IO Level (Note2)	Description				
	48 LQFP	64 LQFP	100 LQFP			Main function (AF0)	AF1	AF2	AF3 (HT32F1755) (HT32F1765)	AF3 (HT32F2755)
XTAL-32KIN	18	22	31	AI/O (BK)	—	XTAL32KIN	PB4	—	—	—
XTAL-32KOUT	19	23	32	AI/O (BK)	—	XTAL32KOUT	PB5	—	—	—
RTCOUT	20	24	33	I/O (BK)	5V-T	RTCOUT	PB6_WAKEUP	—	—	—
PB7	—	25	34	I/O	5V-T	PB7	GT0_ETI	I2C1_SDA	UR0_DTR	UR0_DTR
PB8	—	—	35	I/O	5V-T	PB8	UR0_RTS/TXE	—	—	—
PB9	—	—	36	I/O	5V-T	PB9	UR0_CTS/SCK	—	—	—
PB10	—	—	37	I/O	5V-T	PB10	UR0_TX	—	—	—
XTALIN	21	26	38	AI/O	—	XTALIN	PB11	—	—	—
XTALOUT	22	27	39	AI/O	—	XTALOUT	PB12	—	—	—
VDD33_2	23	28	40	P	—	3.3V voltage for digital I/O				
VSS33_2	24	29	41	P	—	Ground reference for digital I/O				
PB13	—	—	42	I/O	5V-T	PB13	UR0_RX	—	—	—
PB14	—	—	43	I/O	5V-T	PB14	UR1_CTS/SCK	GT1_ETI	—	—
PB15	—	—	44	I/O	5V-T	PB15	UR1_RTS/TXE	—	—	—
PC0	—	30	45	I/O	5V-T	PC0	SPI1_SEL	GT1_CH0	I2C1_SCL	I2C1_SCL
PC1	—	31	46	I/O	5V-T	PC1	SPI1_SCK	GT1_CH1	I2C1_SDA	I2C1_SDA
PC2	—	32	47	I/O	5V-T	PC2	SPI1_MOSI	GT1_CH2	UR0_RI	UR0_RI
PC3	—	33	48	I/O	5V-T	PC3	SPI1_MISO	GT1_CH3	UR0_DCD	UR0_DCD
PC4	—	—	49	I/O	5V-T	PC4	UR1_TX	I2C0_SCL	—	—
PC5	—	—	50	I/O	5V-T	PC5	UR1_RX	I2C0_SDA	—	—
PC6	—	—	51	I/O	5V-T	PC6	I2C1_SCL	SCI_CLK	—	—
PC7	—	—	52	I/O	5V-T	PC7	I2C1_SDA	SCI_DIO	—	—
PC8	25	34	53	I/O	5V-T_PU	PC8_BOOT0	CKOUT	—	UR0_TX	UR0_TX
PC9	26	35	54	I/O	5V-T_PU	PC9_BOOT1	—	—	—	—
PC10	27	36	55	I/O	5V-T	PC10	SCI_DET	MT_ETI	UR0_RX	UR0_RX
PE11	28	37	56	I/O	5V-T	JTDO_TRACESWO	PE11	—	—	—

Pin Name	Pins			Type (Note1)	IO Level (Note2)	Description				
	48 LQFP	64 LQFP	100 LQFP			Main function (AF0)	AF1	AF2	AF3 (HT32F1755) (HT32F1765)	AF3 (HT32F2755)
PE12	29	38	57	I/O	5V-T_PU	JTCK_SWCLK	PE12	—	—	—
PE13	30	39	58	I/O	5V-T_PU	JTMS/SWDIO	PE13	—	—	—
PE14	31	40	59	I/O	5V-T_PU	JTDI	PE14	MT_CH0	UR1_TX	CSIF_HSYNC
PE15	32	41	60	I/O	5V-T_PU	JTRST	PE15	MT_CH0N	UR1_RX	CSIF_VSYNC
VDD33_3	—	42	61	P	—	3.3V voltage for digital I/O				
VSS33_3	—	43	62	P	—	Ground reference for digital I/O				
PC11	33	44	63	I/O	5V-T	PC11	I2C0_SCL	MT_CH1	UR0_RTS/TXE	CSIF_PCK
PC12	34	45	64	I/O	5V-T	PC12	I2C0_SDA	MT_CH1N	UR0_CTS/SCK	CSIF_MCK
PC13	—	46	65	I/O	5V-T	PC13	SCI_CLK	MT_CH0	UR1_RTS/TXE	UR1_RTS/TXE
PC14	—	47	66	I/O	5V-T	PC14	SCI_DIO	MT_CH0N	UR1_CTS/SCK	UR1_CTS/SCK
PC15	—	48	67	I/O	5V-T	PC15	SCI_DET	GT0_ETI	UR0_DSR	UR0_DSR
PD0	—	—	68	I/O	5V-T	PD0	GT0_CH0	SPI0_SEL	UR0_DTR	UR0_DTR
PD1	—	—	69	I/O	5V-T	PD1	GT0_CH1	SPI0_SCK	UR0_RI	UR0_RI
PD2	—	—	70	I/O	5V-T	PD2	GT0_CH2	SPI0_MOSI	UR0_DCD	UR0_DCD
PD3	—	—	71	I/O	5V-T	PD3	GT0_CH3	SPI0_MISO	—	—
PD4	—	—	72	I/O	5V-T	PD4	SPI1_SEL	—	—	—
PD5	—	—	73	I/O	5V-T	PD5	SPI1_SCK	—	—	—
PD6	—	—	74	I/O	5V-T	PD6	SPI1_MOSI	—	—	—
PD7	—	—	75	I/O	5V-T	PD7	SPI1_MISO	—	—	—
VDD33_3	35	—	—	P	—	3.3V voltage for digital I/O				
VSS33_3	36	—	—	P	—	Ground reference for digital I/O				
PD8	37	49	76	I/O	5V-T	PD8	SPI0_SEL	MT_CH2	GT1_CH0	CSIF_D0
PD9	38	50	77	I/O	5V-T	PD9	SPI0_SCK	MT_CH2N	GT1_CH1	CSIF_D1
PD10	39	51	78	I/O	5V-T	PD10	SPI0_MOSI	MT_CH3	GT1_CH2	CSIF_D2
PD11	40	52	79	I/O	5V-T	PD11	SPI0_MISO	MT_BRK	GT1_CH3	CSIF_D3
PD12	—	53	80	I/O	5V-T	PD12	MT_CH0	I2C0_SCL	GT1_ETI	GT1_ETI

Pin Name	Pins			Type (Note1)	IO Level (Note2)	Description				
	48 LQFP	64 LQFP	100 LQFP			Main function (AF0)	AF1	AF2	AF3 (HT32F1755) (HT32F1765)	AF3 (HT32F2755)
PD13	—	54	81	I/O	5V-T	PD13	MT_CH0N	I2C0_SDA	GT0_ETI	GT0_ETI
PD14	—	—	82	I/O	5V-T	PD14	MT_CH1	SCI_CLK	—	—
PD15	—	—	83	I/O	5V-T	PD15	MT_CH1N	SCI_DIO	—	—
PE0	—	—	84	I/O	5V-T	PE0	MT_CH2	—	—	—
VDD33_4	—	55	85	P	—	3.3V voltage for digital I/O				
VSS33_4	—	56	86	P	—	Ground reference for digital I/O				
PE1	—	—	87	I/O	5V-T	PE1	MT_CH2N	—	—	—
PE2	—	—	88	I/O	5V-T	PE2	MT_CH3	—	—	—
PE3	—	—	89	I/O	5V-T	PE3	MT_BRK	—	—	—
PE4	—	—	90	I/O	5V-T	PE4	MT_ETI	—	—	—
PE5	41	57	91	AI/O	—	PE5	CN0	GT0_CH0	SPI1_SEL	CSIF_D4
PE6	42	58	92	AI/O	—	PE6	CP0	GT0_CH1	SPI1_SCK	CSIF_D5
PE7	43	59	93	AI/O	—	PE7	AOUT0	GT0_CH2	SPI1_MOSI	CSIF_D6
PE8	44	60	94	AI/O	—	PE8	CN1	GT0_CH3	SPI1_MISO	CSIF_D7
PE9	45	61	95	AI/O	—	PE9	CP1	GT0_ETI	I2C1_SCL	I2C1_SCL
PE10	46	62	96	AI/O	—	PE10	AOUT1	GT1_ETI	I2C1_SDA	I2C1_SDA
VDDA	47	63	97	P	—	3.3V analog voltage for ADC and OPA/Comparator				
VREF+	—	—	98	P	—	ADC positive reference voltage has to be lower or equal to VDDA				
VREF-	—	—	99	P	—	ADC negative reference voltage has to be directly connected to VSSA				
VSSA	48	64	100	P	—	Ground reference for the ADC and OPA/Comparator				

NOTES: 1. I = input, O = output, A = Analog port, P = power supply, PU = pull-up, BK = Back-up domain.

2. 5V-T = 5V tolerant.

3. The GPIOs are in an AF0 state after a V_{DD18} power on reset (POR) except for the RTCOUT pin of in the Backup Domain I/O. The RTCOUT pin is reset by the Backup Domain power-on-reset (PORB) or by a Backup Domain software reset (BAK_RST bit in BAK_CR register).

4. The backup domain of I/O pins has drive current capability limitation of < 1mA @ V_{BAT} = 3.3V.

4 Electrical Characteristics

Absolute Maximum Ratings

The following table shows the absolute maximum ratings of the device. These are stress ratings only. Stresses beyond absolute maximum ratings may cause permanent damage to the device. Note that the device is not guaranteed to operate properly at the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Table 3. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
V_{DD33}	External main supply voltage	V_{SS} - 0.3	V_{SS} + 3.6	V
V_{DDA}	External analog supply voltage	V_{SSA} - 0.3	V_{SSA} + 3.6	V
V_{BAT}	External battery supply voltage	V_{SS} - 0.3	V_{SS} + 3.6	V
V_{LDOIN}	External LDO supply voltage	V_{SS} - 0.3	V_{SS} + 3.6	V
V_{IN}	Input voltage on 5V-tolerant I/O	V_{SS} - 0.3	V_{SS} + 5.5	V
	Input voltage on other I/O	V_{SS} - 0.3	V_{DD33} + 0.3	V
T_A	Ambient operating temperature range	-40	+85	°C
T_{STG}	Storage temperature range	-55	+150	°C
T_J	Maximum junction temperature	—	125	°C
P_D	Total power dissipation	—	500	mW
V_{ESD}	Electrostatic discharge voltage (human body mode)	-4000	+4000	V

Recommended DC Characteristics

Table 4. Recommended DC Operating Conditions

T_A = 25°C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD33}	I/O Operating voltage	—	2.7	3.3	3.6	V
V_{DDA}	Analog operating voltage	—	2.7	3.3	3.6	V
V_{BAT}	Battery supply operating voltage	—	2.7	3.3	3.6	V
V_{LDOIN}	LDO operating voltage	—	2.7	3.3	3.6	V

On-Chip LDO Voltage Regulator Characteristics

Table 5. LDO Characteristics

T_A = 25°C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{LDOOUT}	Internal regulator output voltage	V_{LDOIN} = 3.3V Regulator input	1.71	1.8	1.89	V
I_{LDOOUT}	Output current	V_{LDOIN} = 2.7V Regulator input	—	—	200	mA
C_{LDO}	External filter capacitor value for internal core power supply	The capacitor value is dependent on the core power current consumption	2.2	—	10	μF

Power Consumption

Table 6. Power Consumption Characteristics

T_A = 25°C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DD}	Supply current (Run mode)	V_{DD33} = V_{BAT} = 3.3V, HSE = 8MHz, PLL = 144MHz, f_{HCLK} = 72MHz, f_{PCLK} = 72MHz, All peripherals enabled	—	60	72	mA
		V_{DD33} = V_{BAT} = 3.3V, HSE = 8MHz, PLL = 144MHz, f_{HCLK} = 72MHz, f_{PCLK} = 72MHz, All peripherals disabled	—	27	34	mA
	Supply current (Sleep mode)	V_{DD} = V_{BAT} = 3.3V, HSE = 8MHz, PLL = 144MHz, f_{HCLK} = 0MHz, f_{PCLK} = 72MHz, All peripherals enabled	—	42	50	mA
		V_{DD33} = V_{BAT} = 3.3V, HSE = 8MHz, PLL = 144MHz, f_{HCLK} = 0MHz, f_{PCLK} = 72MHz, All peripherals disabled	—	9	12	mA
	Supply current (Deep-Sleep1 mode)	V_{DD33} = V_{BAT} = 3.3V, All clock off (HSE/PLL/f_{HCLK}), LDO in low power mode, LSI on, RTC on	—	58	90	μA
	Supply current (Deep-Sleep2 mode)	V_{DD33} = V_{BAT} = 3.3V, All clock off (HSE/PLL/f_{HCLK}), LDO off (DMOS on), LSI on, RTC on	—	18	25	μA
	Supply current (Power-Down mode)	V_{DD33} = V_{BAT} = 3.3V, LDO off, LSE on, LSI off, RTC on	—	—	—	μA
		V_{DD33} = V_{BAT} = 3.3V, LDO off, LSE on, LSI off, RTC off	—	—	—	μA
		V_{DD33} = V_{BAT} = 3.3V, LDO off, LSE off, LSI on, RTC on	—	—	—	μA
		V_{DD33} = V_{BAT} = 3.3V, LDO off, LSE off, LSI on, RTC off	—	5	6	μA
I_{BAT}	Battery supply current (Power-Down mode)	V_{DD33} not present, V_{BAT} = 3.3V, LDO off, LSE off, LSI on, RTC on	—	4	—	μA
		V_{DD33} not present, V_{BAT} = 3.3V, LDO off, LSE off, LSI on, RTC off	—	3.9	—	μA

NOTES: 1. HSE is the high speed external oscillator. HSI means 8MHz high speed internal oscillator.
2. LSE means low speed external oscillator. LSI means 32.768KHz low speed internal oscillator.
3. RTC means real time clock.
4. Code = while (1) { 208 NOP } executed in Flash.

Reset and Supply Monitor Characteristics

Table 7. LVD/BOD Characteristics

T_A = 25°C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{BOD}	Brown Out Detector Voltage	—	—	2.6	—	V
V_{LVD}	Voltage of Low Voltage Detector	LVDS (Note1) = '00'	—	2.7	—	V
		LVDS (Note1) = '01'	—	2.8	—	V
		LVDS (Note1) = '10'	—	2.9	—	V
		LVDS (Note1) = '11'	—	3.0	—	V
V_{POR}	Power On Reset Voltage	—	—	1.36	—	V

NOTE: LVDS field is in PWRCU LVDCSR register.

External Clock Characteristics

Table 8. High Speed External Clock (HSE) Characteristics

T_A = 25°C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSE}	High Speed External oscillator frequency (HSE)	V_{DD33} = 3.3V	4	—	16	MHz
C_{HSE}	Recommended load capacitance on XTAL32IN and XTAL32OUT pins	—	—	TBD	—	pF
R_{FHSE}	Recommended external feedback resistor between XTAL32IN and XTAL32OUT pins	—	—	1.0	—	MΩ
D_{HSE}	HSE Oscillator Duty cycle	—	40	—	60	%
I_{DDHSE}	HSE Oscillator Operating Current	V_{DD33} = 3.3V, T_A = 25°C	—	0.96	—	mA
I_{STBHSE}	HSE Oscillator Standby current	V_{DD33} = 3.3V, T_A = 25°C	—	—	0.1	μA
t_{SUHSE}	HSE Oscillator Startup time	V_{DD33} = 3.3V, T_A = 25°C	—	—	4	ms

Table 9. Low Speed External Clock (LSE) Characteristics

T_A = 25°C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSE}	Low Speed External oscillator frequency (LSE)	V_{DD33} = V_{BAT} = 3.3V	—	32.768	—	kHz
C_{LSE}	Recommended load capacitance on XTAL32KIN and XTAL32KOUT pins	—	—	TBD	—	pF
R_{FLSE}	Recommended external feedback resistor between XTAL32KIN and XTAL32KOUT pins	—	—	10	—	MΩ
D_{LSE}	LSE Oscillator Duty cycle	—	40	—	60	%
I_{DDLSE}	LSE Oscillator Operating Current	V_{DD33} = V_{BAT} = 3.3V, LSESM = 0 (Normal startup mode)	—	1.7	—	μA
I_{STBLSE}	LSE Oscillator Standby current	V_{DD33} = V_{BAT} = 3.3V, LSESM = 1 (Fast startup mode)	—	3	8	μA
t_{SULSE}	LSE Oscillator Startup time	V_{DD33} = V_{BAT} = 3.3V, LSESM = 1 (Fast startup mode)	—	200	—	ms

Internal Clock Characteristics

Table 10. High Speed Internal Clock (HSI) Characteristics

T_A = 25°C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	High Speed Internal Oscillator Frequency (HSI)	V_{DD33} = 3.3V, T_A = -40°C ~ +85°C	—	8	—	MHz
ACC_{HSI}	HSI Oscillator Frequency accuracy	Factory-trimmed, V_{DD33} = 3.3V, T_A = -40°C ~ +85°C	-5	—	+5	%
D_{HSI}	HSI Oscillator Duty cycle	V_{DD33} = 3.3V, f_{HSI} = 8MHz	35	—	65	%
I_{DDHSI}	HSI Oscillator Operating Current	V_{DD33} = 3.3V, f_{HSI} = 8MHz	—	0.92	—	mA
t_{SUHSI}	HSI Oscillator Startup time	V_{DD33} = 3.3V, f_{HSI} = 8MHz, HSIRCBL = 0 (HSI Ready Counter Bits Length 7 Bits)	—	17	—	μs

NOTE: HSIRCBL field is in PWRCU HSIRCR register.

Table 11. Low Speed Internal Clock (LSI) Characteristics

T_A = 25°C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSI}	Low Speed Internal Oscillator Frequency(LSI)	V_{DD33} = V_{BAT} = 3.3V, T_A = -40°C ~ +85°C	25	32	43	kHz
I_{DDLSI}	LSI Oscillator Operating Current	V_{DD33} = V_{BAT} = 3.3V, T_A = 25°C	—	1.0	2	μA
t_{SULSI}	LSI Oscillator Startup time	V_{DD33} = V_{BAT} = 3.3V, T_A = 25°C	—	35	—	ms

PLL Characteristics

Table 12. PLL Characteristics

T_A = 25°C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PLLIN}	PLL input clock	—	4	—	16	MHz
f_{PLL}	PLL output clock	—	8	—	144	MHz
t_{LOCK}	PLL lock time	—	—	TBD	—	ms

Memory Characteristics

Table 13. Flash Memory Characteristics

T_A = 25°C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
N_{ENDU}	Number of guaranteed program /erase cycles before failure. (Endurance)	T_A= -40°C ~ +85°C	20	—	—	kcycles
T_{RET}	Data retention time	T_A = 25°C	100	—	—	Years
t_{PROG}	Word programming time	T_A = -40°C ~ +85°C	40	—	—	μs
t_{ERASE}	Page erase time	T_A = -40°C ~ +85°C	20	—	40	ms
t_{MERASE}	Mass erase time	T_A = -40°C ~ +85°C	20	—	40	ms

I/O Port Characteristics

Table 14. I/O Port Characteristics

T_A = 25°C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
I_{IL}	Low level input current	3.3V IO	V_I = 0V, On-chip pull-up resister disabled.	—	—	3	μA
		5V-tolerant IO		—	—	3	μA
		Reset pin		—	—	3	μA
I_{IH}	High level input current	3.3V IO	V_I = V_{DD33}, On-chip pull-down resister disabled.	—	—	3	μA
		5V-tolerant IO		—	—	3	μA
		Reset pin		—	—	3	μA
V_{IL}	Low level input voltage	3.3V IO		-0.3	—	0.8	V
		5V-tolerant IO		-0.3	—	0.8	V
		Reset pin		-0.3	—	0.8	V
V_{IH}	High level input voltage	3.3V IO		2	—	3.6	V
		5V-tolerant IO		2	—	5.5	V
		Reset pin		2	—	5.5	V
V_{HYS}	Schmitt Trigger Input Voltage Hysteresis	3.3V IO		—	400	—	mV
		5V-tolerant IO		—	400	—	mV
		Reset pin		—	400	—	mV
I_{OL}	Low level output current (GPO Sink current)	3.3V IO 4mA drive, V_{OL} = 0.4V		4	—	—	mA
		3.3V IO 8mA drive, V_{OL} = 0.4V		8	—	—	mA
		5V-tolerant 8mA drive IO, V_{OL}=0.4V		8	—	—	mA
		5V-tolerant 12mA drive IO, V_{OL}=0.4V		12	—	—	mA
		Backup Domain IO drive @ V_{BAT} =3.3V, V_{OL} = 0.4V, PB4, PB5, PB6		—	—	1	mA
I_{OH}	High level output current (GPO Source current)	3.3V I/O 4mA drive, V_{OH}=V_{DD33} - 0.4V		4	—	—	mA
		3.3V I/O 8mA drive, V_{OH}=V_{DD33} - 0.4V		8	—	—	mA
		5V-tolerant I/O 8mA drive, V_{OH} = V_{DD33} - 0.4V		8	—	—	mA
		5V-tolerant I/O 12mA drive, V_{OH} = V_{DD33} - 0.4V		12	—	—	mA
		Backup Domain IO drive@V_{BAT}=3.3V, V_{OH} = V_{DD33} - 0.4V, PB4, PB5, PB6		—	—	1	mA
V_{OL}	Low level output voltage	3.3V 4mA drive IO, I_{OL} = 4mA		—	—	0.4	V
		3.3V 8mA drive IO, I_{OL} = 8mA		—	—	0.4	V
		5V-tolerant 8mA drive IO, I_{OL}=8mA		—	—	0.4	V
		5V-tolerant 12mA drive IO, I_{OL}=12mA		—	—	0.4	V
V_{OH}	High level output voltage	3.3V 4mA drive IO, I_{OH} = 4mA		V_{DD33} - 0.4V	—	—	V
		3.3V 8mA drive IO, I_{OH} = 8mA		V_{DD33} - 0.4V	—	—	V
		5V-tolerant 8mA drive IO, I_{OH}=8mA		V_{DD33} - 0.4V	—	—	V
		5V-tolerant 12mA drive IO, I_{OH}=12mA		V_{DD33} - 0.4V	—	—	V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{PU}	Internal pull-up resistor	3.3V I/O	34	—	74	kΩ
		5V-tolerant I/O	38	—	89	kΩ
R_{PD}	Internal pull-down resistor	3.3V I/O	29	—	86	kΩ
		5V-tolerant I/O	35	—	107	kΩ

ADC Characteristics

Table 15. ADC Characteristics

T_A = 25°C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Operating voltage	—	2.7	3.3	3.6	V
V_{ADCIN}	A/D Converter input voltage range	—	0	—	V_{REF+}	V
V_{REF+}	A/D Converter Reference voltage	—	—	V_{DDA}	V_{DDA}	V
I_{ADC}	Current consumption	V_{DDA} = 3.3V	—	1	TBD	mA
I_{ADC_DN}	Power down current consumption	V_{DDA} = 3.3V	—	1	10	μA
f_{ADC}	A/D Converter clock	—	0.7	—	14	MHz
f_S	Sampling rate	—	0.05	—	1	MHz
$f_{ADCCONV}$	A/D Converter conversion time	—	—	14	—	$1/f_{ADC}$ Cycles
R_I	Input sampling switch resistance	—	—	—	1	kΩ
C_I	Input sampling capacitance	No pin/pad capacitance included	—	—	5	pF
t_{SU}	Start up time	—	—	—	1	μs
N	Resolution	—	—	12	—	bits
INL	Integral Non-linearity error	f_S = 1MHz, V_{DDA} = 3.3V	-—	±2	±5	LSB
DNL	Differential Non-linearity error	f_S = 1MHz, V_{DDA} = 3.3V	—	—	±1	LSB
E_O	Offset error	—	—	—	±10	LSB
E_G	Gain error	—	—	—	±10	LSB

NOTES: 1. Guaranteed by design, not tested in production.

2. The figure below shows the equivalent circuit of the A/D Converter Sample-and-Hold input stage where C_I is the storage capacitor, RI is the resistance of the sampling switch and R_S is the output impedance of the signal source V_S. Normally the sampling phase duration is approximately, $1.5/f_{ADC}$. The capacitance, C_I, must be charged within this time frame and it must be ensured that the voltage at its terminals becomes sufficiently close to V_S for accuracy. To guarantee this, R_S may not have an arbitrarily large value.

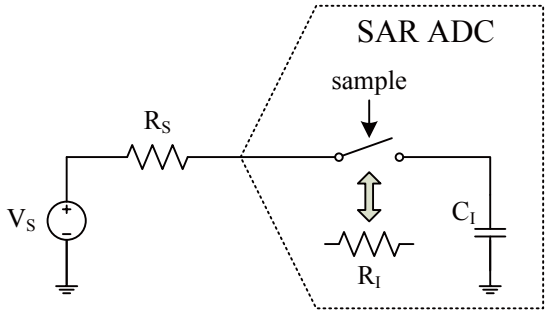


Figure 7. ADC Sampling Network Model

The worst case occurs when the extremities of the input range (0V and V_{REF}) are sampled consecutively. In this situation a sampling error below 1/4 LSB is ensured by using the following equation:

$$R_S < \frac{1.5}{f_{ADC} C_I \ln(2^{N+2})} - R_I$$

where f_{ADC} is the ADC clock frequency and N is the ADC resolution (N = 12 in this case). A safe margin should be considered due to the pin/pad parasitic capacitances, which are not accounted for in this simple model.

If, in a system where this A/D Converter is used, there are no rail-to-rail input voltage variations between consecutive sampling phases, Rs may be larger than the value indicated by the equation above.

Operation Amplifier/Comparator Characteristics

Table 16. OPA/CMP Characteristics

T_A = 25°C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Operating voltage	—	2.7	3.3	3.6	V
$I_{OPA/CMP}$	Typical operating current	—	—	230	—	μA
I_{OPA/CMP_DN}	Power down supply current	Assign registers OPAEN = 0 and EN_OPAOP = 0	—	—	0.1	μA
V_{IOS}	Input offset voltage	V_{DDA} = 3.3V, AnOF[5:0] = '100000'	-15	—	15	mV
		V_{DDA} = 3.3V, After calibration	-1	—	1	mV
V_{IOS_DRIFT}	Input offset voltage drift	T_A = -40°C ~ +85°C	—	—	0.04	mV/°C
R_{INPUT}	Input resistance	—	—	10	—	MΩ
GV	Voltage Gain	—	60	100	—	dB
U_t	Unit-Gain Bandwidth	R_L = 100kΩ	—	1.3	—	MHz
		R_L = 100kΩ, C_L = 100pF	—	1.24	—	
V_{CM}	Common mode voltage range	V_{DDA} = 3.3V	V_{SSA}	—	V_{DDA} – 1.2	V
V_{OV}	OPA output voltage swing	V_{DDA} = 3.3V	V_{SSA} + 0.3	—	V_{DDA} – 0.5	V
t_{RT}	Comparator response time	V_{DDA} = 3.3V; Input Overdrive = ±10mV	—	1	—	μs
SR	Slew Rate	V_{DDA} = 3.3V; Output capacitor load C_L=100pF	—	1.6	—	V/μs

NOTE: Guaranteed by design, not tested in production.

GPTM/MCTM Characteristics

Table 17. GPTM/MCTM Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{TM}	Timer clock source for GPTM and MCTM	—	—	—	72	MHz
t_{RES}	Timer resolution time	—	1	—	—	f_{TM}
f_{EXT}	External signal frequency on channel 1 ~ 4	—	—	—	1/2	f_{TM}
RES	Timer resolution	—	—	—	16	bits

I²C Characteristics

Table 18. I²C Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCL}	SCL clock frequency	—	—	—	400	kHz
$t_{SCL(H)}$	SCL clock high time	—	600	—	—	ns
$t_{SCL(L)}$	SCL clock low time	—	1300	—	—	ns
t_{FALL}	SCL and SDA fall time	—	—	—	300	ns
t_{RISE}	SCL and SDA rise time	—	—	—	300	ns
$t_{SU(STA)}$	START condition setup time	—	600	—	—	ns
$t_{H(STA)}$	START condition hold time	—	600	—	—	ns
$t_{SU(SDA)}$	SDA data setup time	—	100	—	—	ns
$t_{H(SDA)}$	SDA data hold time	—	0	—	—	ns
$t_{SU(STO)}$	STOP condition setup time	—	600	—	—	ns

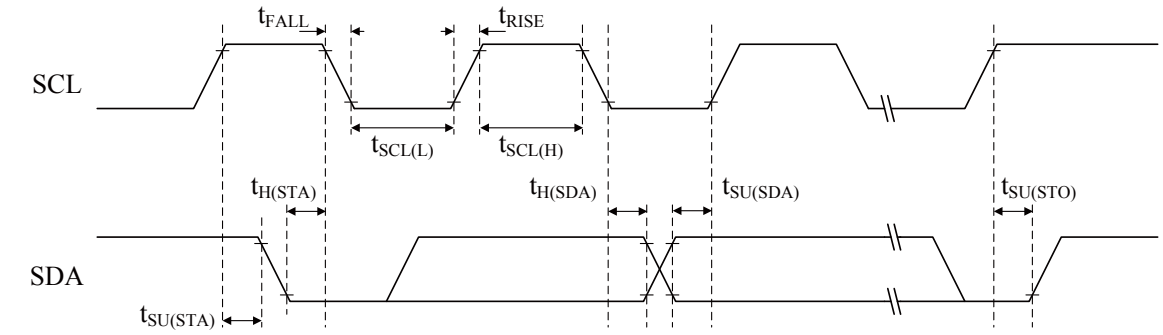


Figure 8. I²C Timing Diagrams

SPI Characteristics

Table 19. SPI Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK}	SCK clock frequency	—	—	—	$f_{PCLK}/4$	MHz
$t_{SCK(H)}$	SCK clock high time	—	$f_{PCLK}/8$	—	—	ns
$t_{SCK(L)}$	SCK clock low time	—	$f_{PCLK}/8$	—	—	ns
SPI Master mode						
$t_{V(MO)}$	Data output valid time	—	—	—	5	ns
$t_{H(MO)}$	Data output hold time	—	2	—	—	ns
$t_{SU(MI)}$	Data input setup time	—	5	—	—	ns
$t_{H(MI)}$	Data input hold time	—	5	—	—	ns
SPI Slave mode						
$t_{SU(SEL)}$	SEL enable setup time	—	4 t_{PCLK}	—	—	ns
$t_{H(SEL)}$	SEL enable hold time	—	2 t_{PCLK}	—	—	ns
$t_{A(SO)}$	Data output access time	—	—	—	3 t_{PCLK}	ns
$t_{DIS(SO)}$	Data output disable time	—	—	—	10	ns
$t_{V(SO)}$	Data output valid time	—	—	—	25	ns
$t_{H(SO)}$	Data output hold time	—	15	—	—	ns
$t_{SU(SI)}$	Data input setup time	—	5	—	—	ns
$t_{H(SI)}$	Data input hold time	—	4	—	—	ns

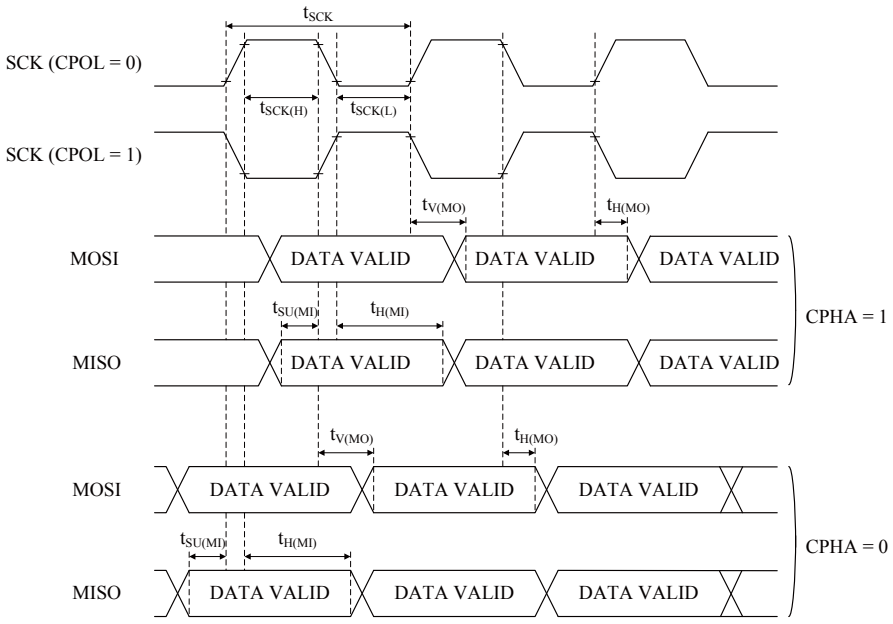


Figure 9. SPI Timing Diagrams – SPI Master Mode

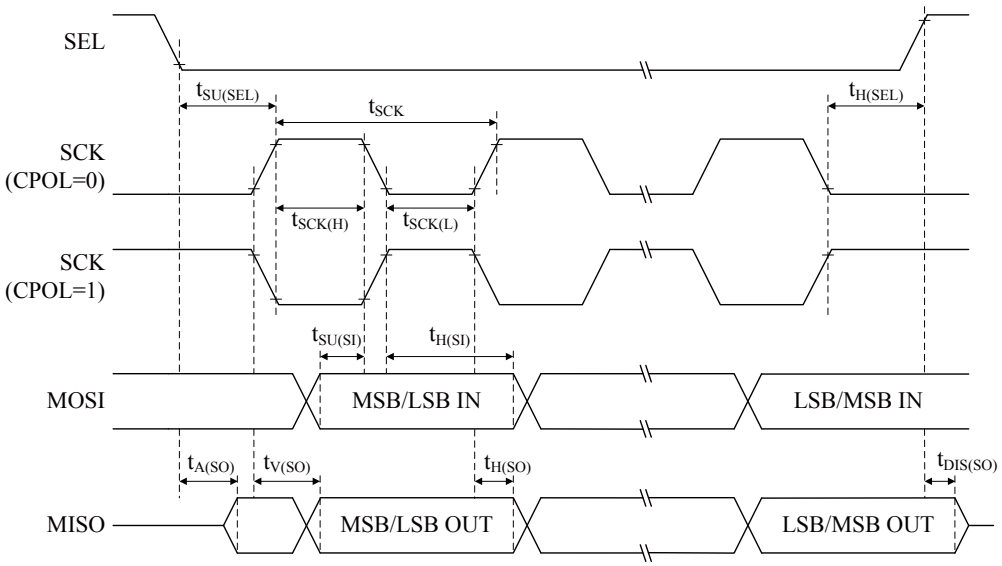


Figure 10. SPI Timing Diagrams – SPI Slave Mode and CPHA=1

CSIF Characteristics

Table 20. CSIF Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{MCK}	CSIF_MCK clock frequency output	—	—	—	36	MHz
f_{PCK}	CSIF_PCK clock frequency input	—	—	—	24	MHz
r_F	APB clock and CSIF_PCK clock input frequency ratio	f_{PCLK}/f_{PCK}	—	—	3	—

USB Characteristics

The USB interface is USB-IF certified – Full Speed.

Table 21. USB DC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	USB Operating voltage	—	3.0	—	3.6	V
V_{DI}	Differential input sensitivity	|USBDP-USBDM|	0.2	—	—	V
V_{CM}	Common mode voltage range	—	0.8	—	2.5	V
V_{SE}	Single-ended receiver threshold	—	0.8	—	2.0	V
V_{OL}	Pad output low voltage	R_L of 1.5kΩ to V_{DD}	0	—	0.3	V
V_{OH}	Pad output high voltage		2.8	—	3.6	V
V_{CRS}	Differential output signal cross-point voltage	—	1.3	—	2.0	V
Z_{DRV}	Driver output resistance	—	—	10	—	Ω
C_{IN}	Transceiver pad capacitance	—	—	—	20	pF

NOTES: 1. Guaranteed by design, not tested in production.

2. To be compliant with the USB 2.0 full-speed electrical specification, the USBDP pin should be pulled up with a 1.5kΩ external resistor to a 3.0 to 3.6V voltage supply.

3. The USB functionality is ensured down to 2.7V but not the full USB electrical characteristics which will experience degradation in the 2.7 to 3.0V V_{DD} voltage range.

4. R_L is the load connected to the USB driver USBDP.

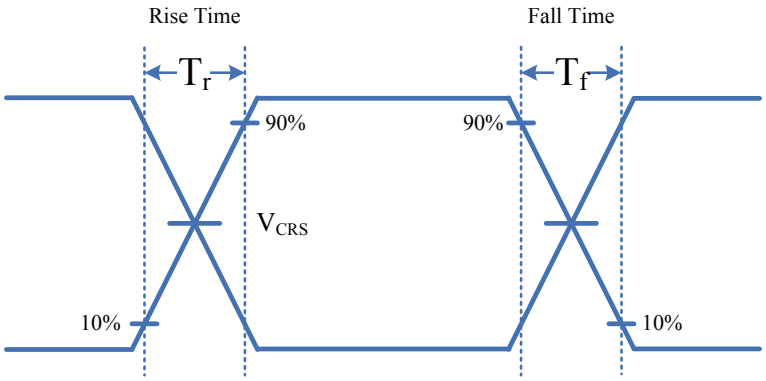


Figure 11. USB Signal Rise Time and Fall time and Cross-Point Voltage (V_{CRS}) Definition

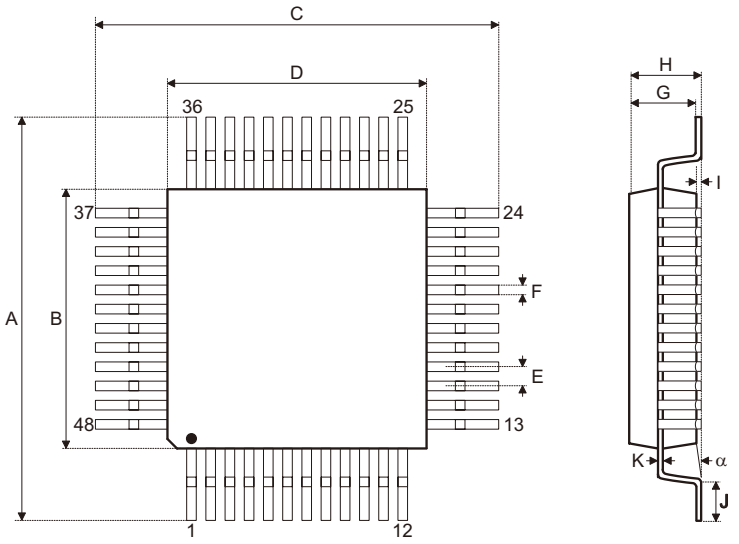
Table 22. USB AC Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_r	Rise time	C_L = 50pF	4	—	20	ns
T_f	Fall time	C_L = 50pF	4	—	20	ns
$T_{r/f}$	Rise time / fall time matching	$T_{r/f} = T_r / T_f$	90	—	110	%

5 Package Information

Note that the package information provided here is for consultation purposes only. As this information may be updated at regular intervals users are reminded to consult the Holtek website (http://www.holtek.com.tw/english/literature/package.pdf) for the latest version of the package information.

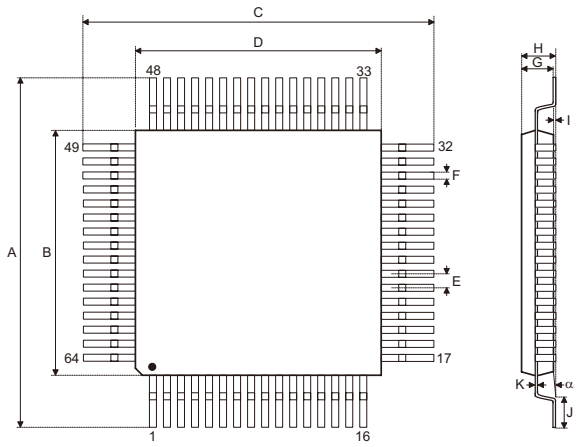
48-pin LQFP (7mm×7mm) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	0.350	—	0.358
B	0.272	—	0.280
C	0.350	—	0.358
D	0.272	—	0.280
E	—	0.020	—
F	—	0.008	—
G	0.053	—	0.057
H	—	—	0.063
I	—	0.004	—
J	0.018	—	0.030
K	0.004	—	0.008
α	0°	—	7°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	8.90	—	9.10
B	6.90	—	7.10
C	8.90	—	9.10
D	6.90	—	7.10
E	—	0.50	—
F	—	0.20	—
G	1.35	—	1.45
H	—	—	1.60
I	—	0.10	—
J	0.45	—	0.75
K	0.10	—	0.20
α	0°	—	7°

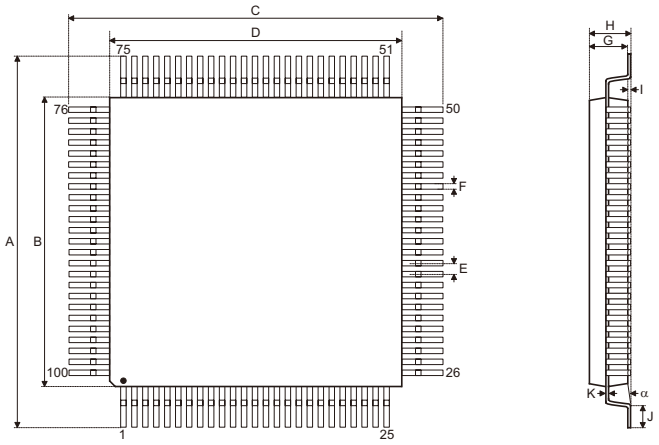
64-pin LQFP (7mm×7mm) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	0.350	—	0.358
B	0.272	—	0.280
C	0.350	—	0.358
D	0.272	—	0.280
E	—	0.016	—
F	0.005	—	0.009
G	0.053	—	0.057
H	—	—	0.063
I	0.002	—	0.006
J	0.018	—	0.030
K	0.004	—	0.008
α	0°	—	7°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	8.90	—	9.10
B	6.90	—	7.10
C	8.90	—	9.10
D	6.90	—	7.10
E	—	0.40	—
F	0.13	—	0.23
G	1.35	—	1.45
H	—	—	1.60
I	0.05	—	0.15
J	0.45	—	0.75
K	0.09	—	0.20
α	0°	—	7°

100-pin LQFP (14mm×14mm) Outline Dimensions



Symbol	Dimensions in inch		
	Min.	Nom.	Max.
A	0.626	—	0.634
B	0.547	—	0.555
C	0.626	—	0.634
D	0.547	—	0.555
E	—	0.020	—
F	—	0.008	—
G	0.053	—	0.057
H	—	—	0.063
I	—	0.004	—
J	0.018	—	0.030
K	0.004	—	0.008
α	0°	—	7°

Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	15.90	—	16.10
B	13.90	—	14.10
C	15.90	—	16.10
D	13.90	—	14.10
E	—	0.50	—
F	—	0.20	—
G	1.35	—	1.45
H	—	—	1.60
I	—	0.10	—
J	0.45	—	0.75
K	0.10	—	0.20
α	0°	—	7°

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