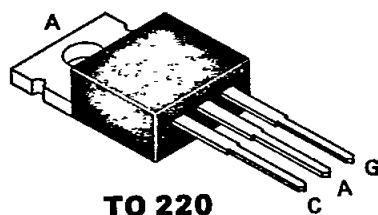


**S1005BH –
S1005NH SCR'S****10 A 200–800 V < 5 mA**

The S1005 series silicon controlled rectifiers are high performance glass passivated PNP devices. These parts are intended for general purpose high voltage applications where moderate gate sensitivity is required.

**Absolute Maximum Ratings** $T_A = 25^\circ\text{C}$ unless otherwise noted

Parameter	Part Nr.	Symbol	Min.	Max.	Unit	Test Conditions
Repetitive Peak Off State Voltage	S1005BH S1005DH S1005MH S1005NH	V_{DRM} V_{RRM}	200 400 600 800		V	$T_j = -40^\circ\text{C}$ to 125°C $R_{\text{GK}} = 1\text{K}\Omega$
On-State Current		$I_{\text{T(RMS)}}$	10		A	
Average On-State Current		$I_{\text{T(AV)}}$	6.4		A	
Nonrept. On-State Current		I_{TSM}	110		A	
Nonrept. On-State Current		I_{TSM}	100		A	Half Cycle, 50 Hz
Fusing Current		I^2t	32		A^2s	$t = 10\text{ ms}$, Half Cycle
Peak Gate Current		I_{GM}	4		A	$10\mu\text{s}$ max.
Peak Gate Dissipation		P_{GM}	10		W	$10\mu\text{s}$ max.
Gate Dissipation		$P_{\text{G(AV)}}$	1		W	20 ms max.
Operating Temperature		T_j	-40	125	$^\circ\text{C}$	
Storage Temperature		T_{stg}	-40	125	$^\circ\text{C}$	
Soldering Temperature		T_{sld}		250	$^\circ\text{C}$	1.6 mm from case, 10 s max.

Electrical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Min.	Max.	Unit	Test Conditions
Off-State Leakage Current	$I_{\text{DRM}}/I_{\text{RRM}}$		1.5	mA	@ $V_{\text{DRM}} + V_{\text{RRM}}$, $R_{\text{GK}} = 1\text{K}\Omega$, $T_j = 125^\circ\text{C}$
Off-State Leakage Current	$I_{\text{DRM}}/I_{\text{RRM}}$		5	μA	@ $V_{\text{DRM}} + V_{\text{RRM}}$, $R_{\text{GK}} = 1\text{K}\Omega$, $T_j = 25^\circ\text{C}$
On-State Voltage	V_{T}		2.05	V	at $I_{\text{T}} = 20\text{ A}$, $T_j = 25^\circ\text{C}$
On-State Threshold Voltage	$V_{\text{T(TO)}}$		1.15	V	$T_j = 125^\circ\text{C}$
On-State Slope Resistance	r_{T}		52	$\text{m}\Omega$	$T_j = 125^\circ\text{C}$
Gate Trigger Current	I_{GT}		5	mA	$V_{\text{D}} = 7\text{ V}$
Gate Trigger Voltage	V_{GT}		2.0	V	$V_{\text{D}} = 7\text{ V}$
Holding Current	I_{H}		7.5	mA	$R_{\text{GK}} = 1\text{K}\Omega$
Latching Current	I_{L}		15	mA	$R_{\text{GK}} = 1\text{K}\Omega$
Critical Rate of Voltage Rise	dv/dt	20		$\text{V}/\mu\text{s}$	$V_{\text{D}} = .67 \times V_{\text{DRM}}$, $R_{\text{GK}} = 1\text{K}\Omega$, $T_j = 125^\circ\text{C}$
Critical Rate of Current Rise	di/dt	100		$\text{A}/\mu\text{s}$	$I_{\text{G}} = 25\text{ mA}$, $di_{\text{G}}/dt = 0.25\text{ A}/\mu\text{s}$, $T_j = 125^\circ\text{C}$
Gate Controlled Delay Time	t_{gd}		500	ns	$I_{\text{G}} = 25\text{ mA}$, $di_{\text{G}}/dt = 0.25\text{ A}/\mu\text{s}$
Commutated Turn-Off Time	t_{q}		50	μs	$T_{\text{C}} = 85^\circ\text{C}$, $V_{\text{D}} = .67 \times V_{\text{DRM}}$, $V_{\text{R}} = 35\text{ V}$, $I_{\text{T}} = I_{\text{T(AV)}}$
Thermal Resistance junc. to case	$R_{\theta\text{jc}}$		3	K/W	
Thermal Resistance junc. to amb.	$R_{\theta\text{ja}}$		60	K/W	

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