SPECIFICATION

OF

ORGANIC LIGHT EMITTING DIODES MODULE

UNITED RADIANT TECHNOLOGY CORP. 光聯科技 Sep-22-2008 品管部 QC DEPT.

CUSTOMER : URT-STD

Model No. : UMOH-8255N-O

Model version : 0

Document Revision : 0

CUSTOMER APPROVED SIGNATURE			

This specification need to be signed by purchaser or customer as a specification of products production and delivery from URT. Without signature of this specification , any purchase order for this model no. will be treated and considered that this specification is automatically acknowledged and accepted by purchaser or customer.

U.R.T. UNITED RADIANT TECHNOLOGY CORPORATION

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APPROVED	CHECKED	CHECKED	PREPARED	Date

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Revision record

Document Revision	Model No. Version No.	Description	Revision by
0	UMOH-8255N-O Version No. 0		H.C.Lin Neo Hor 22-Sep-2008

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1. BASIC SPECIFICATION

1.1 Mechanical specifications

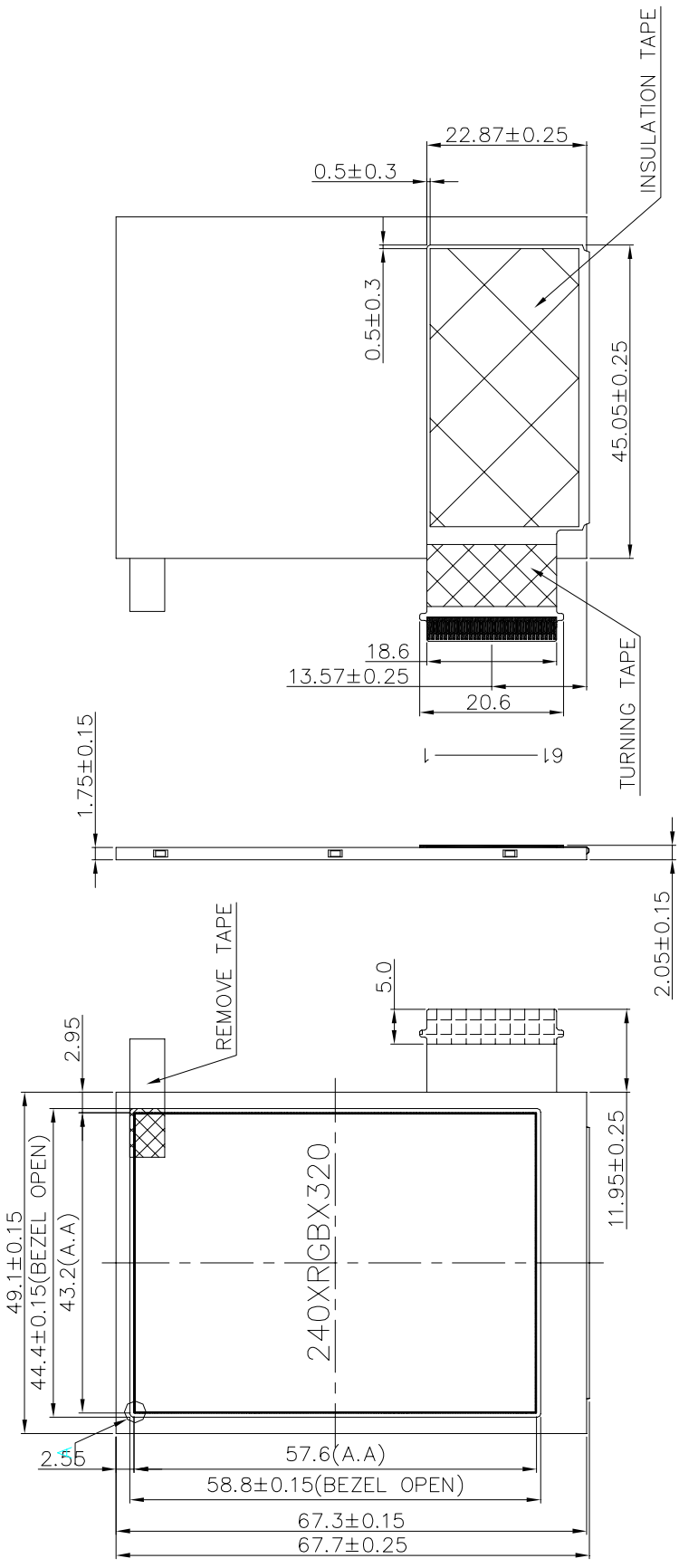
Items	Nominal Dimension	Unit
Dot Matrix	240*RGB*320	dots
Module Size (W x H x T)	49.1 x 67.7 x 1.75	mm.
Active Area (W x H)	43.2 x 57.6	mm.
Dot Pitch (W x H)	0.18 x 0.18	mm.
Driving IC Package	COG	-
Weight	16	g

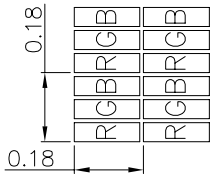
* Expose the driver IC under blaze (luminosity over than 1 cd) when using the LCM may cause IC operating failure.

1.2 Display specification

Display	Descriptions	Note
LCD Type	Display	-
LCD Mode	262K Full Color	-
Background Color	-	-
Backlight Type	-	-
Backlight Color	-	-
Viewing Direction	-	-

1.3 Outline dimension





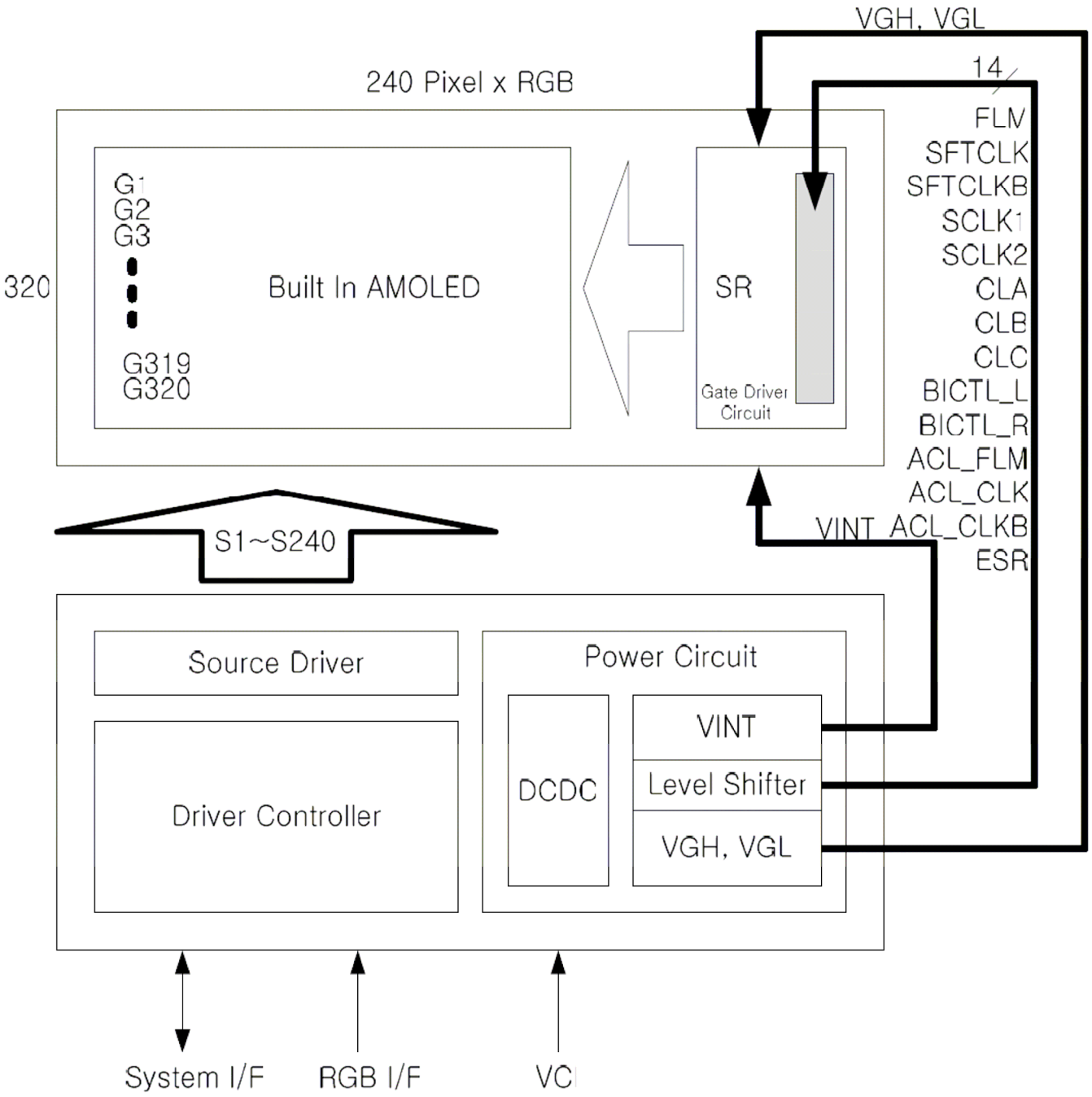
DETAIL A

NOTE:
1. DOT MATRIX: 240X320
2. DOT PITCH: 0.18X0.18(mm)
3. CONNECTOR: HIROSE FH23-61S-0.3SHW(05)

PIN ASSIGNMENT

No	Define	No	Define	No	Define	No	Define	No	Define
1	AR_VDD	14	C32M	27	DB13	40	DB0	53	VREGIOUT
2	AR_VSS	15	VLOUT3	28	DB12	41	VSYNC	54	VCI
3	VCI	16	VLOUT2	29	DB11	42	HSYNC	55	VGH
4	VCI1	17	C21P	30	DB10	43	DOTCLK	56	VGL
5	GND	18	C21M	31	DB9	44	ENABLE	57	GND
6	C12M	19	VGS	32	DB8	45	SDI	58	X-
7	C12P	20	IOVCC	33	DB7	46	SDO	59	Y-
8	C11M	21	SPB	34	DB6	47	CSB	60	X+
9	C11P	22	ID_MIB	35	DB5	48	RW_WRB	61	Y+
10	VLOUT1	23	DB17	36	DB4	49	RS		
11	C31P	24	DB16	37	DB3	50	E_RDB		
12	C31M	25	DB15	38	DB2	51	RESETB		
13	C32P	26	DB14	39	DB1	52	MVDD		

1.4 Block diagram:



1.5 Interface pin :

PIN	Symbol	I/O	Description	Remarks
1	AR_VDD	I	Positive voltage for OLED(+4.6V)	
2	AR_VSS	I	Nagative voltage for OLED(-4.4V)	
3	VCI	I	Power supply for analog circuit(2.5v~3.3v)	
4	VCI1	O	A reference voltage for 1st booster(connect a 1u/10v capacitance to gnd)	
5	GND	I	Ground	
6	C12M	I	External capacitance connect pin between C12M and C12P (1u/10V)	
7	C12P	I		
8	C11M	I	External capacitance connect pin between C11M and C11P	
9	C11P	I		
10	VLOUT1	O	1st booster output pin. (1u/10V)	
11	C31P	I	External capacitance connect pin between C31M and C31P (1u/10V)	
12	C31M	I		
13	C32P	I	External capacitance connect pin between C32M and C32P (1u/10V)	
14	C32M	I		
15	VLOUT3	O	3rd booster output pin. (1u/16V)	
16	VLOUT2	O	2nd booster output pin. (1u/16V)	
17	C21P	I	External capacitance connect pin between C21M and C21P. (1u/10V)	
18	C21M	I		
19	VGS	I	A reference level for the grayscale voltage generation circuit. (connect to gnd)	
20	IOVCC	I	I/O power supply	
21	SPB	I	Select the CPU interface mode. (0=parallel interface 1=serial interface)	
22	ID_MIB	I	Select the CPU type (0=intel 80x-system 1=motorola 68x-system)	
23	DB17	I/O	BI-directional data bus. When CPU I/F, 18-bit interface : DB 17-0 16-bit interface : DB 17-10 , DB 8-1 9-bit interface : DB 8-0 8-bit interface : DB 8-1 When RGB I/F 18-bit interface : DB 17-0 18-bit interface : DB 17-0 16-bit interface : DB 17-10, DB 8-1 6-bit interface : DB 8-3 Fix unused pin to the VSS level	
24	DB16	I/O		
25	DB15	I/O		
26	DB14	I/O		
27	DB13	I/O		
28	DB12	I/O		
29	DB11	I/O		
30	DB10	I/O		
31	DB9	I/O		
32	DB8	I/O		
33	DB7	I/O		

1.5.1 Interface Pin : (cont)

<table>
<tr><td>34</td><td>DB6</td><td>I/O</td><td></td><td></td></tr>
<tr><td>35</td><td>DB5</td><td>I/O</td><td></td><td></td></tr>
<tr><td>36</td><td>DB4</td><td>I/O</td><td></td><td></td></tr>
<tr><td>37</td><td>DB3</td><td>I/O</td><td></td><td></td></tr>
<tr><td>38</td><td>DB2</td><td>I/O</td><td></td><td></td></tr>
<tr><td>39</td><td>DB1</td><td>I/O</td><td></td><td></td></tr>
<tr><td>40</td><td>DB0</td><td>I/O</td><td></td><td></td></tr>
<tr><td>41</td><td>VSYNC</td><td>I</td><td>Frame-synchronizing signal.
(VSPL=0 Low active, VSPL=1 High active)
FIX this pin at VSS level if the pin is not used</td><td></td></tr>
<tr><td>42</td><td>HSYNC</td><td>I</td><td>Line-synchronizing signal.
(HSPL=0 Low active, HSPL=1 High active)
FIX this pin at VSS level if the pin is not used</td><td></td></tr>
<tr><td>43</td><td>DOTCLK</td><td>I</td><td>Input pin for clock signal of external interface : dot clock.
DPL=0 Display data is fetched at DOTCLK's rising edge
DPL=1 Display data is fetched at DOTCLK's falling edge
Fix this pin at VSS level if the pin is not used.</td><td></td></tr>
<tr><td>44</td><td>ENABLE</td><td>I</td><td>Data enablesignal pin for RGB interface.
<table>
<tr><td>EPL</td><td>ENABLE</td><td>GRAM write</td><td>GRAM address</td></tr>
<tr><td>0</td><td>0</td><td>Valid</td><td>Updated</td></tr>
<tr><td>0</td><td>1</td><td>Invalid</td><td>Held</td></tr>
<tr><td>1</td><td>0</td><td>Invalid</td><td>Held</td></tr>
<tr><td>1</td><td>1</td><td>Valid</td><td>Updated</td></tr>
</table></td><td></td></tr>
<tr><td>45</td><td>SDI</td><td>I</td><td>For a serial peripheral interface(SPI), input data is fetched at the rising edge of the SCL signal, Fix SDI pin at VSS level if the pin is not used.</td><td></td></tr>
<tr><td>46</td><td>SDO</td><td>I</td><td>For a serial peripheral interface (SPI), serves as the serial data olutput pin(SDO), Successive bits are output at the falling edge of the SCL signal.</td><td></td></tr>
<tr><td>47</td><td>CSB</td><td>I</td><td>Chip select signal input pin.
0= driver IC is selected and can be accessed.
1= driver IC is not selected and cannot be accessed.</td><td></td></tr>
<tr><td>448</td><td>RW_WRB</td><td>I</td><td>
<table>
<tr><td>Pin function</td><td>CPU type</td><td>Pin description</td></tr>
<tr><td>RW</td><td>68-system</td><td>Read/Write operation selection pin
0=write 1=read</td></tr>
<tr><td>WRB</td><td>80_system</td><td>Write strobe signal.(Input pin)
Data is fetched at the rising edge.</td></tr>
<tr><td>SCL</td><td>SPI</td><td>The synchronous clock signal</td></tr>
</table></td><td></td></tr>
<tr><td>49</td><td>RS</td><td>I</td><td>Register select pin.
0=Index/status, 1=instruction parameter, GRAM data
Must be fixed at VDD3 level when not used.</td><td></td></tr>
<tr><td>50</td><td>E_RDB</td><td>I</td><td>
<table>
<tr><td>Pin Function</td><td>CPU type</td><td>Pin description</td></tr>
<tr><td>E</td><td>68-system</td><td>Read/Writeoperation enable pin</td></tr>
<tr><td>RDB</td><td>80_system</td><td>Read strobe signal.
Read out data at the low level</td></tr>
<tr><td colspan="3">When SPI mode is selected , fix this pin at VDD3 level</td></tr>
</table></td><td></td></tr>
<tr><td>51</td><td>RESETB</td><td>I</td><td>Reset pin initializes the IC when low. Should be reset after power-on.</td><td></td></tr>
<tr><td>52</td><td>MVDD</td><td>O</td><td>Internal power for RAM. Connect a capacitance(1u/10v) to gnd.</td><td></td></tr>
<tr><td>53</td><td>VREG1OUT</td><td>O</td><td>A reference level for the grayscale voltage. Connect a capacitance(1u/10v) to gnd.</td><td></td></tr>
<tr><td>54</td><td>VCI</td><td>I</td><td>Power supply for analog circuit(2.5v~3.3v)</td><td></td></tr>
</table>

1.5.2 Interface Pin : (cont)

55	VGH	O	The positive voltage used in the gate driver. Connect a capacitance(1u/10v) to gnd.	
56	VGL	O	The negative voltage used in the gate driver. Connect a capacitance(1u/10v) to gnd.	
57	GND		Ground	
58	NC		NO Connection	
59	NC		NO Connection	
60	NC		NO Connection	
61	NC		NO Connection	

2. ELECTRICAL CHARACTERISTICS

2.1 Absolute Maximum Ratings

Items	Symbol	Min.	Max.	Unit
Supply voltage1	**VDD3**	-0.3	5	V
Supply voltage2	**VCI**	-0.3	5	V
Input voltage	**Vin**	-0.3	VDD+0.5	V
Operating temperature range	T_{OP}	-20	60	℃
Storage temperature range	T_{ST}	-30	80	℃

2.2 DC Characteristics

Items	Symbol	Min.	Typ.	Max.	Unit	Condition
Driving voltage	VGH	3.0	-	8.0	V	
	VGL	-8.0	-	-3.0	V	
	VINT	-4.0	-	-1.0	V	
Logic operating Voltage	RVDD	1.45	1.5	1.55	V	
Power supply voltage	VCI	2.5	2.8	3.3	V	
Power supply voltage	VDD3	1.65	1.8	3.3	V	
Operating frequency	Fosc	1161.1	1290.2	1419.3	kHZ	
1st booster input voltage	Vci1	2.1	-	2.75	V	
Current consumption during normal operation	IVDD3	-	1.0	5.0	uA	NOTE
	IVCI	-	3.5	4.0	mA	
Stand by mode current	IVDD3	-	0.1	5	uA	
	IVCI	-	10	20	uA	
Input High level voltage	VIH	0.7VDD3	-	VDD3	V	
Input low level voltage	VIL	0	-	0.3VDD3	V	
Output High level voltage	VOH	0.8VDD3	-	VDD3	V	
Output low level voltage	VOL	0	-	0.2VDD3	V	
VREG1OUT		4.185	4.2	4.215	V	

NOTE:

VDD3=1.8V, VCI=2.8V, fosc=1290.2KHz (320 display line), NL[5:0]=" 10_1000", SAP[2:0]="101", DC22[2:0]="100", DC12[2:0]="010" , BT[1:0]=10, VC[3:0]="1000", VGH[4:0]="10100", VGL[4:0]="10100", VINT[3:0]="0101'

2.3 Command Sequence (Recommend by U.R.T.)

Measuring surrounding: Dark room

Surrounding temperature: 25oC

IOVCC = 1.65V ~ 3.3V

a. AR_VDD= 4.6V+/- 0.03V, AR_VSS= -4.4V+/- 0.03V

b. IC Initial Register Setting:

R03h: 0x0030 // 16bit mode

R10h: 0x0000 // IC standby off

R18h: 0x0028 // Frame Rate = 80 Hz

RF8h: 0x000F // VGH=+5V

RF9h: 0x000F // VGL=-5V

R05h: 0x0001 // display on

Gamma Register Setting:

R70h: 0x2580

R71h: 0x2780

R72h: 0x3380

R73h: 0x1D18

R74h: 0x1F11

R75h: 0x2419

R76h: 0x1A14

R77h: 0x211A

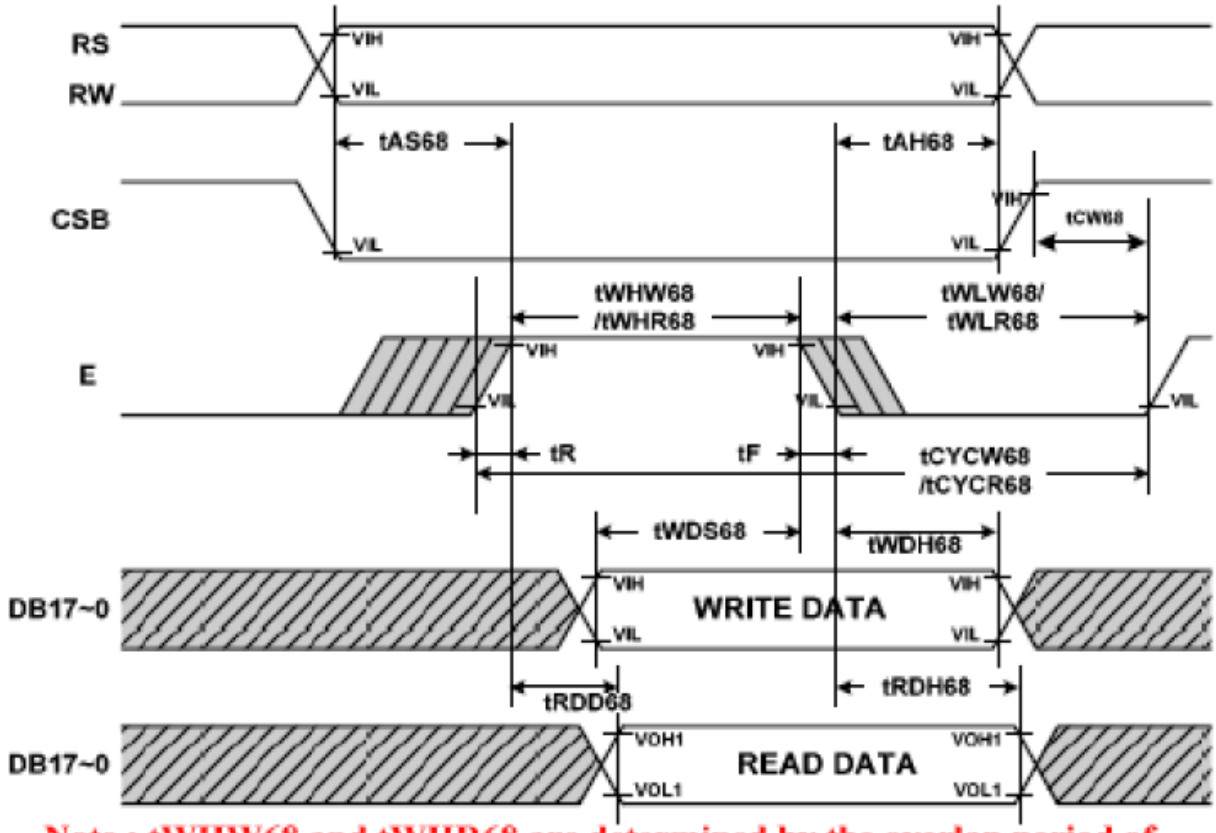
R78h: 0x2013

2.4 AC Characteristics

CPU interface M68

(VDD = 1.5V, VDD3 = 1.65 to 3.3V, TA = -40 to +85°C)

Characteristic		Symbol	Specification		Unit
			Min.	Max.	
Cycle time	Write	tCYCW68	85	-	ns
	Read	tCYCR68	500	-	ns
Pulse rise / fall time		tR, tF	-	15	ns
Pulse width low	Write	tWLW68	27.5	-	ns
	Read	tWLR68	250	-	ns
Pulse width high	Write	tWHW68	27.5	-	ns
	Read	tWHR68	250	-	ns
RS,RW to CSB, E setup time		tAS68	10	-	ns
RS,RW to CSB, E hold time		tAH68	2	-	ns
CSB to E time		tCW68	15	-	ns
Write data setup time		tWDS68	40	-	ns
Write data hold time		tWDH68	15	-	ns
Read data delay time		tRDD68	-	200	ns
Read data hold time		tRDH68	5	-	ns

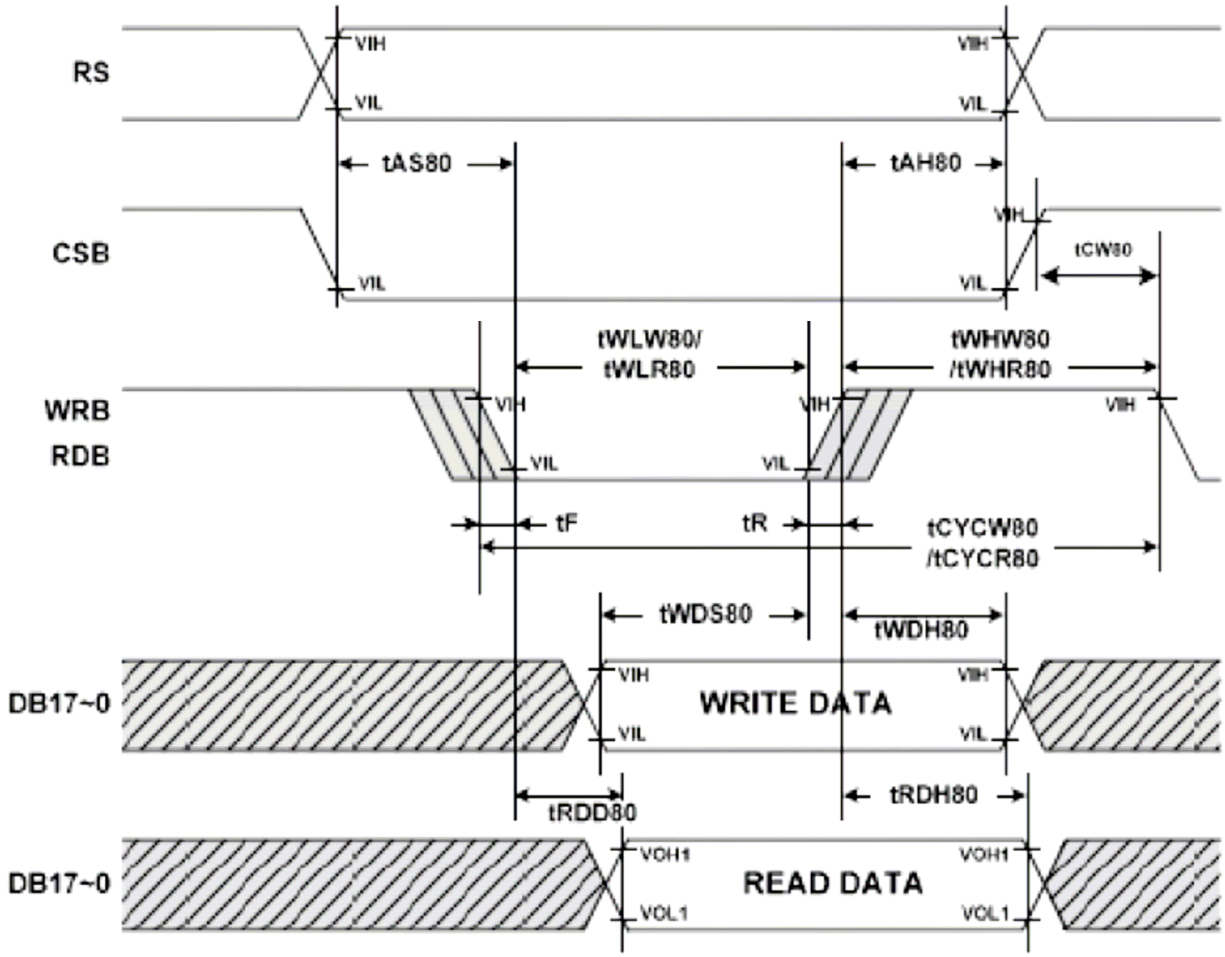


Note : tWHW68 and tWHR68 are determined by the overlap period of low CSB and high E

CPU interface M80

(VDD = 1.5V, VDD3 = 1.65 to 3.3V, TA = -40 to +85°C)

Characteristic		Symbol	Specification		Unit
			Min.	Max.	
Cycle time	Write	tCYCW80	85	-	ns
	Read	tCYCR80	500	-	ns
Pulse rise / fall time		tR, tF	-	15	ns
Pulse width low	Write	tWLW80	27.5	-	ns
	Read	tWLR80	250	-	ns
Pulse width high	Write	tWHW80	27.5	-	ns
	Read	tWHR80	250	-	ns
RS to CSB, WRB(RDB) setup time		tAS80	10	-	ns
RS to CSB, WRB(RDB) hold time		tAH80	2	-	ns
CSB to WRB(RDB) time		tCW80	15	-	ns
Write data setup time		tWDS80	40	-	ns
Write data hold time		tWDH80	15	-	ns
Read data delay time		tRDD80	-	200	ns
Read data hold time		tRDH80	5	-	ns



Note : tWLW80 and tWLR80 are determined by the overlap period of low CSB and low WRB or low CSB and low RDB

Image Data format for 18bit CPU interface (262k color)

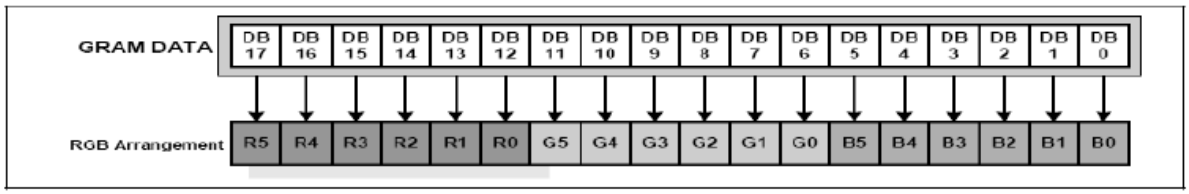


Image Data format for 16bit CPU interface (65k color)

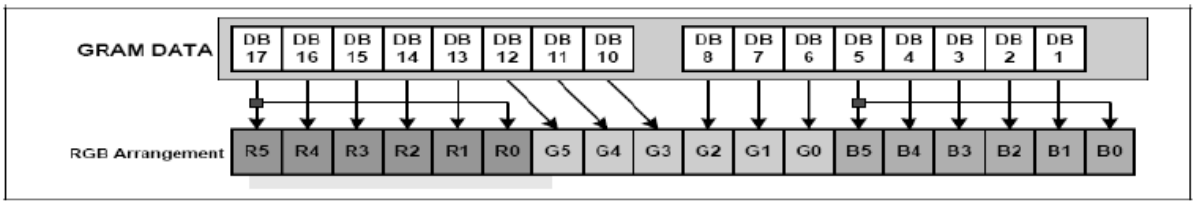


Image Data format for 9bit CPU interface (262k color)

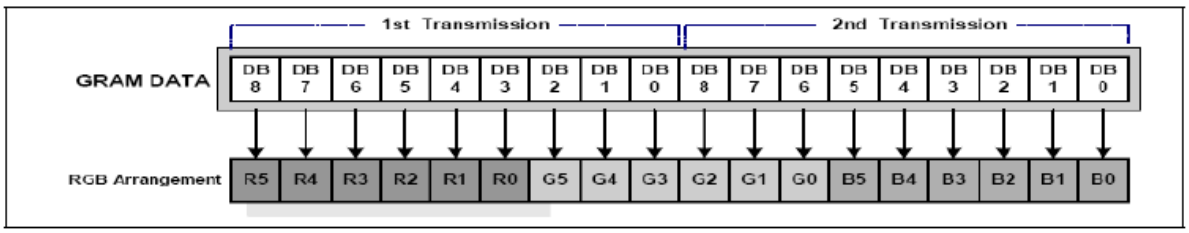
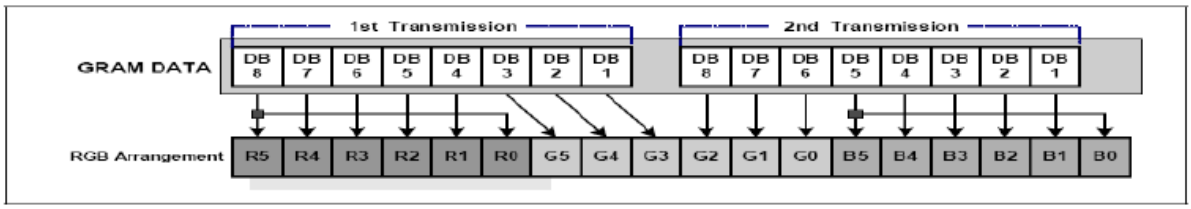


Image Data format for 8bit CPU interface (65K color)

Case 1:



Case 2:

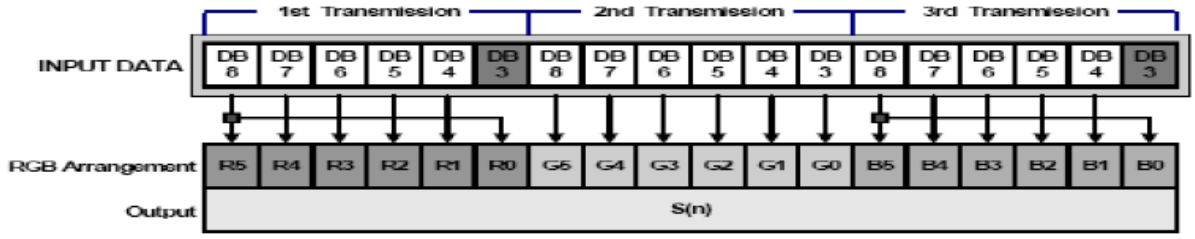
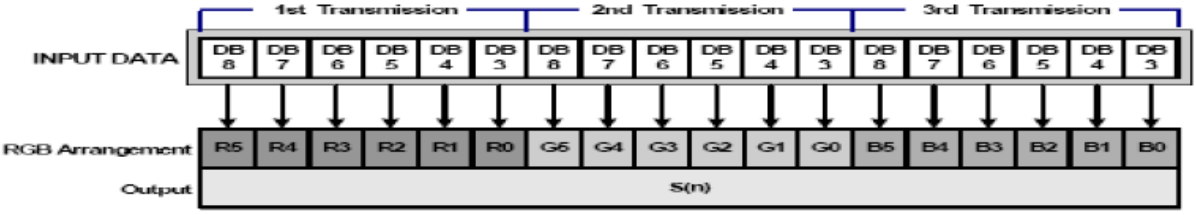


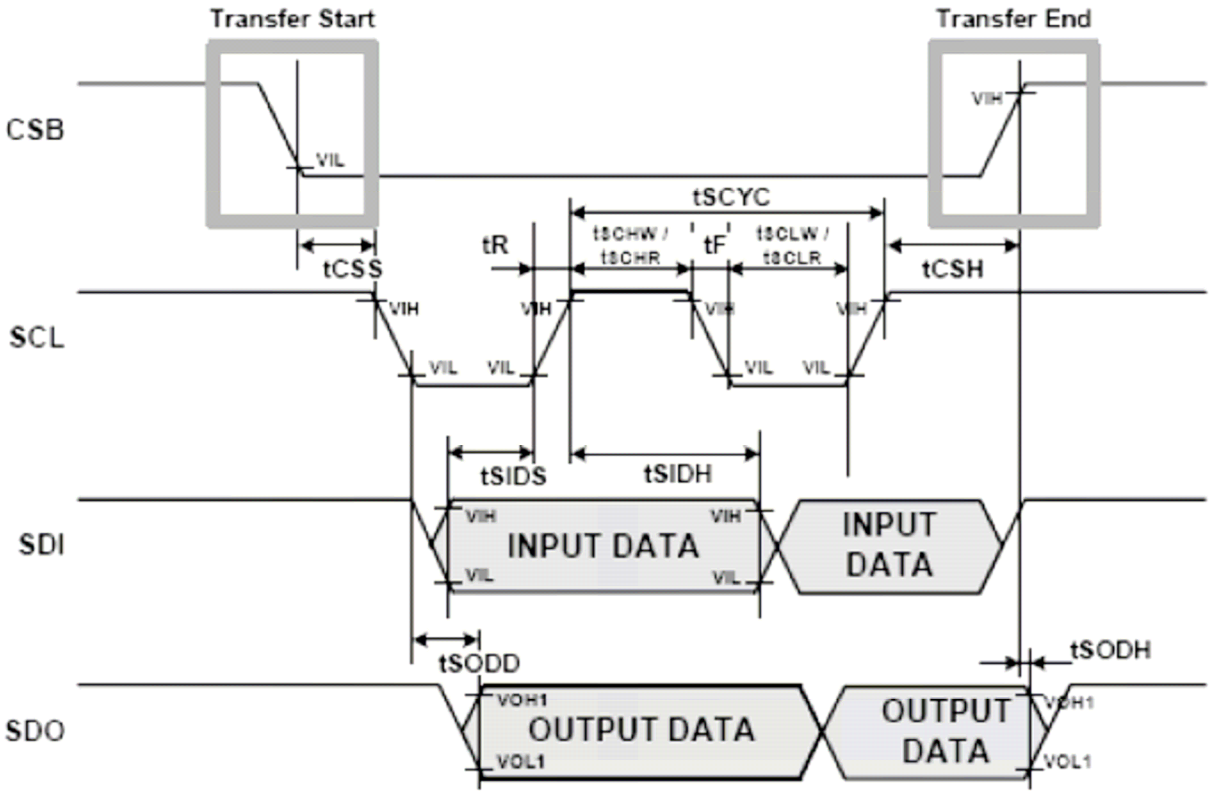
Image Data format for 8bit CPU interface (262K color)

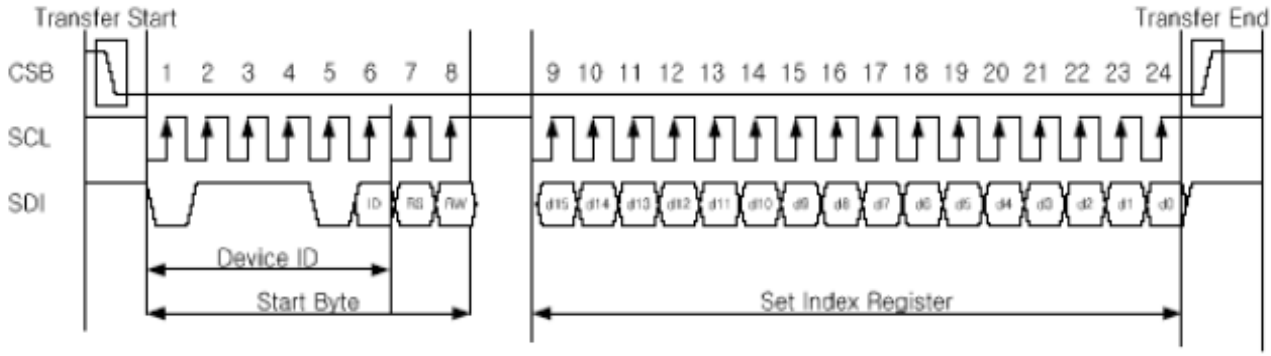


SPI Interface

(VDD = 1.5V, VDD3 = 1.65 to 3.3V, TA = -40 to +85°C)

Characteristic	Symbol	Specification		Unit
		Min.	Max.	
Serial clock write cycle time	tSCYC	130	-	ns
Serial clock read cycle time	tSCYC	250	-	ns
Serial clock rise / fall time	tR, tF	-	15	ns
Pulse width high for write	tSCHW	50	-	ns
Pulse width high for read	tSCHR	110	-	ns
Pulse width low for write	tSCLW	50	-	ns
Pulse width low for read	tSCLR	110	-	ns
Chip select setup time	tCSS	20	-	ns
Chip select hold time	tCSH	60	-	ns
Serial input data setup time	tSIDS	30	-	ns
Serial input data hold time	tSIDH	30	-	ns
Serial output data delay time	tSODD	-	130	ns
Serial output data hold time	tSODH	5	-	ns





(Note) RS="0" : Index data

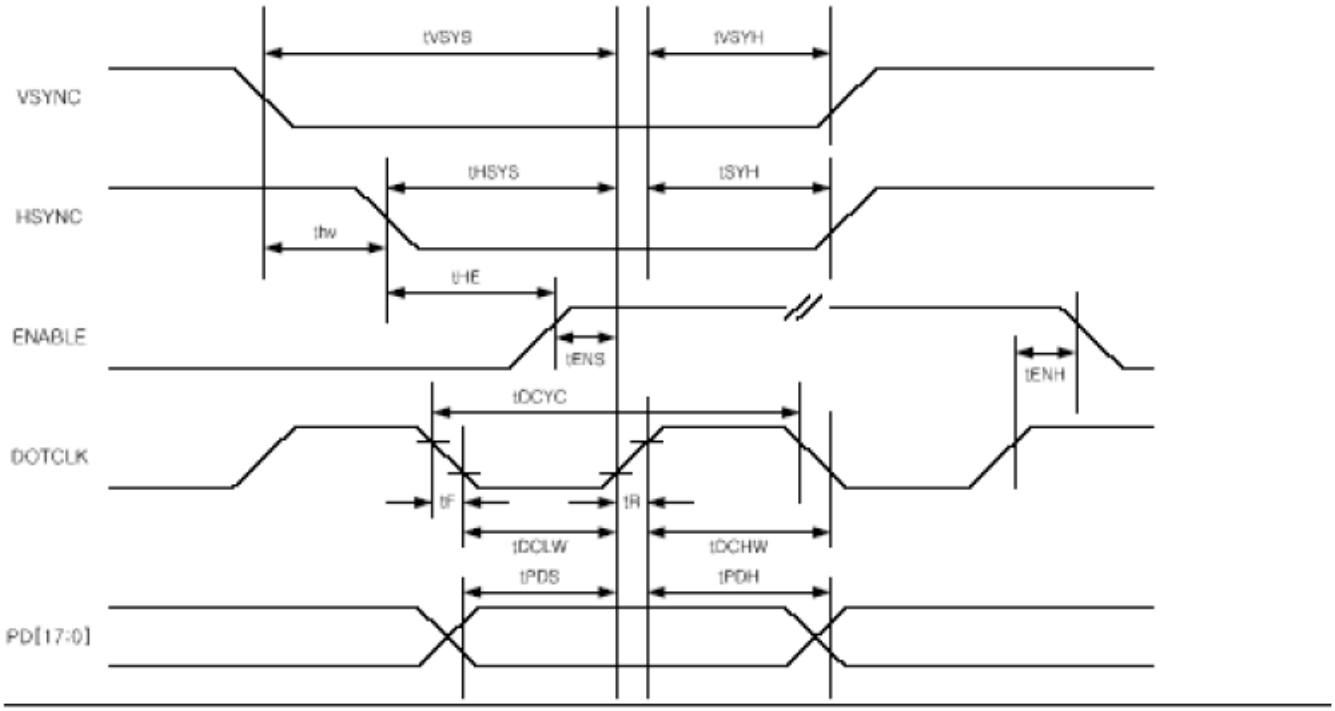
RS="1" : Instruction data

RGB Interface

(VDD = 1.5V, VDD3 = 1.65 to 3.3V, TA = -40 to +85°C)

Characteristic	Symbol	Specification		Unit		Unit
		Min.	Max.	Min.	Max.	
DOTCLK cycle time	tDCYC	100	-	55	-	ns
DOTCLK rise / fall time	tR, tF	-	15	-	15	ns
DOTCLK pulse width high	tDCHW	40	-	25	-	ns
DOTCLK pulse width low	tDCLW	40	-	25	-	ns
Vertical sync setup time	tVSYS	30	-	30	-	ns
Vertical sync hold time	tVSYH	30	-	30	-	ns
Horizontal sync setup time	tHSYS	30		30		ns
Horizontal sync hold time	tHSYH	30		30		ns
ENABLE setup time	tENS	30	-	30	-	ns
ENABLE hold time	tENH	20	-	20	-	ns
PD data setup time	tPDS	30	-	30	-	ns
PD data hold time	tPDH	20	-	20	-	ns
HSYNC-ENABLE time	tHE	1	HBP	1	HBP	tDCYC
VSYNC-HSYNC time	tHV	1	175	1	527	tDCYC

Note
1. HBP is horizontal back-porch.



(When VSPL=0, HSPL=0, DPL=0, EPL=1)

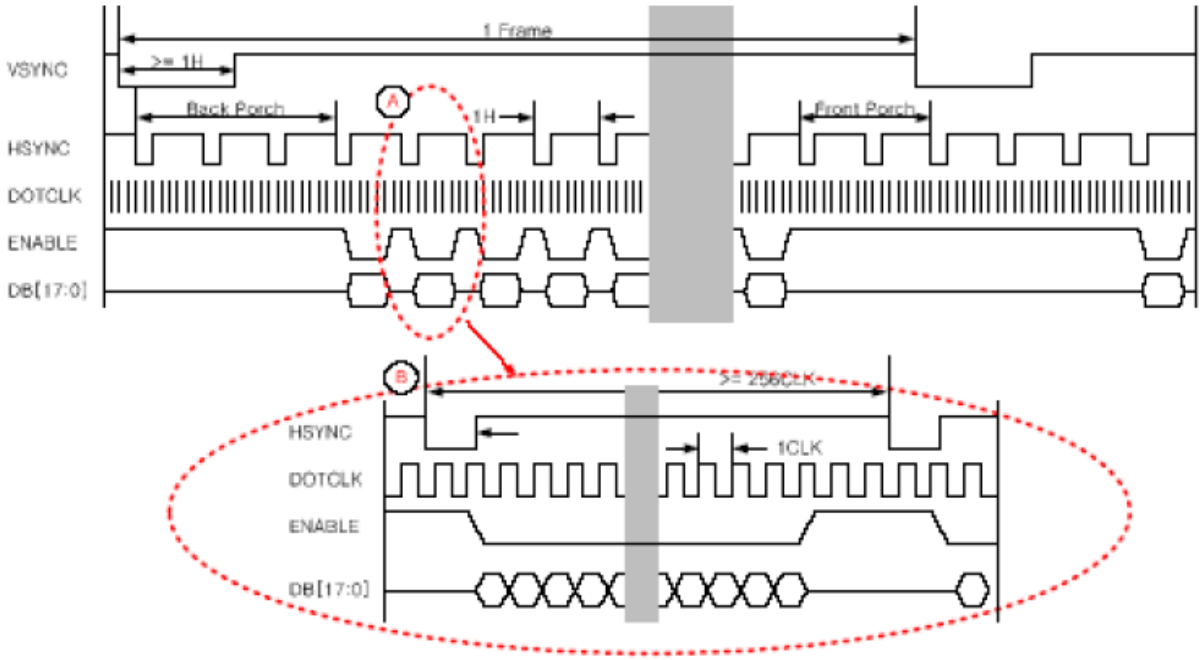


Image Data format for 18bit RGB interface (262k color)

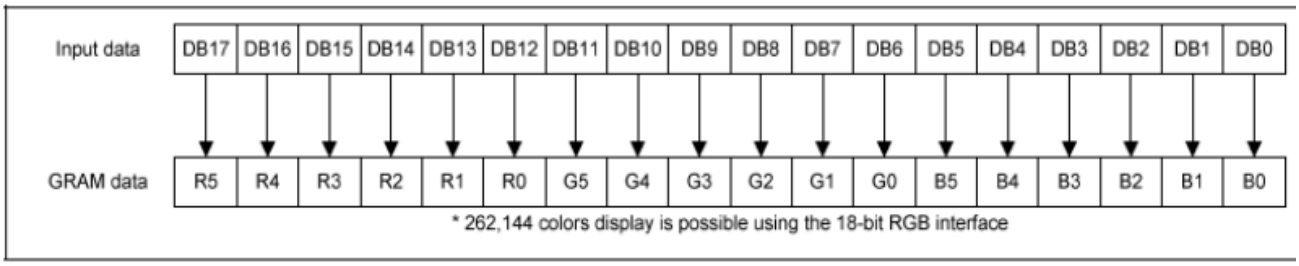


Image Data format for 16bit RGB interface (65k color)

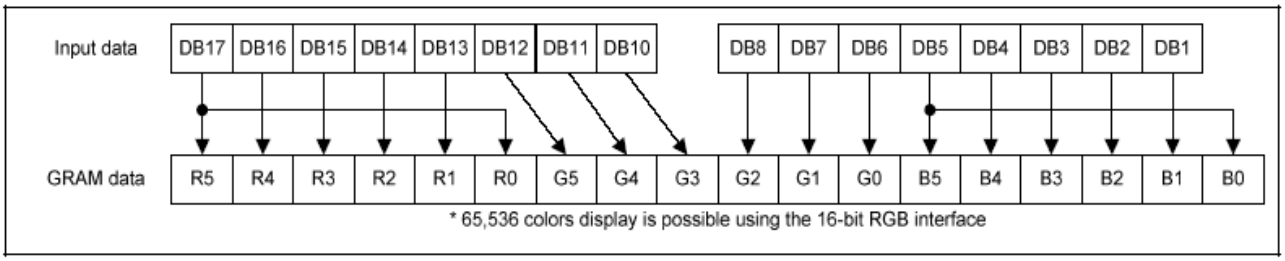
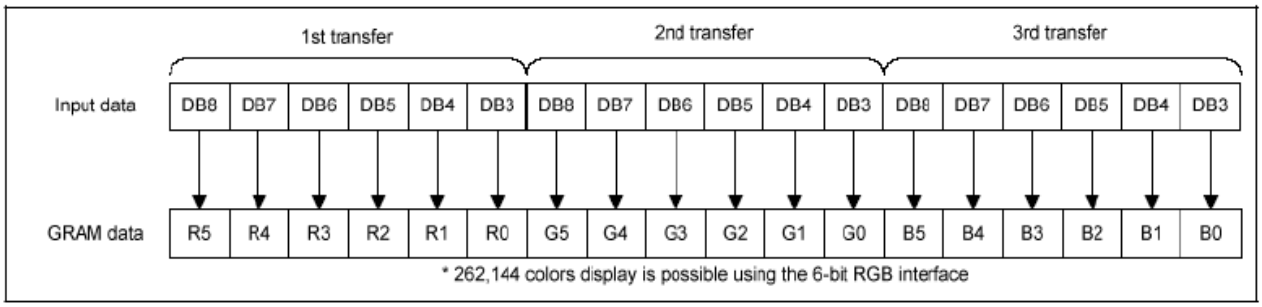


Image Data format for 6bit RGB interface (262k color)



3. OPTICAL CHARACTERISTICS

3.1 Characteristics

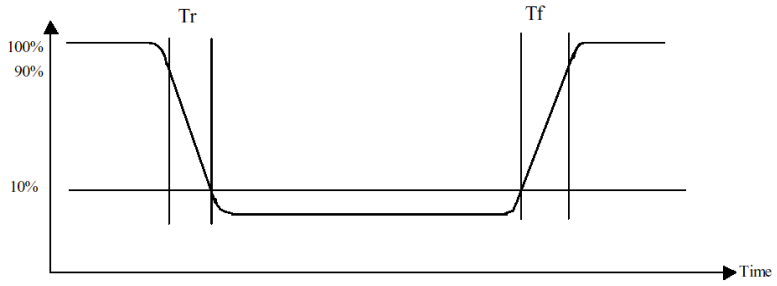
Electrical and Optical Characteristics

No.	Item	symbol / temp.	Min.	Typ.	Max.	Unit	Note
1	Response Time	Tres	-	-	50	us	-
2	Viewing Angle		VA	160	170	degree	-
3	Contrast	Cr	5000:1	10000:1	-	-	-
4	Operating Luminance	L	170	200	230	cd/m^2	

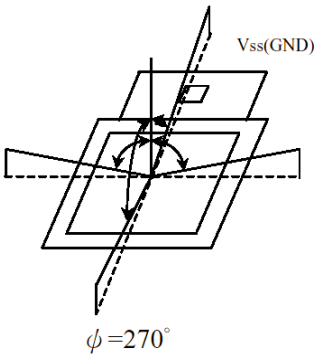
3.2 Definition of optical characteristics

Measurement condition :

[Note 1] Definition of Response Time



[Note 2] Definition of Viewing Angle :



Viewing Angle= CR>10

[Note 3] Definition of Contrast Ratio :

$$CR = \frac{\text{Luminance with all pixels white}}{\text{Luminance with all pixels black}}$$

4. RELIABILITY :

Item No	Items	Condition
1	High temperature operating	60 ℃ , 200 hours
2	Low temperature operating	-20 ℃ , 200 hours
3	High temperature storage	80 ℃ , 200 hours
4	Low temperature storage	-30 ℃ , 200 hours
5	High temperature & humidity storage	60℃, 90%RH, 100 hours
6	Thermal Shock storage	-30℃, 30min.<=> 80℃, 30min. 10 Cycles
7	Vibration test	10 => 55 =>10 => 55 => 10 Hz , within 1 minute Amplitude : 1.5mm. 15 minutes for each Direction (X,Y,Z)
8	Drop test	Packed, 100CM free fall, 6 sides, 1 corner, 3edges
9	Life time	50,000 hours 25℃ , 70%RH below , specification condition driving

* One single product test for only one item.

* Judgment after test : keep in room temperature for more than 2 hours.

- Current consumption < 2 times of initial value
- Contrast > 1/2 initial value
- Function : work normally

5. PRODUCT HANDLING AND APPLICATION

☐ PRECAUTION FOR HANDLING OLED MODULE

- The LCD module contains a C-MOS LSI. People who operate the OLED module should wear ESD protection eguipement to prevent ESD hurt on products.
- Do not input any signal before power is turned on.
- Do not take OLED module from its packaging bag until it is assembled.
- Peel off the OLED module protective film slowly since static electricity may be generated.
- Pay attention to the humidity of the work shop, 50~60%RH is satisfactory.
- Use a non-leak iron for soldering OLED module.
- Do not touch the display surface or connection terminals area with bare hands.Smudges on the display surface reduce the insulation between terminals.
- Cautions for soldering to OLED module:

  Condition for soldering I/O terminals:
  Temperature at iron tip :280℃±10℃.
  Soldering time : 3~4sec./ terminals.
  Type of solder : Eutectic solder(rosin flux filled).

☐ PRECAUTION FOR STORING OLED MODULE

- To avoid degradation of the device , do not store the module under the conditions of direct sunlight , high temperature or high humidity . Keep the module in bags designed to prevent static electricity charging under low temperature / normal humidity conditions(avoid high temperature / high humidity and low temperature below 0℃)

☐ USING ON MEDICAL CARE , SAFETY OR HAZARDOUS APPLICATION OR SYSTEM

- For the application in medical care, safety and hazardous prodcuts or systems, an authorization from URT is required. URT will not responsible for any damage or loss which caused by the products without any authorization given by URT.
- This product is not allowed to be designed and used for military application and/or purpose.
- The delivery of this product to the countries and/or regions where the embargoes are imposed by U.N. is prohibited.
- The application and delivery of this product must comply with Startegic High-Tech Commodities (SHTC) export control and the sales to the embargoed and/or sanctioned countries or regions are strictly prohibited.

6. DATE CODE OF PRODUCTS

- Date code will be shown on each product :

- **Y MM DD - XXX**

  Year Month Day - Production lots

- Example: 2 1 2 2 3 - 0 0 3 ==>Year 2002, Dec.,23rd , Batch no.03

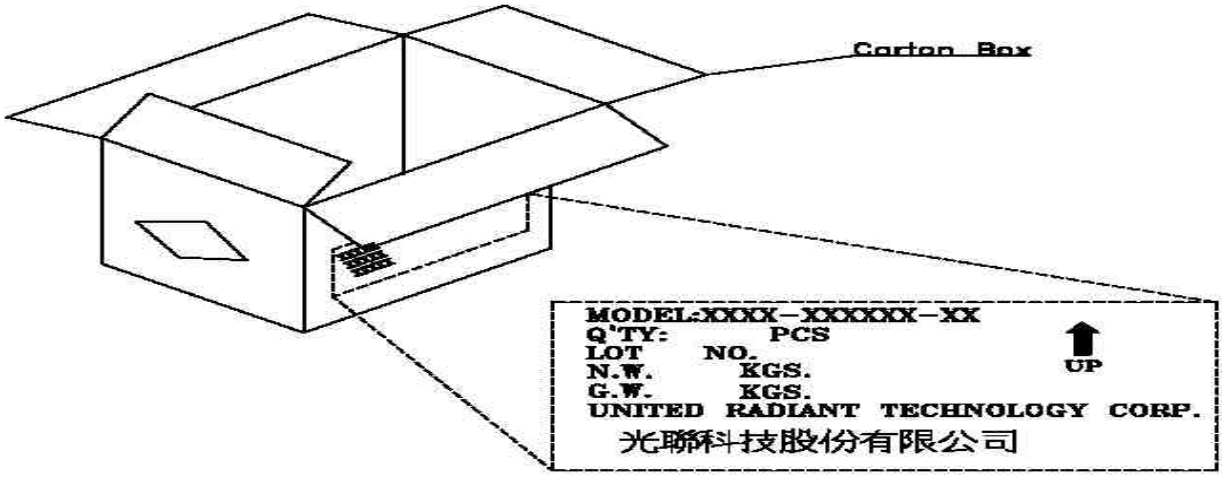
7. PACKING

Instruction of lot number:

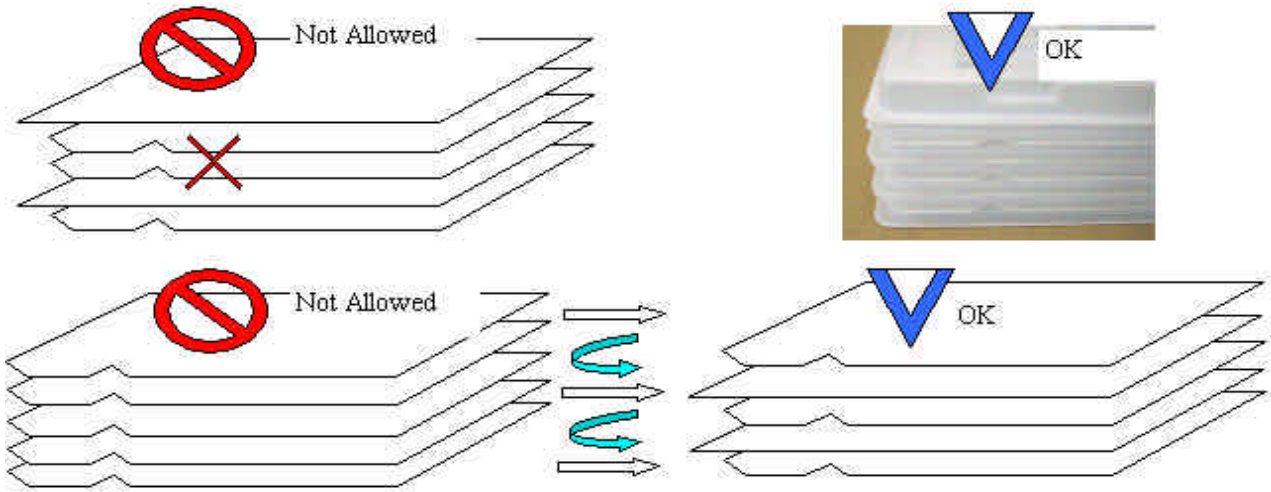
LOT NO. : 0 0 0 8 3 5 2 5 (EX)

- Date: 01—1 st, 02—2 ed, ... 31—31 th
- Week: 1 ——— 6
- Week of Month: 1 ——— 5
- Month: 01—January, 02—February, ... 12—December
- Year: 00—2000, 01—2001

Lable of carton:



Packing tray must be stacked with alternated direction to each others.
To tacks packing trays in same direction will cause product damaged.



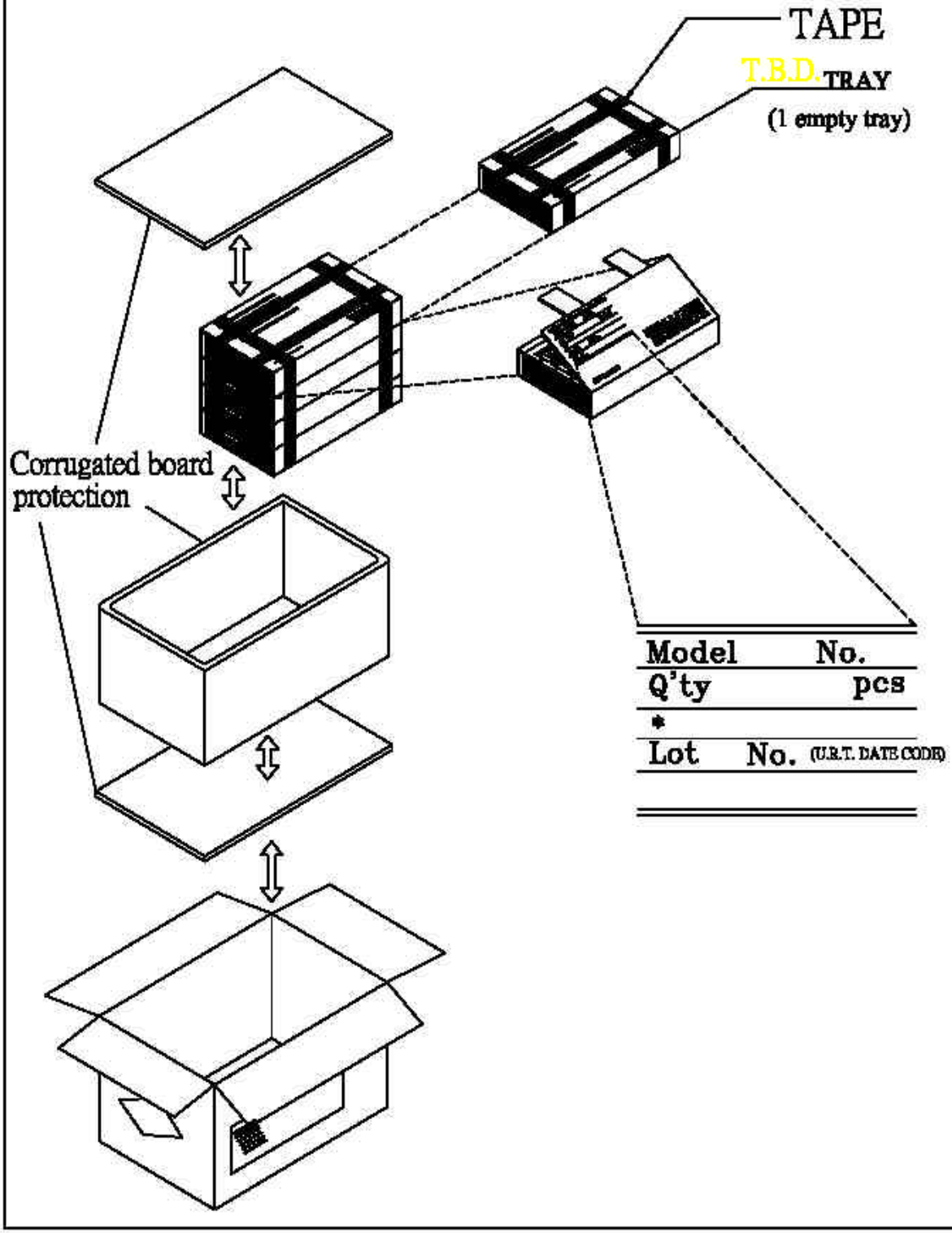
MODEL NO: UM*

T.B.D. pcs / Tray
T.B.D. Tray / Box
T.B.D. Box / Carton
T.B.D. pcs / Carton

NOTE:

(1)Be warned ,the direction of the tray has to turn it by 180 degree before stack it up.Otherwise, it will be packager's responsibility!!

(2)Safe Stack : 5 cartons only



8. INSPECTION STANDARD

8.1. QUALITY :

THE QUALITY OF GOODS SUPPLIED TO PURCHASER SHALL COME UP TO THE FOLLOWING STANDARD.

8.1.1. THE METHOD OF PRESERVING GOODS

AFTER DELIVERY OF GOODS FROM U.R.T. TO PURCHASER. PURCHASER SHALL CONTROL THE LCM AT -10 ℃ ～ 40 ℃ ,AND IT MIGHT BE DESIRABLE TO KEEP AT THE NORMAL ROOM TEMPERATURE AND HUMIDITY UNTIL INCOMING INSPECTION OR THROWING INTO PROCESS LINE.

8.1.2. INCOMING INSPECTION

(A) THE METHOD OF INSPECTION

IF PURCHASER MAKE AN INCOMING INSPECTION , A SAMPLING PLAN SHALL BE APPLIED ON THE CONDITION THAT QUALITY OF ONE DELIVERY SHALL BE REGARDED AS ONE LOT.

(B) THE STANDARD OF QUALITY

ISO-2859-1 (or MIL-STD-105E) , LEVEL Ⅱ SINGLE PLAN.

CLASS	AQL(%)
CRITICAL	0.4 %
MAJOR	0.65 %
MINOR	1.5 %
TOTAL	1.5 %

EVERY ITEM SHALL BE INSPECTED ACCORDING TO THE CLASS.

(C) MEASURE

IF AS THE RESULT OF ABOVE RECEIVING INSPECTION , A LOT OUT IS DISCOVERED. PURCHASER SHALL BE INFORM SELLER OF IT WITHIN SEVEN DAYS. BUT FIRST SHIPMENT WITHIN FOURTEEN DAYS.

8.1.3. WARRANTY POLICY

U.R.T. WILL PROVIDE ONE-YEAR WARRANTY FOR THE PRODUCTS ONLY IF UNDER SPECIFICATION OPERATING CONDITIONS. U.R.T. WILL REPLACE NEW PRODUCTS FOR THESE DEFECT PRODUCTS WHICH UNDER WARRANTY PERIOD AND BELONG TO THE RESPONSIBILITY OF U.R.T.

8.2. CHECKING CONDITION

8.2.1. CHECKING DIRECTION SHALL BE IN THE 45 DEGREE AREA TO FACE THE SAMPLE.

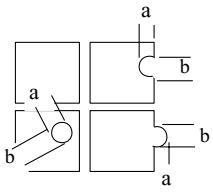
8.2.2. CHECKER SHALL SEE OVER 30 cm. WITH BARE EYES FAR FROM SAMPLE AND USING 2 PCS. OF 20W FLUORESCENT LAMP.

8.3. INSPECTION PLAN :

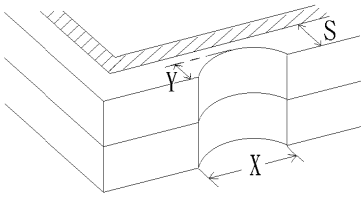
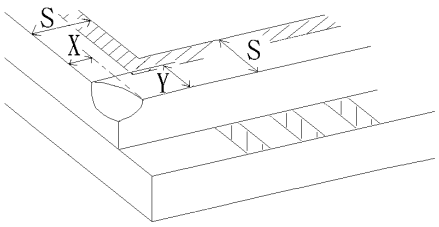
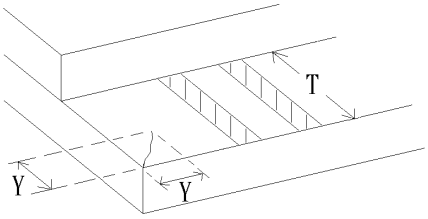
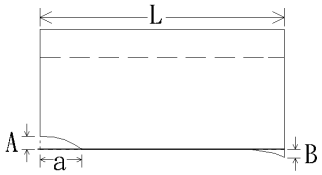
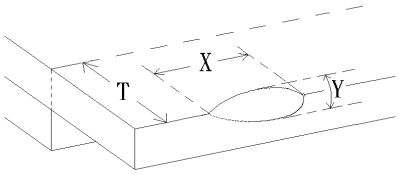
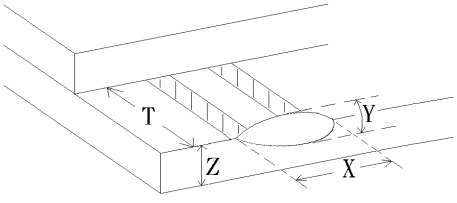
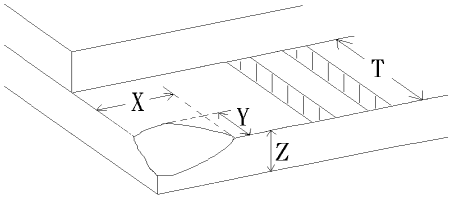
CLASS	ITEM	JUDGEMENT	CLASS
PACKING & INDICATE	1. OUTSIDE AND INSIDE PACKAGE	"MODEL NO." , "LOT NO." AND "QUANTITY" SHOULD INDICATE ON THE PACKAGE.	Minor
	2. MODEL MIXED AND QUANTITY	OTHER MODEL MIXED.....REJECTED QUANTITY SHORT OR OVER.....REJECTED	Critical
	3. PRODUCT INDICATION	"MODEL NO." SHOULD INDICATE ON THE PRODUCT	Major
ASSEMBLY	4. DIMENSION, LCD GLASS SCRATCH AND SCRIBE DEFECT.	ACCORDING TO SPECIFICATION OR DRAWING.	Major
APPEARANCE	5. VIEWING AREA	POLARIZER EDGE OR LCD'S SEALING LINE IS VISABLE IN THE VIEWING AREA ……..REJECTED	Minor
	6. BLEMISH、BLACK SPOT、 WHITE SPOT IN THE LCD AND LCD GLASS CRACKS	ACCORDING TO STANDARD OF VISUAL INSPECTION (INSIDE VIEWING AREA)	Minor
	7. BLEMISH、BLACK SPOT WHITE SPOT AND SCRATCH ON THE POLARIZER	ACCORDING TO STANDARD OF VISUAL INSPECTION (INSIDE VIEWING AREA)	Minor
	8. BUBBLE IN POLARIZER	ACCORDING TO STANDARD OF VISUAL INSPECTION (INSIDE VIEWING AREA)	Minor
	9. LCD'S RAINBOW COLOR	STRONG DEVIATION COLOR (OR NEWTON RING) OF LCD.....REJECTED. OR ACCORDING TO LIMITED SAMPLE (IF NEEDED, AND INSIDE VIEWING AREA)	Minor
ELECTRICAL	10. ELECTRICAL AND OPTICAL CHARACTERISTICS (CONTRAST、VOP、 CHROMATICITY … ETC)	ACCORDING TO SPECIFICATION OR DRAWING . (INSIDE VIEWING AREA)	Critical
	11.MISSING LINE	MISSING DOT、LINE、CHARACTER ....REJECTED	Critical
	12.SHORT CIRCUIT、 WRONG PATTERN DISPLAY	NON DISPLAY、WRONG PATTERN DISPLAY、CURRENT CONSUMPTION OUT OF SPECIFICATION..... REJECTED	Critical
	13. PIN HOLE、PATTERN DEFORMITY	ACCORDING TO STANDARD OF VISUAL INSPECTION	Minor

8.4. STANDARD OF VISUAL INSPECTION

<table>
<tr><th>NO.</th><th>CLASS</th><th>ITEM</th><th>JUDGEMENT</th></tr>
<tr><td>8.4.1</td><td>MINOR</td><td>· BLEMISH、BLACK SPOT、
WHITE SPOT IN THE LCD.

· BLEMISH、BLACK SPOT、
WHITE SPOT AND SCRATCH
ON THE POLARIZER</td><td>(A) ROUND TYPE: unit : mm.
<table>
<tr><th>DIAMETER (mm.)</th><th>ACCEPTABLE Q'TY</th></tr>
<tr><td>Φ ≦ 0.1</td><td>DISREGARD</td></tr>
<tr><td>0.1 < Φ ≦ 0.2</td><td>2</td></tr>
<tr><td>0.2 < Φ ≦ 0.25</td><td>1</td></tr>
<tr><td>0.25 < Φ</td><td>0</td></tr>
</table>
NOTE: Φ=(LENGTH+WIDTH)/2
(B) LINER TYPE: unit : mm.
<table>
<tr><th>LENGTH</th><th>WIDTH</th><th>ACCEPTABLE Q'TY</th></tr>
<tr><td>------</td><td>W ≦0.03</td><td>DISREGARD</td></tr>
<tr><td>L ≦ 5.0</td><td>0.03 < W ≦0.05</td><td>3</td></tr>
<tr><td>L ≦ 5.0</td><td>0.05 < W ≦0.07</td><td>1</td></tr>
<tr><td>------</td><td>0.07 < W</td><td>FOLLOW ROUND TYPE</td></tr>
</table></td></tr>
<tr><td>8.4.2</td><td>MINOR</td><td>BUBBLE IN POLARIZER</td><td>unit : mm.
<table>
<tr><th>DIAMETER</th><th>ACCEPTABLE Q'TY</th></tr>
<tr><td>Φ ≦0.15</td><td>DISREGARD</td></tr>
<tr><td>0.15 < Φ ≦ 0.5</td><td>2</td></tr>
<tr><td>0.5 < Φ</td><td>0</td></tr>
</table></td></tr>
<tr><td>8.4.3</td><td>MINOR</td><td>PIN HOLE 、
PATTERN DEFORMITY</td><td> 

Φ=(a+b)/2
unit : mm.
<table>
<tr><th>DIAMETER</th><th>ACC. Q'TY</th></tr>
<tr><td>Φ ≦ 0.1</td><td>DISREGARD</td></tr>
<tr><td>0.1 < Φ ≦ 0.25</td><td>3</td></tr>
<tr><td>0.25 < Φ</td><td>0</td></tr>
</table></td></tr>
</table>

NO.	CLASS	ITEM	JUDGEMENT
8.4.4	MINOR	CHIPPING	 Y > S REJ.
8.4.5	MINOR	CHIPPING	 X or Y > S REJ.
8.4.6	MAJOR	GLASS CRACK	 Y > (1/2) T REJ.
8.4.7	MAJOR	SCRIBE DEFECT	 1. a> L/3 , A>1.5mm. REJ. 2. B : ACCORDING TO DIMENSION
8.4.8	MINOR	CHIPPING (ON THE TERMINAL AREA)	 Φ= (x+y)/2 > 2.5 mm REJ.
8.4.9	MINOR	CHIPPING (ON THE TERMINAL SURFACE)	 Y > (1/3) T REJ.
8.4.10	MINOR	CHIPPING	 Y > T REJ.