

RoHS Compliant Product
A suffix of "-C" specifies halogen & lead-free

DESCRIPTION

These miniature surface mount MOSFETs utilize high cell density process. Low $R_{DS(on)}$ assures minimal power loss and conserves energy, making this device ideal for use in power management circuitry. Typical applications are PWMDC-DC converters, power management in portable and battery-powered products such as computers, printers, battery charger, telecommunication power system, and telephones power system.

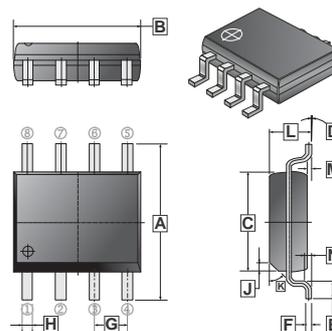
FEATURES

- Low $R_{DS(on)}$ provides higher efficiency and extends battery life.
- Miniature SOP-8 surface mount package saves board space.
- High power and current handling capability.
- Extended V_{GS} range (± 25) for battery pack applications.

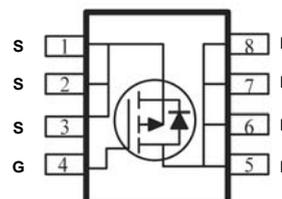
PACKAGE INFORMATION

Package	MPQ	LeaderSize
SOP-8	2.5K	13' inch

SOP-8



REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	5.80	6.20	H	0.35	0.49
B	4.80	5.00	J	0.375 REF.	
C	3.80	4.00	K	45°	
D	0°	8°	L	1.35	1.75
E	0.40	0.90	M	0.10	0.25
F	0.19	0.25	N	0.25 REF.	
G	1.27 TYP.				



MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Ratings	Unit
Drain-Source Voltage	V_{DS}	-30	V
Gate-Source Voltage	V_{GS}	± 25	V
Continuous Drain Current ^a	$I_D @ T_A = 25^\circ\text{C}$	-9.5	A
	$I_D @ T_A = 70^\circ\text{C}$	-8.3	A
Pulsed Drain Current ^b	I_{DM}	± 50	A
Continuous Source Current (Diode Conduction) ¹	I_S	-2.1	A
Total Power Dissipation ¹	$P_D @ T_A = 25^\circ\text{C}$	3.1	W
	$P_D @ T_A = 70^\circ\text{C}$	2.6	W
Operating Junction & Storage Temperature Range	T_J, T_{STG}	-55 ~ 150	$^\circ\text{C}$
Thermal Resistance Ratings			
Thermal Resistance Junction-Case (Max.) ¹	$t \leq 5 \text{ sec}$	$R_{\theta JC}$	25 $^\circ\text{C} / \text{W}$
Thermal Resistance Junction-Ambient (Max.) ¹	$t \leq 10 \text{ sec}$	$R_{\theta JA}$	50 $^\circ\text{C} / \text{W}$

Notes

1. Surface Mounted on 1" x 1" FR4 Board.
2. Pulse width limited by maximum junction temperature.

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Static						
Gate Threshold Voltage	$V_{GS(th)}$	-1	-	-	V	$V_{DS} = V_{GS}, I_D = -250\mu\text{A}$
Gate-Body Leakage	I_{GSS}	-	-	± 100	nA	$V_{DS} = 0\text{V}, V_{GS} = \pm 25\text{V}$
Zero Gate Voltage Drain Current	I_{DSS}	-	-	-1	μA	$V_{DS} = -24\text{V}, V_{GS} = 0\text{V}$
		-	-	-5	μA	$V_{DS} = -24\text{V}, V_{GS} = 0\text{V}, T_J = 55^\circ\text{C}$
On-State Drain Current ¹	$I_{D(on)}$	-50	-	-	A	$V_{DS} = -5\text{V}, V_{GS} = -10\text{V}$
Drain-Source On-Resistance ¹	$R_{DS(ON)}$	-	-	19	m Ω	$V_{GS} = -10\text{V}, I_D = -9.5\text{A}$
		-	-	30		$V_{GS} = -4.5\text{V}, I_D = -7.5\text{A}$
		-	-	29		$V_{GS} = -10\text{V}, I_D = -9.5\text{A}, T_J = 55^\circ\text{C}$
Forward Transconductance ¹	g_{fs}	-	31	-	S	$V_{DS} = -15\text{V}, I_D = -9.5\text{A}$
Diode Forward Voltage	V_{SD}	-	-0.7	-	V	$I_S = -2.1\text{A}, V_{GS} = 0\text{V}$
Dynamic ²						
Total Gate Charge	Q_g	-	15.3	-	nC	$I_D = -9.5\text{A}$ $V_{DS} = -15\text{V}$ $V_{GS} = -4.5\text{V}$
Gate-Source Charge	Q_{gs}	-	5.2	-		
Gate-Drain Charge	Q_{gd}	-	5.8	-		
Switching						
Turn-On Delay Time	$T_{d(on)}$	-	15	-	nS	$V_{DD} = -15\text{V}, I_D = -1\text{A}$ $V_{GEN} = -10\text{V}, R_L = 15\Omega$ $R_G = 6\Omega$
Rise Time	T_r	-	12	-		
Turn-Off Delay Time	$T_{d(off)}$	-	62	-		
Fall Time	T_f	-	46	-		

Notes:

- Pulse test : $PW \leq 300\mu\text{s}$ duty cycle $\leq 2\%$.
- Guaranteed by design, not subject to production testing.

CHARACTERISTIC CURVES

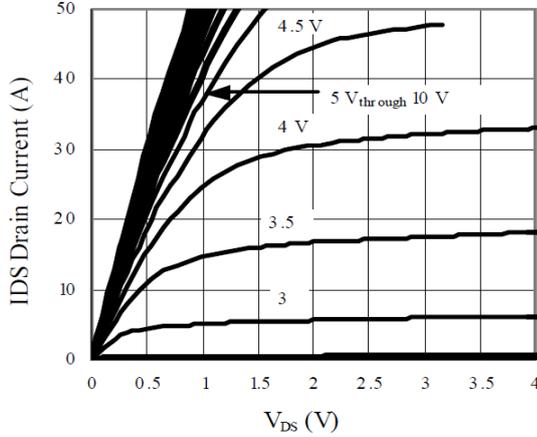


Figure 1. On-Region Characteristics

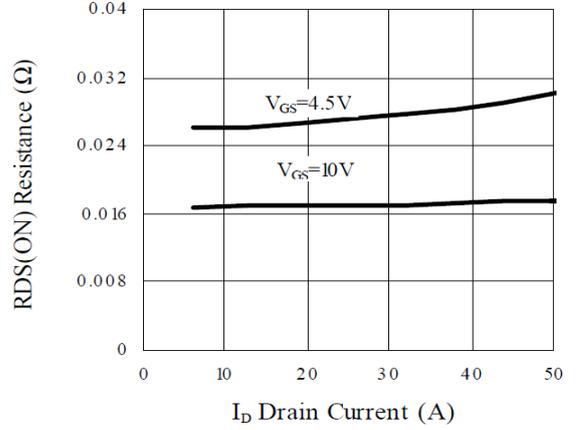


Figure 2. On-Resistance with Drain Current

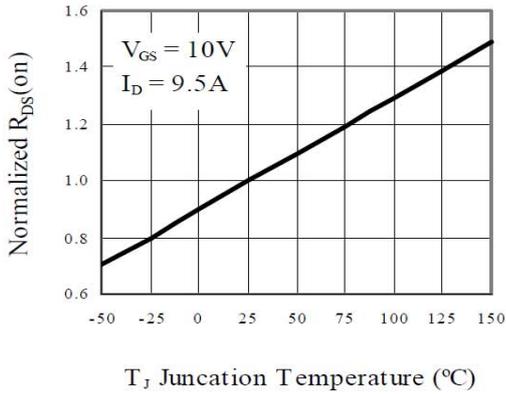


Figure 3. On-Resistance Variation with Temperature

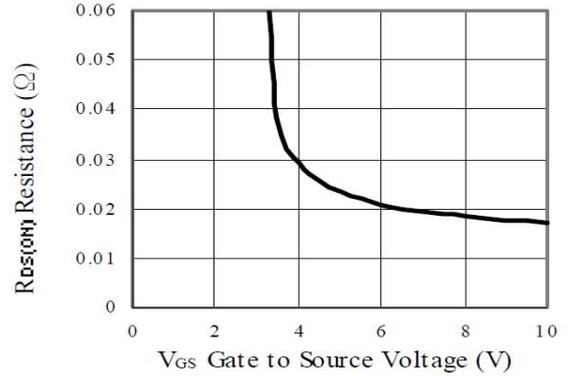


Figure 4. On-Resistance Variation with Gate to Source Voltage

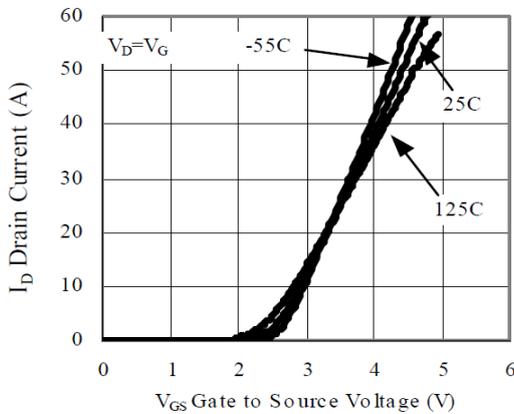


Figure 5. Transfer Characteristics

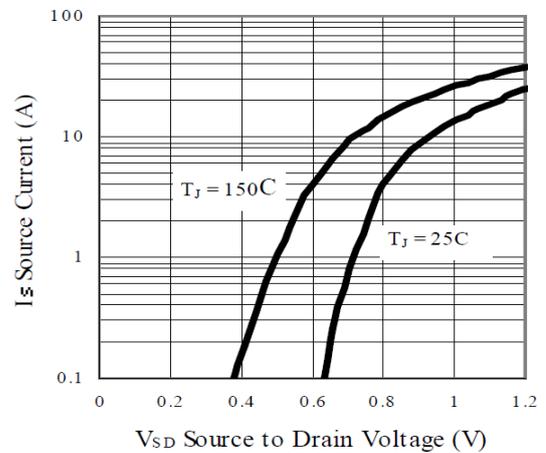


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature

CHARACTERISTIC CURVES

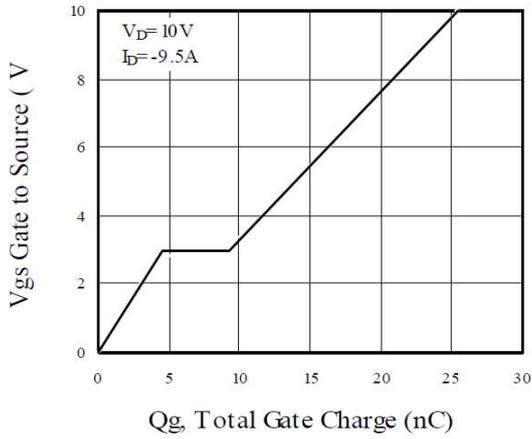


Figure 7. Gate Charge Characteristics

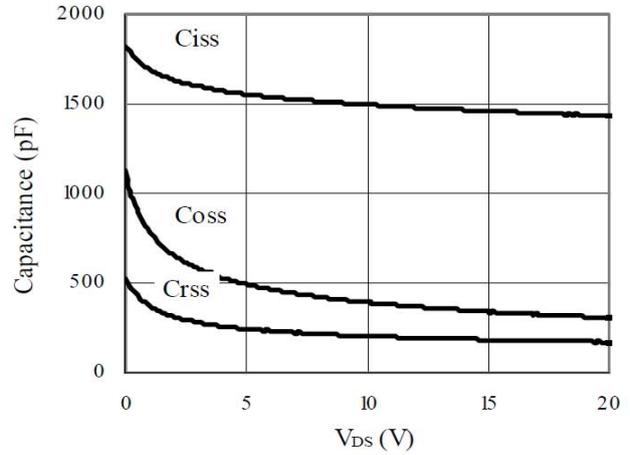


Figure 8. Capacitance Characteristics

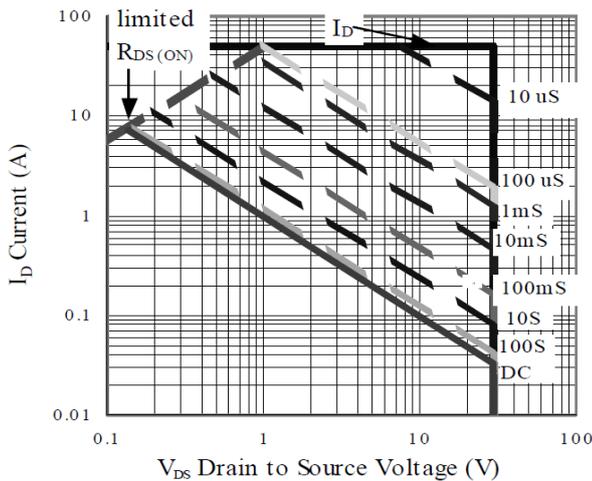


Figure 9. Maximum Safe Operating Area

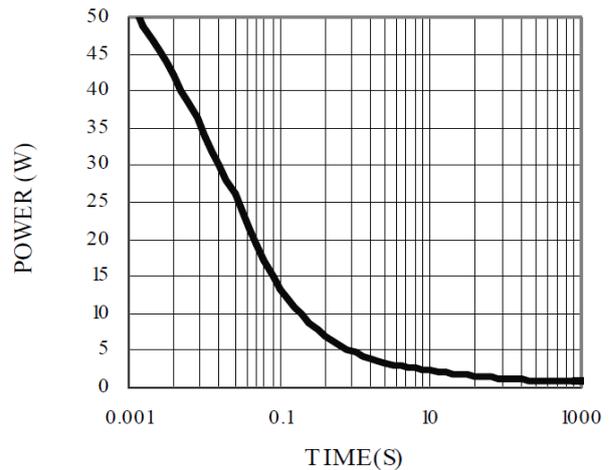


Figure 10. Single Pulse Maximum Power Dissipation

Normalized Thermal Transient Junction to Ambient

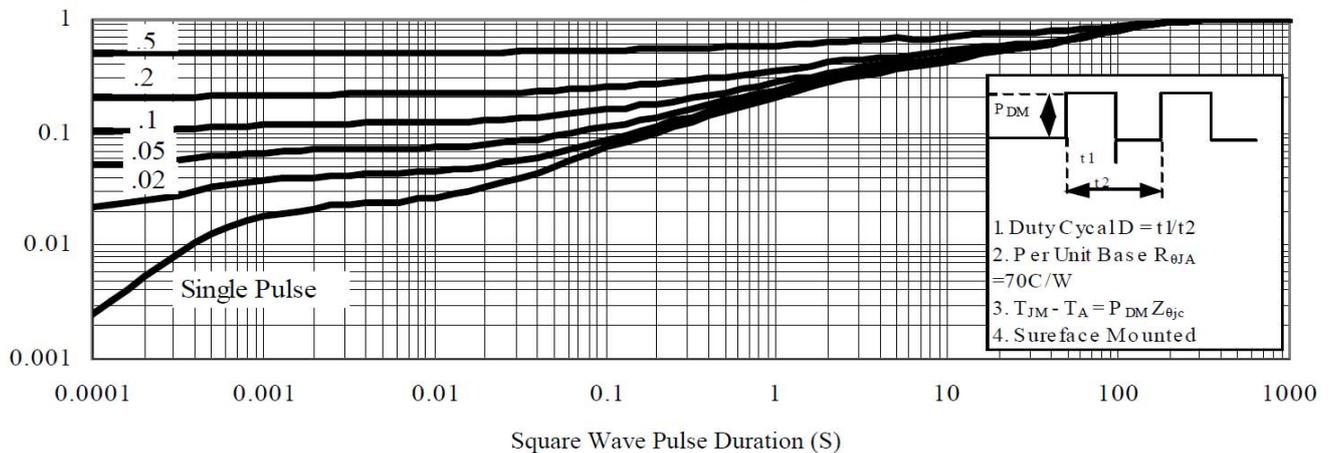


Figure 11. Transient Thermal Response Curve