Never stop thinking

p-Channel Power MOSFET

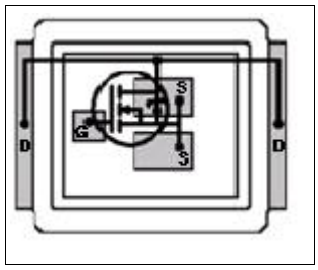
OptiMOS™ P3
BSB027P03LX3 G

Data Sheet

1.9, 2011-03-02
Preliminary

Industrial & Multimarket

1 Description



OptiMOS™ P3 -30V products are class leading power P-Channel MOSFETs for highest power density and energy efficient solutions. Lowest on state resistance in small footprint packages make OptiMOS™ P3 -30V the best choice for the demanding requirements of load switch, high-side switch and battery management applications. OptiMOS™ P3 products are available in high performance packages to tackle your most challenging applications giving full flexibility in optimizing space, efficiency and cost.

Features

- **P-Channel MOSFET**
- Very low on-resistance $R_{DS(on)}$
- Qualified for consumer level application
- Pb-free plating; RoHS compliant
- Halogen-free according to IEC61249-2-21
- Double sided cooling
- Compatible with DirectFET® package MX footprint and outline[1)]
- 100% avalanche tested
- Low parasitic inductance
- Low profile (<0.7 mm)

Applications

- load switch
- high-side switch
- battery management

Table 1 Key Performance Parameters

Parameter	Value	Unit		Related Links
V_{DS}	-30	V		IFX OptiMOS webpage
$R_{DS(on),max}$	2.7	mΩ		IFX OptiMOS product brief
I_D	142	A		IFX OptiMOS spice models
Q_{OSS}	108	nC		IFX Design tools
$Q_{g\cdot typ}$	75			

Type	Package	Marking
BSB027P03LX3 G	MG-WDSON-2	5003

1) DirectFET ® is a trademark of International Rectifier Corporation. BSB027P03LX3 GG uses DirectFET ® technology licensed from International Rectifier Corporation

2 Maximum ratings

at T_j = 25 °C, unless otherwise specified.

Table 2 Maximum ratings

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current	I_D	-	-	142	A	V_{GS}=10 V, T_C=25 °C
				90		V_{GS}=10 V, T_C=100 °C
				27		V_{GS}=10 V, T_A=25 °C, R_{thJA}=45 K/W)[1]
Pulsed drain current[2]	$I_{D,pulse}$	-	-	400		T_C=25 °C
Avalanche current, single pulse[3]	I_{AS}			40		T_C=25 °C
Avalanche energy, single pulse	E_{AS}	-	-	290	mJ	I_D=40 A,R_{GS}=25 Ω
Gate source voltage	V_{GS}	-20	-	20	V	
Power dissipation	P_{tot}	-	-	78	W	T_C=25 °C
				2.8		T_A=25 °C, R_{thJA}=45[1] K/W
Operating and storage temperature	T_j,T_{stg}	-40	-	150	°C	
IEC climatic category; DIN IEC 68-1		55/150/56				

1) Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6cm2 (one layer, 70 µm thick) copper area for drain connection. PCB is vertical in still air

2) See figure 3 for more detailed information

3) See figure 13 for more detailed information

3 Thermal characteristics

Table 3 Thermal characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	R_{thJC}	-	1.0	-	°K/W	bottom
		-	-	1.6		top
Device on PCB	R_{thJA}	-	-	45		6 cm^2 cooling area[1]

1) Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm2 (one layer, 70µm thick) copper area for drain conneciton. PCB is vertical in still air.

4 Electrical characteristics

Electrical characteristics, at Tj=25 °C, unless otherwise specified.

Table 4 Static characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	30	-	-	V	V_{GS}=0 V, I_D=1 mA
Gate threshold voltage	$V_{GS(th)}$	-1	-1.5	-2		V_{DS}=V_{GS}, I_D=250 µA
Zero gate voltage drain current	I_{DSS}	-	0.1	10	µA	V_{DS}=30V, V_{GS}=0 V, T_j=25 °C
		-	10	100		V_{DS}=30 V, V_{GS}=0 V, T_j=125 °C
Gate-source leakage current	I_{GSS}	-	10	100	nA	V_{GS}=20 V, V_{DS}=0 V
Drain-source on-state resistance	$R_{DS(on)}$	-	3.4	4.2	mΩ	V_{GS}=4.5 V, I_D=25A
			2.3	2.7		V_{GS}=10 V, I_D=30A
Gate resistance	R_G	-	2.5	-	Ω	
Transconductance	g_{fs}	55	110		S	|V_{DS}|>2|$I_{D\|RDS(on)max}$, I_D=30 A

Table 5 Dynamic characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	13000	17000	pF	V_{GS}=0 V, V_{DS}=15 V, f=1 MHz
Output capacitance	C_{oss}	-	5800	7700		
Reverse transfer capacitance	C_{rss}	-	380	570		
Turn-on delay time	$t_{d(on)}$	-	27	41	ns	V_{DD}=15V, V_{GS}=10 V, I_D=30 A, R_G= 1.6 Ω
Rise time	t_r	-	11	17		
Turn-off delay time	$t_{d(off)}$	-	80	120		
Fall time	t_f	-	14	21		

Table 6 Gate charge characteristics[1)]

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	Q_{gs}	-	33	44	nC	V_{DD}=15 V, I_D=30 A, V_{GS}=0 to 4.5 V
Gate charge at threshold	$Q_{g(th)}$		19	25		
Gate to drain charge	Q_{gd}	-	17	28		
Switching charge	Q_{sw}	-	31	47		
Gate charge total	Q_g		75	100		
Gate plateau voltage	$V_{plateau}$	-	2.8	-	V	
Gate charge total	Q_g		158	210	nC	V_{DD}=15 V, I_D=30A,V_{GS}=0 to10V
Gate charge total, sync. FET	$Q_{g(sync)}$		65	86		V_{DS}=0.1V, V_{GS}=0 to 4.5V
Output charge	Q_{oss}		108	143		V_{DD}=15 V, V_{GS}=0 V

1) See figure 16 for gate charge parameter definition

Table 7 Reverse diode characteristics

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	I_S			78	A	T_C=25 °C
Diode pulse current	$I_{S,pulse}$			310		
Diode forward voltage	V_{SD}	-	0.8	1.0	V	V_{GS}=0 V, I_F=30 A, T_j=25 °C
Reverse recovery charge	Q_{rr}	-	119	149	nC	V_R=15V, I_F=I_S, di_F/dt=400 A/µs

5 Electrical characteristics diagrams

Table 8

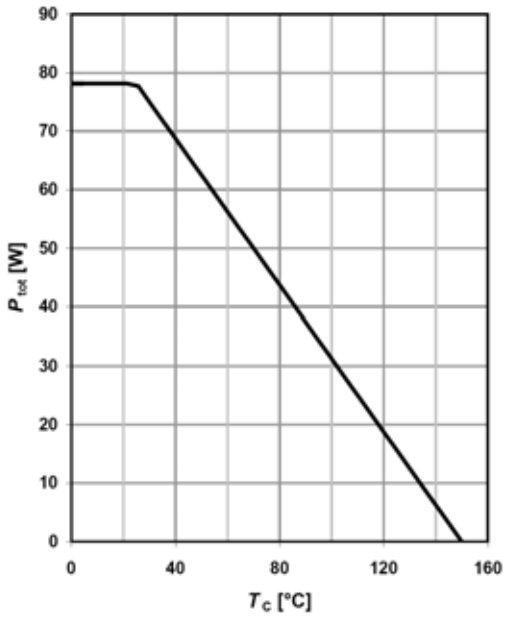
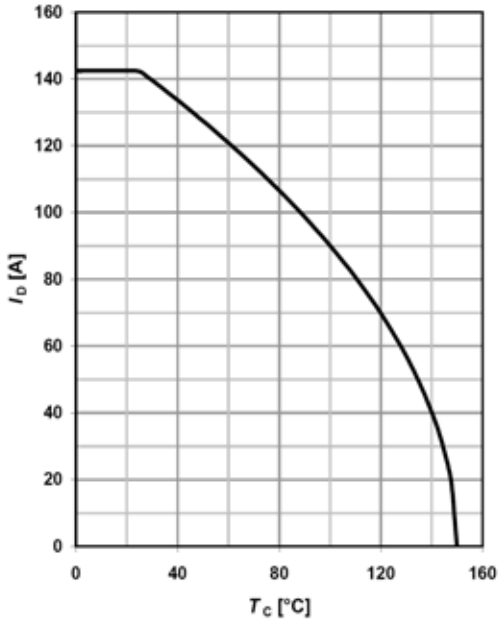
1 Power dissipation	2 Drain current
	
P_{tot} = f(T_C)	I_D=$f(T_C)$; parameter:V_{GS}

Table 9

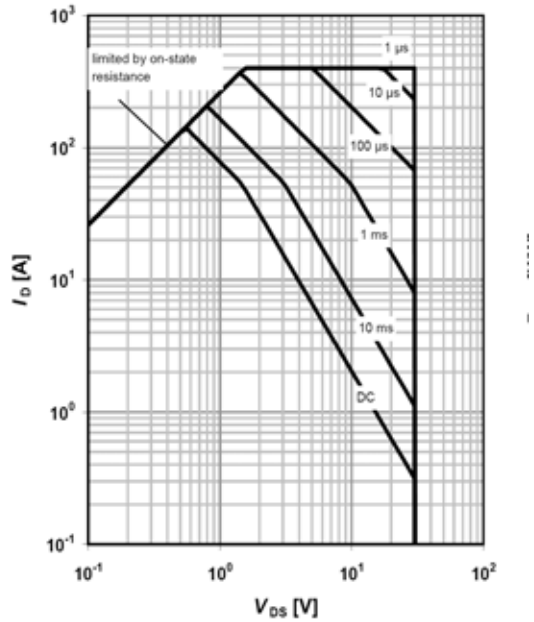
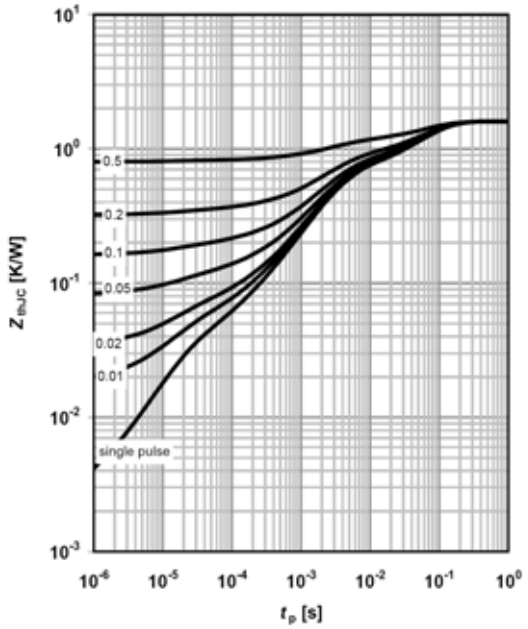
3 Safe operating area T_C=25 °C	4 Max. transient thermal impedance
	
I_D=f(V_{DS}); T_j=25 °C; D=0; parameter: T_p	$Z_{(thJC)}$=f(t_p); parameter: D=t_p/T

Table 10

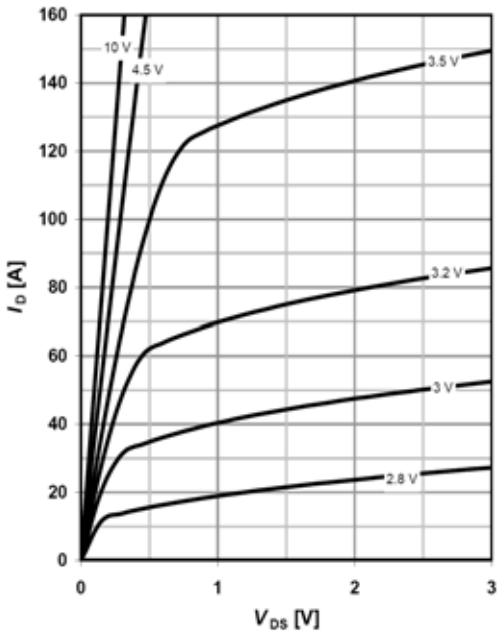
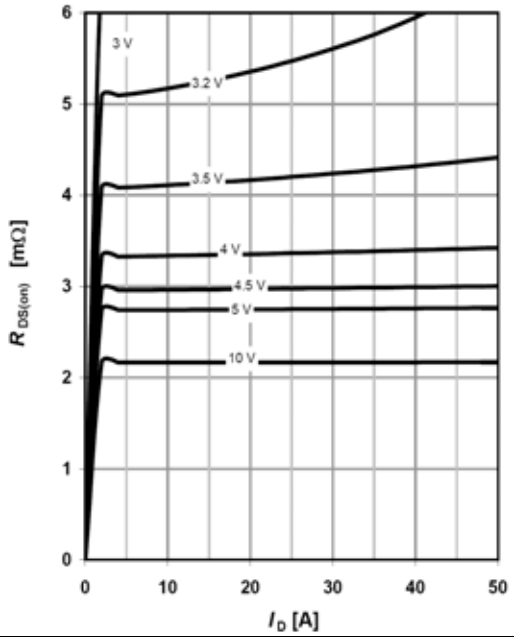
5 Typ. output characteristics T_C=25 °C	6 Typ. drain-source on-state resistance
	
I_D=f(V_{DS}); T_j=25 °C; parameter: V_{GS}	$R_{DS(on)}$=f(I_D); T_j=25 °C; parameter: V_{GS}

Table 11

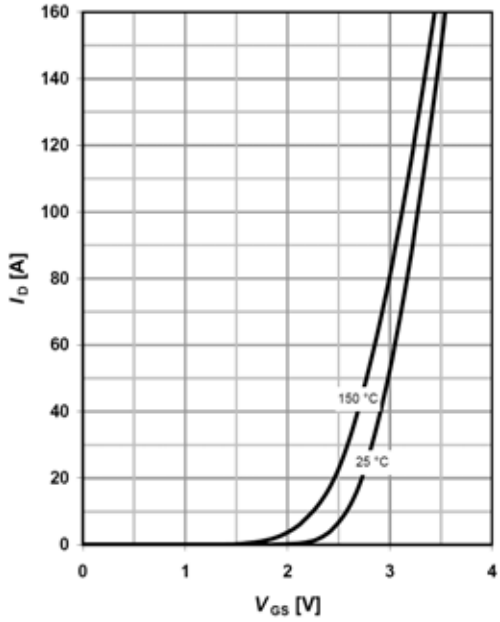
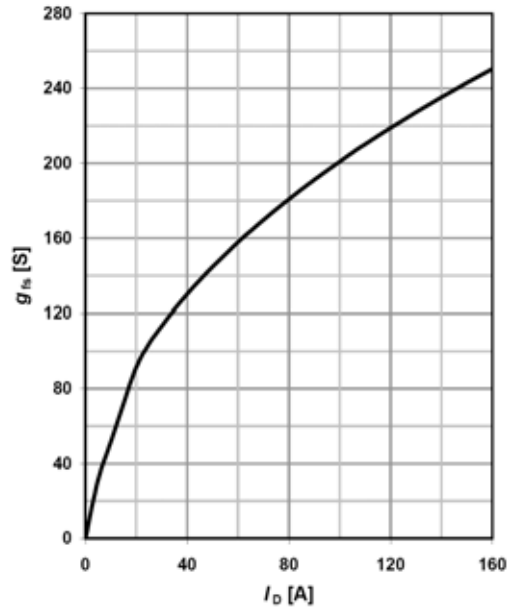
7 Typ. transfer characteristics	8 Typ. forward transconductance
	
I_D=f(VGS); |V_{DS}|>2|I_D|$R_{DS(on)max}$	g_{fs}=f(I_D); T_j=25 °C

Table 12

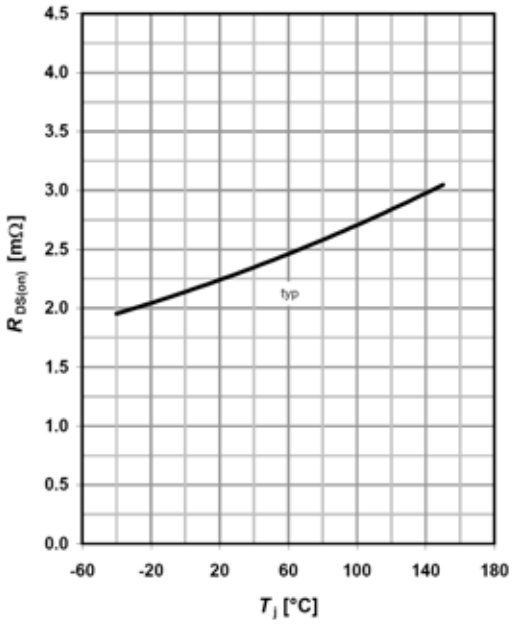
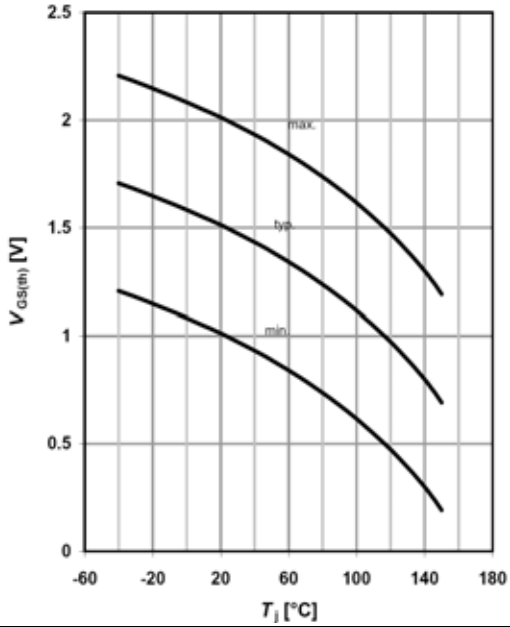
9 Drain-source on-state resistance	10 Typ. gate threshold voltage
	
$R_{DS(on)}=f(T_j)$; I_D=30 A; V_{GS}=10 V	$V_{GS(th)}=f(T_j)$; $V_{GS}=V_{DS}$;I_D=250µA

Table 13

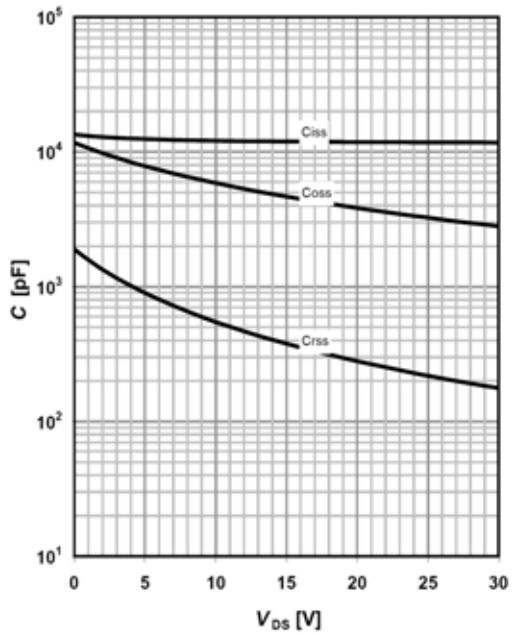
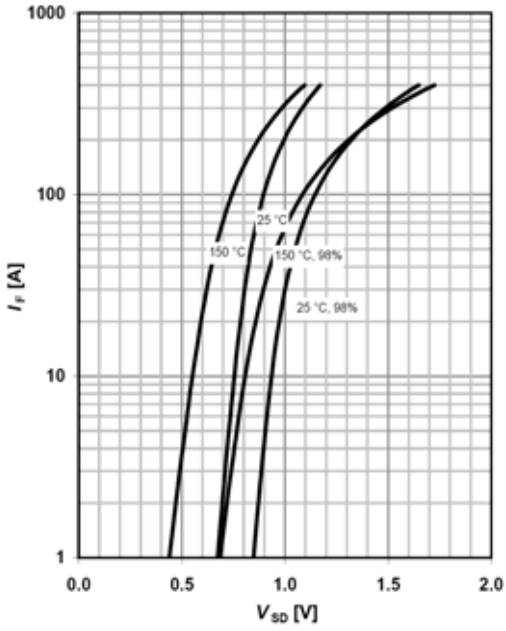
11 Typ. capacitances	12 Forward characteristics of reverse diode
	
C=f(V_{DS}); V_{GS}=0 V; f=1 MHz	$I_F=f(V_{SD})$; parameter: T_j

Table 14

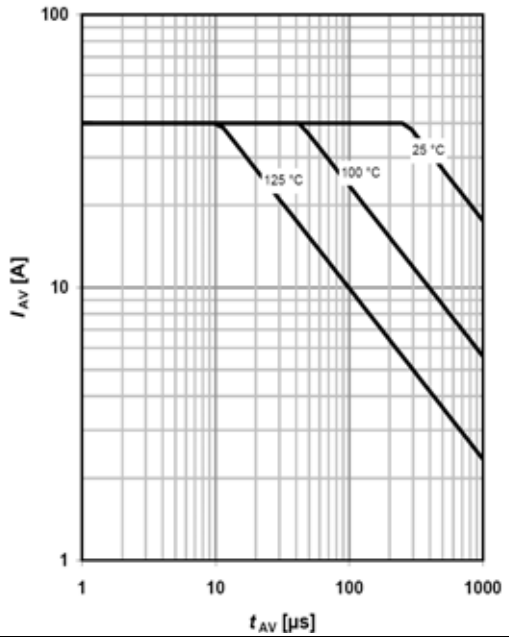
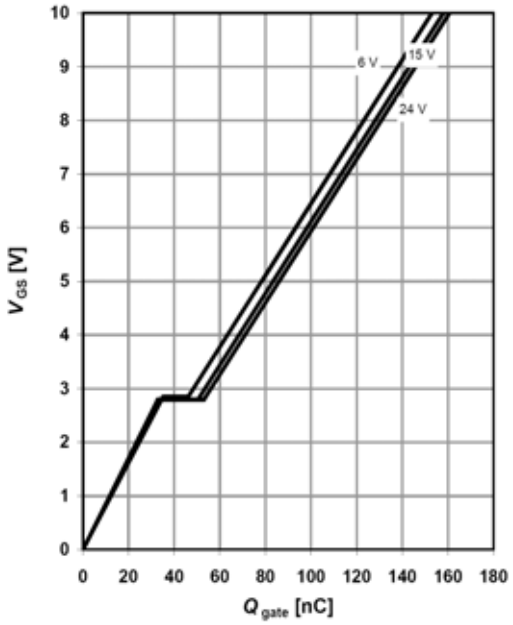
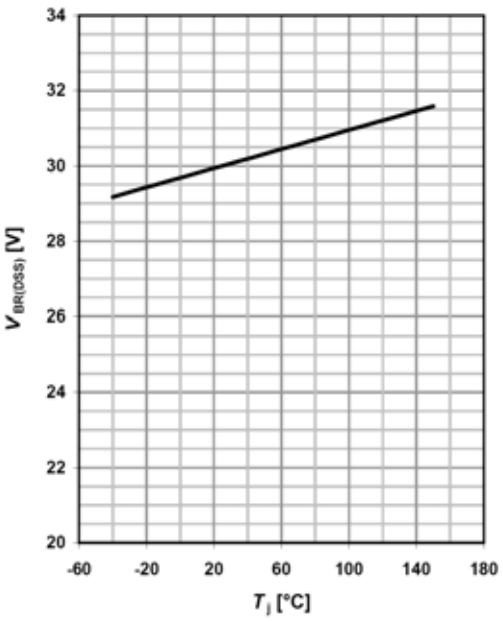
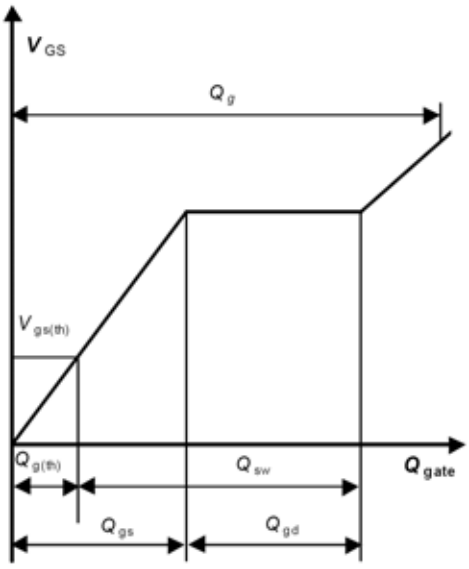
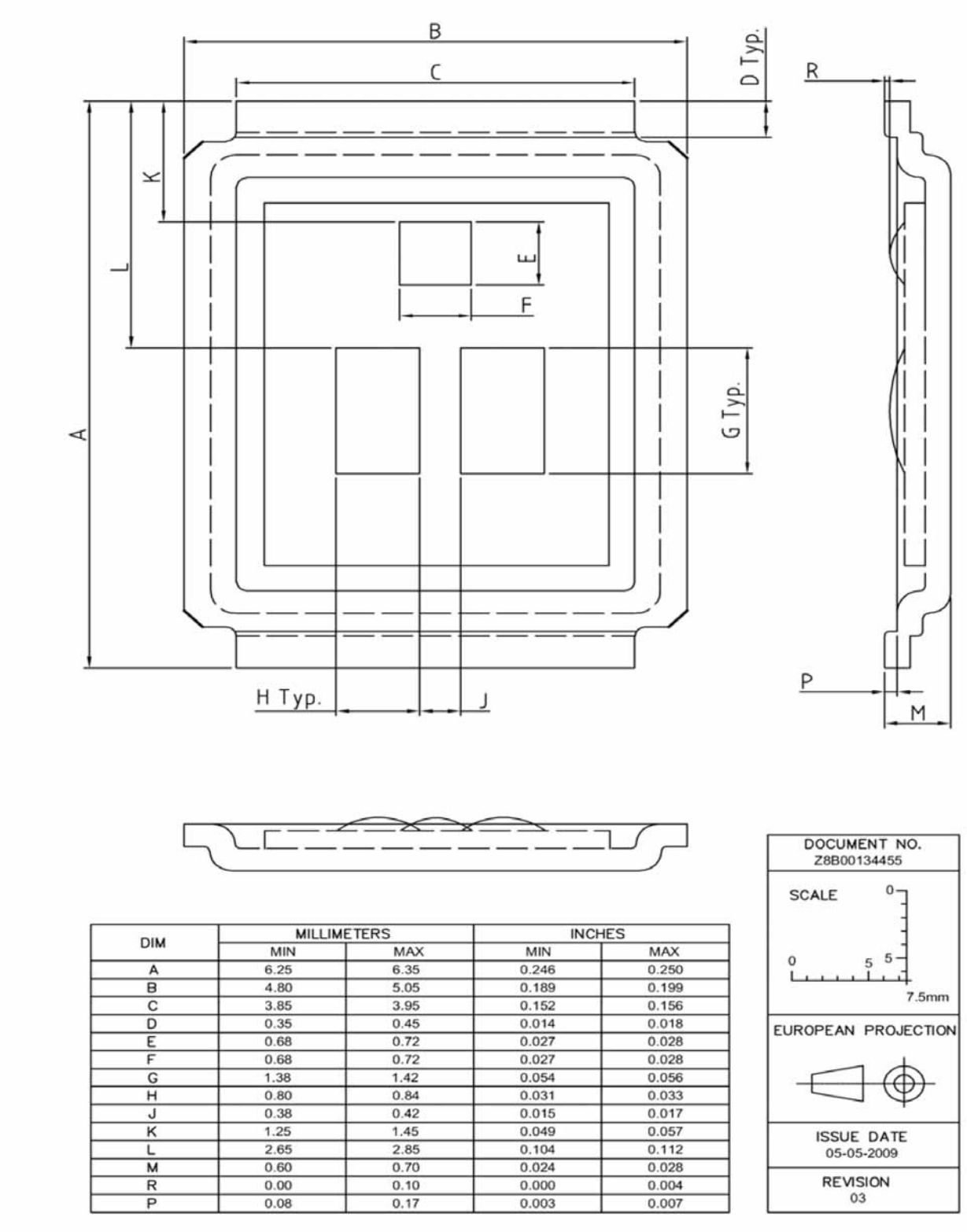
13 Avalanche characteristics	14 Typ. gate charge
	
I_{AS}=f(t_{AV}); R_{GS}=25 Ω; parameter: $T_{j(start)}$	V_{GS}=f(Q_{gate}); I_D=30 A pulsed; parameter: V_{DD}

Table 15

15 Drain-source breakdown voltage	16 Gate charge waveforms
	
$V_{BR(DSS)}$=f(V_{DS}); I_D=1 mA	

6 Package outlines



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.25	6.35	0.246	0.250
B	4.80	5.05	0.189	0.199
C	3.85	3.95	0.152	0.156
D	0.35	0.45	0.014	0.018
E	0.68	0.72	0.027	0.028
F	0.68	0.72	0.027	0.028
G	1.38	1.42	0.054	0.056
H	0.80	0.84	0.031	0.033
J	0.38	0.42	0.015	0.017
K	1.25	1.45	0.049	0.057
L	2.65	2.85	0.104	0.112
M	0.60	0.70	0.024	0.028
R	0.00	0.10	0.000	0.004
P	0.08	0.17	0.003	0.007

Figure 1 Outlines MG-WDSON-2, dimensions in mm/inches

7 Package outlines

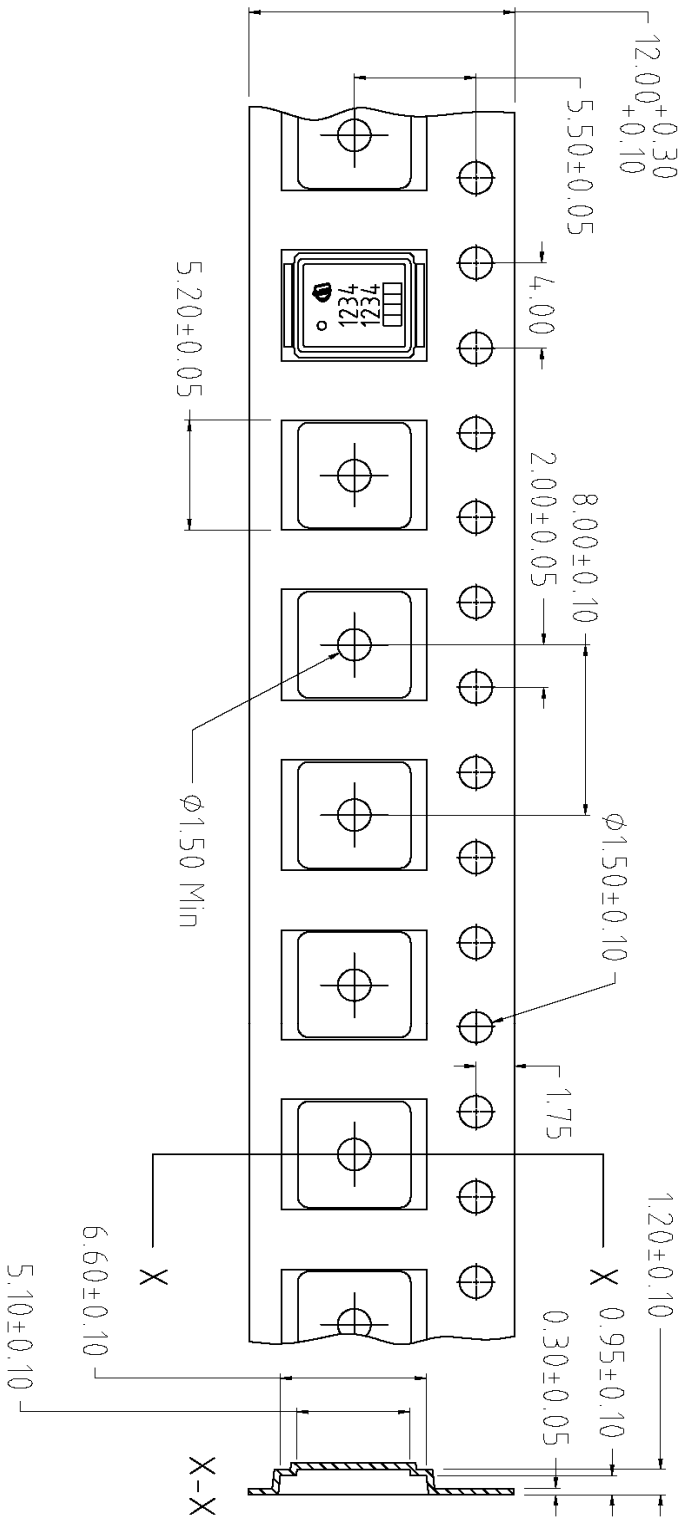
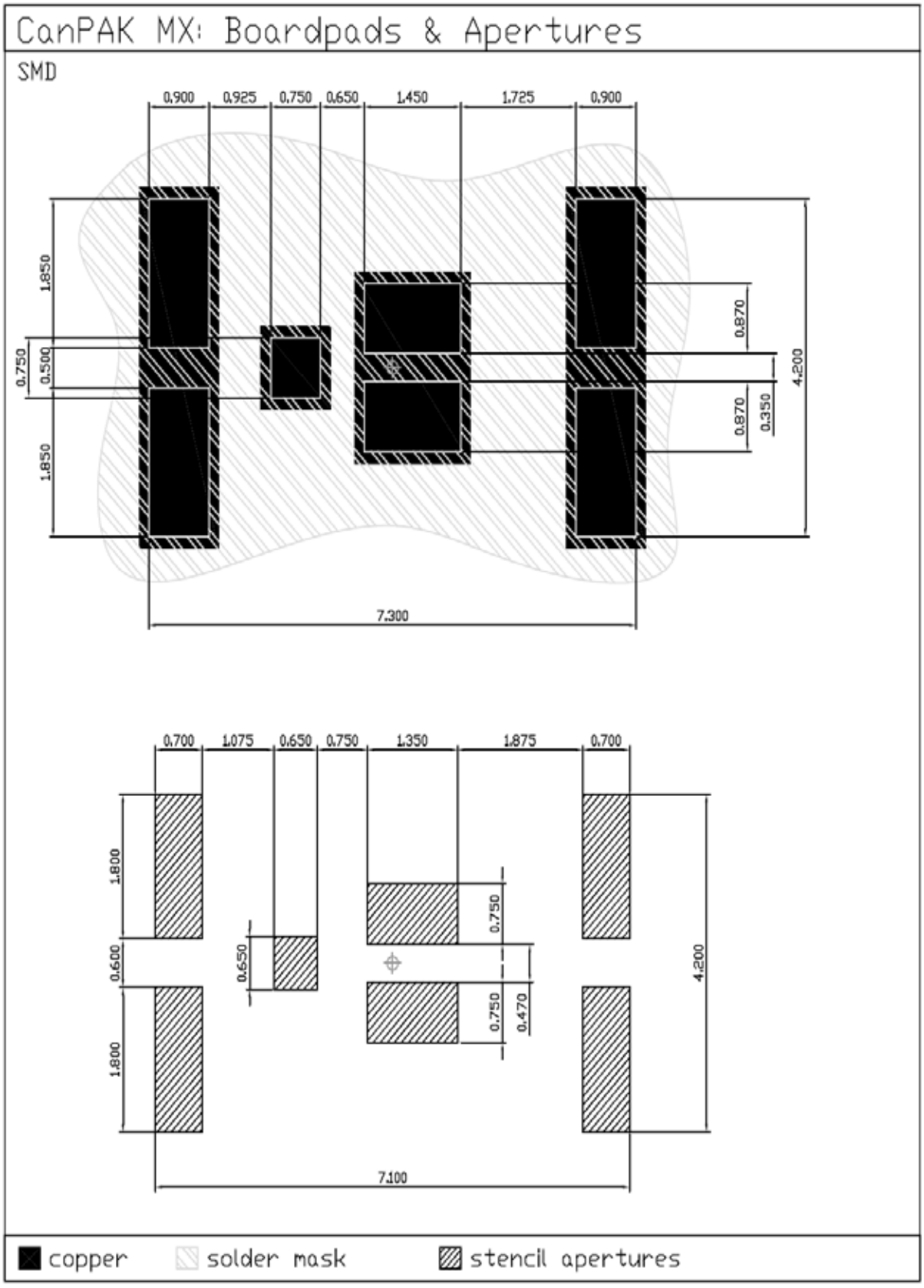


Figure 2 Outlines MG-WDSON-2, dimensions in mm/inches

8 Package outlines



9 Revision History

Revision History: 2011-03-02, 1.9

Previous Revision:

Revision	Subjects (major changes since last revision)
0.1	Release of target data sheet
1.9	Release of preliminary data sheet

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