

Mono/Stereo High-Power Class-D Amplifier

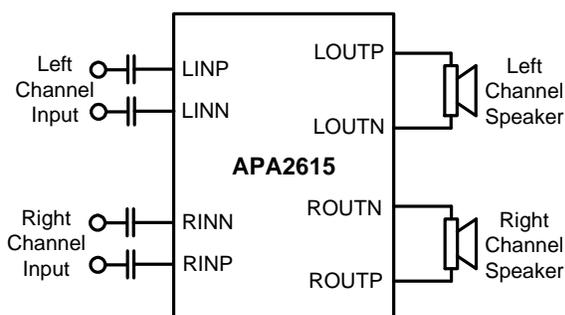
Features

- **Operating Voltage: 8.0V-16.5V**
- **High Efficiency 90% at $P_o=10W$, 8W Speaker, $V_{DD}=12V$**
- **Low Shutdown Current**
– $I_{DD}=5mA$ at $V_{DD}=16.5V$
- **Power Limit Function**
- **Switchable Non-Clip Function /DRC (Dynamic Range Control) Function**
- **Build-In Oscillator**
- **Spread Clock Function**
- **External Synchronization Function**
- **Master/Slaver Synchronization Function**
- **DC Detection Function**
- **Stereo/Monaural Function**
- **Shutdown and Mute Function**
- **Thermal and Over-Current Protections with Auto-Recovery**
- **Pin-to-Pin Compatible YDA148**
- **Space Saving Package QFN5.2x6.2-32**
- **Lead Free and Green Devices Available (RoHS Compliant)**

Applications

- LCD TV

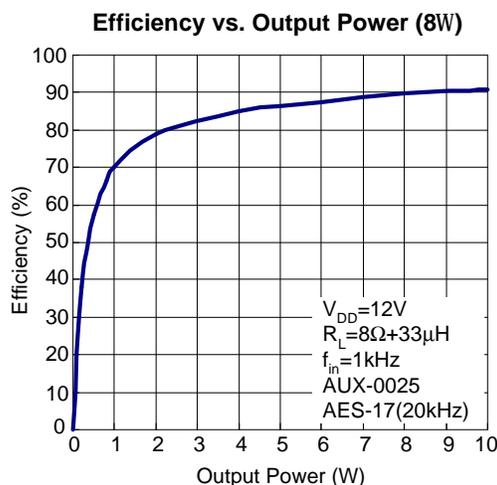
Simplified Application Circuit



General Description

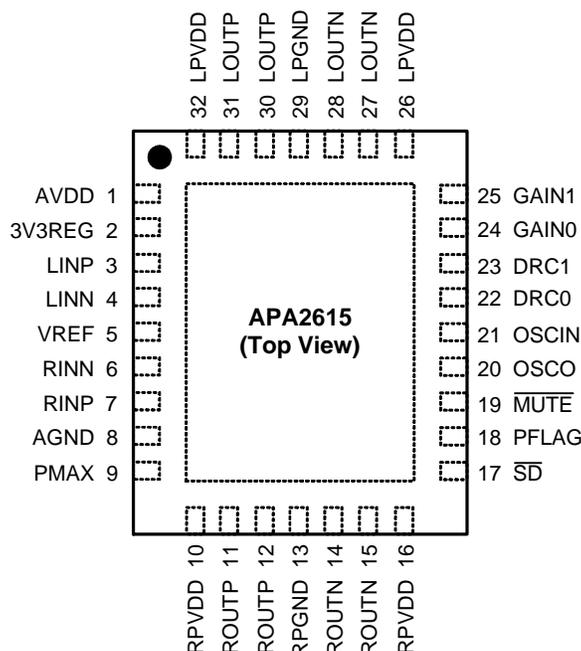
The APA2615 is a stereo, high efficiency, Class-D audio amplifier available in a QFN5.2x6.2-32 package.

The filter-free Class-D architecture eliminates the external low pass filters, and save the PCB space and BOM costs. The APA2615 also has a spread clock function that reduces the high frequency radiation and low the EMI noise. The Zero-crossing-change function changes the gain when both output (V_{OUTP} and V_{OUTN}) crossing together can minimum the pop noise. The power limit function can protect the speaker when output signal excess the speaker limit rating. The non-clip and DRC functions are eliminate the distortion at large input signal, and can fit the high dynamic input signal to a small dynamic speaker. The operating voltage is from 8V to 16.5V. The APA2615 is capable of driving 10W at 12V or 18W at 16V into 8Ω speaker and provides thermal and over-current protections. It also can detect the DC that prevents the speaker voice coil from being destroyed.



ANPEC reserves the right to make changes to improve reliability or manufacturability without notice, and advise customers to obtain the latest version of relevant information to verify before placing orders.

Pin Configuration



Ordering and Marking Information

<p>APA2615 □□□-□□□</p> <ul style="list-style-type: none"> └─ Assembly Material └─ Handling Code └─ Temperature Range └─ Package Code 	<p>Package Code QA : QFN5.2x6.2-32 Operating Ambient Temperature Range I : -40 to 85 °C Handling Code TR : Tape & Reel Assembly Material G : Halogen and Lead Free Device</p>
<p>APA2615 QA : XXXXX</p>	<p>XXXXX - Date Code</p>

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines “Green” to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Rating	Unit
V_{DD}	Supply Voltage (RPVDD to RPGND, LPVDD to LPGND, AVDD to AGND)	-0.3 to 20	V
V_{SD}	Input Voltage (\overline{SD} to AGND)	-0.3 to 20	
V_{in}	Input Voltage (LINN, LINP, RINN and RINP to AGND)	-0.3 to 4	
$V_{control}$	Input Voltage (\overline{MUTE} , PMAX, DRC0, DRC1, GAIN0 and GAIN1 to AGND)	-0.3 to 4	
V_{PGND_AGND}	Input Voltage (LPGND, RPGND to AGND)	-0.3 to +0.3	

Absolute Maximum Ratings (Cont.) (Note 1)

Symbol	Parameter	Rating	Unit
T _J	Maximum Junction Temperature	150	°C
T _{STG}	Storage Temperature Range	-65 to +150	°C
T _{SDR}	Soldering Temperature Range, 10 Seconds	260	°C
P _D	Power Dissipation	Internally Limited	W

Note1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
θ _{JA}	Junction-to-Ambient Resistance in Free Air ^(Note 2) QFN5.2x6.2-32	22	°C/W
θ _{JC}	Junction-to-Case Resistance in Free Air ^(Note 3) QFN5.2x6.2-32	4	°C/W

Note 2: θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. The exposed pad of QFN5.2X6.2-32 is soldered directly on the PCB.

Note 3: The case temperature is measured at the center of the exposed pad on the underside of the QFN5.2X6.2-32 package.

Recommended Operating Conditions (Note 4)

Symbol	Parameter	Range		Unit	
		Min.	Max.		
V _{DD}	Supply Voltage	8.0	16.5	V	
V _{IH}	High Level Threshold Voltage	SD	2.5		16.5
		MUTE, PMAX, DRC0, DRC1, GAIN0, GAIN1	2.5		3.6
V _{IL}	Low Level Threshold Voltage	SD	0		1
		MUTE, PMAX, DRC0, DRC1, GAIN0, GAIN1	0		1
V _{IC}	Common Mode Input Voltage	0	3		
T _A	Ambient Temperature Range	-40	85	°C	
T _J	Junction Temperature Range	-40	125		
R _L	Speaker Resistance	3.5	-	Ω	

Note 4: At stereo mode, if the R_L=4Ω, the V_{DD} should not exceed 12V or it may trigger the Over-Current Protection.

Electrical Characteristics

V_{DD}=12V, GND=0V, T_A= 25°C, A_v=22dB (unless otherwise noted)

Symbol	Parameter	Test Conditions	APA2615			Unit
			Min.	Typ.	Max.	
V _{3V3REG}		I _o =2mA	2.85	3.3	3.75	V
V _{VREF}			-	V _{3V3REG} /2	-	
V _{DET}	The DC Detection Active Voltage at Output	DC detection (>0.5s)	-	2	2.5	

Electrical Characteristics (Cont.)

$V_{DD}=12V$, $GND=0V$, $T_A=25^{\circ}C$, $A_v=22dB$ (unless otherwise noted)

Symbol	Parameter	Test Conditions	APA2615			Unit
			Min.	Typ.	Max.	
V_{FLAG}	Protection Flag Output Voltage	$I_{SOURCING}=0.4mA$	-	-	0.4	V
V_{OSCOH}	Oscillator Output Voltage	$I_{SOURCING}=4mA$	2.2	-	-	
V_{OSCOL}	Oscillator Output Voltage	$I_{SINKING}=4mA$	-	-	0.6	
T_{SD}	Recovery Time from Shutdown	$C_5=0.1\mu F$	-	1	1.5	s
T_{MUTE}	Recovery Time from Mute		-	-	0.001	
I_{DD}	Supply Current	No Load	-	18	36	mA
I_{MUTE}	Mute Current		-	2	10	
I_{SD}	Shutdown Current	$\overline{SD} = 0V$	-	5	100	μA
I_I	Input Current	\overline{SD} , \overline{MUTE} , DRC0, DRC1, GAIN0, GAIN1	-	-	5	
F_{OSC}	Internal Oscillator Frequency		400	500	600	kHz
F_{OSCI}	External Clock at OSCI Pin		400	500	600	
DC_{OSCI}	Duty Cycle of External Clock		40	-	60	%
R_{DSON}	Static Drain-Source On-State Resistance (P-channel and N channel Power MOSFET)	$V_{DD}=8V$, $I_L=0.8A$	-	530	-	m Ω
		$V_{DD}=12V$, $I_L=1A$	-	480	-	
		$V_{DD}=16V$, $I_L=1.4A$	-	440	-	
R_i	Input Resistor	RINN, RINP, LINN, LINP (Gain independent)	8	10	12	k Ω
R_o	Output Resistor	ROUTN, ROUTP, LOUTN, LOUTP	-	300	-	
η	Efficiency	Stereo, $R_L=8\Omega$, $P_O=9W$	-	89	-	%
		Stereo, $R_L=4\Omega$, $P_O=15W$	-	85	-	
A_v	Closed-Loop Gain	DRC[1:0] (0,0), GAIN (0,0)	-	22	-	dB
		DRC (0,0), GAIN (0,1)	-	28	-	
		DRC (0,0), GAIN (1,0)	-	34	-	
		DRC (0,0), GAIN (1,1)	-	16	-	
		DRC (0,1), GAIN (0,0)	-	34	-	
		DRC (0,1), GAIN (0,1)	-	40	-	
		DRC (0,1), GAIN (1,0)	-	46	-	
		DRC (0,1), GAIN (1,1)	-	28	-	
		DRC (1,0), GAIN (0,0)	-	34	-	
		DRC (1,0), GAIN (0,1)	-	40	-	
		DRC (1,0), GAIN (1,0)	-	46	-	
		DRC (1,0), GAIN (1,1)	-	28	-	
		DRC (1,1), GAIN (0,0)	-	34	-	
		DRC (1,1), GAIN (0,1)	-	40	-	
		DRC (1,1), GAIN (1,0)	-	46	-	
DRC (1,1), GAIN (1,1)	-	28	-			

Electrical Characteristics (Cont.)

$V_{DD}=12V, GND=0V, T_A=25^{\circ}C, A_V=22dB$ (unless otherwise noted)

STEREO MODE

Symbol	Parameter	Test Conditions	APA2615			Unit	
			Min.	Typ.	Max.		
$V_{DD}=16V, T_A=25^{\circ}C$							
P_O	Output Power	THD+N=1% $f_{in}=1kHz$	$R_L=8\Omega$	-	14	-	W
		THD+N=10% $f_{in}=1kHz$	$R_L=8\Omega$	-	18	-	
THD+N	Total Harmonic Distortion Plus Noise	$f_{in}=1kHz$	$R_L=8\Omega$ $P_O=10W$	-	0.05	0.1	%
Crosstalk	Channel Separation	$P_O=1W, R_L=8\Omega, f_{in}=1kHz$		-	-70	-60	dB
PSRR	Power Supply Rejection Ratio	$R_L=8\Omega$	$f_{in}=100Hz$	-	-65	-55	
			$f_{in}=1kHz$	-	-65	-55	
CMRR	Common Mode Rejection Ration	$f_{in}=1kHz, R_L=8\Omega, V_{in}=0.1V_{pp}, A_V=22dB$		-	-65	-55	
Att_{Mute}	Mute Attenuation	$f_{in}=1kHz, R_L=8\Omega, V_{in}=1V_{pp}$		-	-115	-100	
$Att_{shutdown}$	Shutdown Attenuation	$f_{in}=1kHz, R_L=8\Omega, V_{in}=1V_{pp}$		-	-115	-100	
V_{OS}	Offset Voltage	No load, $A_V=22dB$		-	-	20	mV
V_n	Noise Output Voltage	With A-weighting Filter ($A_V=22dB$)		-	250	500	μV_{rms}
$V_{DD}=12V, T_A=25^{\circ}C$							
P_O	Output Power	THD+N=1% $f_{in}=1kHz$	$R_L=4\Omega$	-	14	-	W
			$R_L=8\Omega$	-	8	-	
		THD+N=10% $f_{in}=1kHz$	$R_L=4\Omega$	-	17	-	
			$R_L=8\Omega$	-	10	-	
THD+N	Total Harmonic Distortion Plus Noise	$f_{in}=1kHz$	$R_L=4\Omega$ $P_O=10W$	-	0.07	0.1	%
			$R_L=8\Omega$ $P_O=6W$	-	0.07	0.1	
Crosstalk	Channel Separation	$P_O=0.5W, R_L=8\Omega, f_{in}=1kHz$		-	-70	-60	dB
PSRR	Power Supply Rejection Ratio	$R_L=8\Omega,$	$f_{in}=100Hz$	-	-65	-55	
			$f_{in}=1kHz$	-	-65	-55	
CMRR	Common Mode Rejection Ration	$f_{in}=1kHz, R_L=8\Omega, V_{in}=0.1V_{pp}, A_V=22dB$		-	-65	-55	
Att_{Mute}	Mute Attenuation	$f_{in}=1kHz, R_L=8\Omega, V_{in}=1V_{pp}$		-	-115	-100	
$Att_{shutdown}$	Shutdown Attenuation	$f_{in}=1kHz, R_L=8\Omega, V_{in}=1V_{pp}$		-	-115	-100	
V_{OS}	Offset Voltage	No load, $A_V=22dB$		-	-	20	mV
V_n	Noise Output Voltage	With A-weighting Filter ($A_V=22dB$)		-	230	500	μV_{rms}
$V_{DD}=8V, T_A=25^{\circ}C$							
P_O	Output Power	THD+N=1% $f_{in}=1kHz$	$R_L=4\Omega$	-	6	-	W
			$R_L=8\Omega$	-	3.5	-	
		THD+N=10% $f_{in}=1kHz$	$R_L=4\Omega$	-	7.5	-	
			$R_L=8\Omega$	-	4.5	-	

Electrical Characteristics (Cont.)

$V_{DD}=12V$, $GND=0V$, $T_A=25^{\circ}C$ (unless otherwise noted)

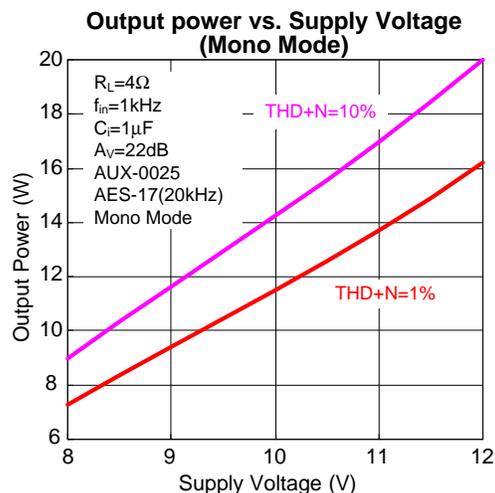
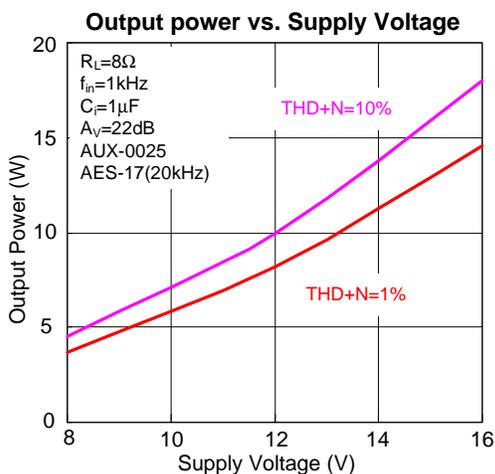
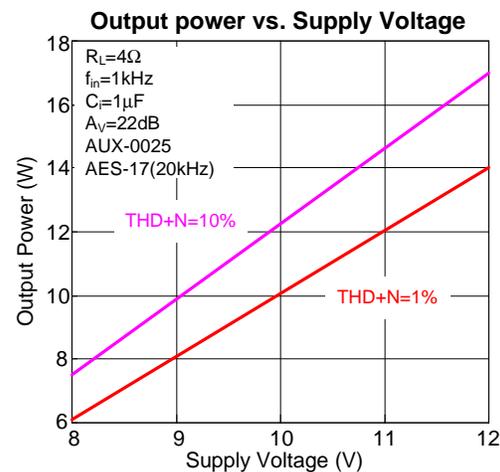
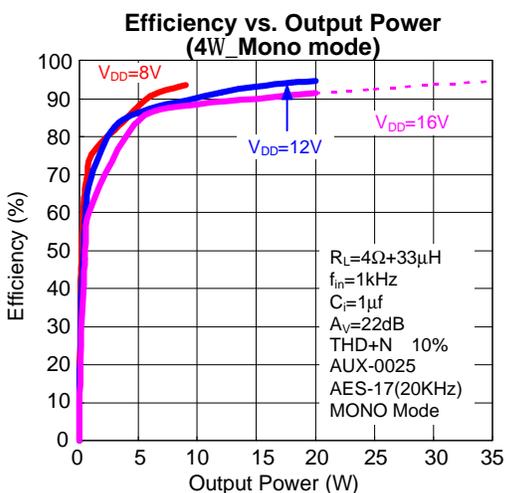
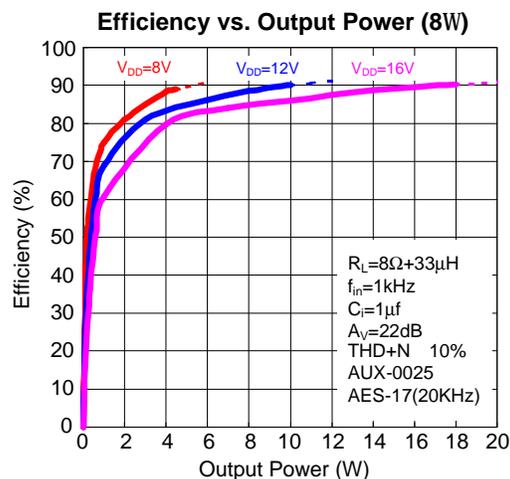
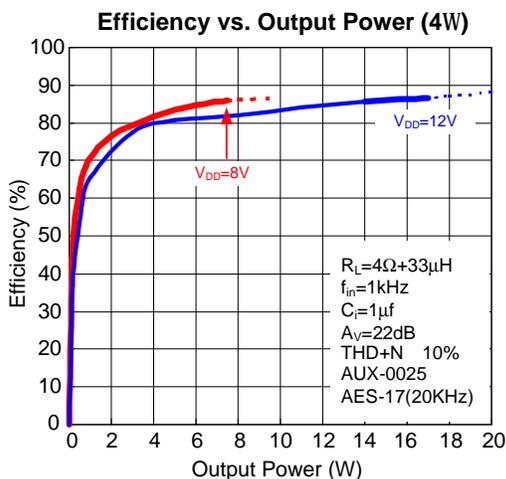
STEREO MODE

Symbol	Parameter	Test Conditions	APA2615			Unit	
			Min.	Typ.	Max.		
$V_{DD}=8V, T_A=25^{\circ}C$ (CONT.)							
THD+N	Total Harmonic Distortion Plus Noise	$f_{in}=1kHz$	$R_L=4\Omega$ $P_O=4.5W$	-	0.1	0.2	%
			$R_L=8\Omega$ $P_O=2.5W$	-	0.1	0.2	
Crosstalk	Channel Separation	$P_O=0.5W, R_L=8\Omega, f_{in}=1kHz$	-	-60	-60	dB	
PSRR	Power Supply Rejection Ratio	$R_L=8\Omega$	$f_{in}=100Hz$	-	-65		-55
			$f_{in}=1kHz$	-	-65		-55
CMRR	Common Mode Rejection Ration	$f_{in}=1kHz, R_L=8\Omega, V_{in}=0.1V_{pp}, A_V=22dB$	-	-70	-55		
Att_{Mute}	Mute Attenuation	$f_{in}=1kHz, R_L=8\Omega, V_{in}=1V_{pp}$	-	-115	-100		
$Att_{shutdown}$	Shutdown Attenuation	$f_{in}=1kHz, R_L=8\Omega, V_{in}=1V_{pp}$	-	-115	-100		
V_{OS}	Offset Voltage	No load, $A_V=22dB$	-	-	20	mV	
V_n	Noise Output Voltage	With A-weighting Filter ($A_V=22dB$)	-	200	400	μV_{rms}	

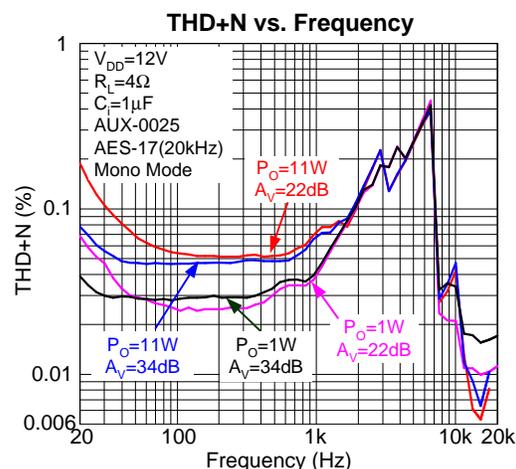
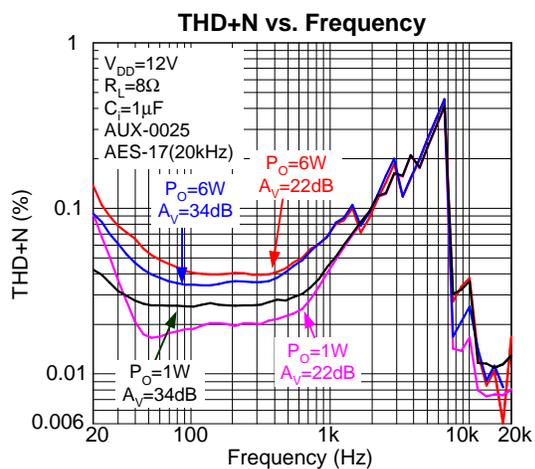
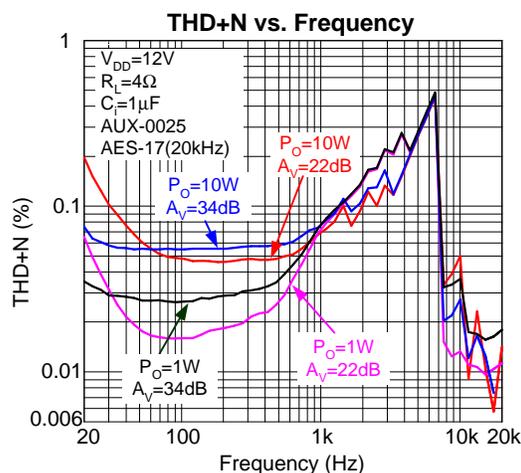
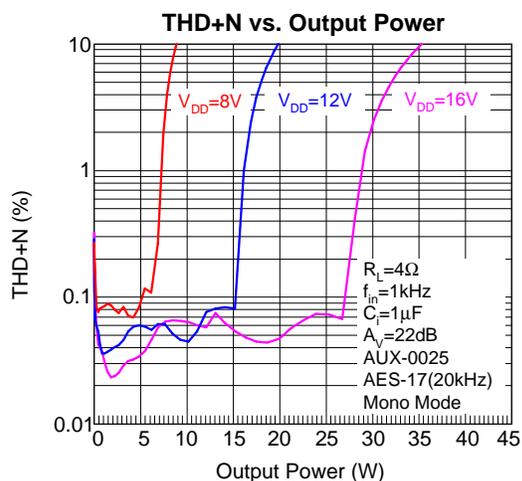
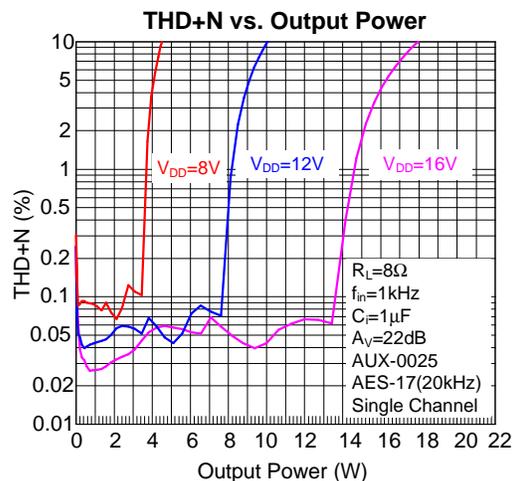
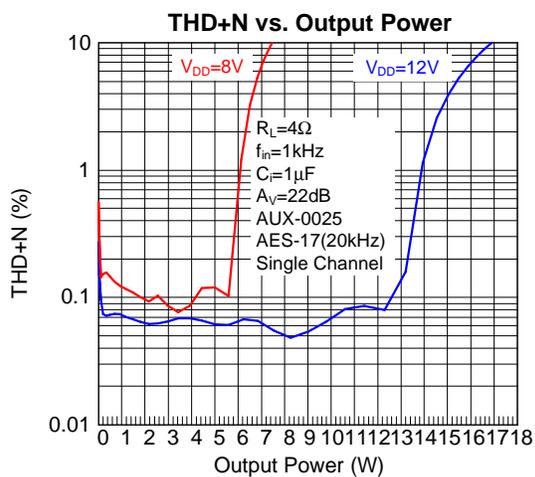
MONO MODE

Symbol	Parameter	Test Conditions	APA2615			Unit	
			Min.	Typ.	Max.		
$V_{DD}=12V, T_A=25^{\circ}C$							
P_O	Output Power	THD+N=1% $f_{in}=1kHz$	$R_L=4\Omega$	-	16	-	W
			$R_L=8\Omega$	-	8.5	-	
		THD+N=10% $f_{in}=1kHz$	$R_L=4\Omega$	-	20	-	
			$R_L=8\Omega$	-	11	-	
THD+N	Total Harmonic Distortion Plus Noise	$f_{in}=1kHz$	$R_L=4\Omega$ $P_O=12W$	-	0.08	0.2	%
			$R_L=8\Omega$ $P_O=6W$	-	0.1	0.2	
PSRR	Power Supply Rejection Ratio	$R_L=8\Omega,$	$f_{in}=100Hz$	-	-65	-55	dB
			$f_{in}=1kHz$	-	-65	-55	
CMRR	Common Mode Rejection Ration	$f_{in}=1kHz, R_L=8\Omega, V_{in}=0.1V_{pp}, A_V=22dB$	-	-60	-55	dB	
Att_{Mute}	Mute Attenuation	$f_{in}=1kHz, R_L=8\Omega, V_{in}=1V_{rms}$	-	-115	-100		
$Att_{shutdown}$	Shutdown Attenuation	$f_{in}=1kHz, R_L=8\Omega, V_{in}=1V_{rms}$	-	-115	-100		
V_{OS}	Offset Voltage	No load, $A_V=22dB$	-	-	20	mV	
V_n	Noise Output Voltage	With A-weighting Filter ($A_V=22dB$)	-	200	400	μV_{rms}	

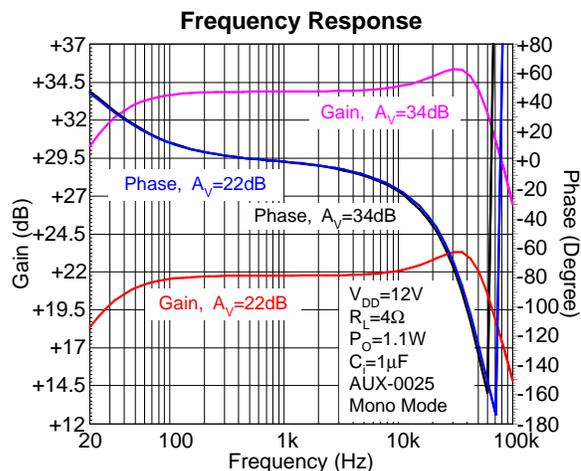
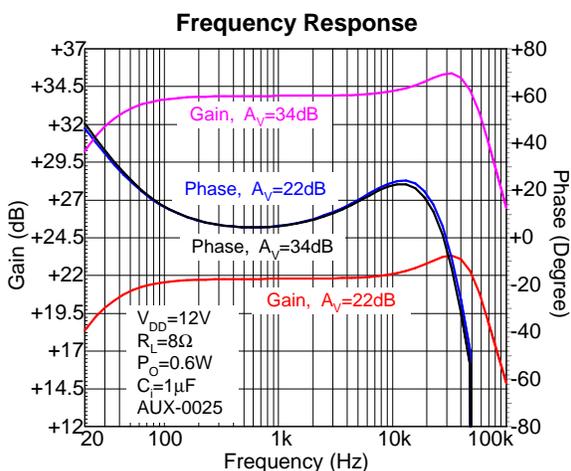
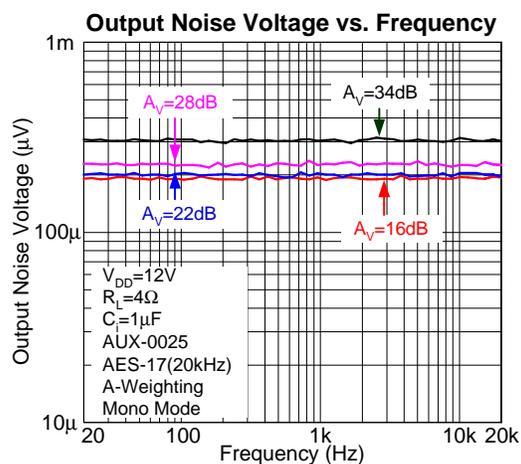
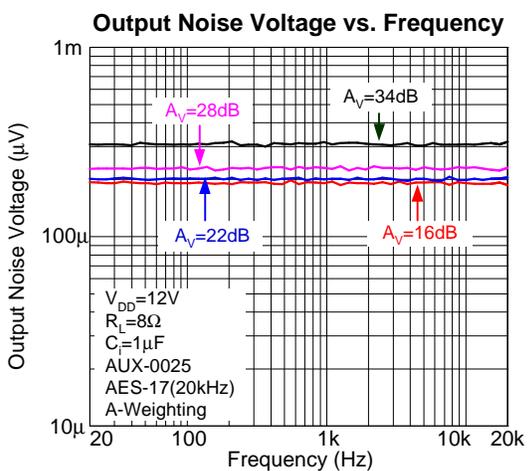
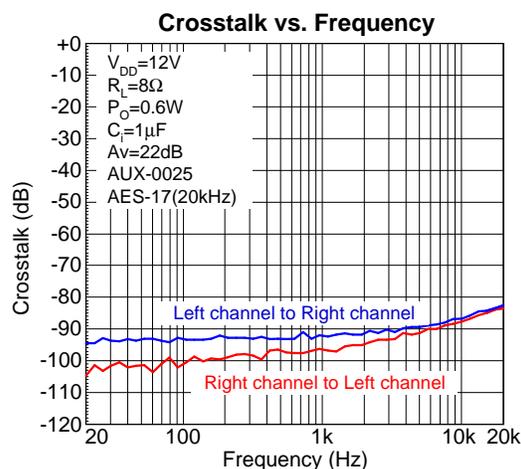
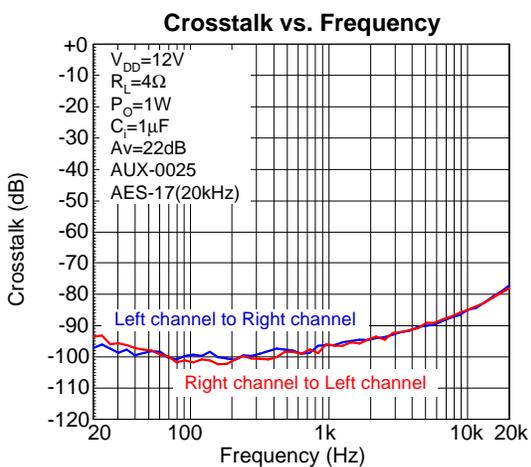
Typical Operating Characteristics



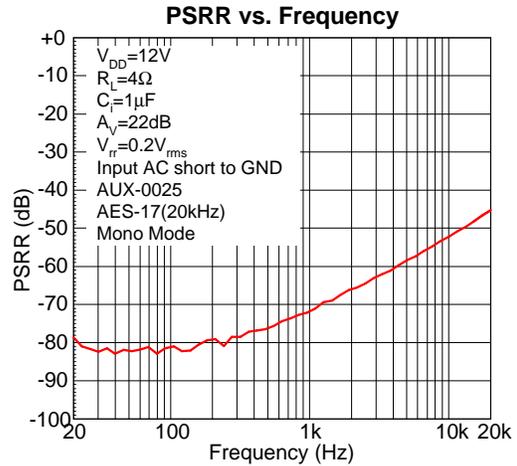
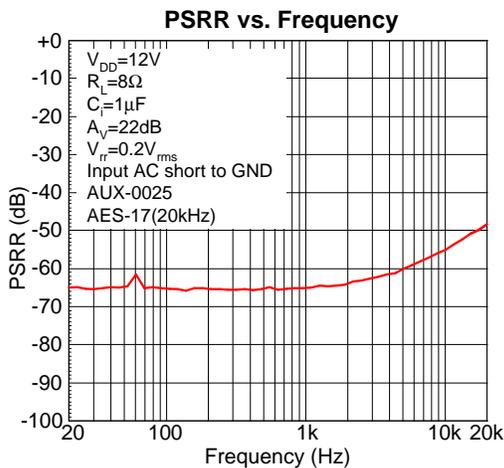
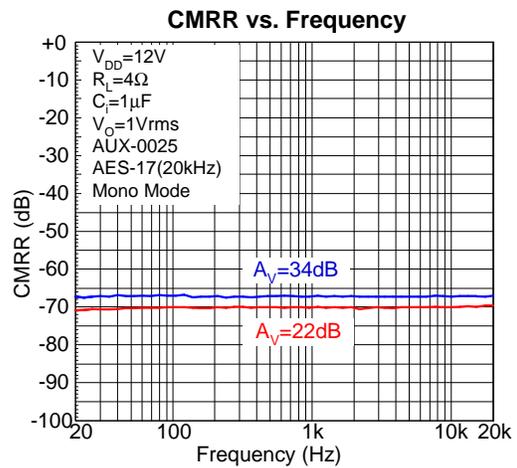
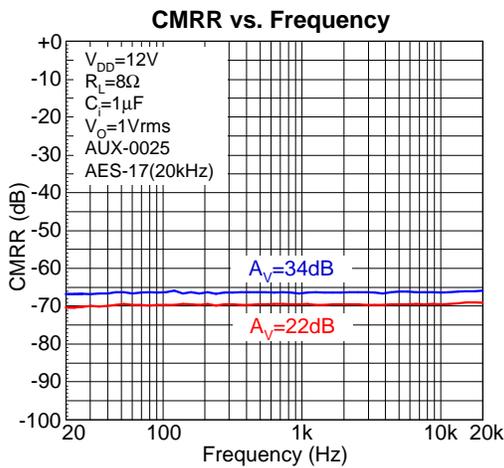
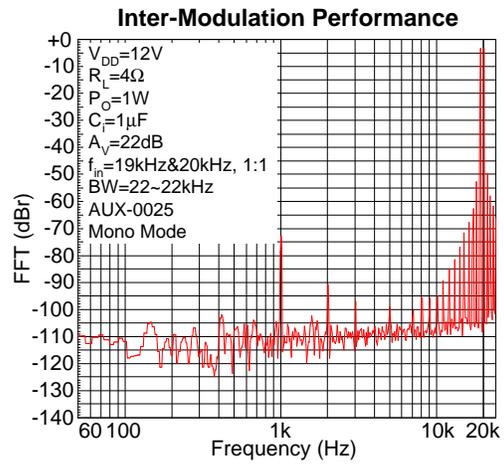
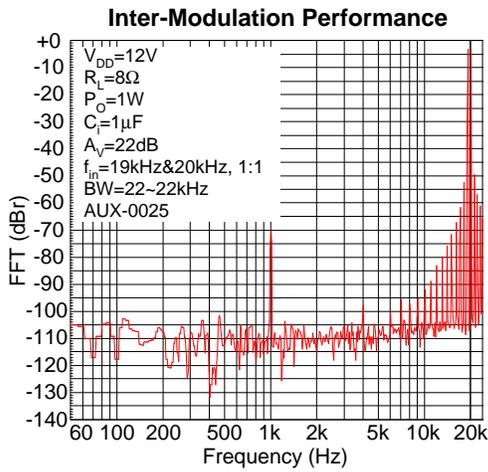
Typical Operating Characteristics (Cont.)



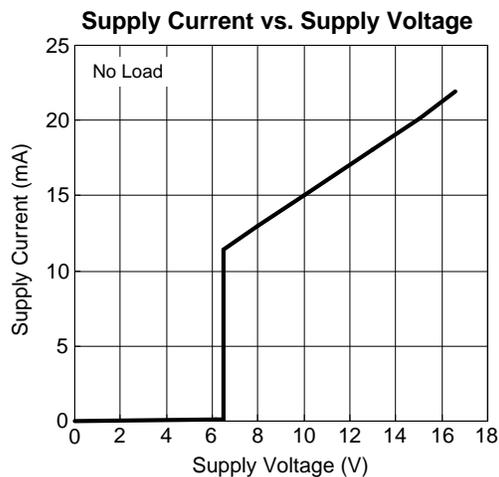
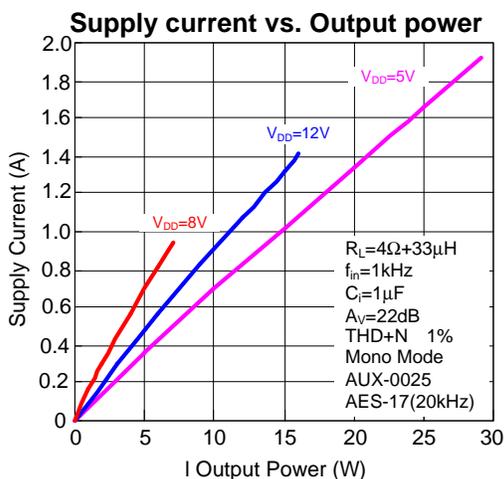
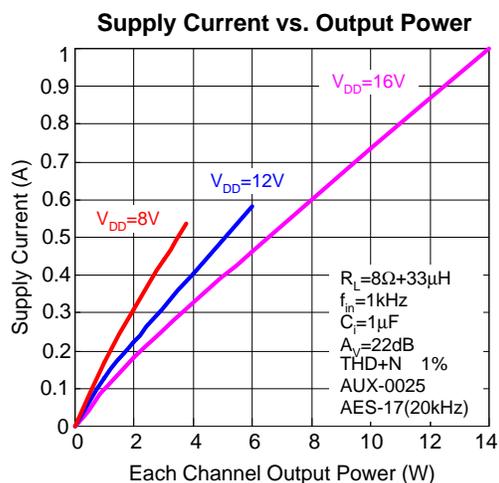
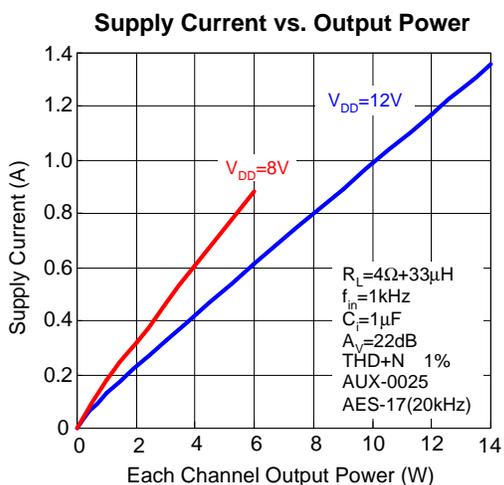
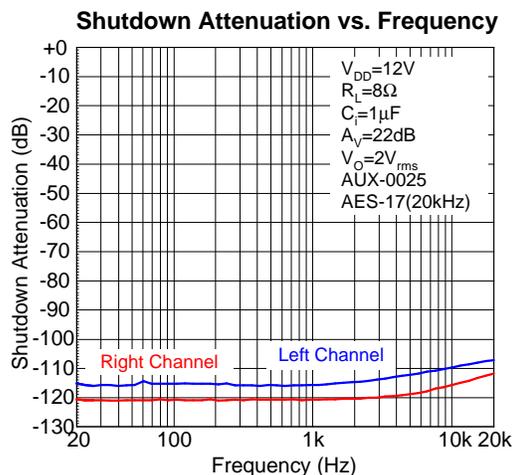
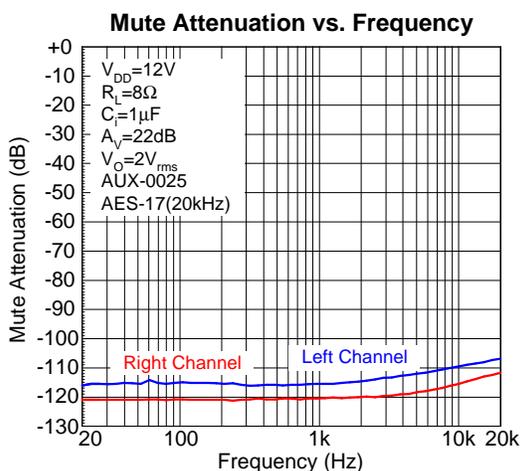
Typical Operating Characteristics (Cont.)



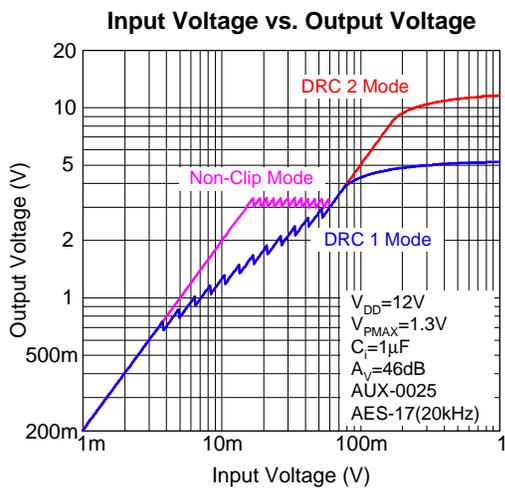
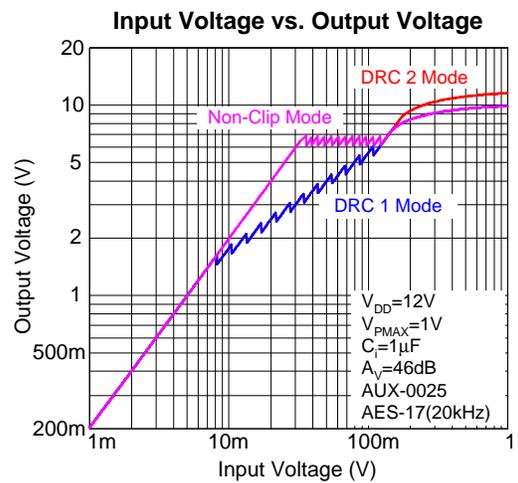
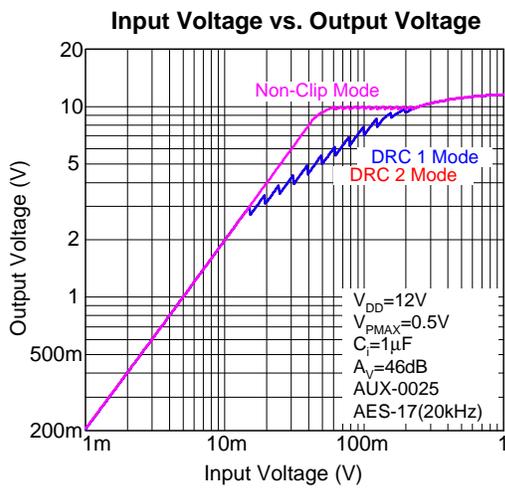
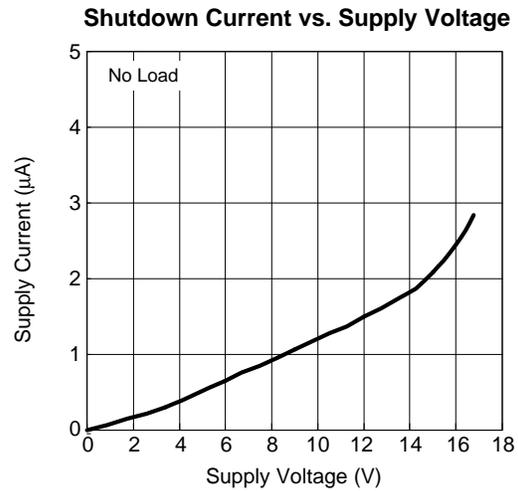
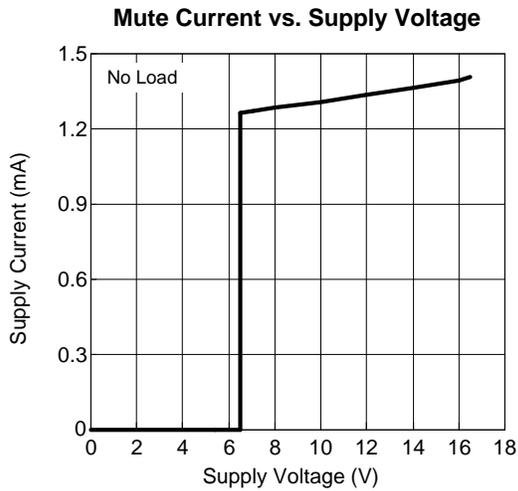
Typical Operating Characteristics (Cont.)



Typical Operating Characteristics (Cont.)

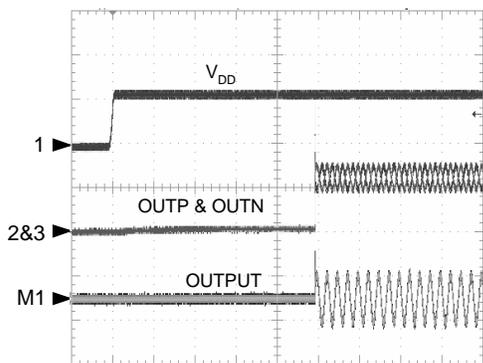


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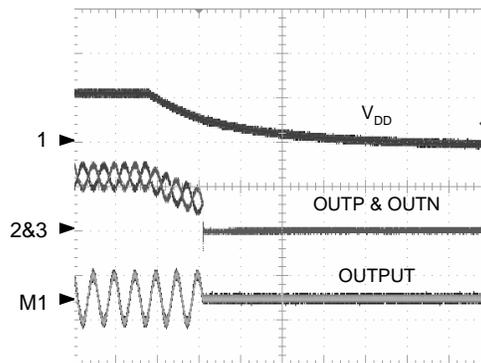
Typical Operating Characteristics (Cont.)

Power On



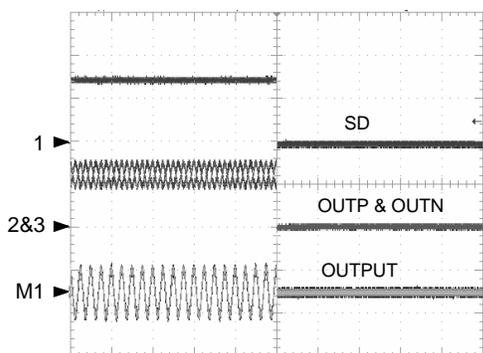
CH1: V_{DD} , 10V/Div, DC
 CH2: OUTP, 5V/Div, DC
 CH3: OUTN, 5V/Div, DC
 CHM1: OUTPUT, 5V/Div, DC
 TIME: 200ms/Div

Power Off



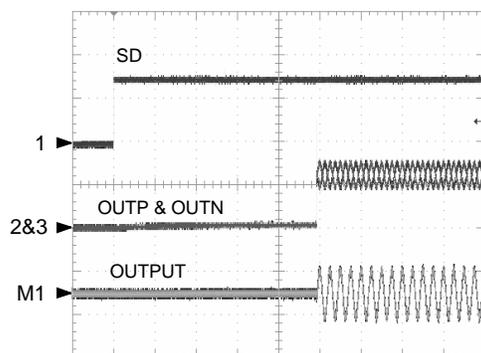
CH1: V_{DD} , 10V/Div, DC
 CH2: OUTP, 5V/Div, DC
 CH3: OUTN, 5V/Div, DC
 CHM1: OUTPUT, 5V/Div, DC
 TIME: 100ms/Div

Shutdown



CH1: SD, 2V/Div, DC
 CH2: OUTP, 5V/Div, DC
 CH3: OUTN, 5V/Div, DC
 CHM1: OUTPUT, 5V/Div, DC
 TIME: 200ms/Div

Shutdown Release

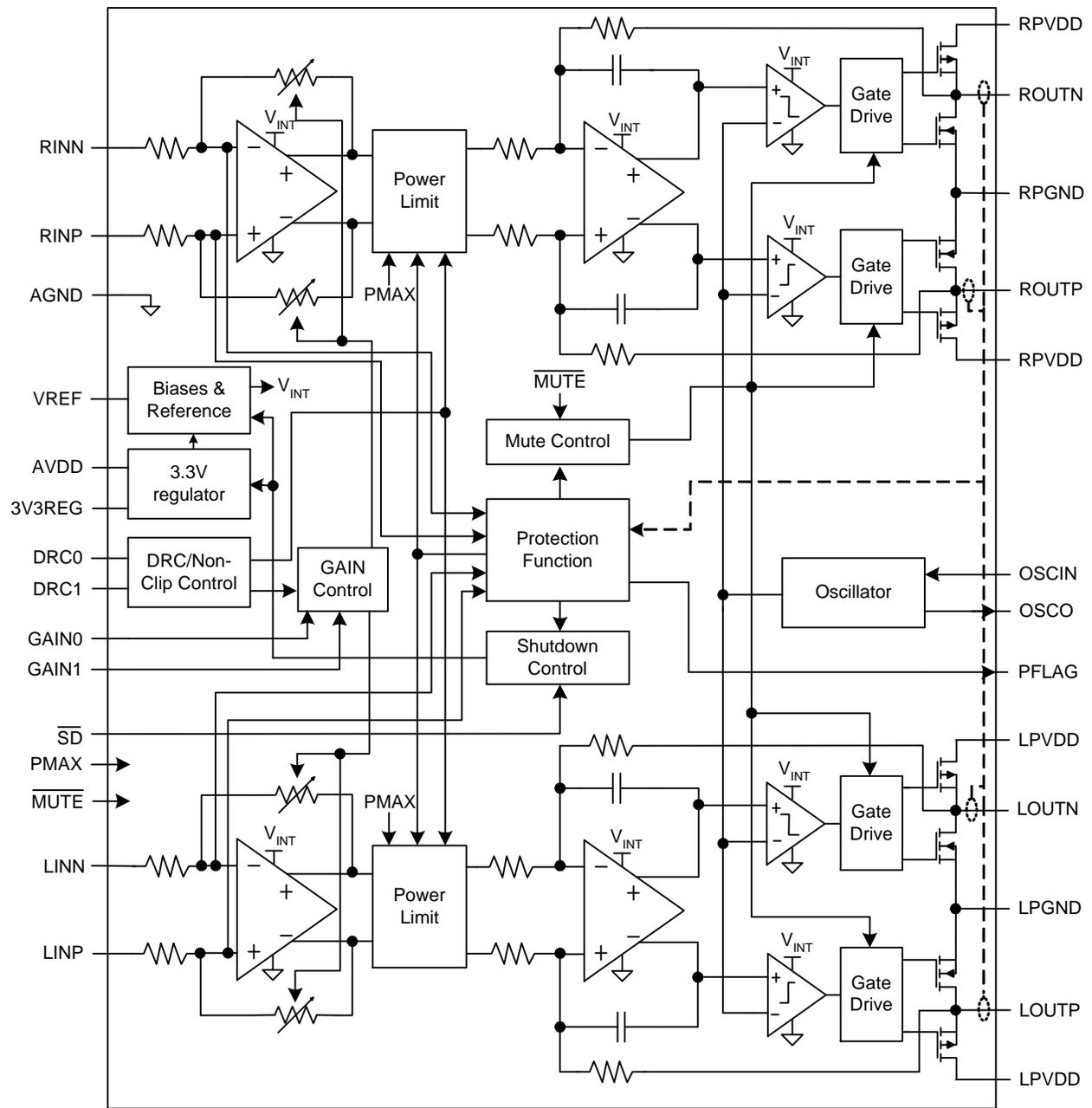


CH1: SD, 2V/Div, DC
 CH2: OUTP, 5V/Div, DC
 CH3: OUTN, 5V/Div, DC
 CHM1: OUTPUT, 5V/Div, DC
 TIME: 200ms/Div

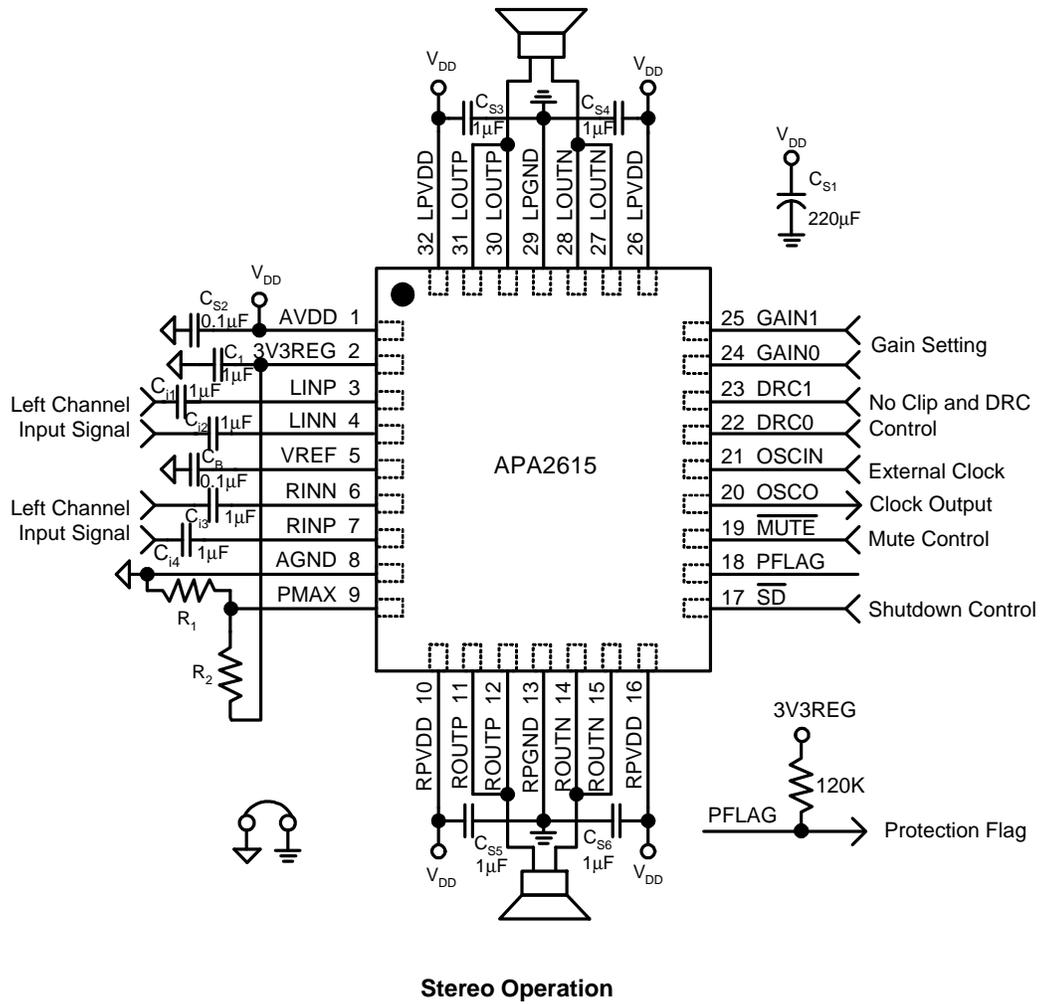
Pin Description

PIN		I/O/P	FUNCTION
NO.	NAME		
1	AVDD	P	Power supply for control block.
2	3V3REG	O	Regulator output, 3.3V. Only for internal used.
3	LINP	I	The positive input of left channel amplifier.
4	LINN	I	The negative input of left channel amplifier.
5	VREF	P	The reference voltage output.
6	RINN	I	The negative input of right channel amplifier.
7	RINP	I	The positive input of right channel amplifier.
8	AGND	P	Ground connection for control block.
9	PMAX	I	Input for set the power limit function. Enable: $P_{O(MAX)}=(1.65-V_{P_{MAX}}) \times 11.23$, Disable: GND.
10,16	RPVDD	P	The power supply for right channel Class-D amplifier.
11,12	ROUTP	O	The positive output of right channel Class-D amplifier.
13	RPGND	P	Ground connection for right channel Class-D amplifier.
14,15	ROUTN	O	The negative output of right channel Class-D amplifier.
17	\overline{SD}	I	Shutdown mode control input, place entire IC in shutdown mode when held low.
18	PFLAG	O	Protection flag output (open drain).
19	\overline{MUTE}	I	Mute mode control input; pull low to mute the Class-D amplifier's output.
20	OSCO	O	The internal oscillator's output, for synchronization other APA2615s.
21	OSCIN	I	External clock input.
22	DRC0	I	Non-clip and DRC (Dynamic Range Compress) control; LSB bit 0.
23	DRC1	I	Non-clip and DRC (Dynamic Range Compress) control; MSB bit 1.
24	GAIN0	I	Control pin for internal gain setting, LSB, bit0.
25	GAIN1	I	Control pin for internal gain setting, MSB, bit1.
26,32	LPVDD	P	The power supply for left channel Class-D amplifier.
27,28	LOUTN	O	The negative output of left channel Class-D amplifier.
29	LPGND	P	Ground connection for left channel Class-D amplifier.
30,31	LOUTP	O	The positive output of left channel Class-D amplifier.

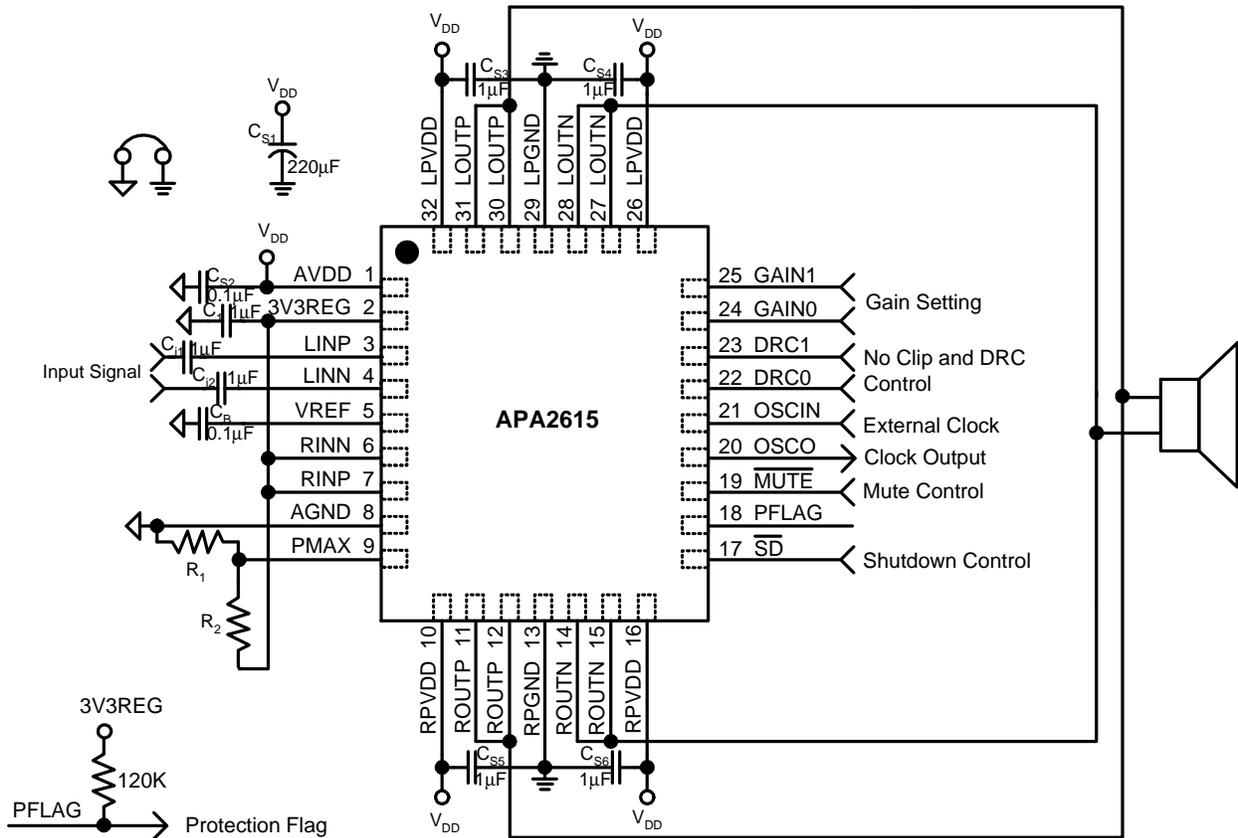
Block Diagram



Typical Application Circuits



Typical Application Circuits (Cont.)



Monaural Operation

Function Description

Class D Operation

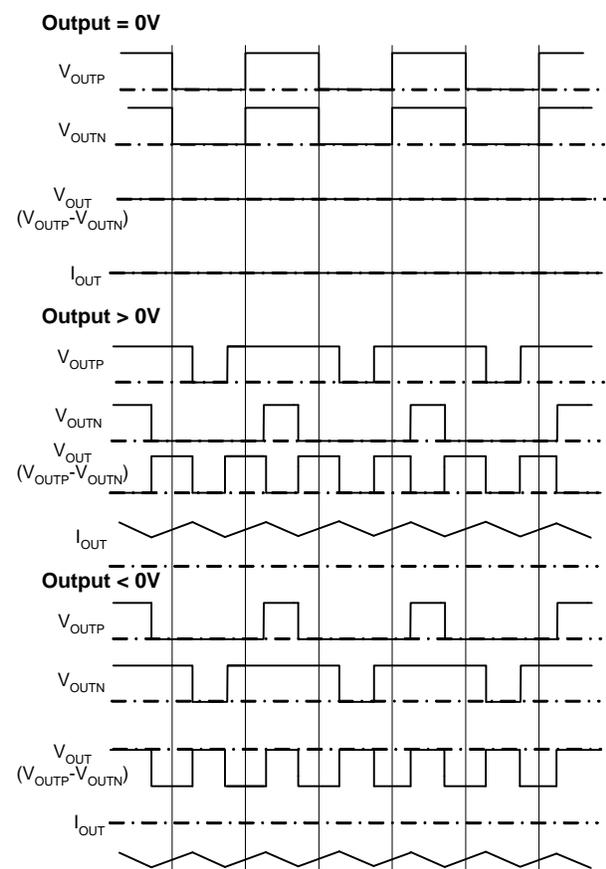


Figure 1. The APA2615 Output Waveform (Voltage & Current)

The APA2615 power amplifier modulation scheme is shown in figure 1. The outputs V_{OUTP} and V_{OUTN} are in phase with each other when no input signals. When output $> 0V$, the duty cycle of V_{OUTP} is greater than 50% and V_{OUTN} is less than 50%; when Output $< 0V$, the duty cycle of V_{OUTP} is less than 50% and V_{OUTN} is greater than 50%. This method reduces the switching current across the load and reduces the I^2R losses in the load that improves the amplifier's efficiency.

This modulation scheme has very short pulses across the load, this making the small ripple current and very little loss on the load, and the LC filter can be eliminated in most applications. Added the LC filter can increase the efficiency by filter the ripple current.

3.3V Regulator Operation

The 3V3REG regulates the voltage at 3.3V and only for internal circuit used. And connect a capacitor from $1\mu F$ to $4.7\mu F$ (X5R or above) for stable. ($0.8\mu F$ or more should be secured including its variation and temperature change.)

Reference Voltage

The voltage output of VREF pin is equal to $V_{3V3REG}/2$ and needs to connect a capacitor of $0.1\mu F$ for voltage stabilization.

Gain Setting Operation

Table 1. The gain setting

GAIN1	GAIN0	DRC1	DRC0	Gain
0	0	0	0	22dB
0	1	0	0	28dB
1	0	0	0	34dB
1	1	0	0	16dB
0	0	X	1	34dB
0	1	X	1	40dB
1	0	X	1	46dB
1	1	X	1	28dB
0	0	1	X	34dB
0	1	1	X	40dB
1	0	1	X	46dB
1	1	1	X	28dB

The APA2615's gain can be set by GAIN0, GAIN1. The detail gain setting value is list at table 1.

Mute Operation

At mute state, the Class-D output will be forced at 50% duty at OUTP and OUTN, so differential is zero, and output signals have be disabled. The recovery time of mute state to normal operation is about 1ms (max.).

Shutdown Operation

In order to reduce power consumption while not in use, the APA2615 contains a shutdown function to externally turn off the amplifier bias circuitry. This shutdown feature turns the amplifier off when logic low is placed on the \overline{SD} pin for APA2615. The trigger point between a logic high and logic low level is typically 1.5V. It is the best to switch between the ground and the supply voltage VDD to provide maximum device performance. By switching the \overline{SD} pin to low level, the amplifier enters a low-consumption-

Function Description (Cont.)

Shutdown Operation (Cont.)

current state, I_{DD} for APA2615 is in the shutdown mode. On normal operating, APA2615's \overline{SD} pin should pull to a high level to keep the IC out of the shutdown mode. The \overline{SD} pin should be tied to a definite voltage to avoid unwanted state change.

Oscillator Operation

OSCI PIN	Mode	OSCO
0 fixed	Internal fixed clock mode	Internal fixed clock output
1 fixed	Internal spread clock mode (5)	Internal spread clock output
Clock in	External clock mode	External clock buffer output

When the OSCI pin pulls low, the APA2615 works at internal fixed clock mode, and OSCO pin is output that fixed clock (500kHz); when the OSCI pin pulls high, the APA2615 works at internal spread clock mode, and the clock range is from 400kHz to 600kHz; the OSCO pin is the buffer for output these spread clock.

Apply the external clock to the OSCI pin, the APA2615 will work at external clock mode, and the external clock should at the range from 400kHz to 600kHz and the duty cycle should be at range from 40% to 60%, and the OSCO is the external clock's output buffer.

Power Limit Operation

This function limits the maximum output power of APA2615 for prevent exceeding the maximum power of speaker. Except DRC 2 mode, this function is always enabled. The setting value can be a voltage divider by resistor that connects 3V3REG and GND.

The maximum power limit value (peak voltage) = $(1.65 \cdot V_{P_{MAX}}) \times 11.23$.

Non-Clip Operation

When the DRC [1:0]=01 (DRC1=Low, and DRC0=High), the non-clip mode is active. The gain is increasing by 12dB compared to the normal mode. The output peak voltage becomes the power limit value. If the peak voltage exceeds the power limit value, it will be attenuated to the power limit value, and the maximum attenuation is -12dB. The attack time is zero second and needs 7.7

seconds to release the non-clip function from -12dB to 0dB.

The Non-clip operation should be switched under power-off or shut down mode to prevent the pop noise between the mode switching.

DRC Operation

DRC1	DRC0	Mode
0	0	Normal mode (DRC mode off , Non-clip mode off)
0	1	Non-Clip mode
1	0	DRC 1 mode
1	1	DRC 2 mode

DRC1 mode: DRC [1:0]=10 (DRC1=High, and DRC0=Low), the DRC 1 mode is active. The gain is increasing by 12dB compared to the normal mode. The power limit value is the point that active the Dynamic Range Compression function, and the maximum attenuation is -12dB. The attack time is zero second and needs 3.9 seconds to release the non-clip function from -12dB to 0dB.

DRC2 mode: DRC [1:0]=11 (DRC1=High, and DRC0=High), similar to the DRC 1 mode, but not perform the power limit function.

The DRC operation should be switched under power-off or shut down mode to prevent the pop noise between the mode switching.

Stereo/Mono Switching Operation

When connects the RINN and RINP to 3V3REG before power-on, the APA2615 will enter the monaural operational when power-on. In this operation, the output of ROUTP should connect to LOU TP for positive output, and the ROUN should connect to LOU TN for negative output, the input signal will via LINN and LINP to input the APA2615.

This mode can increase more output power compared to the stereo mode single channel's output power.

Multi-APA2615 Synchronization Operation

The external clock synchronization function and the clock output function are prepared and the use of master/slave configuration realizes carrier clock synchronization.

Function Description (Cont.)

Multi-APA2615 Synchronization Operation (Cont.)

When using it with multi chips synchronized, one is used as a master chip and the other is used as a slave chip. At this time, connect OSCO pin of a master chip to OSCI pin of a slave chip. When using 3 pieces of APA2615 (master/slave1/slave2), connect OSCO terminal of a slave1 chip to OSCI pin of a slave2 chip.

Protection Flag Operation

Protection Function	PFLAG Output	Latch	Class-D Output State	Cancellation
DC Detection	Low	Yes	Weak low	Shutdown or Power-Off
UVLO	High-Z	-	Weak low	-
Over Current Protection	Low	Yes	Weak low	Shutdown or Power-Off
Thermal protection (power limit)	-	No	Power limit (-6dB)	Shutdown or Power-Off or Lower temperature
Thermal protection (class-D off)	Low	No	Weak low	Shutdown or Power-Off or Low temperature

DC Detection Operation

When a DC signal applies to the input of APA2615 and the time exceeds 0.5s, APA2615 will turn-off the Class-D output, and the PFLAG pin will pull low. This function protects the speaker to be destroyed by large DC offset. At mute mode, the DC detection function will be disabled. The DC detection state will latch and need power-off or shut down to release the protection.

Connect PFLAG to \overline{SD} pin, the DC detection will be auto recovery.

Over-Current Protection

The APA2615 monitors the output current. When the current exceeds the current-limit threshold, the APA2615 turn-off the output to prevent the IC from being damaged in over-current or short-circuit condition, and the APA2615 will latch at this state until shutdown or power-off to release the over-current protection. PFLAG will pull-high when the protection occurs.

Connect PFLAG to SD pin, the over-current protection will be auto recovery.

Thermal Protection

The thermal protection has two modes to prevent the APA2615 from being destroyed by over temperature.

When the junction temperature exceeds 155°C and under the 165°C, the APA2615 will limit the output power by 6dB to lower the temperature. This calls thermal limit mode. When the junction temperature falls down to 130°C, the thermal limit state will be cancelled.

When junction temperature exceeds 165°C, the Class-D output would turn-off, and the PFLAG pin will pull-low. This calls thermal mute mode. All the state will be cancelled when junction lower than 130°C. Some conditions, like $V_{DD}=5V$, $R_L=4\Omega$, can't meet spec $P_o=14W$ because IC into thermal shutdown. Output power curve use dot line to indicate thermal limit.

Application Information

Square Wave into the Speaker

Apply the square wave into the speaker may cause the voice coil of speaker jump out the air gap and deface the voice coil. However, it depends on the amplitude of square wave is high enough and the bandwidth of speaker is higher than the square wave's frequency. For 500kHz switching frequency, this is not issue for the speaker because the frequency is beyond the audio band, and can't significantly move the voice coil, as cone movement is proportional to $1/f^2$ for frequency out of audio band.

Input Resistance, R_i

The APA2615's input resistor is fixed and the value is 18.8k Ω . The input resistance has wide variation (+/-15%) which is being caused by manufacture.

Input Capacitor, C_i

In the typical application, an input capacitor, C_i , is required to allow the amplifier to bias the input signal to the proper DC level for optimum operation. In this case, C_i and the input impedance R_i form a high-pass filter with the corner frequency determined in the following equation:

$$f_{C(\text{highpass})} = \frac{1}{2\pi R_i C_i} \quad (1)$$

The value of C_i must be considered carefully because it directly affects the low frequency performance of the circuit. Where R_i is 18.8k Ω and the specification calls for a flat bass response down to 40Hz. The equation is reconfigured as below:

$$C_i = \frac{1}{2\pi R_i f_c} \quad (2)$$

When the input resistance variation is considered, the C_i is 0.22 μF , so a value in the range of 0.22 μF to 1.0 μF would be chosen. A further consideration for this capacitor is the leakage path from the input source through the input network ($R_i + R_p, C_i$) to the load.

This leakage current creates a DC offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain applications. For this reason, a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifiers' inputs in most applications because the DC level of the amplifiers' inputs is held at $V_{3V3REG}/2$. Please note that it is important to confirm the capacitor polarity in the application.

Output Low-Pass Filter

If the traces from APA2615 to speaker are short, it doesn't require output filter for FCC & CE standard.

A ferrite bead may need if it's failing the test for FCC or CE tested without the LC filter. The figure 2 is the sample for added ferrite bead; the ferrite shows choosing high impedance in high frequency.

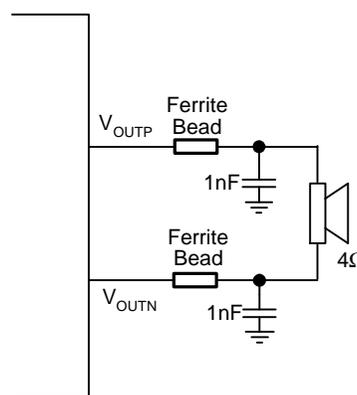


Figure 2. Ferrite bead output filter

Figure 3 and Figure 4 are examples for added the LC filter (Butterworth), it's recommended for the situation that the trace from amplifier to speaker is too long, and needs to eliminate the radiated emission or EMI.

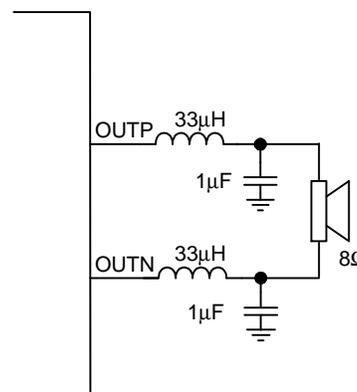


Figure 3. LC output filter for 8 Ω speaker
Inductor : TOKO 11RHBP A7503AY-330M

Application Information (Cont.)

Output Low-Pass Filter (Cont.)

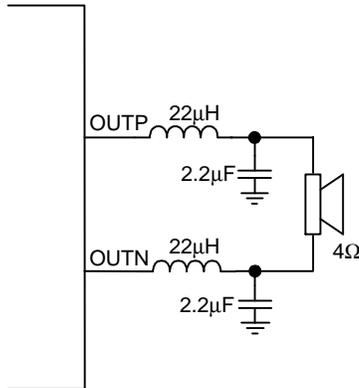


Figure 4. LC output filter for 4Ω speaker
Inductor : TOKO 11RHBP A7503AY-220M

Figure 3 and 4's low pass filter cut-off frequency are 25kHz (F_c).

$$f_{C(\text{lowpass})} = \frac{1}{2\pi\sqrt{LC}} \quad (3)$$

Power-Supply Decoupling Capacitor, C_s

The APA2615 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents the oscillations being caused by long lead length between the amplifier and the speaker.

The optimum decoupling is achieved by using two different types of capacitors that target on different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1μF placed as close as possible to the device AVDD pin and 1mF placed to the LPVDD and RPVDD leads for works best. For filtering lower frequency noise signals, a large aluminum electrolytic capacitor of 220μF or greater placed near the audio power amplifier is recommended.

Layout Recommendation

In high power Class-D power amplifier, a correct layout is important to ensure proper operation of the amplifier and avoid the switch noise radiation. In general, interconnecting impedance should be minimized by using short and wide printed circuit traces. Especial for the high slew rate output PWM signal to speaker, these loops should be as small as possible.

1. All components should be placed close to the APA2615. For example, the input capacitor (C_i) should be close to APA2615's input pins to avoid causing noise coupling to APA2615's high impedance inputs; the decoupling capacitor (C_s) should be placed by the APA2615's power pin to decouple the power rail noise.
2. The output traces should be short, wide, (>50mil) and symmetric, and this loop like the figure 5, should be as small as possible, (this loop is high slew rate and high current path).

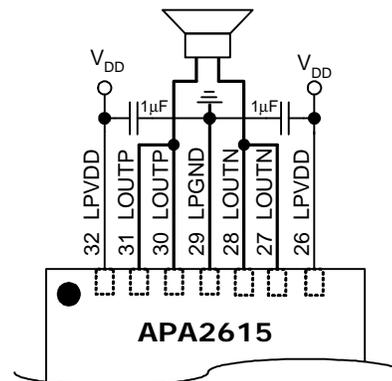


Figure 5. APA2615 Output Topology

3. The input trace should be short and symmetric.
4. The power trace width should greater than 50mil.
5. The QFN5.2x6.2-32 Thermal PAD should be soldered on PCB, and the ground plane needs soldered mask (to avoid short circuit) except the Thermal PAD area. Like the figure 6 illustrate.

Application Information (Cont.)

Layout Recommendation (Cont.)

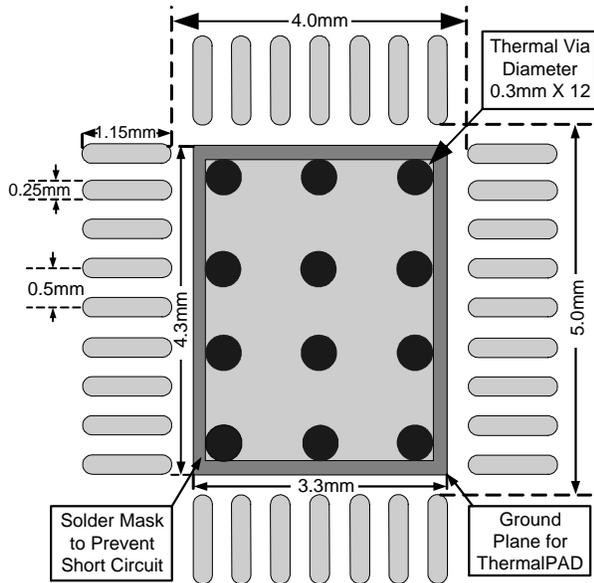
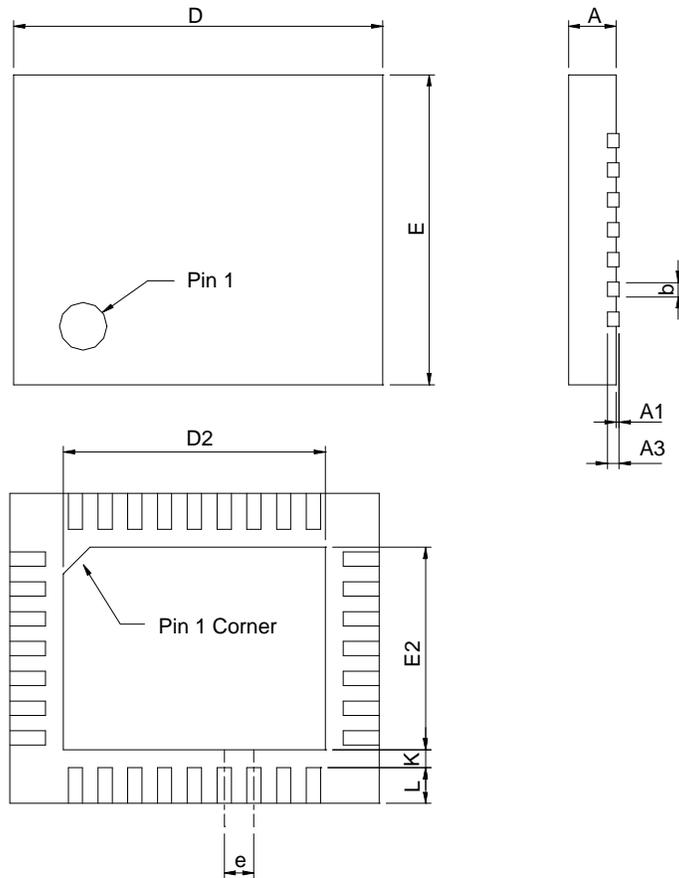


Figure 6. QFN5.2x6.2-32 Land Pattern Recommendation

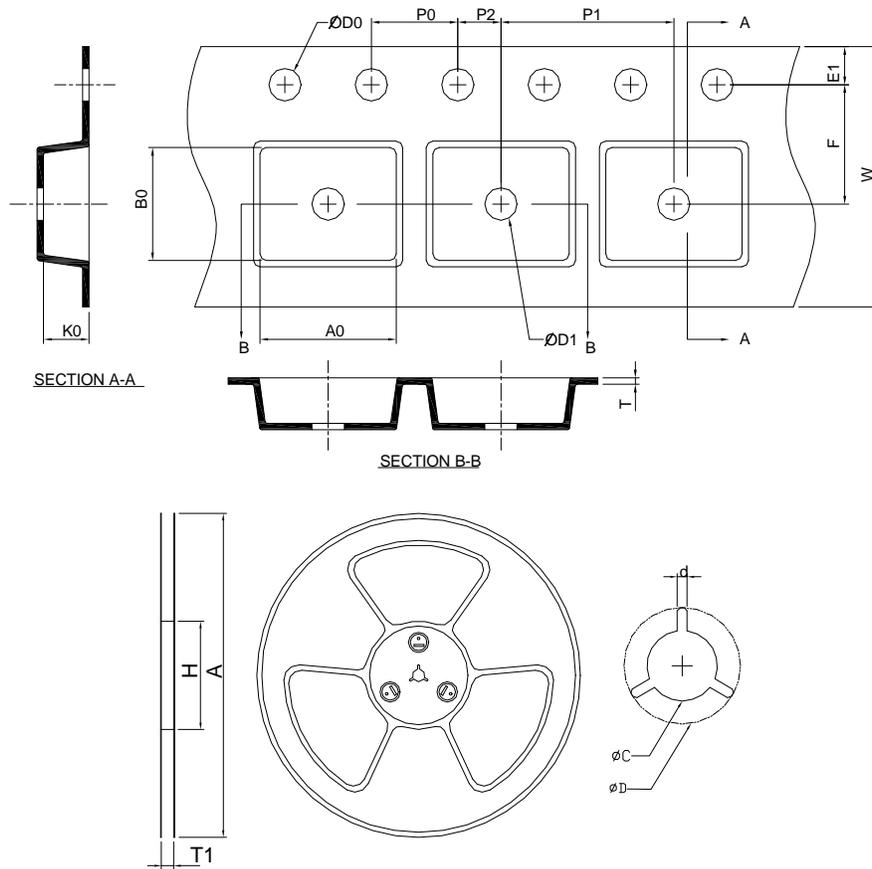
Package Information

QFN5.2x6.2-32



SYMBOL	QFN5.2x6.2-32			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.80	1.00	0.031	0.039
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.18	0.30	0.007	0.012
D	6.10	6.30	0.240	0.248
D2	4.20	4.60	0.165	0.181
E	5.10	5.30	0.201	0.209
E2	3.20	3.60	0.126	0.142
e	0.50 BSC		0.020 BSC	
L	0.50	0.70	0.020	0.028
K	0.20		0.008	

Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
QFN5.2x6.2-32	330.0 ±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0 ±0.30	1.75 ±0.10	5.5 ±0.10
	P0	P1	P2	D0	D1	T	A0	B0	K0
	4.0 ±0.10	8.0 ±0.10	2.0 ±0.10	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	5.60 ±0.20	6.6 ±0.20	1.30 ±0.20

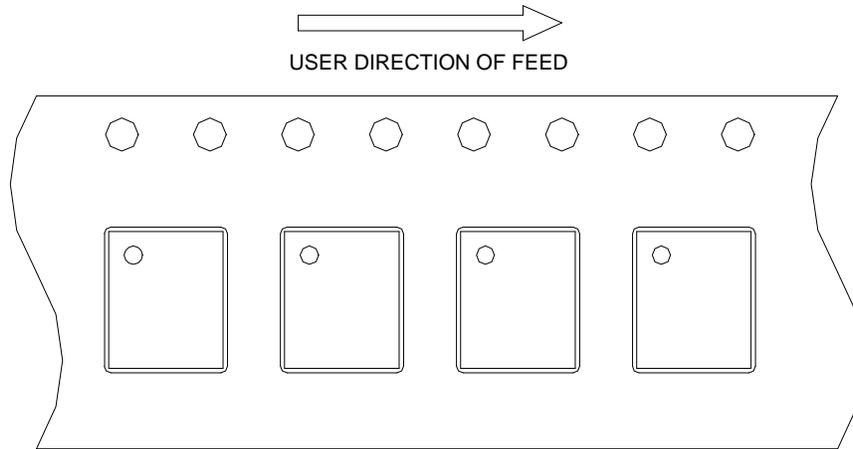
(mm)

Devices Per Unit

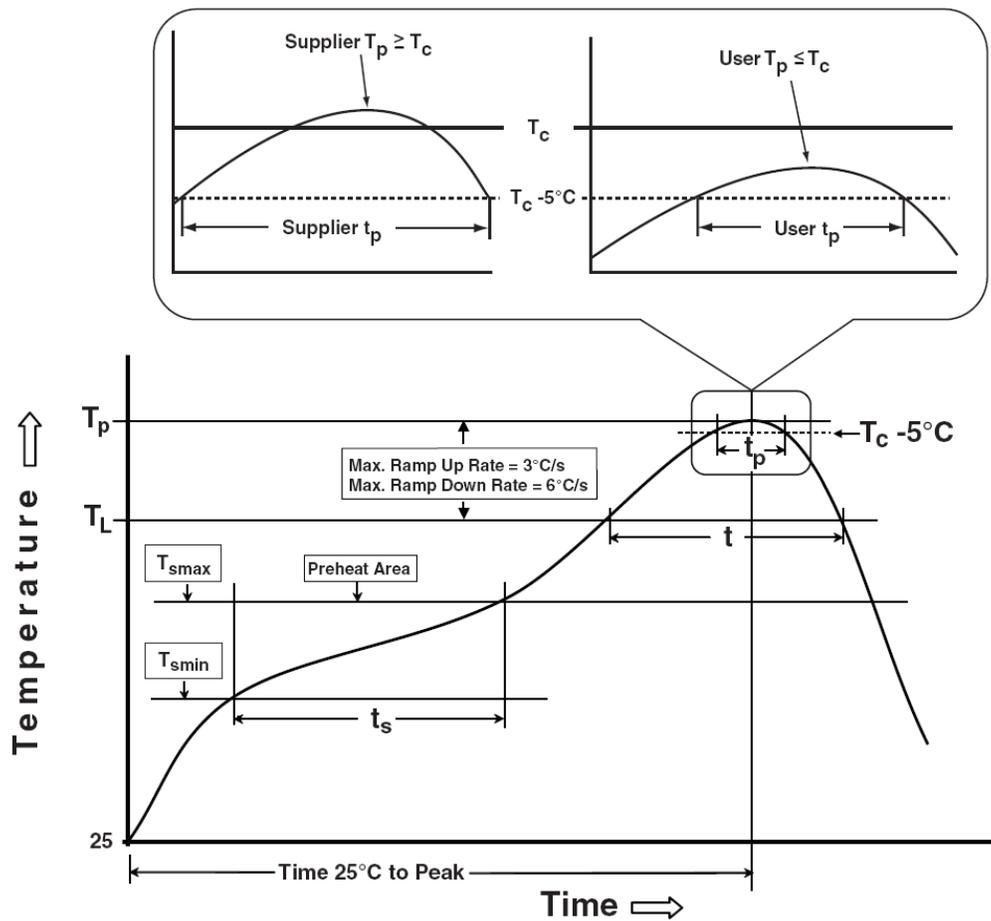
Package Type	Unit	Quantity
QFN5.2x6.2-32	Tape & Reel	2500

Taping Direction Information

QFN5.2x6.2-32



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	100 °C 150 °C 60-120 seconds	150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_p)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_p)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Table 1. SnPb Eutectic Process – Classification Temperatures (T_c)

Package Thickness	Volume mm ³ <350	Volume mm ³ ≥350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (T_c)

Package Thickness	Volume mm ³ <350	Volume mm ³ 350-2000	Volume mm ³ >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ $T_j=125^\circ\text{C}$
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM 2KV
MM	JESD-22, A115	VMM 200V
Latch-Up	JESD 78	10ms, 1 _{tr} 100mA

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