6W Stereo Class-D Audio Power Amplifier

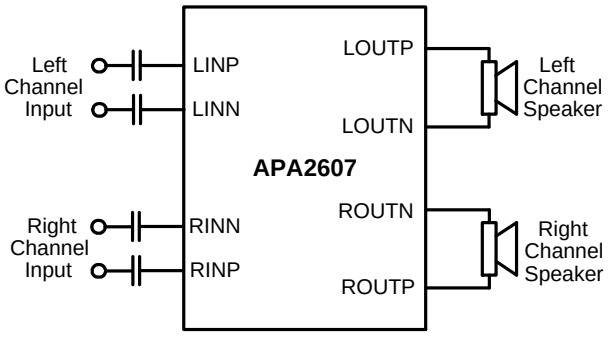
Features

- **Operating Voltage: 8.0V-16.5V**
- **High Efficiency 90% at P_O = 6W, 8Ω Speaker, V_{DD} = 12V**
- **Low Shutdown Current**
  - I_{DD}=5μA at V_{DD}=16.5V
- **Power Limit Function**
- **Switchable Non-Clip Function/DRC (Dynamic Range Control) Function**
- **Build-in Oscillator**
- **Spread Clock Function**
- **External Synchronization Function**
- **Master/Slaver Synchronization Function**
- **DC Detection Function**
- **Stereo/Monaural Function**
- **Shutdown and Mute Function**
- **Thermal and Over-Current Protections with Auto-Recovery**
- **Space Saving Package TQFN5x5-32**
- **Lead Free and Green Devices Available (RoHS Compliant)**

Applications

- **LCD TVs**

Simplified Application Circuit

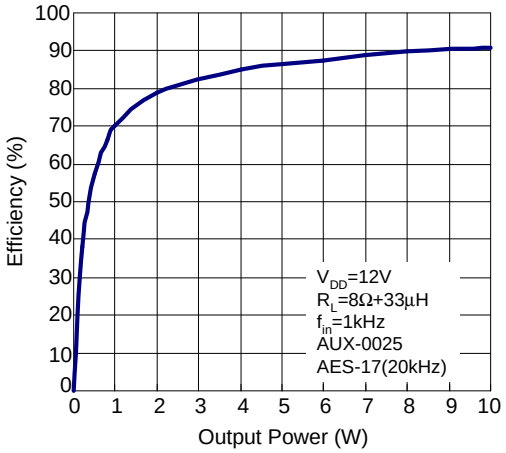


General Description

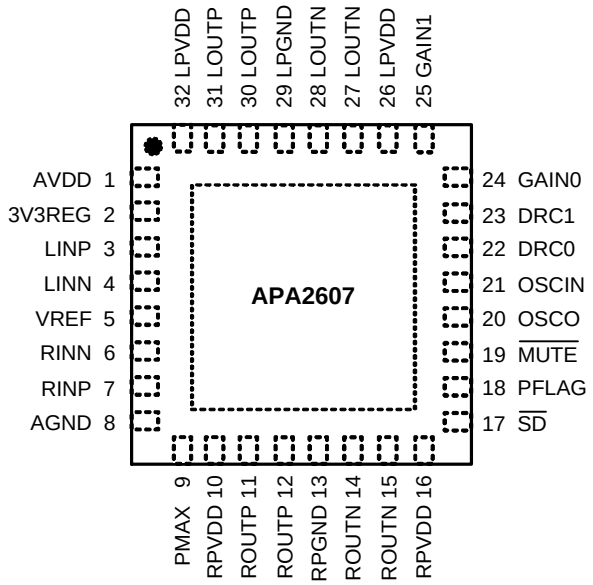
The APA2607 is a stereo, high efficiency, Class-D audio amplifier available in a TQFN5x5-32 package.

The filter-free Class-D architecture eliminates the external low pass filters and saves the PCB space and BOM costs. The APA2607 also has spread clock function that reduces the high frequency radiation and low the EMI noise. The Zero-crossing-change function changes the gain when both output (V_{OUTP} and V_{OUTN}) crossing together can minimum the pop noise. The power limit function can protect the speaker when output signal excesses the speaker limit rating. The non-clip and DRC functions eliminate the distortion at large input signal and can fit the high dynamic input signal to a small dynamic speaker. The operating voltage is from 8V to 16.5V. The APA2607 is capable of driving 6W at 12V into 8Ω speaker and provides thermal and over-current protections. The APA2607 also can detect the DC that prevents the speaker voice coil being destroyed.

Efficiency vs. Output Power (8W)



Pin Configuration



TQFN5x5-32
(Top View)

Ordering and Marking Information

APA2607 □□□-□□ □ Assembly Material Handling Code Temperature Range Package Code	Package Code QB : TQFN5x5-32 Operating Ambient Temperature Range I : -40 to 85 °C Handling Code TR : Tape & Reel Assembly Material G : Halogen and Lead Free Device
APA2607 QB: 	XXXXX - Date Code

Note : ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines “Green” to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Rating	Unit
V_{DD}	Supply Voltage (RPVDD to RPGND, LPVDD to LPGND, AVDD to AGND)	-0.3 to 20	V
$V_{\overline{SD}}$	Input Voltage ($\overline{SD}$ to AGND)	-0.3 to 20	
V_{IN}	Input Voltage (LINN, LINP, RINN and RINP to AGND)	-0.3 to 4	
$V_{CONTROL}$	Input Voltage ($\overline{MUTE}$, PMAX, DRC0, DRC1, GAIN0 and GAIN1 to AGND)	-0.3 to 4	
V_{PGND_AGND}	Input Voltage (LPGND, RPGND to AGND)	-0.3 to +0.3	
T_J	Maximum Junction Temperature	150	°C
T_{STG}	Storage Temperature Range	-65 to +150	°C
T_{SDR}	Maximum Soldering Temperature Range, 10 Seconds	260	°C
P_D	Power Dissipation	Internally Limited	W

Note1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Junction-to-Ambient Resistance in Free Air (Note 2) TQFN5x5-32	28	°C/W
θ_{JC}	Junction-to-Case Resistance in Free Air (Note 3) TQFN5x5-32	6	°C/W

Note 2: θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. The exposed pad of TQFN5X5-32 is soldered directly on the PCB.

Note 3: The case temperature is measured at the center of the exposed pad on the underside of the TQFN5X5-32 package.

Recommended Operating Conditions (Note 4)

Symbol	Parameter		Range		Unit
			Min.	Max.	
V_{DD}	Supply Voltage		8.0	16.5	V
V_{IH}	High Level Threshold Voltage	$\overline{SD}$	2.5	16.5	
		$\overline{MUTE}$, PMAX, DRC0, DRC1, GAIN0, GAIN1	2.5	3.6	
V_{IL}	Low Level Threshold Voltage	$\overline{SD}$	0	1	
		$\overline{MUTE}$, PMAX, DRC0, DRC1, GAIN0, GAIN1	0	1	
V_{IC}	Common Mode Input Voltage		-	3	
T_A	Ambient Temperature Range		-40	85	°C
T_J	Junction Temperature Range		-40	125	
R_L	Speaker Resistance		3.5	-	Ω

Note 4: At stereo mode, if the R_L=4Ω, the V_{DD} should not excess 12V or it may trigger the Over-Current Protection.

Electrical Characteristics

V_{DD}=12V, GND=0V, T_A=25°C (unless otherwise noted)

Symbol	Parameter	Test Conditions	APA2607			Unit
			Min.	Typ.	Max.	
V_{3V3REG}		I_O=2mA	2.85	3.3	3.75	V
V_{VREF}			-	V_{3V3REG}/2	-	
V_{DET}	The DC Detection Active Voltage at Output	DC detection (>0.5s)	-	2	2.5	
V_{FLAG}	Protection Flag Output Voltage	$I_{SOUCING}$=0.4mA	-	-	0.4	
V_{OSCO}	Oscillator Output Voltage	$I_{SINKING}$=$I_{SOUCING}$=4mA	2.2	-	-	V_{PP}
$T_{\overline{SD}}$	Recovery Time from Shutdown	C_5=0.1µF	-	1	1.5	s
T_{MUTE}	Recovery Time from Mute		-	-	0.001	
I_{DD}	Supply Current	No Load	-	18	36	mA
I_{MUTE}	Mute Current		-	2	10	
I_{SD}	Shutdown Current	$\overline{SD}$ = 0V	-	5	100	µA
II	Input Current	$\overline{SD}$, $\overline{MUTE}$, DRC0, DRC1, GAIN0, GAIN1	-	-	5	
F_{OSC}	Internal Oscillator Frequency		400	500	600	kHz
F_{OSCI}	External Clock at OSCI Pin		400	500	600	
DT_{OSCI}	Duty Cycle of External Clock		40	-	60	%
R_{DSON}	Static Drain-Source On-State Resistance (P-Channel and N-Channel Power MOSFET)	V_{DD}=8V, I_L=0.8A	-	530	-	mΩ
		V_{DD}=12V, I_L=1A	-	480	-	
		V_{DD}=16V, I_L=1.4A	-	440	-	
R_i	Input Resistor	RINN, RINP, LINN, LINP (Gain independent)	-	10	-	kΩ
R_O	Output Resistor	ROUTN, ROUTP, LOUTN, LOUTP	-	300	-	
η	Efficiency	Stereo, R_L=8Ω, P_O=6W	-	89	-	%
A_V	Closed-Loop Gain	DRC [1:0] (0,0), GAIN (0,0)	-	22	-	dB
		DRC (0,0), GAIN (0,1)	-	28	-	
		DRC (0,0), GAIN (1,0)	-	34	-	
		DRC (0,0), GAIN (1,1)	-	16	-	
		DRC (0,1), GAIN (0,0)	-	34	-	
		DRC (0,1), GAIN (0,1)	-	40	-	
		DRC (0,1), GAIN (1,0)	-	46	-	
		DRC (0,1), GAIN (1,1)	-	28	-	
		DRC (1,0), GAIN (0,0)	-	34	-	
		DRC (1,0), GAIN (0,1)	-	40	-	
		DRC (1,0), GAIN (1,0)	-	46	-	
		DRC (1,0), GAIN (1,1)	-	28	-	
		DRC (1,1), GAIN (0,0)	-	34	-	
		DRC (1,1), GAIN (0,1)	-	40	-	

Electrical Characteristics (Cont.)

V_{DD}=12V, GND=0V, T_A=25°C (unless otherwise noted)

Symbol	Parameter	Test Conditions	APA2607			Unit
			Min.	Typ.	Max.	
A_V	Closed-Loop Gain	DRC (1,1), GAIN (1,0)	-	46	-	dB
		DRC (1,1), GAIN (1,1)	-	28	-	

Stereo Mode

Symbol	Parameter	Test Conditions		APA2607			Unit
				Min.	Typ.	Max.	
V_{DD}=16V, T_A=25°C							
P_O	Output Power	THD+N=1% f_{in}=1kHz	R_L=8Ω	-	12	-	W
		THD+N=10% f_{in}=1kHz	R_L=8Ω	-	15	-	
THD+N	Total Harmonic Distortion Pulse Noise	f_{in}=1kHz	R_L=8Ω, P_O=6W	-	0.07	0.1	%
Crosstalk	Channel Separation	P_O=0.5W, R_L=8Ω,f_{in}=1kHz		-	-70	-60	dB
PSRR	Power Supply Rejection Ratio	R_L=8Ω	f_{in}=100Hz	-	-65	-55	
			f_{in}=1kHz	-	-65	-55	
CMRR	Common Mode Rejection Ration	f_{in}=1kHz, R_L=8Ω,V_{in}=0.1Vpp		-	-65	-55	
Att_{Mute}	Mute Attenuation	f_{in}=1kHz, R_L=8Ω,V_{in}=1Vpp		-	-115	-100	
$Att_{shutdown}$	Shutdown Attenuation	f_{in}=1kHz, R_L=8Ω, V_{in}=1Vpp		-	-115	-100	
V_{OS}	Offset Voltage	No load, A_v=22dB		-	-	20	mV
V_n	Noise Output Voltage	With A-weighted Filter (A_v=22dB)		-	230	500	μVrms
V_{DD}=12V, T_A=25°C							
P_O	Output Power	THD+N=1% f_{in}=1kHz	R_L=4Ω	-	10	-	W
			R_L=8Ω	-	6	-	
		THD+N=10% f_{in}=1kHz	R_L=4Ω	-	14	-	
			R_L=8Ω	-	8	-	
THD+N	Total Harmonic Distortion Pulse Noise	f_{in}=1kHz	R_L=4Ω, P_O=7W	-	0.07	0.1	%
			R_L=8Ω, P_O=4.5W	-	0.07	0.1	
Crosstalk	Channel Separation	P_O=0.5W, R_L=8Ω, f_{in}=1kHz		-	-70	-60	dB
PSRR	Power Supply Rejection Ratio	R_L=8Ω	f_{in}=100Hz	-	-65	-55	
			f_{in}=1kHz	-	-65	-55	
CMRR	Common Mode Rejection Ration	f_{in}=1kHz, R_L=8Ω, V_{IN}=0.1V_{pp}, A_V=22dB		-	-65	-55	
Att_{Mute}	Mute Attenuation	f_{in}=1kHz, R_L=8Ω, V_{IN}=1V_{pp}		-	-115	-100	
$Att_{shutdown}$	Shutdown Attenuation	f_{in}=1kHz, R_L=8Ω, V_{IN}=1V_{pp}		-	-115	-100	
V_{OS}	Offset Voltage	No load, A_V=22dB		-	-	20	mV
V_n	Noise Output Voltage	With A-weighting Filter (A_V=22dB)		-	230	500	μVrms

Electrical Characteristics (Cont.)

V_{DD}=12V, GND=0V, T_A=25°C (unless otherwise noted)

Stereo Mode (Cont.)

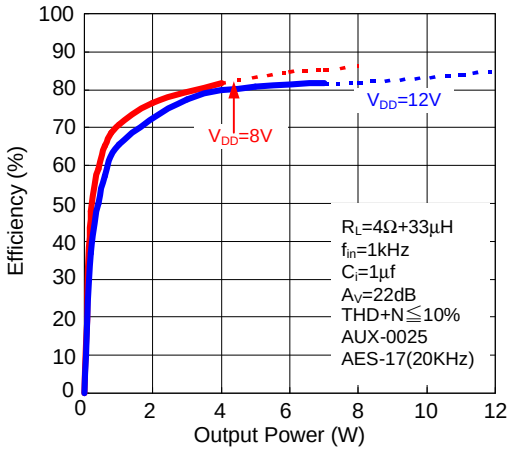
Symbol	Parameter	Test Conditions		APA2607			Unit
				Min.	Typ.	Max.	
V_{DD}=8V, T_A=25°C							
P_O	Output Power	THD+N=1% f_{in}=1kHz	R_L=4Ω	-	5.5	-	W
			R_L=8Ω	-	3.2	-	
		THD+N=10% f_{in}=1kHz	R_L=4Ω	-	7	-	
			R_L=8Ω	-	4	-	
THD+N	Total Harmonic Distortion Pulse Noise	f_{in}=1kHz	R_L=4Ω, P_O=4.5W	-	0.1	0.2	%
			R_L=8Ω, P_O=2.5W	-	0.1	0.2	
Crosstalk	Channel Separation	P_O=0.5W, R_L=8Ω, f_{in}=1kHz		-	-60	-60	dB
PSRR	Power Supply Rejection Ratio	R_L=8Ω	f_{in}=100Hz	-	-65	-55	
			f_{in}=1kHz	-	-65	-55	
CMRR	Common Mode Rejection Ration	f_{in}=1kHz, R_L=8Ω, V_{IN}=0.1V_{pp}, A_V=22dB		-	-70	-55	
Att_{Mute}	Mute Attenuation	f_{in}=1kHz, R_L=8Ω, V_{IN}=1V_{pp}		-	-115	-100	
$Att_{shutdown}$	Shutdown Attenuation	f_{in}=1kHz, R_L=8Ω, V_{IN}=1V_{pp}		-	-115	-100	
V_{OS}	Offset Voltage	No load, A_V=22dB		-	-	20	mV
V_n	Noise Output Voltage	With A-weighting Filter (A_V=22dB)		-	200	400	μVrms

MONO Mode

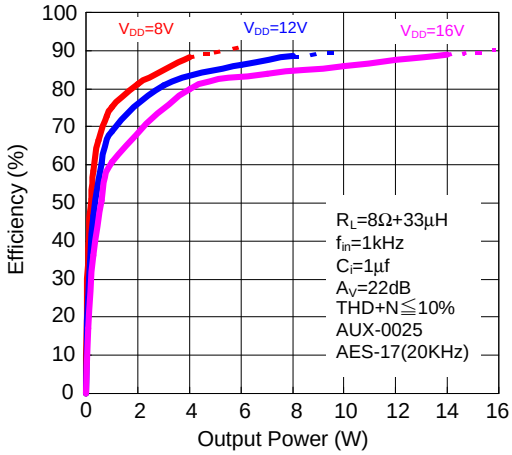
Symbol	Parameter	Test Conditions		APA2607			Unit
				Min.	Typ.	Max.	
V_{DD}=12V, T_A=25°C							
P_O	Output Power	THD+N=1% f_{in}=1kHz	R_L=4Ω	-	12	-	W
		THD+N=10% f_{in}=1kHz	R_L=4Ω	-	14	-	
THD+N	Total Harmonic Distortion Pulse Noise	f_{in}=1kHz	R_L=4Ω P_O=8W	-	0.08	0.2	%
PSRR	Power Supply Rejection Ratio	R_L=8Ω	f_{in}=100Hz	-	-65	-55	dB
			f_{in}=1kHz	-	-65	-55	
CMRR	Common Mode Rejection Ration	f_{in}=1kHz, R_L=8Ω, V_{IN}=0.1V_{pp}, A_V=22dB		-	-60	-55	
Att_{Mute}	Mute Attenuation	f_{in}=1kHz, R_L=8Ω, V_{IN}=1Vrms		-	-115	-100	
$Att_{shutdown}$	Shutdown Attenuation	f_{in}=1kHz, R_L=8Ω, V_{IN}=1Vrms		-	-115	-100	
V_{OS}	Offset Voltage	No load, A_V=22dB		-	-	20	mV
V_n	Noise Output Voltage	With A-weighting Filter (A_V=22dB)		-	200	400	μVrms

Typical Operating Characteristics

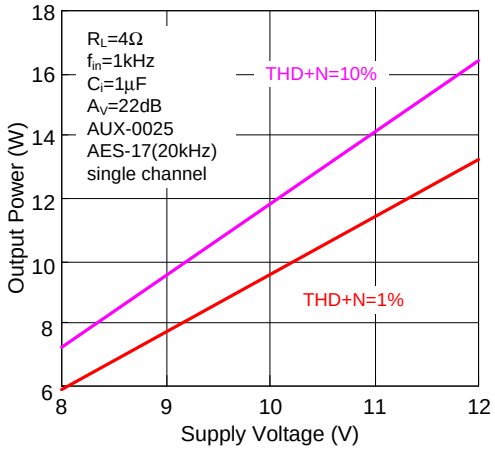
Efficiency vs. Output Power (4W)



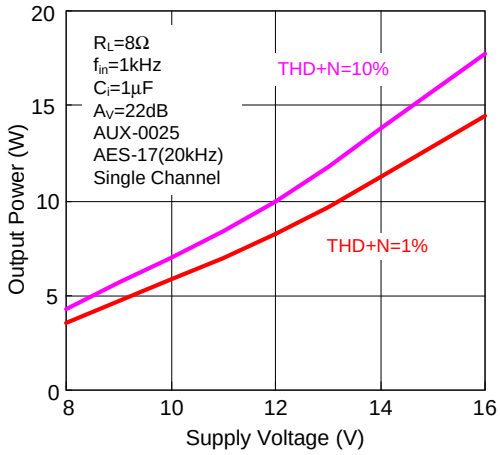
Efficiency vs. Output Power (8W)



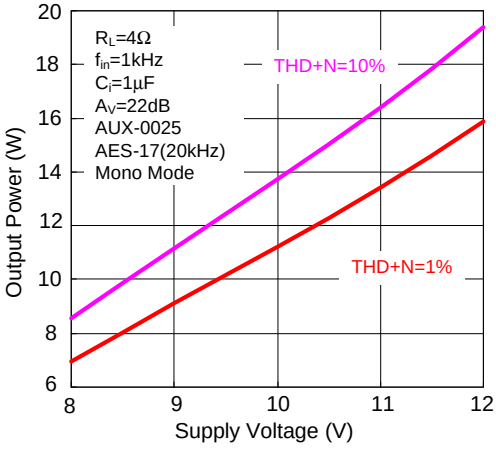
Output Power vs. Supply Voltage



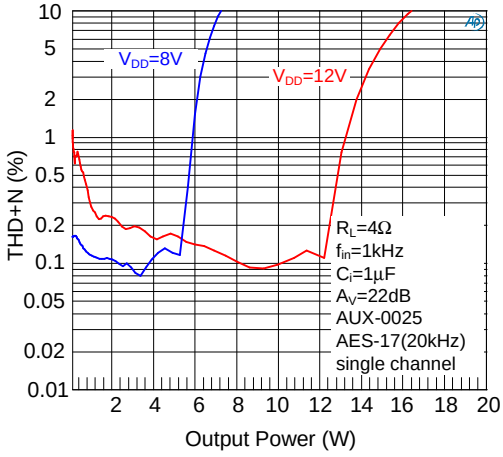
Output Power vs. Supply Voltage



Output Power vs. Supply Voltage (Mono Mode)

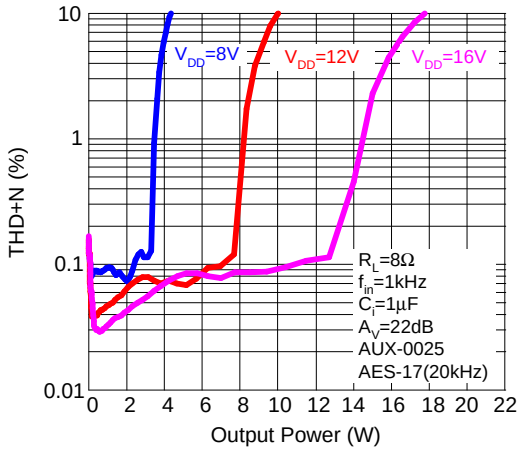


THD+N vs. Output Power

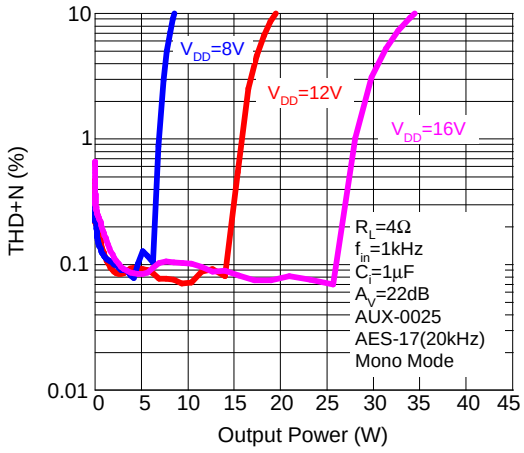


Typical Operating Characteristics (Cont.)

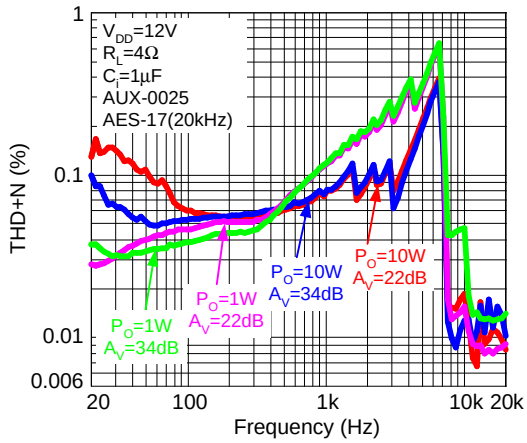
THD+N vs. Output Power



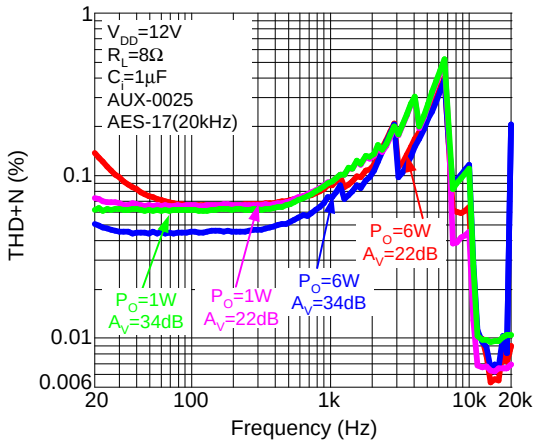
THD+N vs. Output Power



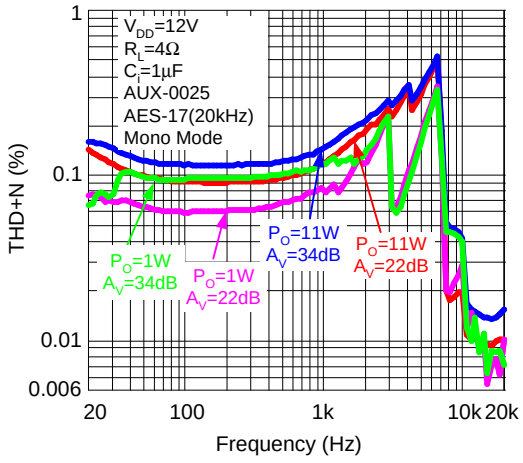
THD+N vs. Frequency



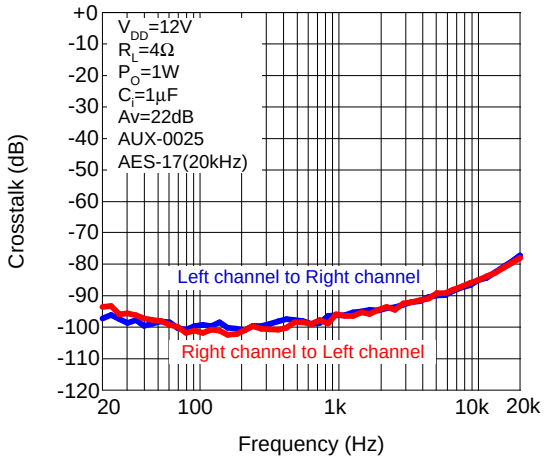
THD+N vs. Frequency



THD+N vs. Frequency

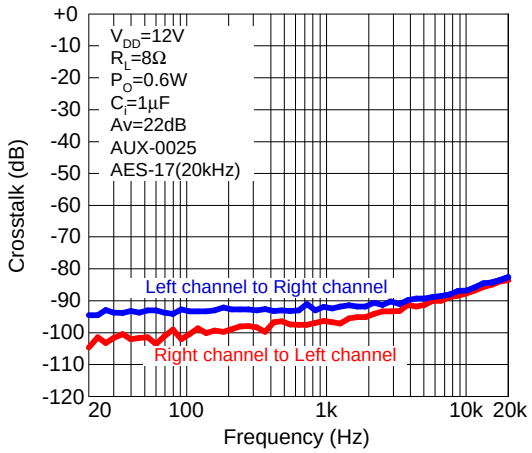


Crosstalk vs. Frequency

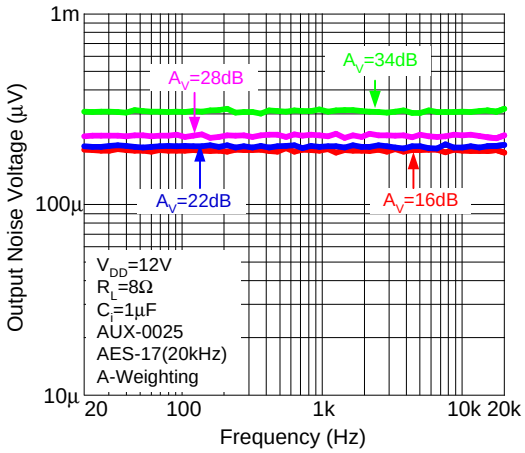


Typical Operating Characteristics (Cont.)

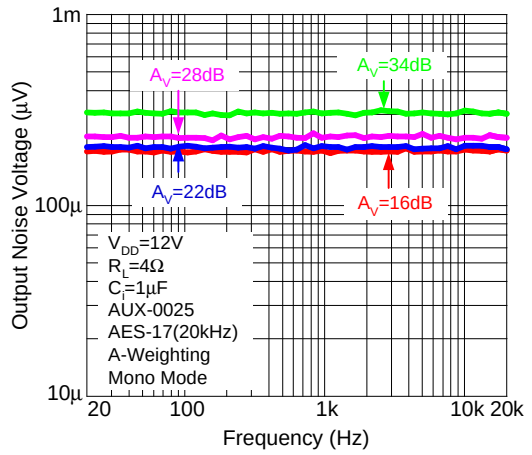
Crosstalk vs. Frequency



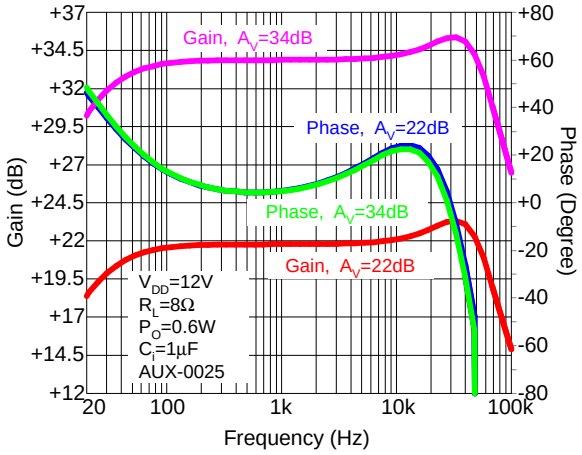
Output Noise Voltage vs. Frequency



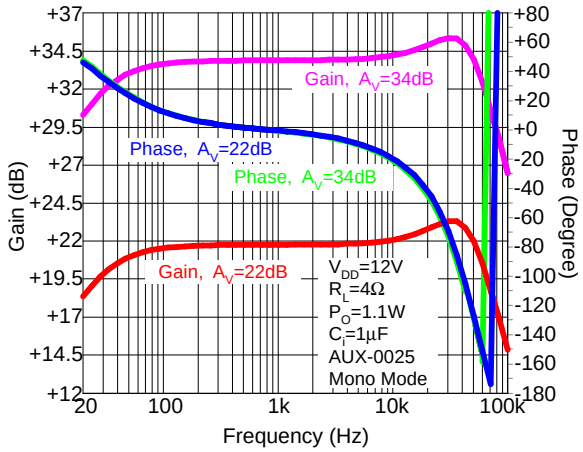
Output Noise Voltage vs. Frequency



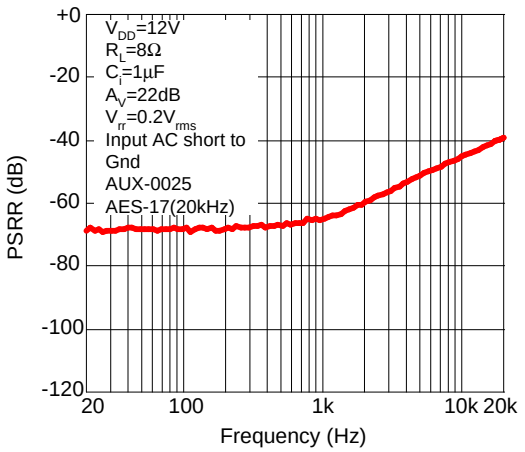
Frequency Response



Frequency Response

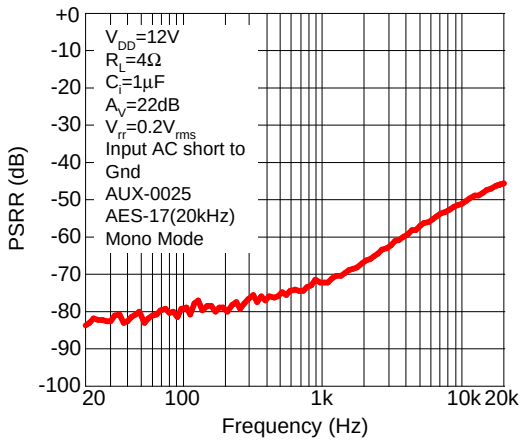


PSRR vs. Frequency

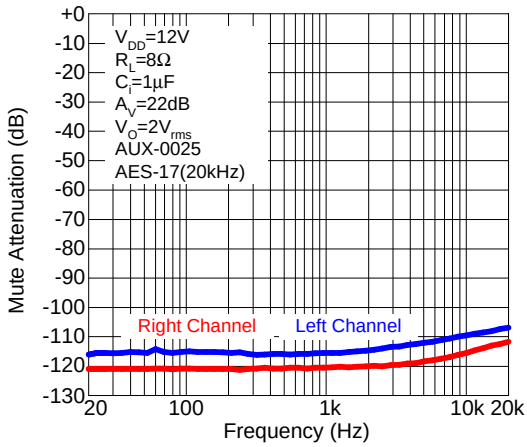


Typical Operating Characteristics (Cont.)

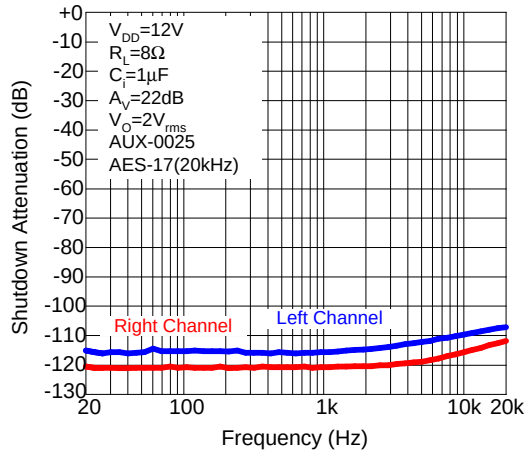
PSRR vs. Frequency



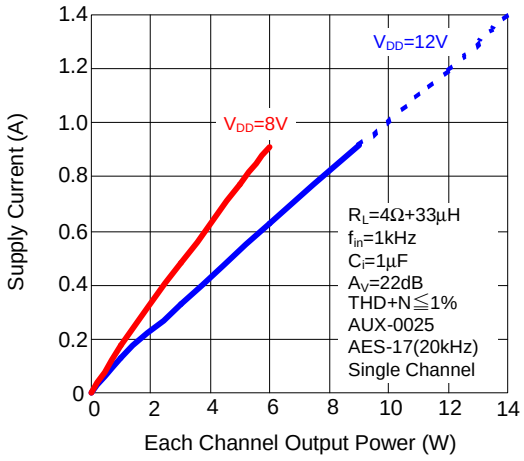
Mute Attenuation vs. Frequency



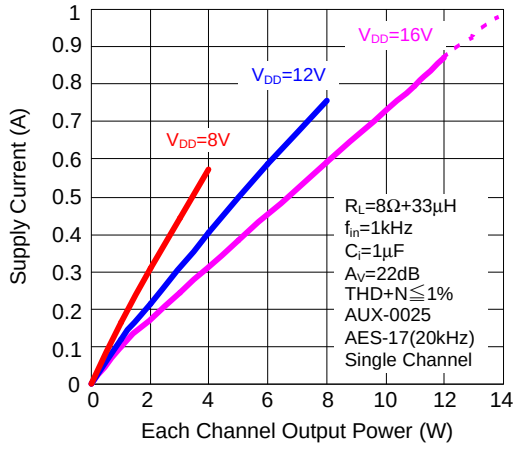
Shutdown Attenuation vs. Frequency



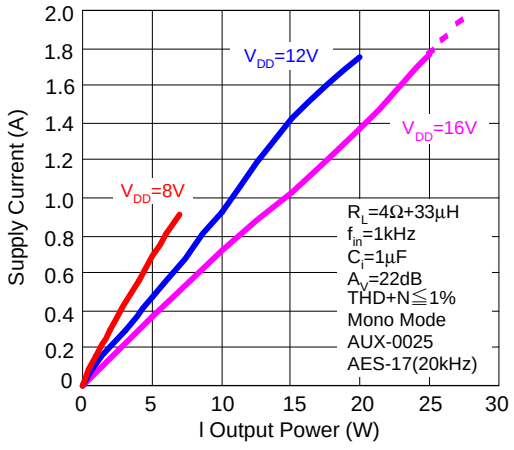
Supply Current vs. Output Power



Supply Current vs. Output Power

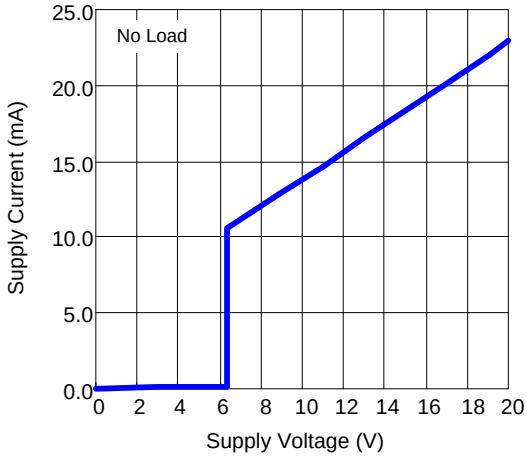


Supply Current vs. Output Power

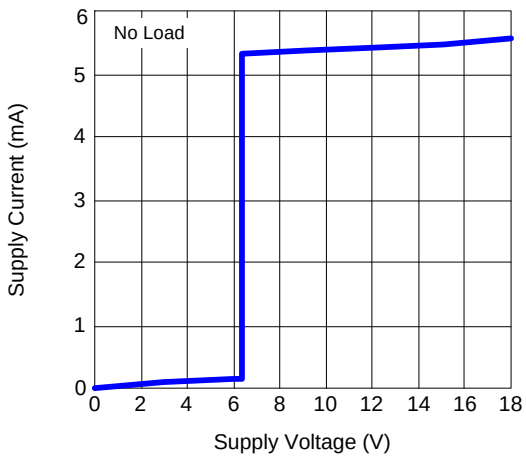


Typical Operating Characteristics (Cont.)

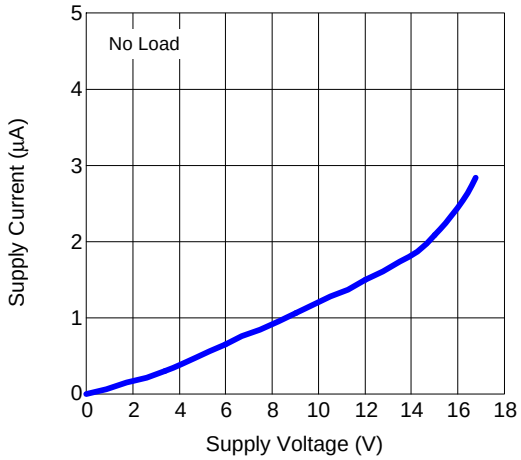
Supply Current vs. Supply Voltage



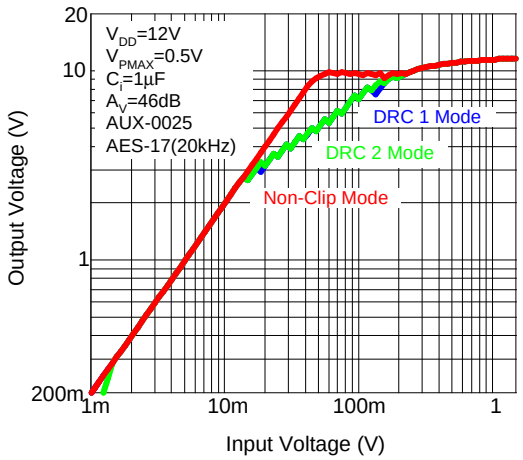
Mute Current vs. Supply Voltage



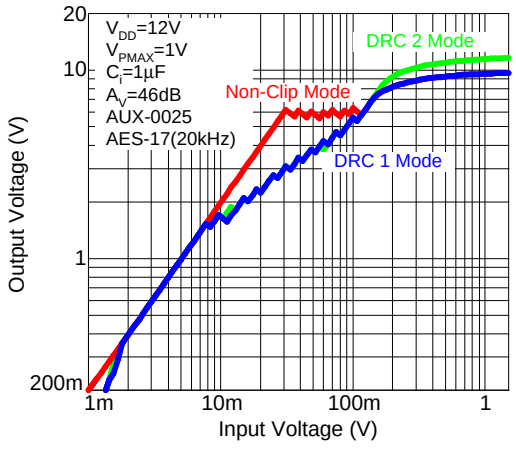
Shutdown Current vs. Supply Voltage



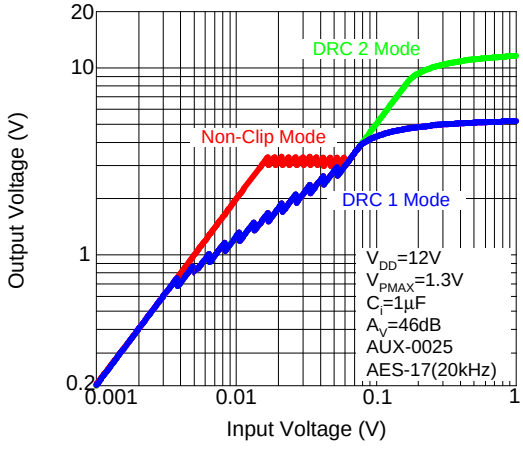
Input Voltage vs. Output Voltage



Input Voltage vs. Output Voltage



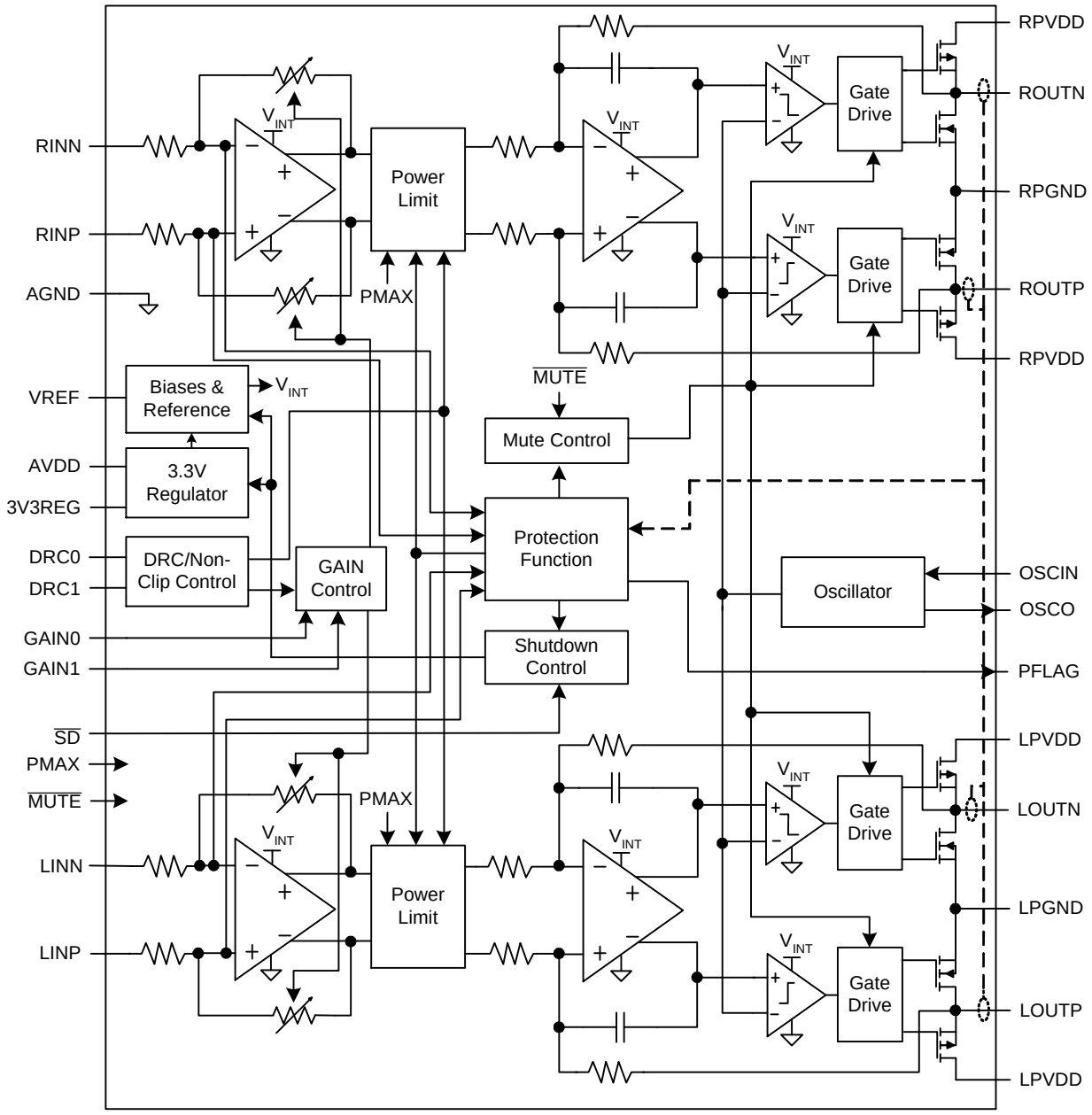
Input Voltage vs. Output Voltage



Pin Description

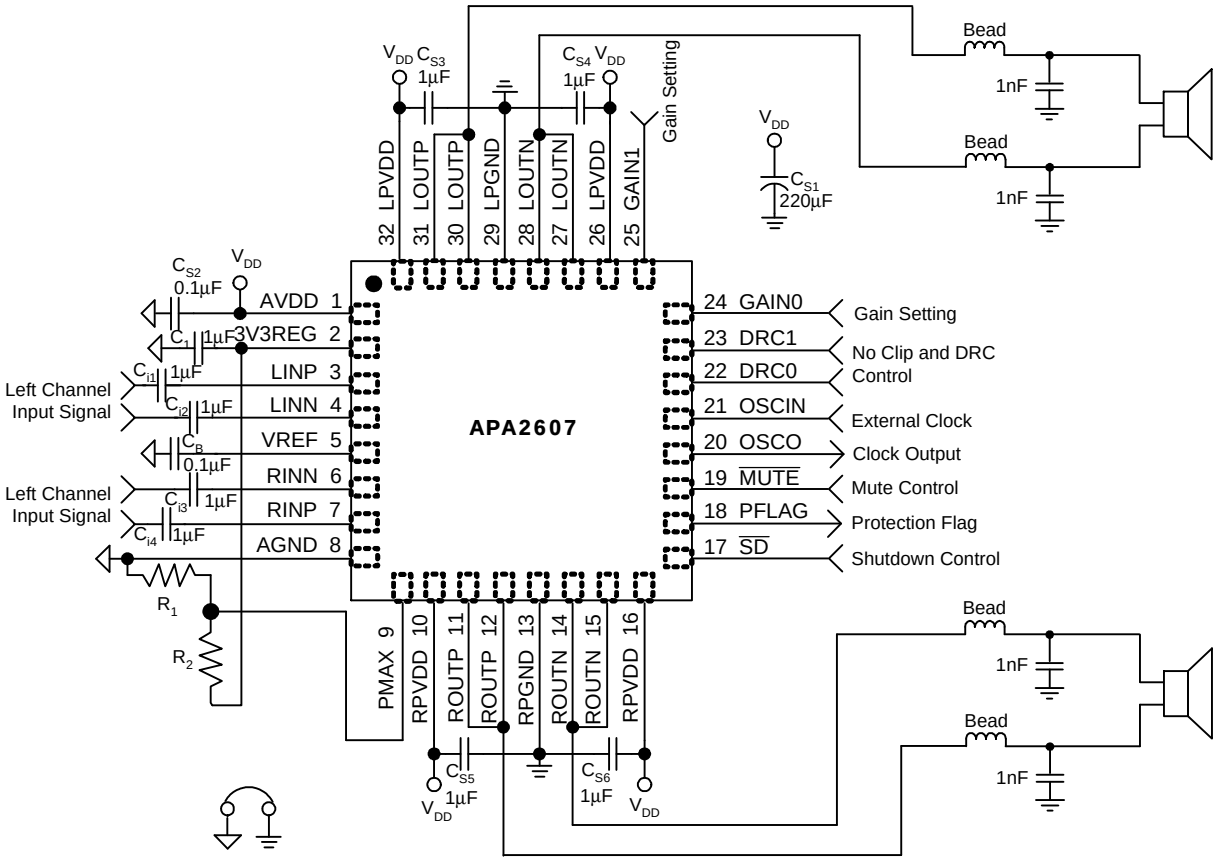
PIN		I/O/P	FUNCTION
NO.	NAME		
1	AVDD	P	Power supply for control block.
2	3V3REG	O	Regulator output, 3.3V.
3	LINP	I	The positive input of left channel amplifier.
4	LINN	I	The negative input of left channel amplifier.
5	VREF	P	The reference voltage output.
6	RINN	I	The negative input of right channel amplifier.
7	RINP	I	The positive input of right channel amplifier.
8	AGND	P	Ground connection for control block.
9	PMAX	I	Input for set the power limit function.
10,16	RPVDD	P	The power supply for right channel Class-D amplifier.
11,12	ROUTP	O	The positive output of right channel Class-D amplifier.
13	RPGND	P	Ground connection for right channel Class-D amplifier.
14,15	ROUTN	O	The negative output of right channel Class-D amplifier.
17	$\overline{SD}$	I	Shutdown mode control input, place entire IC in shutdown mode when held low.
18	PFLAG	O	Protection flag output.
19	$\overline{MUTE}$	I	Mute mode control input; pull low to mute the Class-D amplifier's output.
20	OSCO	O	The internal oscillator's output, for synchronization other APA2607s.
21	OSCIN	I	External clock input.
22	DRC0	I	Non-clip and DRC (Dynamic Range Compress) control; LSB bit 0.
23	DRC1	I	Non-clip and DRC (Dynamic Range Compress) control; MSB bit 1.
24	GAIN0	I	Control pin for internal gain setting, LSB, bit0.
25	GAIN1	I	Control pin for internal gain setting, MSB, bit1.
26,32	LPVDD	P	The power supply for left channel Class-D amplifier.
27,28	LOUTN	O	The negative output of left channel Class-D amplifier.
29	LPGND	P	Ground connection for left channel Class-D amplifier.
30,31	LOUTP	O	The positive output of left channel Class-D amplifier.

Block Diagram



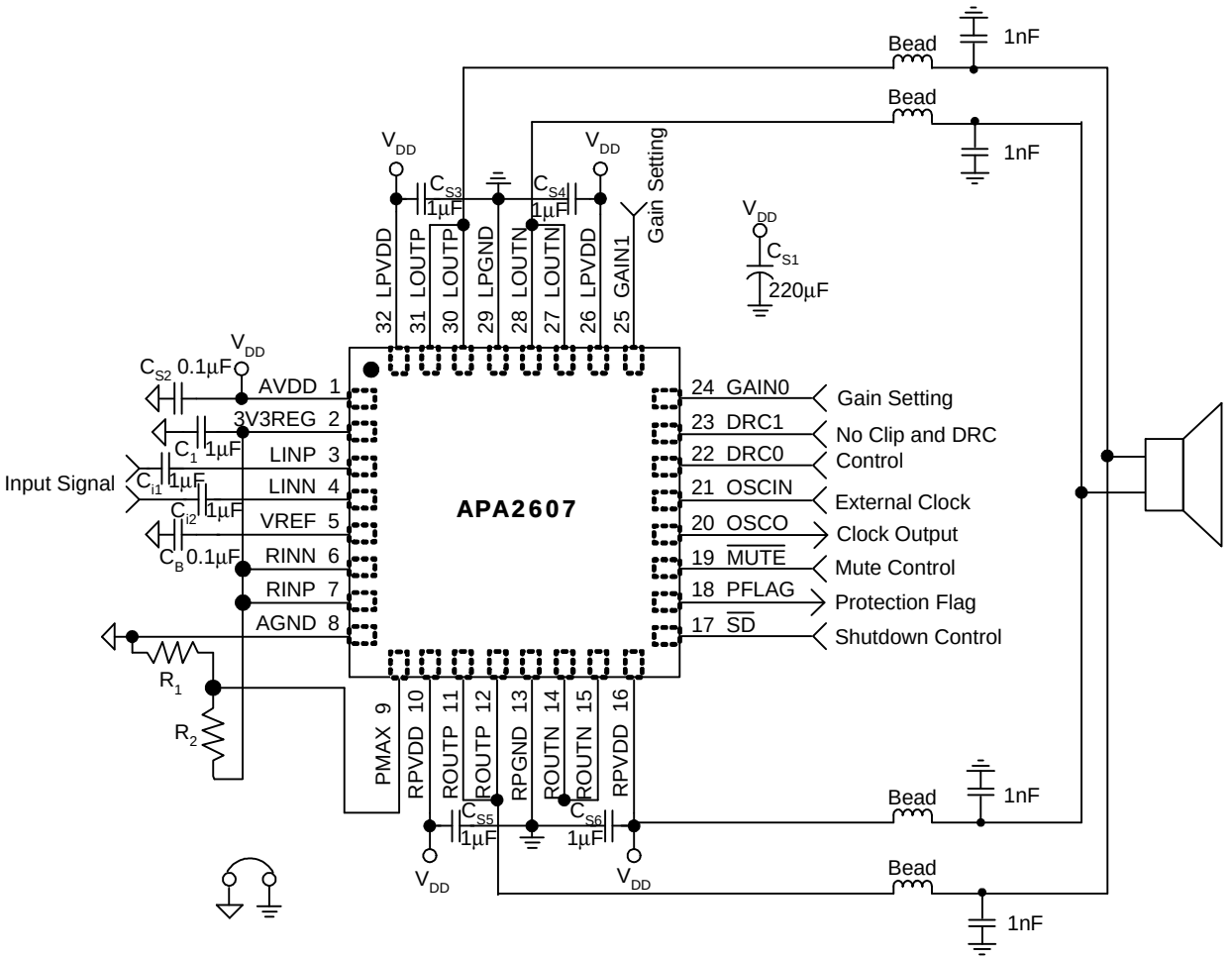
Typical Application Circuit

Stereo Operation



Typical Application Circuit (Cont.)

Monaural Operation



Function Description

Class-D Operation

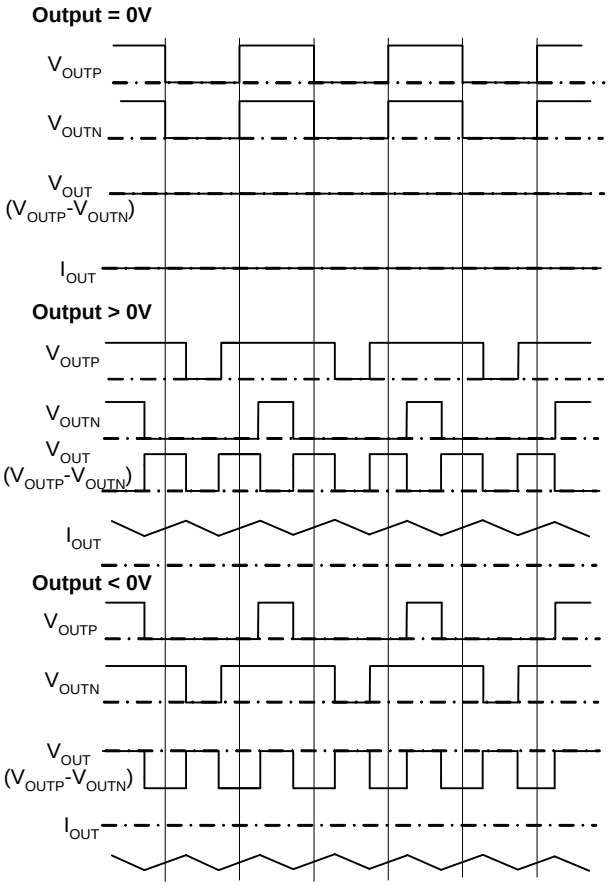


Figure1. The APA2607 Output Waveform (Voltage& Current)

The APA2607 power amplifier modulation scheme is shown in figure 1. The outputs V_{OUTP} and V_{OUTN} are in phase with each other when no input signals. When output > 0V, the duty cycle of V_{OUTP} is greater than 50% and V_{OUTN} is less than 50%; when Output < 0V, the duty cycle of V_{OUTP} is less than 50% and V_{OUTN} is greater than 50%. This method reduces the switching current across the load and reduces the I^2R losses in the load that improves the amplifier's efficiency.

This modulation scheme has very short pulses across the load, this making the small ripple current and very little loss on the load, and the LC filter can be eliminated in most applications. Added the LC filter can increase the efficiency by filter the ripple current.

3.3V Regulator Operation

The 3V3REG regulates the voltage at 3.3V and only for internal circuit used, and connects a capacitor from 1µF to 4.7µF (X5R or above) for stable. (0.8µF or more should be secured including its variation and temperature change.)

Reference Voltage

The voltage output of VREF pin is equal to 3V3REG/2 and needs to connect a capacitor of 0.1µF for voltage stabilization.

Gain Setting Operation

Table 1: The gain setting.

GAIN1	GAIN0	DRC1	DRC0	Gain
0	0	0	0	22dB
0	1	0	0	28dB
1	0	0	0	34dB
1	1	0	0	16dB
0	0	X	1	34dB
0	1	X	1	40dB
1	0	X	1	46dB
1	1	X	1	28dB
0	0	1	X	34dB
0	1	1	X	40dB
1	0	1	X	46dB
1	1	1	X	28dB

The APA2607's gain can be set by GAIN0, GAIN1. The detail gain setting value is listed at table 1.

Mute Operation

At the mute state, the Class-D output is forced at 50% duty at OUTP and OUTN, so differential is zero, and output signals have be disabled. The recovery time of mute state to normal operation is about 1ms (max.).

Shutdown Operation

In order to reduce power consumption while not in use, the APA2607 contains a shutdown function to externally turn off the amplifier bias circuitry. This shutdown feature turns the amplifier off when logic low is placed on the $\overline{SD}$ pin for APA2607. The trigger point between a logic high

Function Description (Cont.)

Shutdown Operation (Cont.)

and logic low level is typically 1.5V. It is best to switch between ground and the supply voltage VDD to provide maximum device performance. By switching the $\overline{SD}$ pin to a low level, the amplifier enters a low-consumption-current state, I_{DD} for APA2607 is in shutdown mode. On normal operating, APA2607's $\overline{SD}$ pin should pull to a high level to keep the IC out of the shutdown mode. The $\overline{SD}$ pin should be tied to a definite voltage to avoid unwanted state changes.

Oscillator Operation

OSCI PIN	Mode	OSCO
0 fixed	Internal fixed clock mode	Internal fixed clock output
1 fixed	Internal spread clock mode (5)	Internal spread clock output
Clock in	External clock mode	External clock buffer output

When the OSCI pin pull low, the APA2607 works at internal fixed clock mode, and OSCO pin is output that fixed clock (500kHz); when the OSCI pin pull high, the APA2607 works at internal spread clock mode, and the clock range is from 400kHz to 600kHz; the OSCO pin is the buffer for output these spread clock.

Apply the external clock to the OSCI pin, the APA2607 will work at external clock mode, and the external clock should at the range from 400kHz to 600kHz and the duty cycle should be at range from 40% to 60%, and the OSCO is the external clock's output buffer.

Power Limit Operation

This function limits the maximum output power of APA2607 for prevent exceed the maximum power of speaker. Except DRC 2 mode, this function is always enabled. The setting value can be a voltage divider by the resistor that connects 3V3REG and GND.

The maximum power limit value (peak voltage)=(1.65-V_{PMAX})x11.23.

Non-Clip Operation

When the DRC [1:0]=01 (DRC1=Low, and DRC0=High), the non-clip mode is active. The gain is increased by 12dB to compare to the normal mode. The output peak voltage becomes to the power limit value. If the peak voltage excesses the power limit value, it will be the attenuation to the power limit value, and the maximum attenuation is -12dB. The attack time is zero second, and needs 7.7 seconds to release the non-clip function from -12dB to 0dB.

The Non-clip operation should be switched under power-off or shutdown mode to prevent the pop noise between the mode switching.

DRC Operation

DRC1	DRC0	MODE
0	0	Normal mode (DRC mode off, Non-clip mode off)
0	1	Non-Clip mode
1	0	DRC 1 mode
1	1	DRC 2 mode

DRC1 mode: DRC [1:0]=10 (DRC1=High, and DRC0 =Low), the DRC 1 mode is active. The gain is increased by 12dB to compare to the normal mode. The power limit value is the point that active the Dynamic Range Compression function. And the maximum attenuation is -12dB. The attack time is zero second, and needs 3.9 seconds to release the non-clip function from -12dB to 0dB.

DRC2 mode: DRC [1:0]=11 (DRC1=High, and DRC0 =High), similar to the DRC 1 mode, but the perform the power limit function.

The DRC operation should be switched under power-off or shutdown mode to prevent the pop noise between the mode switching.

Stereo/Mono Switching Operation

When connecting the RINN and RINP to 3V3REG before power-on, the APA2607 will enter the monaural operational when power-on. In this operation, the output of ROUTP should connect to LOUTP for positive output, and the ROUN should connect to LOUTN for negative output, the input signal will via LINN and LINP to input the APA2607.

This mode can increase more output power to compare to the stereo mode single channel's output power.

Function Description (Cont.)

Multi-APA2607 Synchronization Operation

The external clock synchronization function and clock output function are prepared and the use of master/slave configuration realizes carrier clock synchronization.
When using it with multi chips synchronized, one is used as a master chip and the other is used as a slave chip. At this time, connect OSCO pin of a master chip to OSCI pin of a slave chip. When using 3 pieces of APA2607 (master/slave1/slave2), connect OSCO terminal of a slave1 chip to OSCI pin of a slave2 chip.

Protection Flag Operation

Protection Function	PFLAG Output	Latch	Class-D Output State	Cancellation
DC Detection	Low	Yes	Weak low	Shutdown or Power-Off
UVLO	High-Z	-	Weak low	-
Over-Current Protection	Low	Yes	Weak low	Shutdown or Power-Off
Thermal protection (power limit)	-	No	Power limit (-6dB)	Shutdown or Power-Off or Lower temperature
Thermal protection (class-D off)	Low	No	Weak low	Shutdown or Power-Off or Low temperature

DC Detection Operation

When a DC signal applies to the input of APA2607 and the time excesses 0.5s, the APA2607 will turn off the Class-D output, and the PFLAG pin will pull low. This function protects the speaker to be destroyed by large DC offset. At mute mode, the DC detection function will be disabled. The DC detection state will latch and need power-off or shutdown to release the protection.
Connect PFLAG to /SD pin, the DC detection will be auto recovery.

Over-Current Protection

The APA2607 monitors the output current. When the current exceeds the current-limit threshold, the APA2607 turn-off the output to prevent the IC from damages in over-current or short-circuit condition, and the APA2607 will latch at this state until shutdown or power-off to release the over-current protection. PFLAG will pull-high when protection occur.
Connect PFLAG to $\overline{SD}$ pin, the over-current protection will be auto recovery.

Thermal Protection

The thermal protection has two modes to prevent the APA2607 being destroyed by over-temperature.
When the junction temperature excesses 155°C and under the 165°C, the APA2607 will limit the output power by 6dB to lower the temperature. This calls thermal limit mode. When the junction temperature falls down to 130°C, the thermal limit state will be cancelled.
And when junction temperature excesses 165°C, the Class-D output would turn off, and the PFLAG pin will pull-low. This calls thermal mute mode. All the state will be cancelled when junction lower than 130°C. Some contitions, like V_{DD}=5V, R_L=4Ω, can't meet spec P_O=10W because IC into thermal shutdown. Output power curve use dot line to indicate thermal limit.

Application Information

Square Wave Into the Speaker

Apply the square wave into the speaker may cause the voice coil of speaker jump out the air gap and deface the voice coil. But this depends on the amplitude of square wave high enough and the bandwidth of speaker is higher than the square wave's frequency. For 500kHz switching frequency, this is not issued for the speaker because the frequency is beyond the audio band and can't significantly move the voice coil, as cone movement is proportional to $1/f^2$ for frequency out of audio band.

Input Resistance, R_i

The APA2607's input resistor is fixed and the value is 18kΩ.The input resistance has wide variation (+/-10%) caused by manufacture.

Input Capacitor, C_i

In the typical application, an input capacitor, C_i, is required to allow the amplifier to bias the input signal to the proper DC level for optimum operation. In this case, C_i and the input impedance R_i form a high-pass filter with the corner frequency determined in the following equation:

$$F_{C(highpass)} = \frac{1}{2\pi R_i C_i} \quad (1)$$

The value of C_i must be considered carefully because it directly affects the low frequency performance of the circuit. Where R_i is 18kΩ and the specification calls for a flat bass response down to 40Hz. Equation is reconfigured as below:

$$C_i = \frac{1}{2\pi R_i F_C} \quad (2)$$

When the input resistance variation is considered, the C_i is 0.22µF, so a value in the range of 0.22µF to 1.0µF would be chosen. A further consideration for this capacitor is the leakage path from the input source through the input network (R_i + R_f, C_i) to the load.

This leakage current creates a DC offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain applications. For this reason, a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications because the DC level there is held at $V_{3C3REG}/2$. Please note that it is important to confirm the capacitor polarity in the application.

Output Low-Pass Filter

If the traces form APA2607 to speaker are short, it doesn't require output filter for FCC & CE standard.

A ferrite bead may need if it's failing the test for FCC or CE tested without the LC filter. The figure 2 is the sample for added ferrite bead; the ferrite show choosing high impedance in high frequency.

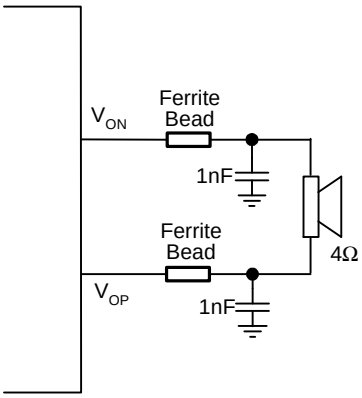


Figure 2. Ferrite bead output filter

Figure 3 and Figure 4 are examples for added the LC filter (But-terworth), it's recommended for the situation that the trace form amplifier to speaker is too long, and needs to eliminate the radiated emission or EMI.

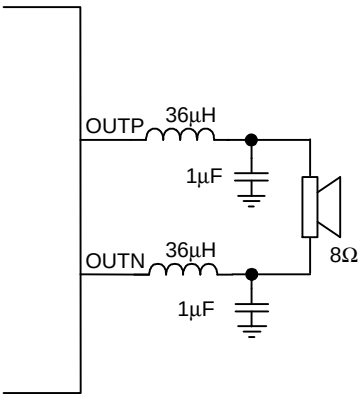


Figure 3. LC output filter for 8Ω speaker

Application Information (Cont.)

Output Low-Pass Filter (Cont.)

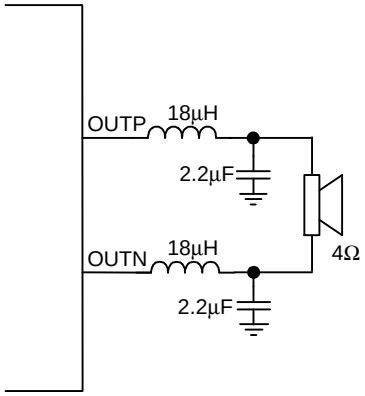


Figure 4. LC output filter for 4Ω speaker

Figure 3 and 4's low pass filter cut-off frequency are 25kHz (F_C).

$$F_{C(lowpass)} = \frac{1}{2\pi\sqrt{LC}} \quad (3)$$

Power-Supply Decoupling Capacitor, C_s

The APA2607 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents the oscillations being caused by long lead length between the amplifier and the speaker.

The optimum decoupling is achieved by using two different types of capacitors that target on different types of noises on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1µF placed as close as possible to the device AVDD pin and 1mF placed to the LPVDD and RPVDD led for works best. For filtering lower frequency noise signals, a large aluminum electrolytic capacitor of 220µF or greater placed near the audio power amplifier is recommended.

Layout Recommendation

In high power Class-D power amplifier, a correct layout is important to ensure proper operation of the amplifier and avoid the switch noise radiation. In general, interconnecting impedance should be minimized by using short, wide printed circuit traces. Especial for the high slew rate output PWM signal to speaker, these loops should be as small as possible.

1. All components should be placed close to the APA2607. For example, the input capacitor (C_i) should be closed to APA2607's input pins to avoid causing noise coupling to APA2607's high impedance inputs; the decoupling capacitor (C_s) should be placed by the APA2607's power pin to decouple the power rail noise.
2. The output traces should be short, wide (>50mil) and symmetric, and this loop like the figure 5, should be as small as possible, (this loop is high slew rate and high current path).

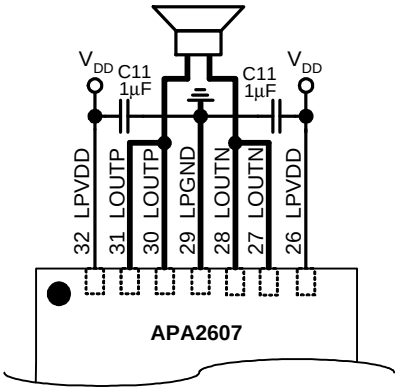


Figure 5. TQFN5x5-32 Land Pattern Recommendation

3. The input trace should be short and symmetric.
4. The power trace width should greater than 50mil.
5. The TQFN5x5-32 Thermal PAD should be soldered on PCB, and the ground plane needs soldered mask (to avoid short-circuit) except the Thermal PAD area. Like the figure 6 illustrate.

Application Information (Cont.)

Layout Recommendation (Cont.)

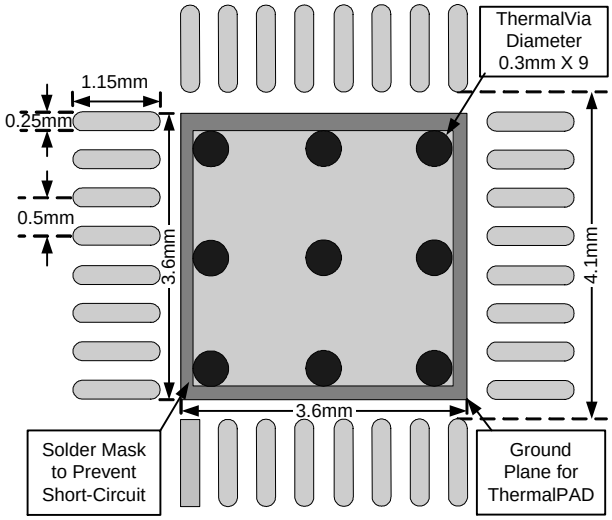
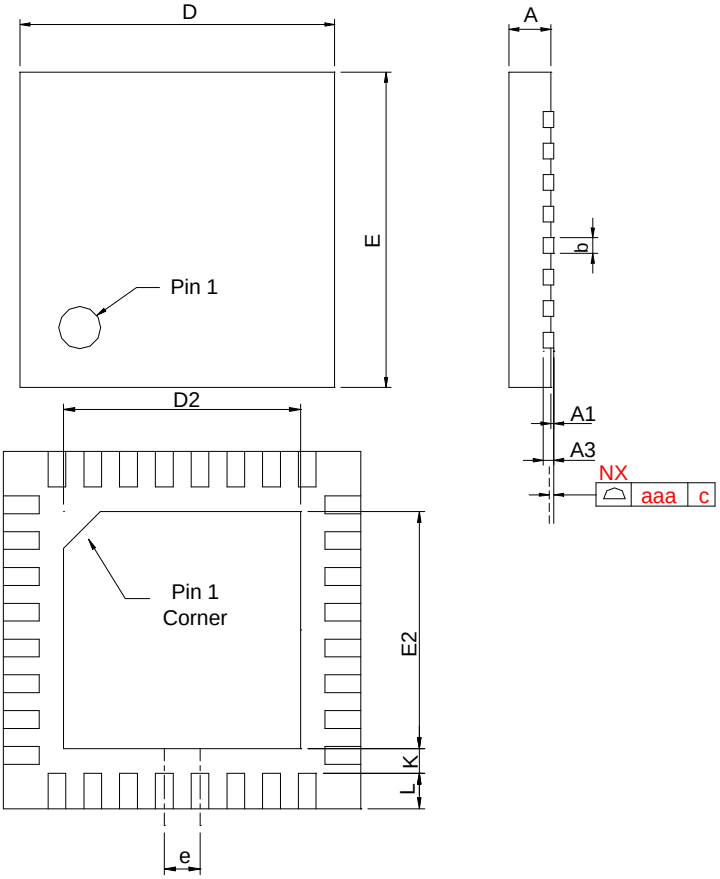


Figure 6. TQFN5x5-32 Land Pattern Recommendation

Package Information

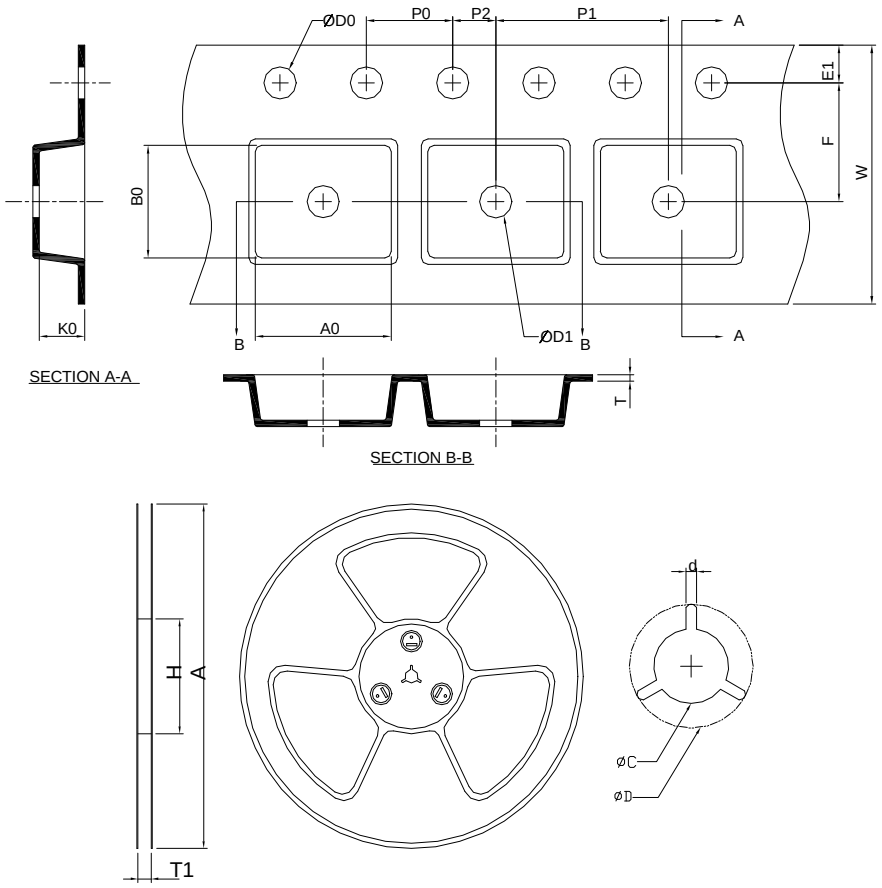
TQFN5x5-32



SYMBOL	TQFN5x5-32			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.18	0.30	0.007	0.012
D	4.90	5.10	0.193	0.201
D2	3.50	3.80	0.138	0.150
E	4.90	5.10	0.193	0.201
E2	3.50	3.80	0.138	0.150
e	0.50 BSC		0.020 BSC	
L	0.35	0.45	0.014	0.018
K	0.20		0.008	
aaa	0.08		0.003	

Note : Followed JEDEC MO-220 WHHD-4.

Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
TQFN5x5-32	330.0±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.10
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	8.0±0.10	2.0±0.10	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	5.30±0.20	5.30±0.20	1.30±0.20

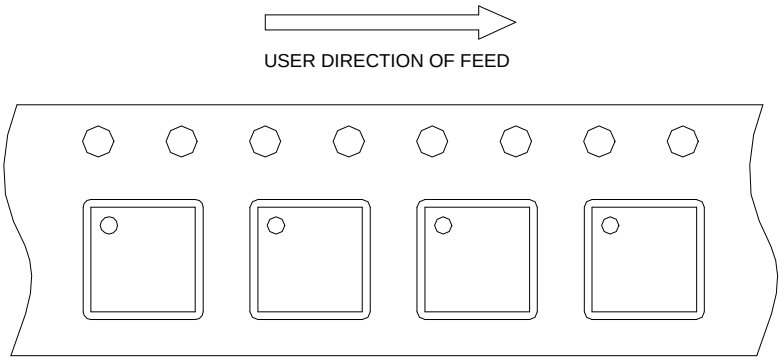
(mm)

Devices Per Unit

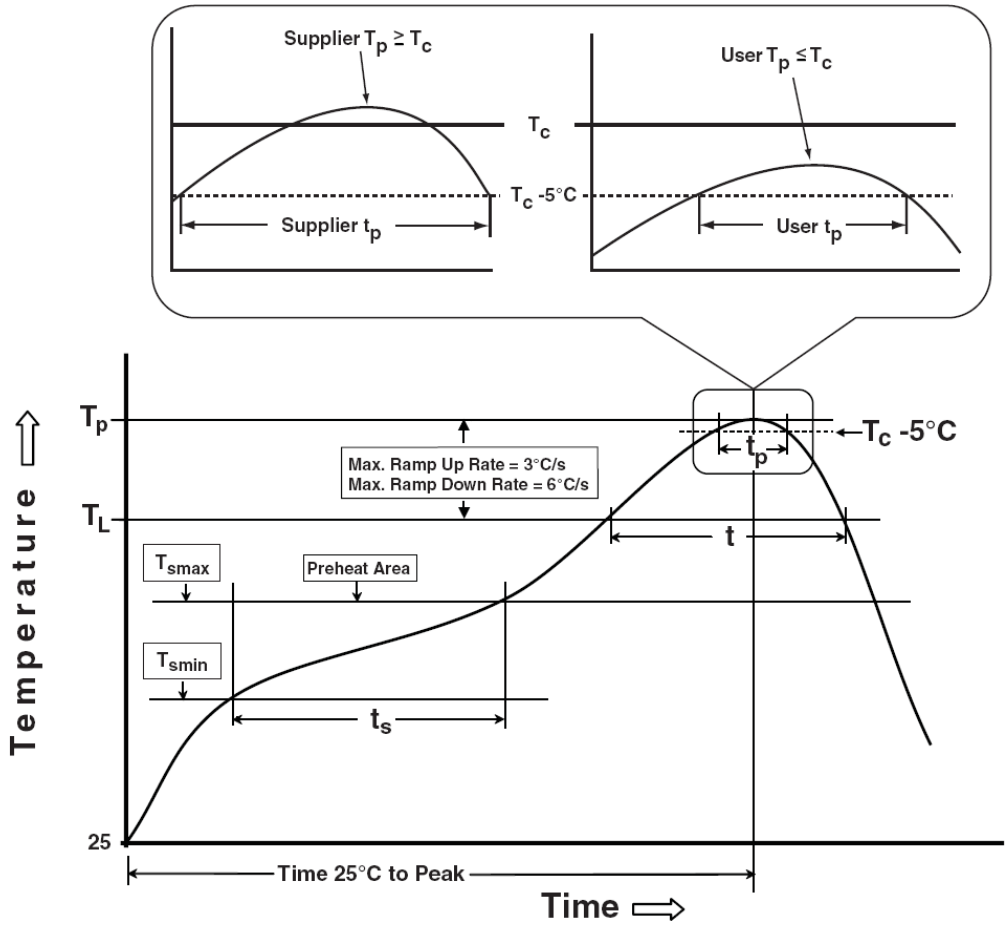
Package Type	Unit	Quantity
TQFN5x5-32	Tape & Reel	2500

Taping Direction Information

TQFN5x5-32



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	100 °C 150 °C 60-120 seconds	150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3 °C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 ³350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ T_j=125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM≧2KV
MM	JESD-22, A115	VMM≧200V
Latch-Up	JESD 78	10ms, 1_{tr}≧100mA

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