3W Stereo Class D Audio Power Amplifier (with DC Volume Control)

Features

- **Operating Voltage: 3.3V-5.5V**
- **High Efficiency 85% at P_O=3W, 4Ω Speaker, V_{DD}=5V**
- **Filter-Free Class D Amplifier**
- **Low Shutdown Current**
  - **I_{DD}=1μA at V_{DD}=5V**
- **64 Steps Volume Adjustable from -80dB to +20dB by DC Voltage with Hysteresis**
- **Output Power at THD+N=1%**
  - **2.6W at V_{DD}=5V ,R_L=3Ω**
  - **2.4W at V_{DD}=5V, R_L=4Ω**
  - **1.4W at V_{DD}=5V, R_L=8Ω**

  Output Power at THD+N=10%
  - **3.2W at V_{DD}=5V ,R_L=3Ω**
  - **3W at V_{DD}=5V, R_L=4Ω**
  - **1.75W at V_{DD}=5V, R_L=8Ω**
- **Less External Components Required**
- **Thermal and Over-Current Protections with Auto-Recovery**
- **Pin-to-Pin Compatible APA2069 and APA2071**
- **Power Enhanced Packages SOP-16P & DIP-16**
- **Lead Free and Green Devices Available (RoHS Compliant)**

Applications

- **LCD TVs**
- **DVD Player**
- **Active Speakers**

General Description

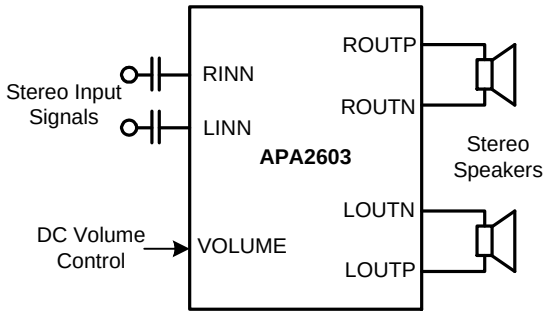
The APA2603 is a stereo, high efficiency, filter-free Class-D audio amplifier available in SOP-16P and DIP-16 packages.

The APA2603 provides the precise DC volume control, the gain range is from -80dB (V_{VOLUME}=5V) to +20dB (V_{VOLUME}=0V) with 64 steps precise control. It's easy to get the suitable amplifier's gain with the 64 steps gain setting. The filter-free architecture eliminates the output filters compared to the traditional Class-D audio amplifier and reduces the external component counts and the components high. Besides, it can save the PCB space, system cost, and simplify the design and the power loss at filter. The APA2603 also integrates the de-pop circuitry that reduces the pops and click noises during power on/off or shutdown enable process.

The APA2603 has build-in, over-current, and thermal protection that prevent the chip being destroyed by short circuit or over temperature situation.

APA2603 is capable of driving 3W at 5V into 4Ω speaker. The efficiency can archive 85% at R_L=4Ω when P_O=3W at V_{DD}=5V.

Simplified Application Circuit

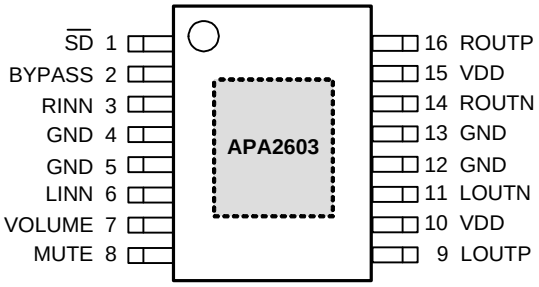


Ordering and Marking Information

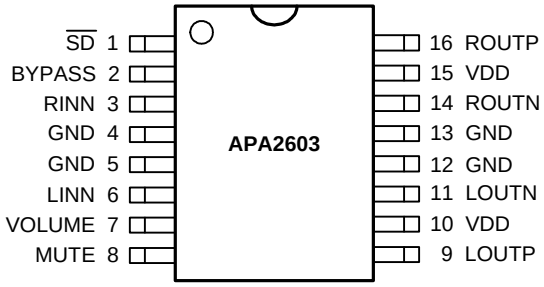
APA2603 □□□-□□ □ Assembly Material Handling Code Temperature Range Package Code	Package Code KA : SOP-16P J : DIP-16 Operating Ambient Temperature Range I : -40 to 85 °C Handling Code TR : Tape & Reel TU : Tube Assembly Material G : Halogen and Lead Free Device
APA2603 KA : 	XXXXX - Date Code
APA2603 J : 	XXXXX - Date Code

Note : ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines "Green" to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Pin Configuration



SOP-16P



DIP-16

 = Thermal Pad (connected the Thermal Pad to GND plane for better dissipation

Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Rating	Unit
V_{DD}	Supply Voltage (VDD to GND)	-0.3 to 6	V
	Input Voltage (LINN, RINN to GND)	-0.3 to V_{DD}+0.3	
	Input Voltage ($\overline{SD}$, MUTE, VOLUME and BYPASS to GND)	-0.3 to V_{DD}+0.3	
T_J	Maximum Junction Temperature	150	°C
T_{STG}	Storage Temperature Range	-65 to +150	
T_{SDR}	Soldering Temperature Range, 10 Seconds	260	
P_D	Power Dissipation	Internally Limited	W

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Thermal Resistance -Junction to Ambient SOP-16P (Note 2) DIP-16 (Note 3)	45	°C/W
θ_{JC}	Thermal Resistance -Junction to Case SOP-16P (Note 4) DIP-16 (Note 5)	8	

Note 2: Please refer to " Layout Recommendation", the Thermal Pad on the bottom of the IC should soldered directly to the PCB's Thermal Pad area that with several thermal vias connect to the ground plan, and the PCB is a 2-layer, 5-inch square area with 2oz copper thickness.

Note 3: Please refer to " Layout Recommendation", the Thermal PIN (PIN4.5.12.13) on the central of the IC should connect to the ground plan, and the PCB is a 2-layer, 5-inch square area with 2oz copper thickness.

Note 4: The case temperature is measured at the center of the Thermal Pad on the underside of the SOP-16P package.

Note 5: The case temperature is measured at the center of the Thermal PIN of the DIP-16 package.

Recommended Operating Conditions

Symbol	Parameter		Range	Unit
V_{DD}	Supply Voltage		3.3~5.5	V
V_{IH}	High Level Threshold Voltage	$\overline{SD}$, MUTE	2 ~V_{DD}	
V_{IL}	Low Level Threshold Voltage	$\overline{SD}$, MUTE	0~0.8	
V_{ICM}	Common Mode Input Voltage		1~V_{DD}-1	
T_A	Ambient Temperature Range		-40~85	°C
T_J	Junction Temperature Range		-40~125	
R_L	Speaker Resistance		2~	Ω

Electrical Characteristics

V_{DD}=5V, GND=0V, T_A= 25°C (unless otherwise noted)

Symbol	Parameter	Test Conditions		APA2603			Unit
				Min.	Typ.	Max.	
I_{DD}	Supply Current	V_{MUTE}=0V, $V_{\overline{SD}}$=5V, No Load		-	8	20	mA
I_{MUTE}	Supply Current (Mute Mode)	V_{MUTE}=5V, $V_{\overline{SD}}$=5V, No Load		-	4	10	
I_{SD}	Supply Current (Mute Mode)	V_{MUTE}=0V, $V_{\overline{SD}}$=0V, No Load		-	1	10	µA
I_i	Input Current	$\overline{SD}$, MUTE, VOLUME		-	-	1	
F_{OSC}	Oscillator Frequency	(V_{DD}=3.3~5.5V, T_A= -40~85°C)		400	500	600	kHz
$R_{i(min)}$	Minimum Input Resistance	A_V=20dB		36	43	50	kΩ
$R_{DS(ON)}$	Static Drain-Source On-State Resistance	V_{DD}=5.5V, I_L=0.8A	P-channel Power MOSFET	-	360	-	mΩ
			N-channel Power MOSFET	-	250	-	
		V_{DD}=4.5V, I_L=0.6A	P-channel Power MOSFET	-	370	-	
			N-channel Power MOSFET	-	260	-	
		V_{DD}=3.6V, I_L=0.4A	P-channel Power MOSFET	-	400	-	
			N-channel Power MOSFET	-	270	-	

Electrical Characteristics (Cont.)

V_{DD}=5V, GND=0V, T_A= 25°C (unless otherwise noted)

Symbol	Parameter	Test Conditions		APA2603			Unit
				Min.	Typ.	Max.	
$T_{START-UP}$	Start-Up Time from Shutdown	Bypass Capacitor, C_1=2.2µF		-	1.2	2	s
V_{DD}=5V, T_A=25℃							
P_O	Output Power	THD+N=1% f_{in}=1kHz	R_L=3Ω	2.3	2.6	-	W
			R_L=4Ω	2.1	2.4	-	
			R_L=8Ω	1	1.4	-	
		THD+N=10% f_{in}=1kHz	R_L=3Ω	2.9	3.2	-	
			R_L=4Ω	2.5	3.0	-	
			R_L=8Ω	1.3	1.75	-	
η	Efficiency	R_L=4Ω, P_O=3W		80	85	-	%
THD+N	Total Harmonic Distortion Plus Noise	f_{in}=1kHz	R_L=3Ω, P_O=1.9W	-	0.2	0.4	
			R_L=4Ω, P_O=1.7W	-	0.1	0.3	
			R_L=8Ω, P_O=1W	-	0.08	0.2	
Crosstalk	Channel Separation	P_O=0.24W, R_L=4Ω, f_{in}=1kHz		-	-100	-60	dB
PSRR	Power Supply Rejection Ratio	R_L=4Ω, Input AC-Ground	f_{in}=100Hz	-	-50	-45	
			f_{in}=1kHz	-	-55	-50	
SNR	Signal to Noise Ratio	With A-weighting Filter P_O = 0.96W, R_L = 8Ω		85	90	-	
Att_{Mute}	Mute Attenuation	f_{in}=1kHz, R_L=8Ω, V_{in}=1Vpp		-	-85	-70	
$Att_{shutdown}$	Shutdown Attenuation	f_{in}=1kHz, R_L=8Ω, V_{in}=1Vpp		-	-110	-100	
V_n	Output Noise	With A-weighting Filter (A_V=20dB)		-	75	100	µVrms
V_{OS}	Output Offset Voltage	R_L=4Ω, A_V=20dB		-	20	30	mV
V_{DD}=3.6V,T_A=25℃							
P_O	Output Power	THD+N=1% f_{in}=1kHz	R_L=3Ω	-	1.3	-	W
			R_L=4Ω	-	1.2	-	
			R_L=8Ω	0.5	0.7	-	
		THD+N=10% f_{in}=1kHz	R_L=3Ω	-	1.6	-	
			R_L=4Ω	-	1.5	-	
			R_L=8Ω	-	0.9	-	
η	Efficiency	R_L=4Ω, P_O=1.5W		78	83	-	%
THD+N	Total Harmonic Distortion Plus Noise	f_{in}=1kHz	R_L=3Ω, P_O=1W	-	0.3	0.5	
			R_L=4Ω, P_O=0.8W	-	0.2	0.4	
			R_L=8Ω, P_O=0.5W	-	0.1	0.3	
Crosstalk	Channel Separation	P_O=0.12W, R_L=4Ω, f_{in}=1kHz			-	-60	dB
PSRR	Power Supply Rejection Ratio	R_L=4Ω, Input AC-Ground	f_{in}=100Hz	-	-50	-45	
			f_{in}=1kHz	-	-55	-50	
SNR	Signal to Noise Ratio	With A-weighting Filter P_O=0.5W, R_L=8Ω		80	85	-	

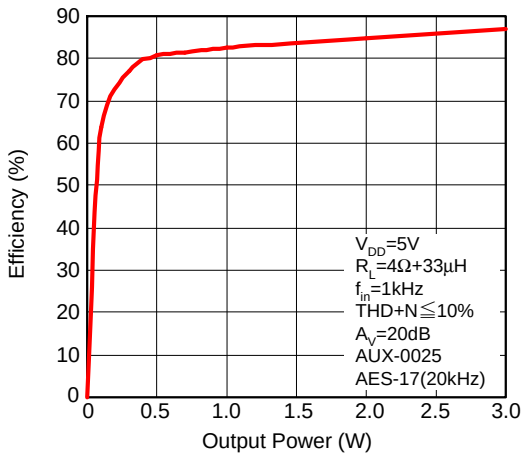
Electrical Characteristics (Cont.)

V_{DD}=5V, GND=0V, T_A= 25°C (unless otherwise noted)

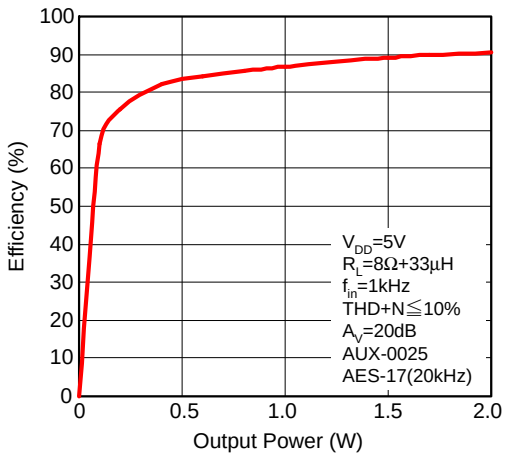
Symbol	Parameter	Test Conditions	APA2603			Unit
			Min.	Typ.	Max.	
V_{DD}=3.6V,T_A=25 ℃ (CONT.)						
Att_{Mute}	Mute Attenuation	f_{in}=1kHz, R_L=8Ω, V_{in}=1Vpp	-	-85	-70	dB
$Att_{shutdown}$	Shutdown Attenuation	f_{in}=1kHz, R_L=8Ω, V_{in}=1Vpp	-	-110	-90	
V_n	Output Noise	With A-weighting Filter (A_V=20dB)	-	75	100	μVrms
V_{OS}	Output Offset Voltage	R_L=4Ω, A_V=20dB	-	20	30	mV

Typical Operating Characteristics

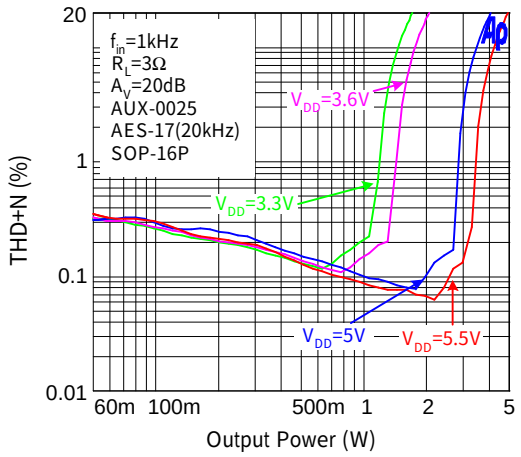
Efficiency vs. Output Power (4W)



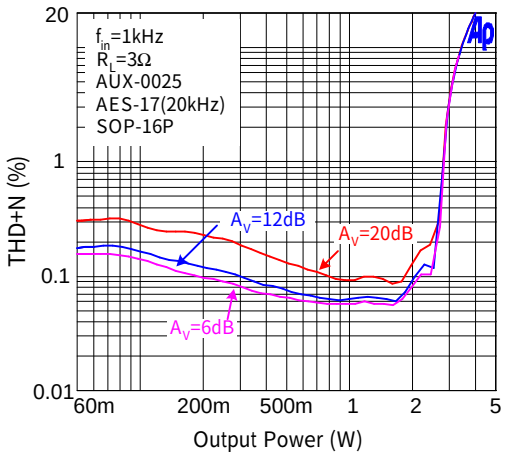
Efficiency vs. Output Power (8W)



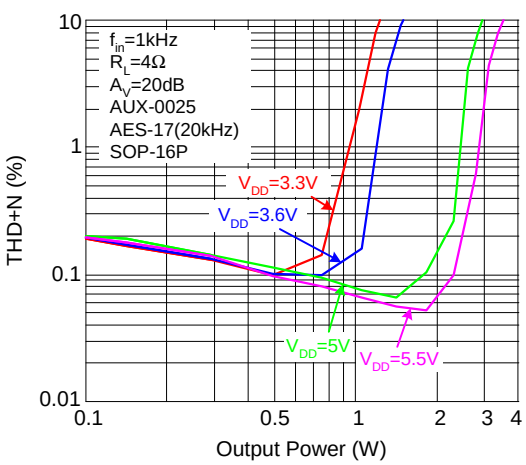
THD+N vs. Output Power



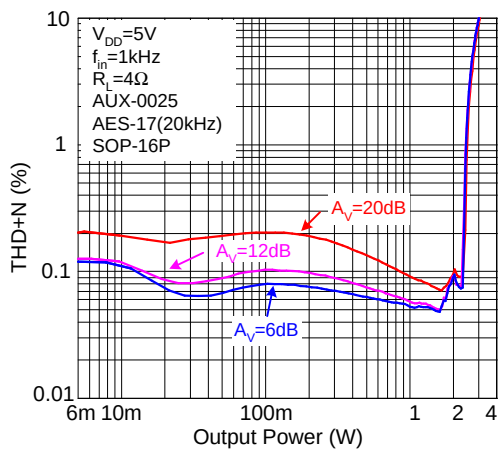
THD+N vs. Output Power



THD+N vs. Output Power

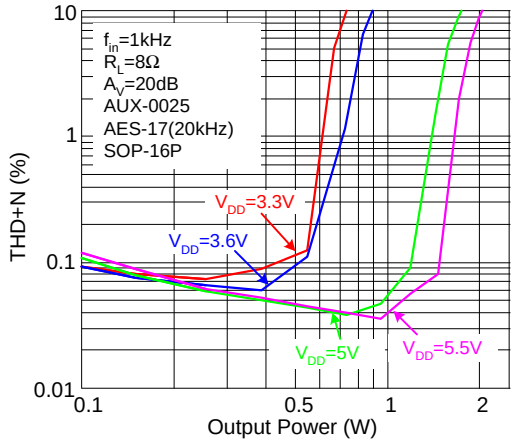


THD+N vs. Output Power

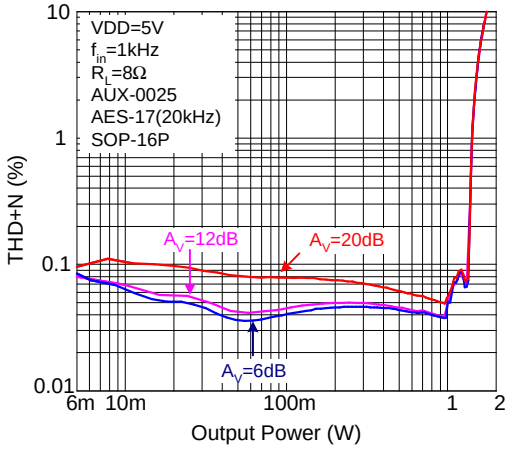


Typical Operating Characteristics (Cont.)

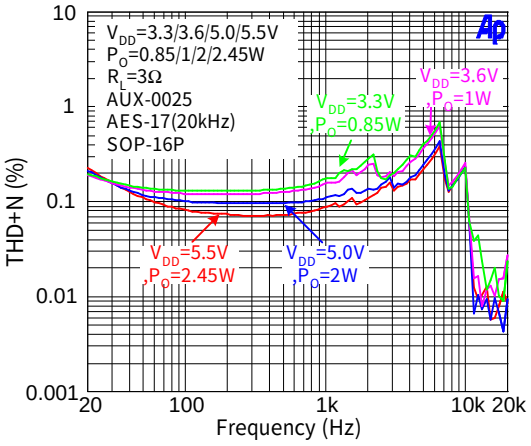
THD+N vs. Output Power



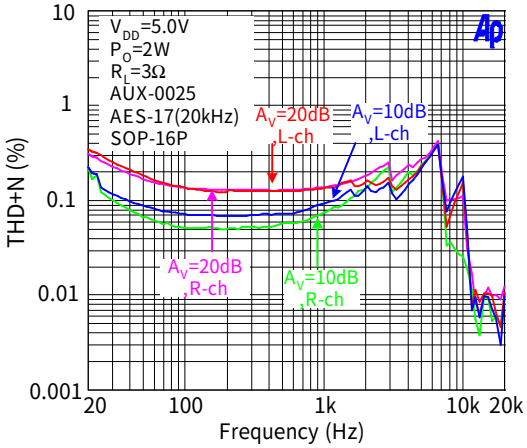
THD+N vs. Output Power



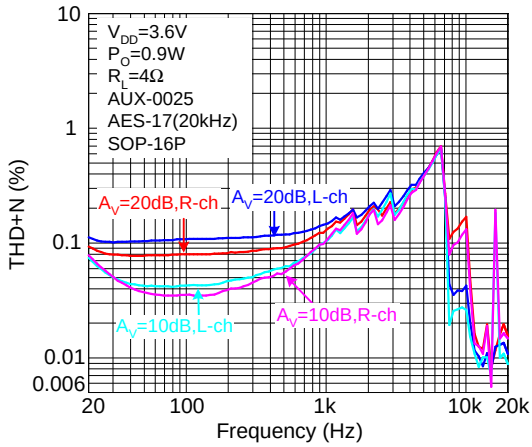
THD+N vs. Frequency



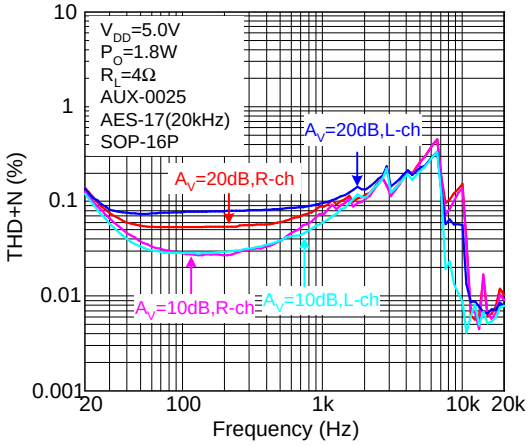
THD+N vs. Frequency



THD+N vs. Frequency

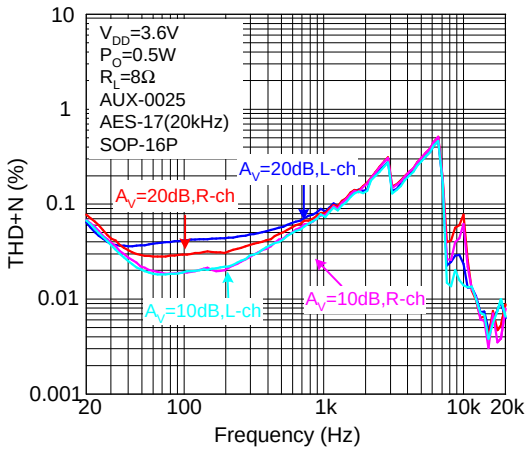


THD+N vs. Frequency

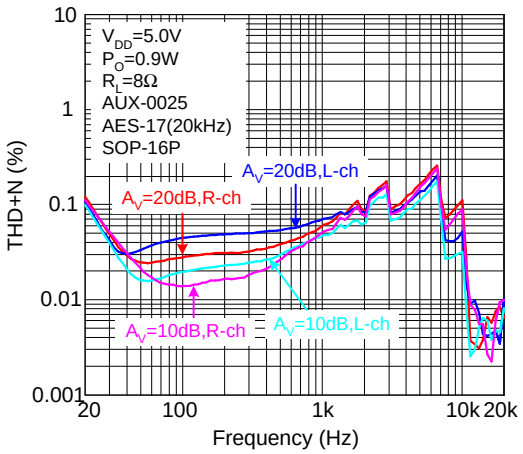


Typical Operating Characteristics (Cont.)

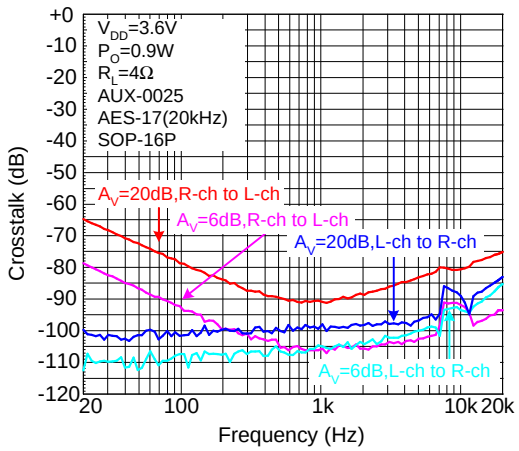
THD+N vs. Frequency



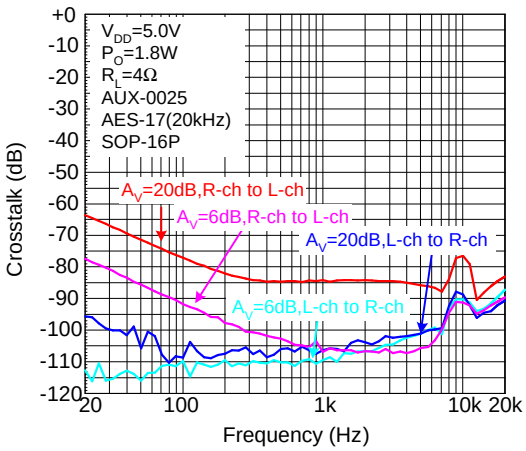
THD+N vs. Frequency



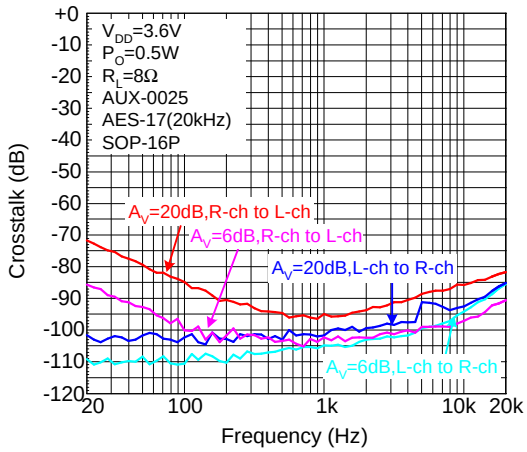
Crosstalk vs. Frequency



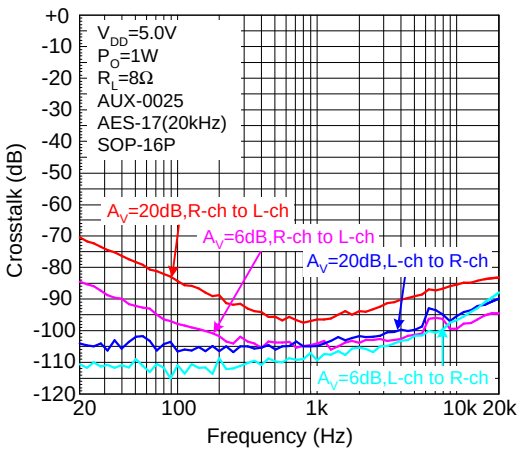
Crosstalk vs. Frequency



Crosstalk vs. Frequency

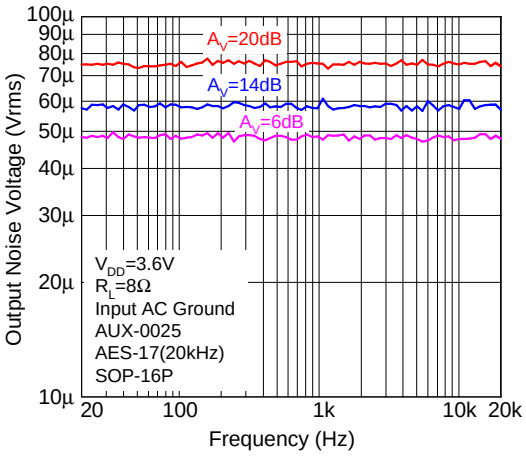


Crosstalk vs. Frequency

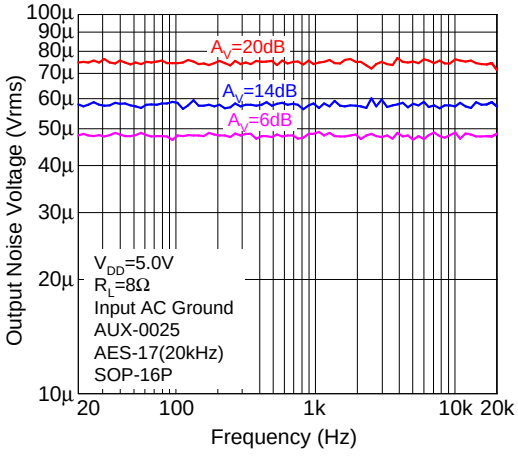


Typical Operating Characteristics (Cont.)

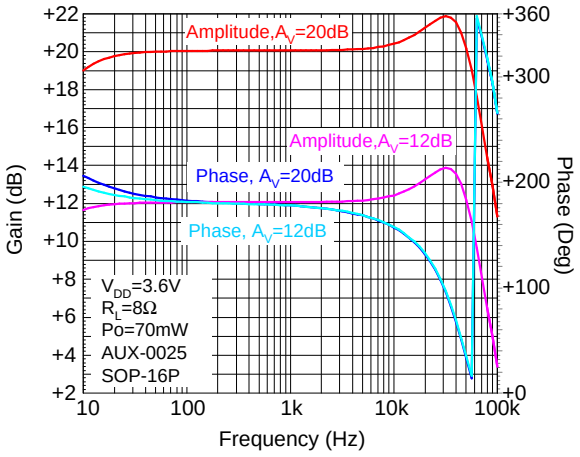
Output Noise Voltage vs. Frequency



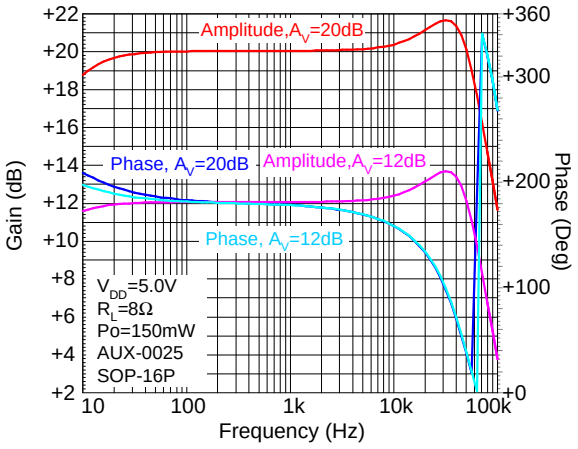
Output Noise Voltage vs. Frequency



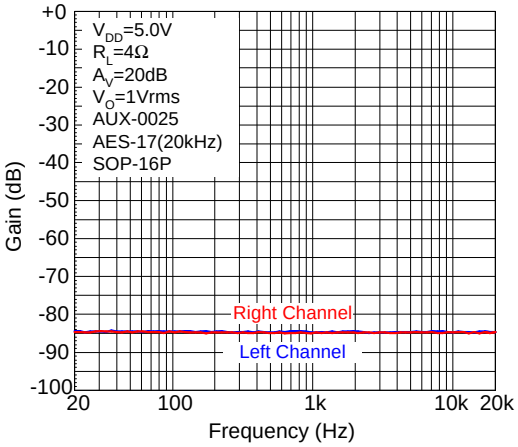
Frequency Response



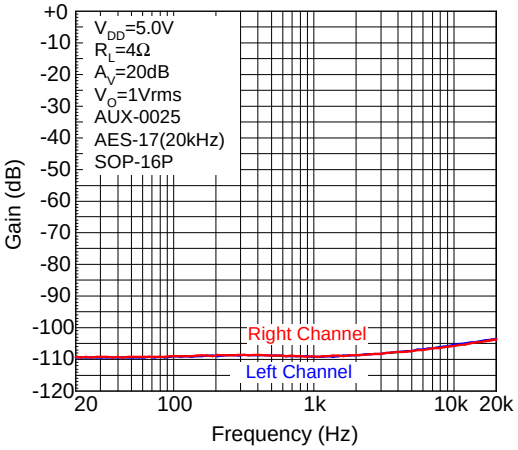
Frequency Response



Mute Attenuation vs. Frequency

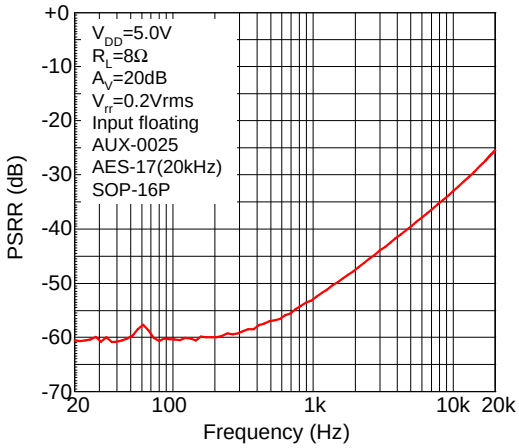


Shutdown Attenuation vs. Frequency

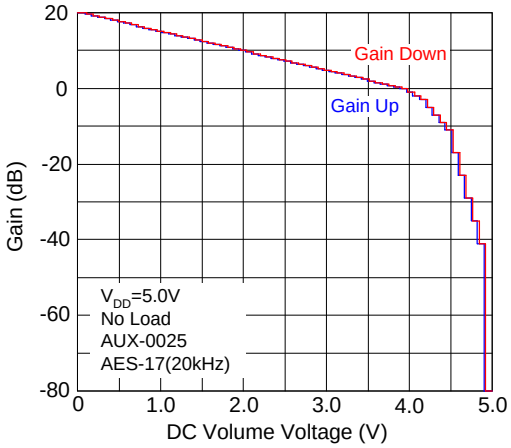


Typical Operating Characteristics (Cont.)

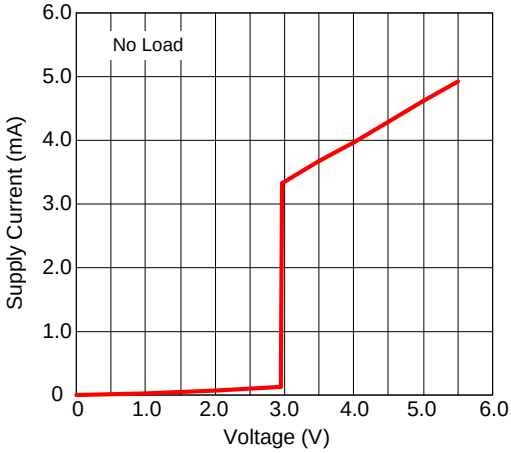
PSRR vs. Frequency



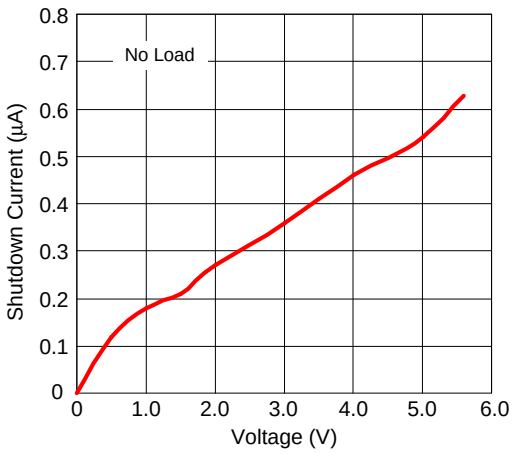
Gain vs. Volume Voltage



Supply Current vs. Voltage



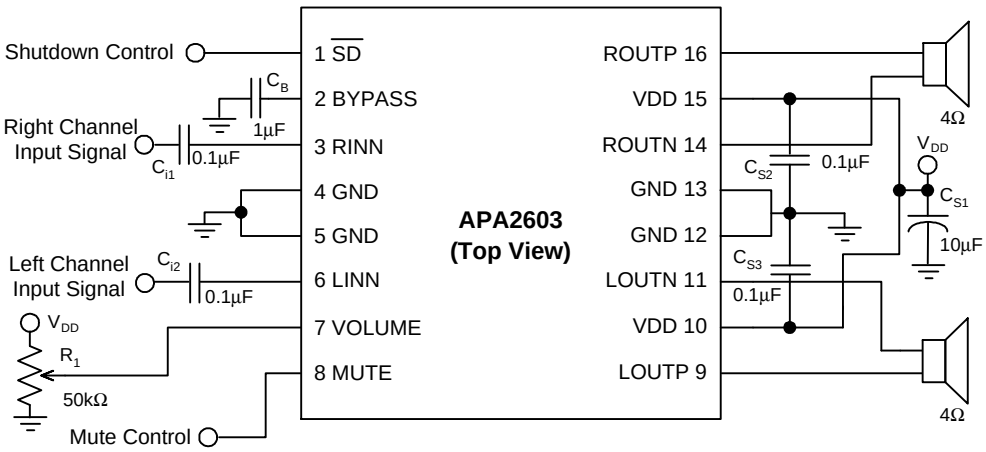
Shutdown Current vs. Voltage



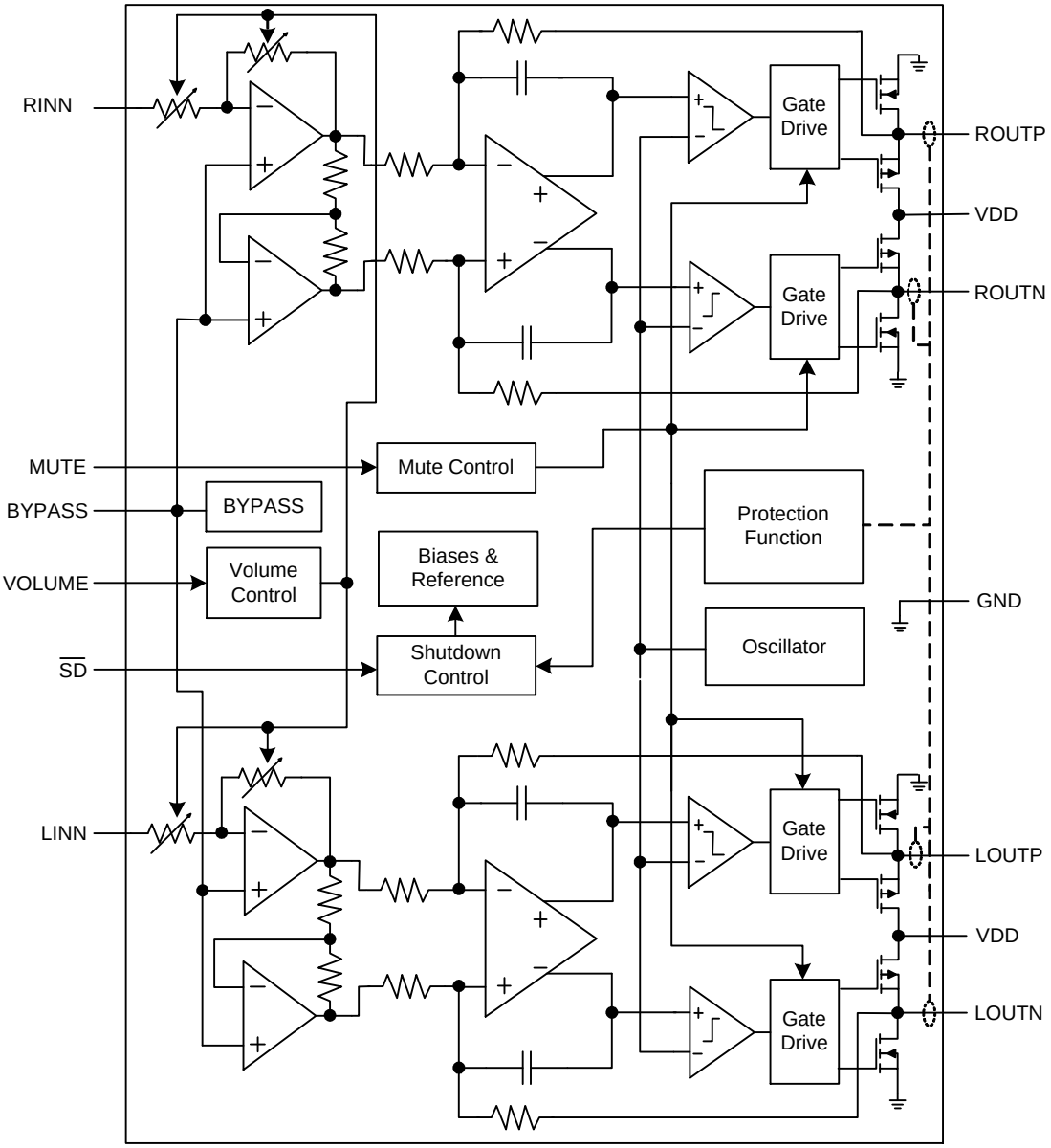
Pin Description

PIN		I/O/P	FUNCTION
NO.	NAME		
1	$\overline{SD}$	I	Shutdown Mode Control Input, Place entire IC in shutdown mode when held low.
2	BYPASS	P	Bias Voltage for Power Amplifiers.
3	RINN	I	Negative Input of Right Channel Power Amplifier.
4,5,12,13	GND	P	Ground Connection.
6	LINN	I	Negative Input of Left Channel Power Amplifier.
7	VOLUME	I	To Set The Amplifier's Gain by Using The DC Voltage.
8	MUTE	I	Mute control signal input, hold low for normal operation, hold high to mute.
9	LOUTP	O	Positive Output of Left Channel Power Amplifier.
10,15	VDD	P	Power Supply.
11	LOUTN	O	Negative Output of Left Channel Power Amplifier.
14	ROUTN	O	Negative Output of Right Channel Power Amplifier.
16	ROUTP	O	Positive Output of Right Channel Power Amplifier.

Typical Application Circuit



Block Diagram



Volume Control Table

Step	Gain	Low (%)	High (%)	Recom (%)	Low (5V)	High(5V)	Recom (5V)
1	20	0.00	2.50	0.00	0.000	0.125	0.00
2	19.6	2.00	3.98	2.99	0.100	0.199	0.15
3	19.2	3.48	5.46	4.47	0.174	0.273	0.22
4	18.8	4.96	6.94	5.95	0.248	0.347	0.30
5	18.4	6.44	8.42	7.43	0.322	0.421	0.37
6	18	7.92	9.90	8.91	0.396	0.495	0.45
7	17.6	9.40	11.38	10.39	0.470	0.569	0.52
8	17.2	10.88	12.86	11.87	0.544	0.643	0.59
9	16.8	12.36	14.34	13.35	0.618	0.717	0.67
10	16.4	13.84	15.82	14.83	0.692	0.791	0.74
11	16	15.32	17.30	16.31	0.766	0.865	0.82
12	15.6	16.80	18.78	17.79	0.840	0.939	0.89
13	15.2	18.28	20.26	19.27	0.914	1.013	0.96
14	14.8	19.76	21.74	20.75	0.988	1.087	1.04
15	14.4	21.24	23.22	22.23	1.062	1.161	1.11
16	14	22.72	24.70	23.71	1.136	1.235	1.19
17	13.6	24.20	26.18	25.19	1.210	1.309	1.26
18	13.2	25.68	27.66	26.67	1.284	1.383	1.33
19	12.8	27.16	29.14	28.15	1.358	1.457	1.41
20	12.4	28.64	30.62	29.63	1.432	1.531	1.48
21	12	30.12	32.10	31.11	1.506	1.605	1.56
22	11.6	31.60	33.58	32.59	1.580	1.679	1.63
23	11.2	33.08	35.06	34.07	1.654	1.753	1.70
24	10.8	34.56	36.54	35.55	1.728	1.827	1.78
25	10.4	36.04	38.02	37.03	1.802	1.901	1.85
26	10	37.52	39.50	38.51	1.876	1.975	1.93
27	9.6	39.00	40.98	39.99	1.950	2.049	2.00
28	9.2	40.48	42.46	41.47	2.024	2.123	2.07
29	8.8	41.96	43.94	42.95	2.098	2.197	2.15
30	8.4	43.44	45.42	44.43	2.172	2.271	2.22
31	8	44.92	46.90	45.91	2.246	2.345	2.30
32	7.6	46.40	48.38	47.39	2.320	2.419	2.37
33	7.2	47.88	49.86	48.87	2.394	2.493	2.44
34	6.8	49.36	51.34	50.35	2.468	2.567	2.52
35	6.4	50.84	52.82	51.83	2.542	2.641	2.59
36	6	52.32	54.30	53.31	2.616	2.715	2.67
37	5.6	53.80	55.78	54.79	2.690	2.789	2.74
38	5.2	55.28	57.26	56.27	2.764	2.863	2.81
39	4.8	56.76	58.74	57.75	2.838	2.937	2.89

Volume Control Table (Cont.)

Step	Gain	Low (%)	High (%)	Recom (%)	Low (5V)	High(5V)	Recom (5V)
40	4.4	58.24	60.22	59.23	2.912	3.011	2.96
41	4	59.72	61.70	60.71	2.986	3.085	3.04
42	3.6	61.20	63.18	62.19	3.060	3.159	3.11
43	3.2	62.68	64.66	63.67	3.134	3.233	3.18
44	2.8	64.16	66.14	65.15	3.208	3.307	3.26
45	2.4	65.64	67.62	66.63	3.282	3.381	3.33
46	2	67.12	69.10	68.11	3.356	3.455	3.41
47	1.6	68.60	70.58	69.59	3.430	3.529	3.48
48	1.2	70.08	72.06	71.07	3.504	3.603	3.55
49	0.8	71.56	73.54	72.55	3.578	3.677	3.63
50	0.4	73.04	75.02	74.03	3.652	3.751	3.70
51	0	74.52	76.50	75.51	3.726	3.825	3.78
52	-1	76.00	77.98	76.99	3.800	3.899	3.85
53	-2	77.48	79.46	78.47	3.874	3.973	3.92
54	-3	78.96	80.94	79.95	3.948	4.047	4.00
55	-5	80.44	82.42	81.43	4.022	4.121	4.07
56	-7	81.92	83.90	82.91	4.096	4.195	4.15
57	-9	83.40	85.38	84.39	4.170	4.269	4.22
58	-11	84.88	86.86	85.87	4.244	4.343	4.29
59	-17	86.36	88.34	87.35	4.318	4.417	4.37
60	-23	87.84	89.82	88.83	4.392	4.491	4.44
61	-29	89.32	91.30	90.31	4.466	4.565	4.52
62	-35	90.80	92.78	91.79	4.540	4.639	4.59
63	-41	92.28	94.26	93.27	4.614	4.713	4.66
64	-80	93.76	100	100.00	4.688	5.000	5.00

Function Description

Class D Operation

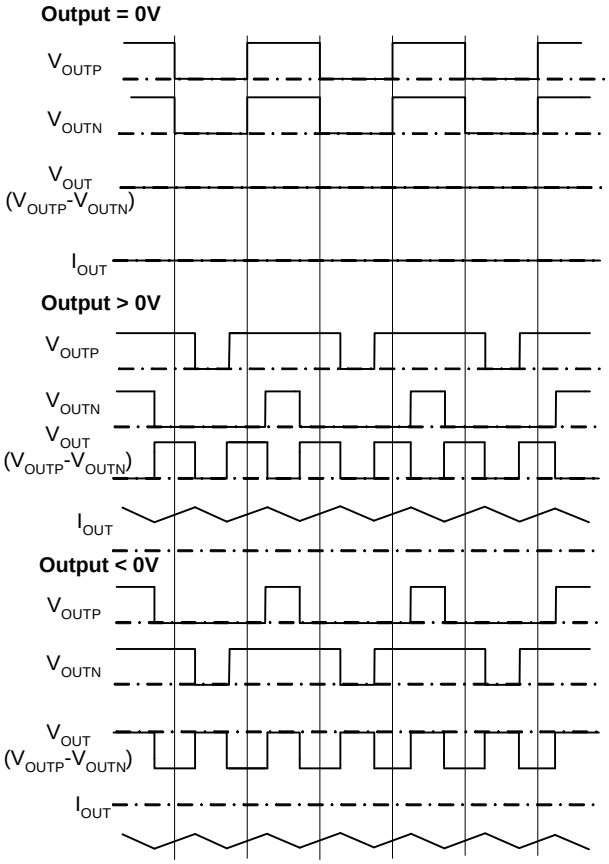


Figure 1. The APA2603 Output Waveform (Voltage& Current)

The APA2603 power amplifier modulation scheme is shown in figure 1; the outputs V_{OUTP} and V_{OUTN} are in phase with each other when no input signals. When output > 0V, the duty cycle of V_{OUTP} is greater than 50% and V_{OUTN} is less than 50%; when output <0V, the duty cycle of V_{OUTP} is less than 50% and V_{OUTN} is greater than 50%. This method reduces the switching current across the load and reduces the I^2R losses in the load that improves the amplifier's efficiency.

This modulation scheme has very short pulses across the load, this making the small ripple current and very little loss on the load, and the LC filter can be eliminated in most applications. Added the LC filter can increase the efficiency by filter the ripple current.

Bypass Voltage

The bypass voltage is equal to $V_{DD}/2$, this voltage is for bias the internal preamplifier stages. The external capacitor for this reference (C_B) is a critical component and serves several important functions.

DC Volume Control Function

The APA2603 has an internal stereo volume control that setting is the function of the DC voltage applied to the VOLUME input pin. The APA2603 volume control consists of 64 steps that are individually selected by a variable DC voltage level on the VOLUME control pin. The range of the steps controlled by the DC voltage are from +20dB to -80dB. Each gain step corresponds to a specific input voltage range, as shown in the table. To minimize the effect of noise on the volume control pin, which can affect the selected gain level, hysteresis and clock delay are implemented. The amount of hysteresis corresponds to half of the step width, as shown in the "DC Volume Control Graph".

For the highest accuracy, the voltage shown in the 'recommended voltage' column of the table is used to select a desired gain. This recommended voltage is exactly halfway between the two nearest transitions. The gains' level are 0.4dB/step from 20dB to 0dB; 1dB/step from 0dB to -3dB; 2dB/step from -3dB to -11dB and 6dB/step from -11dB to -41dB and the last step at -80dB as mute mode.

Mute Operation

When place the logic high on MUTE pin, the APA2603's outputs runs at a constant 50% duty cycle, and the APA2603 is at mute state. Place the logic low on MUTE pin enables the outputs, and the output changes the duty cycle with the input signal. This pin could be used as a quick disable/enable of outputs when changing channels on a television or transitioning between different audio sources. The MUTE pin should never be left floating. When MUTE pin hold high to mute.

Function Description (Cont.)

Shutdown Operation

In order to reduce power consumption while not in use, the APA2603 contains a shutdown function to externally turn off the amplifier bias circuitry. This shutdown feature turns the amplifier off when logic low is placed on the $\overline{SD}$ pin for APA2603. The trigger point between a logic high and logic low level is typically 0.65V. It is the best to switch between the ground and the supply voltage V_{DD} to provide maximum device performance. By switching the $\overline{SD}$ pin to a low level, the amplifier enters a low-consumption-current state, I_{DD} for APA2603 is in shutdown mode. On normal operating, APA2603's $\overline{SD}$ pin should pull to a high level to keep the IC out of the shutdown mode. The $\overline{SD}$ pin should be tied to a definite voltage to avoid unwanted state change.

Over-Current Protection

The APA2603 monitors the output current. When the current exceeds the current-limit threshold, the APA2603 turn-off the output stage to prevent the output device from damaging in over-current or short-circuit condition. The IC will turn-on the output buffer after 1ms. However, if the over-current or short-circuits condition still remains, it enters the Over-Current protection again. The situation will circulate until the over-current or short-circuits has being removed.

Thermal Protection

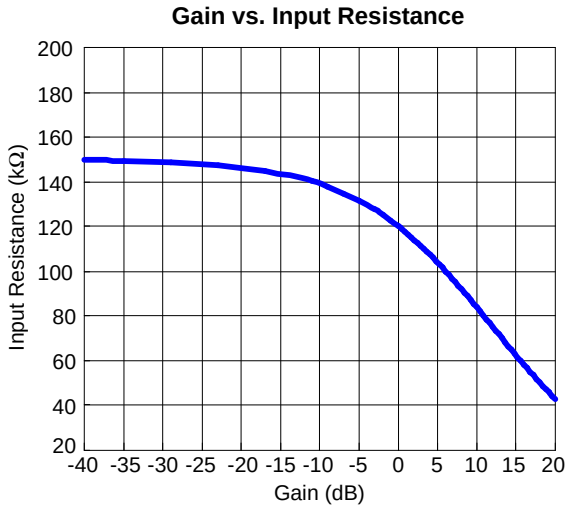
The over-temperature circuit limits the junction temperature of the APA2603. When the junction temperature exceeds T_J = +150°C, a thermal sensor turns off the output buffer, allowing the devices to cool. The thermal sensor allows the amplifier to start-up after the junction temperature down about 125 °C. The thermal protection is designed with a 25 °C hysteresis to lower the average T_J during continuous thermal overload conditions, increasing lifetime of the IC.

Application Information

Square Wave into the Speaker

Apply the square wave into the speaker may cause the voice coil of speaker jumping out the air gap and defacing the voice coil. However, this depends on the amplitude of square wave is high enough and the bandwidth of speaker is higher than the square wave's frequency. For 500kHz switching frequency, this is not issued for the speaker because the frequency is beyond the audio band and can't significantly move the voice coil, as cone movement is proportional to $1/f^2$ for frequency out of audio band.

Input Resistor, R_i



For achieving the 64 steps gain setting, it varies the input resistance network (R_i & R_f) of amplifier. The input resistor's range form smallest to maximum is about 6 times. Therefore, the input high-pass filter's low cutoff frequency will change six times from low to high. The cutoff frequency can be calculated by equation 1.

Input Capacitor, C_i

In the typical application, an input capacitor, C_i, is required to allow the amplifier to bias the input signal to the proper DC level for optimum operation. In this case, C_i and the input impedance R_i form a high-pass filter with the corner frequency determined in the following equation:

$$f_{C(highpass)} = \frac{1}{2\pi R_i C_i} \quad (1)$$

The value of C_i must be considered carefully because it directly affects the low frequency performance of the circuit. Where R_i is 36kΩ (minimum) and the specification calls for a flat bass response down to 50Hz. The equation is reconfigured as below:

$$C_i = \frac{1}{2\pi R_i f_c} \quad (2)$$

When the input resistance variation is considered, the C_i is 0.08µF, so a value in the range of 0.01µF to 0.022µF would be chosen. A further consideration for this capacitor is the leakage path from the input source through the input network (R_i + R_f, C_i) to the load. This leakage current creates a DC offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain applications. For this reason, a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifiers' input in most applications because the DC level of the amplifiers' inputs are held at $V_{DD}/2$. Please note that it is important to confirm the capacitor polarity in the application.

Effective Bypass Capacitor, C_B

As with any power amplifier, proper supply bypassing is critical for low noise performance and high power supply rejection.

The bypass capacitance sffects the startiup time. It is determined in the following wquation:

$$T_{START-UP}=0.5(sec/\mu F) \times C_B + 0.2(sec) \quad (3)$$

The capacitor location on the bypass pin should be as close to the device as possible. The effect of a larger half bypass capacitor is improved PSRR due to increased half-supply stability. The selection of bypass capacitors, especially C_B, is thus dependent upon desired PSRR requirements, click and pop performance.To avoid the start-up pop noise occurred, choose C_i which is not larger than C_B.

Application Information (Cont.)

Ferrite Bead Selection

If the traces form APA2603 to speaker are short, the ferrite bead filters can reduce the high frequency radiated to meet the FCC & CE required.
A ferrite that has very low impedance at low frequencies and high impedance at high frequencies (above 1 MHz) is recommended.

Output Low-Pass Filter

If the traces form APA2603 to speaker are short, it doesn't require output filter for FCC & CE standard.
A ferrite bead may be needed if it's failing the test for FCC or CE tested without the LC filter. The figure 2 is the sample for added ferrite bead; the ferrite shows choosing high impedance in high frequency.

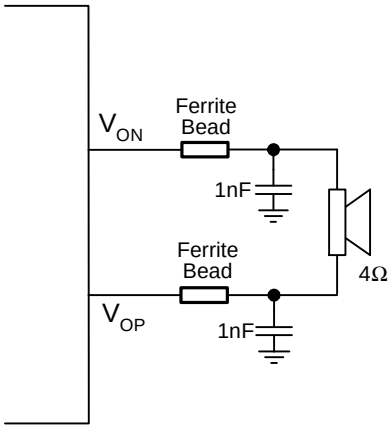


Figure 2. Ferrite bead output filter

Figure 3 and 4 are examples for added the LC filter (Butterworth), it's recommended for the situation that the trace form amplifier to speaker is too long and needs to eliminate the radiated emission or EMI.

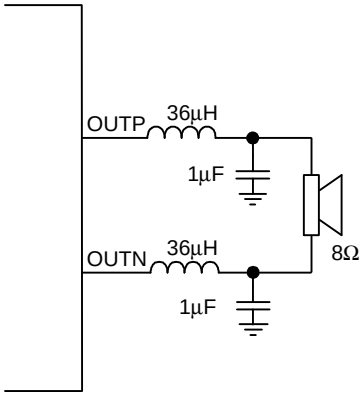


Figure 3. LC output filter for 8Ω speaker

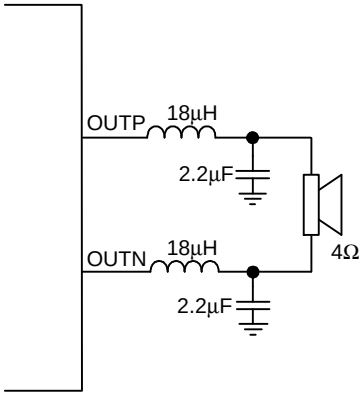


Figure 4. LC output filter for 4Ω speaker

Figure 3 and 4's low pass filter cut-off frequency are 25kHz (F_C).

$$f_{C(lowpass)} = \frac{1}{2\pi\sqrt{LC}} \quad (5)$$

Power-Supply Decoupling Capacitor, C_S

The APA2603 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents the oscillations being caused by long lead length between the amplifier and the speaker.

Application Information (Cont.)

Power-Supply Decoupling Capacitor, C_S (Cont.)

The optimum decoupling is achieved by using two different types of capacitors that target on different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1µF placed as close as possible to the device VDD pin for works best. For filtering lower frequency noise signals, a large aluminum electrolytic capacitor of 10µF or greater placed near the audio power amplifier is recommended.

Layout Recommendation

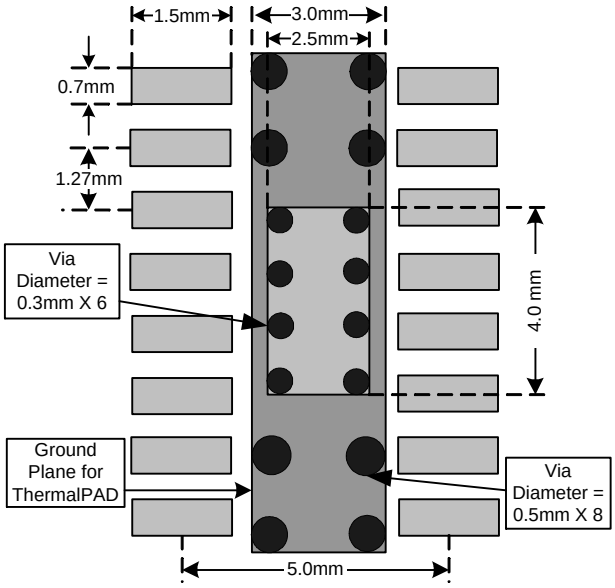


Figure 5. SOP-16P Land Pattern Recommendation

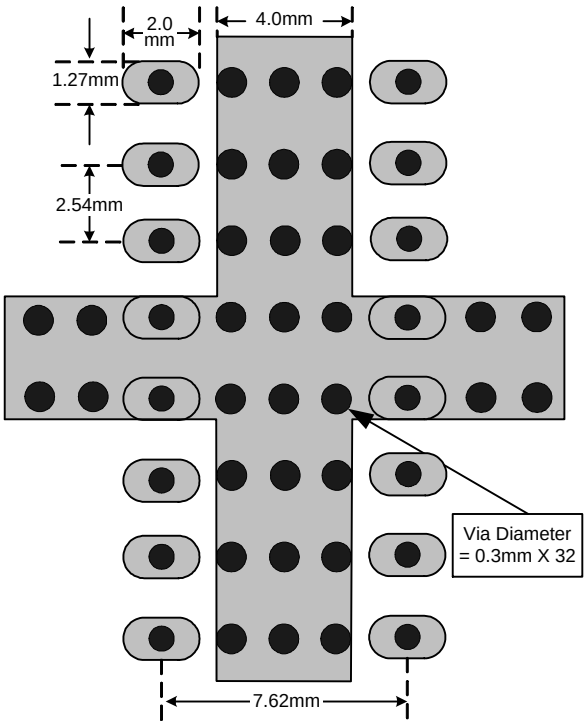
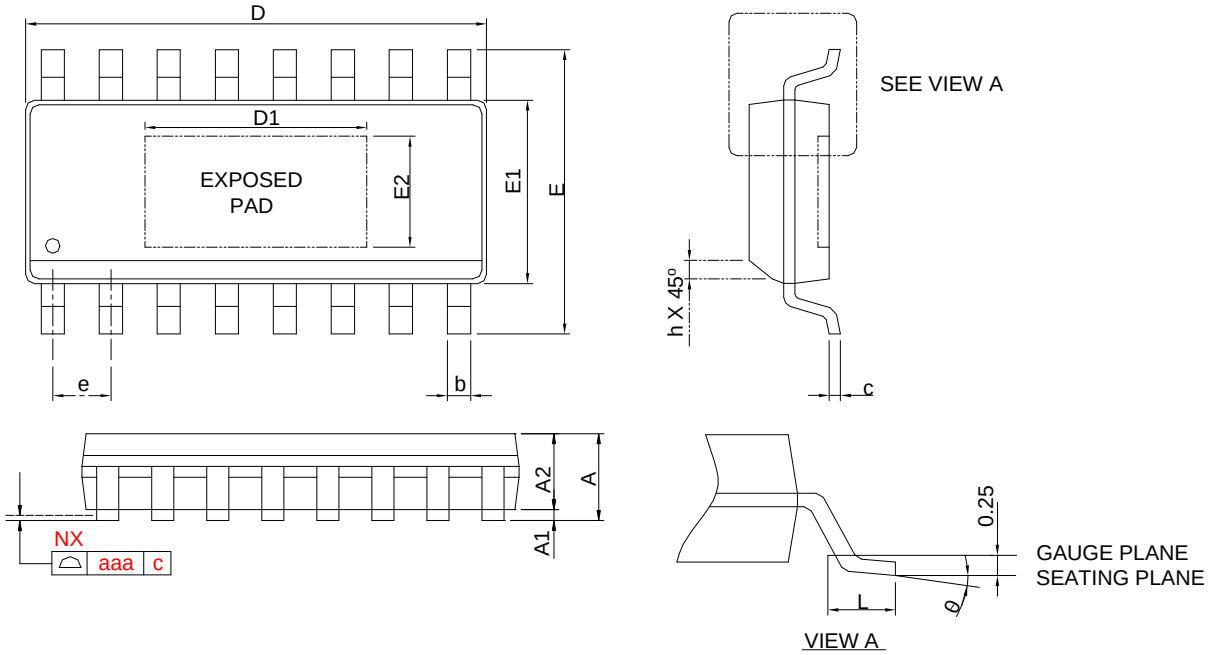


Figure 6. DIP-16 Land Pattern Recommendation

1. All components should be placed close to the APA2603. For example, the input capacitor (C_i) should be close to APA2603's input pins to avoid causing noise coupling to APA2603's high impedance inputs; the decoupling capacitor (Cs) should be placed by the APA2603's power pin to decouple the power rail noise.
2. The output traces should be short, wide (>50mil) and symmetric.
3. The input trace should be short and symmetric.
4. The power trace width should greater than 50mil.
5. The SOP-16P Thermal PAD should be soldered on PCB, and the ground plane needs soldered mask (to avoid short circuit) except the Thermal PAD area. And the DIP-16's pin 4,5,12, and 13 should be connected to the ground plane for thermal transformer.

Package Information

SOP-16P



SYMBOL	SOP-16P			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		1.75		0.069
A1	0.00	0.15	0.000	0.006
A2	1.25		0.049	
b	0.31	0.51	0.012	0.020
c	0.17	0.25	0.007	0.010
D	9.80	10.00	0.386	0.394
D1	3.50	4.50	0.138	0.177
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
E2	2.00	3.00	0.079	0.118
e	1.27 BSC		0.050 BSC	
h	0.25	0.50	0.010	0.020
L	0.40	1.27	0.016	0.050
θ	0°	8°	0°	8°
aaa	0.10		0.004	

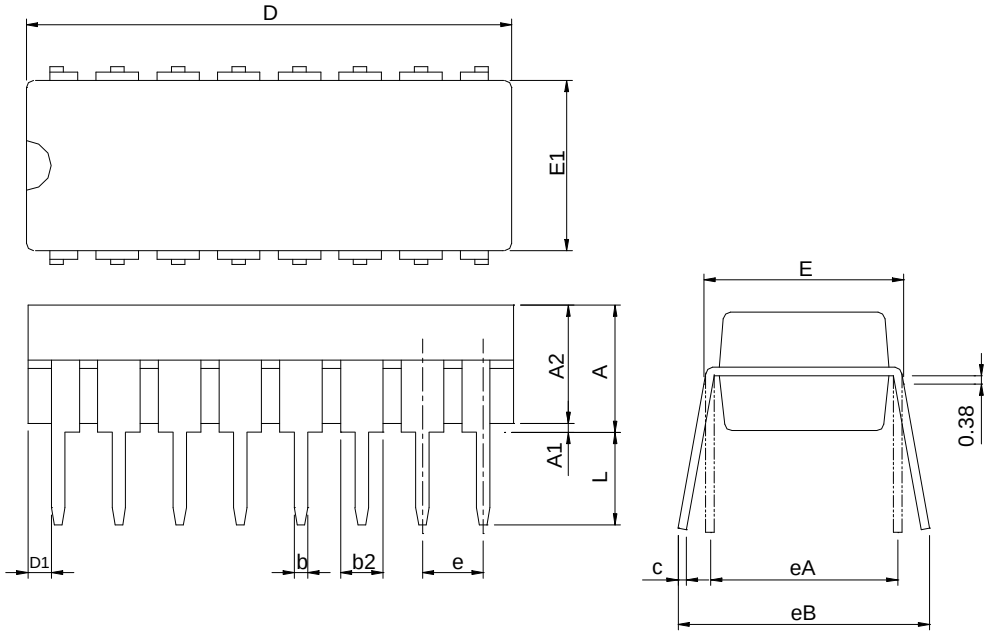
Note : 1. Follow from JEDEC MS-012 BC.

2. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion or gate burrs shall not exceed 6 mil per side.

3. Dimension "E" does not include inter-lead flash or protrusions. Inter-lead flash and protrusions shall not exceed 10 mil per side.

Package Information

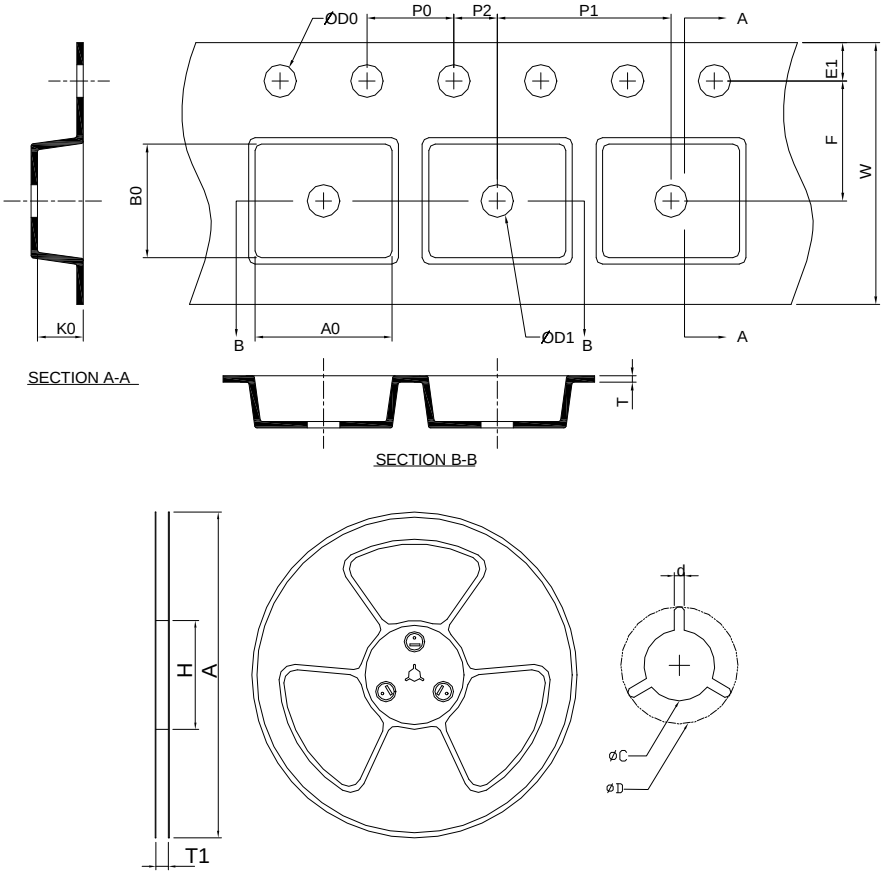
DIP-16



SYMBOL	DIP-16			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		5.33		0.210
A1	0.38		0.015	
A2	2.92	4.95	0.115	0.195
b	0.36	0.56	0.014	0.022
b2	1.14	1.78	0.045	0.070
c	0.20	0.35	0.008	0.014
D	18.6	20.31	0.732	0.800
D1	0.13		0.005	
E	7.62	8.26	0.300	0.325
E1	6.10	7.11	0.240	0.280
e	2.54 BSC		0.100 BSC	
eA	7.62 BSC		0.300 BSC	
eB		10.92		0.430
L	2.92	3.81	0.115	0.150

Note : 1. Followed from JEDEC MS-001AB
2. Dimension D, D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 10 mil.

Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
SOP-16P	330.0±2.00	50 MIN.	16.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	16.0±0.30	1.75±0.10	7.5±0.10
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	8.0±0.10	2.0±0.10	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	6.40±0.20	10.30±0.20	2.10±0.20

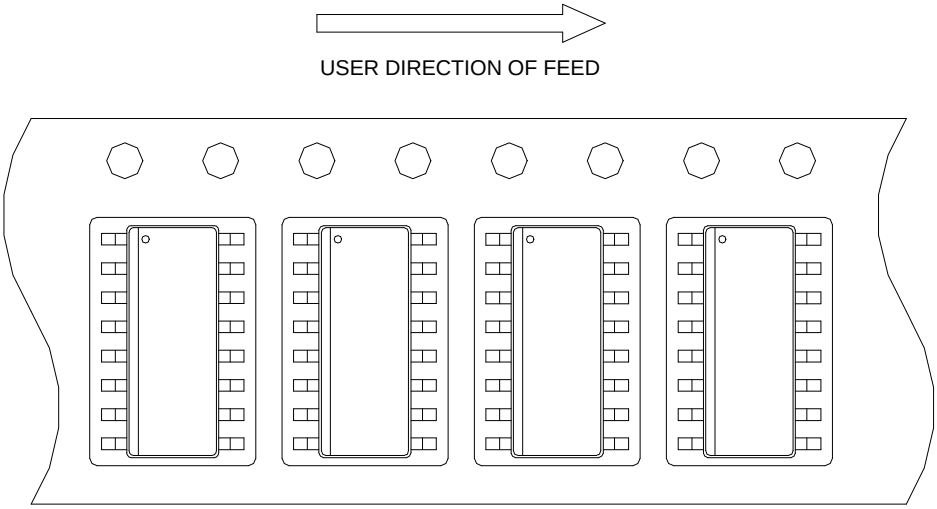
(mm)

Devices Per Unit

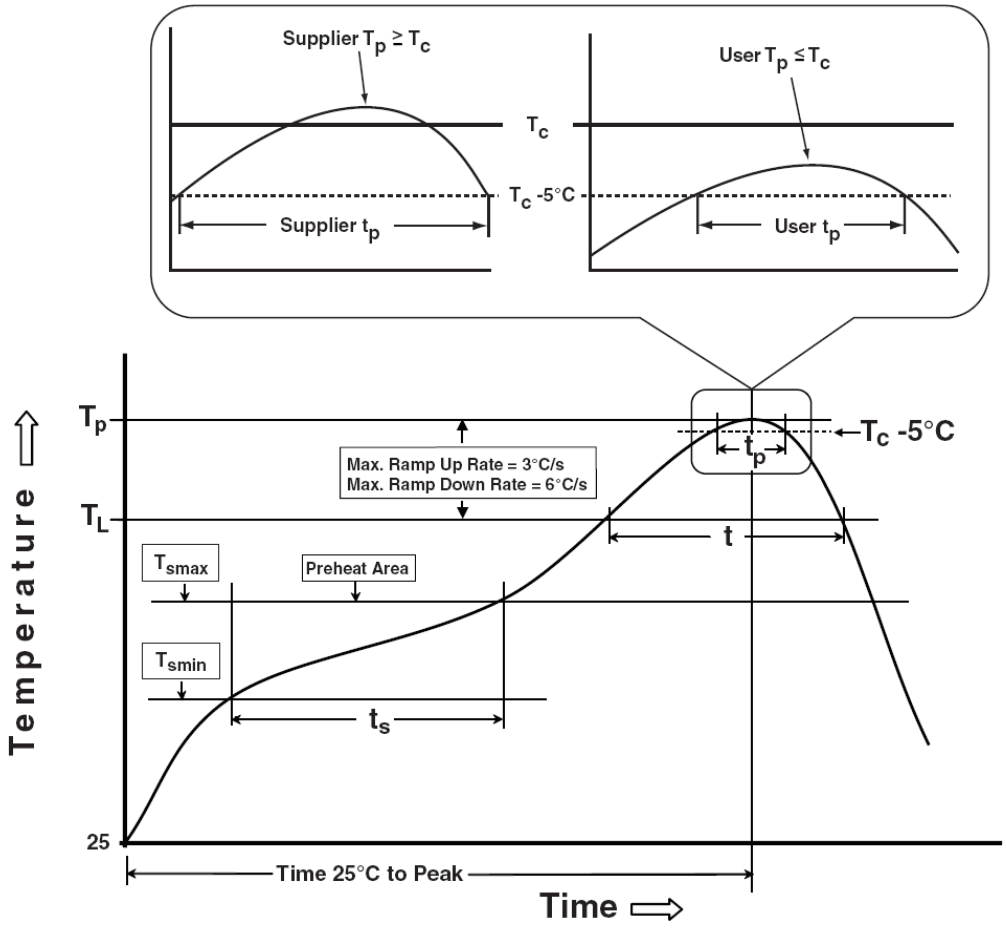
Package Type	Unit	Quantity
SOP-16P	Tape & Reel	2500

Taping Direction Information

SOP-16P



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	 100 °C 150 °C 60-120 seconds	 150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3 °C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 ³350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ T_j=125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM≧2KV
MM	JESD-22, A115	VMM≧200V
Latch-Up	JESD 78	10ms, 1_{tr}≧100mA

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