

# 8-bit Proprietary Microcontrollers

CMOS

## F<sup>2</sup>MC-8FX MB95110A Series

### MB95116A/F118AS/F118AW/FV100A-101

#### ■ DESCRIPTION

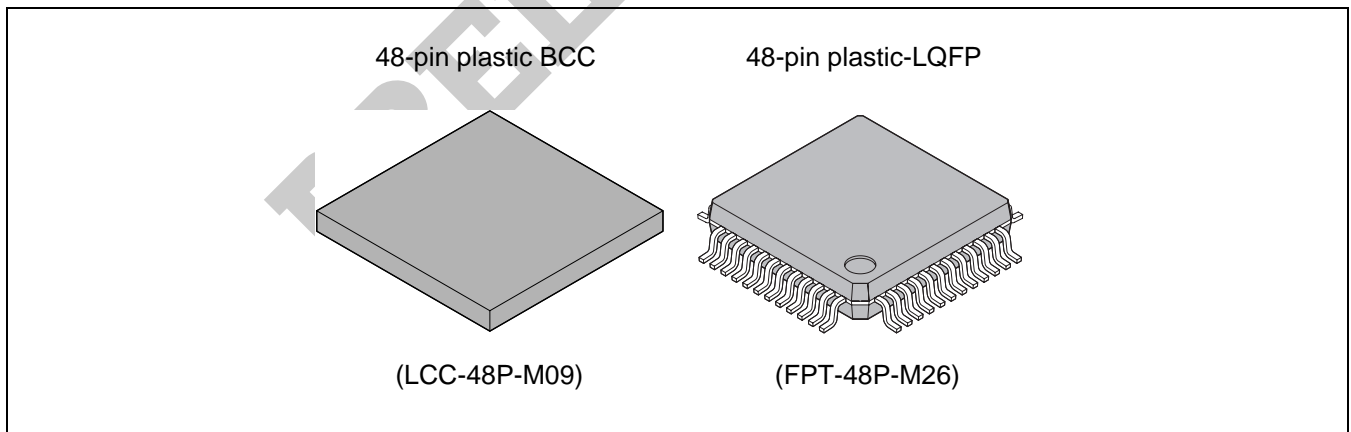
The MB95110A series is general-purpose, single-chip microcontrollers. In addition to a compact instruction set, the microcontrollers contain a variety of peripheral functions.

#### ■ FEATURES

- F<sup>2</sup>MC-8FX CPU core  
Instruction set that is optimum to the controllers
  - Multiplication and division instructions
  - 16-bit arithmetic operation
  - Bit test branch instruction
  - Bit manipulation instructions etc.
- Clock
  - Main clock
  - Main PLL clock
  - Subclock (for dual clock product)
  - Sub PLL clock (for dual clock product)

*(Continued)*

#### ■ PACKAGES



# MB95110A Series

(Continued)

- Timer
  - 8/16-bit compound timer × 2 channels
  - 8/16-bit PPG × 2 channels
  - 16-bit PPG
  - Timebase timer
  - Watch prescaler (for dual clock product)
- LIN-UART
  - Full duplex double buffer
  - Clock asynchronous or synchronous serial transfer capable
- UART/SIO
  - Clock asynchronous or synchronous serial transfer capable
- I<sup>2</sup>C\*
  - Built-in wake-up function
- External interrupt
  - Interrupt by edge detection (rising, falling, or both edges can be selected)
  - Can be used to recover from low-power consumption modes.
- 10-bit A/D converter
  - 10-bit resolution
- Low-power consumption (standby mode)
  - Stop mode
  - Sleep mode
  - Watch mode (for dual clock product)
  - Timebase timer mode
- I/O port: Max 40
  - General-purpose I/O ports (Nch open drain) : 2 ports
  - General-purpose I/O ports (CMOS) : 38 ports

\* : Purchase of Fujitsu I<sup>2</sup>C components conveys a license under the Philips I<sup>2</sup>C Patent Rights to use, these components in an I<sup>2</sup>C system provided that the system conforms to the I<sup>2</sup>C Standard Specification as defined by Philips.

# MB95110A Series

## ■ PRODUCT LINEUP

Part number		MB95116A	MB95F118AS	MB95F118AW	MB95FV100A-101
Parameter					
Type		MASK product	FLASH product		EVA product
ROM capacity		32 Kbytes	60 Kbytes		
RAM capacity		1 Kbytes	2 Kbytes		3.75 Kbytes
Reset output		No			
Option		Selectable single/dual -system*2	Single-system	Dual-system	Selectable single/dual -system*1
CPU functions		Number of basic instructions : 136 Instruction bit length : 8 bits Instruction length : 1 to 3 bytes Data bit length : 1, 8, and 16 bits Minimum instruction execution time : 0.1 μs (at internal 10 MHz) Interrupt processing time : 0.9 μs (at internal 10 MHz)			
Peripheral functions	Ports (Max 40 ports)	General-purpose I/O port (Nch open drain) : 2 ports General-purpose I/O port (CMOS) : 38 ports			
	Timebase timer	Interrupt cycle : 0.5 ms, 2.05 ms, 8.2 ms, 32.8 ms (at main oscillation clock 4 MHz)			
	Watchdog timer	Reset generated cycle At main oscillation clock 10 MHz : Minimum 105 ms At sub oscillation clock 32.768 kHz (for dual clock product) : Minimum 250 ms			
	Wild register	Capable of replacing 3 bytes of data			
	I <sup>2</sup> C bus	Master/slave sending and receiving Bus error function and arbitration function Detecting transmitting direction function Start condition repeated generation and detection functions Built-in wake-up function			
	UART/SIO	Data transfer capable in UART/SIO Full duplex double buffer, variable data length (5/6/7/8-bit), built-in baud rate generator Transfer rate : 2400 bps to 125000 bps (at machine clock 10 MHz) NRZ type transfer format, error detected function LSB-first or MSB-first can be selected. Clock synchronous (SIO) or clock asynchronous (UART) data transfer capable			
	LIN-UART	Dedicated reload timer allowing a wide range of communication speeds to be set. Capable of data transfer synchronous or asynchronous to clock signal. LIN functions available as the LIN master or LIN slave.			
	A/D converter (8 channels)	8-bit or 10-bit resolution can be selected.			
	8/16-bit compound timer (2 channels)	Each channel of the timer can be used as "8-bit timer × 2 channels" or "16-bit timer × 1 channel". Built-in timer function, PWC function, PWM function, capture function and square waveform output Count clock : 7 internal clocks and external clock can be selected.			

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# MB95110A Series

(Continued)

Part number		MB95116A	MB95F118AS	MB95F118AW	MB95FV100A-101
Parameter					
Peripheral functions	16-bit PPG	PWM mode or one-shot mode can be selected. Counter operating clock : Eight selectable clock sources Support for external trigger start			
	8/16-bit PPG (2 channels)	Each channel of the PPG can be used as "8-bit PPG × 2 channels" or "16-bit PPG × 1 channel". Counter operating clock : Eight selectable clock sources			
	Watch counter (for dual clock product)	Count clock : Four selectable clock sources (125ms, 250ms, 500ms, or 1s) Counter value can be set from 0 to 63. (Capable of counting for 1 minute)			
	Watch prescaler (for dual clock product)	Four selectable interval times (125 ms, 250 ms, 500 ms, or 1 s)			
	External interrupt (8 channels)	Interrupt by edge detection (rising, falling, or both edges can be selected) Can be used to recover from standby modes.			
Standby mode		Sleep, stop, watch, and timebase timer			

\*1 : Change by the switch on MCU board.

\*2 : Specify clock mode when ordering MASK ROM.

## ■ SELECT OF OSCILLATION STABILIZATION WAIT TIME (MASK PRODUCT ONLY)

For the MASK product, you can set the mask option when ordering MASK ROM to select the initial value of main clock oscillation stabilization wait time from among the following four values.

Note that the EVA and FLASH products are fixed their initial value of main clock oscillation stabilization wait time at the maximum value.

Selection of oscillation stabilization wait time	Remarks
$(2^2 - 2) / F_{CH}$	0.5 $\mu$ s (at main oscillation clock 4 MHz)
$(2^{12} - 2) / F_{CH}$	Approx. 1.02 ms (at main oscillation clock 4 MHz)
$(2^{13} - 2) / F_{CH}$	Approx. 2.05 ms (at main oscillation clock 4 MHz)
$(2^{14} - 2) / F_{CH}$	Approx. 4.10 ms (at main oscillation clock 4 MHz)

## ■ PACKAGES AND CORRESPONDING PRODUCTS

Part number Package	MB95116A	MB95F118AS	MB95F118AW	MB95FV100A-101
LCC-48P-M09	○	○	○	×
FPT-48P-M26	○	○	○	×
BGA-224P-M08	×	×	×	○

- : Available
- × : Unavailable

# MB95110A Series

## ■ DIFFERENCES AMONG PRODUCTS AND NOTES ON SELECTING PRODUCTS

### • Notes on Using EVA Products

The EVA product has not only the functions of the MB95110A series but also those of other products to support software development for multiple series and products of F<sup>2</sup>MC-8FX family. The I/O addresses for peripheral resources not used by the MB95110A series are therefore access-barred. Read/write access to these access-barred addresses may cause peripheral resources supposed to be unused to operate, resulting in unexpected malfunctions of hardware or software.

Take particular care not to use word, long word, or similar access to read or write odd numbered bytes in the prohibited areas.

Note that the values read from barred addresses are different between the EVA product and the FLASH or MASK product. Therefore, the data must not be used for software processing.

The EVA product does not support the functions of some bits in single-byte registers. Read/write access to these bits does not cause hardware malfunctions. Since the EVA, FLASH, and MASK products are designed to behave completely the same way in terms of hardware and software, you do not have to pay special attention to specific products.

### • Difference of Memory Spaces

If the amount of memory on the EVA product is different from that of the FLASH or MASK product, carefully check the difference in the amount of memory from the product to be actually used when developing software.

### • Current Consumption

- The current consumption of FLASH product is typically greater than for MASK product.
- For details of current consumption, refer to “■ ELECTRICAL CHARACTERISTICS”.

### • Package

For details of information on each package, see “■ PACKAGE DIMENSIONS”.

### • Operating voltage

The operating voltage are different among the EVA, FLASH and MASK products.

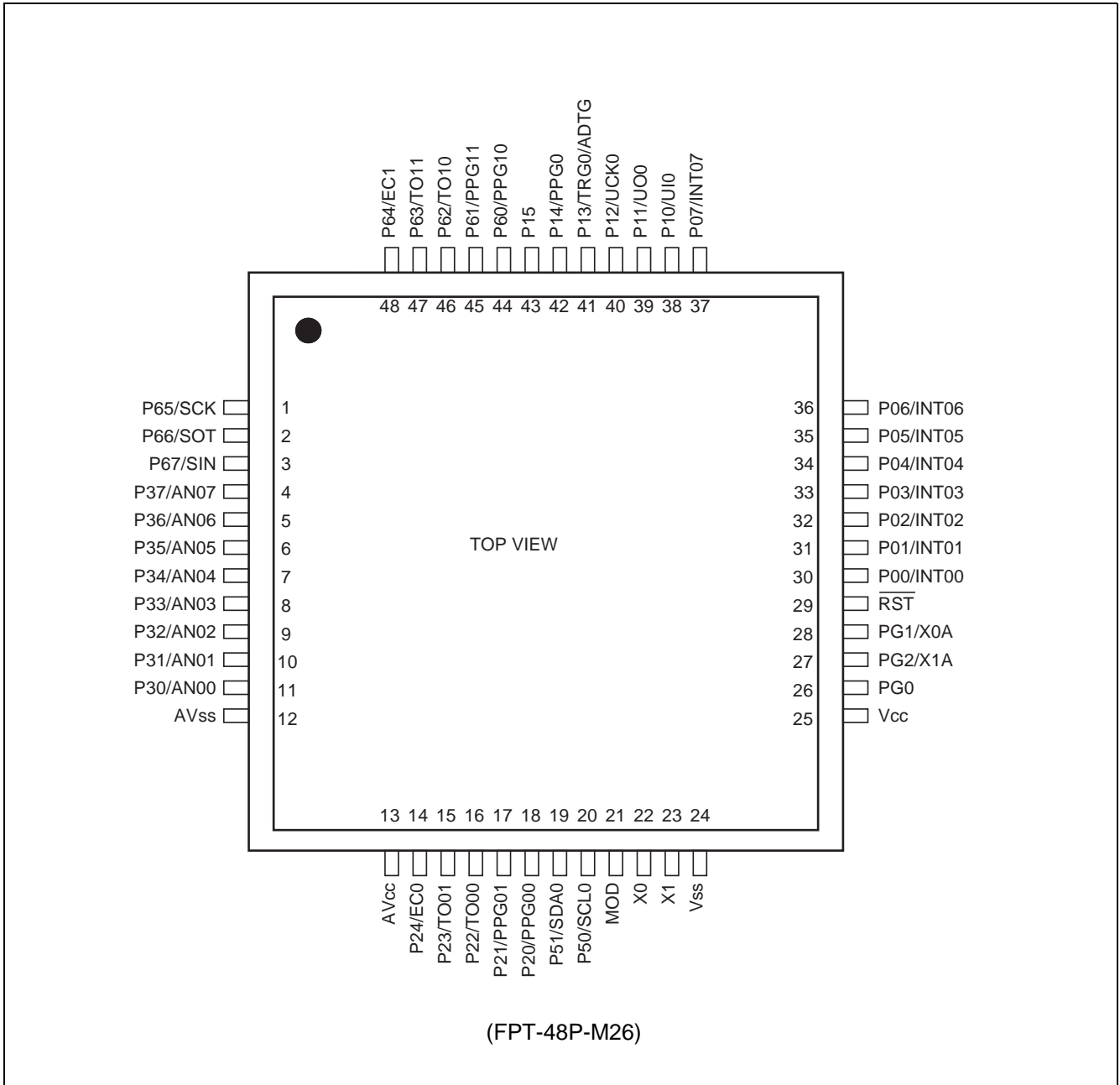
For details of operating voltage, refer to “■ ELECTRICAL CHARACTERISTICS”

### • Difference between $\overline{\text{RST}}$ and MOD pins

The  $\overline{\text{RST}}$  and MOD pins are hysteresis inputs on the MASK product. A pull-down resistor is provided for the MOD pin of the MASK product.



# MB95110A Series





## ■ PIN DESCRIPTION

Pin no.	Pin name	Circuit type	Description
1	P65/SCK	K	General-purpose I/O port. The pin is shared with LIN-UART clock I/O.
2	P66/SOT		General-purpose I/O port. The pin is shared with LIN-UART data output.
3	P67/SIN	L	General-purpose I/O port. The pin is shared with LIN-UART data input.
4	P37/AN07	J	General-purpose I/O port. The pins are shared with A/D analog input.
5	P36/AN06		
6	P35/AN05		
7	P34/AN04		
8	P33/AN03		
9	P32/AN02		
10	P31/AN01		
11	P30/AN00		
12	AVss	—	A/D power supply pin (GND)
13	AVcc	—	A/D power supply pin
14	P24/EC0	H	General-purpose I/O port. The pin is shared with 8/16-bit compound timer ch0 clock input.
15	P23/TO01		General-purpose I/O port. The pins are shared with 8/16-bit compound timer ch0 output.
16	P22/TO00		
17	P21/PPG01		
18	P20/PPG00		
19	P51/SDA0	I	General-purpose I/O port. The pin is shared with I <sup>2</sup> C ch0 data I/O.
20	P50/SCL0		General-purpose I/O port. The pin is shared with I <sup>2</sup> C ch0 clock I/O.
21	MOD	B	Operating mode designation pin
22	X0	A	Crystal oscillation pin
23	X1		
24	Vss	—	Power supply pin (GND)
25	Vcc	—	Power supply pin
26	PG0	H	General-purpose I/O port.
27	PG2/X1A	H/A	Single-system product is general-purpose port. Dual-system product is Crystal oscillation pin (32 kHz).
28	PG1/X0A		
29	$\overline{\text{RST}}$	B'	Reset pin

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# MB95110A Series

(Continued)

Pin no.	Pin name	Circuit type	Description	
30	P00/INT00	C	General-purpose I/O port. The pins are shared with external interrupt input. Large current port.	
31	P01/INT01			
32	P02/INT02			
33	P03/INT03			
34	P04/INT04			
35	P05/INT05			
36	P06/INT06			
37	P07/INT07			
38	P10/UI0	G	General-purpose I/O port. The pin is shared with UART/SIO ch0 data input.	
39	P11/UO0	H	General-purpose I/O port. The pin is shared with UART/SIO ch0 data output.	
40	P12/UCK0		General-purpose I/O port. The pin is shared with UART/SIO ch0 clock I/O.	
41	P13/TRG0/ ADTG		General-purpose I/O port. The pin is shared with 16-bit PPG ch0 trigger input (TRG0) and A/D trigger input (ADTG).	
42	P14/PPG0		General-purpose I/O port. The pin is shared with 16-bit PPG ch0 output.	
43	P15		General-purpose I/O port.	
44	P60/PPG10		K	General-purpose I/O port. The pins are shared with 8/16-bit PPG ch1 output.
45	P61/PPG11	K		General-purpose I/O port. The pins are shared with 8/16-bit compound timer ch1 output.
46	P62/TO10			
47	P63/TO11			
48	P64/EC1			

## ■ I/O CIRCUIT TYPE

Type	Circuit	Remarks
A	<p>X1 (X1A) X0 (X0A) Standby control</p>	<ul style="list-style-type: none"> <li>• Oscillation circuit</li> <li>• High-speed side Feedback resistance value : approx. 1 MΩ</li> <li>• Low-speed side Feedback resistance : approx. 24 MΩ (EVA product : approx. 10 MΩ) Dumping resistance : approx. 144 kΩ (EVA product : without dumping resistance)</li> </ul>
B	<p>R</p>	<ul style="list-style-type: none"> <li>• Only for input</li> <li>• Hysteresis input only for MASK product</li> <li>• With pull-down resistor only for MASK product</li> </ul>
B'		<ul style="list-style-type: none"> <li>• Hysteresis input only for MASK product</li> </ul>
C	<p>Pch Nch Standby control External interrupt enable</p>	<ul style="list-style-type: none"> <li>• CMOS output</li> <li>• Hysteresis input</li> </ul>
G	<p>R Pch Nch Pull-up control Standby control</p>	<ul style="list-style-type: none"> <li>• CMOS output</li> <li>• CMOS input</li> <li>• Hysteresis input</li> <li>• With pull-up control</li> </ul>

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# MB95110A Series

(Continued)

Type	Circuit	Remarks
H		<ul style="list-style-type: none"> <li>• CMOS output</li> <li>• Hysteresis input</li> <li>• With pull-up control</li> </ul>
I		<ul style="list-style-type: none"> <li>• Nch open drain output</li> <li>• CMOS input</li> <li>• Hysteresis input</li> </ul>
J		<ul style="list-style-type: none"> <li>• CMOS output</li> <li>• Hysteresis input</li> <li>• Analog input</li> <li>• With pull-up control</li> </ul>
K		<ul style="list-style-type: none"> <li>• CMOS output</li> <li>• Hysteresis input</li> </ul>
L		<ul style="list-style-type: none"> <li>• CMOS output</li> <li>• CMOS input</li> <li>• Hysteresis input</li> </ul>

## ■ HANDLING DEVICES

### • Preventing Latchup

Care must be taken to ensure that maximum voltage ratings are not exceeded when it is used.

Latchup may occur on CMOS ICs if voltage higher than  $V_{CC}$  or lower than  $V_{SS}$  is applied to input and output pins other than medium- and high-withstand voltage pins or if higher than the rating voltage is applied between  $V_{CC}$  and  $V_{SS}$ .

When latchup occurs, power supply current increases rapidly and might thermally damage elements.

Also, take care to prevent the analog power supply voltage ( $AV_{CC}$ ) and analog input voltage from exceeding the digital power supply voltage ( $V_{CC}$ ) when the analog system power supply is turned on or off.

### • Stable Supply Voltage

Supply voltage should be stabilized.

A sudden change in power-supply voltage may cause a malfunction even within the guaranteed operating range of the  $V_{CC}$  power-supply voltage.

For stabilization, in principle, keep the variation in  $V_{CC}$  ripple (p-p value) in a commercial frequency range (50 Hz to 60 Hz) not to exceed 10% of the  $V_{CC}$  value and suppress the voltage variation so that the transient variation rate does not exceed 0.1 V/ms during a momentary change such as when the power supply is switched.

### • Treatment of Unused Input Pin

An unused input pin may cause a malfunction if it is left open. It should be connected to a pull-up or pull-down resistor.

### • Treatment of Power Supply Pins on A/D Converter

Connect to be  $AV_{CC} = V_{CC}$  and  $AV_{SS} = V_{SS}$  even if the A/D converter is not in use.

### • Precautions for Use of External Clock

Even when an external clock is used, oscillation stabilization wait time is required for power-on reset, wake-up from subclock mode or stop mode.

### • Precaution against Noise to the External Reset Pin ( $\overline{RST}$ )

An input of a reset pulse below the specified level to the external reset pin ( $\overline{RST}$ ) may cause malfunctions. Be sure not to allow an input of a reset pulse below the specified level to the external reset pin ( $\overline{RST}$ ).

# MB95110A Series

## ■ PROGRAMMING FLASH MICROCONTROLLERS USING PARALLEL PROGRAMMER

### • Supported Parallel Programmers and Adapters

The following table lists supported parallel programmers and adapters.

Package	Applicable adapter model	Parallel programmers
FPT-48P-M26	TEF110-108F37AP	AF9708 (Ver 02.35G or more) AF9709/B (Ver 02.35G or more)
LCC-48P-M09	TEF100-108F41AP	AF9723+AF9834 (Ver 02.08E or more)

Notes: • Set all of the J1 to J3 switches on the adapter to "95F108".

- For information on applicable adapter models and parallel programmers, contact the following:  
Flash Support Group, Inc. TEL: 053-428-8380

### • Sector Configuration

The individual sectors of flash memory correspond to addresses used for CPU access and programming by the parallel programmer as follows:

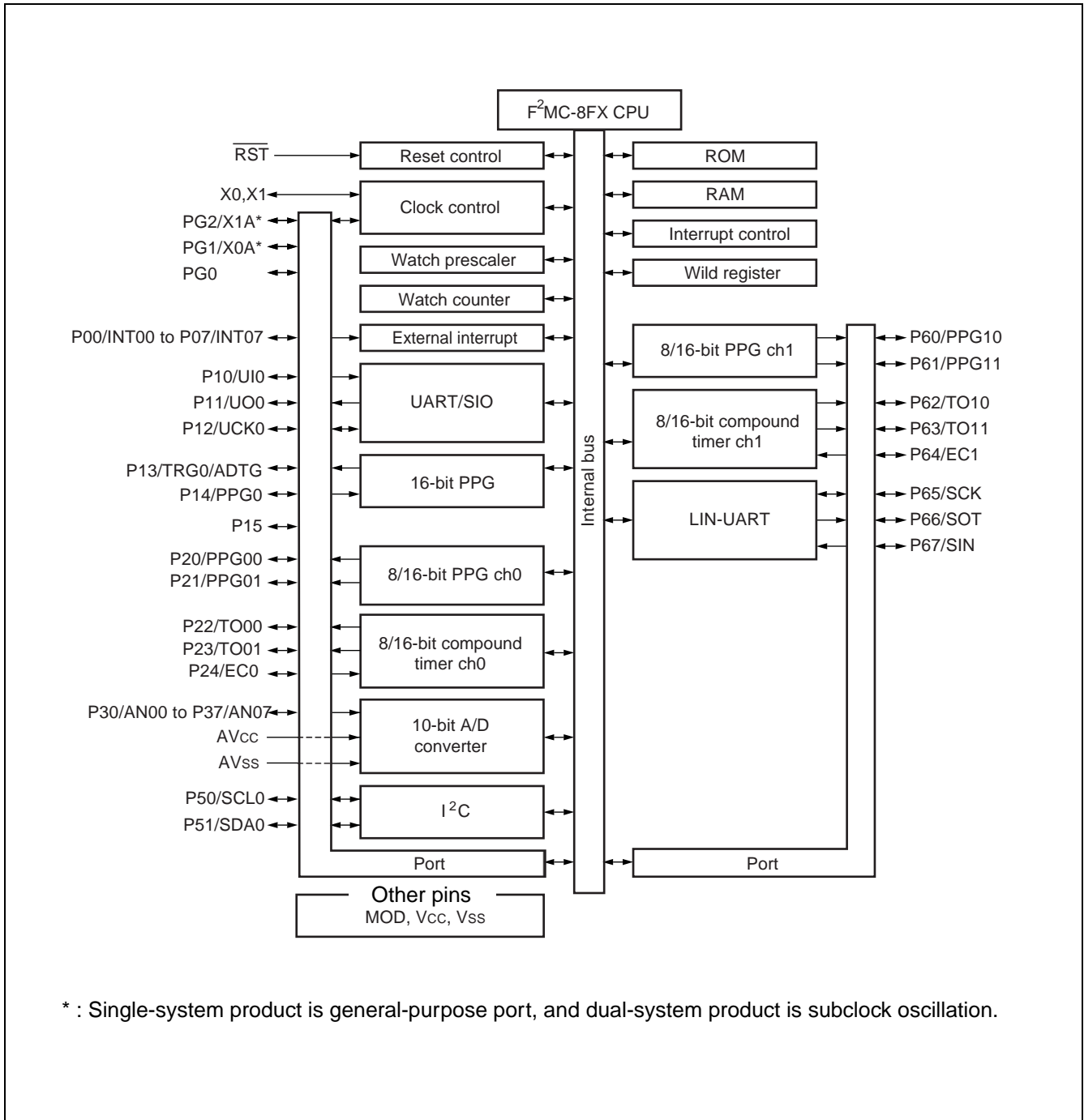
Flash memory	CPU address	Writer address*
SA1 (4 Kbytes)	1000 <sub>H</sub>	71000 <sub>H</sub>
SA2 (4 Kbytes)	1FFF <sub>H</sub>	71FFF <sub>H</sub>
	2000 <sub>H</sub>	72000 <sub>H</sub>
SA3 (4 Kbytes)	2FFF <sub>H</sub>	72FFF <sub>H</sub>
	3000 <sub>H</sub>	73000 <sub>H</sub>
SA4 (16 Kbytes)	3FFF <sub>H</sub>	73FFF <sub>H</sub>
	4000 <sub>H</sub>	74000 <sub>H</sub>
SA5 (16 Kbytes)	7FFF <sub>H</sub>	77FFF <sub>H</sub>
	8000 <sub>H</sub>	78000 <sub>H</sub>
SA6 (4 Kbytes)	BFFF <sub>H</sub>	7BFFF <sub>H</sub>
	C000 <sub>H</sub>	7C000 <sub>H</sub>
SA7 (4 Kbytes)	CFFF <sub>H</sub>	7CFFF <sub>H</sub>
	D000 <sub>H</sub>	7D000 <sub>H</sub>
SA8 (4 Kbytes)	DFFF <sub>H</sub>	7DFFF <sub>H</sub>
	E000 <sub>H</sub>	7E000 <sub>H</sub>
SA9 (4 Kbytes)	EFFF <sub>H</sub>	7EFFF <sub>H</sub>
	F000 <sub>H</sub>	7F000 <sub>H</sub>
	FFF <sub>H</sub>	7FFF <sub>H</sub>

\*: Programmer addresses are equivalent to CPU addresses, used when the parallel programmer programs data into flash memory.  
These programmer addresses are used for the parallel programmer to program or erase data in flash memory.

### • Programming Method

- 1) Set the type code of the parallel programmer to 17226.
- 2) Load program data to programmer addresses 71000<sub>H</sub> to 7FFFF<sub>H</sub>.
- 3) Programmed by parallel programmer

## ■ BLOCK DIAGRAM

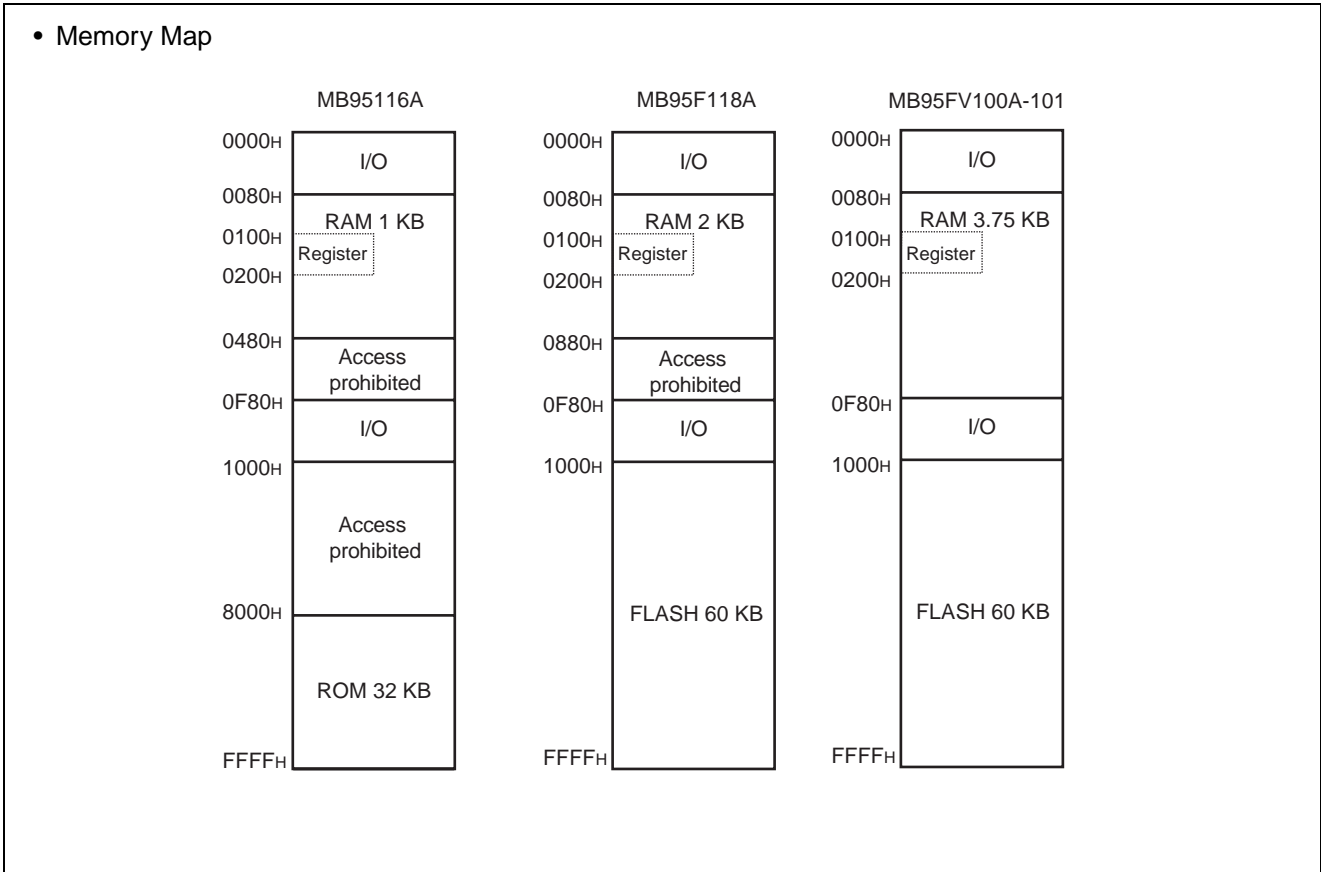


# MB95110A Series

## ■ CPU CORE

### 1. Memory space

Memory space of the MB95110A series is 64 Kbytes and consists of I/O area, data area, and program area. The memory space includes special-purpose areas such as the general-purpose registers and vector table. Memory map of the MB95110A series shown in below.





## 2. Register

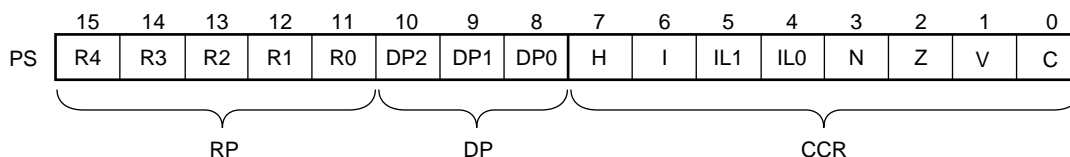
The MB95110A series has two types of registers; dedicated registers in the CPU and general-purpose registers in the memory. The dedicated registers are as follows:

- Program counter (PC) : A 16-bit register to indicate locations where instructions are stored.
- Accumulator (A) : A 16-bit register for temporary storage of arithmetic operations. In the case of an 8-bit data processing instruction, the lower one byte is used.
- Temporary accumulator (T) : A 16-bit register which performs arithmetic operations with the accumulator. In the case of an 8-bit data processing instruction, the lower one byte is used.
- Index register (IX) : A 16-bit register for index modification
- Extra pointer (EP) : A 16-bit pointer to point to a memory address.
- Stack pointer (SP) : A 16-bit register to indicate a stack area.
- Program status (PS) : A 16-bit register for storing a register bank pointer, a direct bank pointer, and a condition code register

Register	Initial Value
PC	FFFD <sub>H</sub>
A	0000 <sub>H</sub>
T	0000 <sub>H</sub>
IX	0000 <sub>H</sub>
EP	0000 <sub>H</sub>
SP	0000 <sub>H</sub>
PS	0030 <sub>H</sub>

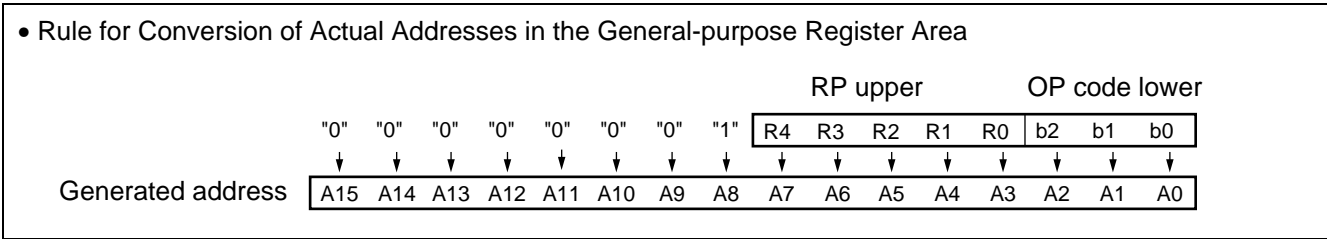
The PS can further be divided into higher 8 bits for use as a register bank pointer (RP) and a direct bank pointer (DP) and the lower 8 bits for use as a condition code register (CCR). (See the diagram below.)

- Structure of the program status



# MB95110A Series

The RP indicates the address of the register bank currently being used. The relationship between the content of RP and the real address conforms to the conversion rule illustrated below:



The DP specifies the area for mapping instructions (16 different instructions such as MOV A, dir) using direct addresses to 0080H to 00FFH.

Direct bank pointer (DP2 to DP0)	Specified address area	Mapping area
Don't care	0000H to 007FH	0000H to 007FH (without mapping)
000B (initial value)	0080H to 00FFH	0080H to 00FFH (without mapping)
001B		0100H to 017FH
010B		0180H to 01FFH
011B		0200H to 027FH
100B		0280H to 02FFH
101B		0300H to 037FH
110B		0380H to 03FFH
111B		0400H to 047FH

The CCR consists of the bits indicating arithmetic operation results or transfer data contents and the bits that control CPU operations at interrupt.

- H flag : Set to "1" when a carry or a borrow from bit 3 to bit 4 occurs as a result of an arithmetic operation. Cleared to "0" otherwise. This flag is for decimal adjustment instructions.
- I flag : Interrupt is enabled when this flag is set to "1". Interrupt is disabled when this flag is set to "0". The flag is set to "0" when reset.
- IL1, IL0 : Indicates the level of the interrupt currently enabled. Processes an interrupt only if its request level is higher than the value indicated by this bit.

IL1	IL0	Interrupt level	Priority
0	0	0	High ↑ ↓ Low = no interruption
0	1	1	
1	0	2	
1	1	3	

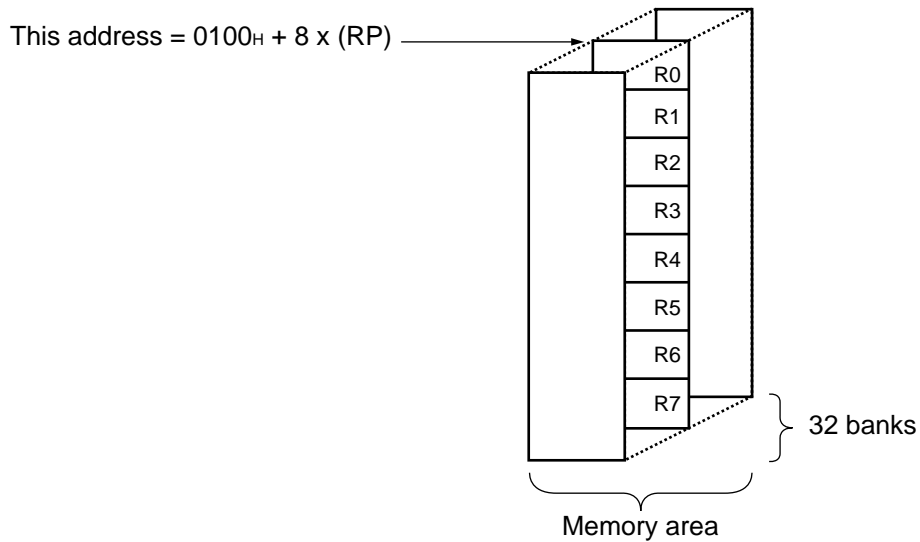
- N flag : Set to "1" if the MSB is set to "1" as the result of an arithmetic operation. Cleared to "0" when the bit is set to "0".
- Z flag : Set to "1" when an arithmetic operation results in 0. Cleared to "0" otherwise.
- V flag : Set to "1" if the complement on 2 overflows as a result of an arithmetic operation. Cleared to "0" otherwise.
- C flag : Set to "1" when a carry or a borrow from bit 7 occurs as a result of an arithmetic operation. Cleared to "0" otherwise. Set to the shift-out value in the case of a shift instruction.

The following general-purpose registers are provided:

General-purpose registers: 8-bit data storage registers

The general-purpose registers are 8 bits and located in the register banks on the memory. One bank contains eight registers. Up to a total of 32 banks can be used on the MB95110A series. The bank currently in use is indicated by the register bank pointer (RP).

- Register Bank Configuration



# MB95110A Series

## ■ I/O MAP

Address	Register abbreviation	Register name	R/W	Initial value
0000 <sub>H</sub>	PDR0	Port 0 data register	R/W	00000000 <sub>B</sub>
0001 <sub>H</sub>	DDR0	Port 0 direction register	R/W	00000000 <sub>B</sub>
0002 <sub>H</sub>	PDR1	Port 1 data register	R/W	00000000 <sub>B</sub>
0003 <sub>H</sub>	DDR1	Port 1 direction register	R/W	00000000 <sub>B</sub>
0004 <sub>H</sub>	—	(Vacancy)	—	—
0005 <sub>H</sub>	WATR	Oscillation stabilization wait time setting register	R/W	11111111 <sub>B</sub>
0006 <sub>H</sub>	PLL	PLL control register	R/W	00000000 <sub>B</sub>
0007 <sub>H</sub>	SYCC	System clock control register	R/W	1010X011 <sub>B</sub>
0008 <sub>H</sub>	STBC	Standby control register	R/W	00000000 <sub>B</sub>
0009 <sub>H</sub>	RSRR	Reset source register	R	XXXXXXXX <sub>B</sub>
000A <sub>H</sub>	TBTC	Timebase timer control register	R/W	00000000 <sub>B</sub>
000B <sub>H</sub>	WPCR	Watch prescaler control register	R/W	00000000 <sub>B</sub>
000C <sub>H</sub>	WDTC	Watchdog timer control register	R/W	00000000 <sub>B</sub>
000D <sub>H</sub>	—	(Vacancy)	—	—
000E <sub>H</sub>	PDR2	Port 2 data register	R/W	00000000 <sub>B</sub>
000F <sub>H</sub>	DDR2	Port 2 direction register	R/W	00000000 <sub>B</sub>
0010 <sub>H</sub>	PDR3	Port 3 data register	R/W	00000000 <sub>B</sub>
0011 <sub>H</sub>	DDR3	Port 3 direction register	R/W	00000000 <sub>B</sub>
0012 <sub>H</sub>	—	(Vacancy)	—	—
0013 <sub>H</sub>				
0014 <sub>H</sub>	PDR5	Port 5 data register	R/W	00000000 <sub>B</sub>
0015 <sub>H</sub>	DDR5	Port 5 direction register	R/W	00000000 <sub>B</sub>
0016 <sub>H</sub>	PDR6	Port 6 data register	R/W	00000000 <sub>B</sub>
0017 <sub>H</sub>	DDR6	Port 6 direction register	R/W	00000000 <sub>B</sub>
0018 <sub>H</sub> to 0029 <sub>H</sub>	—	(Vacancy)	—	—
002A <sub>H</sub>	PDRG	Port G data register	R/W	00000000 <sub>B</sub>
002B <sub>H</sub>	DDRG	Port G direction register	R/W	00000000 <sub>B</sub>
002C <sub>H</sub>	—	(Vacancy)	—	—
002D <sub>H</sub>	PUL1	Port 1 pull-up register	R/W	00000000 <sub>B</sub>
002E <sub>H</sub>	PUL2	Port 2 pull-up register	R/W	00000000 <sub>B</sub>
002F <sub>H</sub>	PUL3	Port 3 pull-up register	R/W	00000000 <sub>B</sub>
0030 <sub>H</sub> to 0034 <sub>H</sub>	—	(Vacancy)	—	—

(Continued)

# MB95110A Series

Address	Register abbreviation	Register name	R/W	Initial value
0035 <sub>H</sub>	PULG	Port G pull-up register	R/W	00000000 <sub>B</sub>
0036 <sub>H</sub>	T01CR1	8/16-bit compound timer 01 control status register 1 ch0	R/W	00000000 <sub>B</sub>
0037 <sub>H</sub>	T00CR1	8/16-bit compound timer 00 control status register 1 ch0	R/W	00000000 <sub>B</sub>
0038 <sub>H</sub>	T11CR1	8/16-bit compound timer 11 control status register 1 ch1	R/W	00000000 <sub>B</sub>
0039 <sub>H</sub>	T10CR1	8/16-bit compound timer 10 control status register 1 ch1	R/W	00000000 <sub>B</sub>
003A <sub>H</sub>	PC01	8/16-bit PPG1 control register ch0	R/W	00000000 <sub>B</sub>
003B <sub>H</sub>	PC00	8/16-bit PPG0 control register ch0	R/W	00000000 <sub>B</sub>
003C <sub>H</sub>	PC11	8/16-bit PPG1 control register ch1	R/W	00000000 <sub>B</sub>
003D <sub>H</sub>	PC10	8/16-bit PPG0 control register ch1	R/W	00000000 <sub>B</sub>
003E <sub>H</sub> to 0041 <sub>H</sub>	—	(Vacancy)	—	—
0042 <sub>H</sub>	PCNTH0	16-bit PPG status control register (Upper byte) ch0	R/W	00000000 <sub>B</sub>
0043 <sub>H</sub>	PCNTL0	16-bit PPG status control register (Lower byte) ch0	R/W	00000000 <sub>B</sub>
0044 <sub>H</sub> to 0047 <sub>H</sub>	—	(Vacancy)	—	—
0048 <sub>H</sub>	EIC00	External interrupt circuit control register ch0/1	R/W	00000000 <sub>B</sub>
0049 <sub>H</sub>	EIC10	External interrupt circuit control register ch2/3	R/W	00000000 <sub>B</sub>
004A <sub>H</sub>	EIC20	External interrupt circuit control register ch4/5	R/W	00000000 <sub>B</sub>
004B <sub>H</sub>	EIC30	External interrupt circuit control register ch6/7	R/W	00000000 <sub>B</sub>
004C <sub>H</sub> to 004F <sub>H</sub>	—	(Vacancy)	—	—
0050 <sub>H</sub>	SCR	LIN-UART serial control register	R/W	00000000 <sub>B</sub>
0051 <sub>H</sub>	SMR	LIN-UART serial mode register	R/W	00000000 <sub>B</sub>
0052 <sub>H</sub>	SSR	LIN-UART serial status register	R/W	00001000 <sub>B</sub>
0053 <sub>H</sub>	RDR/TDR	LIN-UART reception/transmission data register	R/W	00000000 <sub>B</sub>
0054 <sub>H</sub>	ESCR	LIN-UART extended status control register	R/W	00000100 <sub>B</sub>
0055 <sub>H</sub>	ECCR	LIN-UART extended communication control register	R/W	000000XX <sub>B</sub>
0056 <sub>H</sub>	SMC10	UART/SIO serial mode control register 1 ch0	R/W	00000000 <sub>B</sub>
0057 <sub>H</sub>	SMC20	UART/SIO serial mode control register 2 ch0	R/W	00100000 <sub>B</sub>
0058 <sub>H</sub>	SSR0	UART/SIO serial status register ch0	R/W	00000001 <sub>B</sub>
0059 <sub>H</sub>	TDR0	UART/SIO serial output data register ch0	R/W	00000000 <sub>B</sub>
005A <sub>H</sub>	RDR0	UART/SIO serial input data register ch0	R	00000000 <sub>B</sub>
005B <sub>H</sub> to 005F <sub>H</sub>	—	(Vacancy)	—	—

(Continued)

# MB95110A Series

Address	Register abbreviation	Register name	R/W	Initial value
0060 <sub>H</sub>	IBCR00	I <sup>2</sup> C bus control register 0 ch0	R/W	00000000 <sub>B</sub>
0061 <sub>H</sub>	IBCR10	I <sup>2</sup> C bus control register 1 ch0	R/W	00000000 <sub>B</sub>
0062 <sub>H</sub>	IBSR0	I <sup>2</sup> C bus status register ch0	R	00000000 <sub>B</sub>
0063 <sub>H</sub>	IDDR0	I <sup>2</sup> C data register ch0	R/W	00000000 <sub>B</sub>
0064 <sub>H</sub>	IAAR0	I <sup>2</sup> C address register ch0	R/W	00000000 <sub>B</sub>
0065 <sub>H</sub>	ICCR0	I <sup>2</sup> C clock control register ch0	R/W	00000000 <sub>B</sub>
0066 <sub>H</sub> to 006B <sub>H</sub>	—	(Vacancy)	—	—
006C <sub>H</sub>	ADC1	A/D control register 1	R/W	00000000 <sub>B</sub>
006D <sub>H</sub>	ADC2	A/D control register 2	R/W	00000000 <sub>B</sub>
006E <sub>H</sub>	ADDH	A/D data register (Upper byte)	R/W	00000000 <sub>B</sub>
006F <sub>H</sub>	ADDL	A/D data register (Lower byte)	R/W	00000000 <sub>B</sub>
0070 <sub>H</sub>	WCSR	Watch counter status register	R/W	00000000 <sub>B</sub>
0071 <sub>H</sub>	—	(Vacancy)	—	—
0072 <sub>H</sub>	FSR	Flash memory status register	R/W	000X0000 <sub>B</sub>
0073 <sub>H</sub>	SWRE0	Flash memory sector writing control register 0	R/W	00000000 <sub>B</sub>
0074 <sub>H</sub>	SWRE1	Flash memory sector writing control register 1	R/W	00000000 <sub>B</sub>
0075 <sub>H</sub>	—	(Vacancy)	—	—
0076 <sub>H</sub>	WREN	Wild register address compare enable register	R/W	00000000 <sub>B</sub>
0077 <sub>H</sub>	WROR	Wild register data test setting register	R/W	00000000 <sub>B</sub>
0078 <sub>H</sub>	—	(Mirror of register bank pointer (RP) and direct bank pointer (DP) )	—	—
0079 <sub>H</sub>	ILR0	Interrupt level setting register 0	R/W	11111111 <sub>B</sub>
007A <sub>H</sub>	ILR1	Interrupt level setting register 1	R/W	11111111 <sub>B</sub>
007B <sub>H</sub>	ILR2	Interrupt level setting register 2	R/W	11111111 <sub>B</sub>
007C <sub>H</sub>	ILR3	Interrupt level setting register 3	R/W	11111111 <sub>B</sub>
007D <sub>H</sub>	ILR4	Interrupt level setting register 4	R/W	11111111 <sub>B</sub>
007E <sub>H</sub>	ILR5	Interrupt level setting register 5	R/W	11111111 <sub>B</sub>
007F <sub>H</sub>	—	(Vacancy)	—	—
0F80 <sub>H</sub>	WRARH0	Wild register address setting register (Upper byte) ch0	R/W	00000000 <sub>B</sub>
0F81 <sub>H</sub>	WRARL0	Wild register address setting register (Lower byte) ch0	R/W	00000000 <sub>B</sub>
0F82 <sub>H</sub>	WRDR0	Wild register data setting register ch0	R/W	00000000 <sub>B</sub>
0F83 <sub>H</sub>	WRARH1	Wild register address setting register (Upper byte) ch1	R/W	00000000 <sub>B</sub>
0F84 <sub>H</sub>	WRARL1	Wild register address setting register (Lower byte) ch1	R/W	00000000 <sub>B</sub>
0F85 <sub>H</sub>	WRDR1	Wild register data setting register ch1	R/W	00000000 <sub>B</sub>

(Continued)

# MB95110A Series

Address	Register abbreviation	Register name	R/W	Initial value
0F86 <sub>H</sub>	WRARH2	Wild register address setting register (Upper byte) ch2	R/W	00000000 <sub>B</sub>
0F87 <sub>H</sub>	WRARL2	Wild register address setting register (Lower byte) ch2	R/W	00000000 <sub>B</sub>
0F88 <sub>H</sub>	WRDR2	Wild register data setting register ch2	R/W	00000000 <sub>B</sub>
0F89 <sub>H</sub> to 0F91 <sub>H</sub>	—	(Vacancy)	—	—
0F92 <sub>H</sub>	T01CR0	8/16-bit compound timer 01 control status register 0 ch0	R/W	00000000 <sub>B</sub>
0F93 <sub>H</sub>	T00CR0	8/16-bit compound timer 00 control status register 0 ch0	R/W	00000000 <sub>B</sub>
0F94 <sub>H</sub>	T01DR	8/16-bit compound timer 01 data register ch0	R/W	00000000 <sub>B</sub>
0F95 <sub>H</sub>	T00DR	8/16-bit compound timer 00 data register ch0	R/W	00000000 <sub>B</sub>
0F96 <sub>H</sub>	TMCR0	8/16-bit compound timer 00/01 timer mode control register ch0	R/W	00000000 <sub>B</sub>
0F97 <sub>H</sub>	T11CR0	8/16-bit compound timer 11 control status register 0 ch1	R/W	00000000 <sub>B</sub>
0F98 <sub>H</sub>	T10CR0	8/16-bit compound timer 10 control status register 0 ch1	R/W	00000000 <sub>B</sub>
0F99 <sub>H</sub>	T11DR	8/16-bit compound timer 11 data register ch1	R/W	00000000 <sub>B</sub>
0F9A <sub>H</sub>	T10DR	8/16-bit compound timer 10 data register ch1	R/W	00000000 <sub>B</sub>
0F9B <sub>H</sub>	TMCR1	8/16-bit compound timer 10/11 timer mode control register ch1	R/W	00000000 <sub>B</sub>
0F9C <sub>H</sub>	PPS01	8/16-bit PPG1 cycle setting buffer register ch0	R/W	11111111 <sub>B</sub>
0F9D <sub>H</sub>	PPS00	8/16-bit PPG0 cycle setting buffer register ch0	R/W	11111111 <sub>B</sub>
0F9E <sub>H</sub>	PDS01	8/16-bit PPG1 duty setting buffer register ch0	R/W	11111111 <sub>B</sub>
0F9F <sub>H</sub>	PDS00	8/16-bit PPG0 duty setting buffer register ch0	R/W	11111111 <sub>B</sub>
0FA0 <sub>H</sub>	PPS11	8/16-bit PPG1 cycle setting buffer register ch1	R/W	11111111 <sub>B</sub>
0FA1 <sub>H</sub>	PPS10	8/16-bit PPG0 cycle setting buffer register ch1	R/W	11111111 <sub>B</sub>
0FA2 <sub>H</sub>	PDS11	8/16-bit PPG1 duty setting buffer register ch1	R/W	11111111 <sub>B</sub>
0FA3 <sub>H</sub>	PDS10	8/16-bit PPG0 duty setting buffer register ch1	R/W	11111111 <sub>B</sub>
0FA4 <sub>H</sub>	PPGS	8/16-bit PPG starting register	R/W	00000000 <sub>B</sub>
0FA5 <sub>H</sub>	REVC	8/16-bit PPG output inversion register	R/W	00000000 <sub>B</sub>
0FA6 <sub>H</sub> to 0FA9 <sub>H</sub>	—	(Vacancy)	—	—
0FAA <sub>H</sub>	PDCRH0	16-bit PPG down counter register (Upper byte) ch0	R	00000000 <sub>B</sub>
0FAB <sub>H</sub>	PDCRL0	16-bit PPG down counter register (Lower byte) ch0	R	00000000 <sub>B</sub>
0FAC <sub>H</sub>	PCSRH0	16-bit PPG cycle setting buffer register (Upper byte) ch0	R/W	11111111 <sub>B</sub>
0FAD <sub>H</sub>	PCSRL0	16-bit PPG cycle setting buffer register (Lower byte) ch0	R/W	11111111 <sub>B</sub>
0FAE <sub>H</sub>	PDUTH0	16-bit PPG duty setting buffer register (Upper byte) ch0	R/W	11111111 <sub>B</sub>
0FAF <sub>H</sub>	PDUTL0	16-bit PPG duty setting buffer register (Lower byte) ch0	R/W	11111111 <sub>B</sub>

(Continued)

# MB95110A Series

(Continued)

Address	Register abbreviation	Register name	R/W	Initial value
0FB0 <sub>H</sub> to 0FBB <sub>H</sub>	—	(Vacancy)	—	—
0FBC <sub>H</sub>	BGR1	LIN-UART baud rate generator register 1	R/W	00000000 <sub>B</sub>
0FBD <sub>H</sub>	BGR0	LIN-UART baud rate generator register 0	R/W	00000000 <sub>B</sub>
0FBE <sub>H</sub>	PSSR0	UART/SIO prescaler selection register ch0	R/W	00000000 <sub>B</sub>
0FBF <sub>H</sub>	BRSR0	UART/SIO baud rate setting register ch0	R/W	00000000 <sub>B</sub>
0FC0 <sub>H</sub> to 0FC2 <sub>H</sub>	—	(Vacancy)	—	—
0FC3 <sub>H</sub>	AIDRL	A/D input disable register (Lower byte)	R/W	00000000 <sub>B</sub>
0FC4 <sub>H</sub> to 0FE2 <sub>H</sub>	—	(Vacancy)	—	—
0FE3 <sub>H</sub>	WCDR	Watch counter data register	R/W	00111111 <sub>B</sub>
0FE4 <sub>H</sub> to 0FED <sub>H</sub>	—	(Vacancy)	—	—
0FEE <sub>H</sub>	ILSR	Input level select register	R/W	00000000 <sub>B</sub>
0FEF <sub>H</sub>	WICR	Interrupt pin control register	R/W	01000000 <sub>B</sub>
0FF0 <sub>H</sub> to 0FFF <sub>H</sub>	—	(Vacancy)	—	—

- Read/write access symbols

R/W : Readable and Writable

R : Read only

W : Write only

- Initial value symbols


0 : The initial value of this bit is "0".

1 : The initial value of this bit is "1".

X : The initial value of this bit is undefined.



## ■ INTERRUPT SOURCE TABLE

Interrupt source	Interrupt request number	Vector table address		Bit name of interrupt level setting register	Same level priority order (at simultaneous occurrence)
		Upper	Lower		
External interrupt ch0	IRQ0	FFFA <sub>H</sub>	FFFB <sub>H</sub>	L00 [1 : 0]	<div style="text-align: center;">                     High                         Low                 </div>
External interrupt ch4					
External interrupt ch1	IRQ1	FFF8 <sub>H</sub>	FFF9 <sub>H</sub>	L01 [1 : 0]	
External interrupt ch5					
External interrupt ch2	IRQ2	FFF6 <sub>H</sub>	FFF7 <sub>H</sub>	L02 [1 : 0]	
External interrupt ch6					
External interrupt ch3	IRQ3	FFF4 <sub>H</sub>	FFF5 <sub>H</sub>	L03 [1 : 0]	
External interrupt ch7					
UART/SIO ch0	IRQ4	FFF2 <sub>H</sub>	FFF3 <sub>H</sub>	L04 [1 : 0]	
8/16-bit compound timer ch0 (Lower)	IRQ5	FFF0 <sub>H</sub>	FFF1 <sub>H</sub>	L05 [1 : 0]	
8/16-bit compound timer ch0 (Upper)	IRQ6	FFEE <sub>H</sub>	FFEF <sub>H</sub>	L06 [1 : 0]	
LIN-UART (reception)	IRQ7	FFEC <sub>H</sub>	FFED <sub>H</sub>	L07 [1 : 0]	
LIN-UART (transmission)	IRQ8	FFEA <sub>H</sub>	FFEB <sub>H</sub>	L08 [1 : 0]	
8/16-bit PPG ch1 (Lower)	IRQ9	FFE8 <sub>H</sub>	FFE9 <sub>H</sub>	L09 [1 : 0]	
8/16-bit PPG ch1 (Upper)	IRQ10	FFE6 <sub>H</sub>	FFE7 <sub>H</sub>	L10 [1 : 0]	
(Unused)	IRQ11	FFE4 <sub>H</sub>	FFE5 <sub>H</sub>	L11 [1 : 0]	
8/16-bit PPG ch0 (Upper)	IRQ12	FFE2 <sub>H</sub>	FFE3 <sub>H</sub>	L12 [1 : 0]	
8/16-bit PPG ch0 (Lower)	IRQ13	FFE0 <sub>H</sub>	FFE1 <sub>H</sub>	L13 [1 : 0]	
8/16-bit compound timer ch1 (Upper)	IRQ14	FFDE <sub>H</sub>	FFDF <sub>H</sub>	L14 [1 : 0]	
16-bit PPG ch0	IRQ15	FFDC <sub>H</sub>	FFDD <sub>H</sub>	L15 [1 : 0]	
I <sup>2</sup> C ch0	IRQ16	FFDA <sub>H</sub>	FFDB <sub>H</sub>	L16 [1 : 0]	
(Unused)	IRQ17	FFD8 <sub>H</sub>	FFD9 <sub>H</sub>	L17 [1 : 0]	
10-bit A/D converter	IRQ18	FFD6 <sub>H</sub>	FFD7 <sub>H</sub>	L18 [1 : 0]	
Timebase timer	IRQ19	FFD4 <sub>H</sub>	FFD5 <sub>H</sub>	L19 [1 : 0]	
Watch prescaler/counter	IRQ20	FFD2 <sub>H</sub>	FFD3 <sub>H</sub>	L20 [1 : 0]	
(Unused)	IRQ21	FFD0 <sub>H</sub>	FFD1 <sub>H</sub>	L21 [1 : 0]	
8/16-bit compound timer ch1 (Lower)	IRQ22	FFCE <sub>H</sub>	FFCF <sub>H</sub>	L22 [1 : 0]	
FLASH	IRQ23	FFCC <sub>H</sub>	FFCD <sub>H</sub>	L23 [1 : 0]	

# MB95110A Series

## ■ ELECTRICAL CHARACTERISTICS

### 1. Absolute Maximum Ratings

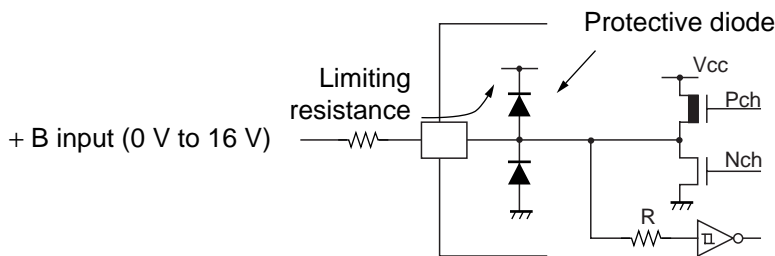
Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage*1	V <sub>CC</sub> , AV <sub>CC</sub>	V <sub>SS</sub> - 0.3	V <sub>SS</sub> + 4.0	V	*2
	AV <sub>R</sub>	V <sub>SS</sub> - 0.3	V <sub>SS</sub> + 4.0		*2 MB95FV100A-101 only
Input voltage*1	V <sub>I1</sub>	V <sub>SS</sub> - 0.3	V <sub>SS</sub> + 4.0	V	Other than P50, P51*3
	V <sub>I2</sub>	V <sub>SS</sub> - 0.3	V <sub>SS</sub> + 6.0		P50, P51
Output voltage*1	V <sub>O</sub>	V <sub>SS</sub> - 0.3	V <sub>SS</sub> + 4.0	V	*3
Maximum clamp current	I <sub>CLAMP</sub>	- 2.0	+ 2.0	mA	Applicable to pins*4
Total maximum clamp current	Σ I <sub>CLAMP</sub>	—	20	mA	Applicable to pins*4
“L” level maximum output current	I <sub>OL1</sub>	—	15	mA	Other than P00 to P07
	I <sub>OL2</sub>		15		P00 to P07
“L” level average current	I <sub>OLAV1</sub>	—	4	mA	Other than P00 to P07 Average output current = operating current × operating ratio (1 pin)
	I <sub>OLAV2</sub>		12		P00 to P07 Average output current = operating current × operating ratio (1 pin)
“L” level total maximum output current	ΣI <sub>OL</sub>	—	100	mA	
“L” level total average output current	ΣI <sub>OLAV</sub>	—	50	mA	Total average output current = operating current × operating ratio (total of pins)
“H” level maximum output current	I <sub>OH1</sub>	—	- 15	mA	Other than P00 to P07
	I <sub>OH2</sub>		- 15		P00 to P07
“H” level average current	I <sub>OHAV1</sub>	—	- 4	mA	Other than P00 to P07 Average output current = operating current × operating ratio (1 pin)
	I <sub>OHAV2</sub>		- 8		P00 to P07 Average output current = operating current × operating ratio (1 pin)
“H” level total maximum output current	ΣI <sub>OH</sub>	—	- 100	mA	
“H” level total average output current	ΣI <sub>OHAV</sub>	—	- 50	mA	Total average output current = operating current × operating ratio (total of pins)
Power consumption	P <sub>d</sub>	—	320	mW	
Operating temperature	T <sub>A</sub>	- 40	+ 85	°C	Other than MB95FV100A-101
Storage temperature	T <sub>stg</sub>	- 55	+ 150	°C	

(Continued)

(Continued)

- \*1 : The parameter is based on  $AV_{CC} = V_{SS} = 0.0$  V.
- \*2 : Apply equal potential to  $AV_{CC}$  and  $V_{CC}$ . AVR should not exceed  $AV_{CC} + 0.3$  V.
- \*3 :  $V_{I1}$  and  $V_{O}$  should not exceed  $V_{CC} + 0.3$  V.  $V_{I1}$  must not exceed the rating voltage. However, if the maximum current to/from an input is limited by some means with external components, the  $I_{CLAMP}$  rating supersedes the  $V_{I1}$  rating.
- \*4 :
  - Applicable to pins : P00 to P07, P10 to P15, P20 to P24, P30 to P37, PG0
  - Use within recommended operating conditions.
  - Use at DC voltage (current).
  - The + B signal should always be applied a limiting resistance placed between the + B signal and the microcontroller.
  - The value of the limiting resistance should be set so that when the + B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
  - Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the VCC pin, and this may affect other devices.
  - Note that if the + B signal is inputted when the microcontroller power supply is off (not fixed at 0 V), the power supply is provided from the pins, so that incomplete operation may result.
  - Note that if the + B input is applied during power-on, the power supply is provided from the pins and the resulting power supply voltage may not be sufficient to operate the power-on reset.
  - Care must be taken not to leave the + B input pin open.
  - Sample recommended circuits :

• Input/Output Equivalent Circuits



**WARNING:** Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

# MB95110A Series

## 2. Recommended Operating Conditions

( $AV_{SS} = V_{SS} = 0.0\text{ V}$ )

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
Power supply voltage	$V_{CC}, AV_{CC}$	1.8*1	3.3*2	V	At normal operating, FLASH product, $T_A = -10\text{ °C to }+85\text{ °C}$
		1.8*1	3.6		At normal operating, MASK product, $T_A = -10\text{ °C to }+85\text{ °C}$
		2.0*1	3.3*2		At normal operating, FLASH product, $T_A = -40\text{ °C to }+85\text{ °C}$
		2.0*1	3.6		At normal operating, MASK product, $T_A = -40\text{ °C to }+85\text{ °C}$
		2.6	3.6		MB95FV100A-101
		1.5	3.3*2		Retain status of stop operation, FLASH product
		1.5	3.6		Retain status of stop operation, MASK product
Operating temperature	$T_A$	- 40	+ 85	°C	Other than MB95FV100A-101

\*1 : The values vary with the operating frequency.

\*2 : Consult Fujitsu separately for a guarantee of a maximum value of 3.6 V.

**WARNING:** The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

### 3. DC Characteristics

( $V_{CC} = AV_{CC} = 3.3\text{ V}$ ,  $AV_{SS} = V_{SS} = 0.0\text{ V}$ ,  $T_A = -40\text{ }^\circ\text{C}$  to  $+85\text{ }^\circ\text{C}$  [MB95FV100A-101 is  $T_A = +25\text{ }^\circ\text{C}$ ])

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage	$V_{IH1}$	P10, P67	*1	0.7 $V_{CC}$	—	$V_{CC} + 0.3$	V	At selecting of CMOS input level (hysteresis input)
	$V_{IH2}$	P50, P51	*1	0.7 $V_{CC}$	—	$V_{SS} + 5.5$	V	At selecting of CMOS input level (hysteresis input)
	$V_{IHS1}$	P00 to P07, P10 to P15, P20 to P24, P30 to P37, P60 to P67, PG0, PG1*2, PG2*2	*1	0.8 $V_{CC}$	—	$V_{CC} + 0.3$	V	Hysteresis input
	$V_{IHS2}$	P50, P51	*1	0.8 $V_{CC}$	—	$V_{SS} + 5.5$	V	Hysteresis input
	$V_{IHM}$	$\overline{RST}$ , MOD	—	0.7 $V_{CC}$	—	$V_{CC} + 0.3$	V	CMOS input (FLASH product)
			—	0.8 $V_{CC}$	—	$V_{CC} + 0.3$	V	Hysteresis input (MASK product)
"L" level input voltage	$V_{IL}$	P10, P50, P51, P67	*1	$V_{SS} - 0.3$	—	0.3 $V_{CC}$	V	At selecting of CMOS input level (hysteresis input)
	$V_{ILS}$	P00 to P07, P10 to P15, P20 to P24, P30 to P37, P50, P51, P60 to P67, PG0, PG1*2, PG2*2	*1	$V_{SS} - 0.3$	—	0.2 $V_{CC}$	V	Hysteresis input
	$V_{ILM}$	$\overline{RST}$ , MOD	—	$V_{SS} - 0.3$	—	0.3 $V_{CC}$	V	CMOS input (FLASH product)
			—	$V_{SS} - 0.3$	—	0.2 $V_{CC}$	V	Hysteresis input (MASK product)
Open drain output application voltage	$V_D$	P50, P51	—	$V_{SS} - 0.3$	—	$V_{SS} + 5.5$	V	
"H" level output voltage	$V_{OH1}$	Output pin other than P00 to P07	$I_{OH} = -4.0\text{ mA}$	2.4	—	—	V	MB95FV100A-101 a conditional : $I_{OH} = -2.0\text{ mA}$
	$V_{OH2}$	P00 to P07	$I_{OH} = -8.0\text{ mA}$	2.4	—	—	V	MB95FV100A-101 a conditional : $I_{OH} = -5.0\text{ mA}$

(Continued)

# MB95110A Series

(Continued)

( $V_{CC} = AV_{CC} = 3.3\text{ V}$ ,  $AV_{SS} = V_{SS} = 0.0\text{ V}$ ,  $T_A = -40\text{ }^\circ\text{C}$  to  $+85\text{ }^\circ\text{C}$  [MB95FV100A-101 is  $T_A = +25\text{ }^\circ\text{C}$ ])

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
“L” level output voltage	$V_{OL1}$	Output pin other than P00 to P07	$I_{OL} = 4.0\text{ mA}$	—	—	0.4	V	MB95FV100A-101 a conditional : $I_{OL} = 3.0\text{ mA}$
	$V_{OL2}$	P00 to P07	$I_{OL} = 12\text{ mA}$	—	—	0.4	V	MB95FV100A-101 a conditional : $I_{OL} = 8.0\text{ mA}$
Input leakage current (High-Z output leakage current)	$I_{LI}$	Port other than P50, P51	$0.0\text{ V} < V_I < V_{CC}$	-5	—	+5	$\mu\text{A}$	When no pull-up resistor is specified
Open drain output leakage current	$I_{LIOD}$	P50, P51	$0.0\text{ V} < V_I < V_{SS} + 5.5\text{ V}$	—	—	+5	$\mu\text{A}$	
Pull-up resistor	$R_{PULL}$	P10 to P15, P20 to P24, P30 to P37, PG0, PG1*2, PG2*2	$V_I = 0.0\text{ V}$	25	50	100	k $\Omega$	When pull-up resistor is specified
Pull-down resistor	$R_{MOD}$	MOD	$V_I = V_{CC}$	50	100	200	k $\Omega$	MASK product only
Power supply current*3	$I_{CC}$	$V_{CC}$ (external clock operation)	$F_{CH} = 20\text{ MHz}$ $f_{mp} = 10\text{ MHz}$ Main clock mode (divided by 2)	—	11	14	mA	FLASH product
				—	7.3	10	mA	MASK product
				—	30	35	mA	FLASH product (at FLASH writing and erasing)
	$I_{CCS}$		$F_{CH} = 20\text{ MHz}$ $f_{mp} = 10\text{ MHz}$ Main Sleep mode (divided by 2)	—	4.5	6	mA	
	$I_{CCL}$		$F_{CL} = 32\text{ kHz}$ $f_{mpl} = 16\text{ kHz}$ Subclock mode (divided by 2), $T_A = +25\text{ }^\circ\text{C}$	—	25	35	$\mu\text{A}$	
$I_{CCLS}$	$F_{CL} = 32\text{ kHz}$ $f_{mpl} = 16\text{ kHz}$ Sub sleep mode (divided by 2), $T_A = +25\text{ }^\circ\text{C}$	—	7	15	$\mu\text{A}$			

(Continued)

(Continued)

( $V_{CC} = AV_{CC} = 3.3\text{ V}$ ,  $AV_{SS} = V_{SS} = 0.0\text{ V}$ ,  $T_A = -40\text{ }^\circ\text{C}$  to  $+85\text{ }^\circ\text{C}$  [MB95FV100A-101 is  $T_A = +25\text{ }^\circ\text{C}$ ])

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current*3	I <sub>CC</sub> T	V <sub>CC</sub> (external clock operation)	F <sub>CL</sub> = 32 kHz Watch mode	—	2	10	μA	FLASH product
			Main stop mode T <sub>A</sub> = +25 °C	—	1	5	μA	MASK product
	I <sub>CC</sub> MPLL		F <sub>CH</sub> = 4 MHz f <sub>mp</sub> = 10 MHz	—	10	14	mA	FLASH product
			Main PLL mode (multiplied by 2.5)	—	6.7	10	mA	MASK product
	I <sub>CC</sub> SPLL		F <sub>CL</sub> = 32 kHz f <sub>mpl</sub> = 128 kHz Sub PLL mode (multiplied by 4), T <sub>A</sub> = +25 °C	—	190	250	μA	
	I <sub>CT</sub> S		F <sub>CH</sub> = 10 MHz Timebase timer mode T <sub>A</sub> = +25 °C	—	0.4	0.5	mA	
	I <sub>CC</sub> H		Substop mode T <sub>A</sub> = +25 °C	—	1	5	μA	
	I <sub>A</sub>		AV <sub>CC</sub>	F <sub>CH</sub> = 10 MHz At A/D converting	—	1.3	2.2	mA
I <sub>AH</sub>	F <sub>CH</sub> = 10 MHz At A/D converting stop T <sub>A</sub> = +25 °C	—		1	5	μA		
Input capacitance	C <sub>IN</sub>	Other than AV <sub>CC</sub> , AV <sub>SS</sub> , V <sub>CC</sub> , and V <sub>SS</sub>	—	5	15	pF		

\*1 : P10, P50, P51, and P67 can switch the input level to either the “CMOS input level” or “hysteresis input level”.  
The switching of the input level can be set by the input level selection register (ILSR).

\*2 : Single-clock products only

\*3 : The power-supply current is determined by the external clock.

- Refer to “4. AC characteristics (1) Clock Timing” for F<sub>CH</sub> and F<sub>CL</sub>.
- Refer to “4. AC characteristics (2) Source Clock/Machine Clock” for f<sub>mp</sub> and f<sub>mpl</sub>.

# MB95110A Series

## 4. AC Characteristics

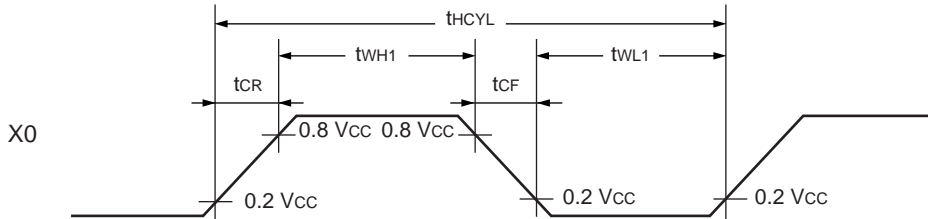
### (1) Clock Timing

(V<sub>CC</sub> = 3.3 V, AV<sub>SS</sub> = V<sub>SS</sub> = 0.0 V, T<sub>A</sub> = -40 °C to +85 °C)

Parameter	Symbol	Pin	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Clock frequency	F <sub>CH</sub>	X0, X1	—	1	—	10	MHz	When using Main oscillation circuit
				1	—	20	MHz	When using external clock
				3	—	10	MHz	Main PLL multiplied by 1
				3	—	5	MHz	Main PLL multiplied by 2
				3	—	4	MHz	Main PLL multiplied by 2.5
	F <sub>CL</sub>	X0A, X1A		—	32.768	—	kHz	When using Sub oscillation circuit
Clock cycle time	t <sub>H CYL</sub>	X0, X1	100	—	1000	ns	When using Main oscillation circuit	
			50	—	1000	ns	When using Sub oscillation circuit	
	t <sub>L CYL</sub>	X0A, X1A	—	30.5	—	μs	Subclock	
Input clock pulse width	t <sub>WH1</sub> t <sub>WL1</sub>	X0	10	—	—	ns	When using external clock Duty ratio is about 30% to 70%.	
	t <sub>WH2</sub> t <sub>WL2</sub>	X0A	—	15.2	—	μs		
Input clock rise time and fall time	t <sub>CR</sub> t <sub>CF</sub>	X0, X0A	—	—	5	ns	When using external clock	

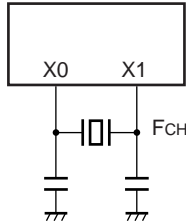


- X0 and X1 Timing and Applying Conditions

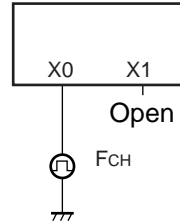


- Main Clock Applying Conditions

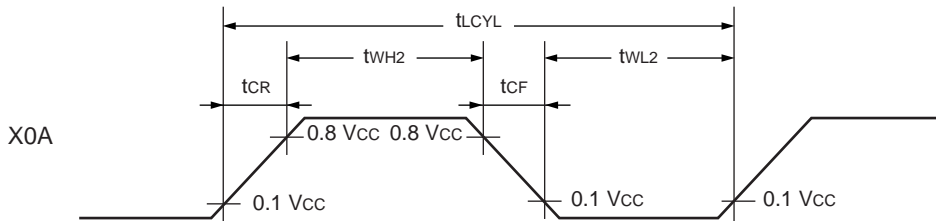
When using a crystal or ceramic oscillator



When using external clock

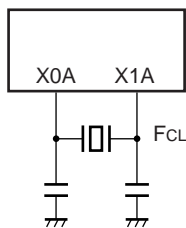


- X0A and X1A Timing and Applying Conditions

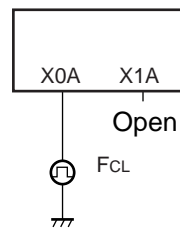


- Subclock Applying Conditions

When using a crystal or ceramic oscillator



When using external clock



# MB95110A Series

## (2) Source Clock/Machine Clock

(V<sub>CC</sub> = 3.3 V, AV<sub>SS</sub> = V<sub>SS</sub> = 0.0 V, T<sub>A</sub> = - 40 °C to + 85 °C)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Source clock* <sup>1</sup> (Clock before setting division)	SCLK	—	100	—	2000	ns	When using Main clock Min : F <sub>CH</sub> = 10 MHz, PLL multiplied by 1 Max : F <sub>CH</sub> = 1 MHz, divided by 2
			7.6	—	61.0	μs	When using Subclock Min : F <sub>CL</sub> = 32 kHz, PLL multiplied by 4 Max : F <sub>CL</sub> = 32 kHz, divided by 2
Source clock frequency	f <sub>sp</sub>	—	0.5	—	10.0	MHz	When using Main clock
	f <sub>spl</sub>	—	16.384	—	131.072	kHz	When using Subclock
Machine clock* <sup>2</sup> (Minimum instruction execution time)	MCLK	—	100	—	32000	ns	When using Main clock Min : SLCK = 10 MHz, no division Max : SLCK = 0.5 MHz, divided by 16
			7.6	—	976.5	μs	When using Subclock Min : SLCK = 131 kHz, no division Max : SLCK = 16 kHz, divided by 16
Machine clock frequency	f <sub>mp</sub>	—	0.031	—	10.000	MHz	When using Main clock
	f <sub>mpl</sub>	—	1.024	—	131.072	kHz	When using Subclock

\*1 : Clock before setting division due to machine clock division ratio selection bit (SYCC : DIV1 and DIV0) . This source clock is divided by the machine clock division ratio selection bit (SYCC : DIV1 and DIV0) , and it becomes the machine clock. Further, the source clock can be selected as follow.

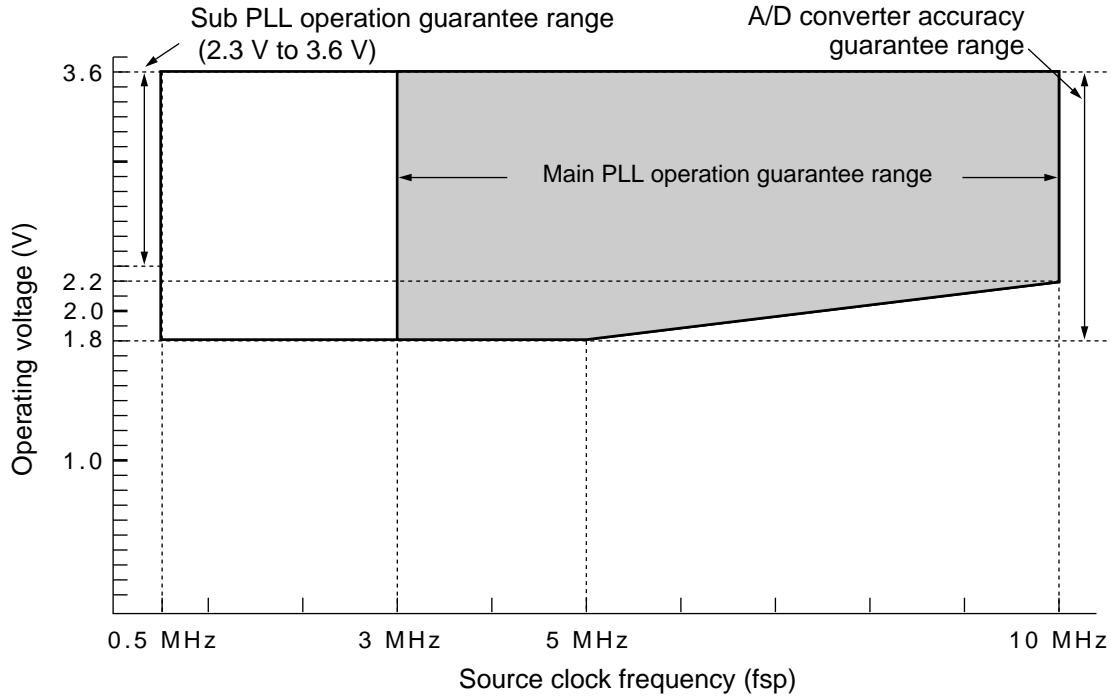
- Main clock divided by 2
- PLL multiplication of main clock (select from 1, 2, 2.5 multiplication)
- Subclock divided by 2
- PLL multiplication of subclock (select from 2, 3, 4 multiplication)

\*2 : Operation clock of the microcontroller. Machine clock can be selected as follow.

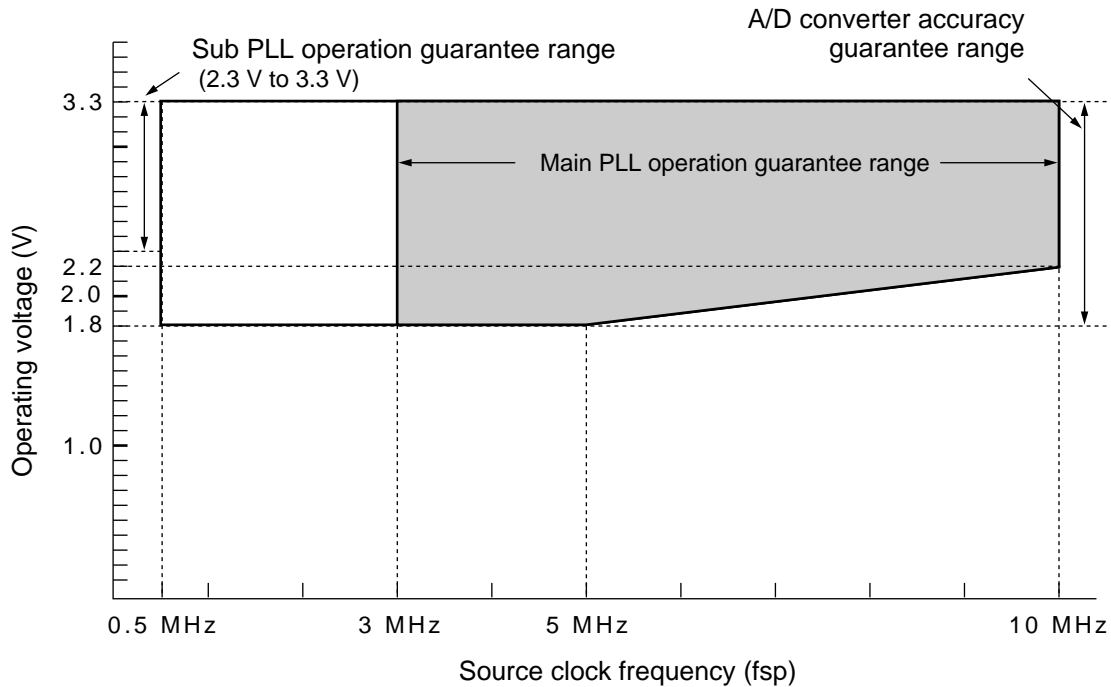
- Source clock (no division)
- Source clock divided by 4
- Source clock divided by 8
- Source clock divided by 16

• **Operating voltage – Operating frequency**

- MASK product



- FLASH product



Note: In operating by 2.0 V or less, only "T<sub>A</sub> = -10 °C to +85 °C" is guaranteed.



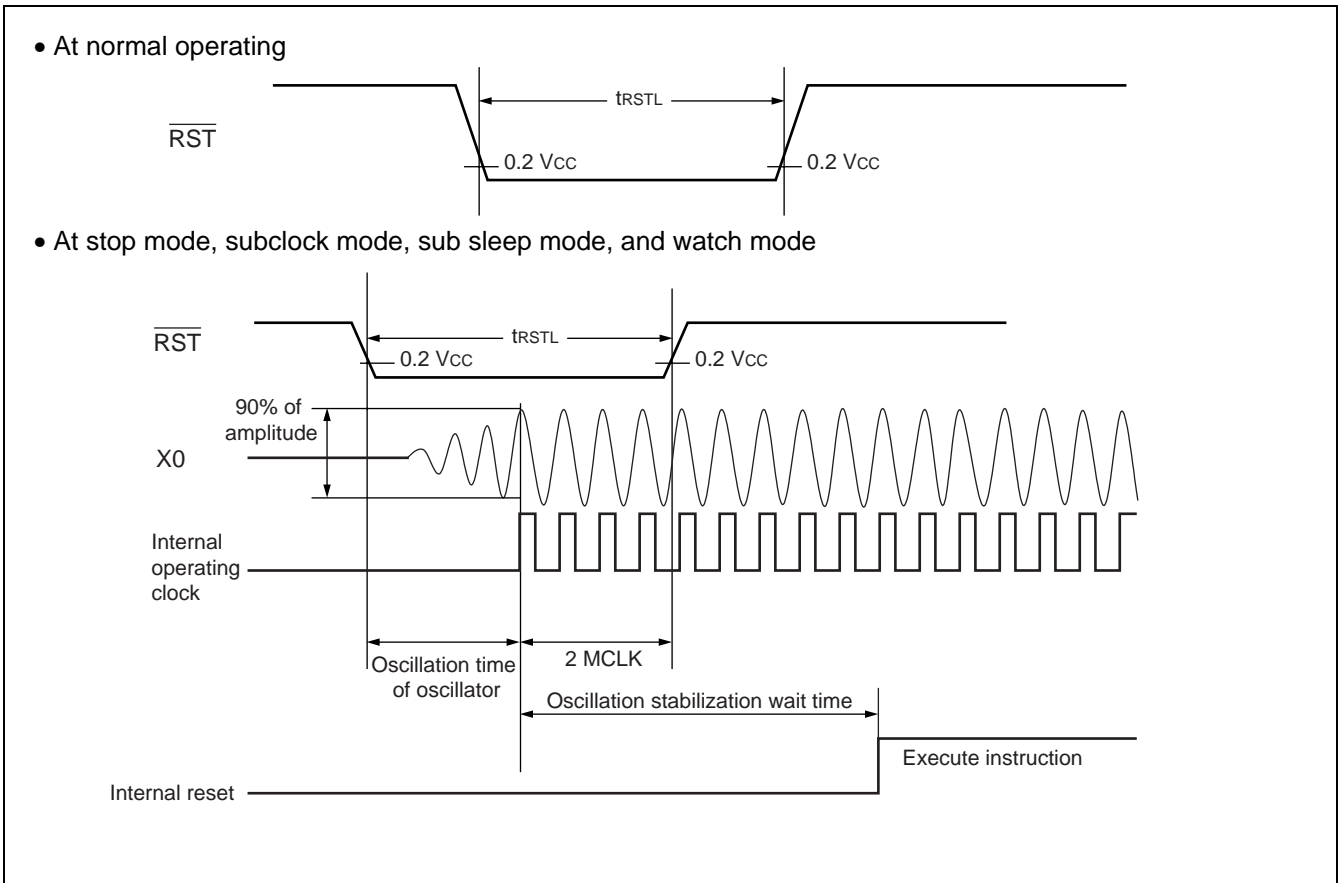
## (3) Reset Timing

( $V_{CC} = 3.3\text{ V}$ ,  $AV_{SS} = V_{SS} = 0.0\text{ V}$ ,  $T_A = -40\text{ }^\circ\text{C}$  to  $+85\text{ }^\circ\text{C}$ )

Parameter	Symbol	Value		Unit	Remarks
		Min	Max		
$\overline{\text{RST}}$ "L" level pulse width	$t_{\text{RSTL}}$	$2\text{ MCLK}^{*1}$	—	ns	At normal operating
		Oscillation time of oscillator <sup>*2</sup> + $2\text{ MCLK}^{*1}$	—	ns	At stop mode, subclock mode, Sub sleep mode, and watch mode

\*1 : Refer to "(2) Source Clock/Machine Clock" for MCLK.

\*2 : Oscillation time of oscillator is the time that the amplitude reaches 90 %. In the crystal oscillator, the oscillation time is between several ms and tens of ms. In FAR/ceramic oscillators, the oscillation time is between hundreds of  $\mu\text{s}$  and several ms. In the external clock, the oscillation time is 0 ms.



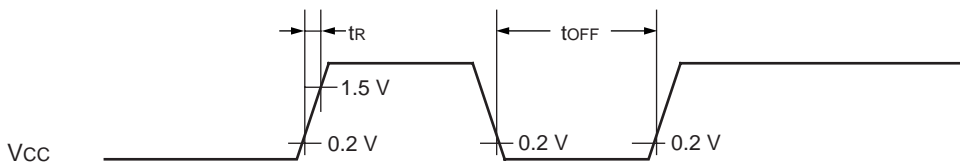
# MB95110A Series

## (4) Power-on Reset

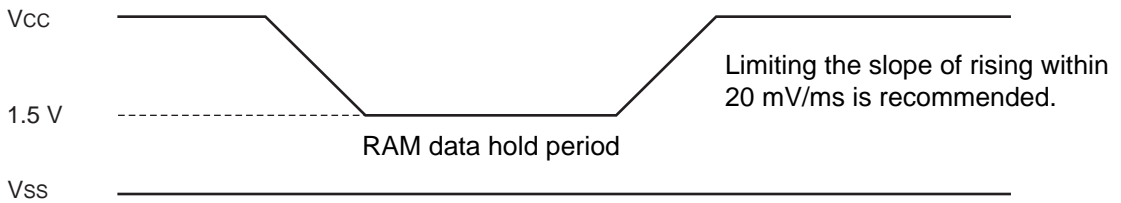
(AV<sub>SS</sub> = V<sub>SS</sub> = 0.0 V, T<sub>A</sub> = - 40 °C to + 85 °C)

Parameter	Symbol	Conditions	Value		Unit	Remarks
			Min	Max		
Power supply rising time	t <sub>R</sub>	—	—	36	ms	
Power supply cutoff time	t <sub>OFF</sub>	—	1	—	ms	Due to repeated operations

Note : The power supply must be turned on within the selected oscillation stabilization time.



Sudden change of power supply voltage may activate the power-on reset function. When changing power supply voltages during operation, set the slope of rising within 20 mV/ms as shown below. In this case, do not use PLL clock. However, if voltage drop is 1V/s or less, use of PLL clock is allowed during operation.

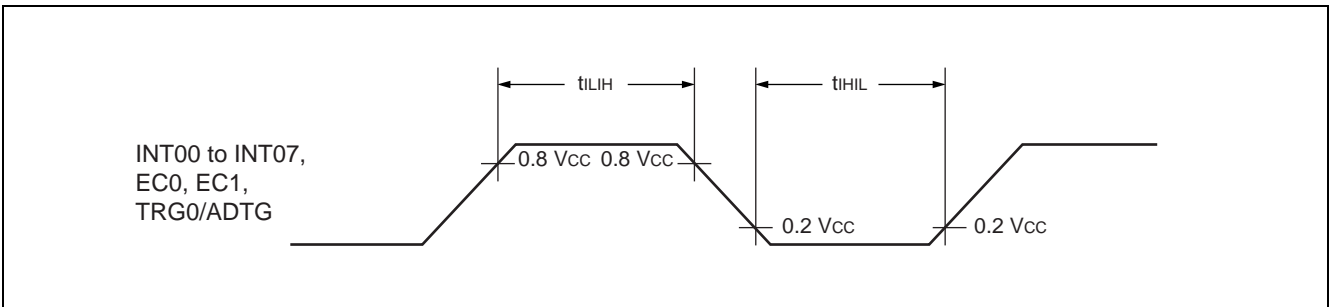


## (5) Peripheral Input Timing

( $V_{CC} = 3.3\text{ V}$ ,  $V_{AVSS} = V_{SS} = 0.0\text{ V}$ ,  $T_A = -40\text{ }^\circ\text{C}$  to  $+85\text{ }^\circ\text{C}$ )

Parameter	Symbol	Pin name	Value		Unit	Remarks
			Min	Max		
Peripheral input "H" pulse width	$t_{LIH}$	INT00 to INT07, EC0, EC1, TRG0/ADTG	2 MCLK*	—	ns	
Peripheral input "L" pulse width	$t_{HIL}$		2 MCLK*	—	ns	

\* : Refer to "(2) Source Clock/Machine Clock" for MCLK.



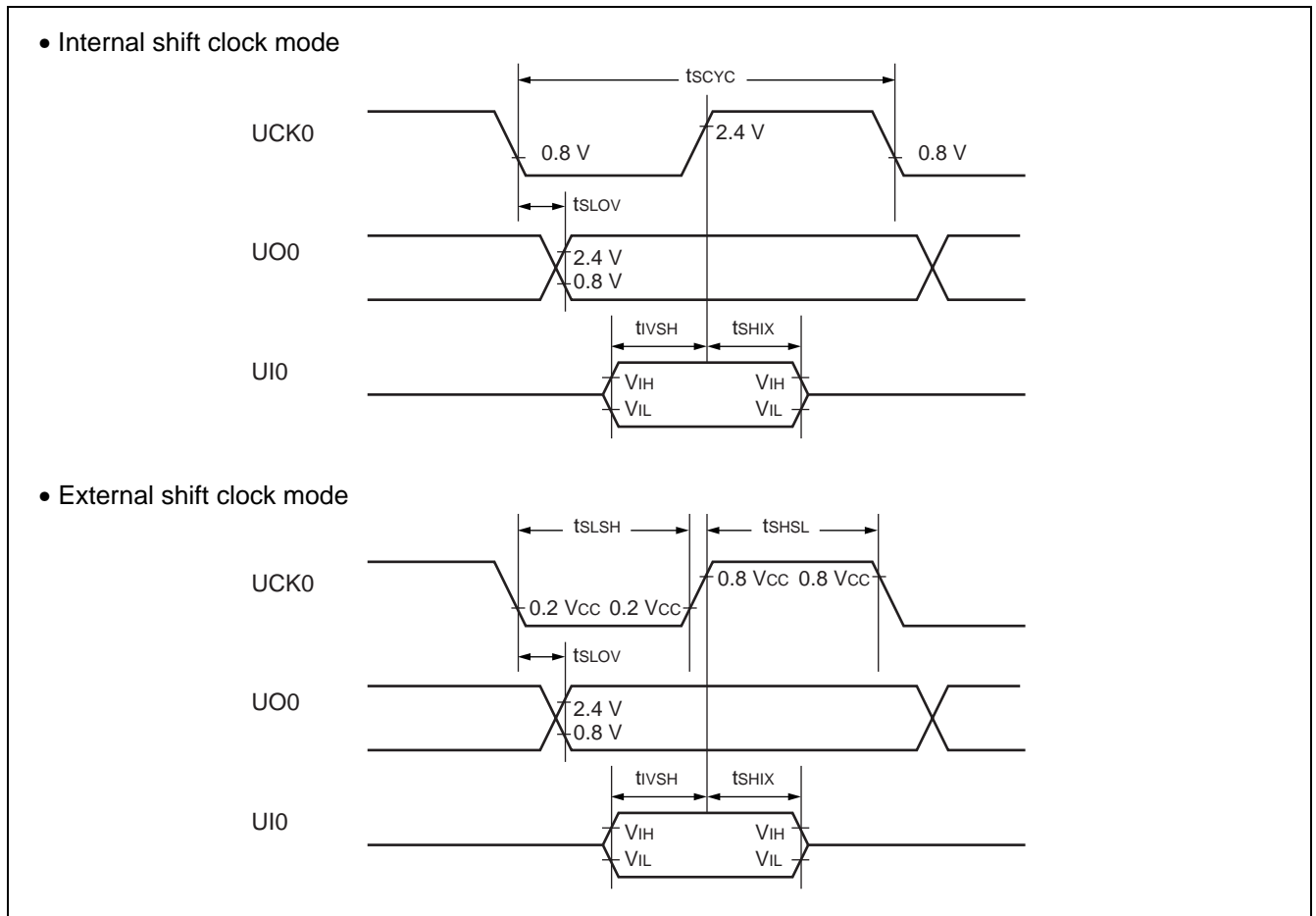
# MB95110A Series

## (6) UART/SIO, Serial I/O Timing

( $V_{CC} = 3.3\text{ V}$ ,  $AV_{SS} = V_{SS} = 0.0\text{ V}$ ,  $T_A = -40\text{ }^\circ\text{C}$  to  $+85\text{ }^\circ\text{C}$ )

Parameter	Symbol	Pin name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	$t_{SCYC}$	UCK0	Internal clock operation	4 MCLK*	—	ns	
UCK ↓ → UO time	$t_{SLOV}$	UCK0, UO0		- 190	190	ns	
Valid UI → UCK ↑	$t_{IVSH}$	UCK0, UI0		2 MCLK*	—	ns	
UCK ↑ → valid UI hold time	$t_{SHIX}$	UCK0, UI0		2 MCLK*	—	ns	
Serial clock "H" pulse width	$t_{SHSL}$	UCK0	External clock operation	4 MCLK*	—	ns	
Serial clock "L" pulse width	$t_{SLSH}$	UCK0		4 MCLK*	—	ns	
UCK ↓ → UO time	$t_{SLOV}$	UCK0, UO0		—	190	ns	
Valid UI → UCK ↑	$t_{IVSH}$	UCK0, UI0		2 MCLK*	—	ns	
UCK ↑ → valid UI hold time	$t_{SHIX}$	UCK0, UI0	2 MCLK*	—	ns		

\* : Refer to "(2) Source Clock/Machine Clock" for MCLK.





## (7) LIN-UART Timing

ESCR : SCES = 0, ECCR : SCDE = 0

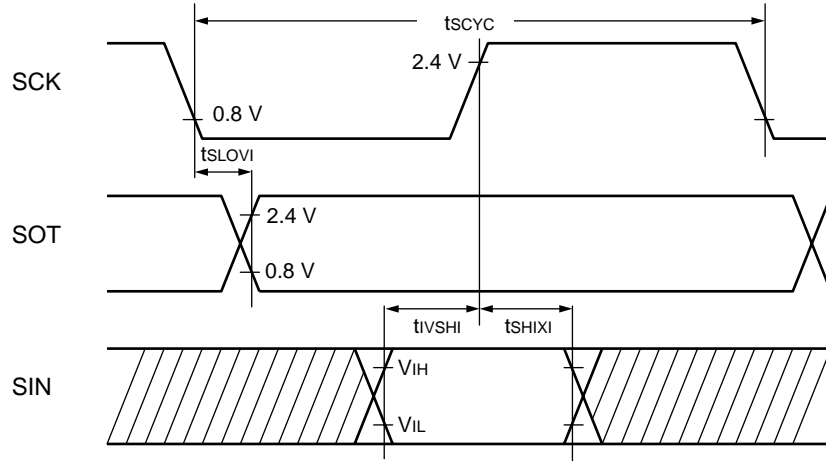
(V<sub>CC</sub> = 3.3 V, AV<sub>SS</sub> = V<sub>SS</sub> = 0.0 V, T<sub>A</sub> = -40 °C to +85 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Serial clock cycle time	t <sub>SCYC</sub>	SCK	Internal clock operation output pin : C <sub>L</sub> = 80 pF + 1 TTL.	5 MCLK*	—	ns
SCK ↑ → SOT delay time	t <sub>SLOVI</sub>	SCK, SOT		-95	95	ns
Valid SIN → SCK ↑	t <sub>IVSHI</sub>	SCK, SIN		MCLK* + 190	—	ns
SCK ↑ → valid SIN hold time	t <sub>SHIXI</sub>	SCK, SIN		0	—	ns
Serial clock "L" pulse width	t <sub>LSH</sub>	SCK	External clock operation output pin : C <sub>L</sub> = 80 pF + 1 TTL.	3 MCLK* - t <sub>r</sub>	—	ns
Serial clock "H" pulse width	t <sub>SHSL</sub>	SCK		MCLK* + 95	—	ns
SCK ↓ → SOT delay time	t <sub>SLOVE</sub>	SCK, SOT		—	2 MCLK* + 95	ns
Valid SIN → SCK ↑	t <sub>IVSHE</sub>	SCK, SIN		190	—	ns
SCK ↑ → Valid SIN hold time	t <sub>SHIXE</sub>	SCK, SIN		MCLK* + 95	—	ns
SCK fall time	t <sub>f</sub>	SCK		—	10	ns
SCK rise time	t <sub>r</sub>	SCK		—	10	ns

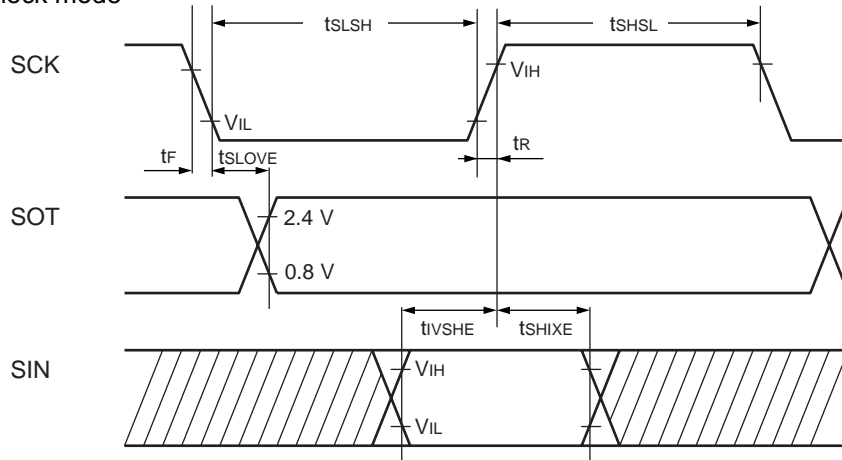
\* : Refer to "(2) Source Clock/Machine Clock" for MCLK.

# MB95110A Series

- Internal shift clock mode



- External shift clock mode



# MB95110A Series

ESCR : SCES = 1, ECCR : SCDE = 0

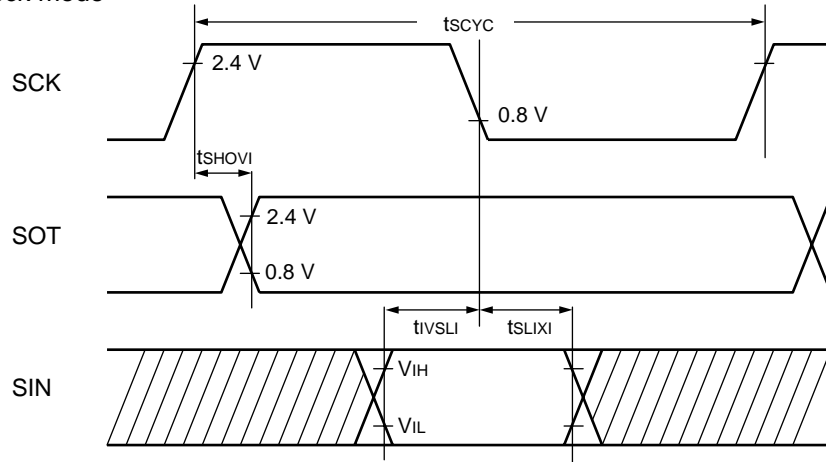
(V<sub>CC</sub> = 3.3 V, AV<sub>SS</sub> = V<sub>SS</sub> = 0.0 V, T<sub>A</sub> = -40 °C to + 85 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Serial clock cycle time	t <sub>SCYC</sub>	SCK	Internal clock operation output pin : C <sub>L</sub> = 80 pF + 1 TTL.	5 MCLK*	—	ns
SCK ↑ → SOT delay time	t <sub>SHOVI</sub>	SCK, SOT		-95	95	ns
Valid SIN → SCK ↓	t <sub>IVSLI</sub>	SCK, SIN		MCLK* + 190	—	ns
SCK ↓ → Valid SIN hold time	t <sub>SLIXI</sub>	SCK, SIN		0	—	ns
Serial clock “H” pulse width	t <sub>SHSL</sub>	SCK	External clock operation output pin : C <sub>L</sub> = 80 pF + 1 TTL.	3 MCLK* - t <sub>R</sub>	—	ns
Serial clock “L” pulse width	t <sub>LSLH</sub>	SCK		MCLK* + 95	—	ns
SCK ↑ → SOT delay time	t <sub>SHOVE</sub>	SCK, SOT		—	2 MCLK* + 95	ns
Valid SIN → SCK ↓	t <sub>IVSLE</sub>	SCK, SIN		190	—	ns
SCK ↓ → Valid SIN hold time	t <sub>SLIXE</sub>	SCK, SIN		MCLK* + 95	—	ns
SCK fall time	t <sub>F</sub>	SCK		—	10	ns
SCK rise time	t <sub>R</sub>	SCK		—	10	ns

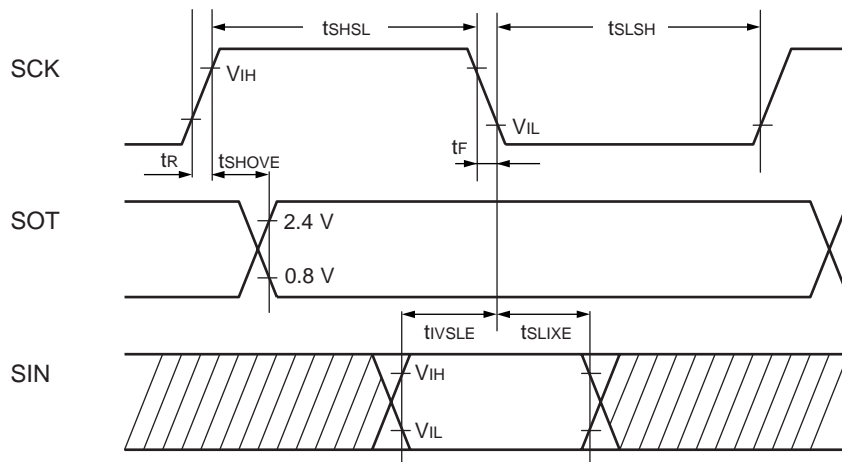
\* : Refer to “ (2) Source Clock/Machine Clock” for MCLK.

# MB95110A Series

- Internal shift clock mode



- External shift clock mode



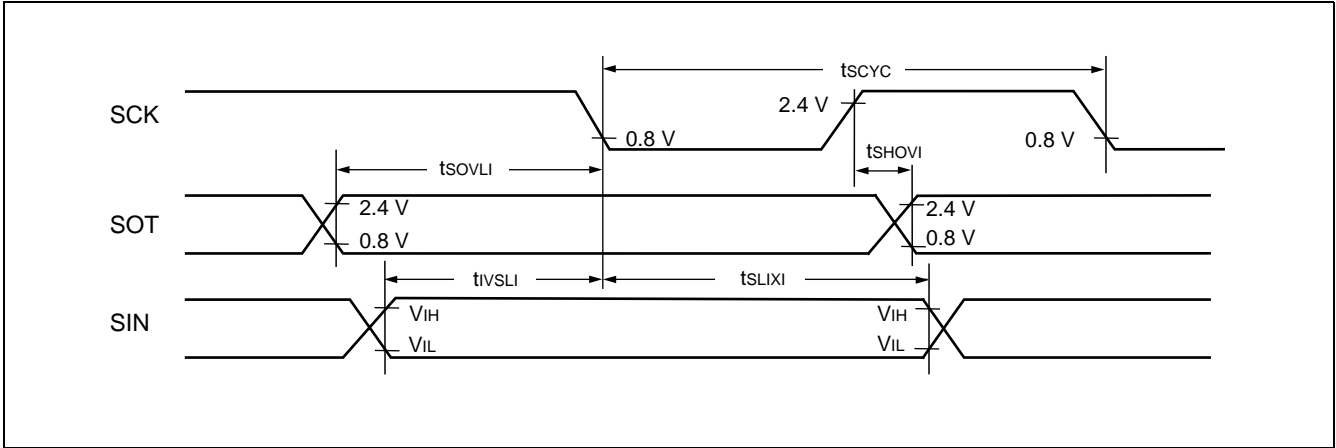
# MB95110A Series

ESCR : SCES = 0, ECCR : SCDE = 1

(V<sub>CC</sub> = 3.3 V, AV<sub>SS</sub> = V<sub>SS</sub> = 0.0 V, T<sub>A</sub> = -40 °C to +85 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Serial clock cycle time	t <sub>SCYC</sub>	SCK	Internal clock operation output pin : C <sub>L</sub> = 80 pF + 1 TTL.	5 MCLK*	—	ns
SCK ↑ → SOT delay time	t <sub>SHOVI</sub>	SCK, SOT		-95	95	ns
Valid SIN → SCK ↓	t <sub>IVSLI</sub>	SCK, SIN		MCLK* + 190	—	ns
SCK ↓ → valid SIN hold time	t <sub>SLIXI</sub>	SCK, SIN		0	—	ns
SOT → SCK ↓ delay time	t <sub>SOVLI</sub>	SCK, SOT		—	4 MCLK*	ns

\* : Refer to “(2) Source Clock/Machine Clock” for MCLK.



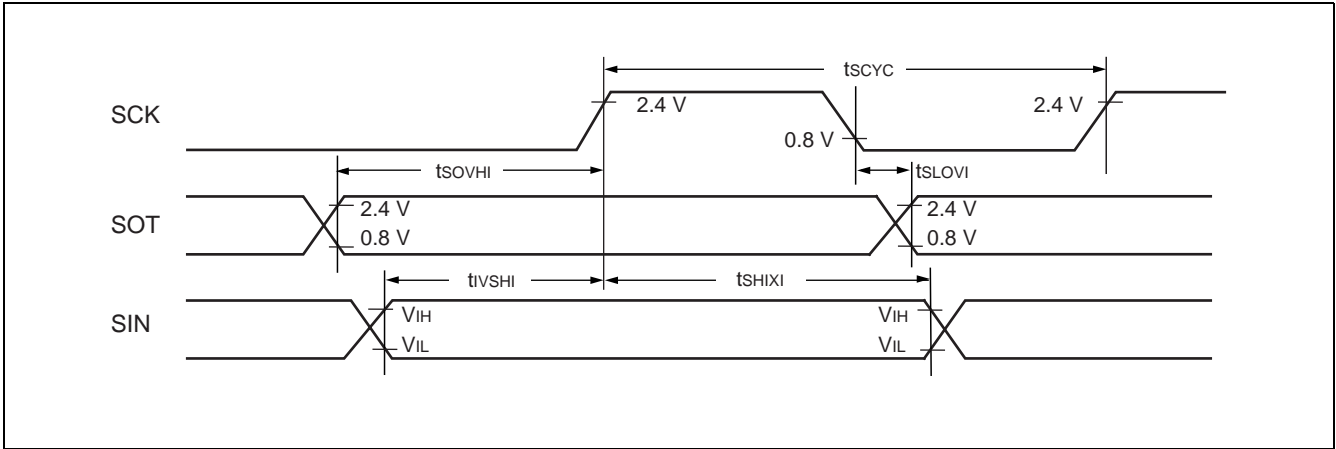
# MB95110A Series

ESCR : SCES = 1, ECCR : SCDE = 1

(V<sub>CC</sub> = 3.3 V, AV<sub>SS</sub> = V<sub>SS</sub> = 0.0 V, T<sub>A</sub> = -40 °C to +85 °C)

Parameter	Symbol	Pin name	Conditions	Value		Unit
				Min	Max	
Serial clock cycle time	t <sub>SCYC</sub>	SCK	Internal clock operation output pin : C <sub>L</sub> = 80 pF + 1 TTL.	5 MCLK*	—	ns
SCK ↓ → SOT delay time	t <sub>SLOVI</sub>	SCK, SOT		-95	95	ns
Valid SIN → SCK ↑	t <sub>IVSHI</sub>	SCK, SIN		MCLK* + 190	—	ns
SCK ↑ → valid SIN hold time	t <sub>SHIXI</sub>	SCK, SIN		0	—	ns
SOT → SCK ↑ delay time	t <sub>SOVHI</sub>	SCK, SOT		—	4 MCLK*	ns

\* : Refer to “(2) Source Clock/Machine Clock” for MCLK.



## (8) I<sup>2</sup>C Timing

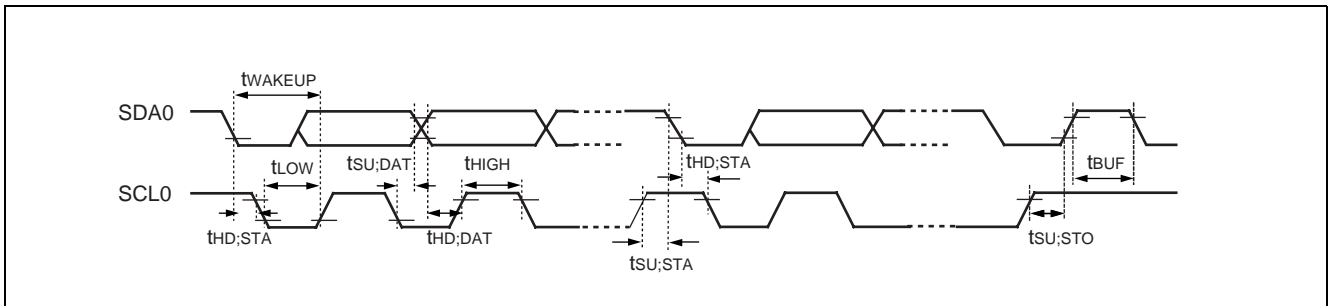
(V<sub>CC</sub> = 3.3 V, AV<sub>SS</sub> = V<sub>SS</sub> = 0.0 V, T<sub>A</sub> = -40 °C to +85 °C)

Parameter	Symbol	Conditions	Value				Unit	Remarks
			Standard-mode		Fast-mode			
			Min	Max	Min	Max		
SCL clock frequency	f <sub>SCL</sub>	R = 1.7 kΩ, C = 50 pF*1	0	100	0	400	kHz	
(Repeat) Start condition hold time SDA ↓ → SCL ↓	t <sub>HD;STA</sub>		4.0	—	0.6	—	μs	
SCL clock "L" width	t <sub>LOW</sub>		4.7	—	1.3	—	μs	
SCL clock "H" width	t <sub>HIGH</sub>		4.0	—	0.6	—	μs	
(Repeat) Start condition setup time SCL ↑ → SDA ↓	t <sub>SU;STA</sub>		4.7	—	0.6	—	μs	
Data hold time SCL ↓ → SDA ↓ ↑	t <sub>HD;DAT</sub>		0	3.45*2	0	0.9*3	μs	
Data setup time SDA ↓ ↑ → SCL ↑	t <sub>SU;DAT</sub>		0.25	—	0.1	—	μs	
Stop condition setup time SCL ↑ → SDA ↑	t <sub>SU;STO</sub>		4	—	0.6	—	μs	
Bus free time between stop condition and start condition	t <sub>BUF</sub>		4.7	—	1.3	—	μs	

\*1 : R, C : Pull-up resistor and load capacitor of the SCL and SDA lines.

\*2 : The maximum t<sub>HD;DAT</sub> have only to be met if the device dose not stretch the "L" width (t<sub>LOW</sub>) of the SCL signal.

\*3 : A Fast-mode I<sup>2</sup>C-bus device can be used in a Standard-mode I<sup>2</sup>C-bus system, but the requirement t<sub>SU;DAT</sub> ≥ 250 ns must then be met.



# MB95110A Series

(V<sub>CC</sub> = 3.3 V, AV<sub>SS</sub> = V<sub>SS</sub> = 0.0 V, T<sub>A</sub> = -40 °C to + 85 °C)

Parameter	Symbol	I/O Timing		Unit	Remarks
		Min	Max		
SCL clock "L" width	t <sub>LOW</sub>	$(2 + nm^{*2} / 2)$ MCLK <sup>*1</sup> - 20	—	ns	Master mode
SCL clock "H" width	t <sub>HIGH</sub>	$(nm^{*2} / 2)$ MCLK <sup>*1</sup> - 20	$(nm^{*2} / 2)$ MCLK <sup>*1</sup> + 20	ns	Master mode
Start condition hold time	t <sub>HD;STA</sub>	$(-1 + nm^{*2} / 2)$ MCLK <sup>*1</sup> - 20	$(-1 + nm^{*2})$ MCLK <sup>*1</sup> + 20	ns	Master mode Maximum value is applied when m, n = 1, 8. Otherwise, the minimum value is applied.
Stop condition setup time	t <sub>SU;STO</sub>	$(1 + nm^{*2} / 2)$ MCLK <sup>*1</sup> - 20	$(1 + nm^{*2} / 2)$ MCLK <sup>*1</sup> + 20	ns	Master mode
Start condition setup time	t <sub>SU;STA</sub>	$(1 + nm^{*2} / 2)$ MCLK <sup>*1</sup> - 20	$(1 + nm^{*2} / 2)$ MCLK <sup>*1</sup> + 20	ns	Master mode
Bus free time between stop condition and start condition	t <sub>BUF</sub>	$(2 nm^{*2} + 4)$ MCLK <sup>*1</sup> - 20	—	ns	
Data hold time	t <sub>HD;DAT</sub>	3 MCLK <sup>*1</sup> - 20	—	ns	Master mode
Data setup time	t <sub>SU;DAT</sub>	$(-2 + nm^{*2} / 2)$ MCLK <sup>*1</sup> - 20	$(-1 + nm^{*2} / 2)$ MCLK <sup>*1</sup> + 20	ns	Master mode When assuming that "L" of SCL is not extended, the minimum value is applied to first bit of continuous data. Otherwise, the maximum value is applied.
Setup time between clearing interrupt and SCL rising	t <sub>SU;INT</sub>	$(nm^{*2} / 2)$ MCLK <sup>*1</sup> - 20	$(1 + nm^{*2} / 2)$ MCLK <sup>*1</sup> + 20	ns	Minimum value is applied to interrupt at 9th SCL↓. Maximum value is applied to interrupt at 8th SCL↓.
SCL clock "L" width	t <sub>LOW</sub>	4 MCLK <sup>*1</sup> - 20	—	ns	At reception
SCL clock "H" width	t <sub>HIGH</sub>	4 MCLK <sup>*1</sup> - 20	—	ns	At reception
Start condition detection	t <sub>HD;STA</sub>	2 MCLK <sup>*1</sup> - 20	—	ns	Undetected when 1 MCLK is used at reception
Stop condition detection	t <sub>SU;STO</sub>	2 MCLK <sup>*1</sup> - 20	—	ns	Undetected when 1 MCLK is used at reception
Restart condition detection condition	t <sub>SU;STA</sub>	2 MCLK <sup>*1</sup> - 20	—	ns	Undetected when 1 MCLK is used at reception
Bus free time	t <sub>BUF</sub>	2 MCLK <sup>*1</sup> - 20	—	ns	At reception
Data hold time	t <sub>HD;DAT</sub>	2 MCLK <sup>*1</sup> - 20	—	ns	At slave transmission mode
Data setup time	t <sub>SU;DAT</sub>	t <sub>LOW</sub> - 3 MCLK <sup>*1</sup> - 20	—	ns	At slave transmission mode
Data hold time	t <sub>HD;DAT</sub>	0	—	ns	At reception
Data setup time	t <sub>SU;DAT</sub>	MCLK <sup>*1</sup> - 20	—	ns	At reception

(Continued)



(Continued)

Parameter	Symbol	I/O Timing		Unit	Remarks
		Min	Max		
SDA↓→SCL↑ (at wakeup function )	t <sub>WAKE-UP</sub>	Oscillation stabilization wait time + 2 MCLK*1 – 20	—	ns	

\*1 : Refer to “ (2) Source Clock/Machine Clock” for MCLK.

- \*2 :
- m is CS4 bit and CS3 bit (bit 4 and bit 3) of clock control register (ICCR) .
  - n is CS2 bit to CS0 bit (bit 2 to bit 0) of clock control register (ICCR) .
  - Actual timing of I<sup>2</sup>C is determined by m and n values set by the machine clock (MCLK) and ICCR [4 : 0].
  - Standard-mode :  
m and n can be set at the range : 0.9 MHz < MCLK (machine clock) < 10 MHz.  
Setting of m and n determines the machine clock that can be used below.
 

(m, n) = (1, 8)	: 0.9 MHz < MCLK ≤ 1 MHz
(m, n) = (1, 22), (5, 4), (6, 4), (7, 4), (8, 4)	: 0.9 MHz < MCLK ≤ 2 MHz
(m, n) = (1, 38), (5, 8), (6, 8), (7, 8), (8, 8)	: 0.9 MHz < MCLK ≤ 4 MHz
(m, n) = (1, 98)	: 0.9 MHz < MCLK ≤ 10 MHz
  - Fast-mode :  
m and n can be set at the range : 3.3 MHz < MCLK (machine clock) < 10 MHz.  
Setting of m and n determines the machine clock that can be used below.
 

(m, n) = (1, 8)	: 3.3 MHz < MCLK ≤ 4 MHz
(m, n) = (1, 22), (5, 4)	: 3.3 MHz < MCLK ≤ 8 MHz
(m, n) = (6, 4)	: 3.3 MHz < MCLK ≤ 10 MHz

# MB95110A Series

## 5. A/D Converter

### (1) A/D Converter Electrical Characteristics

(AVcc = Vcc = 1.8 V to 3.3 V [FLASH product], AVcc = Vcc = 1.8 V to 3.6 V [MASK product], AVss = Vss = 0.0 V, TA = -40 °C to +85 °C)

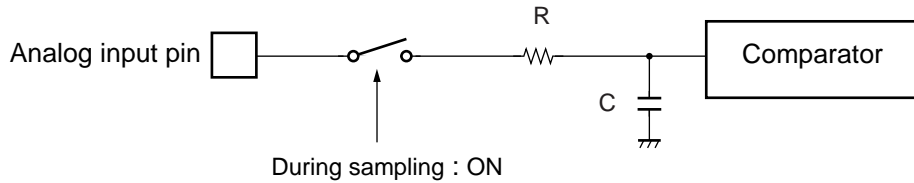
Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Resolution	—	—	—	10	bit	
Total error		-3.0	—	+3.0	LSB	
Linearity error		-2.5	—	+2.5	LSB	
Differential linear error		-1.9	—	+1.9	LSB	
Zero transition voltage	V <sub>OT</sub>	AVss - 1.5 LSB	AVss + 0.5 LSB	AVss + 2.5 LSB	V	FLASH product : 2.7 V ≤ AVcc ≤ 3.3 V MASK product : 2.7 V ≤ AVcc ≤ 3.6 V
		AVss - 0.5 LSB	AVss + 1.5 LSB	AVss + 3.5 LSB	V	1.8 V ≤ AVcc < 2.7 V
Full-scale transition voltage	V <sub>FST</sub>	AVcc - 3.5 LSB	AVcc - 1.5 LSB	AVcc + 0.5 LSB	V	FLASH product : 2.7 V ≤ AVcc ≤ 3.3 V MASK product : 2.7 V ≤ AVcc ≤ 3.6 V
		AVcc - 2.5 LSB	AVcc - 0.5 LSB	AVcc + 1.5 LSB	V	1.8 V ≤ AVcc < 2.7 V
Compare time	—	0.6	—	16,500	μs	FLASH product : 2.7 V ≤ AVcc ≤ 3.3 V MASK product : 2.7 V ≤ AVcc ≤ 3.6 V
		20	—	16,500	μs	1.8 V ≤ AVcc < 2.7 V
Sampling time	—	0.4	—	∞	μs	FLASH product : 2.7 V ≤ AVcc ≤ 3.3 V MASK product : 2.7 V ≤ AVcc ≤ 3.6 V external impedance < at 1.8 kΩ
		30	—	∞	μs	1.8 V ≤ AVcc < 2.7 V external impedance < at 14.8 kΩ
Analog input current	I <sub>AIN</sub>	-0.3	—	0.3	μA	
Analog input voltage range	V <sub>AIN</sub>	AVss	—	AVcc	V	
Reference voltage	—	AVss + 1.8	—	AVcc	V	AVcc pin
Reference voltage supply current	I <sub>R</sub>	—	400	600	μA	AVcc pin, During A/D operation
	I <sub>RH</sub>	—	—	5	μA	AVcc pin, at stop mode

## (2) Notes on Using A/D Converter

### • About the external impedance of analog input and its sampling time

- A/D converter with sample and hold circuit. If the external impedance is too high to keep sufficient sampling time, the analog voltage charged to the internal sample and hold capacitor is insufficient, adversely affecting A/D conversion precision.

#### • Analog input circuit model

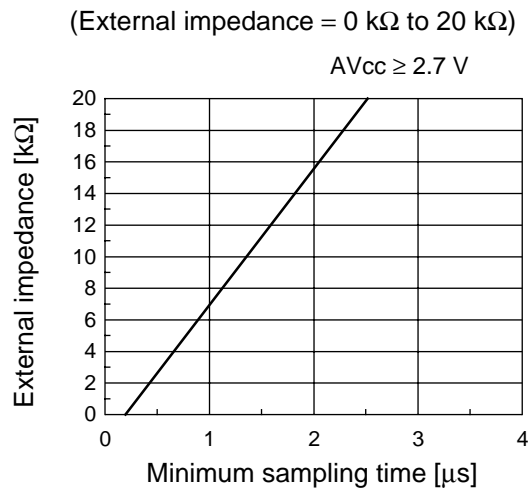
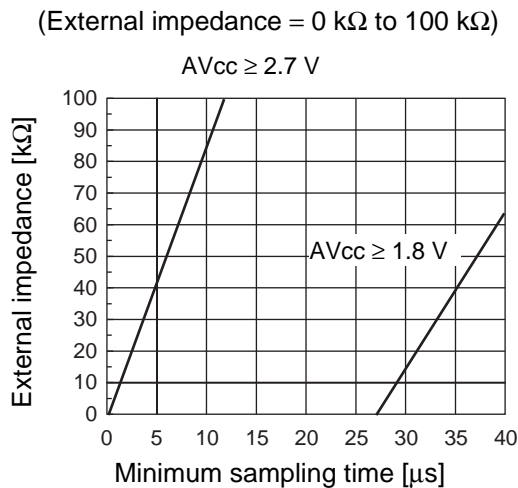


	R	C
$2.7\text{ V} \leq AV_{CC} \leq 3.6\text{ V}$	1.7 k $\Omega$ (Max)	14.5 pF (Max)
$1.8\text{ V} \leq AV_{CC} < 2.7\text{ V}$	84 k $\Omega$ (Max)	25.2 pF (Max)

Note : The values are reference values.

- To satisfy the A/D conversion precision standard, consider the relationship between the external impedance and minimum sampling time and either adjust the resistor value and operating frequency or decrease the external impedance so that the sampling time is longer than the minimum value.

#### • The relationship between external impedance and minimum sampling time



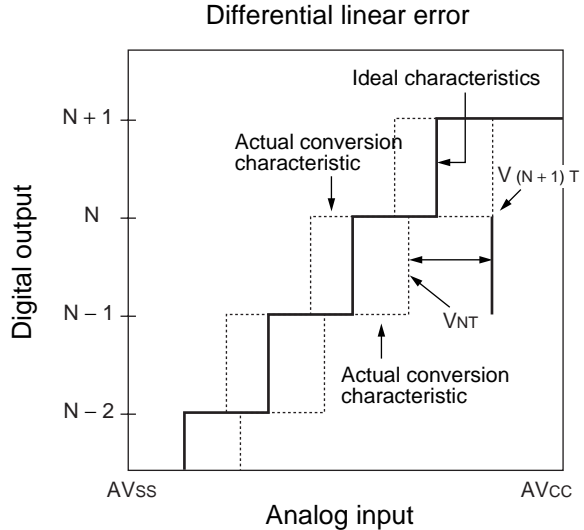
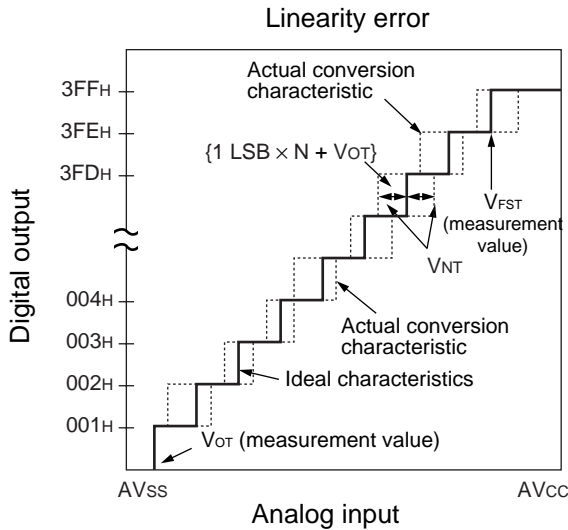
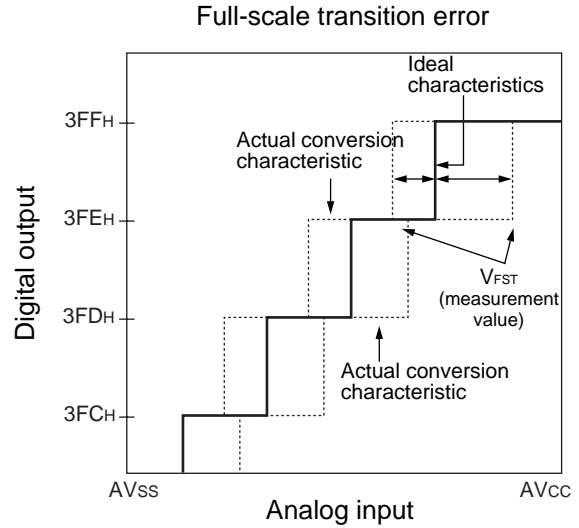
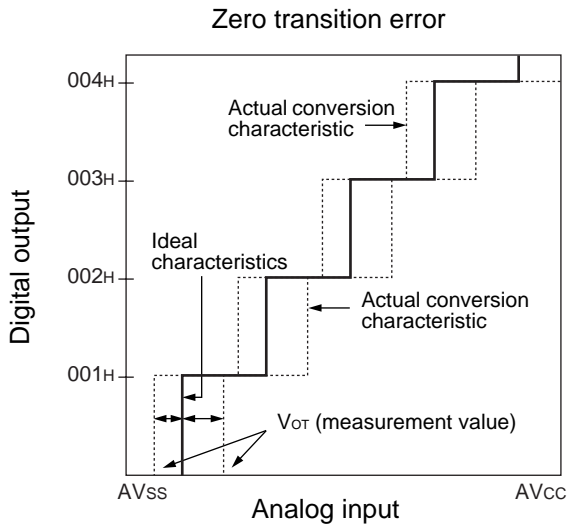
- If the sampling time cannot be sufficient, connect a capacitor of about 0.1  $\mu\text{F}$  to the analog input pin.

### • About errors

As  $|AV_{CC} - AV_{SS}|$  becomes smaller, values of relative errors grow larger.



(Continued)



$$\text{Linear error in digital output } N = \frac{V_{NT} - \{1 \text{ LSB} \times N + V_{OT}\}}{1 \text{ LSB}}$$

$$\text{Differential linear error in digital output } N = \frac{V_{(N+1)T} - V_{NT}}{1 \text{ LSB}} - 1$$

$V_{NT}$  : A voltage at which digital output transits from (N - 1) to N.

$V_{OT}$  (Ideal value) =  $AV_{SS} + 0.5 \text{ LSB}$  [V]

$V_{FST}$  (Ideal value) =  $AV_{CC} - 1.5 \text{ LSB}$  [V]

# MB95110A Series

## 6. Flash Memory Program/Erase Characteristics

Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Sector erase time (4 Kbytes sector)	—	0.2* <sup>1</sup>	3* <sup>2</sup>	s	Excludes 00 <sub>H</sub> programming prior erasure
Sector erase time (16 Kbytes sector)	—	0.5* <sup>1</sup>	12* <sup>2</sup>	s	Excludes 00 <sub>H</sub> programming prior erasure
Byte programming time	—	32	3600	μs	Excludes system-level overhead
Erase/program cycle	10,000	—	—	cycle	
Power supply voltage at erase/program	2.7	—	3.3	V	
Flash data retention time	20* <sup>3</sup>	—	—	year	Average T <sub>A</sub> = +85 °C

\*1 : T<sub>A</sub> = +25 °C, V<sub>CC</sub> = 3.0 V, 10,000 cycles

\*2 : T<sub>A</sub> = +85 °C, V<sub>CC</sub> = 2.7 V, 10,000 cycles

\*3 : This value comes from the technology qualification (using Arrhenius equation to translate high temperature measurements into normalized value at +85 °C) .

## ■ MASK OPTIONS

No	Part number	MB95116A	MB95F118AS	MB95F118AW	MB95FV100A-101
	Specifying procedure	Specify when ordering MASK	Setting disabled	Setting disabled	Setting disabled
1	Clock mode select • Single-system clock mode • Dual-system clock mode	Selectable	Single-system clock mode	Dual-system clock mode	Changing by the switch on MCU board
2	Selection of oscillation stabilization wait time • Selectable the initial value of main clock oscillation stabilization wait time	Selectable 1 : $(2^2 - 2) / F_{CH}$ 2 : $(2^{12} - 2) / F_{CH}$ 3 : $(2^{13} - 2) / F_{CH}$ 4 : $(2^{14} - 2) / F_{CH}$	Fixed to oscillation stabilization wait time of $(2^{14}-2) / F_{CH}$	Fixed to oscillation stabilization wait time of $(2^{14}-2) / F_{CH}$	Fixed to oscillation stabilization wait time of $(2^{14}-2) / F_{CH}$

## ■ ORDERING INFORMATION

Part number	Package	Remarks
MB95116APV MB95F118ASPV MB95F118AWPV	48-pin plastic BCC (LCC-48P-M09)	
MB95116APMT MB95F118ASPMT MB95F118AWPMT	48-pin plastic LQFP (FPT-48P-M26)	
MB2146-301 (MB95FV100A-101PBT)	MCU board ( 244-pin plastic PFBGA ) (BGA-244P-M08)	



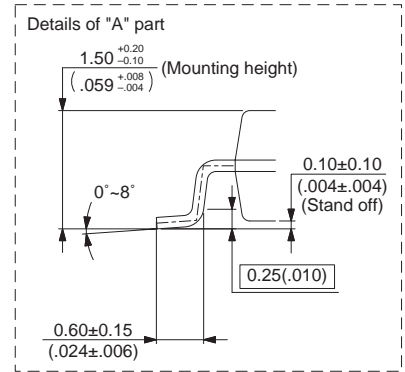
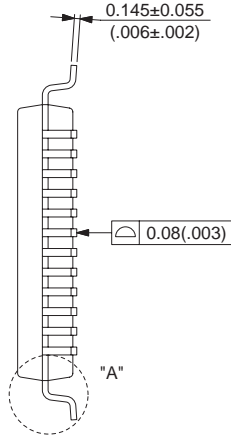
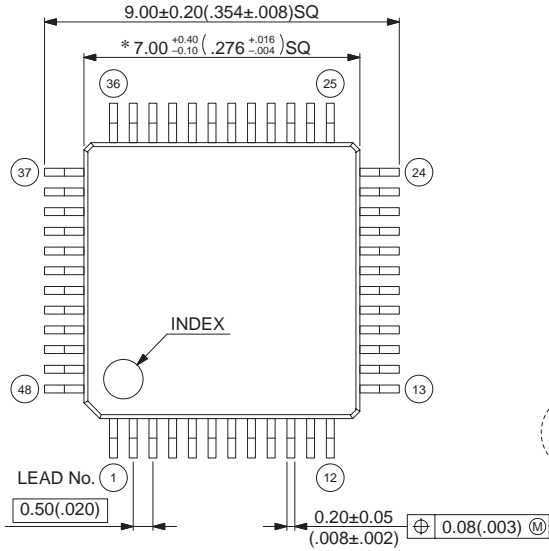


# MB95110A Series

(Continued)

48-pin plastic LQFP  
(FPT-48P-M26)

Note 1) \* : These dimensions do not include resin protrusion.  
 Note 2) Pins width and pins thickness include plating thickness.  
 Note 3) Pins width do not include tie bar cutting remainder.



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Dimensions in mm (inches).  
 Note: The values in parentheses are reference values.

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