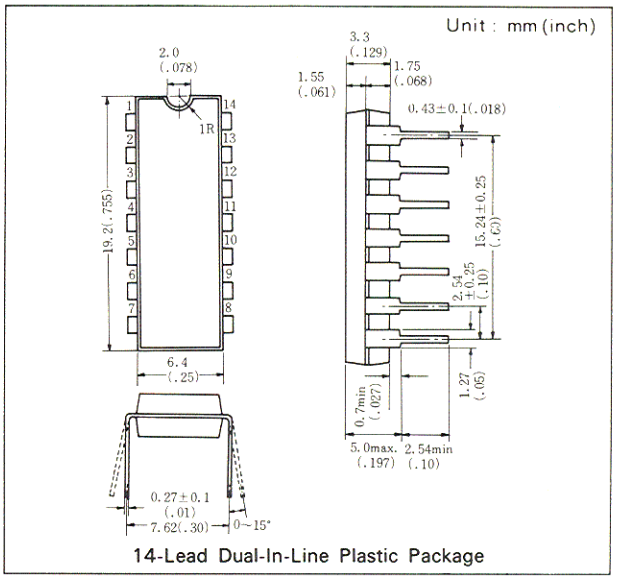
MN3010

DUAL 512-STAGE LOW NOISE BBD

General Description

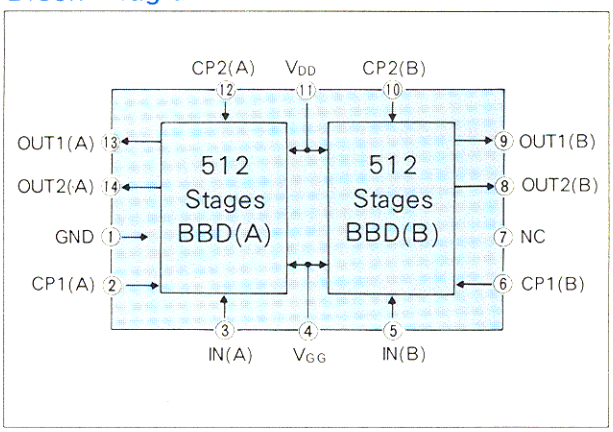
The MN3010 is a dual 512-stage low noise BBD having a wide dynamic range and low distortion characteristics. The device contains two identical BBD's on a single chip with independent input, output and clock terminals as well as common power supply terminals. Each 512-stage BBD provides a signal delay of up to 25.6msec. The two identical BBD's on a same chip offer uniform characteristics and space saving advantage when they are used in parallel or series connection.



Features:

- Wide range of variable delay time:
  2.56~25.6msec. (512-stage)
  5.12~51.2msec. (512×2-stage)
- Clock component cancellation capability.
- No insertion loss: $L_i \simeq 0$ dB typ.
- Wide dynamic range: S/N ≃ 85dB typ.
- Wide frequency response: f_i < 12kHz.
- Total harmonic distortion: THD=0.4% typ. (V_i=0.78Vrms)
- Clock frequency range: 10~100kHz.
- Dual 512-stage configuration: 1024-stage in series connection, and twice as large output in parallel connection.
- P-channel silicon gate, tetrode MOS transistors configuration.
- 14-lead dual-in-line package.

Block Diagram



Applications:

- Vibrato and/ or chorus effects in electronic organs and musical instruments.
- Reverberation effect of electronic musical instruments.
- Variadle or fixed delay of analog signals.

Quick Reference Data

Item	Symbol	Value	Unit
Supply Voltage	V_{DD} V_{GG}	−15, V_{DD}+1	V
Signal Delay Time	t_D	2.56~51.2	msec
Total Harmonic Distortion	THD	0.4	%
Signal to Noise Ratio	S/N	85	dB

Absolute Maximum Ratings (Ta=25℃)

Item	Symbol	Ratings	Unit
Terminal Voltage	V_{DD}, V_{GG}, V_{CP}, V_I	−18～+0.3	V
Output Voltage	V_O	−18～+0.3	V
Operating Temperature	Topr	−20～+60	℃
Storage Temperature	Tstg	−55～+125	℃

Operating Conditions (Ta=25℃)

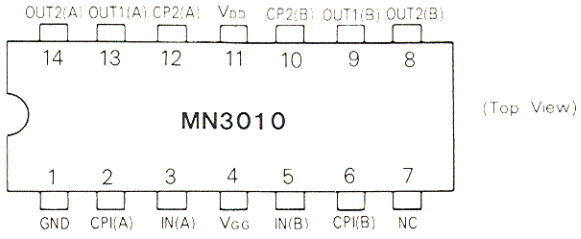
Item	Symbol	Min.	Typ.	Max.	Unit
Drain Supply Voltage	V_{DD}	−14	−15	−16	V
Gate Supply Voltage	V_{GG}		V_{DD}+1		V
Clock Voltage "H" Level	V_{CPH}	0		−1	V
Clock Voltage "L" Level	V_{CPL}		V_{DD}		V
Clock Input Capacitance	C_{CP}			350	pF
Clock Frequency	f_{CP}	10		100	kHz
Clock Pulse Width *2	t_{cpw}			0.5T*1	
Clock Rise Time *2	t_{cpr}			500	nsec
Clock Fall Time *2	t_{cpf}			500	nsec
Clock Cross Point	Vx	0		−3	V

*1 $T=1/f_{CP}$ *2 Clock Pulse Waveforms

Electrical Characteristics (Ta=25℃, $V_{DD}=V_{CPL}=-15V$, $V_{CPH}=0V$, $V_{GG}=-14V$, $R_L=100k\Omega$)

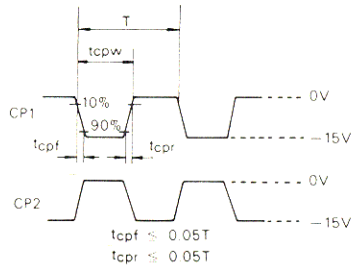
Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Signal Delay Time	t_D		2.56		25.6	msec
Input Signal Frequency	f_i	f_{cp}=40kHz, V_i=1.8 Vrms, 3dB down (0dB at f_i=1kHz)			12	kHz
Input Signal Swing	V_i	f_{cp}=40kHz, f_i=1kHz, THD=2.5%			1.8	Vrms
Insertion Loss	L_i	f_{cp}=40kHz, f_i=1kHz, V_i=1.8 Vrms		0		dB
Total Harmonic Distortion	THD	f_{cp}=40kHz, f_i=1kHz, V_i=0.78Vrms		0.4		%
Noise Voltage	Vno	f_{cp}=100kHz Weighted by "A" curve			0.21	mVrms
Signal to Noise Ratio	S/N	Maximum output voltage to noise voltage		85		dB

Terminal Assignments

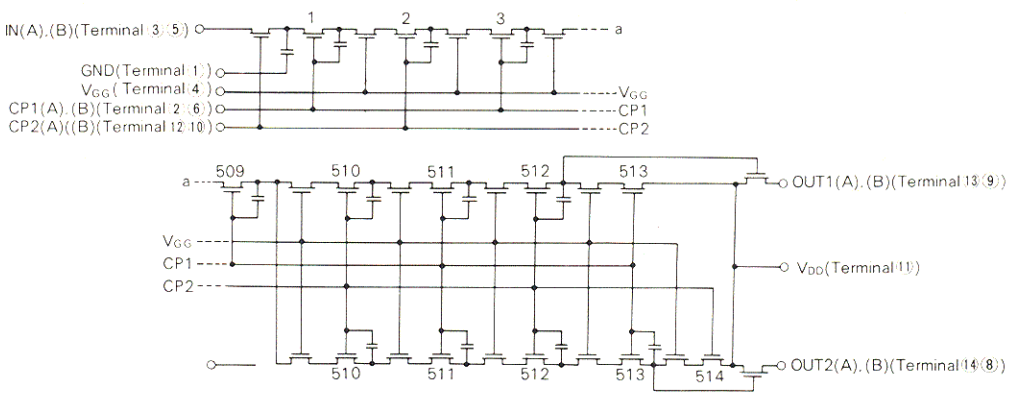


(Top View)

Clock Pulse Waveforms

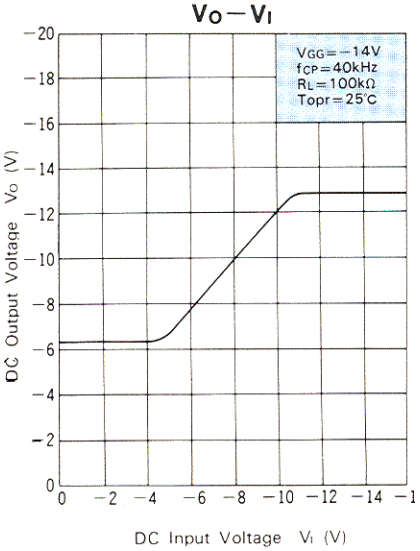


Circuit Diagram

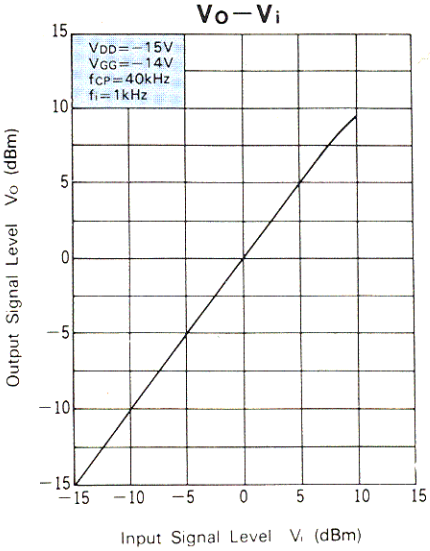


Typical Electrical Characteristic Curves

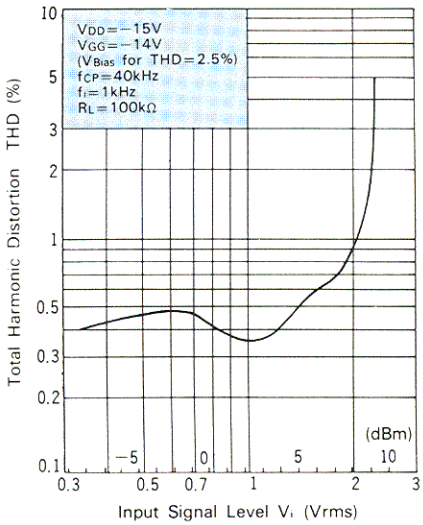
$V_O - V_I$



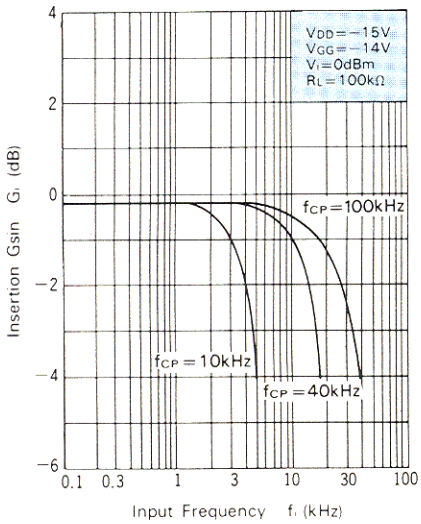
$V_O - V_i$



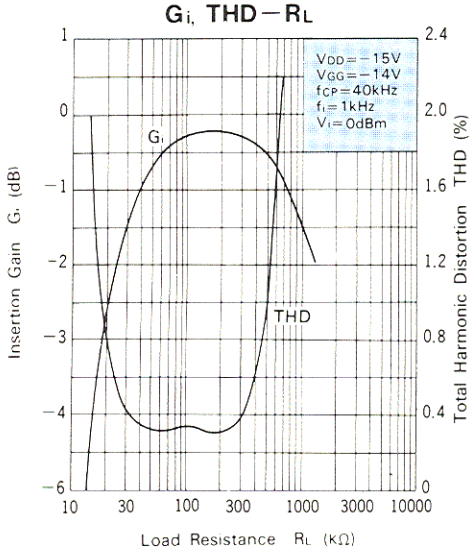
$THD - V_i$



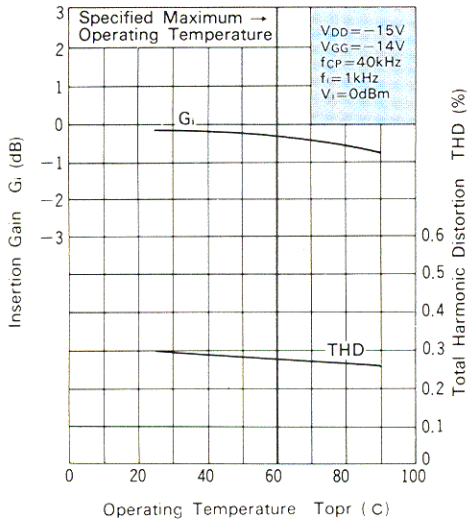
$G_i - f_i$



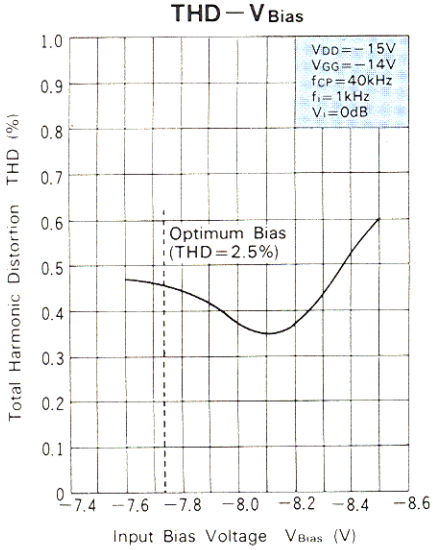
G_i, $THD - R_L$



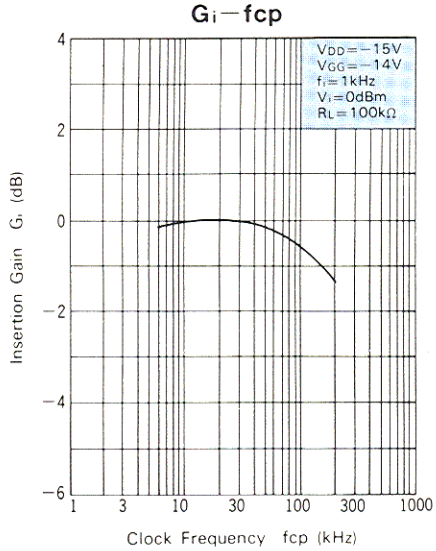
G_i, $THD - Topr$



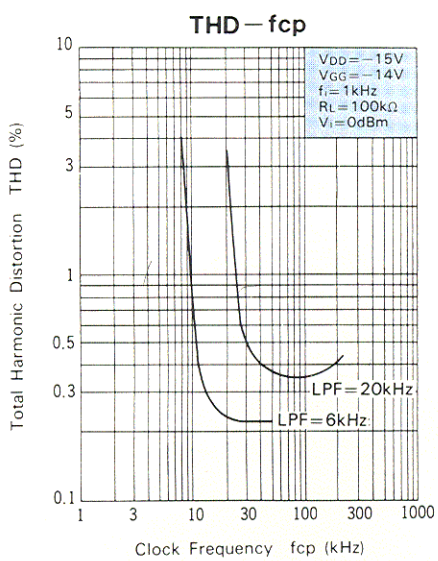
$THD - V_{Bias}$



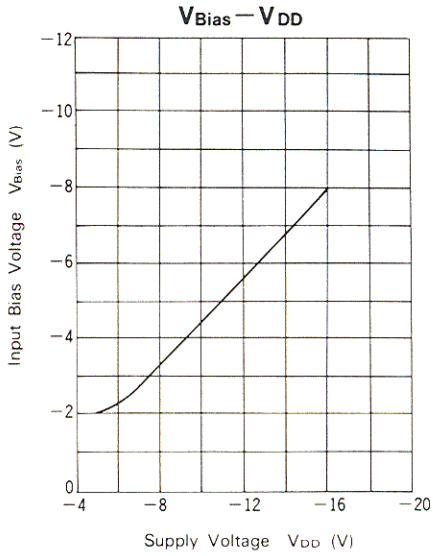
$G_i - fcp$

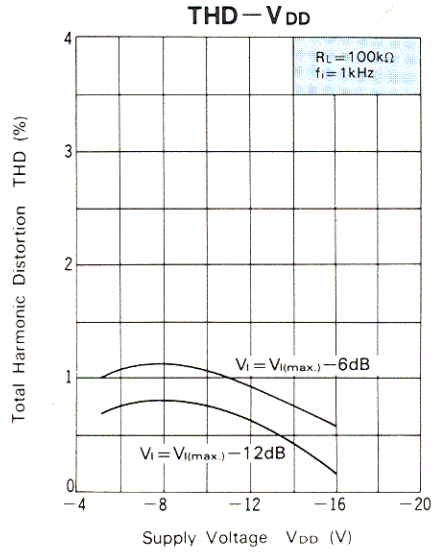


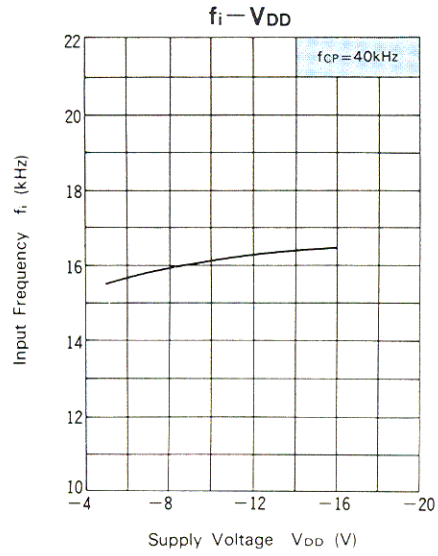
$THD - fcp$

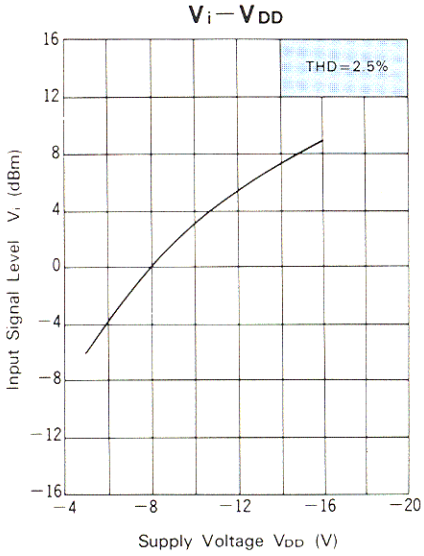


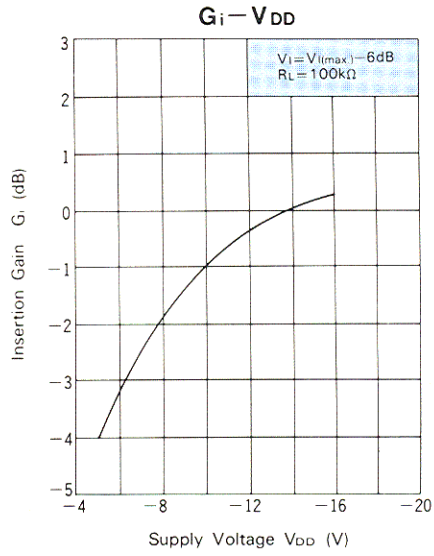
Supply Voltage Characteristics

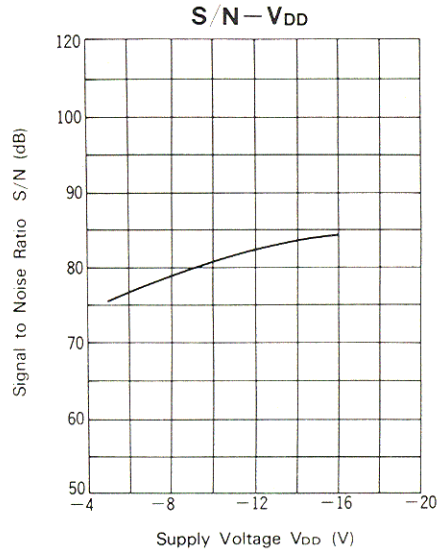




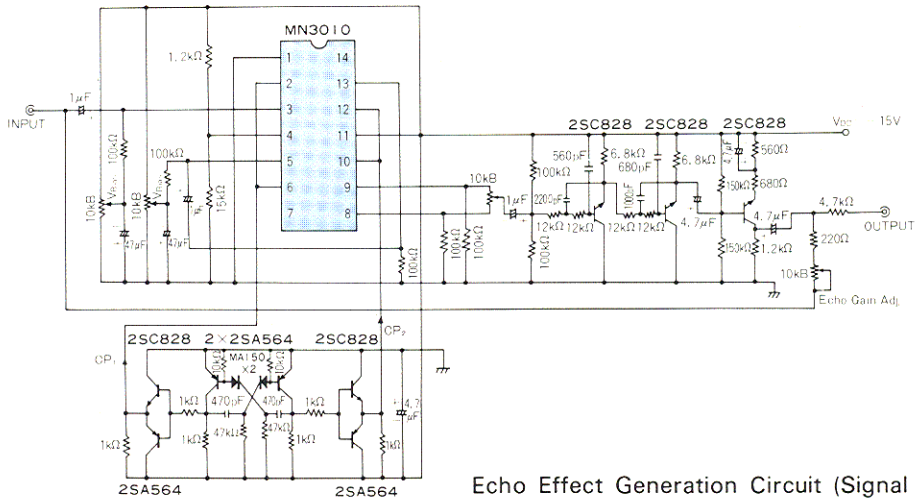








Application Circuit



Echo Effect Generation Circuit (Signal Delay Over 10msec.)