ERROR CORRECTOR FOR COMPACT DISC

GENERAL DESCRIPTION

The SAA7020 detects and corrects errors in digital data received from the demodulator (SAA7010). The data is received serially in frames of 32 x 8-bit symbols and, after processing, is transmitted in a 16-bit serial format to the interpolating and muting circuit (SAA7000). An error flag is generated to warn of data in which errors have not been corrected.

Features

- Internal timing and control circuits
- Serial data input and output
- 8-bit bidirectional data bus to external RAM (2K x 8 bits)
- Corrects up to seven erroneous frames of data
- Generates error flag to identify unreliable data
- Provides a motor speed control output which stabilizes the input data rate and eliminates wow and flutter.

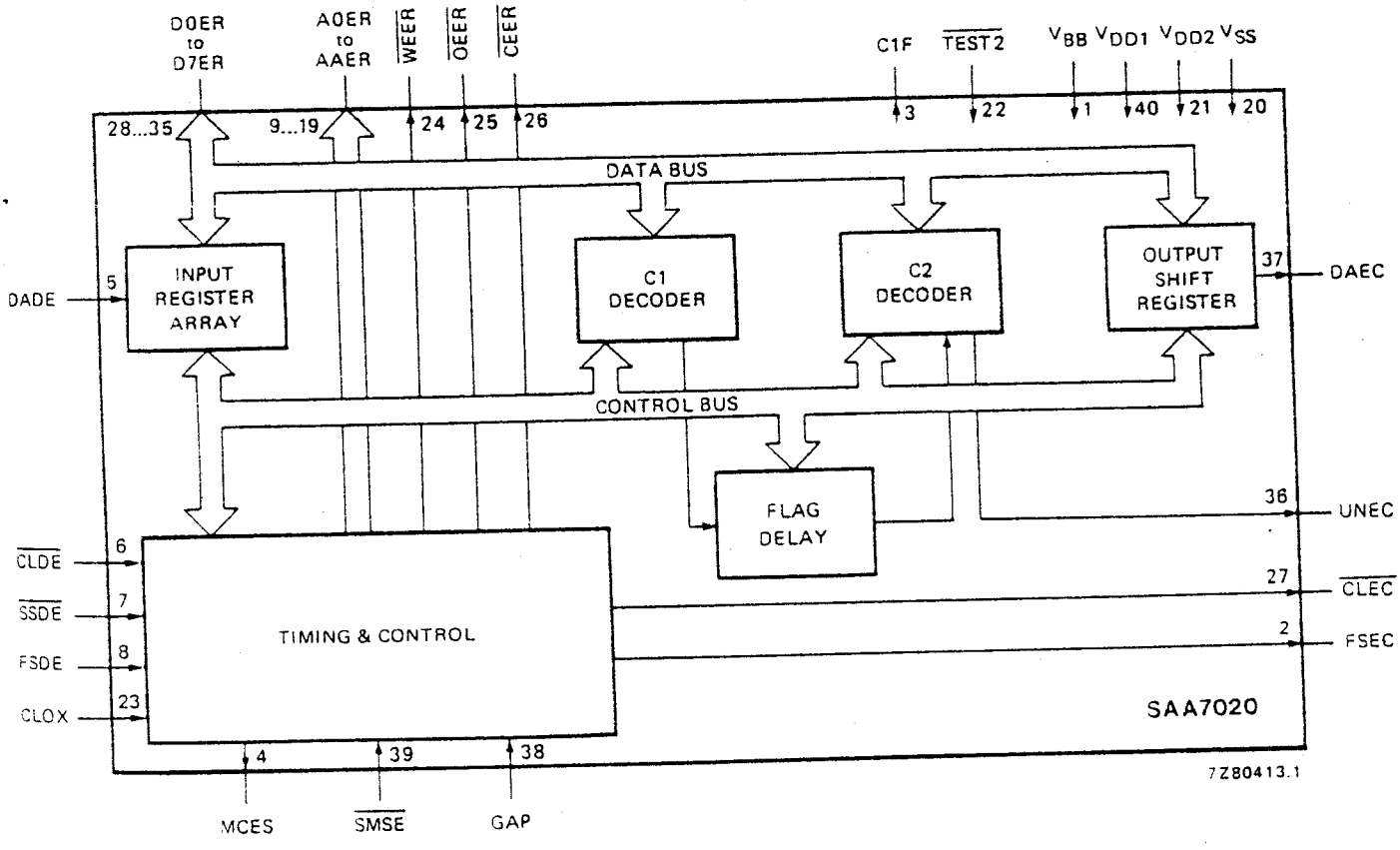

Fig. 1 Block diagram.

PACKAGE OUTLINE

40-lead DIL; plastic (SOT-129).

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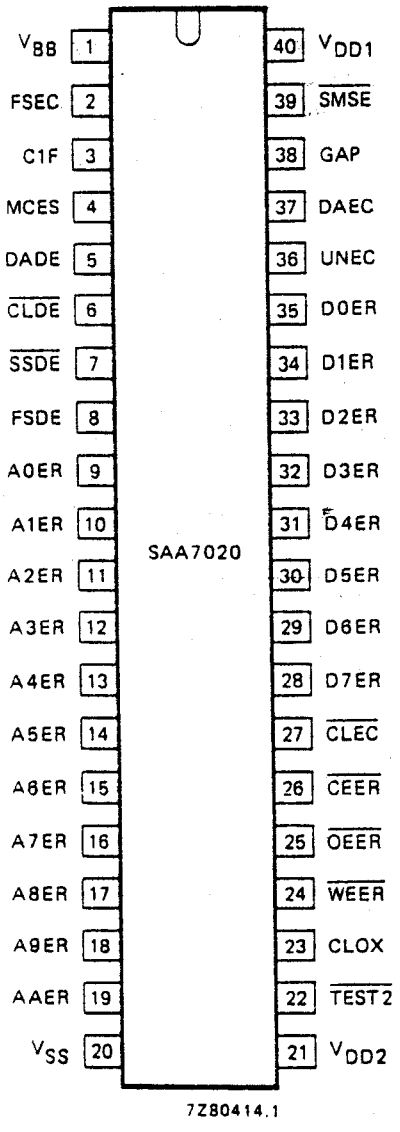

Fig. 2 Pinning diagram.

PINNING

1	V_{BB}	back bias supply
2	FSEC	frame sync pulse output
3	C1F	C1 decoder error flag
4	MCES	motor speed control output
5	DADE	serial data input
6	$\overline{CLDE}$	data bit clock input
7	$\overline{SSDE}$	symbol sync signal input
8	FSDE	frame sync signal input
9-19	A0ER-AAER	address outputs to external RAM
20	V_{SS}	ground
21	V_{DD2}	+ 12 V supply
22	$\overline{TEST2}$	test input
23	CLOX	basic clock input
24	$\overline{WEER}$	write enable output to external RAM
25	$\overline{OEER}$	output enable signal to external RAM
26	$\overline{CEER}$	chip enable output to external RAM
27	$\overline{CLEC}$	output data clock
28-35	D0ER-D7ER	data bus to/from external RAM
36	UNEC	error flag output
37	DAEC	data output (two's complement) and SAA7000 output format control
38	GAP	input to determine DAEC control output to SAA7000
39	$\overline{SMSE}$	mute signal from servo
40	V_{DD1}	+ 5 V supply

ERROR CORRECTOR FOR COMPACT DISC — SAA7020

FUNCTIONAL DESCRIPTION

The SAA7020 error corrector receives data samples from the Compact Disc Digital Audio demodulating system (SAA7010), processes the data samples and then passes them to the interpolating and muting circuit (SAA7000). The processing detects erroneous data and then, if possible, corrects the errors. If error correction is not possible, a flag (UNEC) is generated to warn of unreliable data output. The SAA7020 also controls the motor speed of the disc drive servo.

Serial data received from the demodulator (SAA7010) is arranged in frames of 32 x 8-bit symbols; 24 of the symbols contain audio samples; the remaining eight symbols contain parity information for error detection/correction. The data (DADE) is clocked into the input register array at the demodulator rate by $\overline{\text{CLDE}}$. The input register array comprises a register which accumulates symbols ready for parallel output to an external RAM and a FIFO register which acts as a jitter reduction circuit.

The jitter reduction circuit uses the difference between the input data rate ($\overline{\text{CLDE}}$) and the system data rate (derived from CLOX) to generate the motor speed control signal $\overline{\text{MCES}}$ (Fig. 3). This forms a feedback loop with the disc drive motor to control the disc speed and hence the input data rate. In this way unwanted effects such as wow and flutter are eliminated from the Compact Disc system, the FIFO being capable of handling deviations from the system data rate of up to ± 2 frames.

An 8-bit bidirectional bus is used for transferring data to and from the external RAM (2K x 8 bits) and an 11-bit bus for addressing. Three bits control the RAM; write enable $\overline{\text{WEER}}$, output enable $\overline{\text{OEER}}$ and chip enable $\overline{\text{CEER}}$ (the latter is for operation with dynamic RAMs).

The error correction process makes use of data interleaving and two Reed-Solomon codes, C1 and C2. The C1 decoder can correct one erroneous symbol in a 32-symbol frame after de-interleaving; the C2 decoder can correct two erroneous symbols in a group of 28 symbols. Input data is de-interleaved and read from the RAM by the C1 decoder where syndromes are formed to check for erroneous symbols. If one error is detected it is corrected and the data is written back to the RAM with some parity symbols being discarded. If more than one error is detected the data is written back to the RAM unchanged but internal C1 flags are set to mark these symbols as unreliable. The data in the RAM is then further de-interleaved and read back to the C2 decoder. The symbols are then checked for errors as previously, if one error is detected it is corrected and the symbols are again written back to the RAM. If two error flags are detected erasure correction is attempted when the flags are received from C1. The corrected data is then written back to the RAM. If more than two symbols are in error the data is written back to the RAM unchanged but a flag is set to mark these symbols as unreliable. At this stage the remaining parity bits are discarded.

After processing, the data is held in the RAM to give a 5-frame delay so that the error warning flag UNEC can be sent to the interpolation and muting circuit (SAA7000). The UNEC flag is also output when $\overline{\text{SMSE}}$ is active, this warns of data to be immediately muted. At the end of the 5-frame delay, the data is read back to the output shift register to be serially shifted out at DAEC.

Pin functions

pin no.	mnemonic	description
1	V_{BB}	Back bias supply voltage: −2,5 V ± 20%.
2	FSEC	Frame sync pulse output, data is valid on the falling edge (Figs 5 and 9).
3	C1F	This output pin flags uncorrectable C1 errors.
4	MCES	Motor control error signal; this open drain output provides a pulse width modulated signal to control the rate of data entry. If the data rate has been correct for a period, MCES duty cycle = 50%; if low, the duty cycle < 50%; if high, the duty cycle > 50% (Fig. 3).
5	DADE	Serial data input. The data is clocked in by $\overline{CLDE}$ in 8-bit symbols, the most-significant bit first (Figs 4 and 6).
6	$\overline{CLDE}$	Data clock input, data is accepted into DADE on the negative transition of $\overline{CLDE}$ (Figs 4 and 6).
7	$\overline{SSDE}$	Input indicating the last bit of a symbol. A symbol is counted and clocked in when $\overline{SSDE}$ is LOW during the negative transition of $\overline{CLDE}$; for correct operation, $\overline{SSDE}$ must remain LOW for only one negative transition in eight (Figs 4 and 6).
8	FSDE	Input indicating the end of a data frame. Indication is given when FSDE is HIGH during a negative transition of $\overline{CLDE}$.
9-19	A0ER-AAER	Eleven address outputs to the external RAM. When data is being received at DADE, $\overline{CLDE}$, etc. then addresses A0ER to AAER are completely exercised every four frames allowing refresh to be automatic for dynamic RAMs (Figs 7 and 8).
20	V_{SS}	Ground.
21	V_{DD2}	Positive supply voltage: + 12 V ± 10%.
22	$\overline{TEST2}$	Test input. Connect to V_{DD1} or V_{DD2} for normal operation.
23	CLOX	System clock input, typical frequency = 4,2336 MHz (Fig. 6).
24	$\overline{WEER}$	Write enable output to external RAM; when LOW, SAA7020 is writing to the RAM (Fig. 7).
25	$\overline{OEER}$	Output enable to external RAM; when HIGH, memory output buffers must be in the high impedance state (Figs 7 and 8).
26	$\overline{CEER}$	Chip enable output for use with dynamic memories (Figs 7 and 8).
27	$\overline{CLEC}$	Output data clock; data is valid on the falling edge (Figs 5 and 9).
28-35	D0ER-D7ER	Input/output ports for 8-bit bidirectional bus from/to external RAM. The outputs are in the high impedance state when $\overline{OEER}$ is LOW (Figs 7 and 8).
36	UNEC	Error flag output; when HIGH, indicates that output data is unreliable. During active data output (i.e. when $\overline{CLEC}$ is operating) UNEC applies to each symbol of 8 bits of data output at that time. Before each data word of two symbols is output, UNEC applies to the whole data word that will follow in five frames time.

ERROR CORRECTOR FOR COMPACT DISC — SAA7020

FUNCTIONAL DESCRIPTION (continued)

pin no.	mnemonic	description
37	DAEC	Serial data output. Data is clocked out by $\overline{CLEC}$ and is in 16-bit words separated by gaps. Each word is in two's complement format with the most-significant bit first and comprises two 8-bit symbols. Data is valid on the falling edge of $\overline{CLEC}$. During the gap between the data words, the state of pin 38 (GAP) acts as an output from DAEC (Figs 5 and 9).
38	GAP	The input level at this pin is reflected in the state of the output from DAEC between data words and is used to control the output format of the SAA7000. When GAP is HIGH, DAEC gap level is HIGH, and vice versa (Fig. 5).
39	$\overline{SMSE}$	Select muting input. If $\overline{SMSE}$ is held LOW, the UNEC output will be held HIGH causing the interpolation and muting circuit (SAA7000) to mute the data.
40	V_{DD1}	Positive supply voltage: + 5 V ± 10%.

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HANDLING

Inputs and outputs are protected against electrostatic charge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices (see 'Handling MOS Devices').

RATINGS

Limiting values in accordance with the Absolute Maximum Rating System (IEC 134); V_{SS} = 0 V

Supply voltage 1 range (pin 40)	V_{DD1}	−0,3 to + 7,5 V
Supply voltage 2 range (pin 21)	V_{DD2}	−0,3 to + 15 V
Back bias supply voltage range (pin 1)	V_{BB}	−4 to + 0,3 V
Input voltage range (except TEST)	V_I	−0,3 to + 7,5 V
Input voltage range (TEST only)	V_I	−0,3 to + 15 V
Output voltage range (except MCES)	V_O	−0,3 to + 7,5 V
Output voltage range (MCES only) applied through a 10 kΩ resistor	V_O	−0,35 to + 15 V
Output current	I_O	max. 10 mA
Operating ambient temperature range	T_{amb}	−20 to + 70 °C
Storage temperature range	T_{stg}	−55 to + 125 °C

ERROR CORRECTOR FOR COMPACT DISC SAA7020

CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = −20 to + 70 °C unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supplies					
Supply voltage 1 (pin 40)	V_{DD1}	4,5	5,0	5,5	V
Supply voltage 2 (pin 21)	V_{DD2}	10,8	12,0	13,2	V
Back bias supply voltage (pin 1)	$-V_{BB}$	2,0	2,5	3,0	V
Supply current 1 (pin 40)	I_{DD1}	–	145	280	mA
Supply current 2 (pin 21)	I_{DD2}	–	14	26	mA
Back bias supply current (pin 1)	$-I_{BB}$	–	–	500	μA
Inputs (except D0ER-D7ER)					
Input voltage LOW	V_{IL}	−0,3	–	+ 0,8	V
Input voltage HIGH (except $\overline{SMSE}$)	V_{IH}	2,4	–	6,5	V
Input voltage HIGH ($\overline{SMSE}$ only)	V_{IH}	2,0	–	6,5	V
Input current (note 1)	I_I	−1	–	+ 1	μA
Input capacitance	C_I	–	–	7	pF
Input/output D0ER-D7ER					
Input voltage LOW	V_{IL}	−0,3	–	+ 0,8	V
Input voltage HIGH	V_{IH}	2,0	–	6,5	V
Input current (notes 1 and 2)	I_I	−10	–	+ 10	μA
Input capacitance	C_I	–	–	10	pF
Output voltage LOW at $-I_{OL}$ = 1,6 mA (notes 3 and 4)	V_{OL}	0	–	0,4	V
Output voltage HIGH at I_{OH} = 0,2 mA (notes 3 and 4)	V_{OH}	3,0	–	V_{DD1} + 0,5	V
Load capacitance (notes 3 and 4)	C_L	–	–	150	pF
Outputs A0ER-AAER, $\overline{WEER}$, $\overline{OEER}$, $\overline{CEER}$, DAEC, UNEC, FSEC, $\overline{CLEC}$ (notes 3 and 4)					
Output voltage LOW at $-I_{OL}$ = 1,6 mA	V_{OL}	0	–	0,4	V
Output voltage HIGH at I_{OH} = 0,2 mA	V_{OH}	3,0	–	V_{DD1} + 0,5	V
Load capacitance	C_L	–	–	150	pF
Output MCES (open drain) (note 5)					
Output voltage LOW with pin 4 connected to V_{DD2} via a 10 kΩ resistor	V_{OL}	0	–	0,4	V
Output current with output OFF and pin 4 connected to V_{DD2} via a 10 kΩ resistor; T_{amb} = 25 °C	I_{OH}	–	–	20	μA

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parameter	symbol	min.	typ.	max.	unit
Input CLOX (note 6)					
Operating frequency	f_{IN}	3,0	4,2336	4,5	MHz
Input clock LOW	t_{IXL}	40	–	–	ns
Input clock HIGH	t_{IXH}	40	–	–	ns
Inputs DADE, $\overline{\text{CLDE}}$, $\overline{\text{SSDE}}$, FSDE (note 7)					
Input rise time	t_{IR}	–	–	50	ns
Input fall time	t_{IF}	–	–	50	ns
$\overline{\text{CLDE}}$ period	t_{ICP}	1 CLOX period	–	20	µs
$\overline{\text{CLDE}}$ HIGH	t_{ICH}	100	–	–	ns
$\overline{\text{CLDE}}$ LOW	t_{ICL}	100	–	–	ns
DADE/$\overline{\text{SSDE}}$/FSDE to $\overline{\text{CLDE}}$ set-up time	t_{IDS}	50	–	–	ns
$\overline{\text{CLDE}}$ to DADE/$\overline{\text{SSDE}}$/FSDE hold time	t_{IDH}	80	–	–	ns
$\overline{\text{SSDE}}$ LOW time	t_{SSL}	–	1	–	$\overline{\text{CLDE}}$ period
$\overline{\text{CLDE}}$ gap after FSDE	t_{FCG}	6	–	–	CLOX periods
Input $\overline{\text{SMSE}}$ (note 7)					
Input rise time	t_{IR}	–	1	100	µs
Input fall time	t_{IF}	–	1	100	µs
SMSE to UNEC output delay time	t_{SMD}	–	–	20	CLOX periods
Outputs $\overline{\text{CLEC}}$, DAEC, UNEC, FSEC (notes 3, 4, 7 and 8)					
Output rise time	t_{OR}	–	–	50	ns
Output fall time	t_{OF}	–	–	40	ns
$\overline{\text{CLEC}}$ HIGH	t_{OCH}	130	–	350	ns
$\overline{\text{CLEC}}$ LOW	t_{OCL}	130	–	–	ns
FSEC HIGH	t_{FSH}	6 CLOX periods −180	–	6 CLOX periods + 180	ns
$\overline{\text{CLEC}}$ to FSEC delay time	t_{CFD}	3 CLOX periods −300	–	3 CLOX periods + 300	ns
DAEC/UNEC to FSEC set-up time	t_{UFS}	100	–	–	ns
FSEC to DAEC/UNEC hold time	t_{UFH}	12	–	–	CLOX periods

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parameter	symbol	min.	typ.	max.	unit
RAM interfaces A0ER-AAER, D0ER-D7ER, $\overline{OEER}$, $\overline{CEER}$, $\overline{WEER}$ (notes 3, 4 and 7)					
Output rise time	t_{OR}	–	–	30	ns
Output fall time	t_{OF}	–	–	25	ns
Cycle time	t_C	390	–	670	ns
Read cycle timing					
$\overline{CEER}$ HIGH time	t_{CEH}	65	–	–	ns
$\overline{CEER}$ LOW time	t_{CEL}	265	–	–	ns
A0ER-AAER to $\overline{CEER}$ set-up time	t_{ACS}	0	–	–	ns
$\overline{CEER}$ to A0ER-AAER hold time	t_{ACH}	300	–	–	ns
D0ER-D7ER to $\overline{OEER}$ set-up time	t_{DOS}	85	–	–	ns
$\overline{OEER}$ to D0ER-D7ER hold time	t_{DOH}	0	–	–	ns
D0ER-D7ER to A0ER-AAER set-up time	t_{DAS}	85	–	–	ns
A0ER-AAER to D0ER-D7ER hold time	t_{DAH}	0	–	–	ns
$\overline{OEER}$ to D0ER-D7ER from RAM active	t_{OLZ}	0	–	–	ns
$\overline{OEER}$ to D0ER-D7ER from RAM high impedance state	t_{OHZ}	0	–	100	ns
$\overline{OEER}$ LOW to A0ER-AAER valid	t_{OAD}	−25	–	+ 25	ns
Write cycle timing					
$\overline{CEER}$ HIGH time	t_{CEH}	196	–	–	ns
$\overline{CEER}$ LOW time	t_{CEL}	196	–	–	ns
A0ER-AAER to $\overline{CEER}$ set-up time	t_{ACS}	100	–	–	ns
A0ER-AAER to $\overline{WEER}$ set-up time	t_{AWS}	50	–	–	ns
$\overline{WEER}$ to A0ER-AAER hold time	t_{AWH}	50	–	–	ns
$\overline{WEER}$ to $\overline{CEER}$ set-up time	t_{WCS}	50	–	–	ns
$\overline{CEER}$ to $\overline{WEER}$ hold time	t_{WCH}	65	–	–	ns
D0ER-D7ER to $\overline{CEER}$ set-up time	t_{DCS}	50	–	–	ns
$\overline{CEER}$ to D0ER-D7ER hold time	t_{DCH}	150	–	–	ns
$\overline{WEER}$ to $\overline{CEER}$ recovery time	t_{WR}	65	–	–	ns
D0ER-D7ER to $\overline{WEER}$ set-up time	t_{DWS}	150	–	–	ns
$\overline{WEER}$ to D0ER-D7ER hold time	t_{DWH}	100	–	–	ns
$\overline{OEER}$ to D0ER-D7ER output active	t_{DOZ}	100	–	–	ns
$\overline{OEER}$ to D0ER-D7ER output in high impedance state	t_{ODZ}	20	–	–	ns

NOTES TO THE CHARACTERISTICS

1. Measured from −0,3 to + 6,5 V at T_{amb} = 25 °C; V_{DD1} = 6,5 V.
2. Input/output port in high impedance state (OFF); measured from 0 to 6 V at T_{amb} = 25 °C.
3. Output loading: 1 TTL gate + C_L = 50 pF.
4. All outputs are protected against short-circuit to V_{SS} and V_{DD1}. The maximum load capacitance that can be applied before the short-circuit protection becomes active is 150 pF.
5. Phase detector gain for average MCES output voltage = 1,1 V per frame. Phase detector control range = ± 2 frames.
6. All maximum or minimum values assume respective frequency where appropriate.
7. Reference levels = 0,8 V and 2,4 V.
8. The DAEC level during the advanced UNEC period is defined by the state at pin 38 (GAP). If this state changes during $\overline{CLEC}$ LOW, the timings are applicable. If the state at pin 38 changes at other times, DAEC follows with a delay of between 20 and 500 ns.

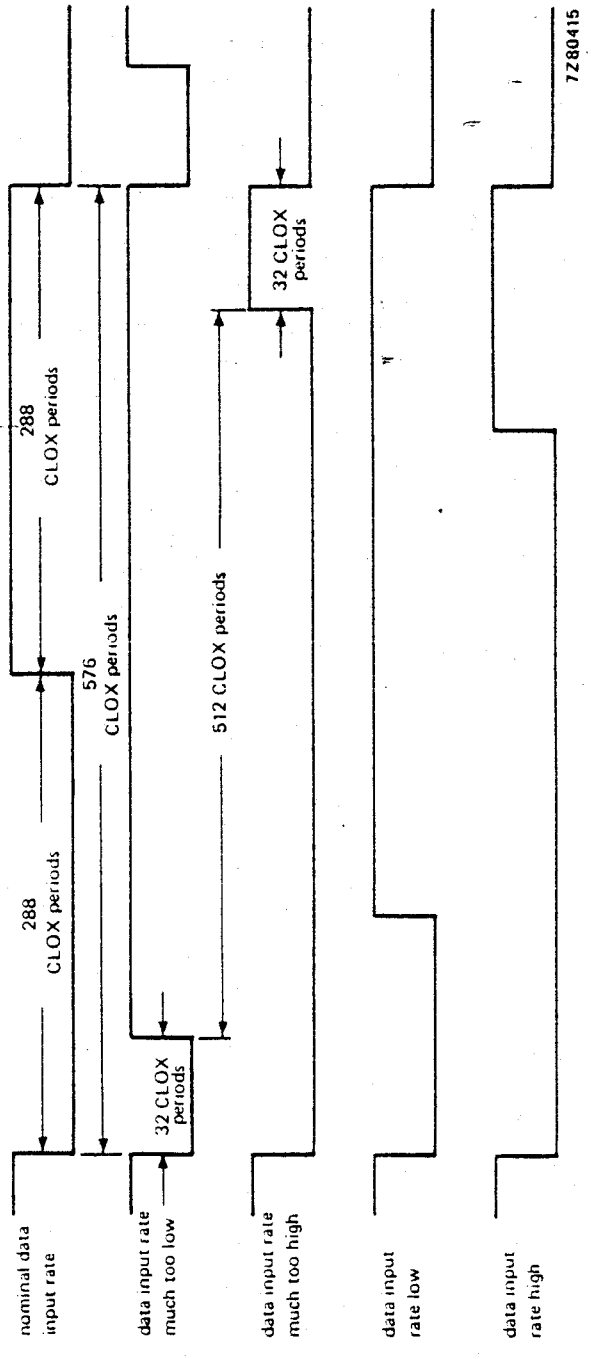


Fig. 3 MCES output waveforms: waveforms are updated each frame (576 CLOX periods); open drain output, rise times depend on external pull-up circuit. This output has an internal clamp to prevent the voltage at pin 4 (MCES) rising above V_{DD2} + 1,8 V maximum.

DEVELOPMENT SAMPLE DATA

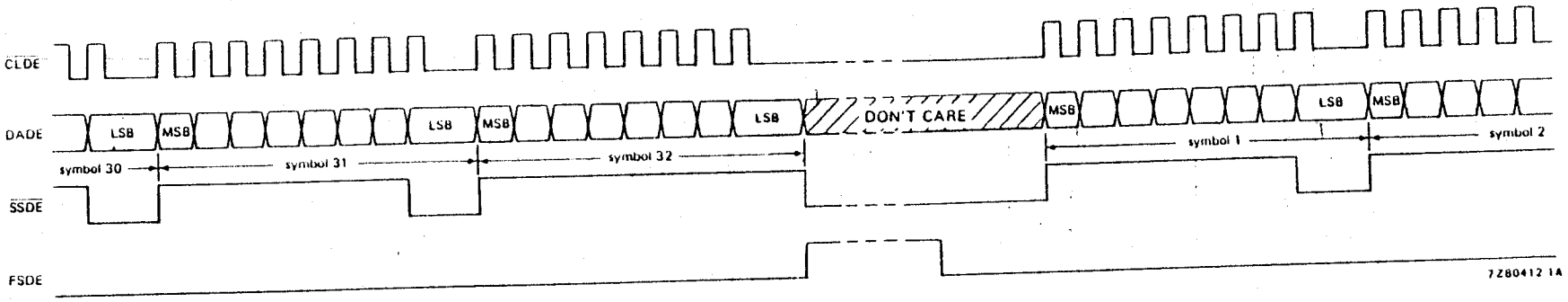
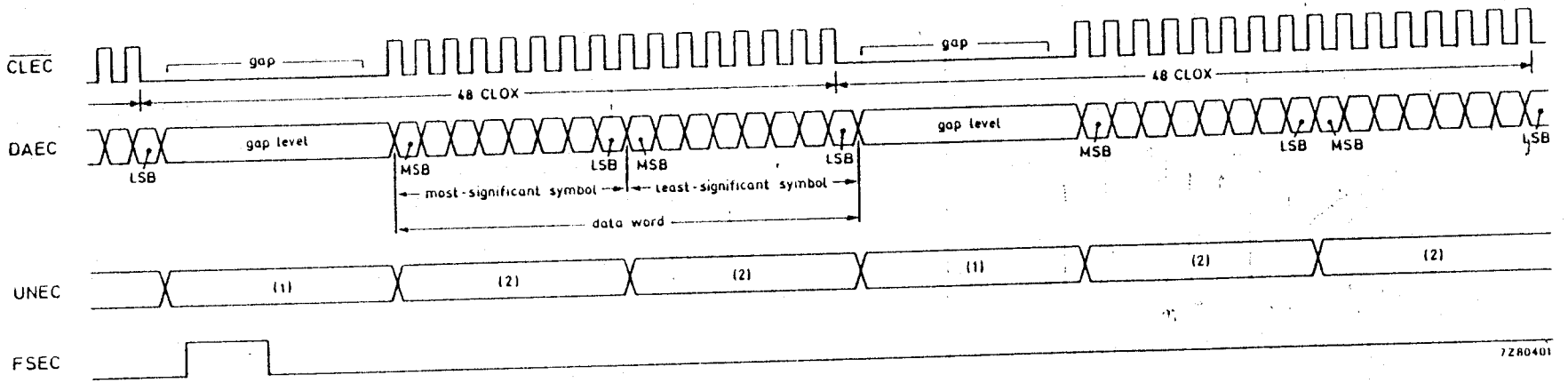


Fig. 4 Typical input waveforms from SAA7010/SAA7011.



(1) When HIGH indicates unreliability of data word that will follow five frames later.
(2) When HIGH indicates unreliability of current symbol.

Fig. 5 Typical output waveforms to SAA7000.

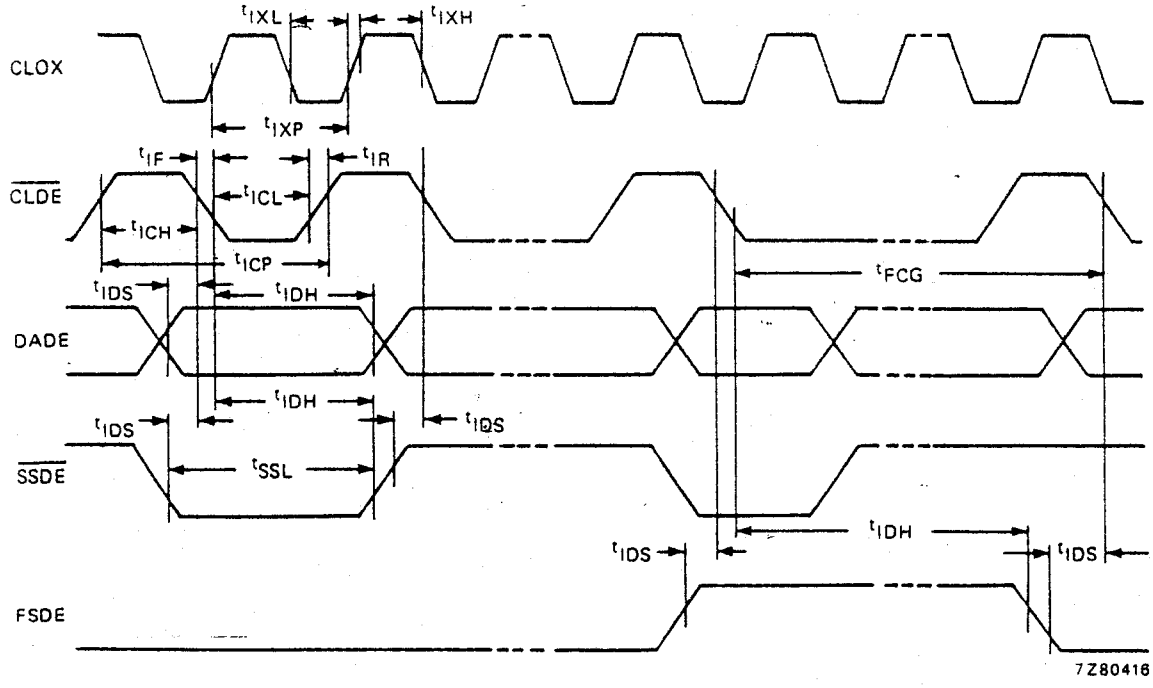


Fig. 6 Input waveform timing; reference levels = 0,8 V and 2,4 V.

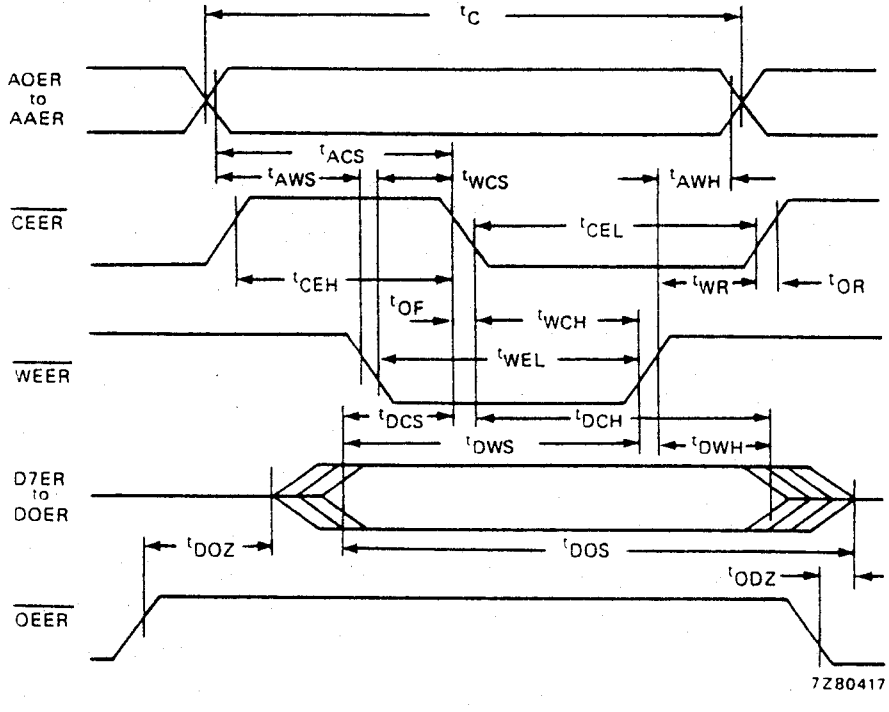


Fig. 7 RAM interface write cycle timing; reference levels = 0,8 V and 2,4 V, output loading = 1 TTL gate and C_L = 50 pF.

ERROR CORRECTOR FOR COMPACT DISC

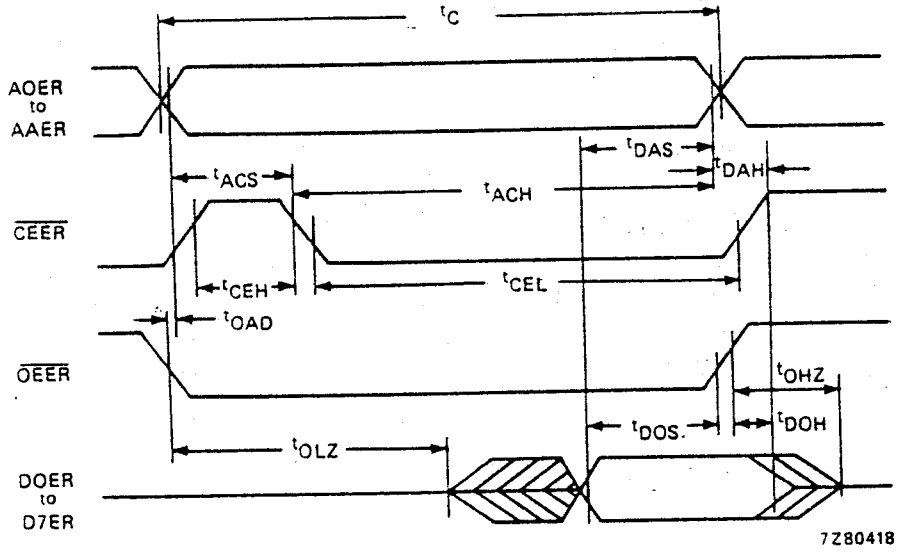
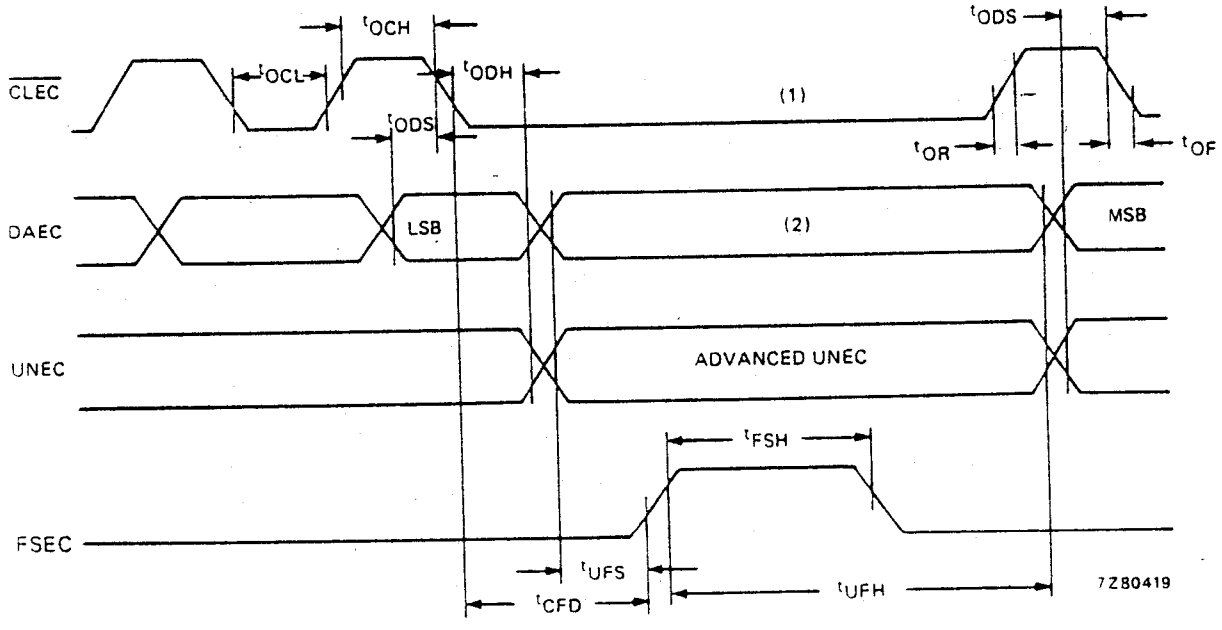


Fig. 8 RAM interface read cycle timing; reference levels = 0,8 V and 2,4 V; output loading = 1 TTL gate and C_L = 50 pF; $\overline{WEER}$ is HIGH during read cycle.



(1) $\overline{CLEC}$ remains LOW for 8 $\overline{CLEC}$ cycle periods.
(2) DAEC level during this period is defined by the level on pin 38 (GAP). If GAP changes during $\overline{CLEC}$ active, the above timings apply. If GAP changes at other times, DAEC follows with a delay of 20 to 500 ns.

Fig. 9 Output waveform timing; reference levels = 0,8 V and 2,4 V, output loading = 1 TTL gate and C_L = 50 pF.