

J174 / J175 / J176 / J177

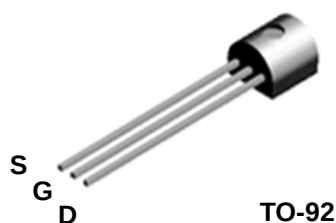
MMBFJ175 / MMBFJ176 / MMBFJ177

P-Channel Switch

Description

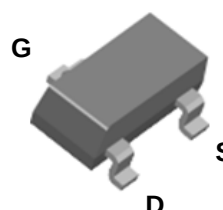
This device is designed for low-level analog switching sample-and-hold circuits and chopper-stabilized amplifiers. Sourced from process 88.

J174 / 175 / 176 / 177⁽¹⁾



TO-92

MMBFJ175 / 176 / 177



SOT-23

Mark: 6W / 6X / 6Y

Note: Source & drain are interchangeable.

Ordering Information

Part Number	Top Mark	Package	Packing Method
J175_D26Z	J175	TO-92-3L	Tape and Reel
J176_D74Z	J176	TO-92-3L	Ammo
MMBFJ175	6W	SOT-23 3L	Tape and Reel
MMBFJ176	6X	SOT-23 3L	Tape and Reel
MMBFJ177	6Y	SOT-23 3L	Tape and Reel

Note:

1. J174 & J177 are obsoleted.

Absolute Maximum Ratings⁽²⁾

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. Values are at $T_A = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Ratings	Units
V_{DG}	Drain-Gate Voltage	-30	V
V_{GS}	Gate-Source Voltage	30	V
I_{GF}	Forward Gate Current	50	mA
$T_J, T_{STG}^{(3)}$	Operating and Storage Junction Temperature Range	-55 to + 150	$^\circ\text{C}$

Notes:

- These ratings are limiting values above which the serviceability of any semiconductor device may be impaired.
- These ratings are based on a maximum junction temperature of 150°C .

These are steady-state limits. Fairchild Semiconductor should be consulted on applications involving pulsed or low duty cycle operations.

Thermal Characteristics⁽⁴⁾

Values are at $T_A = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Maximum		Units
		J175 - 176	MMBFJ175 - 177	
P_D	Total Device Dissipation	350	225	mW
	Derate above 25°C	2.8	1.8	mW/ $^\circ\text{C}$
$R_{\theta JC}$	Thermal Resistance, Junction to Case	125		$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	357	556	$^\circ\text{C/W}$

Note:

- PCB size: FR-4 76 x 114 x 0.6 T mm³ (3.0" x 4.5" x 0.062") with minimum land pattern size.

Electrical Characteristics

Values are at $T_A = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Condition		Min.	Max.	Units
Off Characteristics						
B _{(BR)GSS}	Gate-Source Breakdown Voltage	I _G = 1.0 μA, V _{DS} = 0		30		V
I _{GSS}	Gate Reverse Current	V _{GS} = 20 V, V _{DS} = 0			1.0	nA
V _{GS(off)}	Gate-Source Cut-Off Voltage	V _{DS} = -15 V, I _D = -10 nA	174	5.0	10.0	V
			175	3.0	6.0	V
			176	1.0	4.0	V
			177	0.8	2.5	V
On Characteristics						
I _{DSS}	Zero-Gate Voltage Drain Current	V _{DS} = -15 V, I _{GS} = 0	174	-20	-100	mA
			175	-7.0	-60.0	
			176	-2.0	-25	
			177	-1.5	-20.0	
r _{DS(on)}	Drain-Source On Resistance	I _C ≤ 50 mA, I _B = 5.0 mA	174		85	Ω
			175		125	
			176		250	
			177		300	

Typical Performance Characteristics

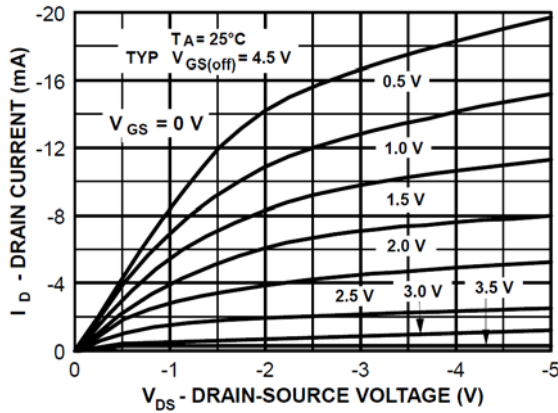


Figure 1. Common Drain-Source

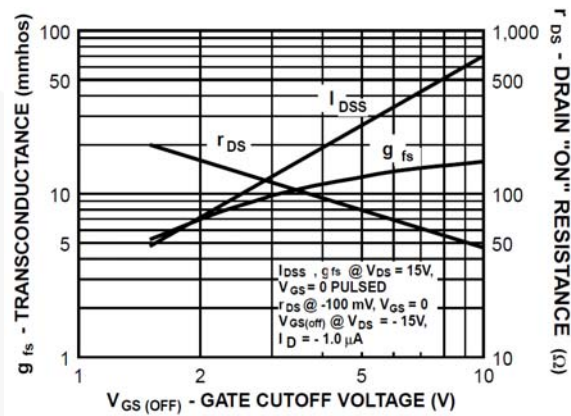


Figure 2. Parameter Interactions

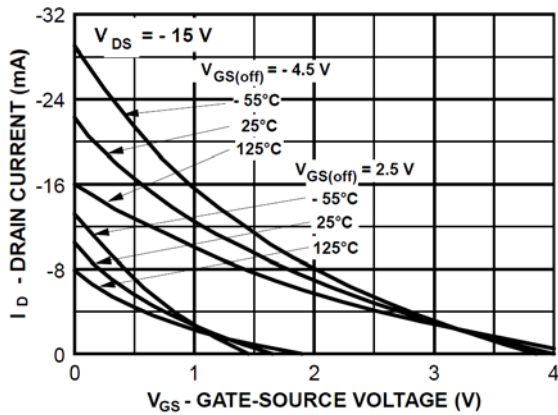


Figure 3. Transfer Characteristics

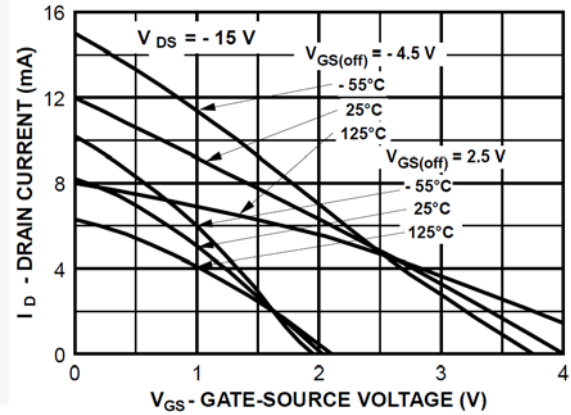


Figure 4. Transfer Characteristics

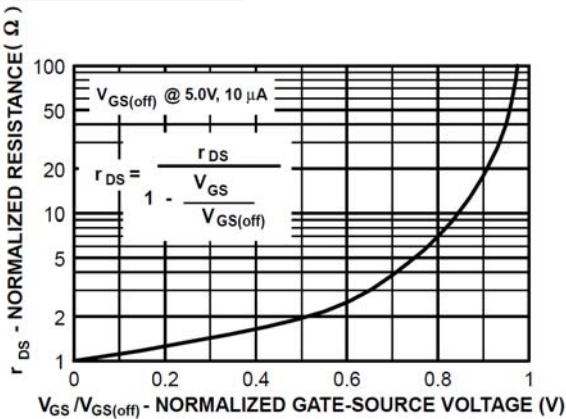


Figure 5. Normalized Drain Resistance vs. Bias Voltage

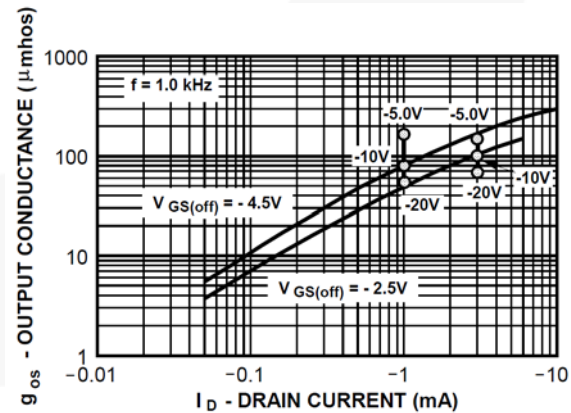


Figure 6. Output Conductance vs. Drain Current

Typical Performance Characteristics (Continued)

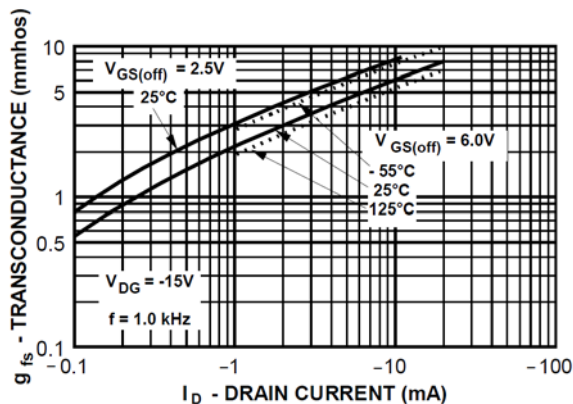


Figure 7. Transconductance vs. Drain Current

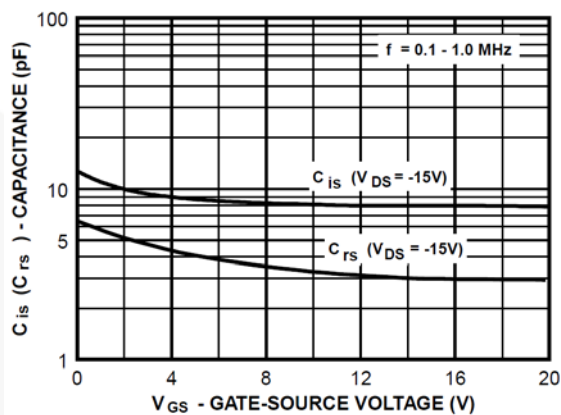


Figure 8. Capacitance vs. Voltage

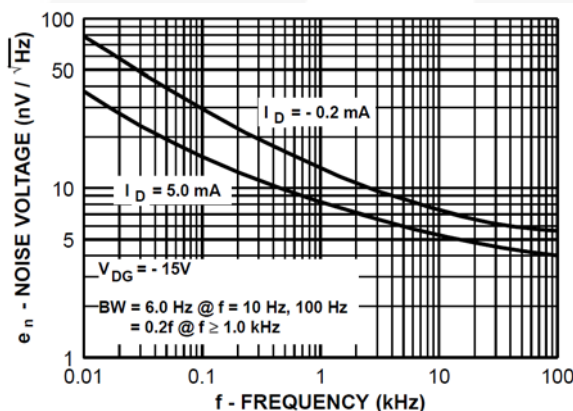


Figure 9. Noise Voltage vs. Frequency

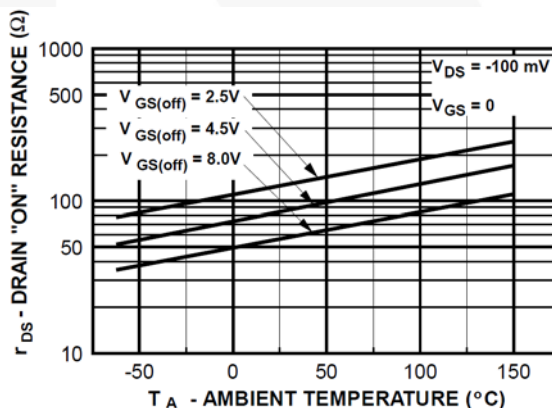


Figure 10. Channel Resistance vs. Temperature

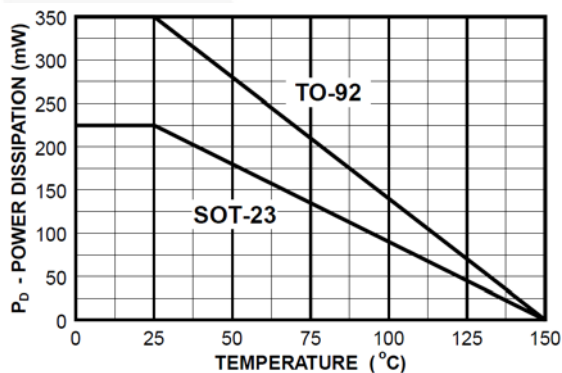
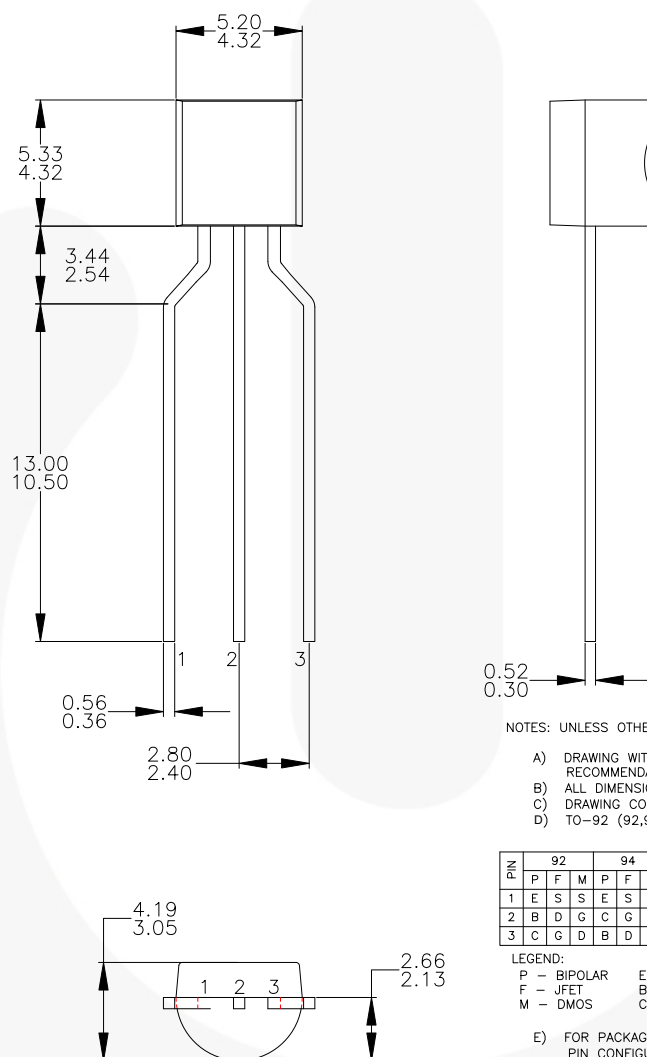


Figure 11. Power Dissipation vs. Ambient Temperature

Physical Dimensions

TO-92



NOTES: UNLESS OTHERWISE SPECIFIED

- A) DRAWING WITH REFERENCE TO JEDEC TO-92 RECOMMENDATIONS.
 B) ALL DIMENSIONS ARE IN MILLIMETERS.
 C) DRAWING CONFORMS TO ASME Y14.5M-1994.
 D) TO-92 (92,94,96,97,98) PIN CONFIGURATION:

PIN	92	94	96	97	98
1	P	F	M	P	F
2	E	S	S	E	S
3	B	D	G	C	D
4	C	G	D	B	G

LEGEND:

P — BIPOLAR E — EMITTER D — DRAIN
 F — JFET B — BASE S — SOURCE
 M — DMOS C — COLLECTOR G — GATE

- E) FOR PACKAGE 92, 94, 96, 97 AND 98:
 PIN CONFIGURATION DRAIN "D" AND SOURCE "S"
 ARE INTERCHANGEABLE AT JFET "F" OPTION.
 F) DRAWING FILENAME: MKT-ZA03FREV2.

Figure 12. 3-LEAD, TO92, MOLDED, 0.200 IN LINE SPACING LD FORM (J61Z OPTION) (ACTIVE)

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For current tape and reel specifications, visit Fairchild Semiconductor's online packaging area:

http://www.fairchildsemi.com/packaging/tr/to92_tr.pdf.

Physical Dimensions (Continued)

SOT-23

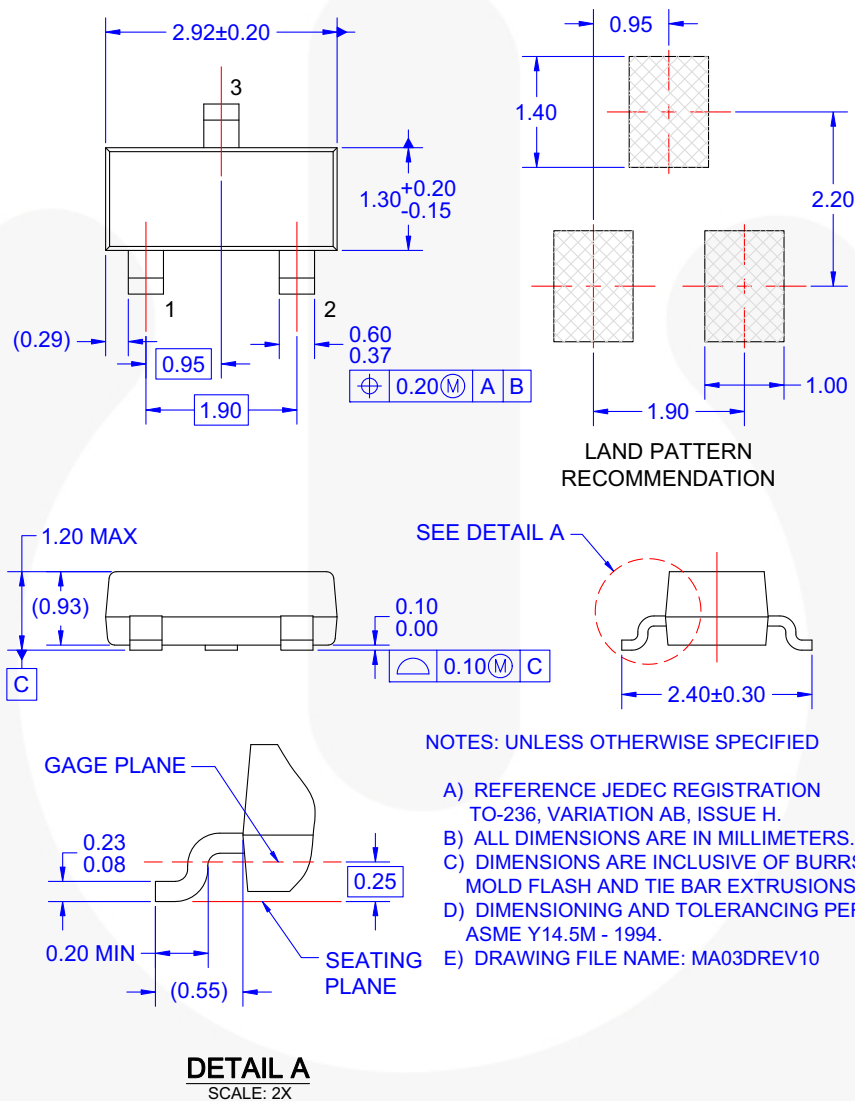


Figure 13. 3-LEAD, SOT23, JEDEC TO-236, LOW PROFILE (ACTIVE)

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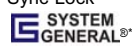
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