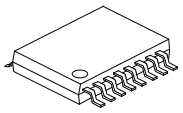
VGA OR DVI-I PORT COMPANION CIRCUIT



SSOP-16

■ DESCRIPTION

The UTC **CCVGA7C9** is an ESD solution for the VGA or DVI-I port connector. This device integrates ESD protection for all signals, level shifting for the DDC signals and buffering for the SYNC signals. ESD protection for the VIDEO, DDC and SYNC lines is implemented with low-capacitance current steering diodes.

Separate positive supply rails are provided for the VIDEO, DDC and SYNC channels to facilitate interfacing with low voltage video controller ICs to provide design flexibility in multi-supply-voltage environments.

Two non-inverting drivers provide buffering for the HSYNC and VSYNC signals from the video controller IC (SYNC1, SYNC2). These buffers accept TTL input levels and convert them to CMOS output levels that swing between Ground and V_{CC_SYNC}, which is typically 5V. Additionally, each driver has a series termination resistor (R_T) connected to the SYNC_OUT pin, eliminating the external termination resistors typically required for the HSYNC and VSYNC lines of the video cable. There are three versions with different values of RT to allow termination at typically 65Ω (UTC **CCVGA7C9**−00) or 15Ω (UTC **CCVGA7C9**−02).

Two N-channel MOSFETs provide the level shifting function required when the DDC controller is operated at a lower supply voltage than the monitor. The gate terminals for the MOSFETs (V_{CC_DDC}) should be connected to the supply rail (typically 3.3 V) that supplies power to the transceivers of the DDC controller.

All ESD diodes are designed to safely handle the high current spikes specified by IEC-61000-4-2 Level 4 (±8kV contact discharge if C_{BYP} is present, ±4kV if not). The ESD protection for the DDC signal pins are designed to prevent “back current” when the device is powered down while connected to a monitor that is powered up.

■ FEATURES

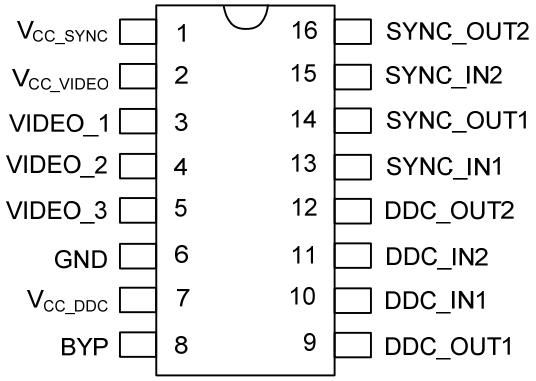
* 7 Channels of ESD protection for all VGA port connector pins meeting IEC-61000-4-2 Level 4 ESD requirements (±8kV contact discharge)
* Includes ESD protection, level-shifting, buffering and sync impedance matching
* Very low loading capacitance from ESD protection diodes on VIDEO lines (4pF maximum)
* 5V drivers for HSYNC and VSYNC lines
* Integrated impedance matching resistors on sync lines
* Bi-directional level shifting N-Channel FETs provided for DDC_CLK & DDC_DATA channels
* Backdrive protection on DDC lines

■ ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
CCVGA7C9L-R16-T	CCVGA7C9G-R16-T	SSOP-16	Tube
CCVGA7C9L-R16-R	CCVGA7C9G-R16-R	SSOP-16	Tape Reel

L8401L-R16-T (1)Packing Type (2)Package Type (3)Lead Free	(1) T: Tube, R: Tape Reel (2) R16: SSOP-16 (3) L: Lead Free, G: Halogen Free

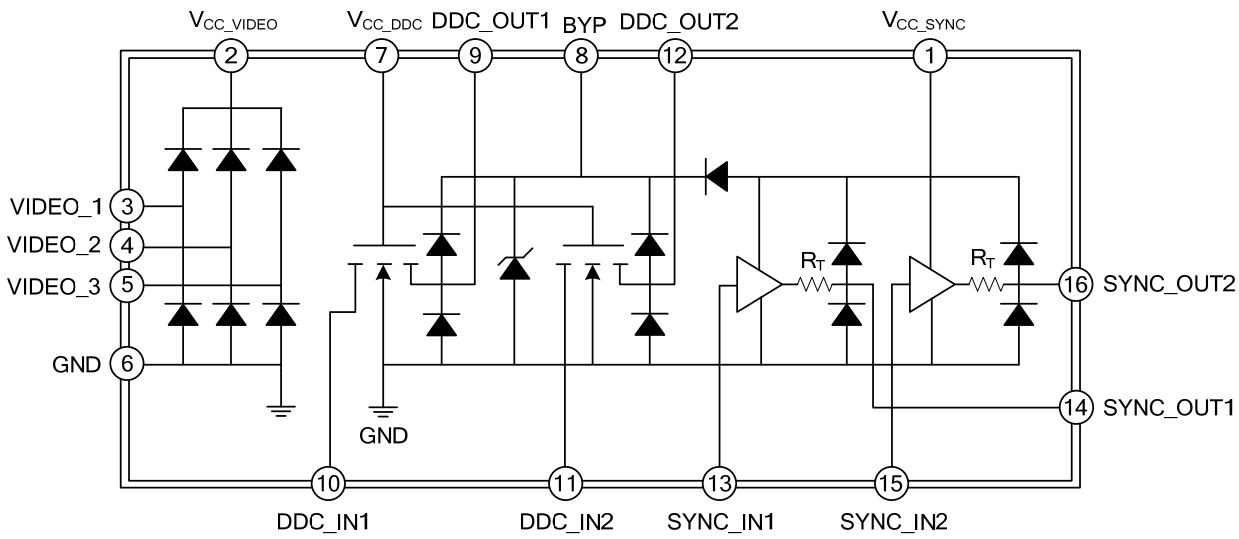
■ PIN CONFIGURATION



■ PIN DESCRIPTION

PIN NO.	PIN NAME	DESCRIPTION
1	V_{CC_SYNC}	This is an isolated supply input for the SYNC_1 and SYNC_2 level shifters and their associated ESD protection circuits.
2	V_{CC_VIDEO}	This is a supply pin specifically for the VIDEO_1, VIDEO_2 and VIDEO_3 ESD protection circuits.
3	VIDEO_1	Video signal ESD protection channel. This pin is typically tied one of the video lines between the VGA controller device and the video connector.
4	VIDEO_2	
5	VIDEO_3	
6	GND	Ground.
7	V_{CC_DDC}	This is an isolated supply input for the DDC_1 and DDC_2 level-shifting N-FET gates.
8	BYP	This input is Using a 0.2uF bypass capacitor will increase the ESD robustness of the system.
9	DDC_OUT1	DDC signal output. Connects to the video connector side of one of the sync lines
10	DDC_IN1	DDC signal input. Connects to the VGA controller side of one of the sync lines.
11	DDC_IN2	
12	DDC_OUT2	DDC signal output. Connects to the video connector side of one of the sync lines.
13	SYNC_IN1	Sync signal buffer input. Connects to the VGA controller side of one of the sync lines.
14	SYNC_OUT1	Sync signal buffer output. Connects to the video connector side of one of the sync lines.
15	SYNC_IN2	Sync signal buffer input. Connects to the VGA controller side of one of the sync lines.
16	SYNC_OUT2	Sync signal buffer output. Connects to the video connector side of one of the sync lines.

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATING

PARAMETER		SYMBOL	RATINGS	UNIT
V_{CC_VIDEO}, V_{CC_DDC} and V_{CC_SYNC} Supply Voltage Inputs		V_{CC_VIDEO}, V_{CC_DDC}, V_{CC_SYNC}	[GND-0.5]~+6.0	V
ESD Diode Forward Current (One Diode Conducting at a Time)			10	mA
DC Voltage at Inputs	VIDEO_1, VIDEO_2, VIDEO_3		[GND-0.5]~[V_{CC_VIDEO}+0.5]	V
	DDC_IN1, DDC_IN2		[GND-0.5]~6.0	V
	DDC_OUT1, DDC_OUT2		[GND-0.5]~6.0	V
	SYNC_IN1, SYNC_IN2		[GND-0.5]~[V_{CC_SYNC}+0.5]	V
Operating Temperature Range		T_{OPR}	-40~+85	°C
Storage Temperature		T_{STG}	-40~+150	°C

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ ELECTRICAL CHARACTERISTICS (Note 1)

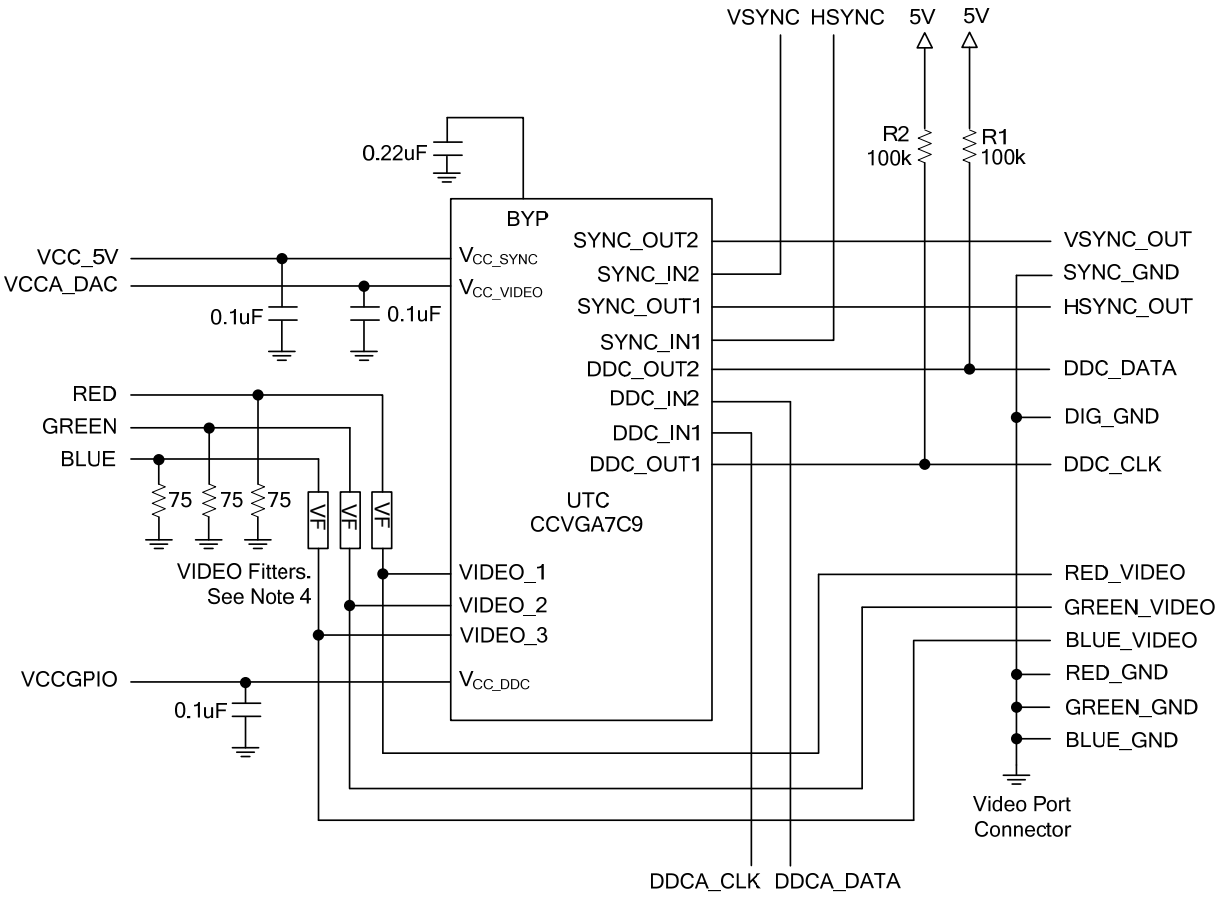
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC_VIDEO} Supply Current	I_{CC_VIDEO}	V_{CC_VIDEO}=5.0V, VIDEO Inputs at V_{CC_VIDEO} or GND			10	μA
V_{CC_DDC} Supply Current	I_{CC_DDC}	V_{CC_DDC}=5.0V			10	μA
V_{CC_SYNC} Supply Current	I_{CC_SYNC}	V_{CC_SYNC}=5V, SYNC Inputs at GND or V_{CC_SYNC}, SYNC Outputs Unloaded			50	μA
		V_{CC_SYNC}=5V, SYNC Inputs at 3.0 V, SYNC Outputs Unloaded			2.0	mA
ESD Diode Forward Voltage	V_F	I_F=10mA			1.0	V
Logic High Input Voltage	V_{IH}	V_{CC_SYNC}=5.0V, (Note 2)	2.0			V
Logic Low Input Voltage	V_{IL}	V_{CC_SYNC}=5.0V, (Note 2)			0.6	V
Logic High Output Voltage	V_{OH}	I_{OH}=0mA, V_{CC_SYNC}=5.0V, (Note 2)	4.85			V
Logic Low Output Voltage	V_{OL}	I_{OL}=0mA, V_{CC_SYNC}=5.0V, (Note 2)			0.15	V
SYNC Driver Output Resistance (CCVGA7C9−00 only)	R_{OUT}	V_{CC_SYNC}=5.0V, SYNC Inputs at GND or 3.0V		65		Ω
SYNC Driver Output Resistance (CCVGA7C9−02 only)	R_{OUT}	V_{CC_SYNC}=5.0V, SYNC Inputs at GND or 3.0V, (Note 2)		15		Ω
Logic High Output Voltage (CCVGA7C9−02 only)	V_{OH-02}	I_{OH}=24mA, V_{CC_SYNC}=5.0V, (Note 2)	2.0			V
Logic Low Output Voltage (CCVGA7C9−02 only)	V_{OL-02}	I_{OL}=24mA, V_{CC_SYNC}=5.0V, (Note 2)			0.8	V
Input Current VIDEO Inputs	I_{IN}	V_{CC_VIDEO}=5.0V, V_{IN}=V_{CC_VIDEO} or GND			±1	μA
SYNC_IN1, SYNC_IN2 Inputs		V_{CC_SYNC}=5.0V, V_{IN}=V_{CC_SYNC} or GND			±1	μA
Level Shifting N−MOSFET ”OFF” State Leakage Current	I_{OFF}	(V_{CC_DDC} - V_{DDC_IN})≤0.4V, V_{DDC_OUT}=V_{CC_DDC}			10	μA
		(V_{CC_DDC} - V_{DDC_OUT})≤0.4V, V_{DDC_IN} = V_{CC_DDC}			10	μA
Voltage Drop Across Level-Shifting N-MOSFET when “ON”	V_{ON}	V_{CC_DDC}=2.5V, V_S=GND, I_{DS}=3mA			0.18	V
VIDEO Input Capacitance (Note 3)	C_{IN_VID}	V_{CC_VIDEO}=5.0V, V_{IN}=2.5V, f=1MHz			4	pF
		V_{CC_VIDEO}=2.5V, V_{IN}=1.25V, f=1MHz			4.5	pF
SYNC Driver L => H Propagation Delay	t_{PLH}	C_L=50pF, V_{CC}=5.0V, Input tR and tF≤5ns			12	ns

■ ELECTRICAL CHARACTERISTICS(Cont.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SYNC Driver H => L Propagation Delay	t_{PHL}	C_L=50pF, V_{CC}=5.0V, Input t_R and t_F≤5ns			12	ns
SYNC Driver Output Rise & Fall Times	t_R, t_F	C_L=50pF, V_{CC}=5.0V, Input t_R and t_F≤5ns		4		ns
ESD Withstand Voltage (Note 3)	V_{ESD}	V_{CC_VIDEO}=V_{CC_SYNC}=5V	±8			kV

Notes: 1. All parameters specified over standard operating conditions unless otherwise noted.
2. These parameters apply only to the SYNC drivers. Note that R_{OUT}=R_T + R_{BUFFER}.
3. The SYNC_OUT pins on the UTC **CCVGA7C9**-02 are guaranteed for 2kV HBM ESD protection.

■ TYPICAL APPLICATION CIRCUIT



Notes:

1. The UTC **CCVGA7C9** should be placed as close to the VGA or DVI−I connector as possible.
2. The ESD protection channels VIDEO_1, VIDEO_2, VIDEO_3 may be used interchangeably between the R, G, B signals.
3. If differential video signal routing is used, the RED, BLUE, and GREEN signal lines should be terminated with external 37.5Ω resistors.
4. “VF” are external video filters for the RGB signals.
5. The DDC level shifters DDC_IN, DDC_OUT, may be used interchangeably between DDCA_CLK and DDCA_DATA.
6. The SYNC buffers may be used interchangeably between HSYNC and VSYNC.