F1C28

Datasheet

Confidential / Preliminary Documentation

Revision 1.0

Bluetooth®

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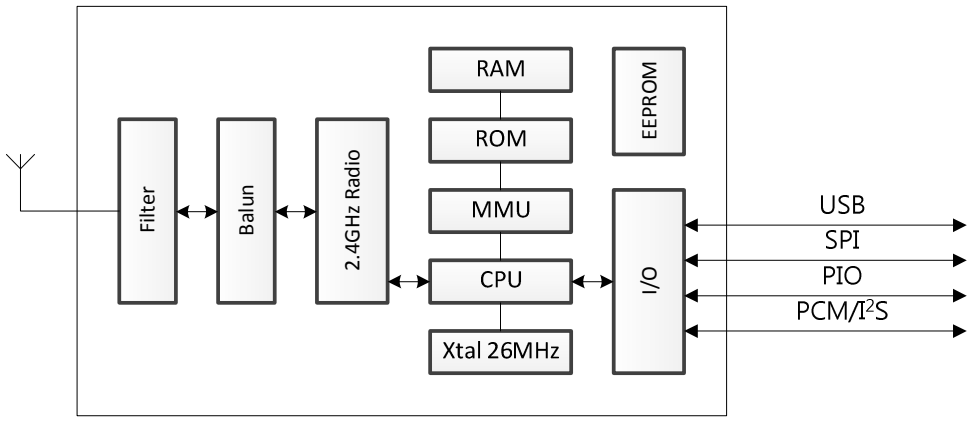
1. General

1.1 Overview

This specification covers Bluetooth module (class-2) which complies with Bluetooth specification version 4.0 and integrates RF & Baseband controller in small package. This Module has adopted CSR's CSR8510 ROM WLCSP chipset.

All detailed specification including pinouts and electrical specification may be changed without notice.



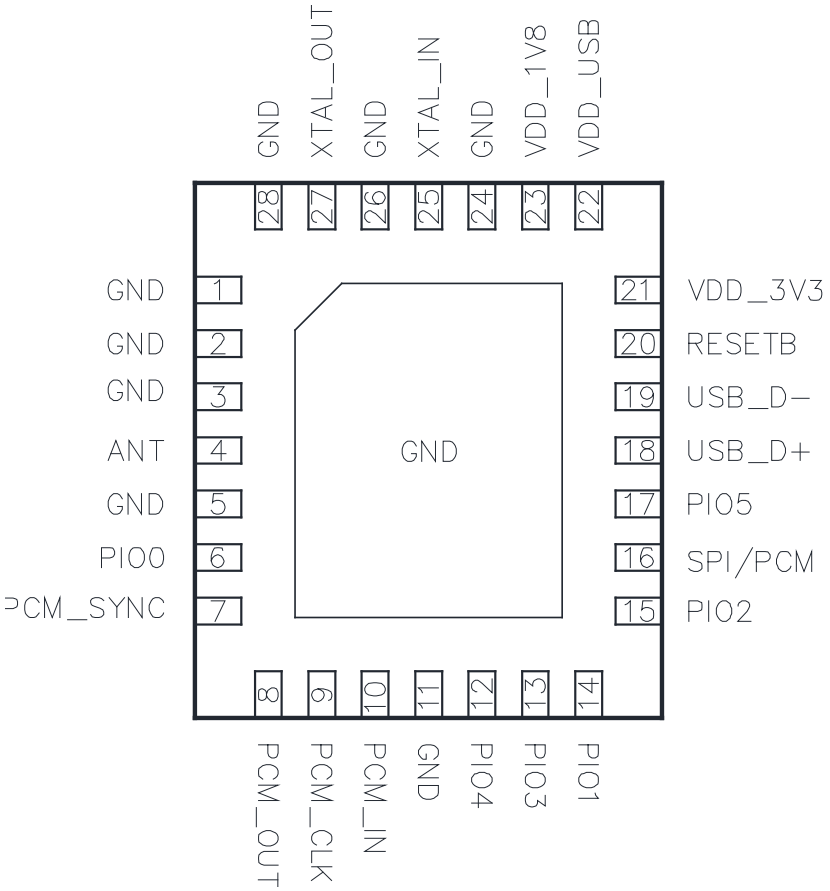
1.2 Features

- Fully Qualified Bluetooth v4.0 specification system
- Dual-mode Bluetooth / Bluetooth low energy
- Draft Bluetooth low energy HID boot mode support
- Enhanced Data Rate (EDR) compliant with v2.1.E.2 of specification for both 2Mbps and 3Mbps modulation modes
- Full-speed Bluetooth Operation with Full Piconet Support and Scatternet Support
- Scatternet Support
- Low Power selectable 1.8 to 3.6V I/O
- No External regulators required for USB supply operation
- Full-Speed (12Mbps) USB 2.0 interface
- PCM/I²S digital audio interface
- Support for IEEE802.11 Co-existence
- Bluetooth low energy
- On Module SBC Encoding
- RoHS Compliant
- Integrated transcoders for A-law, u-law and linear PCM
- Standard HCI USB support
- Integrated 16Kbit EEPROM(Option)
- Integrated 26MHz reference clock
- Operating temperature range (-30℃ ~ +85℃)
- Supply voltage Range (1.8V ~ 5.75V)
- Competitive Size (6mm x 7mm x 1.5mm : QFN 36Pin)

1.3 Application

- Notebooks and Desktop
- TV Set-top boxes
- USB Bluetooth Dongles
- Bluetooth low energy
- Bluetooth designs requiring the USB interface and an HCI interface

1.4 Pinout Diagram

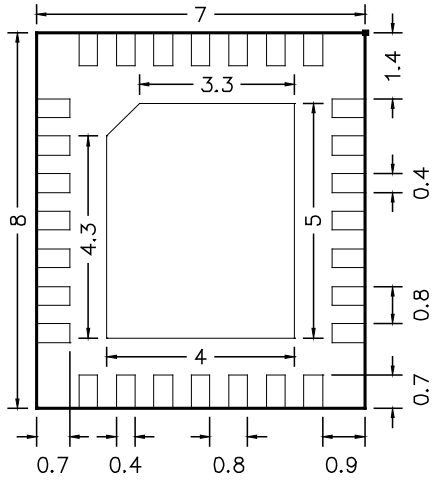


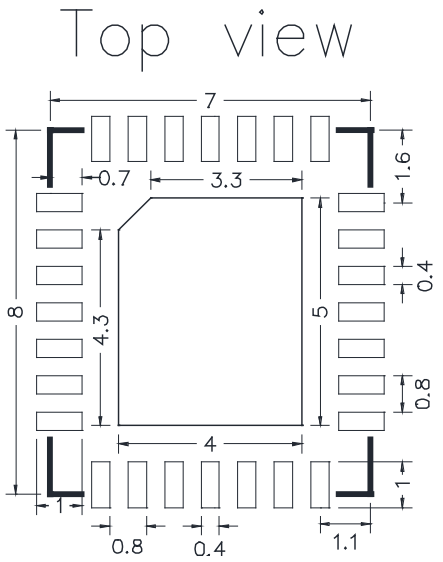
Top View

1.5 Device Terminal Descriptions

	PIN	Name	Description
PCM/SPI	PCM_OUT/SPI_MISO	8	PCM1 Synchronous data output / SPI data output
	PCM_IN/SPI_MOSI	10	PCM1 Synchronous data input / SPI data input
	PCM_CLK/SPI_CLK	9	PCM1 Synchronous data clock / SPI clock
	PCM_SYNC/SPI_CSB	7	PCM1 Synchronous data sync / SPI chip select, active low
USB	USB -	19	USB -
	USB +	18	USB + with selectable internal 1.5k pull-up resistor
PIO	PIO0	6	Programmable input/output line PIO 3,4 Can be used to form I2C interface(Option)
	PIO1	14	
	PIO2	15	
	PIO3	13	
	PIO4	12	
	PIO5	17	
Other Pins	ANT	4	RF Connection to Antenna
	GND	1,2,3,5,11,24,26,28	Ground
	VDD_USB	22	Input to USB Regulator. Connect to external USB bus supply.
	VDD_3V3	21	D.C input voltage for operation (3.0~3.3V)
	VDD_1V8	23	Output from internal high-voltage to 1.8V regulator.
	SPI/PCM#	16	High : SPI Mode , Low : PCM(PIO) Mode
	RESETB	20	Reset if low.
	X-Tal_IN	25	External Clock In(Option). Typical NC
	X-Tal_OUT	27	External Clock Out(Option). Typical NC

1.6 Module Dimension & Land Pattern





Land Pattern

2. Characteristics

2.1 Electrical Characteristics

Absolute Maximum Ratings		
Rating	Minimum	Maximum
Storage temperature	-40°C	85°C
VDD_USB	3.0V	5.75V
VDD_3V3	3.0V	4.8V
VDD_1V8	1.7V	1.95V

Recommended Operating Temperature Conditions		
Operating Condition	Minimum	Maximum
Operating temperature range	-30°C	85°C

Recommended Operating Conditions		
Operating Condition	Typical	
VDD_USB	5V	IN
VDD_3V3	3.3V	IN / OUT
VDD_1V8	1.8V	IN / OUT

2.2 RF Characteristics

Transmitter

Specification	Condition	Min	Typ	Max	Unit
Output transmit power	Normal	-6	1	4	dBm
Transmit power density	Normal			4	dBm
Transmit power control	Normal	2		8	dBm
Frequency Range	Normal	2400		2483.5	MHz
20dB bandwidth for modulated carrier	Normal		900	1000	KHz
Adjacent channel transmit power	±2MHz ±3MHz ±4MHz			-20 -40 -40	dBm
Modulation Characteristics	f1avg f2max f2avg / f1avg	140 115		175 80	KHz KHz %
Initial carrier frequency tolerance	Normal	-20		20	KHz
Carrier frequency Drift	One slot packet(DH1) Three slot packet(DH3) Five slot packet(DH5)	-25 -40 -40		25 40 40	KHz

Transceiver

Specification	Condition	Min	Typ	Max	Unit
Adjacent channel transmit power	30MHz ~ 1GHz 1GHz ~12.75GHz 1.8GHz ~5.1GHz 5.1GHz ~5.3GHz			-36 -30 -47 -47	dBm

Receiver

Specification	Condition	Min	Typ	Max	Unit
Sensitivity level (0.1% BER)	Single slot packets	-70	-80		dBm
Transmit power density	Multi slot packet	-70	-80		dBm
C/I performance	co-channel 1MHz (Adjacent channel) 2MHz (2nd Adjacent channel) 3MHz (3rd Adjacent channel)			11 0 -30 -40	dB
Blocking performance	30MHz ~ 2000MHz 2000MHz ~ 2400MHz 2500MHz ~ 3000MHz 3000MHz ~ 12.75GHz	-10 -27 -27 -10			dBm
Intermodulation performance	n=5	-39			dBm
Maximum input level		-20	-10		dBm

3. Terminal Interface Description

Host Interface only USB

3.1 WLAN Coexistence Interface

Dedicated hardware is provided to implement a variety of WLAN coexistence schemes. There is support for:

- Channel skipping AFH
- Priority signaling
- Channel signaling
- Host passing of channel instructions

The CSR8510 WLCSP supports the WLAN coexistence schemes:

- Unity-3
- Unity-3e
- Unity+

For more information see Bluetooth and IEEE 802.11 b/g Co-existence Solutions Overview.

3.2 USB

F1C28 Bluetooth Module has a full-speed (12Mbps) USB interface for communicating with other compatible digital devices. The USB interface on the F1Q28 Bluetooth Module acts as a USB peripheral, responding to requests from a master host controller.

F1Q28 Bluetooth Module supports the Universal Serial Bus Specification,

Revision v2.0 (USB v2.0 Specification), available from http://www.usb.org.

For more information on how to integrate the USB interface on CSR8310 QFN see the Bluetooth and USB Design Considerations Application Note .

As well as describing USB basics and architecture, the application note describes:

- Power distribution for high and low bus-powered configurations
- Power distribution for self-powered configuration, which includes USB VBUS monitoring
- USB enumeration
- Electrical design guidelines for the power supply and data lines, as well as PCB tracks and the effects of ferrite beads
- USB suspend modes and Bluetooth low-power modes:
  - Global suspend
  - Selective suspend, includes remote wake
  - Wake on Bluetooth, includes permitted devices and set-up prior to selective suspend
  - Suspend mode current draw

■ PIO status in suspend mode

■ Resume, detach and wake PIOs

■ Battery charging from USB, which describes dead battery provision, charge currents, charging in suspend modes and USB VBUS voltage consideration

■ USB termination when interface is not in use

■ Internal modules, certification and non-specification compliant operation

3.3 I²C

EEPROM operation is not applicable to parts in UART mode.

F1Q28 Bluetooth Module uses an Internal I²C EEPROM (16Kb) to store device specific configuration information (PS-Keys) such as Bluetooth address and USB descriptors.

EEPROM I²C Interface

EEPROM	F1C28	Description
SCL	PIO[3]	I²C Clock
SDA	PIO[4]	I²C Data
WP	NC	Write protect. Not driven by the CSR 8510 WLCSP. The Line the EEPROM WP Line active on PCB.

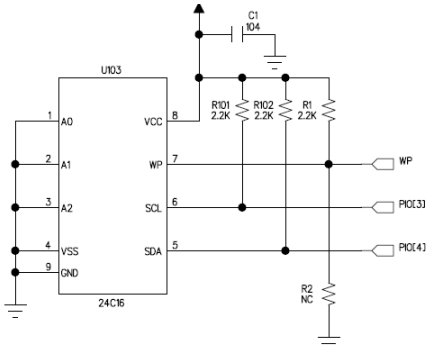
3.3.1 External EEPROM

Follow the I²C standard timing recommendations regarding correct pull-up and I²C bus data-line capacitance limits.

By default, the EEPROM is accessed at I²C standard (100kHz or below) rate, and switch able to fast 400kHz mode by PS Key if the EEPROM supports fast I²C.

CSR recommends 400kHz capable EEPROM in these applications to ensure the USB bus power mode boot timing specifications are met.

Alternatively, download the PS Keys from the USB host. This requires a 26MHz crystal operation, which enables the USB host interface to function using the default PS Key configuration. The host must then supply all required PS Key information.



3.4 Audio Interface

SPI/PCM# Selection (Pin 16 Selection)

SPI Interface : 3V3 10Kohm Full Up

PCM Interface : GND 10Kohm Full Down

F1C28 Bluetooth Module has a digital audio interface that can be configured as a PCM or I²S support.

3.4.1 PCM Configuration

Pulse Code Modulation (PCM) is a standard method used to digitize audio (particularly voice) patterns for transmission over digital communication channels. Through its PCM interface, this module has hardware support for continual transmission and reception of PCM data, so reducing processor overhead for wireless headset applications. This module offers a bi-directional digital audio interface that route directly into the baseband layer of the on-chip firmware. It dose not pass through the HCI protocol layer.

Hardware allows the data to be sent to and received from a SCO connection. This module interfaces directly to PCM audio devices including the following:

- Qualcomm MSM 3000 series and MSM 5000 series CDMA baseband devices
- OKI MSM7705 for channel A-law and u-law CODEC
- Motorola MC145481 8-bit A-law and u-law CODEC
- Motorola MC145483 13-bit linear CODEC
- STW 5093 and 5094 14-bit linear CODECs

F1Q28 has a digital audio interface that can be configured as a PCM port.

The audio PCM interface on the F1Q28 supports:

■ Continuous transmission and reception of PCM encoded audio data over Bluetooth.

■ Processor overhead reduction through hardware support for continual transmission and reception of PCM data

■ A bidirectional digital audio interface that routes directly into the baseband layer of the firmware. It does not pass through the HCI protocol layer.

■ Hardware on the F1Q28 for sending data to and from a SCO connection.

■ Up to 3 SCO connections on the PCM interface at any one time.

■ PCM interface master, generating PCM_SYNC and PCM_CLK.

■ PCM interface slave, accepting externally generated PCM_SYNC and PCM_CLK.

■ Various clock formats including:

■ Long Frame Sync

■ Short Frame Sync

■ GCI timing environments

■ 13-bit or 16-bit linear, 8-bit μ-law or A-law commanded sample formats.

■ Receives and transmits on any selection of 3 of the first 4 slots following PCM_SYNC.

The PCM configuration options are enabled by setting the PS Key PSKEY_PCM_CONFIG32.

The PCM configuration is set using two PS keys, PSKEY_PCM_CONFIG32. and PSKEY_PCM_LOW_JITTER_CONFIG. The default for long frame sync and interface master generating 256KHz PCM_CLK with no tri-state of PCM_OUT.

Parameter	Possible value
Mode	Slave, Master
Clock rate	Master Mode : 128,256,512,1536,2400 KHz Slave Mode : up to 2400 KHz
Sync formats	Long frame sync, Short frame sync
Data formats	13 or 16bit linear, 8-bit A-law to u-law

3.4.2 I²S Configuration

The digital audio interface supports the industry standard formats for I²S, left-justified or right-justified.

The interface shares the same pins as the PCM interface, which means each audio bus is mutually exclusive in its usage.

PCM Interface	I²S Interface
PCM_OUT	SD_OUT
PCM_IN	SD_IN
PCM_SYNC	WS
PCM_CLK	SCK

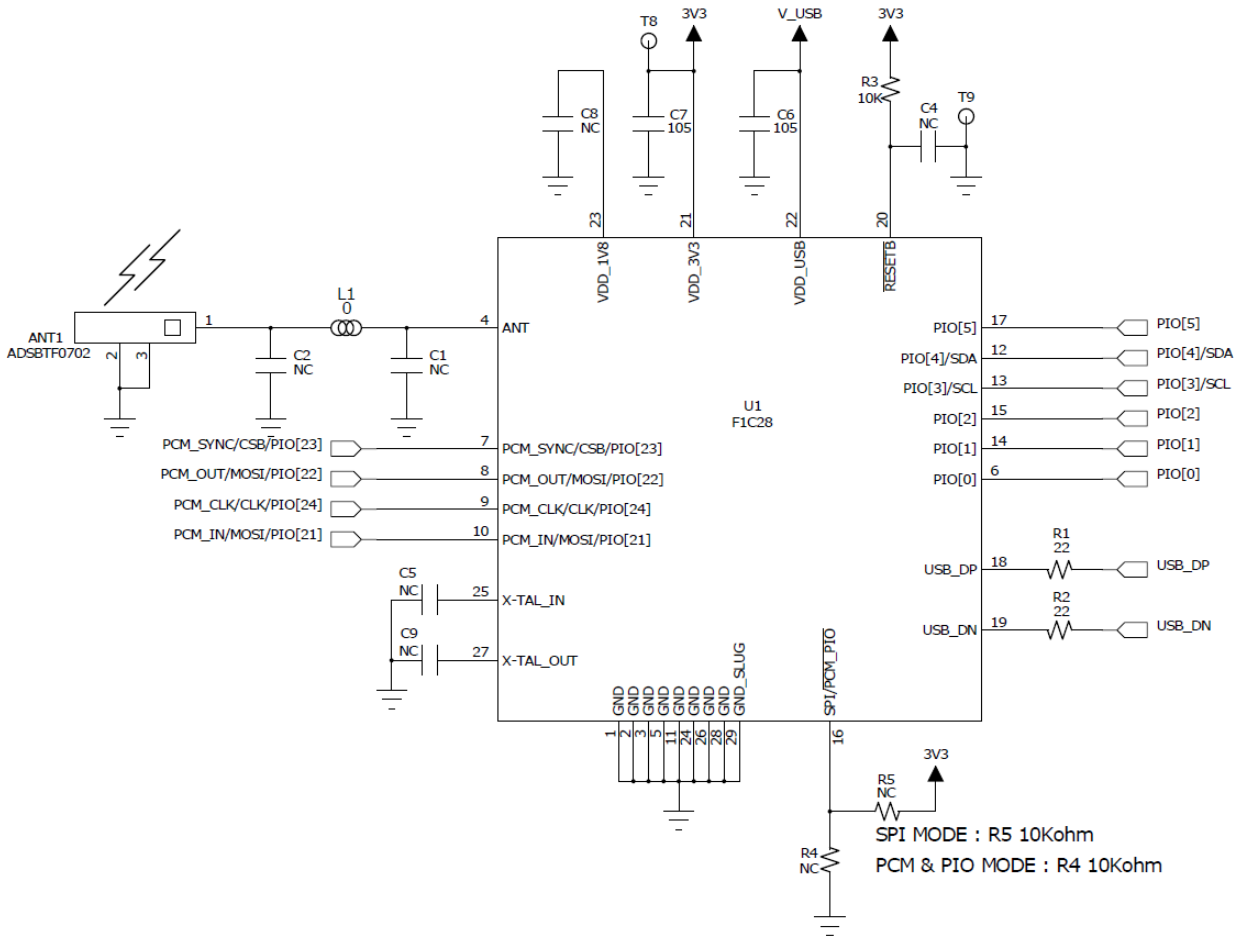
Configure the digital audio interface using PSKEY_DIGITAL_AUDIO_CONFIG, see the PS Key file.

3.5 Digital Pin State On Reset

Pin Name / Group	I/O Type	No Core Supply Reset	Full Chip Reset
VREG_EN_RST#	Digital input	Strong pull-down	N/A
SPI_CLK / PCM_CLK	Digital bidirectional tri-stated	Weak pull-down	Weak pull-down
SPI_CS# / PCM_SYNC	Digital bidirectional tri-stated	Weak pull-up (SPI) Weak pull-down (PCM)	Weak pull-up (SPI) Weak pull-down (PCM /PIO)
SPI_MISO / PCM_OUT	Digital output tri-stated	Weak pull-down	Weak pull-down
SPI_MOSI / PCM_IN	Digital input	Weak pull-down	Weak pull-down
PIO[5:0]	Digital bidirectional tri-stated	Weak pull-down	Weak pull-down

4. Application Schematic

F1C28_Rev01_Application.pdf F1C28_Rev01_Application.sch



5. Revision History

Revision	Date	Change Descriptions	Issued by
Rev 1.0	2011.12.29	Initial Release	J.M.KWON