ABOV SEMICONDUCTOR
8-BIT SINGLE-CHIP MICROCONTROLLERS

MC80F0304/0308/0316
MC80C0304/0308/0316

User's Manual (Ver. 2.12)

ABOV
SEMICONDUCTOR

Version 2.12

Published by
FAE Team

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REVISION HISTORY

VERSION 2.12 (November 4, 2011) This Book

Logo is changed.

The dimensions of 28 SOP package outline drawing is fixed.

VERSION 2.11 (May 14, 2008)

Corrected Stack End Address to 0100_H at Figure 8-4 on page 34.

Corrected the address of PU2 to $00FE_H$ at Figure 8-1 on page 38.

Corrected the bit name of TM1to T1CK1,T1CK0,T1CN and T1ST at Figure 13-17 on page 75.

Corrected the PWM1HR to T1PWHR at Figure 13-20 on page 77.

Corrected the initial value of WDT Timer to “Enable” at Figure 20-1 on page 110.

VERSION 2.10 (April 4, 2008)

Updated the description for Figure 14-4 A/D Converter Control & Result Register on page 80.

The format of Instruction Set and Revision History was renewed.

Fixed some errata.

VERSION 2.02 (SEP 28, 2007) This book

Fix error in description and diagram of 8 bit event counter.

VERSION 2.01 (MAY 5, 2007)

Fix error in figure 9-2 : change R04, R07 and EC0,EC1 of PSR1 to R05, R06 and T0O, T2O (page 38)
Fix pin number error of 28 pin package in Table 5-2. (page 9)

VERSION 2.0 (MAR. 2007)

Add T_{VDD} parameter specification and change T_{POR} in DC Electrical Characteristics.
Note for configuration option is added and fix some errata.

VERSION 1.92 (JAN. 2007)

Mask Order Sheet is updated

VERSION 1.91 (NOV. 2006)

Fix some errata in Section 13.6 PWM mode.

VERSION 1.9 (SEP. 2006)

Add 32 SOP package type.

VERSION 1.81 (AUG. 2006)

Fix some errata in Figure 18-2 and Figure 18-3.

VERSION 1.8 (JUL. 2006)

Correct Interrupts Sequence and example codes in Chapter 18.
Mask Order Sheet is updated

Delete chapter 15.3.
Fix some errata.

VERSION 1.7 (JUN. 2006)

Correct the description of TM1 in Figure13-1.
$f_{XIN}/2$, $f_{XIN}/8$ and timer0 clock instead of $f_{XIN}/4$, $f_{XIN}/16$ and timer2 clock are selected when T1CK[1..0] is “01b”, “10b”, “11b” respectively.

VERSION 1.6 (MAY.2006)

Update notification in Chapter 26.3 Hardware Conditions to Enter the ISP Mode. (Condition to enter ISP in case of using RESET pin as input pin)
Correct the schematic of ISP configuration and Reference ISP Board circuit.
Add chapters about sequence to enter ISP/User mode and ACK mode and update chapters 26.3 to chapter 26.6
Fix some font error in chapter 25. Emulator Board Setting.

VERSION 1.5 (APR. 2006)

Update Typical Characteristics

VERSION 1.4 (APR. 2006)

Correct SIO Block diagram, Timing and usage.

VERSION 1.3 (MAR. 2006)

The company name, MagnaChip Semiconductor Ltd. changed to ABOV Semiconductor Co.,Ltd..

Add 28 SOP package type.

VERSION 1.2 (OCT. 2005)

Add notification that the DAA, DAS decimal adjust instructions are not supported.

VERSION 1.1 (JUN. 2005)

Add Pb free package

VERSION 1.0 (MAY. 2005)

Fix some errata.

VERSION 0.1 (MAR. 2005)

First Edition.

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MC80F0304/0308/0316
MC80C0304/0308/0316

CMOS SINGLE-CHIP 8-BIT MICROCONTROLLER WITH 10-BIT A/D CONVERTER AND UART

1. OVERVIEW

1.1 Description

The MC80F0304/0308/0316 is advanced CMOS 8-bit microcontroller with 4K/8K/16K bytes of FLASH. This is a powerful microcontroller which provides a highly flexible and cost effective solution to many embedded control applications. This provides the following features : 4K/8K/16K bytes of FLASH, 512 bytes of RAM, 8/16-bit timer/counter, watchdog timer, 10-bit A/D converter, 8-bit Serial Input/Output, UART, buzzer driving port, 10-bit PWM output and on-chip oscillator and clock circuitry. It also has ONP, noise filter, PFD for improving noise immunity. In addition, the MC80F0304/0308/0316 supports power saving modes to reduce power consumption.

This document **explaines the base MC80F0316**, the other's eliminated functions are same as below table.

Device Name		FLASH Size	RAM	ADC	I/O PORT	Package
FLASH	MASK ROM					
MC80F0304B/08B/16B	MC80C0304B/08B/16B	4K/8K/16K	512B	16 channel	30 port	32 PDIP
MC80F0304D32/ 08D32/16D32	MC80C0304D32/ 08D32/16D32				30 port	32 SOP
MC80F0304G/08G/16G	MC80C0304G/08G/16G				26 port	28 SKDIP
MC80F0304D/08D/16D	MC80C0304D/08D/16D				26 port	28 SOP

1.2 Features

- **4K/8K/16K Bytes On-chip ROM**
- **FLASH Memory**
  - Endurance : 1000 cycles
  - Data retention time : 10 years
- **512 Bytes On-chip Data RAM**
  (Included stack memory)
- **Minimum Instruction Execution Time:**
  - 333ns at 12MHz (NOP instruction)
- **Programmable I/O pins**
  (LED direct driving can be a source and sink)
  - MC80F0316B : 30(29)
  - MC80F0316D32 : 30(29)
  - MC80F0316G : 26(25)
  - MC80F0316D : 26(25)
- **One 8-bit Basic Interval Timer**
- **Four 8-bit Timer/counters**
  (or two 16-bit Timer/counter)
- **One Watchdog timer**
- **Two 10-bit High Speed PWM Outputs**
- **10-bit A/D converter : 16 channels**
- **Two 8-bit Serial Communication Interface**
  - One Serial I/O and one UART
- **One Buzzer Driving port**
  - 488Hz ~ 250kHz@4MHz
- **Four External Interrupt input ports**
- **On-chip POR (Power on Reset)**
- **Thirteen Interrupt sources**
  - External input : 4
  - Timer : 6
  - A/D Conversion : 1
  - Serial Interface : 1
  - UART : 1
- **Built in Noise Immunity Circuit**
  - Noise filter
  - PFD (Power fail detector)
  - ONP (Oscillation Noise Protector)
- **Power Down Mode**
  - Stop mode
  - Sleep mode
  - RC-WDT mode
- **Operating Voltage & Frequency**

- 2.7V ~ 5.5V (at 1 ~ 8MHz) : FLASH
- 2.0V ~ 5.5V (at 1 ~ 4.2MHz) : MASK
- 4.5V ~ 5.5V (at 1 ~ 12MHz) : FLASH,MASK

- **Operating Temperature : -40°C ~ 85°C**
- **Oscillator Type**
  - Crystal
  - Ceramic resonator
  - External RC Oscillator (C can be omitted)
  - Internal Oscillator (4MHz/2MHz)
- **Package**
  - 28SKDIP, 28SOP, 32PDIP
  - Avalilable Pb free package

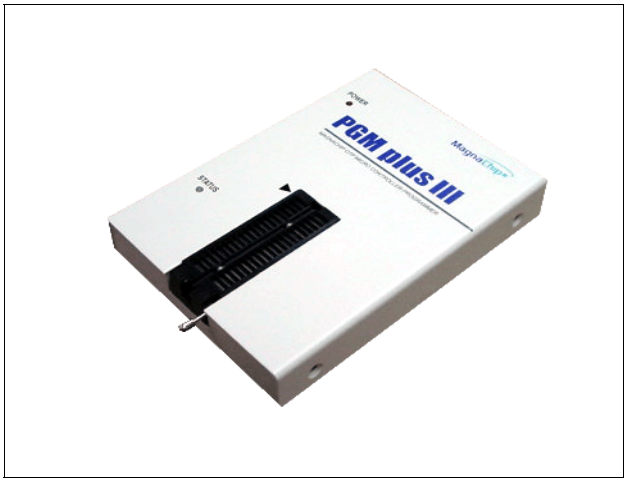
1.3 Development Tools

The MC80F0304/0308/0316 is supported by a full-featured macro assembler, an in-circuit emulator CHOICE-Dr.™ and OTP programmers. There are two different type of programmers such as single type and gang type. Macro assembler operates under the MS-Windows 95 and upversioned Windows OS.

Please contact sales part of ABOV semiconductor.

Software	- MS-Windows based assembler - MS-Windows based Debugger - HMS800 C compiler
Hardware (Emulator)	- CHOICE-Dr. - CHOICE-Dr. EVA80C0x B/D
FLASH Writer	- CHOICE - SIGMA I/II (Single writer) - PGM Plus III (Single writer) - Standalone GANG4 I/II (Gang writer)

Choice-Dr. (Emulator)



PGMplus III (Single Writer)

Standalone Gang4 II (Gang Writer)

1.4 Ordering Information

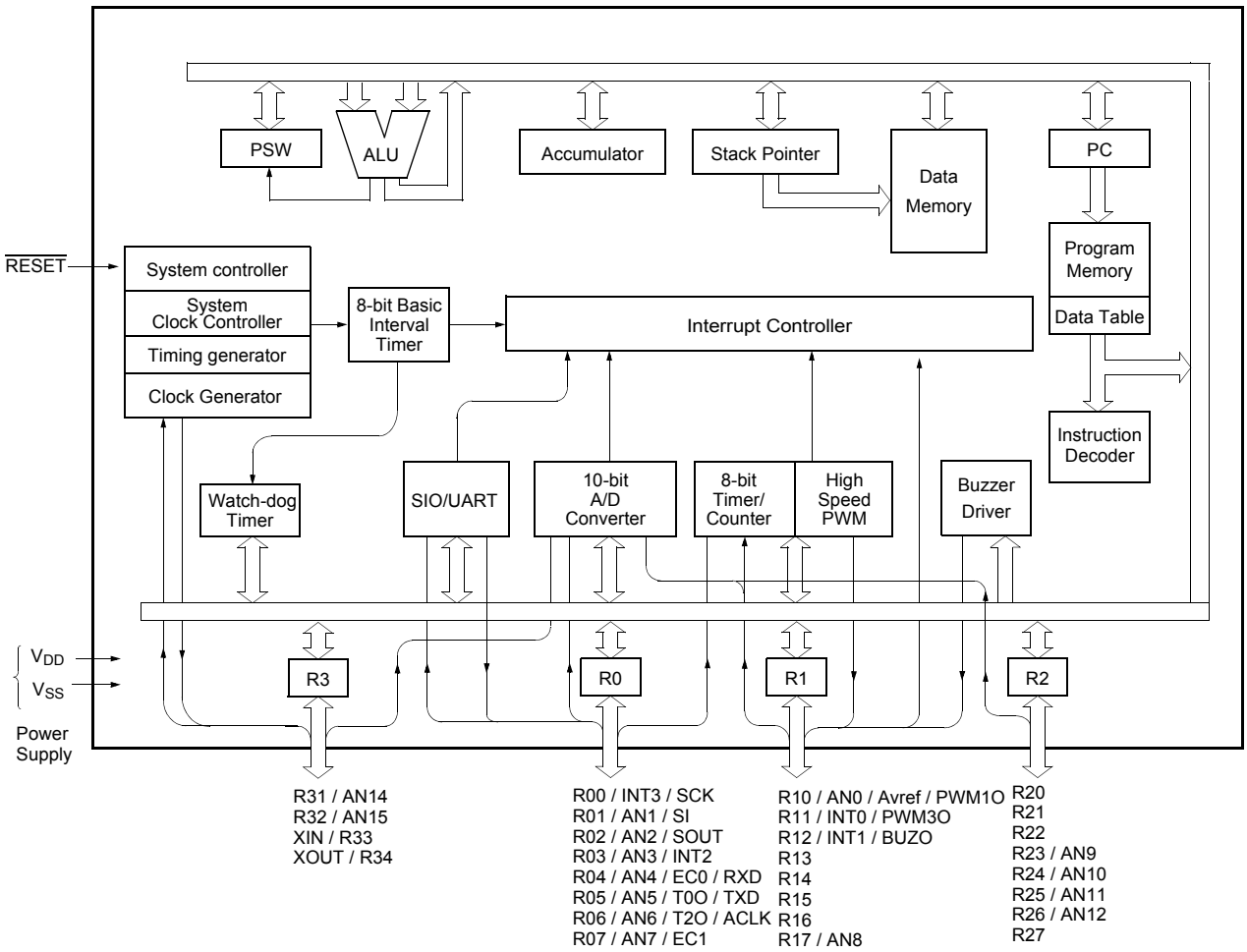
	Device name	MASK ROM	FLASH ROM	RAM	Package
MASK version	MC80C0316B MC80C0316D32 MC80C0316G MC80C0316D	16K bytes 16K bytes 16K bytes 16K bytes	-	512bytes	32PDIP 32SOP 28SKDIP 28SOP
	MC80C0308B MC80C0308D32 MC80C0308G MC80C0308D	8K bytes 8K bytes 8K bytes 8K bytes		512bytes	32PDIP 32SOP 28SKDIP 28SOP
	MC80C0304B MC80C0304D32 MC80C0404G MC80C0304D	4K bytes 4K bytes 4K bytes 4K bytes		512bytes	32PDIP 32SOP 28SKDIP 28SOP
FLASH version	MC80F0316B MC80F0316D32 MC80F0316G MC80F0316D	-	16K bytes 16K bytes 16K bytes 16K bytes	512bytes	32PDIP 32SOP 28SKDIP 28SOP
	MC80F0308B MC80F0308D32 MC80F0308G MC80F0308D		8K bytes 8K bytes 8K bytes 8K bytes	512bytes	32PDIP 32SOP 28SKDIP 28SOP
	MC80F0304B MC80F0304D32 MC80F0304G MC80F0304D		4K bytes 4K bytes 4K bytes 4K bytes	512bytes	32PDIP 32SOP 28SKDIP 28SOP

Pb free package:

The “P” Suffix will be added at the original part number.

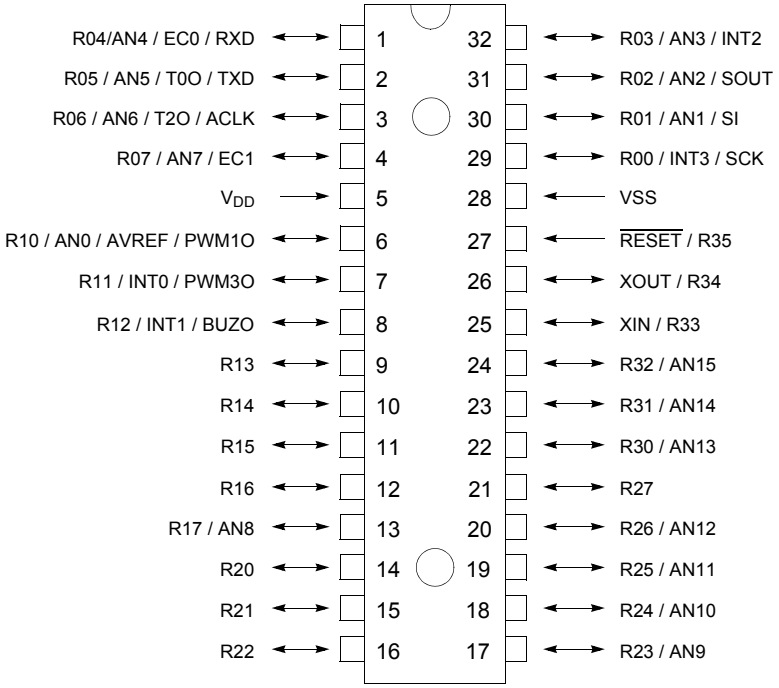
For example; MC80F0316G(Normal package), MC80F0316G P(Pb free package)

2. BLOCK DIAGRAM

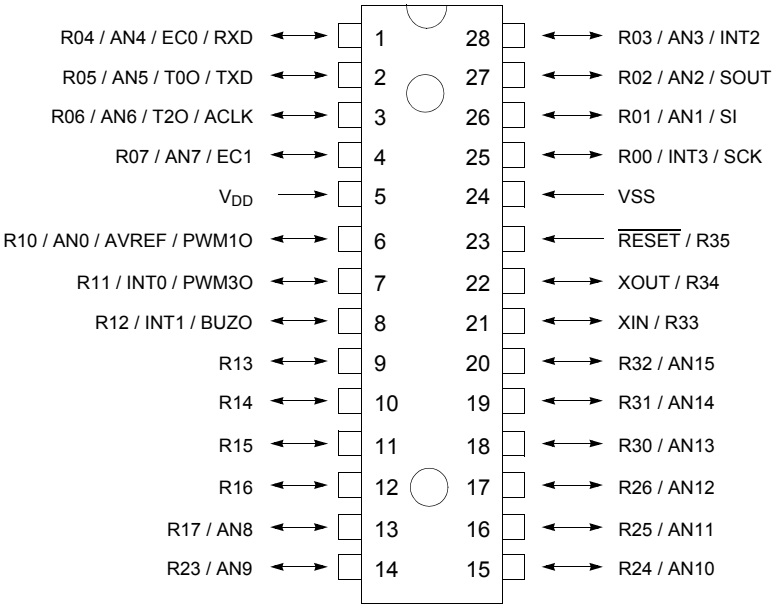


3. PIN ASSIGNMENT

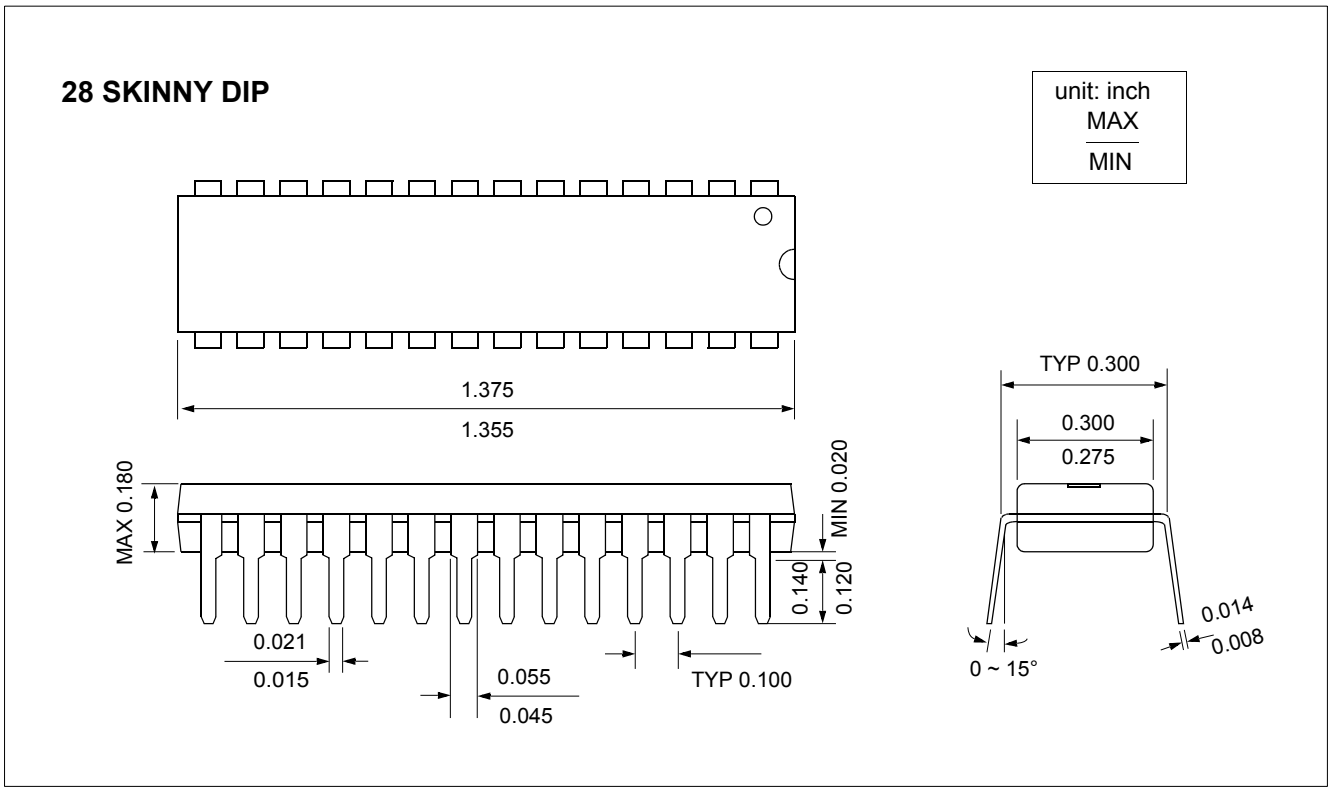
32PDIP



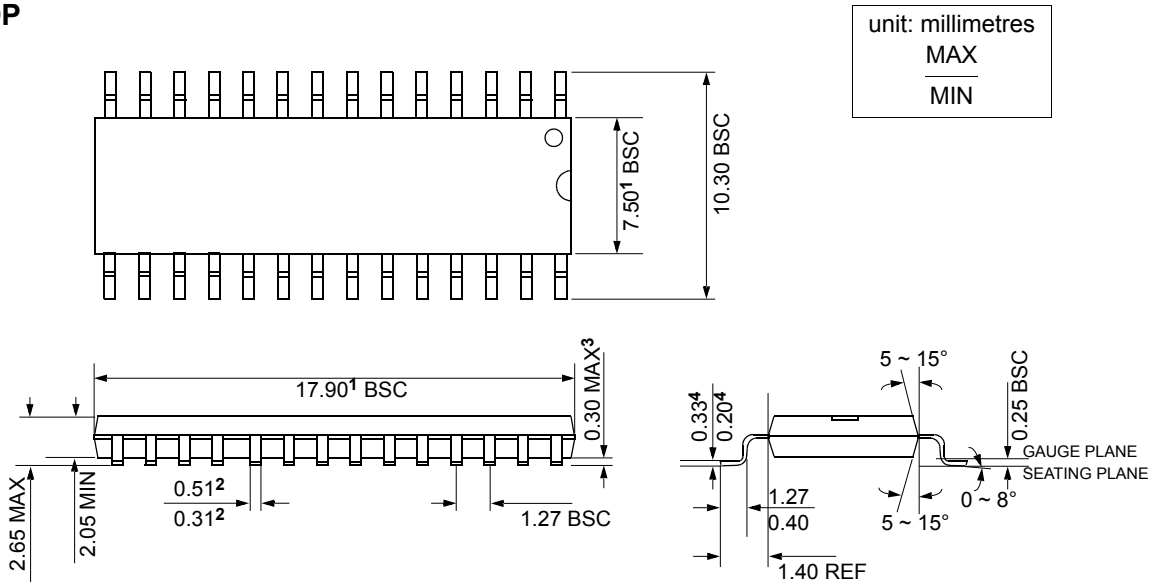
28 SKDIP/ SOP



4. PACKAGE DRAWING



28 SOP



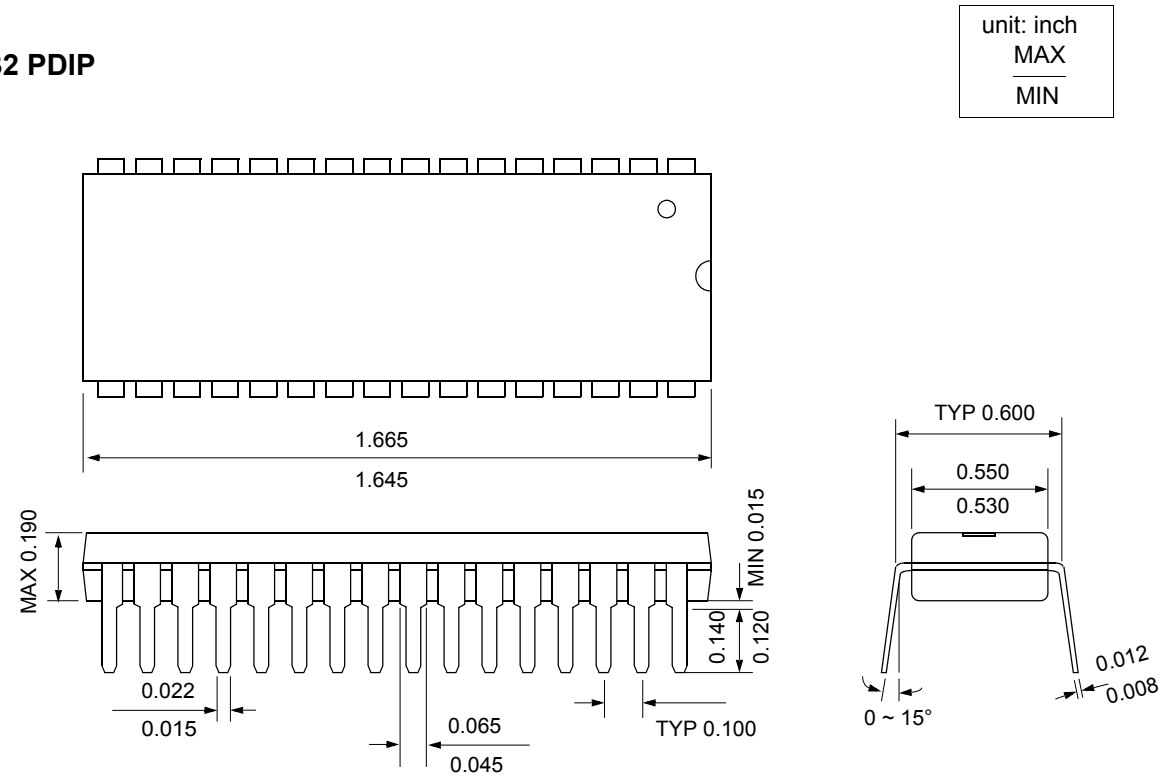
1. 17.90 dimension does not include mold FLASH, protrusions or gate burrs.
   Mold FLASH, protrusions or gate burrs shall not exceed 0.15mm per end.
   7.50 dimension does not include interlead FLASH or protrusion.
   Interlead FLASH or protrusion shall not exceed 0.25mm per side.
   The package top may be smaller than the package bottom.
   17.90 and 7.50 dimensions are determined at the outermost extremes of the plastic body exclusive of mold FLASH.
   Tie bar burrs, gate burrs and interlead FLASH, but including any mismatch between the top and bottom of the plastic body.

2. This dimensions apply to the flat section of the lead between 0.10 to 0.25 mm from the lead tip.
   Dimension does not include dambar protrusion.
   Allowable dambar protrusion shall be 0.10 mm total in excess of the dimension maximum material condition.
   The dambar may not be located on the lower radius of the foot.

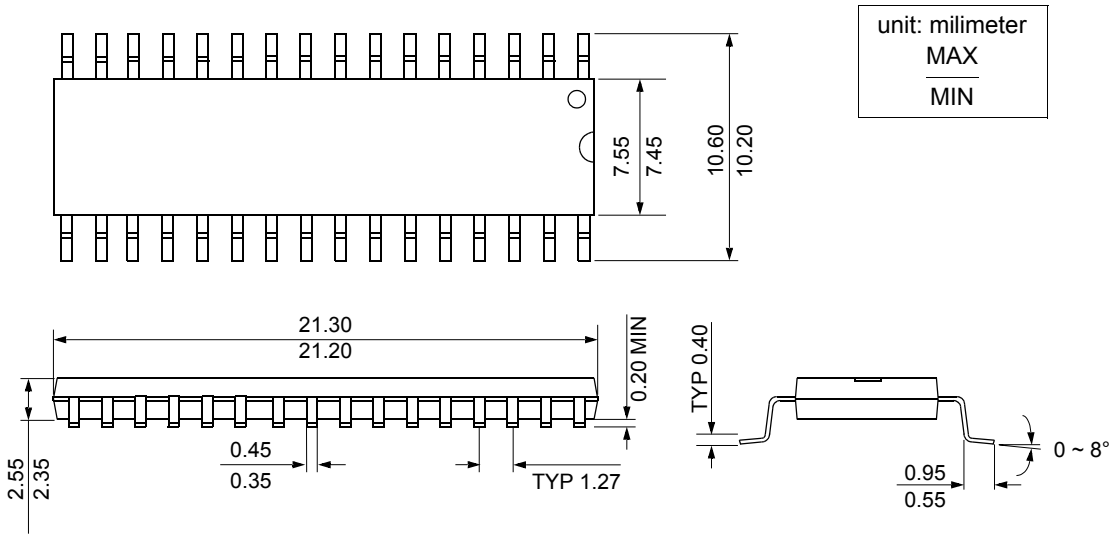
3. This is defined as the vertical distance from the seating plane to the lowers point on the package body excluding the thermal enhancemet on cavity down package configurations.

4. This dimensions apply to the flat section of the lead between 0.10 to 0.25 mm from the lead tip.

32 PDIP


unit: inch
MAX
MIN
1.665
1.645
MAX 0.190
MIN 0.015
0.140
0.120
0.022
0.015
0.065
0.045
TYP 0.100
TYP 0.600
0.550
0.530
0.012
0.008
0 ~ 15°

32 SOP

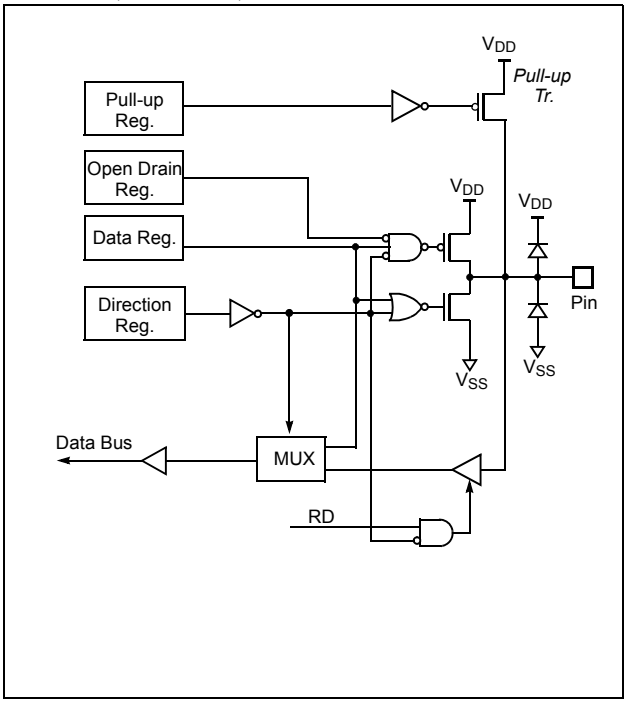

unit: milimeter
MAX
MIN
7.55
7.45
10.60
10.20
21.30
21.20
0.20 MIN
TYP 0.40
2.55
2.35
0.45
0.35
TYP 1.27
0.95
0.55
0 ~ 8°

PIN NAME	Pin No.		In/Out	Function			
	32	28		First	Second	Third	Forth
V_{DD}	5	5	-	Supply voltage			
V_{SS}	28	24	-	Circuit ground			
$\overline{RESET}$ (R35)	27	23	I	Reset signal input	Input only port	-	-
X_{IN} (R33)	25	21	I	Oscillation Input	Normal I/O Port	-	-
X_{OUT} (R34)	26	22	O	Oscillation Output	Normal I/O Port	-	-
R00 (INT3/SCK)	29	25	I/O	Normal I/O Ports	External Interrupt 3	SPI clock Input	-
R01 (AN1/SI)	30	26	I/O		Analog Input Port 1	SPI Data Input	-
R02 (AN2/SOUT)	31	27	I/O		Analog Input Port 2	SPI Data Output	-
R03 (AN3/INT2)	32	28	I/O		Analog Input Port 3	External Interrupt2	-
R04 (AN4/EC0/RXD)	1	1	I/O		Analog Input Port 4	Event Counter	UART RX
R05 (AN5/T0O/TXD)	2	2	I/O		Analog Input Port 5	Timer0 Output	UART TX
R06 (AN6/T2O/ACLK)	3	3	I/O		Analog Input Port 6	Timer2 Output	UART Clock
R07 (AN7/EC1)	4	4	I/O		Analog Input Port 7	Event Counter	-
R10 (AN0/AVref/PWM1O)	6	6	I/O		Analog Input Port 0	Analog Reference	PWM 1 output
R11 (INT0/PWM3O)	7	7	I/O		External Interrupt 0	PWM 3 output	-
R12 (INT1/BUZO)	8	8	I/O		External Interrupt 1	Buzzer Driving Output	-
R13	9	9	I/O		-	-	-
R14	10	10	I/O		-	-	-
R15	11	11	I/O		-	-	-
R16	12	12	I/O		-	-	-
R17	13	13	I/O		Analog Input Port 8	-	-
R20	14	-	I/O		-	-	-
R21	15	-	I/O		-	-	-
R22	16	-	I/O		-	-	-
R23	17	14	I/O		Analog Input Port 9	-	-
R24	18	15	I/O		Analog Input Port 10	-	-
R25	19	16	I/O		Analog Input Port 11	-	-
R26	20	17	I/O		Analog Input Port 12	-	-
R27	21	-	I/O		-	-	-
R30(AN13)	22	18	I/O		Analog Input Port 13	-	-
R31 (AN14)	23	19	I/O		Analog Input Port 14	-	-
R32 (AN15)	24	20	I/O		Analog Input Port 15	-	-

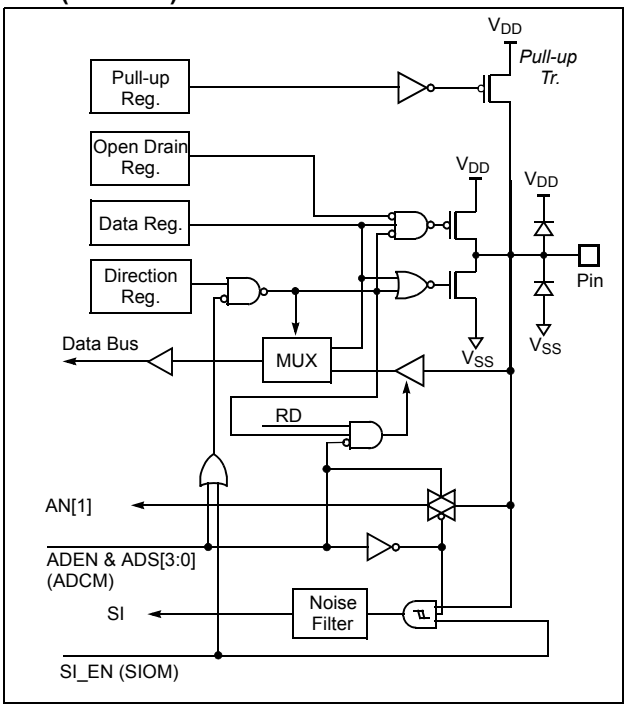
Table 5-5 Pin Description

6. PORT STRUCTURES

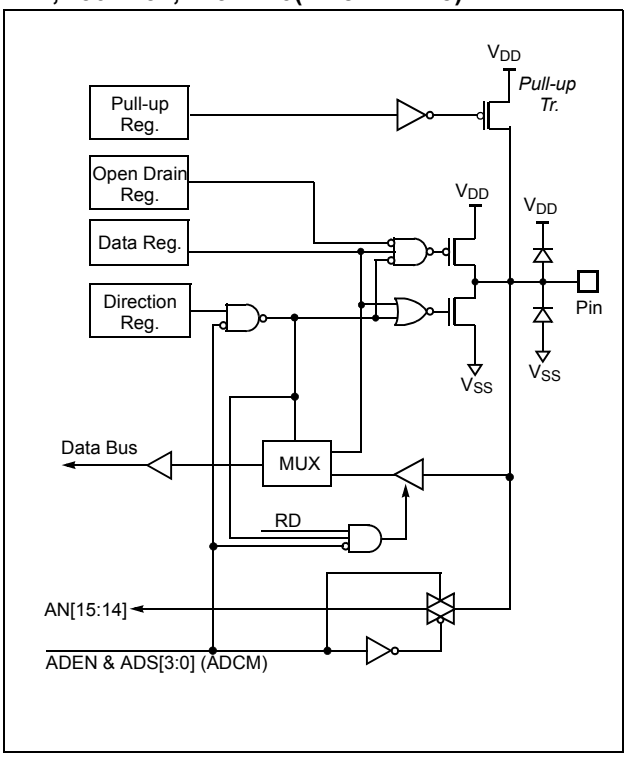
R13~R16,R20~R22,R27



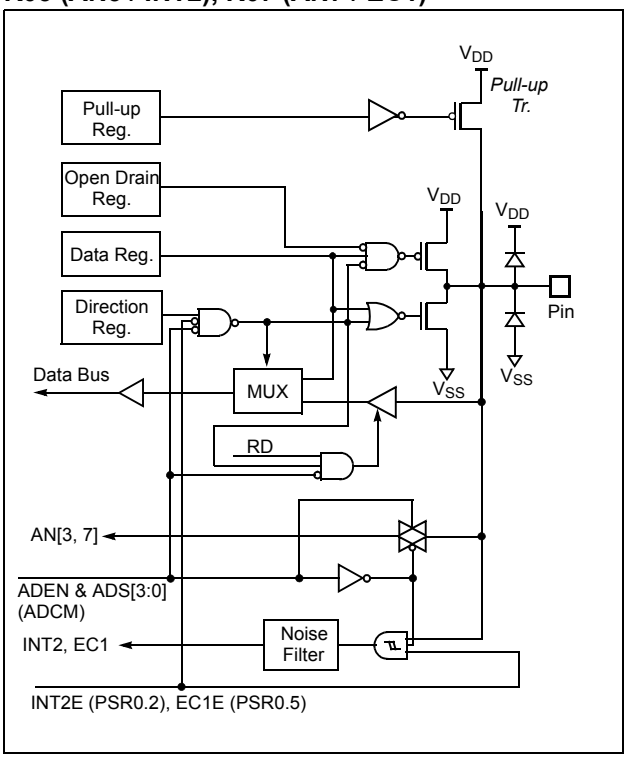
R01 (AN1 / SI)



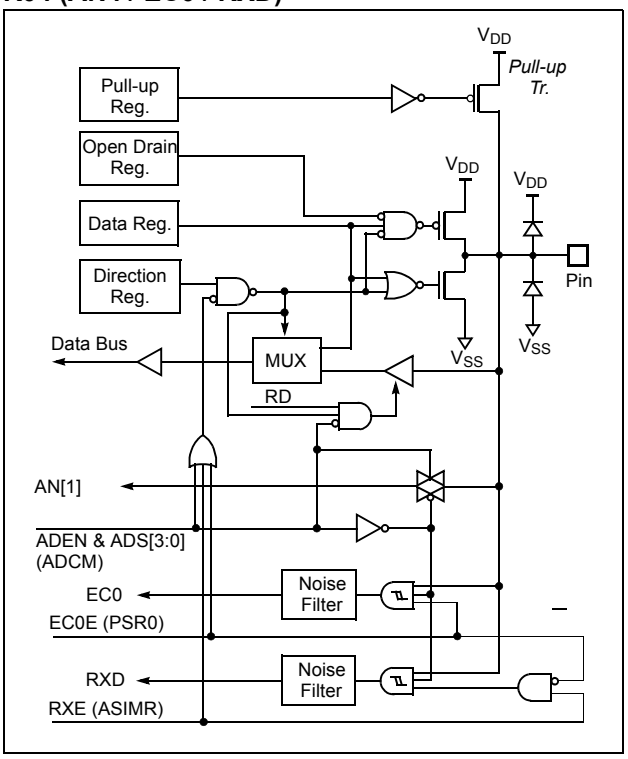
R17,R30~R32,R23~R26(AN8 ~ AN15)



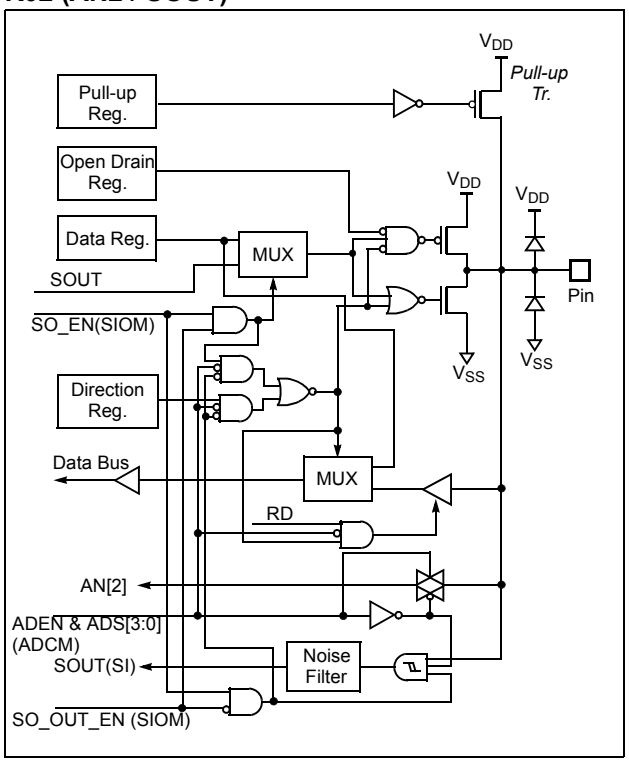
R03 (AN3 / INT2), R07 (AN7 / EC1)



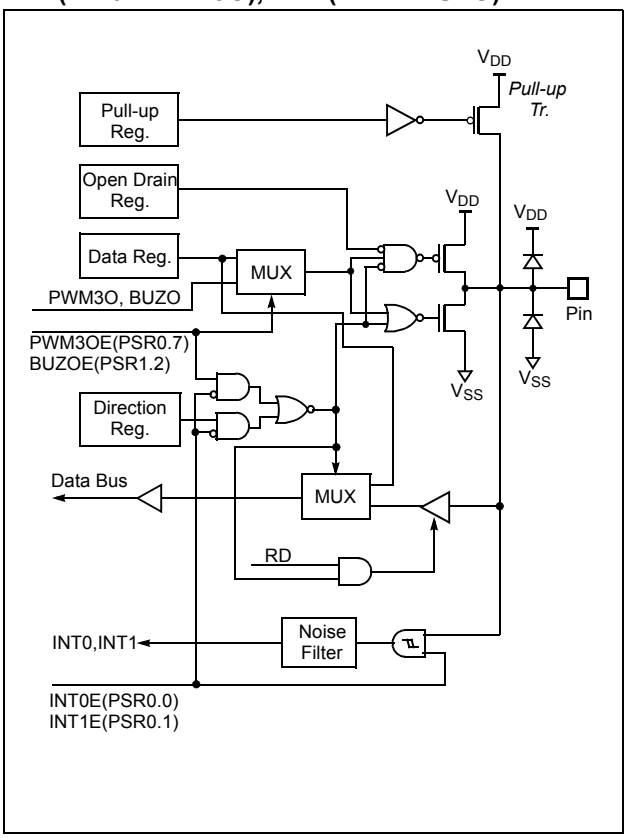
R04 (AN4 / EC0 / RXD)



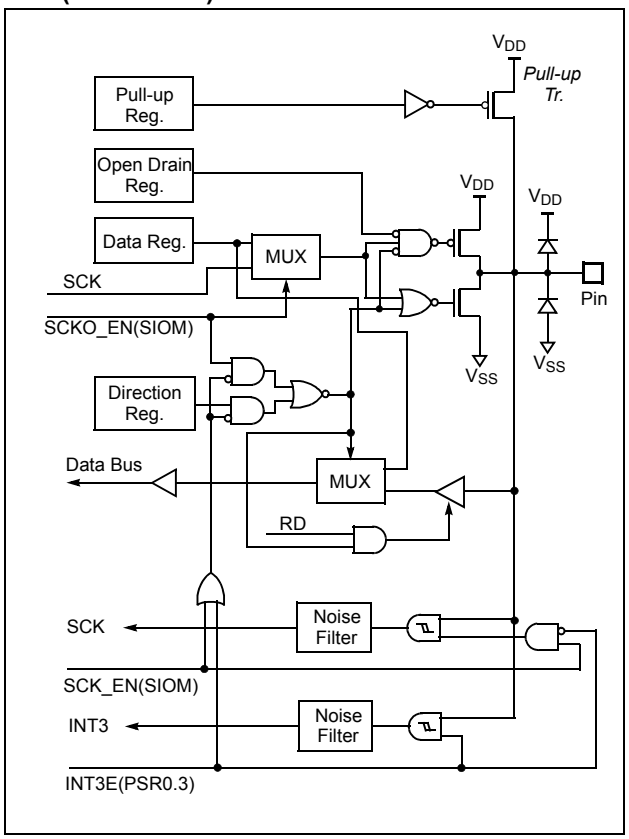
R02 (AN2 / SOUT)



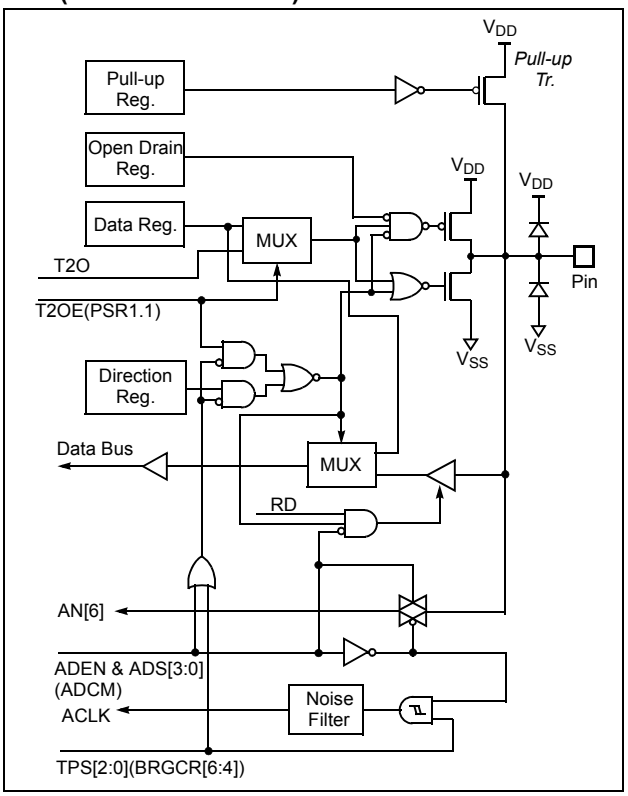
R11 (INT0 / PWM3O), R12 (INT1 / BUZO)



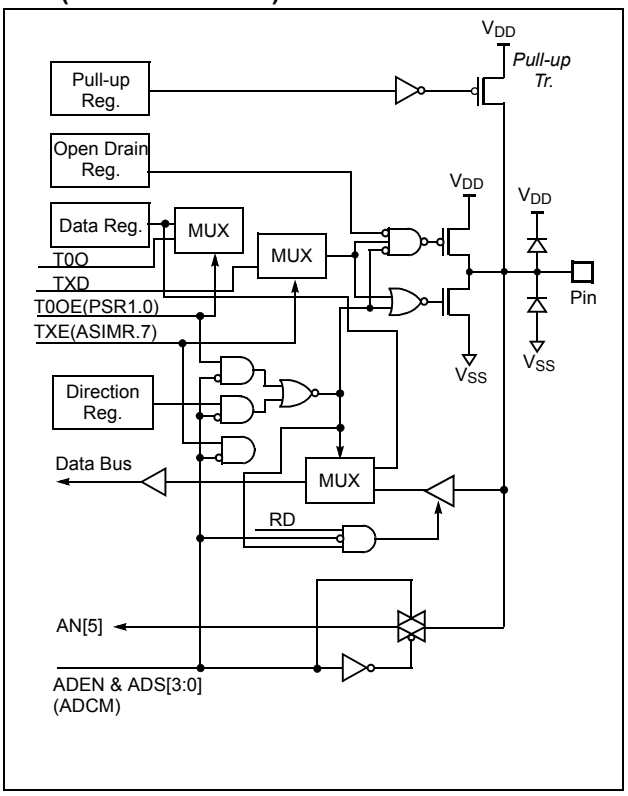
R00 (INT3 / SCK)



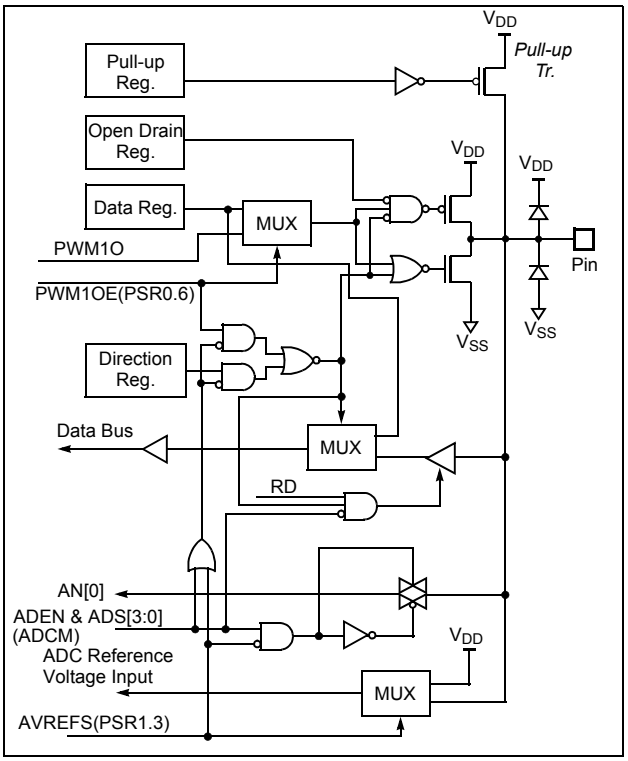
R06 (AN6 / T2O / ACLK)



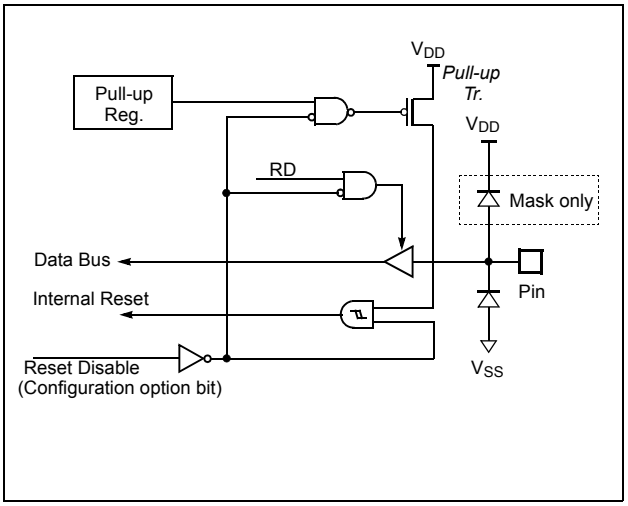
R05 (AN5 / T0O / TXD)



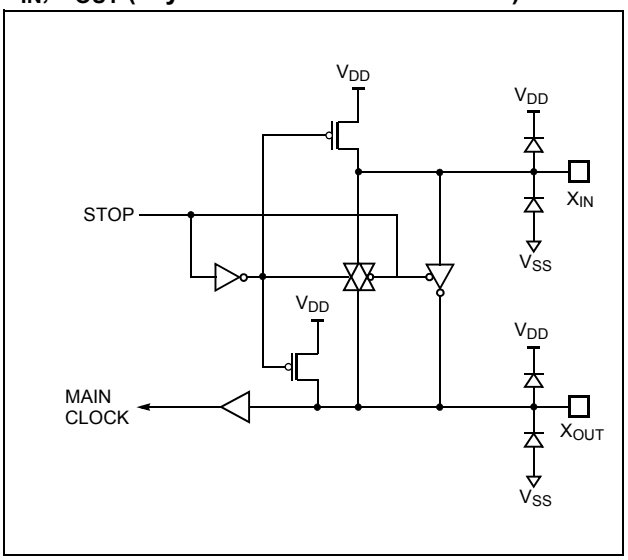
R10 (AN0 / AV_{REF} / PWM1O)



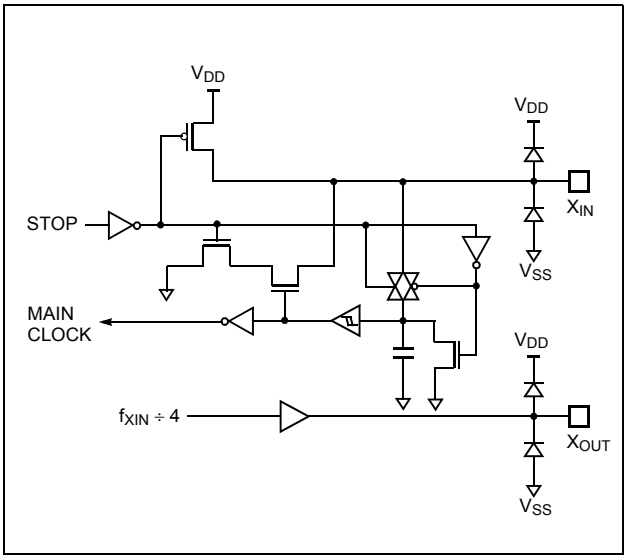
RESET



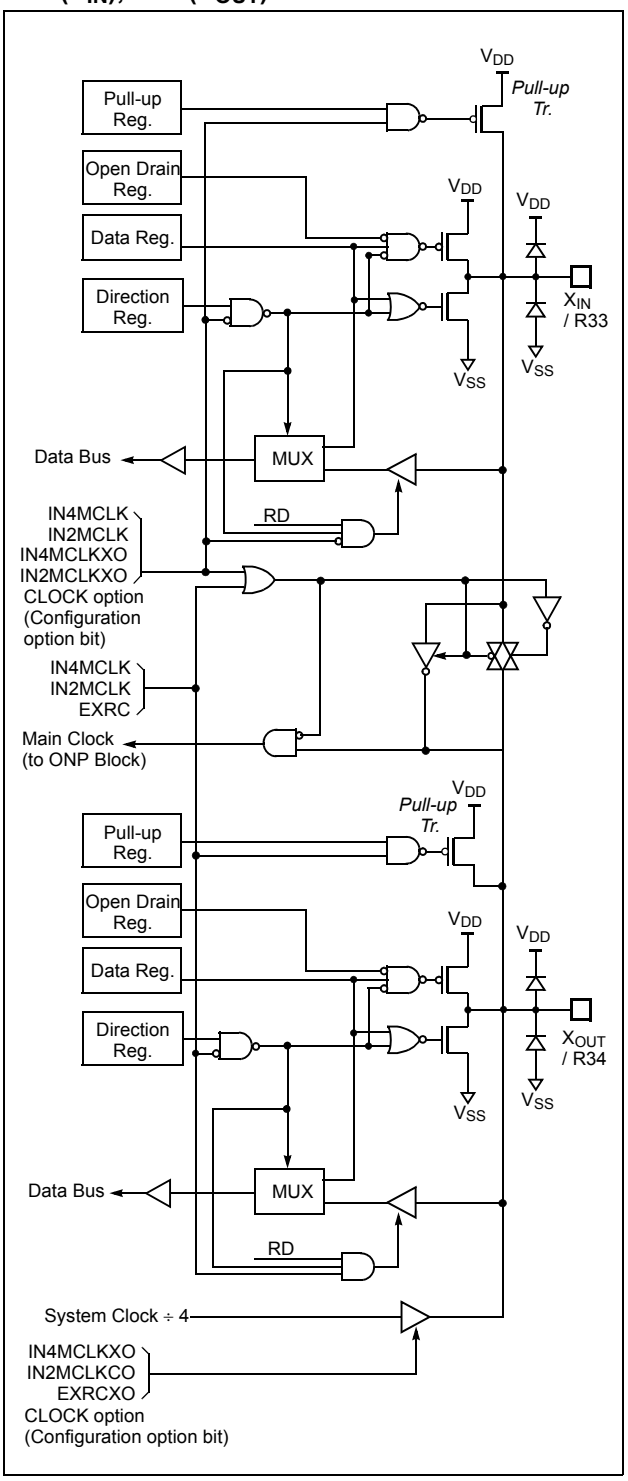
X_{IN}, X_{OUT} (Crystal or Ceramic Resonator)



X_{IN}, X_{OUT} (External RC or R oscillation)



R33 (X_{IN}), R34 (X_{OUT})



7. ELECTRICAL CHARACE TERISTICS

7.1 Absolute Maximum Ratings

Supply voltage ..... -0.3 to +6.0 V

Storage Temperature ..... -65 to +150 °C

Voltage on any pin with respect to Ground (V_{SS}) ..... -0.3 to V_{DD}+0.3V

Maximum current out of V_{SS} pin ..... 200 mA

Maximum current into V_{DD} pin ..... 100 mA

Maximum current sunk by (I_{OL} per I/O Pin) ..... 20 mA

Maximum output current sourced by (I_{OH} per I/O Pin) ..... 10 mA

Maximum current (ΣI_{OL}) ..... 160 mA

Maximum current (ΣI_{OH}) ..... 80 mA

Note: *Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

7.2 Recommended Operating Conditions

Parameter	Symbol	Condition	Specifications		Unit
			Min.	Max.	
Supply Voltage	V_{DD}	f_{XIN}=1~12MHz f_{XIN}=1~8MHz	4.5 2.7	5.5 5.5	V
Operating Frequency	f_{XIN}	V_{DD}=4.5~5.5V V_{DD}=2.7~5.5V(MC80F03XXX) V_{DD}=2.0~5.5V(MC80C03XXX)	1 1 1	12 8 4.2	MHz
Operating Temperature	T_{OPR}	V_{DD} =2.7~5.5V(MC80F03XXX) V_{DD} =2.0~5.5V(MC80C03XXX)	-40	85	°C

7.3 A/D Converter Characteristics

(T_a=-40~85°C, V_{SS}=0V, V_{DD}=2.7~5.5V @f_{XIN}=8MHz)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Resolution		-	-	10	-	BIT
Overall Accuracy	-	-	-	-	±3	LSB
Integral Linearity Error	ILE	V_{DD} = AV_{REF} = 5V CPU Clock = 10MHz V_{SS} = 0V	-	–	±3	LSB
Differential Linearity Error	DLE		-	–	±3	LSB
Offset Error of Top	EOT		-	±1	±3	LSB
Offset Error of Bottom	EOB		-	±0.5	±3	LSB
Conversion Time	T_{CONV}	-	13	-	-	μS
Analog Input Voltage	V_{AIN}	-	V_{SS}	-	V_{DD} (AV_{REF})	V
Analog Reference Voltage	AV_{REF}	-	TBD	-	V_{DD}	V
Analog Input Current	I_{AIN}	V_{DD} = AV_{REF} = 5V	-	-	10	μA
Analog Block Current	I_{AVDD}	V_{DD} = AV_{REF} = 5V V_{DD} = AV_{REF} = 3V	- -	1 0.5	3 1.5	mA
		V_{DD} = AV_{REF} = 5V power down mode	-	100	500	nA

7.4 DC Electrical Characteristics

(T_A=-40~85°C, V_{DD}=5.0V, V_{SS}=0V),

Parameter	Symbol	Pin	Condition	Specifications			Unit
				Min.	Typ.	Max.	
Input High Voltage	V_{IH1}	X_{IN}, $\overline{RESET}$		0.8 V_{DD}	-	V_{DD}	V
	V_{IH2}	Hysteresis Input[1]		0.8 V_{DD}	-	V_{DD}	
	V_{IH3}	Normal Input		0.7 V_{DD}	-	V_{DD}	
Input Low Voltage	V_{IL1}	X_{IN}, $\overline{RESET}$		0	-	0.2 V_{DD}	V
	V_{IL2}	Hysteresis Input[1]		0	-	0.2 V_{DD}	
	V_{IL3}	Normal Input		0	-	0.3 V_{DD}	
Output High Voltage	V_{OH}	All Output Port	V_{DD}=5V, I_{OH}=-5mA	V_{DD} -1	-	-	V
Output Low Voltage	V_{OL}	All Output Port	V_{DD}=5V, I_{OL}=10mA	-	-	1	V
Input Pull-up Current	I_P	Normal Input	V_{DD}=5V	-60	-	-150	μA
Input High Leakage Current	I_{IH1}	All Pins (except X_{IN})	V_{DD}=5V	-	-	5	μA
	I_{IH2}	X_{IN}	V_{DD}=5V	-	12	20	μA
Input Low Leakage Current	I_{IL1}	All Pins (except X_{IN})	V_{DD}=5V	-5	-	-	μA
	I_{IL2}	X_{IN}	V_{DD}=5V	-20	-12	-	μA
Hysteresis	$\lvert V_T \rvert$	Hysteresis Input[1]	V_{DD}=5V	0.5	-	-	V
PFD Voltage	V_{PFD}	V_{DD}		2.4	2.9	3.4	V
POR Voltage[2]	V_{POR}	V_{DD}		2.2	2.7	3.2	V
POR Start Voltage[2]	V_{START}	V_{DD}		-	-	1.9	V
POR Rising Time[2]	T_{POR}	V_{DD}		-	-	40	ms/V
V_{DD} Rising Time[2]	T_{VDD}	V_{DD}		-	-	40	ms/V
Internal RC WDT Period	T_{RCWDT}	X_{OUT}	V_{DD}=5.5V	36	-	90	μS
Operating Current	I_{DD}	V_{DD}	V_{DD}=5.5V, f_{XIN}=12MHz	-	-	15	mA
Sleep Mode Current	I_{SLEEP}	V_{DD}	V_{DD}=5.5V, f_{XIN}=12MHz	-	-	4.5	mA
RCWDT Mode Current at Stop Mode	I_{RCWDT}	V_{DD}	V_{DD}=5.5V	-	-	50	μA
Stop Mode Current	I_{STOP}	V_{DD}	V_{DD}=5.5V, f_{XIN}=12MHz	-	-	5	μA
Internal Oscillation Frequency	f_{IN_CLK}	X_{OUT}	V_{DD}=5V	3	4	5	MHz
$\overline{RESET}$ Input Noise Cancel Time	T_{RST_NC}	$\overline{RESET}$	V_{DD}=5V	1.5		1.8	μs
External RC[2] Oscillator Frequency	$f_{RC\text{-}OSC}$	f_{XOUT} = $f_{RC\text{-}OSC}$ ÷ 4	V_{DD}=5.5V R=30kΩ, C=10pF		2.2		MHz
	$f_{R\text{-}OSC}$	f_{XOUT} = $f_{R\text{-}OSC}$ ÷ 4	V_{DD}=5.5V, R=30kΩ		1.6		MHz

1. Hysteresis Input: INT0 ~INT3(R11,R12,R03,R00),SIO(R00,R01,R02),UART(R04,R06),EC0,EC1
2. These parameters are presented for design guidance only and not tested or guaranteed.

7.5 AC Characteristics

(T_A=-40~+85°C, V_{DD}=5V±10%, V_{SS}=0V)

Parameter	Symbol	Pins	Specifications			Unit
			Min.	Typ.	Max.	
Operating Frequency	f_{CP}	X_{IN}	1	-	8	MHz
External Clock Pulse Width	t_{CPW}	X_{IN}	50	-	-	nS
External Clock Transition Time	t_{RCP},t_{FCP}	X_{IN}	-	-	20	nS
Oscillation Stabilizing Time	t_{ST}	X_{IN}, X_{OUT}	-	-	20	mS
External Input Pulse Width	t_{EPW}	INT0, INT1, INT2, INT3 EC0, EC1	2	-	-	t_{SYS}
$\overline{RESET}$ Input Width	t_{RST}	$\overline{RESET}$	8	-	-	t_{SYS}

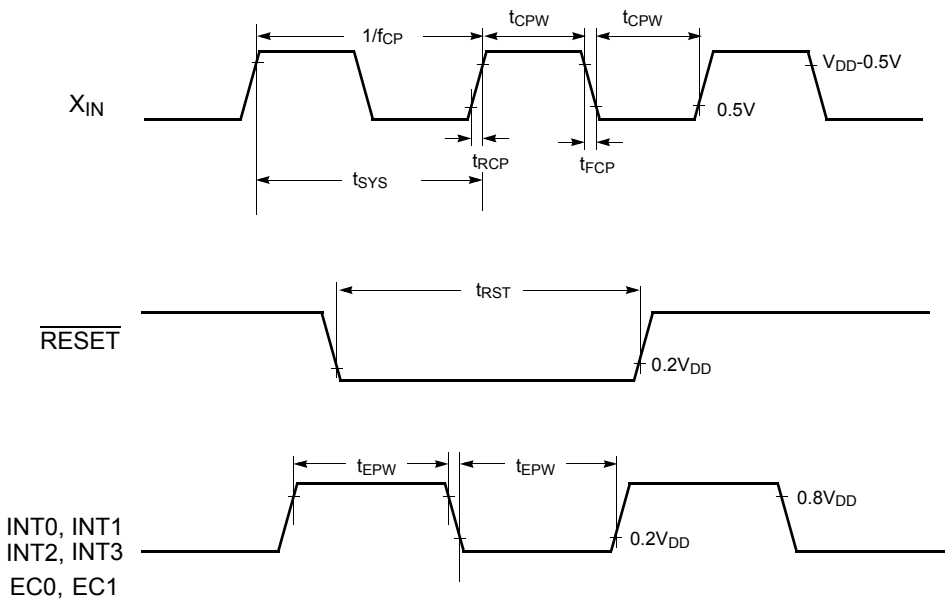


Figure 7-1 Timing Chart

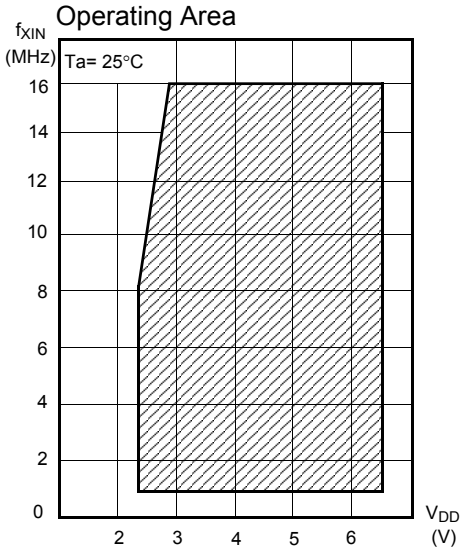
7.6 Typical Characteristics (MC80F0304/08/16)

These graphs and tables provided in this section are for design guidance only and are not tested or guaranteed.

In some graphs or tables the data presented are outside specified operating range (e.g. outside specified V_{DD} range). This is for information only and devices are guaranteed to operate properly only within the specified range.

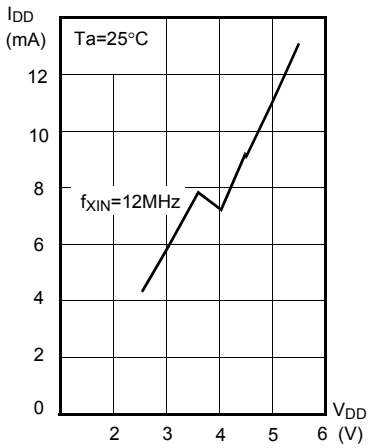
The data presented in this section is a statistical summary of data collected on units from different lots over a period of time. "Typical" represents the mean of the distribution while "max" or "min" represents (mean + 3σ) and (mean − 3σ) respectively where σ is standard deviation

Operating Area



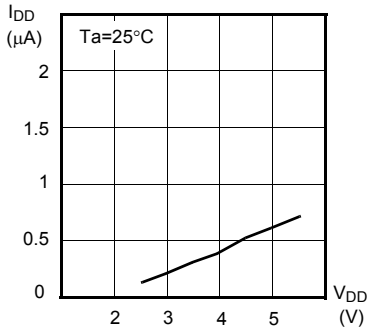
Normal Operation

I_{DD}–V_{DD}



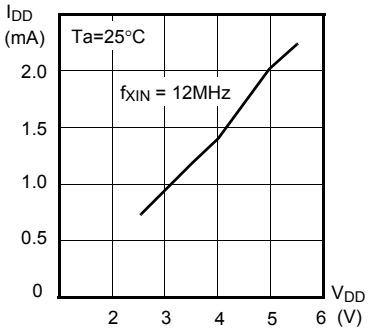
STOP Mode

I_{STOP}–V_{DD}



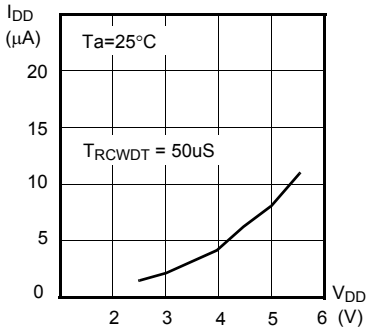
SLEEP Mode

I_{SLEEP}–V_{DD}

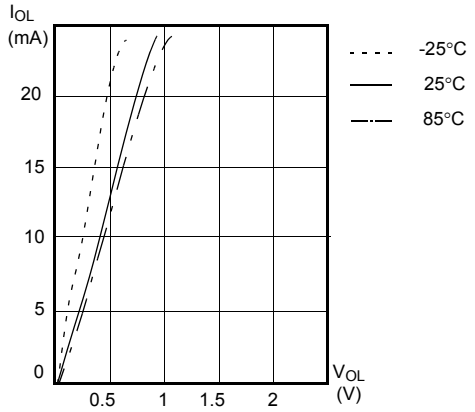


RC-WDT in Stop Mode

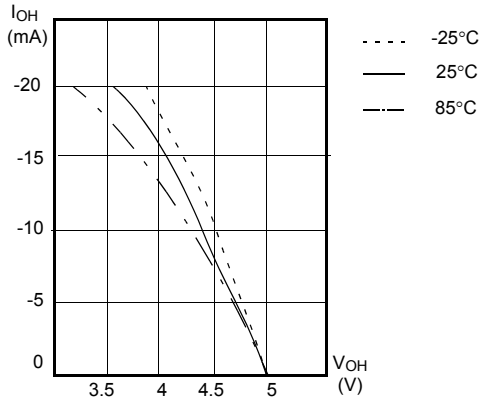
I_{RCWDT}–V_{DD}



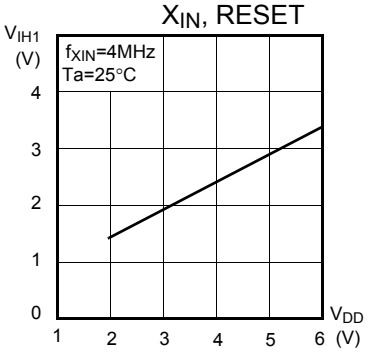
I_{OL}–V_{OL}, V_{DD}=5V



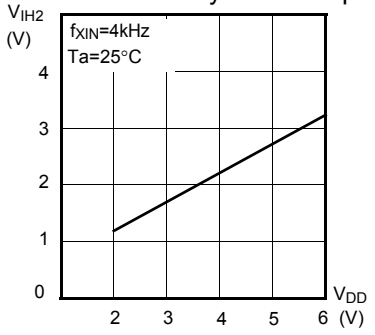
I_{OH}–V_{OH}, V_{DD}=5V



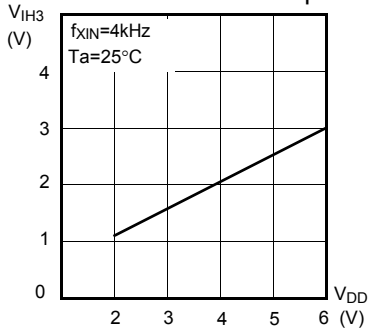
V_{DD}–V_{IH1} X_{IN}, $\overline{RESET}$



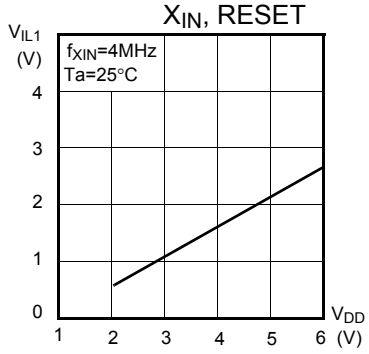
V_{DD}–V_{IH2} Hysteresis input



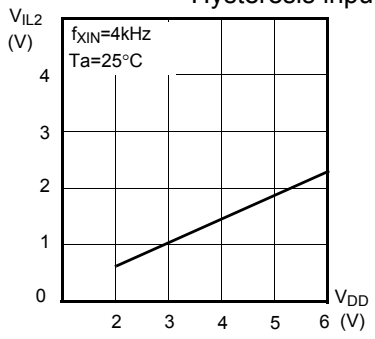
V_{DD}–V_{IH3} Normal input



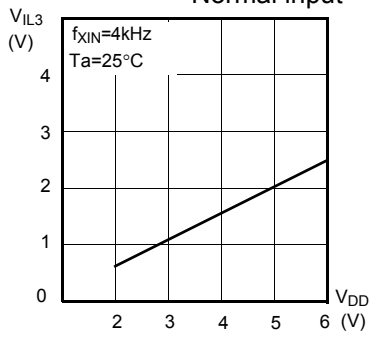
V_{DD}–V_{IL1} X_{IN}, $\overline{RESET}$



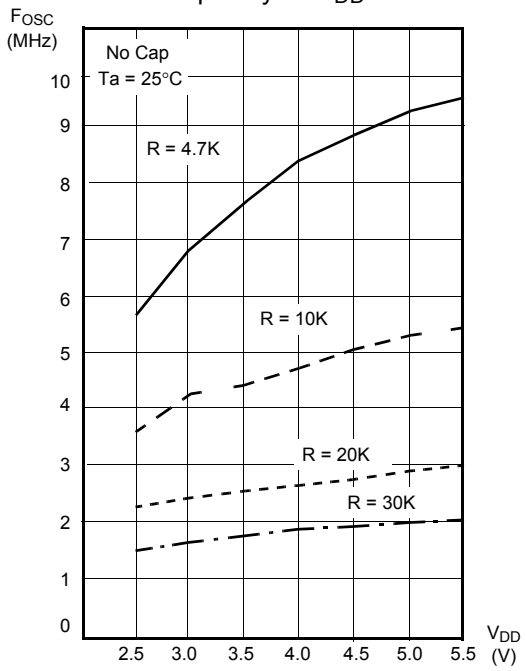
V_{DD}–V_{IL2} Hysteresis input



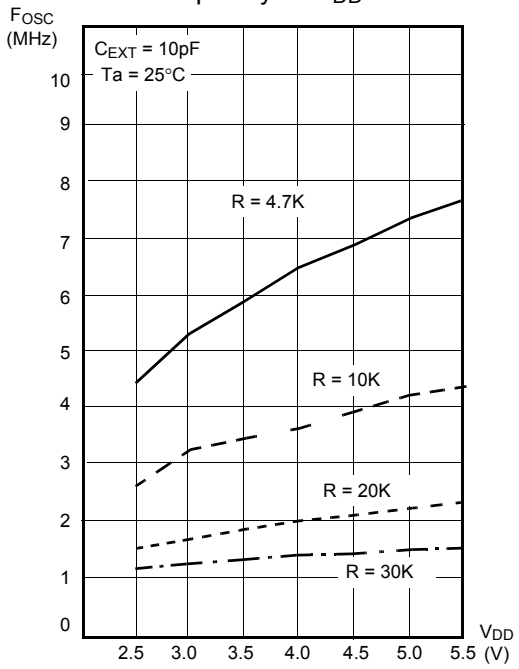
V_{DD}–V_{IL3} Normal input



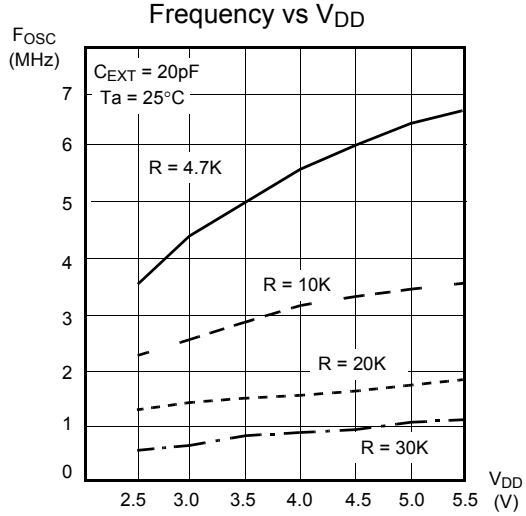
Typical RC Oscillator
Frequency vs V_{DD}



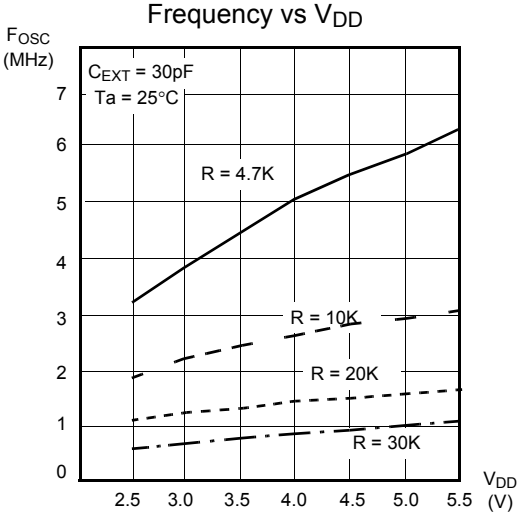
Typical RC Oscillator
Frequency vs V_{DD}



Typical RC Oscillator
Frequency vs V_{DD}

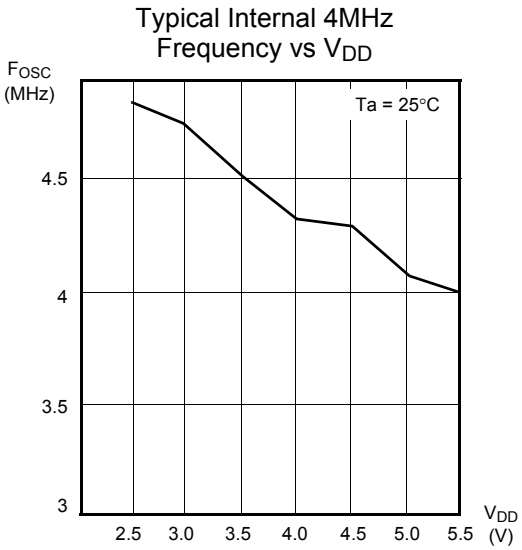


Typical RC Oscillator
Frequency vs V_{DD}



Note: *The external RC oscillation frequencies shown in above are provided for design guidance only and not tested or guaranteed. The user needs to take into account that the external RC oscillation frequencies generated by the same circuit design may be not the same. Because there are variations in the resistance and capacitance due to the tolerance of external R and C components. The parasitic capacitance difference due to the different wiring length and layout may change the external RC oscillation frequencies.*

Note: *The external RC oscillation frequencies of the MC80F0304/0308/0316 may be different from that of the MC80C0304/0308/0316. There may be the difference between package types(PDIP, SOP, SKDIP). The user should modify the value of R and C components to get the proper frequency in exchanging Flash device to Mask device or one package type to another package type.*



Note: *The internal 4MHz oscillation frequencies shown in above are provided for design guidance only and not tested or guaranteed. The user needs to take into account that the internal oscillation of the MC80F0308 may show different frequency with sample by sample, voltage and temperature. The internal oscillation can be used only in timing insensitive application.*

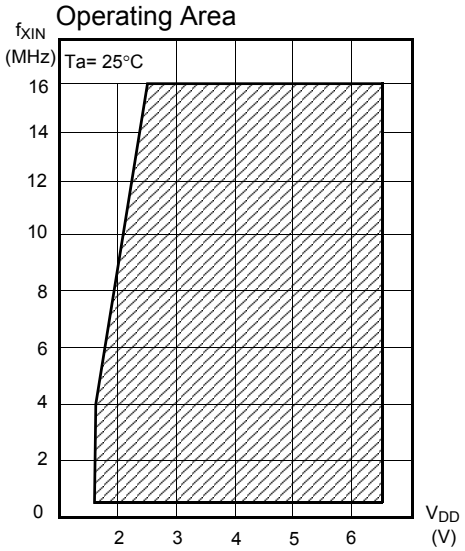
7.7 Typical Characteristics (MC80C0304/08/16)

These graphs and tables provided in this section are for design guidance only and are not tested or guaranteed.

In some graphs or tables the data presented are outside specified operating range (e.g. outside specified V_{DD} range). This is for information only and devices are guaranteed to operate properly only within the specified range.

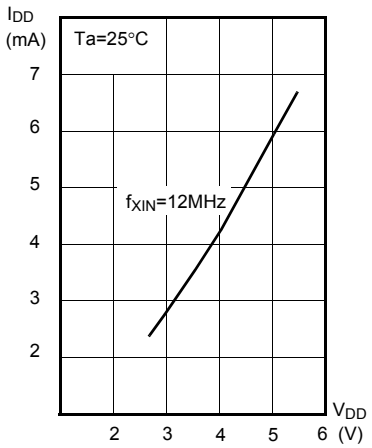
The data presented in this section is a statistical summary of data collected on units from different lots over a period of time. "Typical" represents the mean of the distribution while "max" or "min" represents (mean + 3σ) and (mean − 3σ) respectively where σ is standard deviation

Operating Area



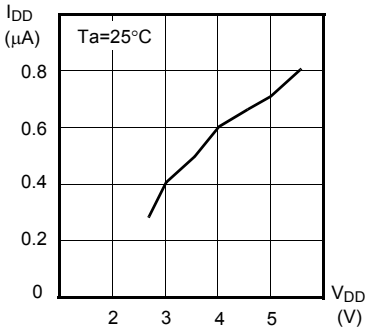
Normal Operation

I_{DD}–V_{DD}



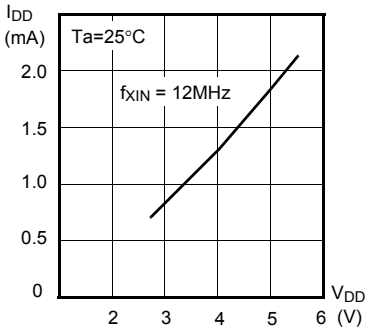
STOP Mode

I_{STOP}–V_{DD}

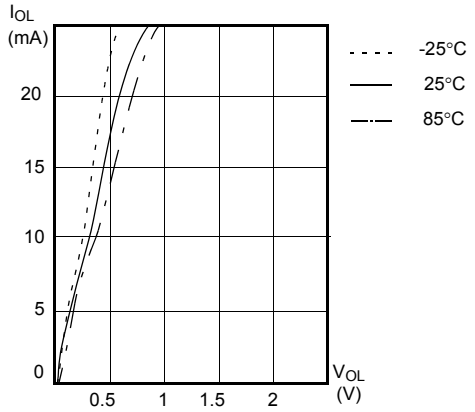


SLEEP Mode

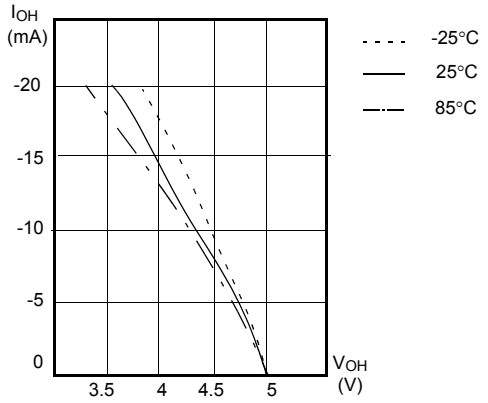
I_{SLEEP}–V_{DD}



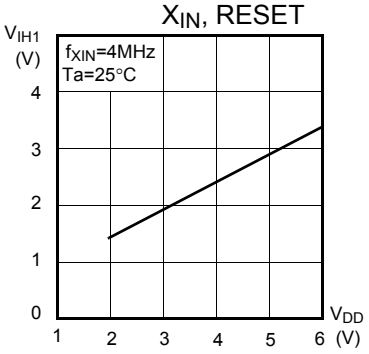
I_{OL}–V_{OL}, V_{DD}=5V



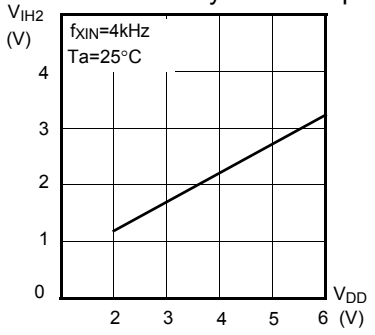
I_{OH}–V_{OH}, V_{DD}=5V



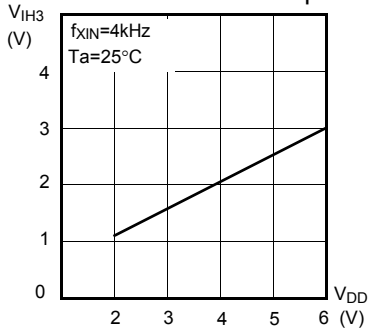
V_{DD}–V_{IH1} X_{IN}, $\overline{RESET}$



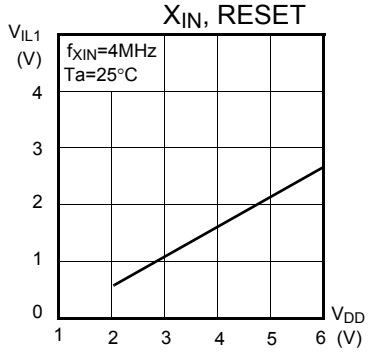
V_{DD}–V_{IH2} Hysteresis input



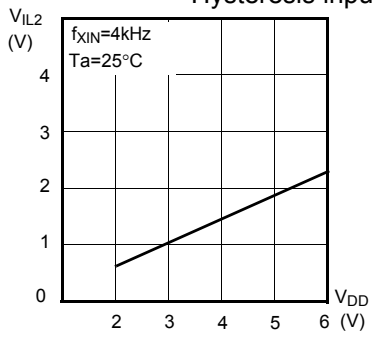
V_{DD}–V_{IH3} Normal input



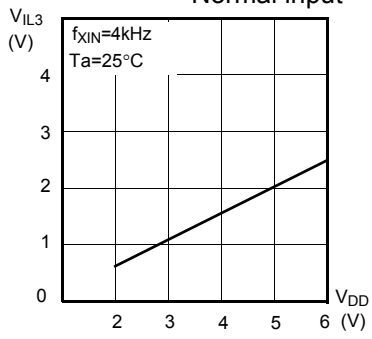
V_{DD}–V_{IL1} X_{IN}, $\overline{RESET}$

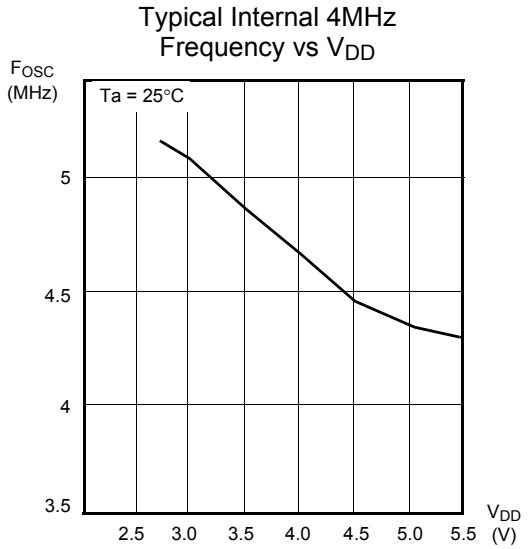


V_{DD}–V_{IL2} Hysteresis input



V_{DD}–V_{IL3} Normal input





Note: *The internal 4MHz oscillation frequencies shown in above are provided for design guidance only and not tested or guaranteed. The user needs to take into account that the internal oscillation of the MC80C0104 or MC80C0204 may show different frequency with sample by sample, voltage and temperature. The internal oscillation can be used only in timing insensitive application.*

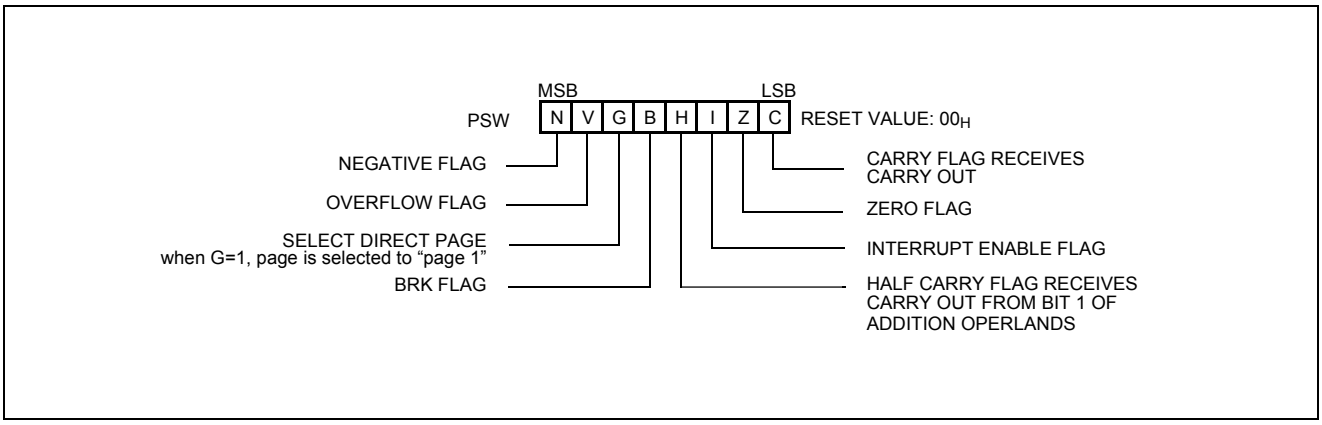


Figure 8-3 PSW (Program Status Word) Register

[Interrupt disable flag I]

This flag enables/disables all interrupts except interrupt caused by Reset or software BRK instruction. All interrupts are disabled when cleared to "0". This flag immediately becomes "0" when an interrupt is served. It is set by the EI instruction and cleared by the DI instruction.

[Half carry flag H]

After operation, this is set when there is a carry from bit 3 of ALU or there is no borrow from bit 4 of ALU. This bit can not be set or cleared except CLRV instruction with Overflow flag (V).

[Break flag B]

This flag is set by software BRK instruction to distinguish BRK from TCALL instruction with the same vector address.

[Direct page flag G]

This flag assigns RAM page for direct addressing mode. In the direct addressing mode, addressing area is from zero page 00_H to $0FF_H$ when this flag is "0". If it is set to "1", addressing area is assigned 100_H to $1FF_H$. It is set by SETG instruction and cleared by CLRG.

[Overflow flag V]

This flag is set to "1" when an overflow occurs as the result of an arithmetic operation involving signs. An overflow occurs when the result of an addition or subtraction exceeds +127($7F_H$) or -128(80_H). The CLRV instruction clears the overflow flag. There is no set instruction. When the BIT instruction is executed, bit 6 of memory is copied to this flag.

[Negative flag N]

This flag is set to match the sign bit (bit 7) status of the result of a data or arithmetic operation. When the BIT instruction is executed, bit 7 of memory is copied to this flag.

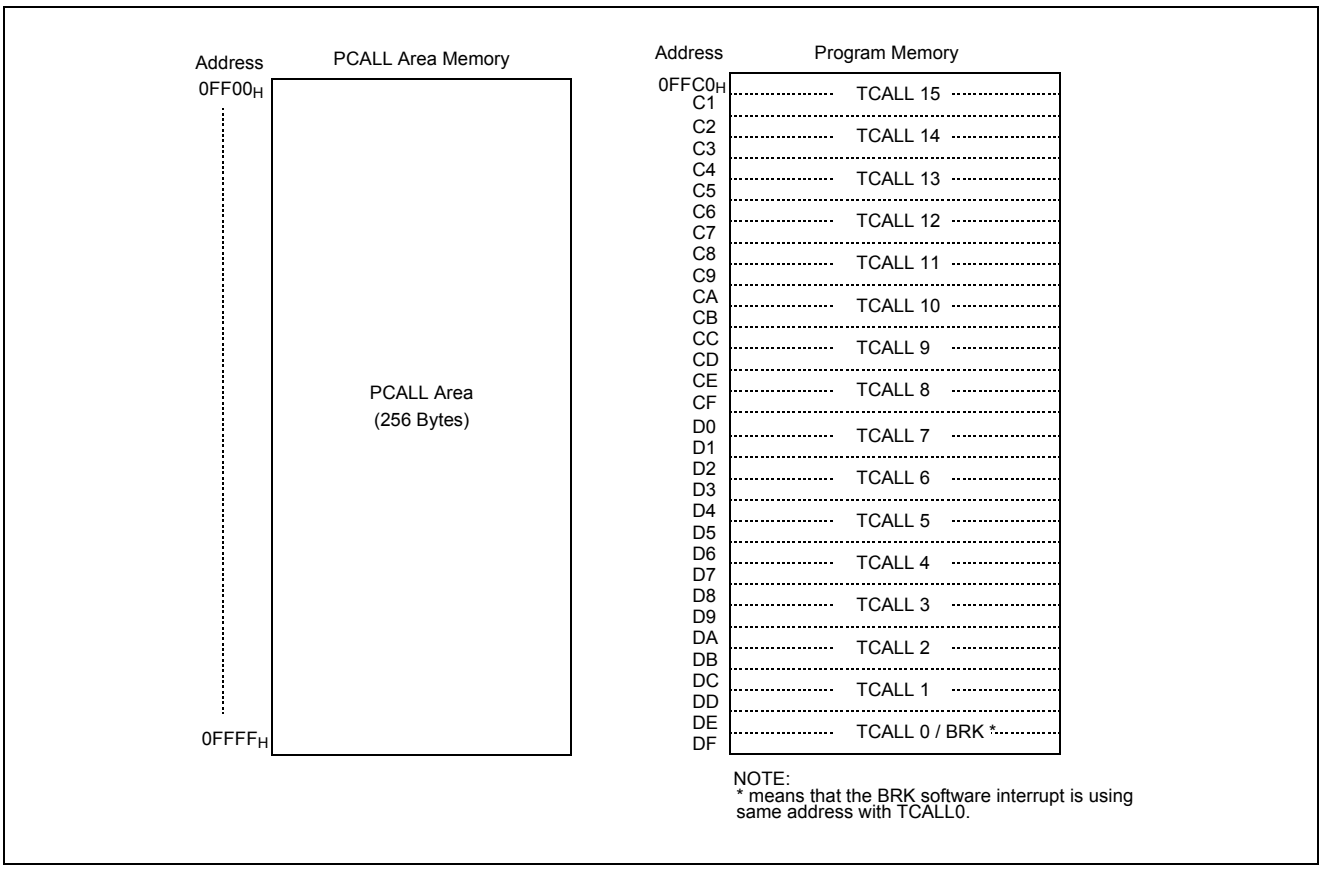
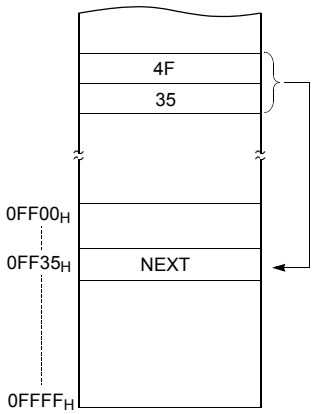


Figure 8-7 PCALL and TCALL Memory Area

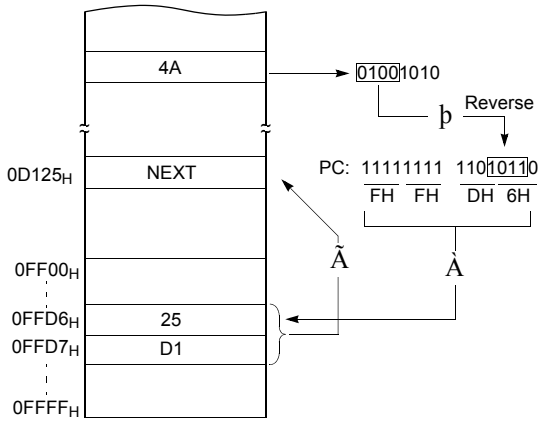
PCALL→ rel

```
4F35      PCALL  35H
```



TCALL→ n

```
4A        TCALL  4
```



Example: The usage software example of Vector address

Address	Register Name	Symbol	R/W	Initial Value								Addressing Mode
				7	6	5	4	3	2	1	0	
00C0	R0 port data register	R0	R/W	0	0	0	0	0	0	0	0	byte, bit[1]
00C1	R0 port I/O direction register	R0IO	W	0	0	0	0	0	0	0	0	byte[2]
00C2	R1 port data register	R1	R/W	0	0	0	0	0	0	0	0	byte, bit
00C3	R1 port I/O direction register	R1IO	W	0	0	0	0	0	0	0	0	byte
00C4	R2 port data register	R2	R/W	0	0	0	0	0	0	0	0	byte, bit
00C5	R2 port I/O direction register	R2IO	W	0	0	0	0	0	0	0	0	byte
00C6	R3 port data register	R3	R/W	-	-	0	0	0	0	0	0	byte, bit
00C7	R3 port I/O direction register	R3IO	W	-	-	0	0	0	0	0	0	byte
00C8	Port 0 Open Drain Selection Register	R0OD	W	0	0	0	0	0	0	0	0	byte
00C9	Port 1 Open Drain Selection Register	R1OD	W	0	0	0	0	0	0	0	0	byte
00CA	Port 2 Open Drain Selection Register	R2OD	W	0	0	0	0	0	0	0	0	byte
00CB	Port 3 Open Drain Selection Register	R3OD	W	-	-	0	0	0	0	0	0	byte
00D0	Timer 0 mode control register	TM0	R/W	-	-	0	0	0	0	0	0	byte, bit
00D1	Timer 0 register	T0	R	0	0	0	0	0	0	0	0	byte
	Timer 0 data register	TDR0	W	1	1	1	1	1	1	1	1	
	Timer 0 capture data register	CDR0	R	0	0	0	0	0	0	0	0	
00D2	Timer 1 mode control register	TM1	R/W	0	0	0	0	0	0	0	0	byte, bit
00D3	Timer 1 data register	TDR1	W	1	1	1	1	1	1	1	1	byte
	Timer 1 PWM period register	T1PPR	W	1	1	1	1	1	1	1	1	byte
00D4	Timer 1 register	T1	R	0	0	0	0	0	0	0	0	byte
	Timer 1 capture data register	CDR1	R	0	0	0	0	0	0	0	0	
	Timer 1 PWM duty register	T1PDR	R/W	0	0	0	0	0	0	0	0	byte
00D5	Timer 1 PWM high register	T1PWHR	W	-	-	-	-	0	0	0	0	bit
00D6	Timer 2 mode control register	TM2	R/W	-	-	0	0	0	0	0	0	byte, bit
00D7	Timer 2 register	T2	R	0	0	0	0	0	0	0	0	byte
	Timer 2 data register	TDR2	W	1	1	1	1	1	1	1	1	
	Timer 2 capture data register	CDR2	R	0	0	0	0	0	0	0	0	
00D8	Timer 3 mode control register	TM3	R/W	0	0	0	0	0	0	0	0	byte, bit
00D9	Timer 3 data register	TDR3	W	1	1	1	1	1	1	1	1	byte
	Timer 3 PWM period register	T3PPR	W	1	1	1	1	1	1	1	1	
00DA	Timer 3 register	T3	R	0	0	0	0	0	0	0	0	byte
	Timer 3 PWM duty register	T3PDR	R/W	0	0	0	0	0	0	0	0	
	Timer 3 capture data register	CDR3	R	0	0	0	0	0	0	0	0	

Table 8-1 Control Registers

Address	Register Name	Symbol	R/W	Initial Value								Addressing Mode
				7	6	5	4	3	2	1	0	
00DB	Timer 3 PWM high register	T3PWHR	W	-	-	-	-	0	0	0	0	byte
00E0	Buzzer driver register	BUZR	W	1	1	1	1	1	1	1	1	byte
00E1	RAM page selection register	RPR	R/W	-	-	-	-	-	0	0	0	byte, bit
00E2	SIO mode control register	SIOM	R/W	0	0	0	0	0	0	0	1	byte, bit
00E3	SIO data shift register	SIOR	R/W	Undefined								byte, bit
00E6	UART mode register	ASIMR	R/W	0	0	0	0	-	0	0	-	byte, bit
00E7	UART status register	ASISR	R	-	-	-	-	-	0	0	0	byte
00E8	UART Baud rate generator control register	BRGCR	R/W	-	0	0	1	0	0	0	0	byte, bit
00E9	UART Receive buffer register	RXBR	R	0	0	0	0	0	0	0	0	byte
	UART Transmit shift register	TXSR	W	1	1	1	1	1	1	1	1	
00EA	Interrupt enable register high	IENH	R/W	0	0	0	0	0	0	0	0	byte, bit
00EB	Interrupt enable register low	IENL	R/W	0	0	0	0	0	0	0	0	byte, bit
00EC	Interrupt request register high	IRQH	R/W	0	0	0	0	0	0	0	0	byte, bit
00ED	Interrupt request register low	IRQL	R/W	0	0	0	0	0	0	0	0	byte, bit
00EE	Interrupt edge selection register	IEDS	R/W	0	0	0	0	0	0	0	0	byte, bit
00EF	A/D converter mode control register	ADCM	R/W	0	0	0	0	0	0	0	1	byte, bit
00F0	A/D converter result high register	ADCRH	R(W)	0	1	0	Undefined					byte
00F1	A/D converter result low register	ADCRL	R	Undefined								byte
00F2	Basic interval timer register	BITR	R	Undefined								byte
	Clock control register	CKCTLR	W	0	-	0	1	0	1	1	1	
00F4	Watch dog timer register	WDTR	W	0	1	1	1	1	1	1	1	byte
	Watch dog timer data register	WDTDR	R	Undefined								
00F5	Stop & sleep mode control register	SSCR	W	0	0	0	0	0	0	0	0	byte
00F7	PFD control register	PFDR	R/W	-	-	-	-	-	0	0	0	byte, bit
00F8	Port selection register 0	PSR0	W	0	0	0	0	0	0	0	0	byte
00F9	Port selection register 1	PSR1	W	-	-	-	-	0	0	0	0	byte
00FC	Pull-up selection register 0	PU0	W	0	0	0	0	0	0	0	0	byte
00FD	Pull-up selection register 1	PU1	W	0	0	0	0	0	0	0	0	byte
00FE	pull-up selection register 2	PU2	W	0	0	0	0	0	0	0	0	byte
00FF	Pull-up selection register 3	PU3	W	-	-	0	0	0	0	0	0	byte

Table 8-1 Control Registers

1. The 'byte, bit' means registers are controlled by both bit and byte manipulation instruction.
   Caution) The R/W register except T1PDR and T3PDR are both can be byte and bit manipulated.

2. The 'byte' means registers are controlled by only byte manipulation instruction. Do not use bit manipulation instruction such as SET1, CLR1 etc. If bit manipulation instruction is used on these registers, content of other seven bits are may varied to unwanted value.

*The mark of '-' means this bit location is reserved.

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0C0H	R0	R0 Port Data Register							
0C1H	R0IO	R0 Port Direction Register							
0C2H	R1	R1 Port Data Register							
0C3H	R1IO	R1 Port Direction Register							
0C4H	R2	R2 Port Data Register							
0C5H	R2IO	R2Port Data Register							
0C6H	R3	R3 Port Data Register							
0C7H	R3IO	R3 Port Direction Register							
0C8H	R0OD	R0 Open Drain Selection Register							
0C9H	R1OD	R1 Open Drain Selection Register							
0CAH	R2OD	R2 Open Drain Selection Register							
0CBH	R3OD	R3 Open Drain Selection Register							
0D0H	TM0	-	-	CAP0	T0CK2	T0CK1	T0CK0	T0CN	T0ST
0D1H	T0/TDR0/ CDR0	Timer0 Register / Timer0 Data Register / Timer0 Capture Data Register							
0D2H	TM1	T1_POL	T1_16BIT	PWM1E	CAP1	T1CK1	T1CK0	T1CN	T1ST
0D3H	TDR1/ T1PPR	Timer1 Data Register / Timer1 PWM Period Register							
0D4H	T1/CDR1	Timer1 Register / Timer1 Capture Data Register							
0D5H	PWM1HR	-	-	-	-	Timer1 PWM High Register			
0D6H	TM2	-	-	CAP2	T2CK2	T2CK1	T2CK0	T2CN	T2ST
0D7H	T2/TDR2/ CDR2	Timer2 Register / Timer2 Data Register / Timer2 Capture Data Register							
0D8H	TM3	T3_POL	T3_16BIT	PWM3E	CAP3	T3CK1	T3CK0	T3CN	T3ST
0D9H	TDR3/ T3PPR	Timer3 Data Register / Timer3 PWM Period Register							
0DAH	T3/CDR3/ T3PDR	Timer3 Register / Timer3 Capture Data Register / Timer3 PWM Duty Register							
0DBH	PWM3HR	-	-	-	-	Timer3 PWM High Register			
0E0H	BUZR	BUCK1	BUCK0	BUR5	BUR4	BUR3	BUR2	BUR1	BUR0
0E1H	RPR	-	-	-	-	-	RPR2	RPR1	RPR0
0E2H	SIOM	POL	IOSW	SM1	SM0	SCK1	SCK0	SIOST	SIOSF

Table 8-2 Control Register Function Description

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0E3H	SIOR	SIO Data Shift Register							
0E6H	ASIMR	TXE	RXE	PS01	PS00	-	SL0	ISRM	-
0E7H	ASISR	-	-	-	-	-	PE0	FE0	OVE0
0E8H	BRGCR0	-	TPS02	TPS01	TPS00	MLD03	MLD02	MLD01	MLD00
0E9H	RXR	UART Receive Buffer Register							
	TXR	UART Transmit Shift Register							
0EAH	IENH	INT0E	INT1E	INT2E	INT3E	RXE	TXE	SIOE	T0E
0EBH	IENL	T1E	T2E	T3E	-	ADCE	WDTE	WTE	BITE
0ECH	IRQH	INT0IF	INT1IF	INT2IF	INT3IF	RXIF	TXIF	SIOIF	T0IF
0EDH	IRQL	T1IF	T2IF	T3IF	T4IF	ADCIF	WDTIF	WTIF	BITIF
0EEH	IEDS	IED3H	IED3L	IED2H	IED2L	IED1H	IED1L	IED0H	IED0L
0EFH	ADCM	ADEN	ADCK	ADS3	ADS2	ADS1	ADS0	ADST	ADSF
0F0H	ADCRH	PSSEL1	PSSEL0	ADC8	-	-	-	ADC Result Reg. High	
0F1H	ADCRL	ADC Result Register Low							
0F2H	BITR[1]	Basic Interval Timer Data Register							
	CKCTLR[1]	ADRST	-	RCWDT	WDTON	BTCL	BTS2	BTS1	BTS0
0F4H	WDTR	WDTCL	7-bit Watchdog Timer Register						
	WDTDR	Watchdog Timer Data Register (Counter Register)							
0F5H	SSCR	Stop & Sleep Mode Control Register							
0F7H	PFDR	-	-	-	-	-	PFDEN	PFDM	PFDS
0F8H	PSR0	PWM3O	PWM1O	EC1E	EC0E	INT3E	INT2E	INT1E	INT0E
0F9H	PSR1	-	-	-	-	XTEN	BUZO	T2O	T0O
0FCH	PU0	R0 Pull-up Selection Register							
0FDH	PU1	R1 Pull-up Selection Register							
0FEH	PU2	R2 Pull-up Selection Register							
0FFH	PU3	R3 Pull-up Selection Register							

Table 8-2 Control Register Function Description

1. The register BITR and CKCTLR are located at same address. Address ECH is read as BITR, written to CKCTLR.

Caution) The registers of dark-shaded area can not be accessed by bit manipulation instruction such as "SET1, CLR1", but should be accessed by register operation instruction such as "LDM dp,#imm".

8.4 Addressing Mode

The MC8 series MCU uses six addressing modes;

- **Register addressing**
- **Immediate addressing**
- **Direct page addressing**
- **Absolute addressing**
- **Indexed addressing**
- **Register-indirect addressing**

Register Addressing

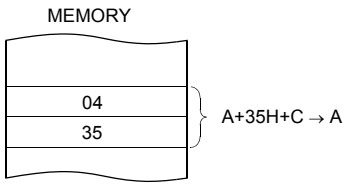
Register addressing accesses the A, X, Y, C and PSW.

Immediate Addressing → #imm

In this mode, second byte (operand) is accessed as a data immediately.

Example:

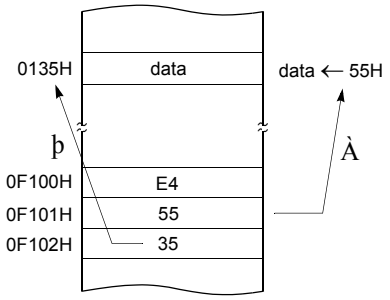
```
0435     ADC    #35H
```



When G-flag is 1, then RAM address is defined by 16-bit address which is composed of 8-bit RAM paging register (RPR) and 8-bit immediate data.

Example: G=1

```
E45535   LDM    35H,#55H
```

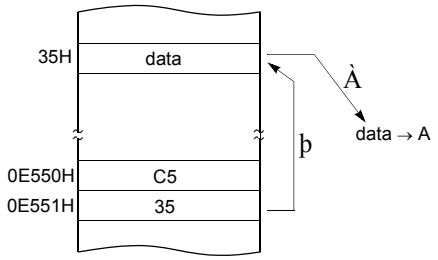


Direct Page Addressing → dp

In this mode, a address is specified within direct page.

Example; G=0

```
C535     LDA    35H          ;A ←RAM[35H]
```



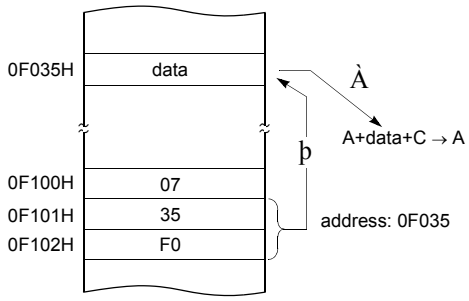
Absolute Addressing → !abs

Absolute addressing sets corresponding memory data to Data, i.e. second byte (Operand I) of command becomes lower level address and third byte (Operand II) becomes upper level address. With 3 bytes command, it is possible to access to whole memory area.

ADC, AND, CMP, CMPX, CMPY, EOR, LDA, LDX, LDY, OR, SBC, STA, STX, STY

Example;

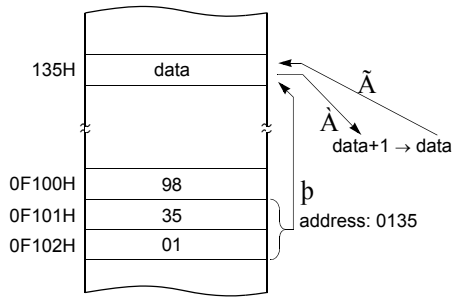
```
0735F0   ADC    !0F035H      ;A ←ROM[0F035H]
```

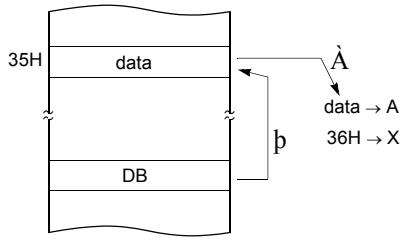


The operation within data memory (RAM)
ASL, BIT, DEC, INC, LSR, ROL, ROR

Example; Addressing accesses the address 0135_H regardless of G-flag.

```
983501   INC    !0135H       ;A ←ROM[135H]
```





Indexed Addressing

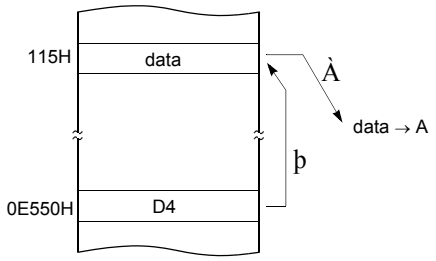
X indexed direct page (no offset) → {X}

In this mode, a address is specified by the X register.

ADC, AND, CMP, EOR, LDA, OR, SBC, STA, XMA

Example; X=15_H, G=1

```
D4       LDA    {X}          ;ACC←RAM[X].
```



X indexed direct page, auto increment→ {X}+

In this mode, a address is specified within direct page by the X register and the content of X is increased by 1.

LDA, STA

Example; G=0, X=35_H

```
DB       LDA    {X}+
```

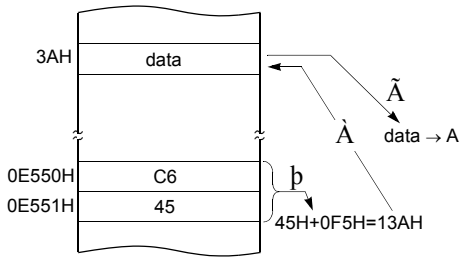
X indexed direct page (8 bit offset) → dp+X

This address value is the second byte (Operand) of command plus the data of X-register. And it assigns the memory in Direct page.

ADC, AND, CMP, EOR, LDA, LDY, OR, SBC, STA STY, XMA, ASL, DEC, INC, LSR, ROL, ROR

Example; G=0, X=$0F5_H$

```
C645     LDA    45H+X
```



Y indexed direct page (8 bit offset) → dp+Y

This address value is the second byte (Operand) of command plus the data of Y-register, which assigns Memory in Direct page.

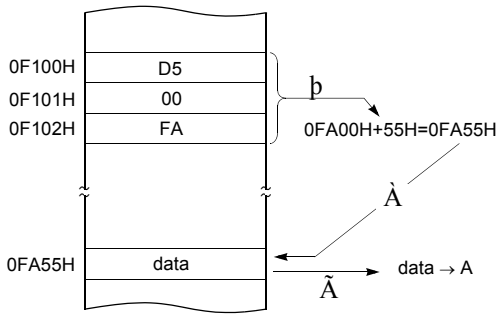
This is same with above (2). Use Y register instead of X.

Y indexed absolute → !abs+Y

Sets the value of 16-bit absolute address plus Y-register data as Memory.This addressing mode can specify memory in whole area.

Example; Y=55_H

```
D500FA   LDA    !0FA00H+Y
```



Indirect Addressing

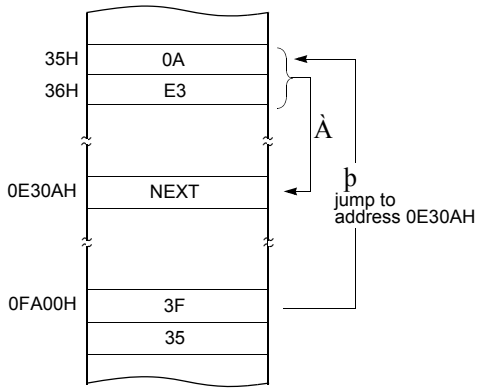
Direct page indirect → [dp]

Assigns data address to use for accomplishing command which sets memory data (or pair memory) by Operand.
Also index can be used with Index register X,Y.

JMP, CALL

Example; G=0

```
3F35     JMP    [35H]
```



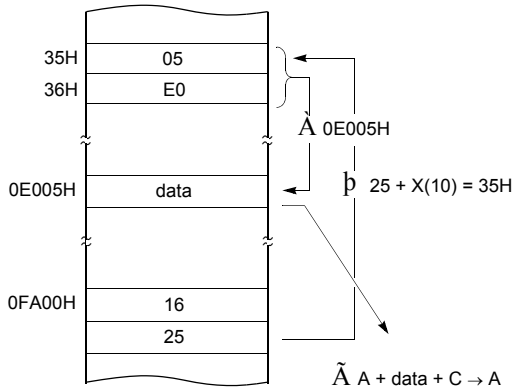
X indexed indirect → [dp+X]

Processes memory data as Data, assigned by 16-bit pair memory which is determined by pair data [dp+X+1][dp+X] Operand plus X-register data in Direct page.

ADC, AND, CMP, EOR, LDA, OR, SBC, STA

Example; G=0, X=10_H

```
1625     ADC    [25H+X]
```



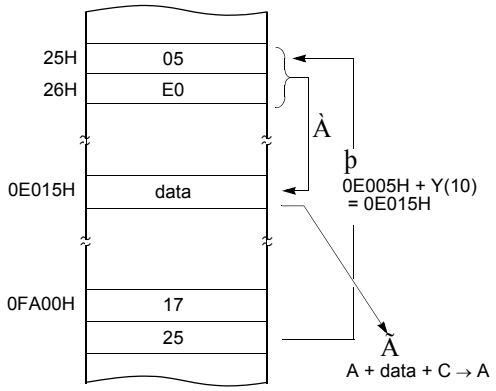
Y indexed indirect → [dp]+Y

Processes memory data as Data, assigned by the data [dp+1][dp] of 16-bit pair memory paired by Operand in Direct page plus Y-register data.

ADC, AND, CMP, EOR, LDA, OR, SBC, STA

Example; G=0, Y=10_H

```
1725     ADC    [25H]+Y
```



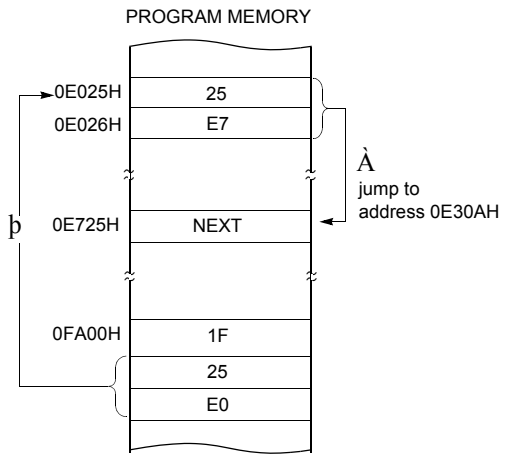
Absolute indirect → [!abs]

The program jumps to address specified by 16-bit absolute address.

JMP

Example; G=0

```
1F25E0   JMP    [!0C025H]
```



counter input 0 (EC0), timer 0 output (T0O), timer 2 output (T2O) and event counter input 1 (EC1). When the alternate function is selected by writing "1" in the corresponding bit of PSR0 or PSR1, port pin can be used as a corresponding alternate features regardless of the direction register R0IO.

The ADC input channel 1~7 (AN1~AN7), SIO data input (SI), SIO data output (SOUT) and UART data input (RXD), UART data output (TXD) and UART clock input (ACLK) can be selected by setting ADCM($00EF_H$), SIOM($00E2_H$) and ASIMR($00E6_H$) register to enable the corresponding peripheral operation and select operation mode.

Port Pin	Alternate Function
R00-	INT3 (External interrupt 3) SCK (SIO clock input/output)
R01	AN1(ADC Input channel 1) SI (SIO data input)I
R02	AN2 (ADC Input channel 2) SOUT (SIO data output)
R03	AN3 (ADC Input channel 3) INT2 (External interrupt 2)
R04	AN4 (ADC Input channel 4) EC0 (Event counter input 0) RXD (UART data input)
R05	AN5 (ADC Input channel 5) T0O (Timer output 0) TXD (UART data output)
R06	AN6 (ADC Input channel 6) T2O (Timer output 2) ACLK (UART clock input)
R07	AN7 (ADC Input channel 7) EC1 (Event counter input 1)

9.2 R1 and R1IO register

R1 is a 5-bit CMOS bidirectional I/O port (address $0C2_H$). Each I/O pin can independently used as an input or an output through the R1IO register (address $0C3_H$). When R10 through R17 pins are used as input ports, an on-chip pull-up resistor can be connected to them in 1-bit units with a pull-up selection register 1 (PU1). Each I/O pin of R1 port can be used to open drain output port by setting the corresponding bit of the open drain selection register 1 (R1OD).

In addition, Port R1 is multiplexed with various alternate functions. The port selection register PSR0 (address $0F8_H$) and PSR1 (address $0F9_H$) control the selection of alternate functions such as Analog reference voltage input (AVREF), external interrupt 0 (INT0), external interrupt 1 (INT1), PWM 1 output (PWM1O), PWM 3 output (PWM3O) and buzzer output (BUZO). When the alternate function is selected by writing "1" in the corresponding bit of PSR0 or PSR1, port pin can be used as a corresponding alternate features regardless of the direction register R1IO.

The ADC input channel 0 (AN0) and channel 8(AN8) can be selected by setting ADCM($00EF_H$) register to enable ADC and select channel 0 and channel 8 .

Port Pin	Alternate Function
R10	AN0 (ADC input channel 0) AVREF (Analog reference voltage)
R11	PWM1O (PWM 1 output) INT0 (External Interrupt 0)
R12	PWM3O (PWM 3 output) INT1 (External Interrupt 1) BUZO (Buzzer output)
R13	-
R14	-
R15	-
R16	-
R17	AN8

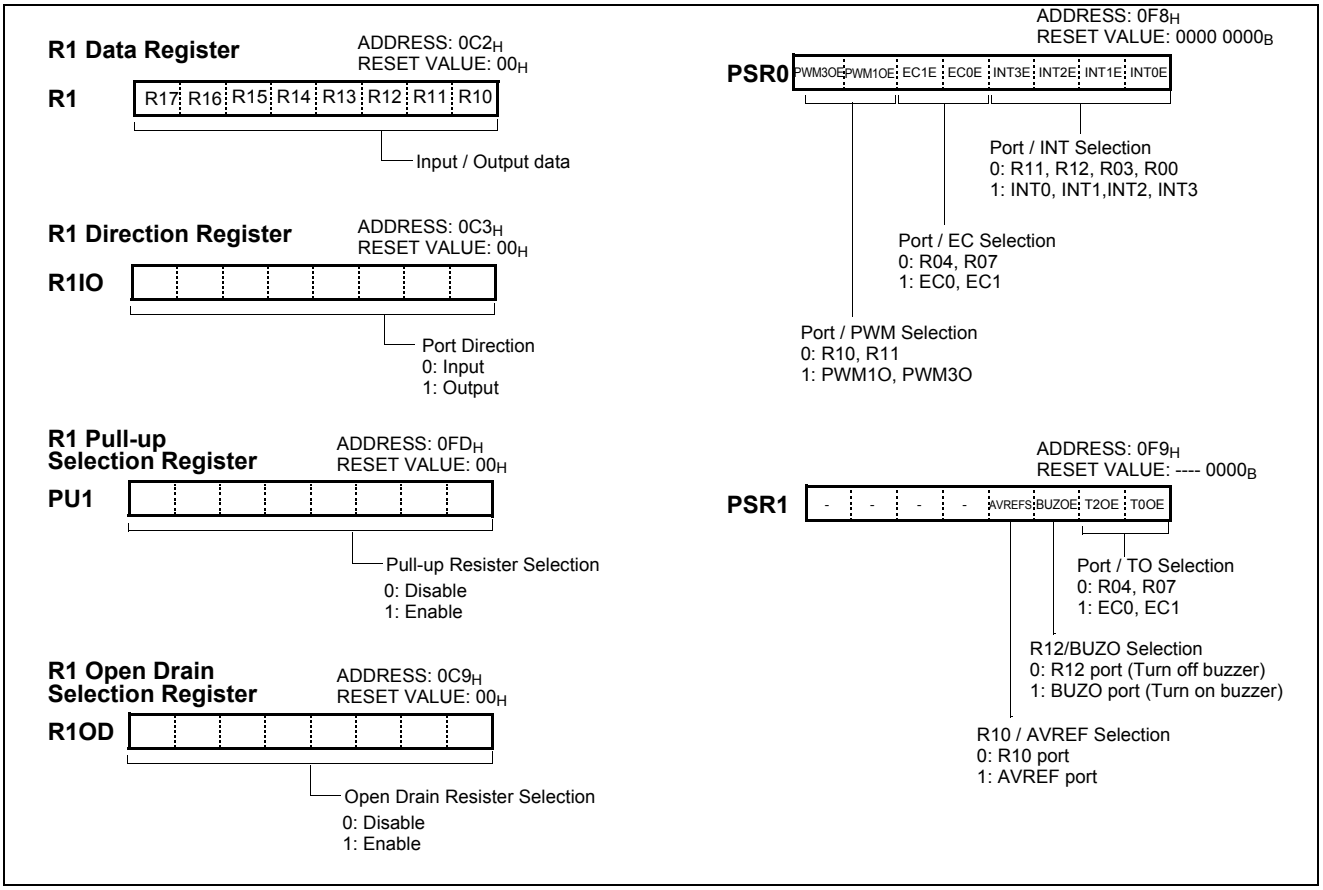


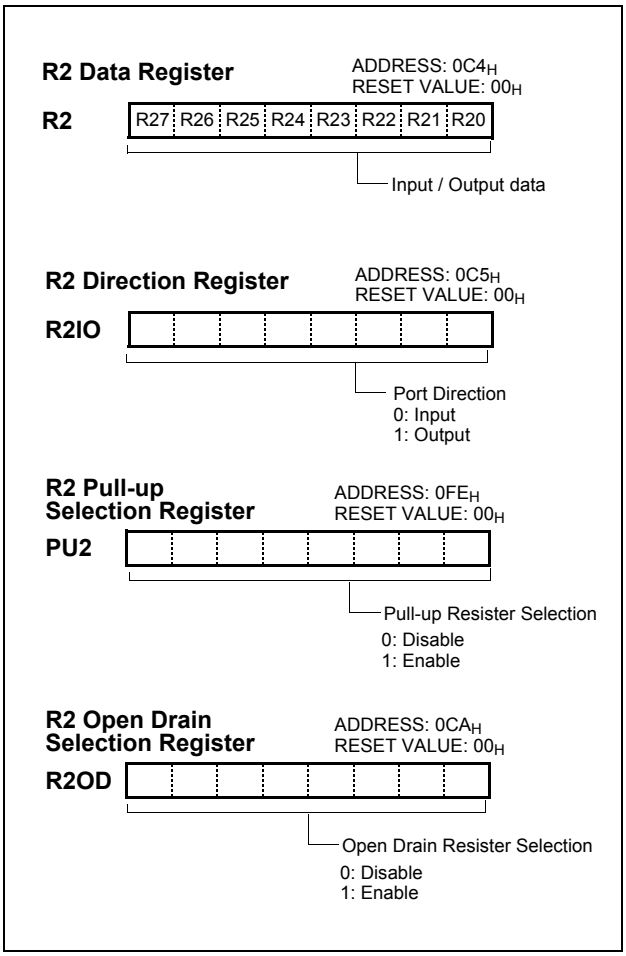
Figure 9-3 R1 Port Register

9.3 R2 and R2IO register

R2 is an 8-bit CMOS bidirectional I/O port (address $0C4_H$). Each I/O pin can independently used as an input or an output through the R3IO register (address $0C5_H$). When R20 through R27 pins are used as input ports, an on-chip pull-up resistor can be connected to them in 1-bit units with a pull-up selection register 2 (PU2). R20 through R27 pins can be used to open drain output port by setting the corresponding bit of the open drain selection register 2 (R2OD).

In addition, Port R2 is multiplexed with alternate functions. R23 R24,R25,and R26 can be used as ADC input channel 9 to 12 by setting ADCM to enable ADC and select channel 9 to 12.

Port Pin	Alternate Function
R20	-
R21	-
R22	-
R23	AN9 (ADC input channel 9)
R24	AN10 (ADC input channel 10)
R25	AN11 (ADC input channel 11)
R26	AN12 (ADC input channel 12)
R27	-



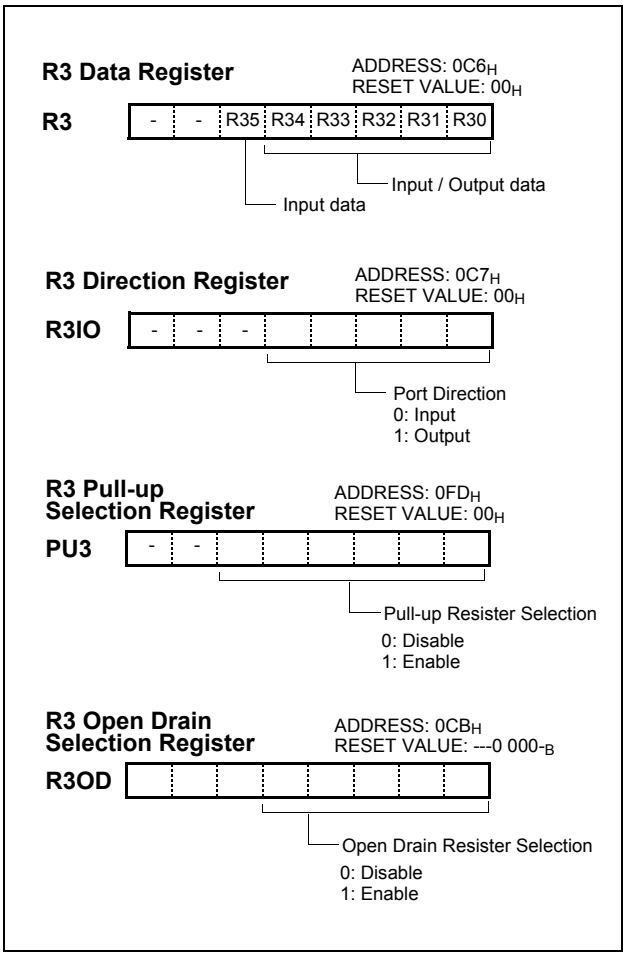
9.4 R3 and R3IO register

R3 is a 6-bit CMOS bidirectional I/O port (address $0C6_H$). Each I/O pin (except R35) can independently used as an input or an output through the R3IO register (address $0C7_H$). R35 is an input only port. When R30 through R35 pins are used as input ports, an on-chip pull-up resistor can be connected to them in 1-bit units with a pull-up selection register 3 (PU3). R30 through R34 pins can be used to open drain output port by setting the corresponding bit of the open drain selection register 1 (R3OD).

In addition, Port R3 is multiplexed with alternate functions. R30 R31,and R32 can be used as ADC input channel 13,14 and 15 by setting ADCM to enable ADC and select channel 13,14 and 15.

Port Pin	Alternate Function
R30	AN13 (ADC input channel 13)
R31	AN14 (ADC input channel 14)
R32	AN15 (ADC input channel 15)

R33, R34 and R35 is multiplexd with X_{IN}, X_{OUT}, and $\overline{RESET}$ pin .


R3 Data Register
ADDRESS: 0C6H
RESET VALUE: 00H
R3
- - R35 R34 R33 R32 R31 R30
Input / Output data
Input data
R3 Direction Register
ADDRESS: 0C7H
RESET VALUE: 00H
R3IO
- - -
Port Direction
0: Input
1: Output
R3 Pull-up Selection Register
ADDRESS: 0FDH
RESET VALUE: 00H
PU3
- -
Pull-up Resister Selection
0: Disable
1: Enable
R3 Open Drain Selection Register
ADDRESS: 0CBH
RESET VALUE: ---0 000-B
R3OD
Open Drain Resister Selection
0: Disable
1: Enable

CKCTLR [2:0]	Source clock	Interrupt (overflow) Period (ms) @ f_{XIN} = 8MHz
000	f_{XIN}÷8	0.256
001	f_{XIN}÷16	0.512
010	f_{XIN}÷32	1.024
011	f_{XIN}÷64	2.048
100	f_{XIN}÷128	4.096
101	f_{XIN}÷256	8.192
110	f_{XIN}÷512	16.384
111	f_{XIN}÷1024	32.768

Table 11-1 Basic Interval Timer Interrupt Period

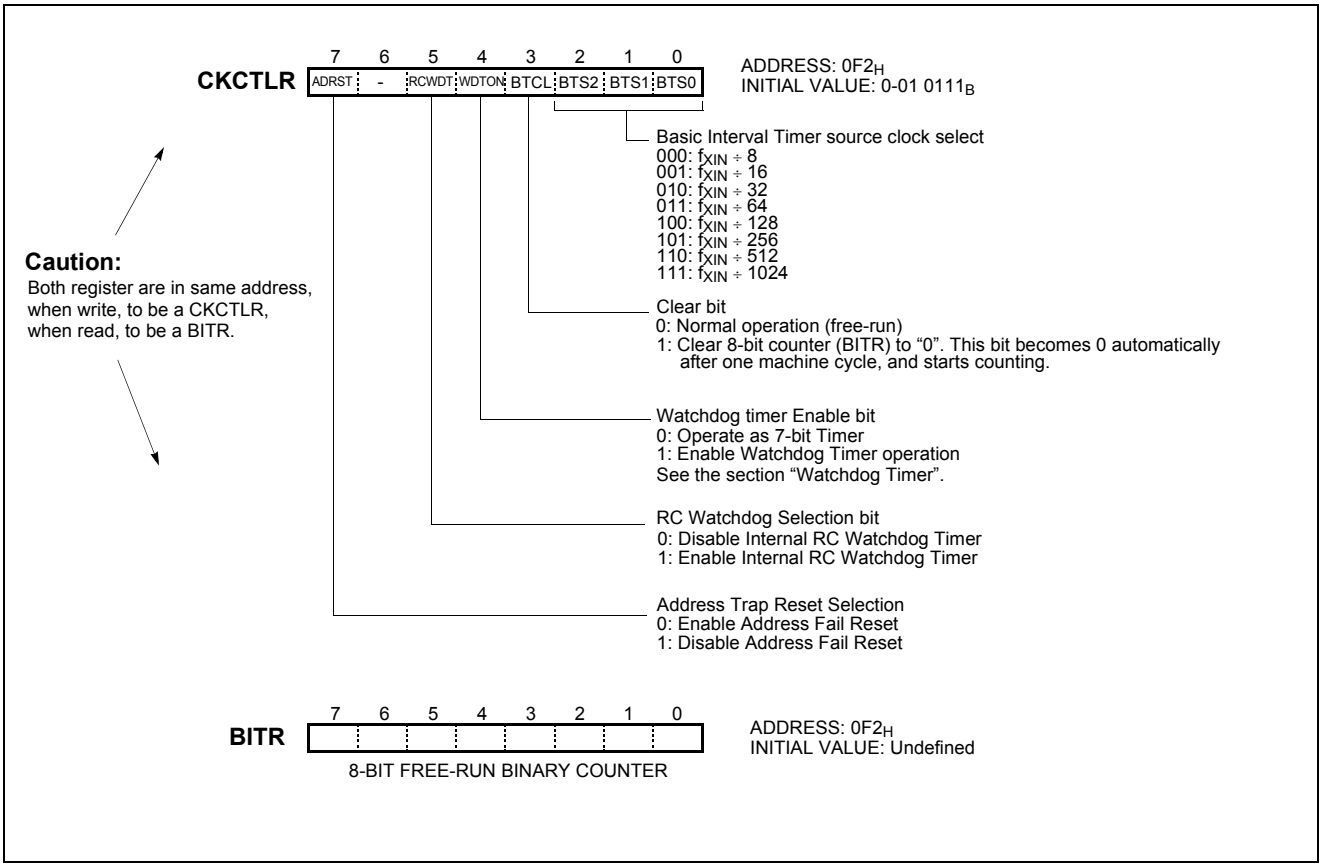


Figure 11-2 BITR: Basic Interval Timer Mode Register

Example 1:

Interrupt request flag is generated every 4.096ms at 4MHz.

```
:
LDM    CKCTLR,#1BH
SET1   BITE
EI
:
```

Example 2:

Interrupt request flag is generated every 4.096ms at 8MHz.

```
:
LDM    CKCTLR,#1CH
SET1   BITE
EI
:
```

time, selecting of output, and clearing of the binary counter. Clearing the binary counter is repeated within the detection time.

If the malfunction occurs for any cause, the watchdog timer output will become active at the rising overflow from the binary counters unless the binary counter is cleared. At this time, when WDTON=1, a reset is generated, which drives the $\overline{\text{RESET}}$ pin to low to reset the internal hardware. When WDTON=0, a watchdog timer interrupt (WDTIF) is generated. The WDTON bit is in register CLKCTLR.

The watchdog timer temporarily stops counting in the STOP mode, and when the STOP mode is released, it automatically restarts (continues counting).

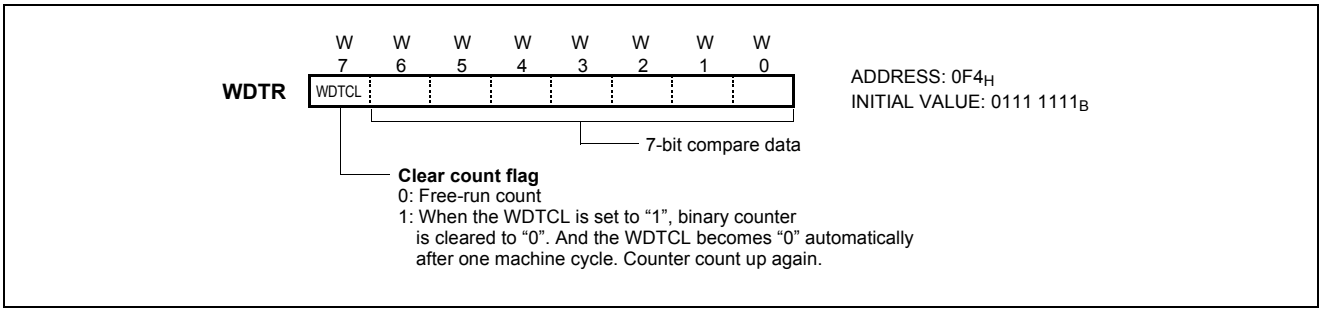


Figure 12-2 WDTR: Watchdog Timer Control Register

Example: Sets the watchdog timer detection time to 1 sec. at 4.194304MHz

```
LDM    CKCTLR,#3FH ;Select 1/1024 clock source,  WDTON ← 1, Clear Counter
LDM    WDTR,#08FH

LDM    WDTR,#08FH ;Clear counter
:
Within WDT
detection time
:
LDM    WDTR,#08FH  ;Clear counter
:
Within WDT
detection time
:
LDM    WDTR,#08FH  ;Clear counter
```

Enable and Disable Watchdog

Watchdog timer is enabled by setting WDTON (bit 4 in CKCTLR) to "1". WDTON is initialized to "0" during reset and it should be set to "1" to operate after reset is released.

Example: Enables watchdog timer for Reset

```
:
LDM    CKCTLR,#xxx1_xxxxB;WDTON ← 1
:
:
```

The watchdog timer is disabled by clearing bit 4 (WDTON) of CKCTLR. The watchdog timer is halted in STOP mode and restarts automatically after STOP mode is released.

Watchdog Timer Interrupt

The watchdog timer can be also used as a simple 7-bit timer by clearing bit4 of CKCTLR to "0". The interval of watchdog timer interrupt is decided by Basic Interval Timer. Interval equation is shown as below.

$$T_{WDT} = (WDTR+1) \times Interval\ of\ BIT$$

The stack pointer (SP) should be initialized before using the watchdog timer output as an interrupt source.

Example: 7-bit timer interrupt set up.

```
LDM    CKCTLR,#xxx0_xxxxB;WDTON ←0
LDM    WDTR,#8FH    ;WDTCL ←1

:
```

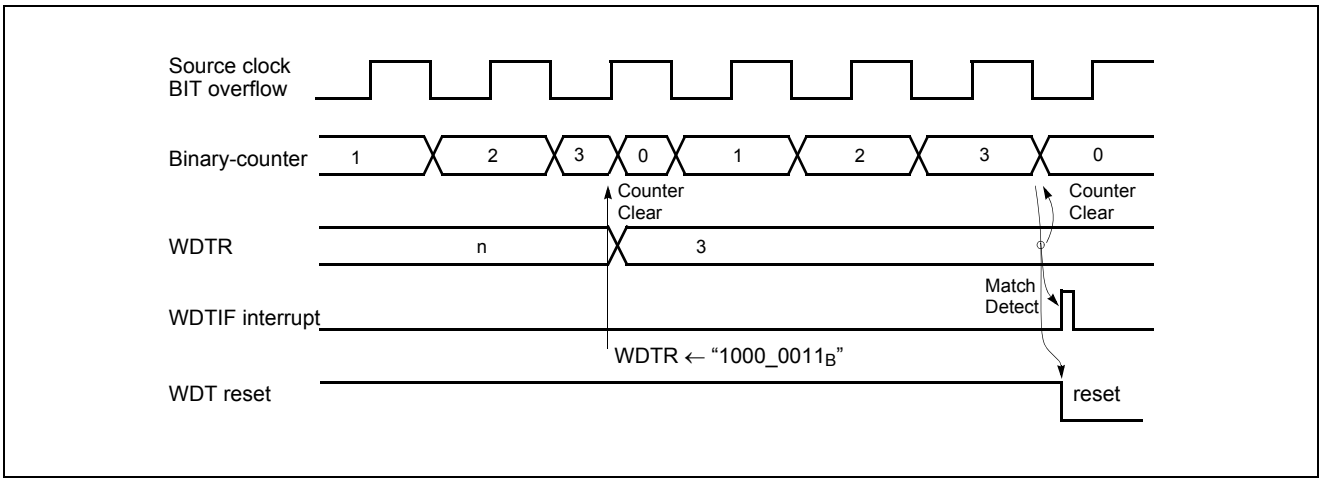


Figure 12-3 Watchdog timer Timing

If the watchdog timer output becomes active, a reset is generated, which drives the $\overline{\text{RESET}}$ pin low to reset the internal hardware.

The main clock oscillator also turns on when a watchdog timer reset is generated in sub clock mode.

TM0

		R/W 5	R/W 4	R/W 3	R/W 2	R/W 1	R/W 0
-	-	CAP0	T0CK2	T0CK1	T0CK0	T0CN	T0ST

ADDRESS: $0D0_H$
INITIAL VALUE: $--00\ 0000_B$

Bit Name	Bit Position	Description
CAP0	TM0.5	0: Timer/Counter mode 1: Capture mode selection flag
T0CK2 T0CK1 T0CK0	TM0.4 TM0.3 TM0.2	000: 8-bit Timer, Clock source is $f_{XIN} \div 2$ 001: 8-bit Timer, Clock source is $f_{XIN} \div 4$ 010: 8-bit Timer, Clock source is $f_{XIN} \div 8$ 011: 8-bit Timer, Clock source is $f_{XIN} \div 32$ 100: 8-bit Timer, Clock source is $f_{XIN} \div 128$ 101: 8-bit Timer, Clock source is $f_{XIN} \div 512$ 110: 8-bit Timer, Clock source is $f_{XIN} \div 2048$ 111: EC0 (External clock)
T0CN	TM0.1	0: Timer count pause 1: Timer count start
T0ST	TM0.0	0: When cleared, stop the counting. 1: When set, Timer 0 Count Register is cleared and start again.

TM1

R/W 7	R/W 6	R/W 5	R/W 4	R/W 3	R/W 2	R/W 1	R/W 0
POL	16BIT	PWM1E	CAP1	T1CK1	T1CK0	T1CN	T1ST

ADDRESS: $0D2_H$
INITIAL VALUE: 00_H

Bit Name	Bit Position	Description
POL	TM1.7	0: PWM Duty Active Low 1: PWM Duty Active High
16BIT	TM1.6	0: 8-bit Mode 1: 16-bit Mode
PWM1E	TM1.5	0: Disable PWM 1: Enable PWM
CAP1	TM1.4	0: Timer/Counter mode 1: Capture mode selection flag
T1CK1 T1CK0	TM1.3 TM1.2	00: 8-bit Timer, Clock source is f_{XIN} 01: 8-bit Timer, Clock source is $f_{XIN} \div 2$ 10: 8-bit Timer, Clock source is $f_{XIN} \div 8$ 11: 8-bit Timer, Clock source is Using the Timer 0 Clock
T1CN	TM1.1	0: Timer count pause 1: Timer count start
T1ST	TM1.0	0: When cleared, stop the counting. 1: When set, Timer 0 Count Register is cleared and start again.

TDR0

R/W 7	R/W 6	R/W 5	R/W 4	R/W 3	R/W 2	R/W 1	R/W 0

ADDRESS: $0D1_H$
INITIAL VALUE: $0FF_H$

TDR1

R/W 7	R/W 6	R/W 5	R/W 4	R/W 3	R/W 2	R/W 1	R/W 0

ADDRESS: $0D3_H$
INITIAL VALUE: $0FF_H$

Read: Count value read
Write: Compare data write

Figure 13-1 TM0, TM1 Registers

TM2

		R/W 5	R/W 4	R/W 3	R/W 2	R/W 1	R/W 0
-	-	CAP2	T2CK2	T2CK1	T2CK0	T2CN	T2ST

ADDRESS: $0D6_H$
INITIAL VALUE: $--00\ 0000_B$

Bit Name	Bit Position	Description
CAP2	TM2.5	0: Timer/Counter mode 1: Capture mode selection flag
T2CK2 T2CK1 T2CK0	TM2.4 TM2.3 TM2.2	000: 8-bit Timer, Clock source is $f_{XIN} \div 2$ 001: 8-bit Timer, Clock source is $f_{XIN} \div 4$ 010: 8-bit Timer, Clock source is $f_{XIN} \div 8$ 011: 8-bit Timer, Clock source is $f_{XIN} \div 16$ 100: 8-bit Timer, Clock source is $f_{XIN} \div 64$ 101: 8-bit Timer, Clock source is $f_{XIN} \div 256$ 110: 8-bit Timer, Clock source is $f_{XIN} \div 1024$ 111: EC1 (External clock)
T2CN	TM2.1	0: Timer count pause 1: Timer count start
T2ST	TM2.0	0: When cleared, stop the counting. 1: When set, Timer 0 Count Register is cleared and start again.

TM3

R/W 7	R/W 6	R/W 5	R/W 4	R/W 3	R/W 2	R/W 1	R/W 0
POL	16BIT	PWM3E	CAP3	T3CK1	T3CK0	T3CN	T3ST

ADDRESS: $0D8_H$
INITIAL VALUE: 00_H

Bit Name	Bit Position	Description
POL	TM3.7	0: PWM Duty Active Low 1: PWM Duty Active High
16BIT	TM3.6	0: 8-bit Mode 1: 16-bit Mode
PWM3E	TM3.5	0: Disable PWM 1: Enable PWM
CAP3	TM3.4	0: Timer/Counter mode 1: Capture mode selection flag
T3CK1 T3CK0	TM3.3 TM3.2	00: 8-bit Timer, Clock source is f_{XIN} 01: 8-bit Timer, Clock source is $f_{XIN} \div 4$ 10: 8-bit Timer, Clock source is $f_{XIN} \div 16$ 11: 8-bit Timer, Clock source is Using the Timer 2 Clock
T3CN	TM3.1	0: Timer count pause 1: Timer count start
T3ST	TM3.0	0: When cleared, stop the counting. 1: When set, Timer 0 Count Register is cleared and start again.

TDR2

R/W 7	R/W 6	R/W 5	R/W 4	R/W 3	R/W 2	R/W 1	R/W 0

ADDRESS: $0D7_H$
INITIAL VALUE: $0FF_H$

TDR3

R/W 7	R/W 6	R/W 5	R/W 4	R/W 3	R/W 2	R/W 1	R/W 0

ADDRESS: $0D9_H$
INITIAL VALUE: $0FF_H$

Read: Count value read
Write: Compare data write

Figure 13-2 TM2, TM3 Registers

TM2

7	6	5	4	3	2	1	0
-	-	CAP2	T2CK2	T2CK1	T2CK0	T2CN	T2ST
-	-	0	X	X	X	X	X

ADDRESS: $0D6_H$
INITIAL VALUE: $--000000_B$

X means don't care

TM3

7	6	5	4	3	2	1	0
POL	16BIT	PWM3E	CAP3	T3CK1	T3CK0	T3CN	T3ST
X	0	0	0	X	X	X	X

ADDRESS: $0D8_H$
INITIAL VALUE: 00_H

X means don't care

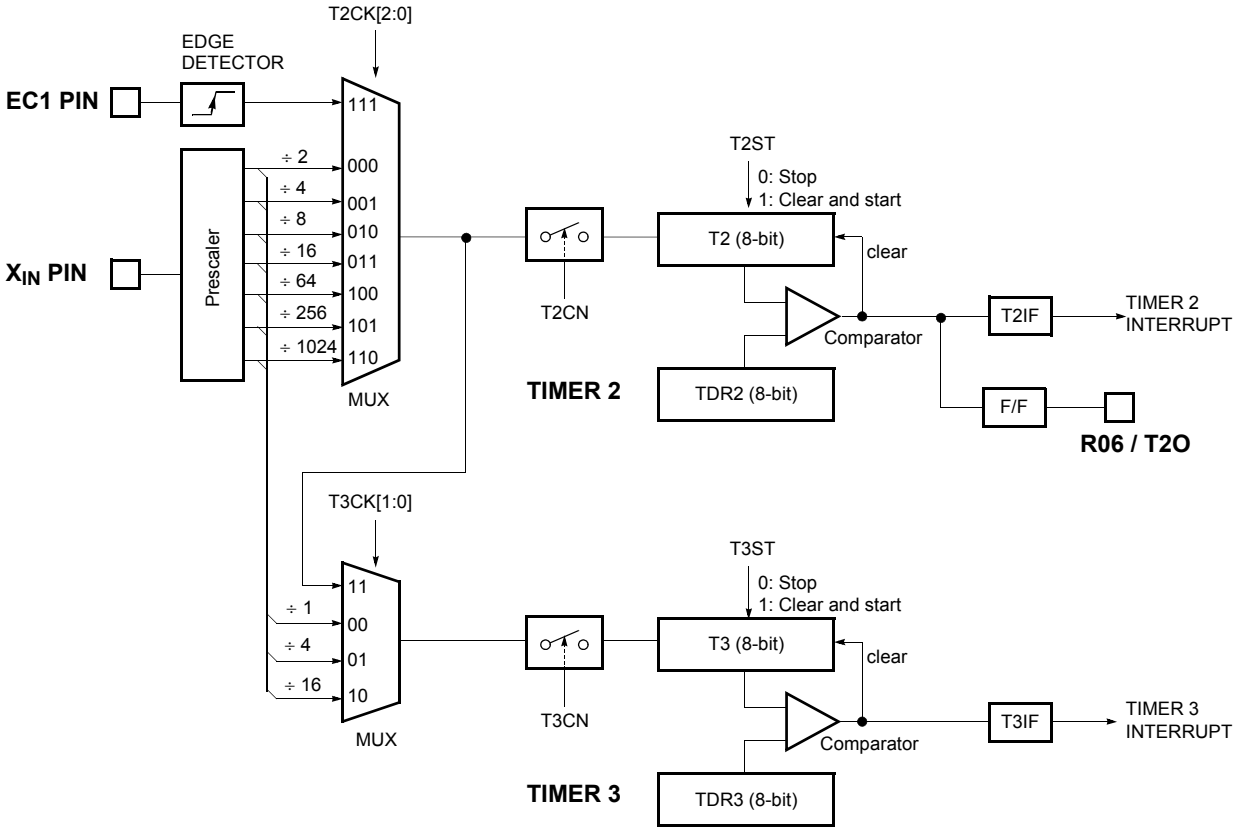


Figure 13-4 8-bit Timer/Counter 2, 3

Example 1:

Timer0 = 2ms 8-bit timer mode at 4MHz
Timer1 = 0.5ms 8-bit timer mode at 4MHz
Timer2 = 1ms 8-bit timer mode at 4MHz
Timer3 = 1ms 8-bit timer mode at 4MHz

```
LDM    TDR0,#249
LDM    TDR1,#249
LDM    TDR2,#249
LDM    TDR3,#249
LDM    TM0,#0000_1111B
LDM    TM1,#0000_1011B
LDM    TM2,#0000_1111B
LDM    TM3,#0000_1011B
SET1   T0E
SET1   T1E
SET1   T2E
SET1   T3E
EI
```

Example 2:

Timer0 = 8-bit event counter mode
Timer1 = 0.5ms 8-bit timer mode at 4MHz
Timer2 = 8-bit event counter mode
Timer3 = 1ms 8-bit timer mode at 4MHz

```
LDM    TDR0,#249
LDM    TDR1,#249
LDM    TDR2,#249
LDM    TDR3,#249
LDM    TM0,#0001_1111B
LDM    TM1,#0000_1011B
LDM    TM2,#0001_1111B
LDM    TM3,#0000_1011B
SET1   T0E
SET1   T1E
SET1   T2E
SET1   T3E
EI
```

These timers have each 8-bit count register and data register. The count register is increased by every internal or external clock input. The internal clock has a prescaler divide ratio option of 2, 4, 8, 32, 128, 512, 2048 selected by control bits T0CK[2:0] of register TM0 or 1, 2, 8 selected by control bits T1CK[1:0] of register TM1, or 2, 4, 8, 16, 64, 256, 1024 selected by control bits T2CK[2:0] of register TM2, or 1, 4, 16 selected by control bits T3CK[1:0] of register TM3. In the Timer 0, timer register T0 increases from 00_H until it matches TDR0 and then reset to 00_H. The match output of Timer 0 generates Timer 0 interrupt (latched in T0IF bit).

In counter function, the counter is increased every 0-to-1 (rising edge) transition of EC0 pin. In order to use counter function, the bit EC0 of the Port Selection Register (PSR0.4) is set to "1". The Timer 0 can be used as a counter by pin EC0 input, but Timer 1 can not. Likewise, In order to use Timer2 as counter function, the bit EC1 of the Port Selection Register (PSR0.5) is set to "1". The Timer 2 can be used as a counter by pin EC1 input, but Timer 3 can not.

8-bit Timer Mode

In the timer mode, the internal clock is used for counting up. Thus, you can think of it as counting internal clock input. The contents of TDR*n* are compared with the contents of up-counter, T*n*. If match is found, a timer *n* interrupt (T*n*IF) is generated and the up-counter is cleared to 0. Counting up is resumed after the up-counter is cleared.

As the value of TDR*n* is changeable by software, time interval is set as you want.

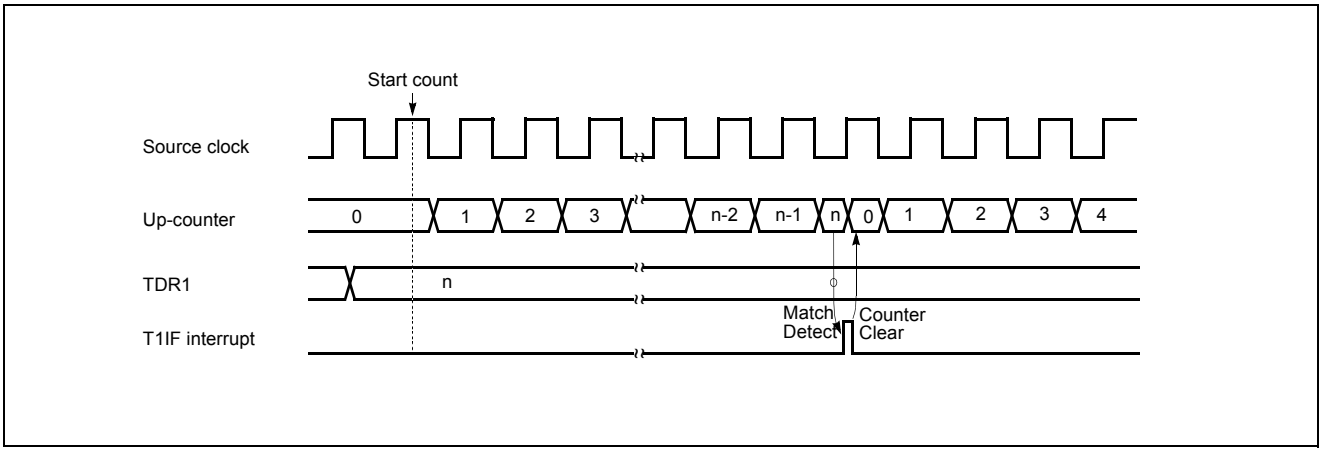


Figure 13-5 Timer Mode Timing Chart

Example: Make 1ms interrupt using by Timer0 at 4MHz

```
LDM    TM0,#0FH     ; divide by 32
LDM    TDR0,#124    ; 8us x (124+1)= 1ms
SET1   T0E          ; Enable Timer 0 Interrupt
EI                  ; Enable Master Interrupt
```

When
- TM0 = 0000 1111_B (8-bit Timer mode, Prescaler divide ratio = 32)
- TDR0 = 124_D = $7C_H$
- f_{XIN} = 4 MHz

$$\text{INTERRUPT PERIOD} = \frac{1}{4 \times 10^6\ \text{Hz}} \times 32 \times (124+1) = 1\ \text{ms}$$

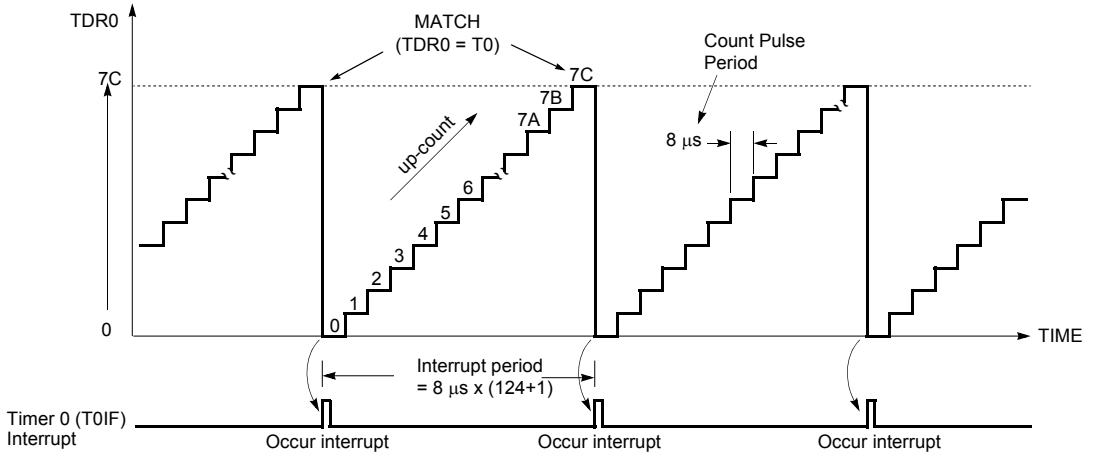


Figure 13-6 Timer Count Example

8-bit Event Counter Mode

In this mode, counting up is started by an external trigger. This trigger means rising edge of the EC0 or EC1 pin input. Source clock is used as an internal clock selected with timer mode register TM0 or TM2. The contents of timer data register TDR*n* (n = 0,1,2,3) are compared with the contents of the up-counter T*n*. If a match is found, an timer interrupt request flag T*n*IF is generated, and the counter is cleared to "0". The counter is restart and count up continuously by every rising edge of the EC0 or EC1 pin input. The maximum frequency applied to the EC0 or EC1 pin is f_{XIN}/2 [Hz].

In order to use event counter function, the bit 4, 5 of the Port Selection Register PSR0(address $0F8_H$) is required to be set to "1".

After reset, the value of timer data register TDR*n* is initialized to "0", The interval period of Timer is calculated as below equation.

$$\text{Period (sec)} = \frac{1}{f_{XIN}} \times 2 \times \text{Divide Ratio} \times (\text{TDRn} + 1)$$

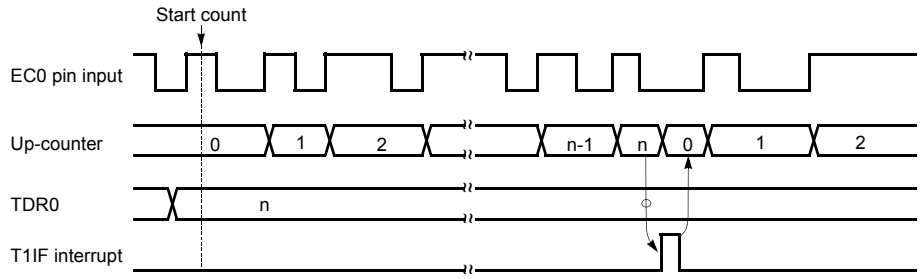


Figure 13-7 Event Counter Mode Timing Chart

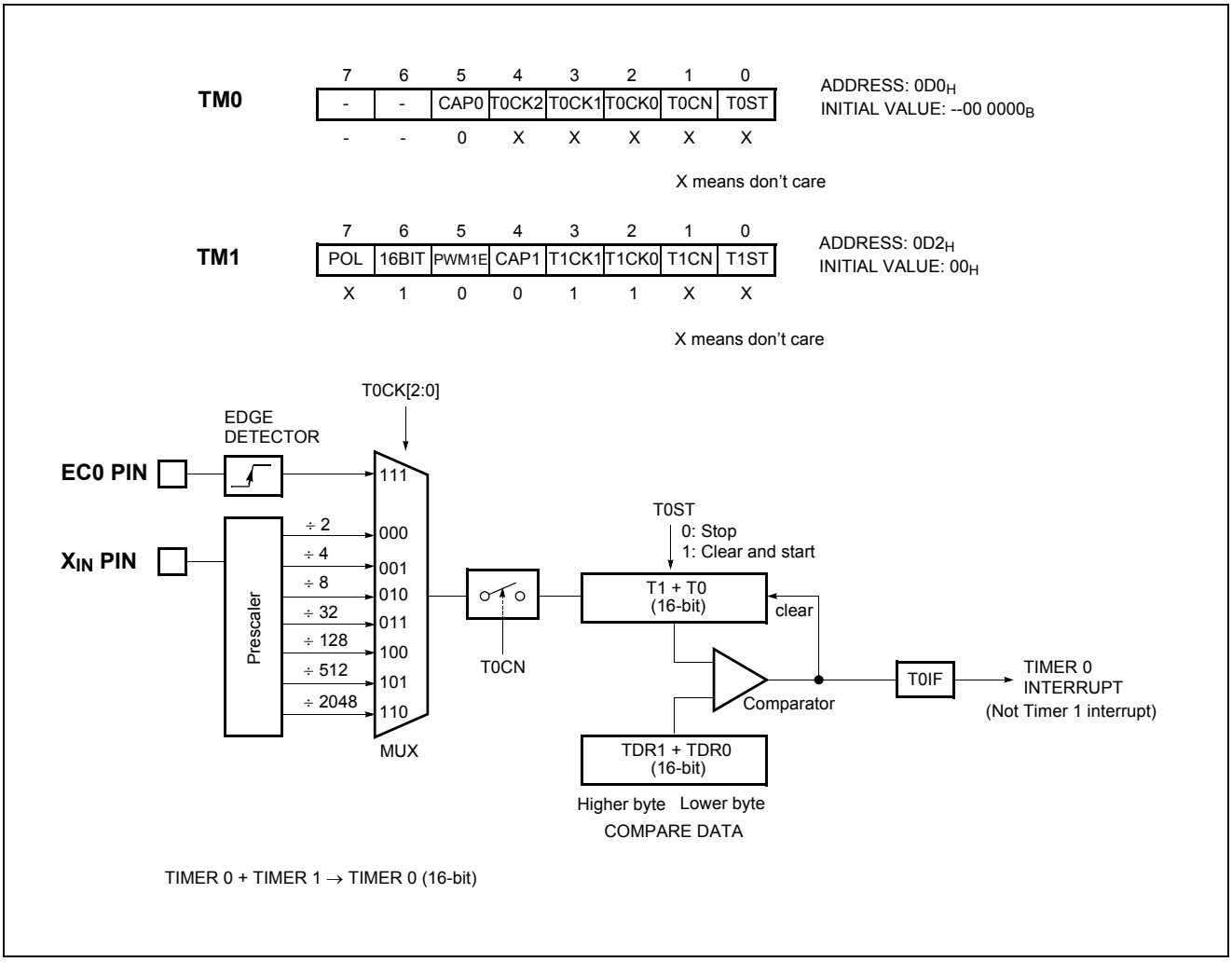


Figure 13-9 16-bit Timer/Counter for Timer 0, 1

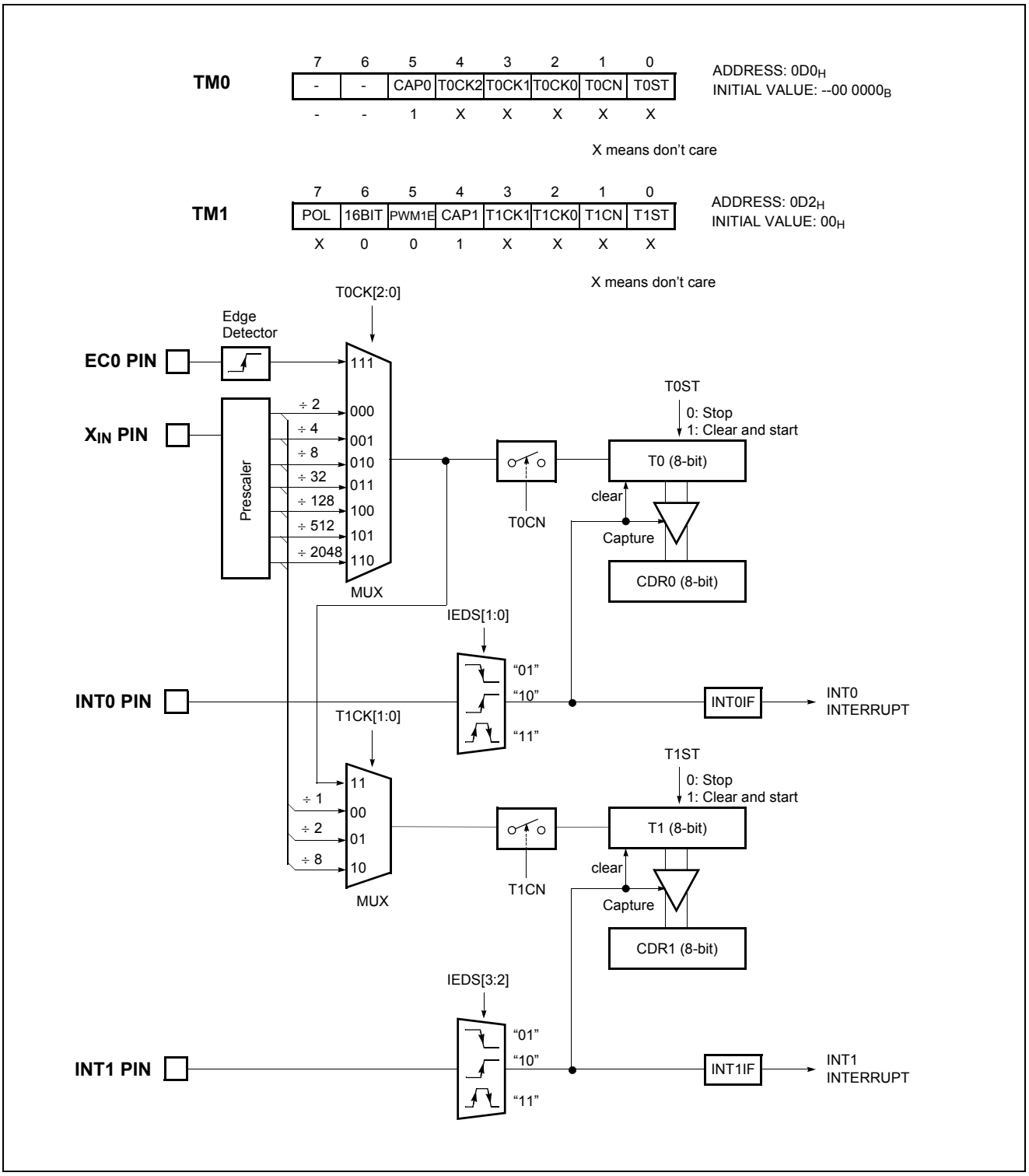


Figure 13-11 8-bit Capture Mode for Timer 0, 1

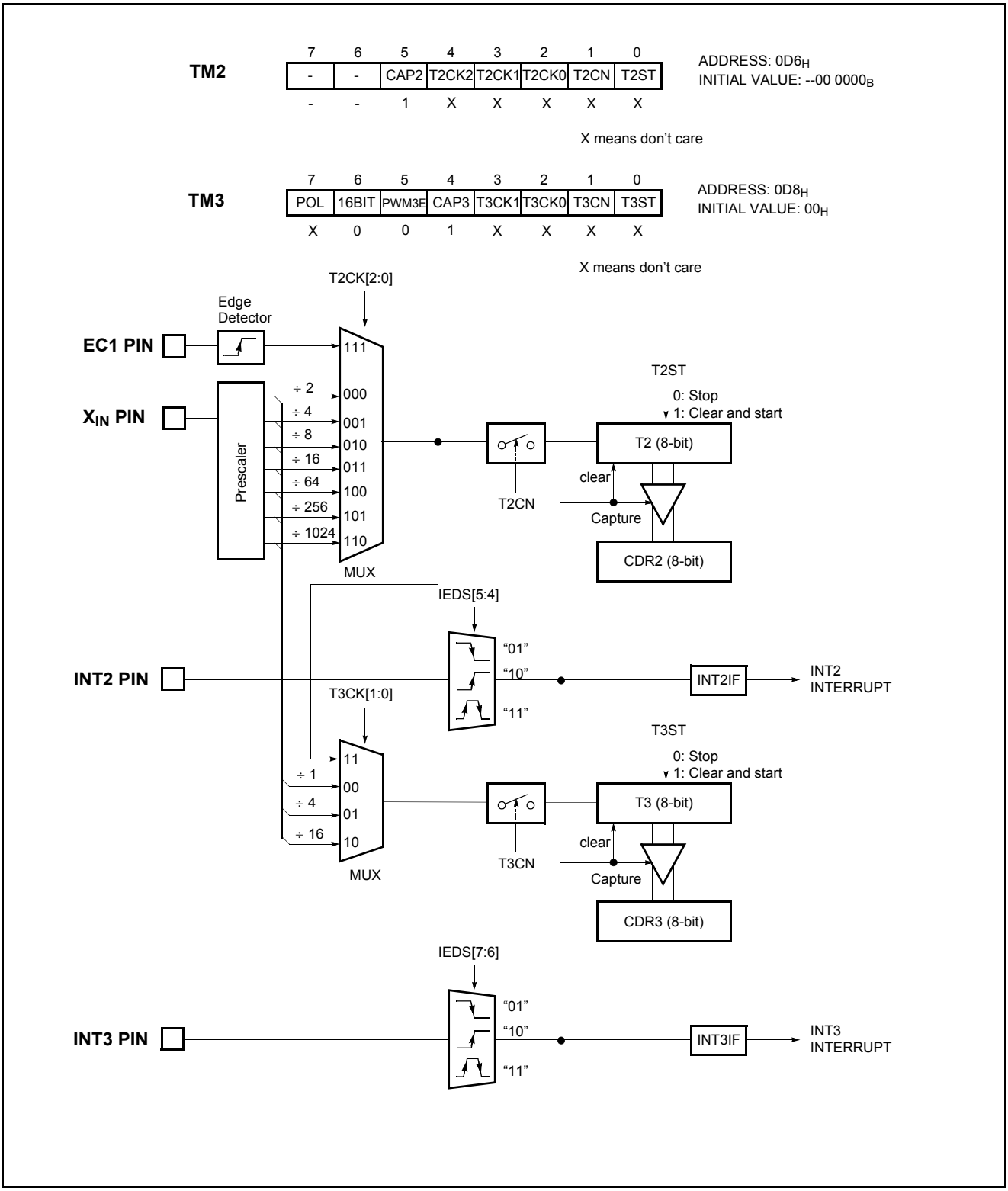


Figure 13-12 8-bit Capture Mode for Timer 2, 3

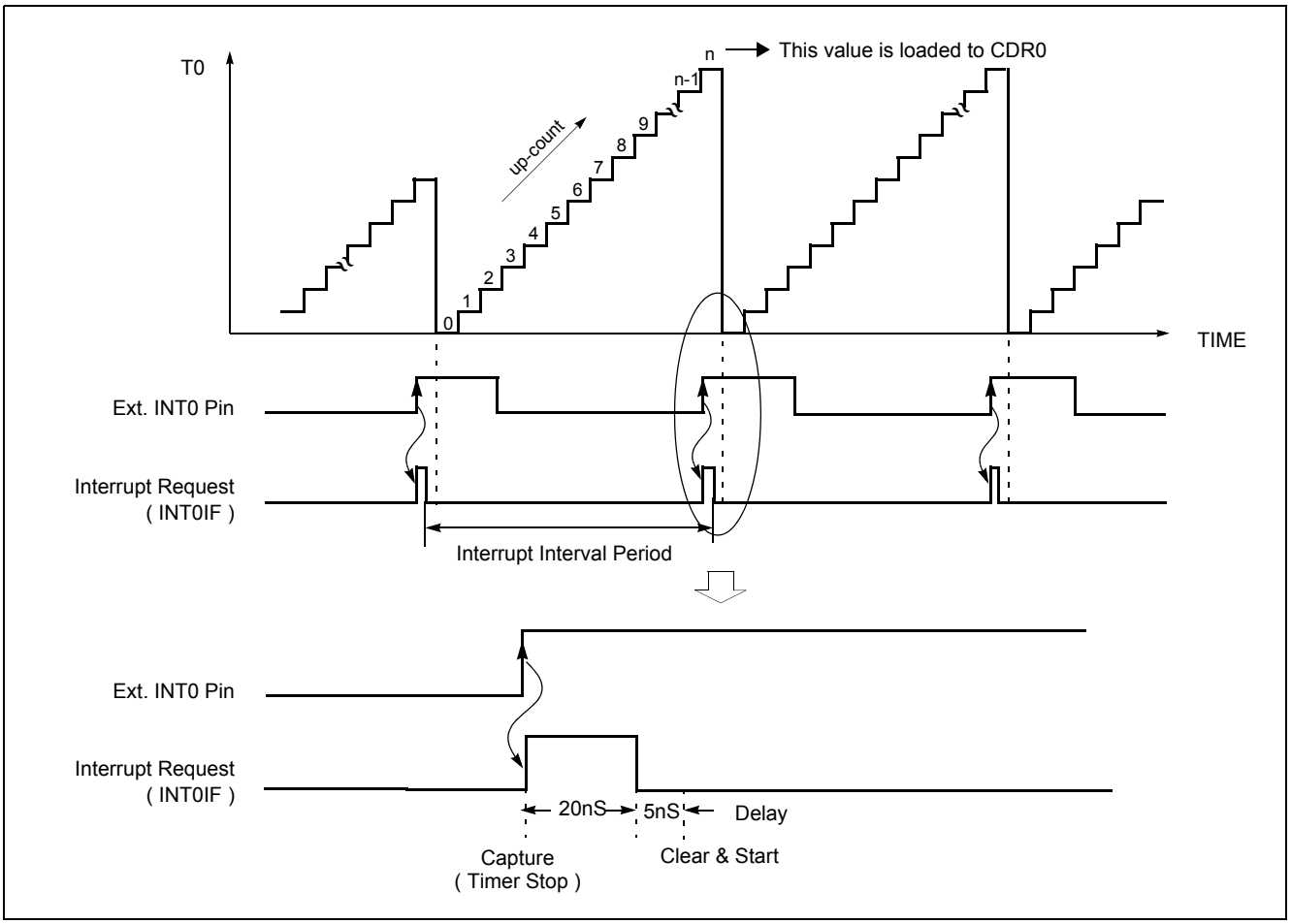


Figure 13-13 Input Capture Operation of Timer 0 Capture mode

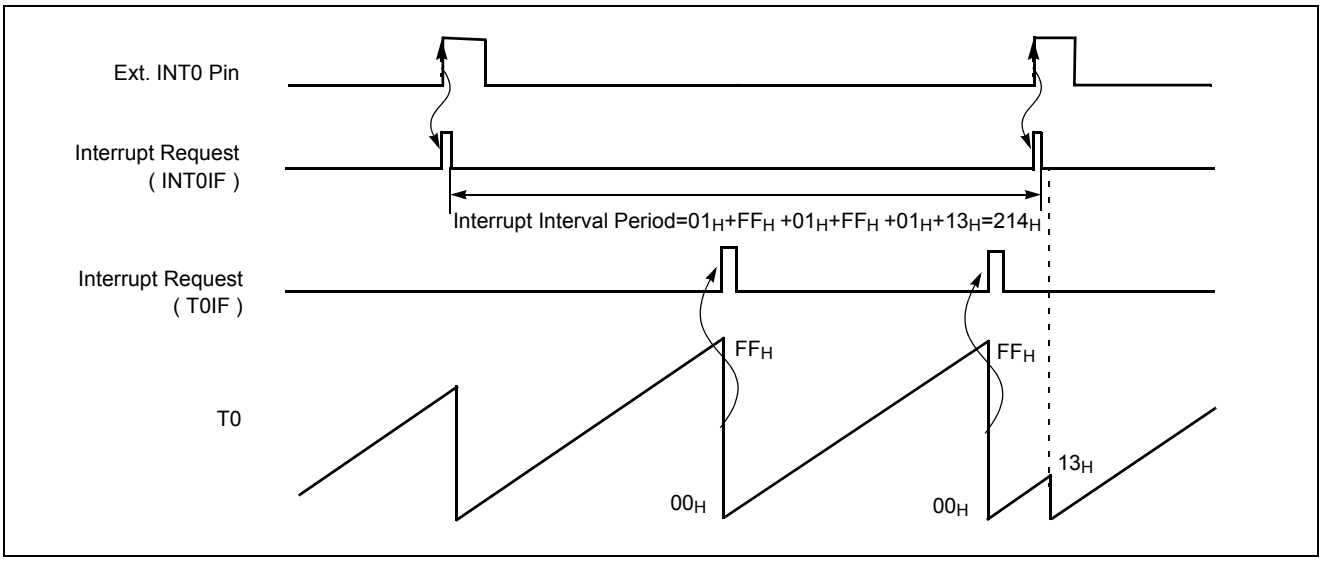


Figure 13-14 Excess Timer Overflow in Capture Mode

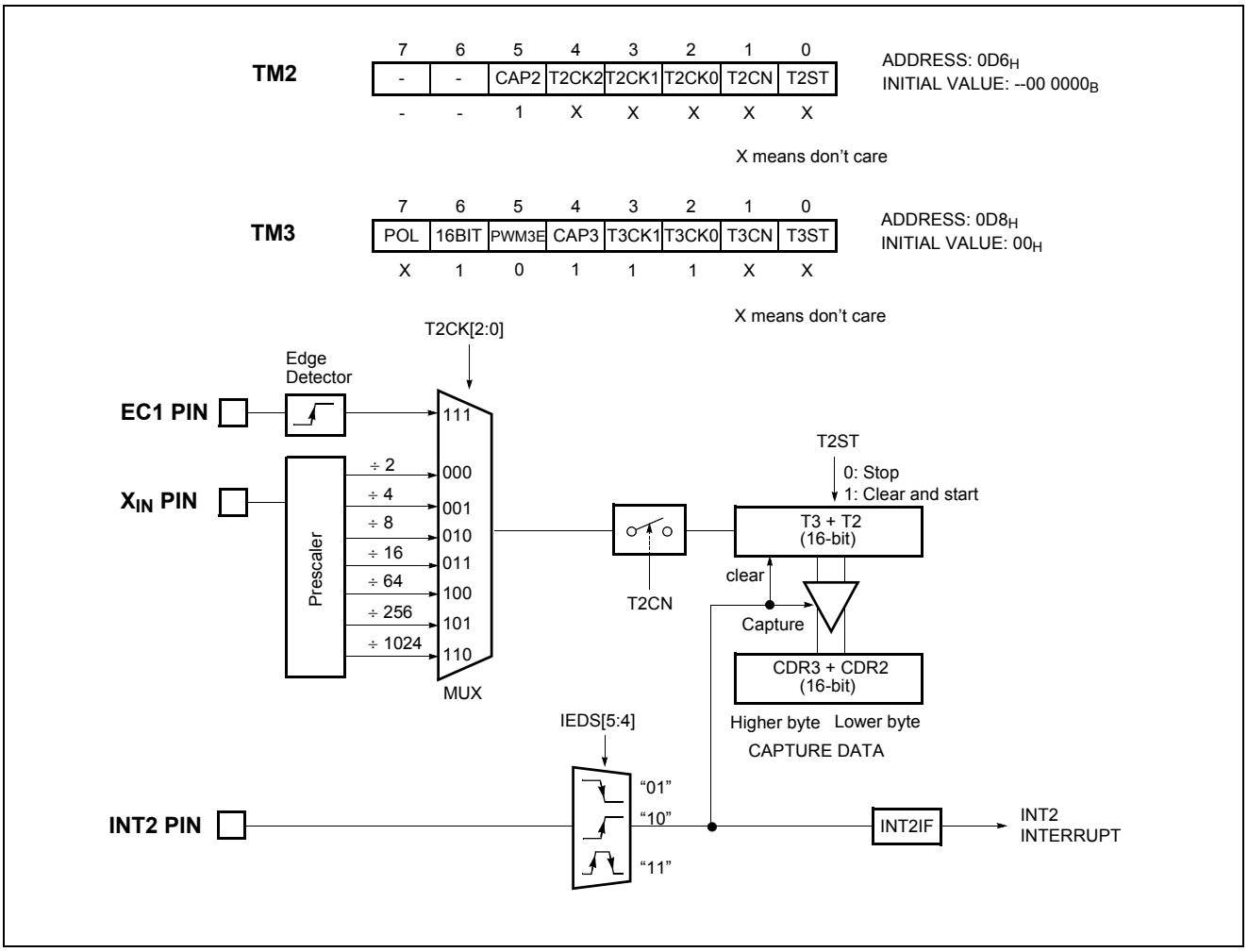


Figure 13-16 16-bit Capture Mode of Timer 2, 3

Example 1:

Timer0 = 16-bit timer mode, 0.5s at 4MHz

```
LDM    TM0,#0000_1111B;8uS
LDM    TM1,#0100_1100B;16bit Mode
LDM    TDR0,#<62499    ;8uS X 62500
LDM    TDR1,#>62499    ;=0.5s
SET1   T0E
EI
:
:
```

Example 2:

Timer0 = 16-bit event counter mode

```
LDM    PSR0,#0001_0000B;EC0 Set
LDM    TM0,#0001_1111B;CounterMode
LDM    TM1,#0100_1100B;16bit Mode
LDM    TDR0,#<0FFH     ;
LDM    TDR1,#>0FFH     ;
SET1   T0E
EI
:
:
```

Example 3:

Timer0 = 16-bit capture mode

```
LDM    PSR0,#0000_0001B;INT0 set
LDM    TM0,#0010_1111B;CaptureMode
LDM    TM1,#0100_1100B;16bit Mode
LDM    TDR0,#<0FFH     ;
LDM    TDR1,#>0FFH     ;
LDM    IEDS,#01H;Falling Edge
SET1   T0E
EI
:
:
```

TM1

R/W 7	R/W 6	R/W 5	R/W 4	R/W 3	R/W 2	R/W 1	R/W 0
POL	16BIT	PWM1E	CAP3	T1CK1	T1CK0	T1CN	T1ST
X	0	1	0	X	X	X	X

ADDRESS: $0D2_H$
INITIAL VALUE: 00_H

X:The value "0" or "1" corresponding your operation.

T1PWHR

- 7	- 6	- 5	- 4	W 3	W 2	W 1	W 0
-	-	-	-	T1PWHR3	T1PWHR2	T1PWHR1	T1PWHR0
-	-	-	-	X	X	X	X
				Period High		Duty High	

ADDRESS: $0D5_H$
INITIAL VALUE: ---- 0000_B
Bit Manipulation Not Available

X:The value "0" or "1" corresponding your operation.

T1PPR

W 7	W 6	W 5	W 4	W 3	W 2	W 1	W 0

ADDRESS: $0D3_H$
INITIAL VALUE: $0FF_H$

T1PDR

R/W 7	R/W 6	R/W 5	R/W 4	R/W 3	R/W 2	R/W 1	R/W 0

ADDRESS: $0D4_H$
INITIAL VALUE: 00_H

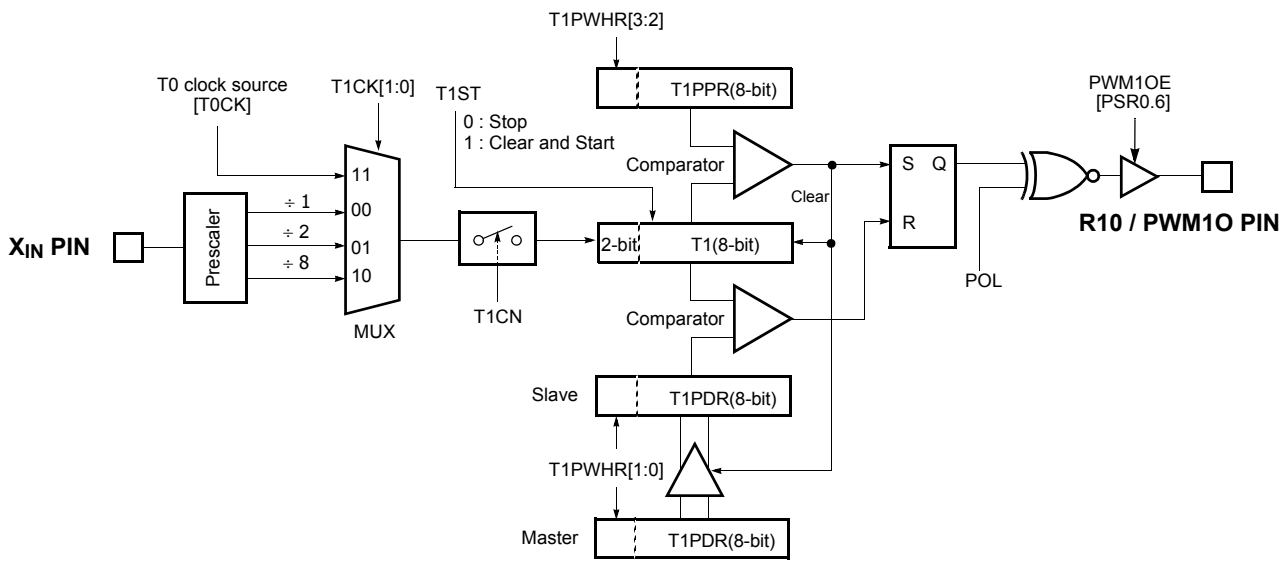


Figure 13-17 PWM1 Mode

TM3

R/W 7	R/W 6	R/W 5	R/W 4	R/W 3	R/W 2	R/W 1	R/W 0
POL	16BIT	PWM3E	CAP3	T3CK1	T3CK0	T3CN	T3ST
X	0	1	0	X	X	X	X

ADDRESS: $0D8_H$
INITIAL VALUE: 00_H

X:The value "0" or "1" corresponding your operation.

T3PWHR

- 7	- 6	- 5	- 4	W 3	W 2	W 1	W 0
-	-	-	-	T3PWHR3	T3PWHR2	T3PWHR1	T3PWHR0
-	-	-	-	X	X	X	X
				Period High		Duty High	

ADDRESS: $0DB_H$
INITIAL VALUE: ---- 0000_B
Bit Manipulation Not Available

X:The value "0" or "1" corresponding your operation.

T3PPR

W 7	W 6	W 5	W 4	W 3	W 2	W 1	W 0

ADDRESS: $0D9_H$
INITIAL VALUE: $0FF_H$

T3PDR

R/W 7	R/W 6	R/W 5	R/W 4	R/W 3	R/W 2	R/W 1	R/W 0

ADDRESS: $0DA_H$
INITIAL VALUE: 00_H

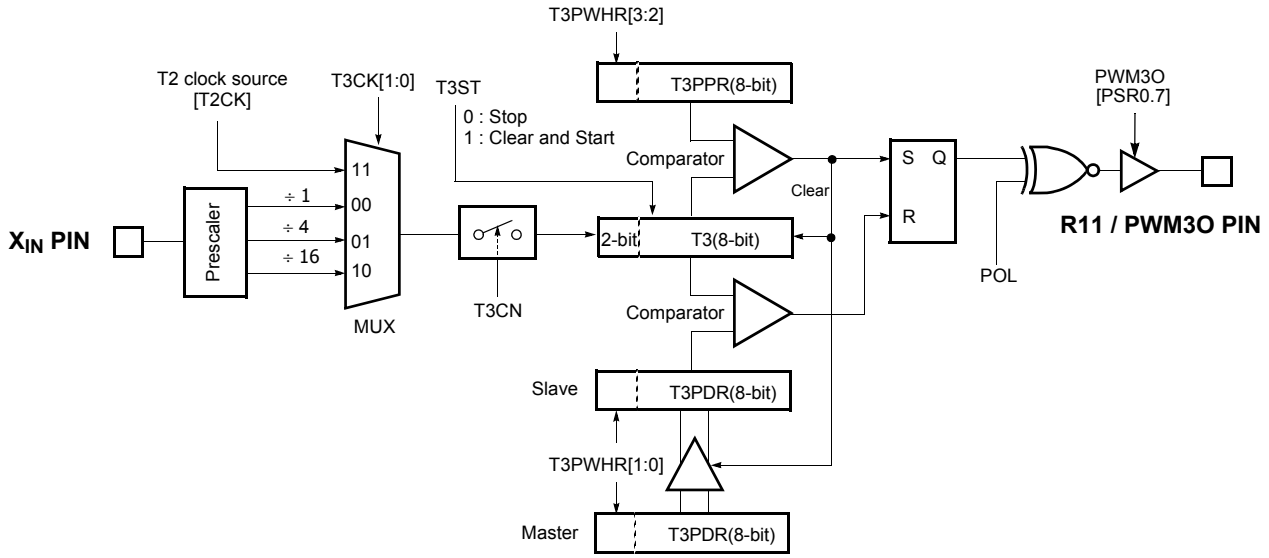


Figure 13-18 PWM3 Mode

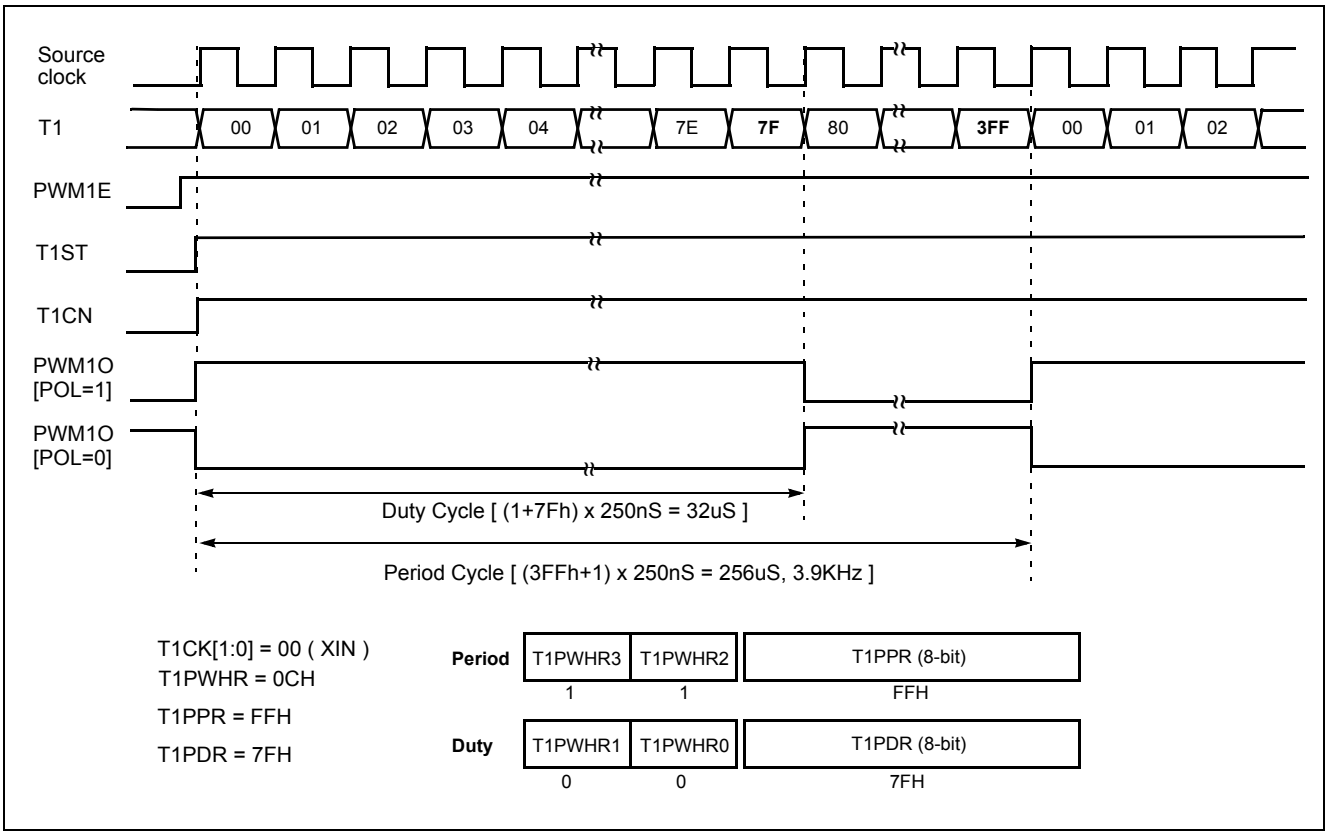


Figure 13-19 Example of PWM1 at 4MHz

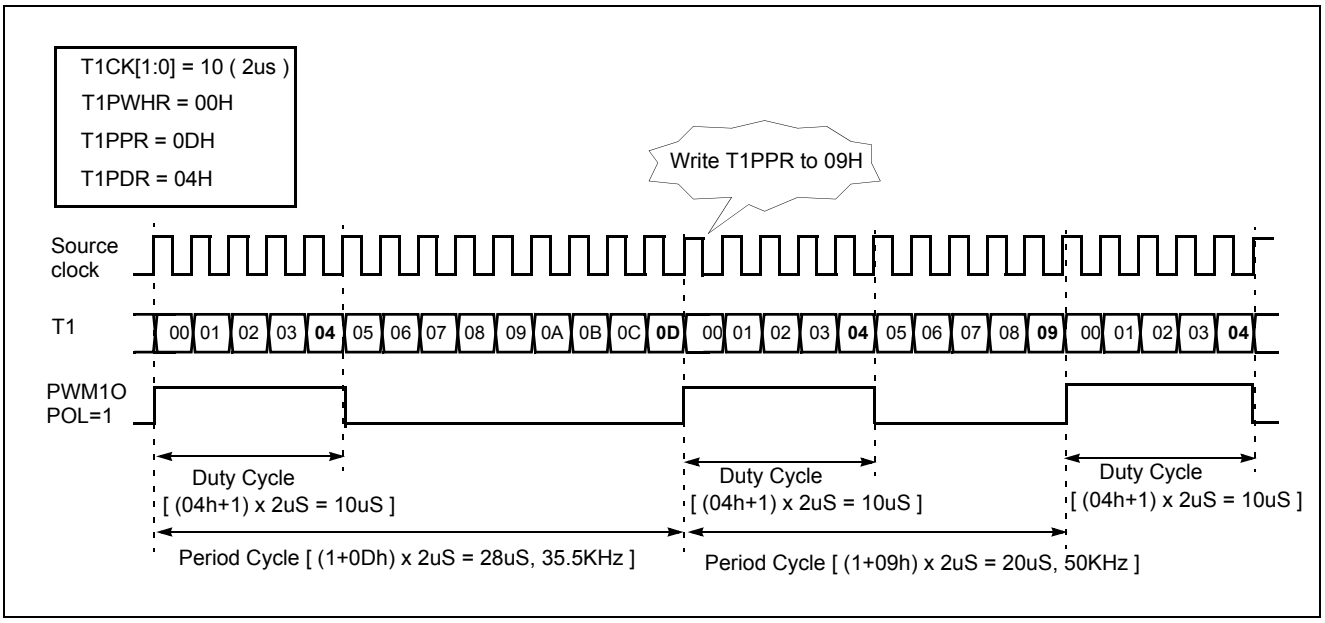
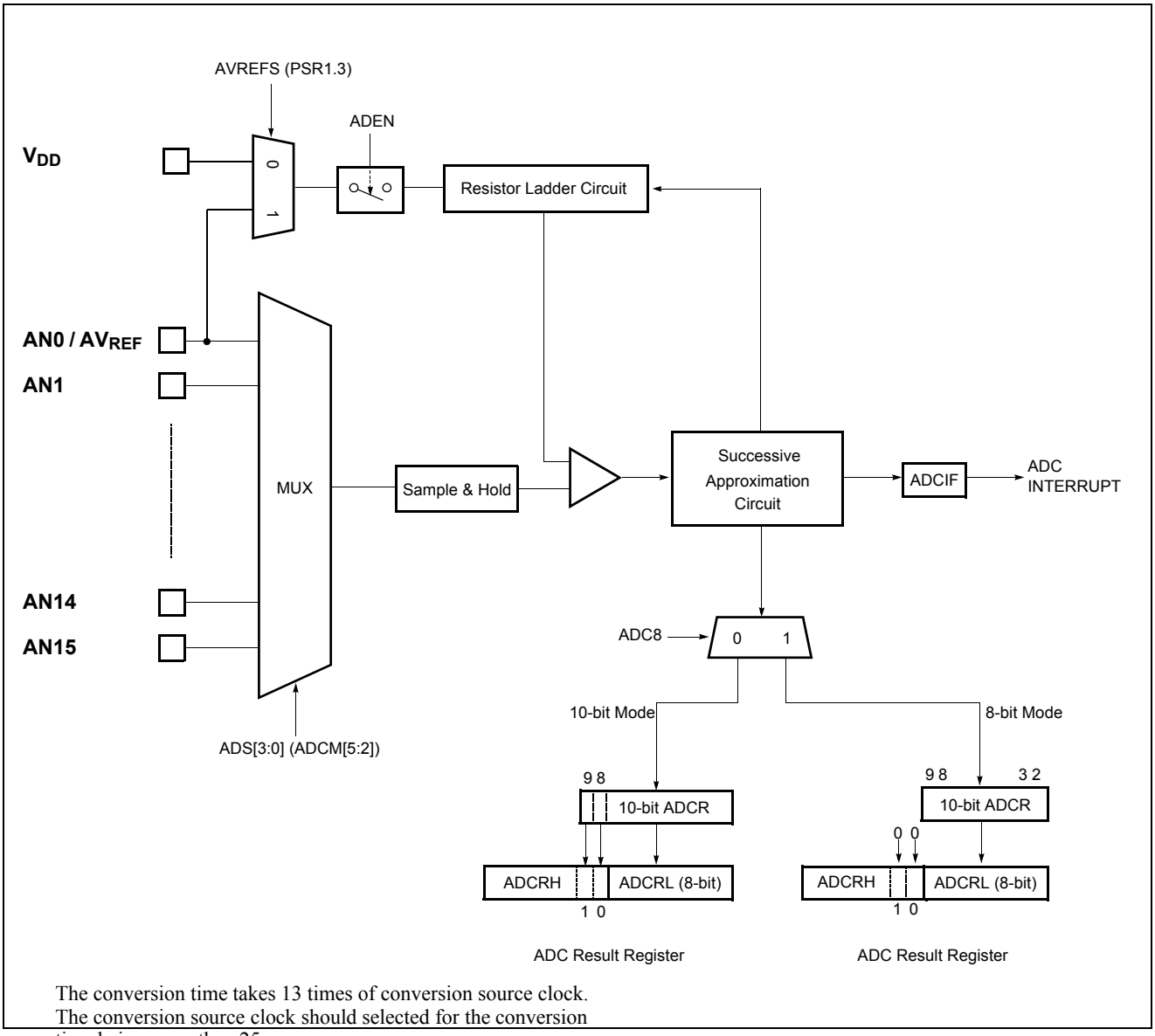


Figure 13-20 Example of Changing the PWM1 Period in Absolute Duty Cycle (@4MHz)

may not be obtainable due to coupling noise. Therefore, avoid applying pulses to pins adjacent to the pin undergoing A/D conversion.

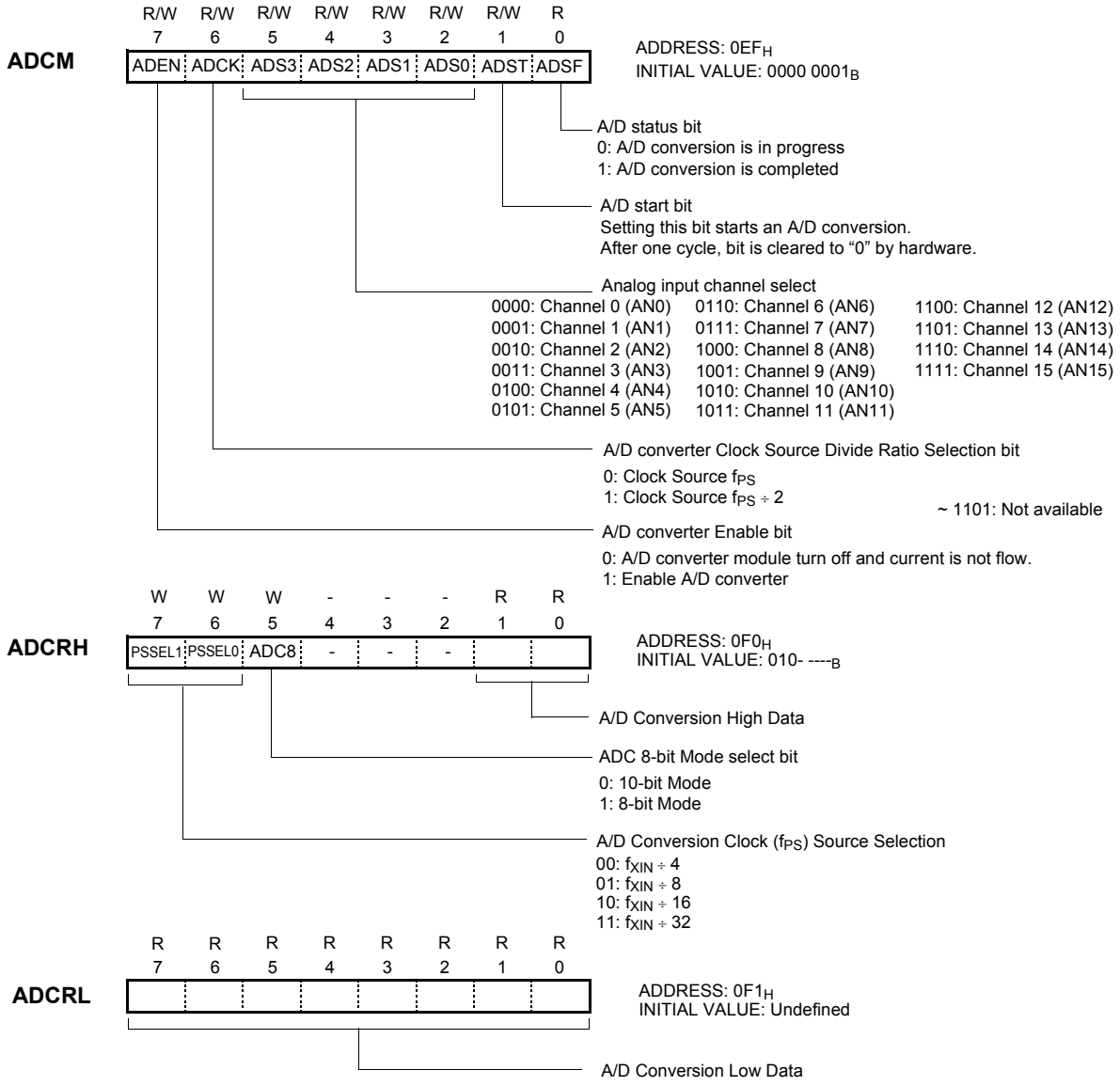
(4) AV_{DD} pin input impedance

A series resistor string of approximately 5KΩ is connected between the AV_{REF} pin and the V_{SS} pin. Therefore, if the output impedance of the analog power source is high, this will result in parallel connection to the series resistor string between the AV_{REF} pin and the V_{SS} pin, and there will be a large analog supply voltage error



The conversion time takes 13 times of conversion source clock.
The conversion source clock should selected for the conversion time being more than 25µs

Figure 14-3 A/D Block Diagram



ADCK	PSSEL1	PSSEL0	PS Clock Selection
0	0	0	PS = f_{XIN} ÷ 4
0	0	1	PS = f_{XIN} ÷ 8
0	1	0	PS = f_{XIN} ÷ 16
0	1	1	PS = f_{XIN} ÷ 32
1	0	0	PS = f_{XIN} ÷ 8
1	0	1	PS = f_{XIN} ÷ 16
1	1	0	PS = f_{XIN} ÷ 32
1	1	1	PS = f_{XIN} ÷ 64

PS : Conversion Source Clock

Conversion Time = T_{PS} x 13

* The conversion time takes 13 times of conversion source clock.
The conversion source clock should selected for the conversion time being more than 25µs.

Figure 14-4 A/D Converter Control & Result Register

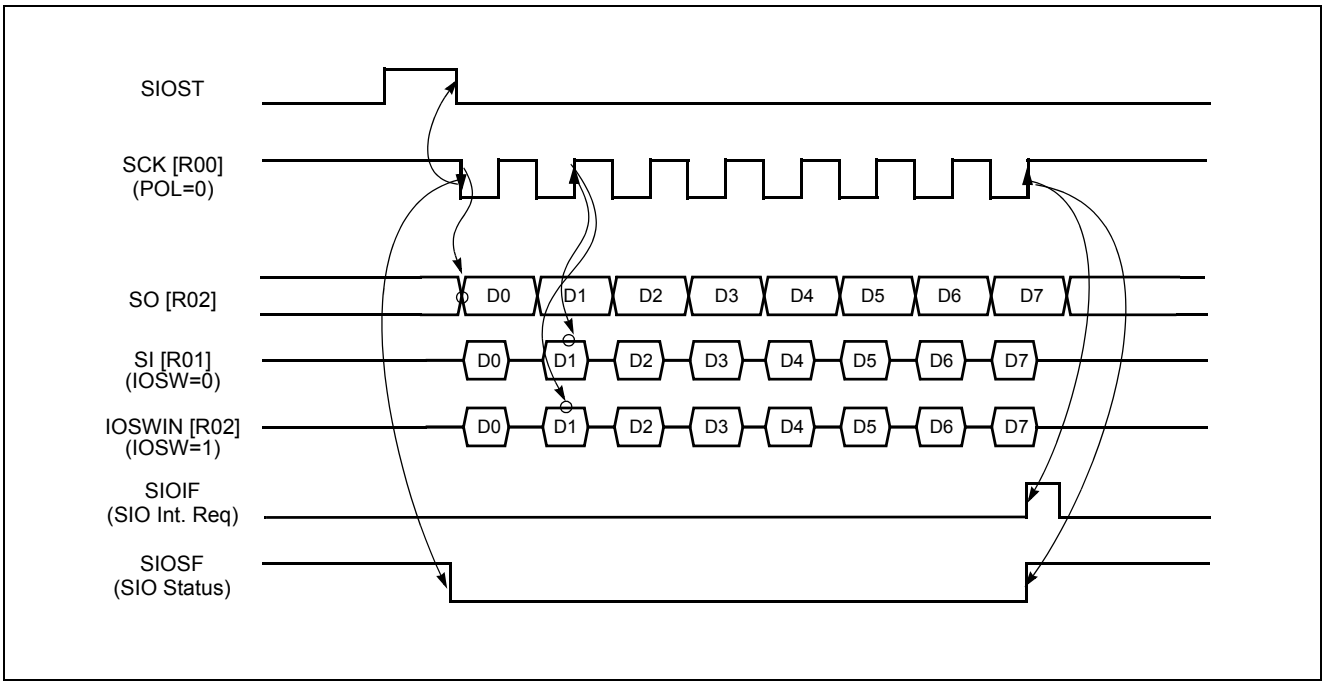


Figure 15-3 Serial I/O Timing Diagram at POL=0

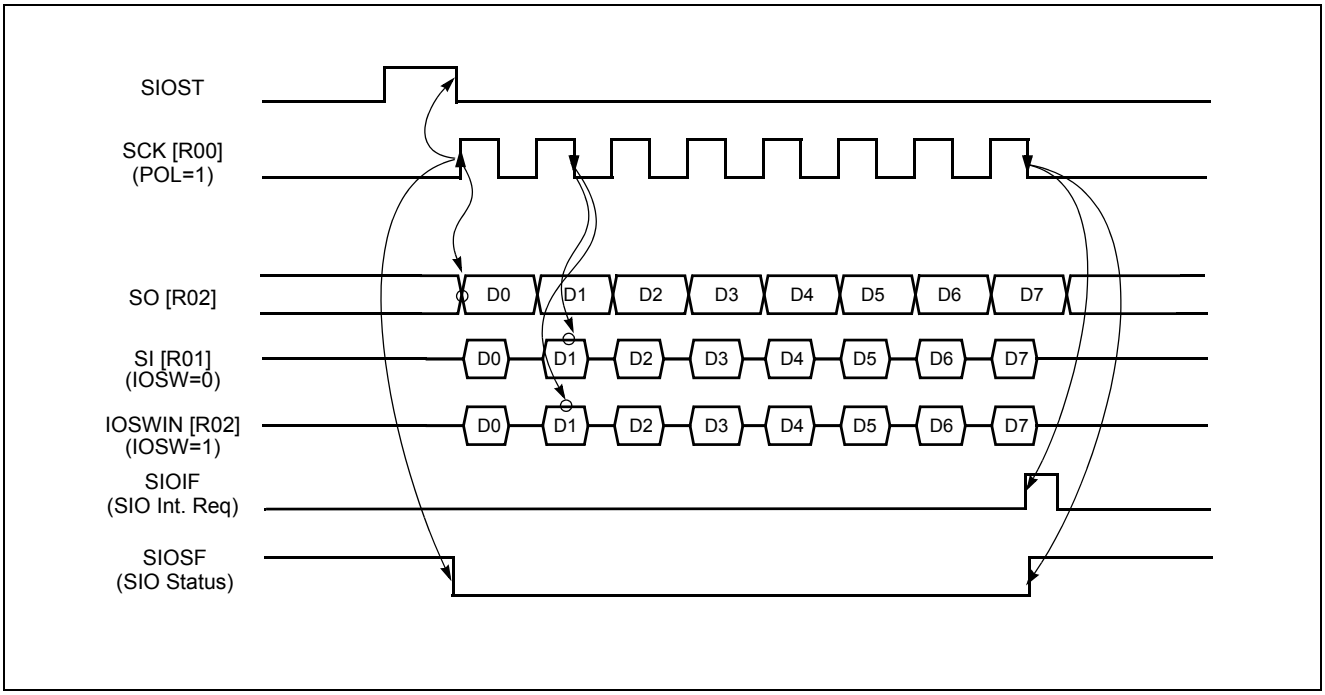


Figure 15-4 Serial I/O Timing Diagram at POL=1

15.2 The usage of Serial I/O

1. Select transmission/receiving mode.
2. In case of sending mode, write data to be send to SIOR.

3. Set SIOST to “1” to start serial transmission.
4. The SIO interrupt is generated at the completion of SIO and SIOIF is set to “1”.
5. In case of receiving mode, the received data is acquired by reading the SIOR.
6. When using polling method, the completion of 1 byte serial communication can be checked by reading SIOST and SIOSF. As shown in example code, wait until SIOST is changed to “0” and then wait the SIOSF is changed to “1” for completion check.

```
   LDM   SIOR,#0AAh       ;set tx data
   LDM   SIOM,#0011_1100b;set SIO mode
   NOP
   LDM   SIOM,#0011_1110b;SIO Start
   NOP
SIO_WAIT:
   NOP
   BBS   SIOST,SIO_WAIT  ;wait first edge
   BBC   SIOSF,SIO_WAIT  ;wait complete
```

Note: *When external clock is used, the frequency should be less than 1MHz and recommended duty is 50%. If both transmission mode is selected and transmission is performed simultaneously, error may be occur.*

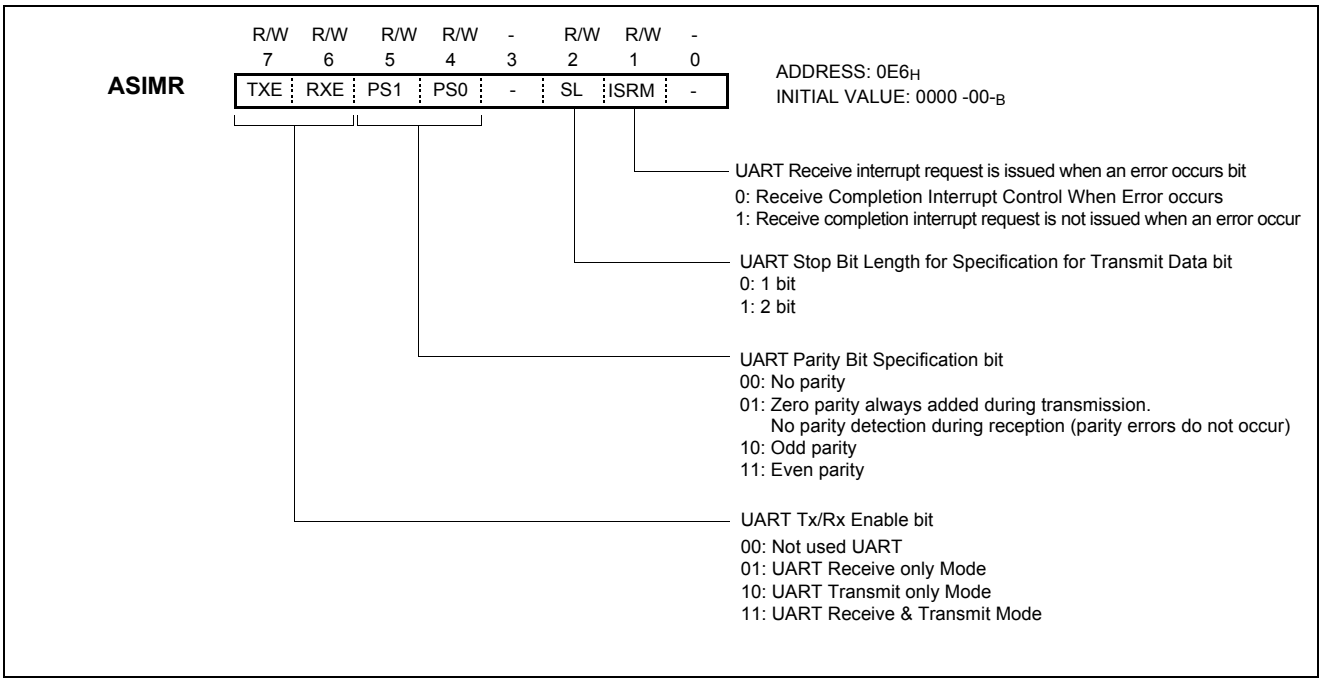


Figure 16-3 Asynchronous Serial Interface Mode register (ASIMR) Format

TXE (ASIMR.7)	RXE(ASIMR.6)	EC0(PSR0.4)	Operation Mode	RXD/R04	TXD/R05
0	0	X[1]	Operation Stop	R04	R05
0	1	0	UART mode (Receive only)	RXD	R05
1	0	X	UART mode (Transmit only)	R04	TXD
1	1	0	UART mode (Transmit and receive)	RXD	TXD

Table 16-2 UART mode and RXD/TXD pin function

1. X:The value "0" or "1" corresponding your operation

rupt request.

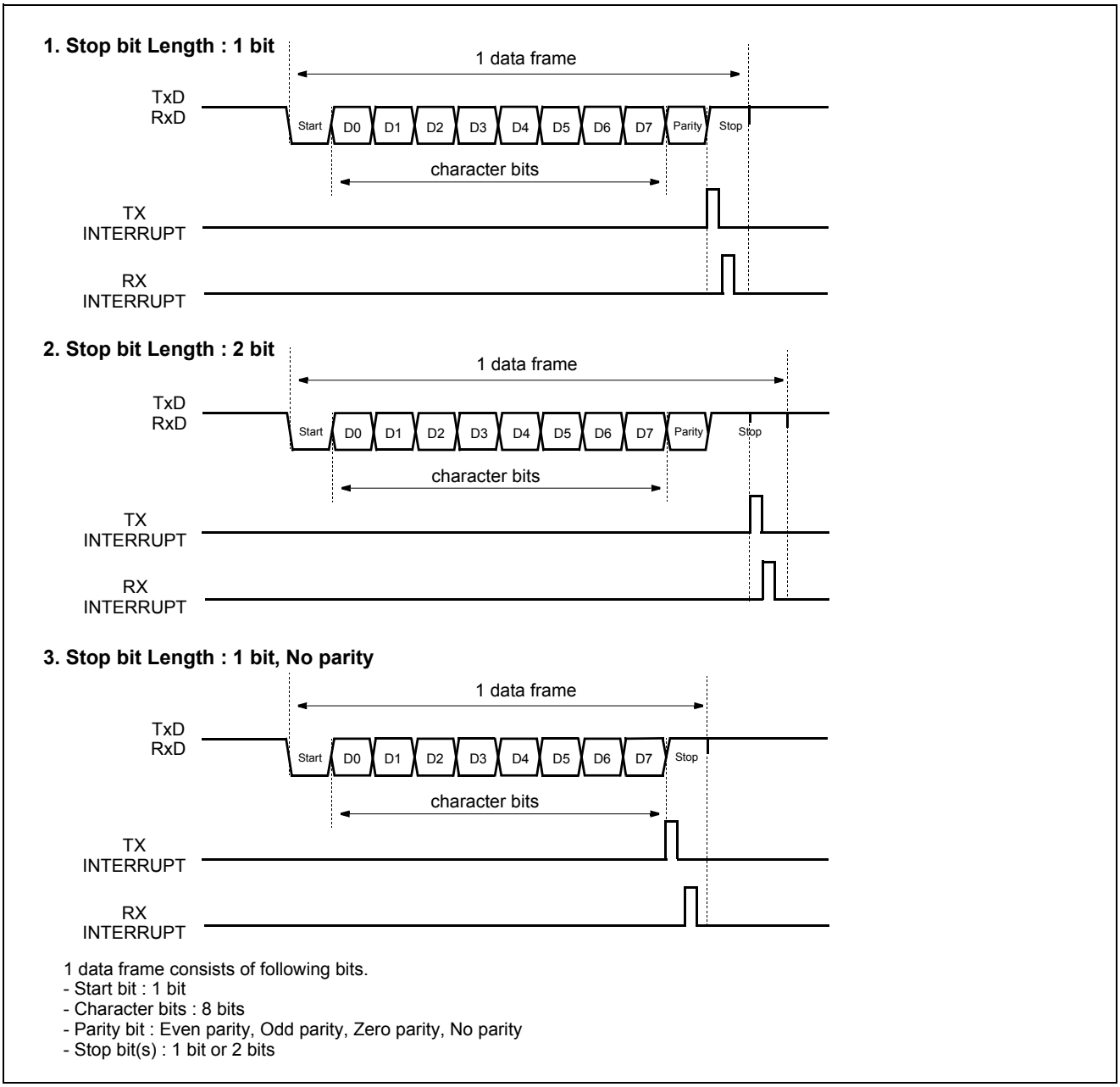


Figure 16-6 UART data format and interrupt timing diagram

16.4 Relationship between main clock and baud rate

The transmit/receive clock that is used to generate the baud rate is obtained by dividing the main system clock. Transmit/Receive clock generation for baud rate is made by using main system clock which is divided. The baud rate generated from the main

system clock is determined according to the following formula.

Baud Rate (bps)	f_{XIN}=11.0592M		f_{XIN}=10.0M		f_{XIN}=8.0M		f_{XIN}=4.0M		f_{XIN}=2.0M	
	BRGCR	ERR(%)	BRGCR	ERR(%)	BRGCR	ERR(%)	BRGCR	ERR (%)	BRGCR	ERR(%)
600	-	-	-	-	-	-	7AH	0.16	6AH	0.16
1200	-	-	-	-	7AH	0.16	6AH	0.16	5AH	0.16
2400	72H	0.00	70H	1.73	6AH	0.16	5AH	0.16	4AH	0.16
4800	62H	0.00	60H	1.73	5AH	0.16	4AH	0.16	3AH	0.16
9600	52H	0.00	50H	1.73	4AH	0.16	3AH	0.16	2AH	0.16
19200	42H	0.00	40H	1.73	3AH	0.16	2AH	0.16	1AH	0.16
31250	36H	0.53	34H	0.00	30H	0.00	20H	0.00	10H	0.00
38400	32H	0.00	30H	1.73	2AH	0.16	1AH	0.16	-	-
57600	28H	0.00	26H	1.35	21H	2.11	11H	2.12	-	-
76800	22H	0.00	20H	1.73	1AH	0.16	-	-	-	-
115200	18H	0.00	16H	1.36	11H	2.12	-	-	-	-

$$\text{Baud Rate} = f_{XIN} \div (2^{n+1}(k+16))$$

Remarks 1. f_{XIN} : Main system clock oscillation frequency
When ACLK is selected as the source clock of the 5-bit counter,
substitute the input clock frequency to ACLK pin for in the above expression.
2. f_{SCK} : Source clock for 5 bit counter
3. n : Value set via TPS0 to TPS2 ($0 \le n \le 7$)
4. k : Source clock for 5 bit counter ($0 \le k \le 14$)

Figure 16-7 Relationship between main clock and Baud Rate

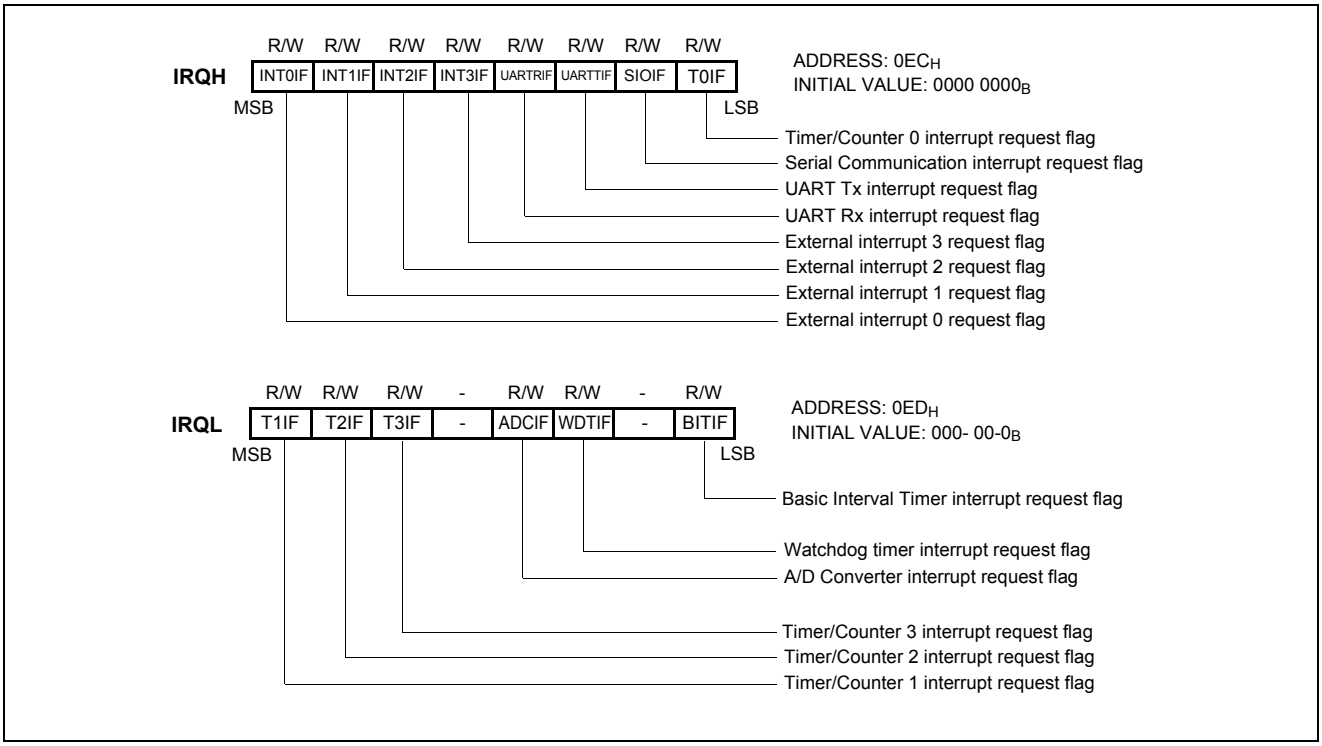


Figure 18-3 Interrupt Request Flag Register

18.1 Interrupt Sequence

An interrupt request is held until the interrupt is accepted or the interrupt latch is cleared to "0" by a reset or an instruction. Interrupt acceptance sequence requires 8 cycles of f_{XIN} (2µs at f_{XIN}=4MHz) after the completion of the current instruction execution. The interrupt service task is terminated upon execution of an interrupt return instruction [RETI].

Interrupt acceptance

1. The interrupt master enable flag (I-flag) is cleared to "0" to temporarily disable the acceptance of any following maskable interrupts. When a non-maskable interrupt is accepted, the acceptance of any following interrupts is temporarily disabled.
2. The contents of the program counter (return address) and the program status word are saved (pushed) onto the stack area. The stack pointer decreases 3 times.
3. The entry address of the interrupt service program is read from the vector table address and the entry address is loaded to the program counter.
4. The instruction stored at the entry address of the inter-

rupt service program is executed.

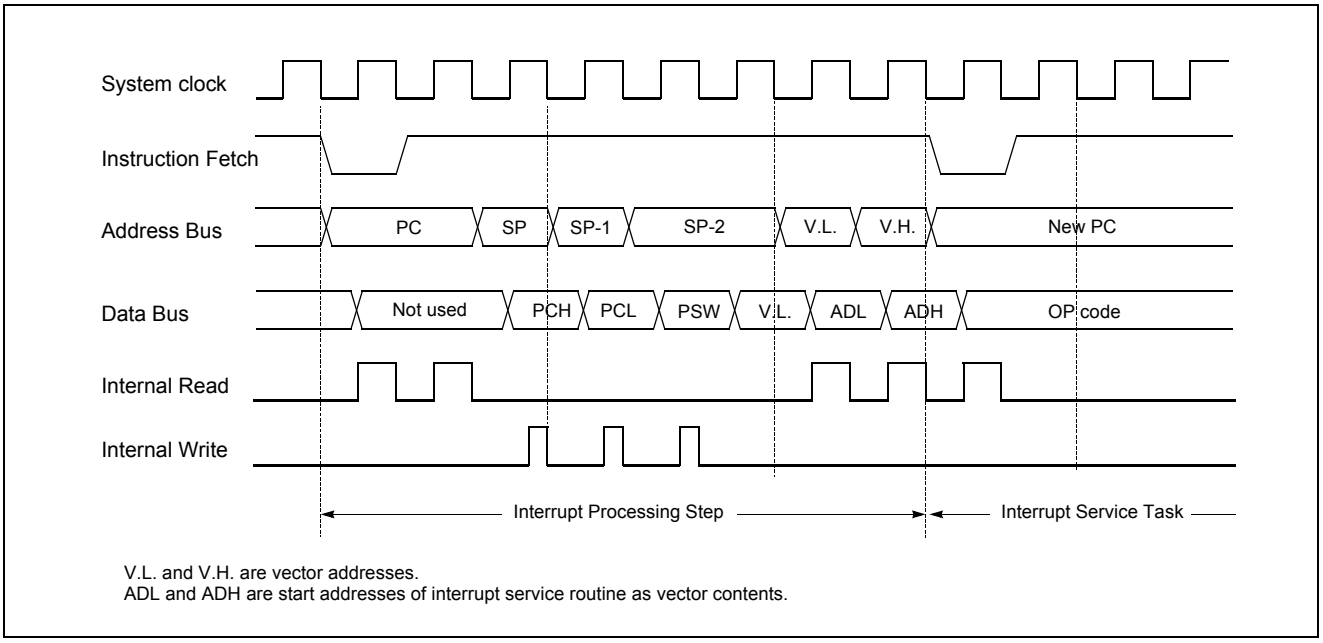
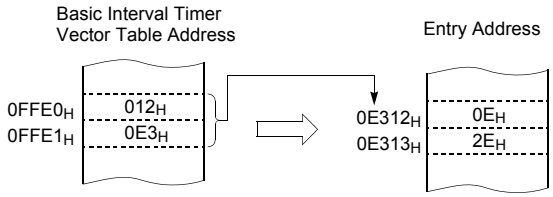


Figure 18-4 Timing chart of Interrupt Acceptance and Interrupt Return Instruction



Correspondence between vector table address for BIT interrupt and the entry address of the interrupt service program.

A interrupt request is not accepted until the I-flag is set to "1" even if a requested interrupt has higher priority than that of the current interrupt being serviced.

When nested interrupt service is required, the I-flag should be set to "1" by "EI" instruction in the interrupt service program. In this case, acceptable interrupt sources are selectively enabled by the individual interrupt enable flags.

Clearing Interrupt Request Flag

The Interrupt Request flag may not cleared itself during interrupt acceptance processing. After interrupt acceptance, it should be cleard as shown in interrupt service routine.

Note: *The MC80F0316 and HMS87C1416B is similar in function, but the interrupt processing method is different. When replacing the HMS87C1416B to MC80F0316, clearing interrupt request flag should be added.*

Example: Clearing Interrupt Request Flag

```
T1_INT:   CLR1   T1IF   ;CLEAR T1 REQUEST
          [interrupt processing]
          RETI          ;RETURN
```

Saving/Restoring General-purpose Register

During interrupt acceptance processing, the program counter and the program status word are automatically saved on the stack, but accumulator and other registers are not saved itself. These registers are saved by the software if necessary. Also, when multiple interrupt services are nested, it is necessary to avoid using the same data memory area for saving registers.

The following method is used to save/restore the general-purpose registers.

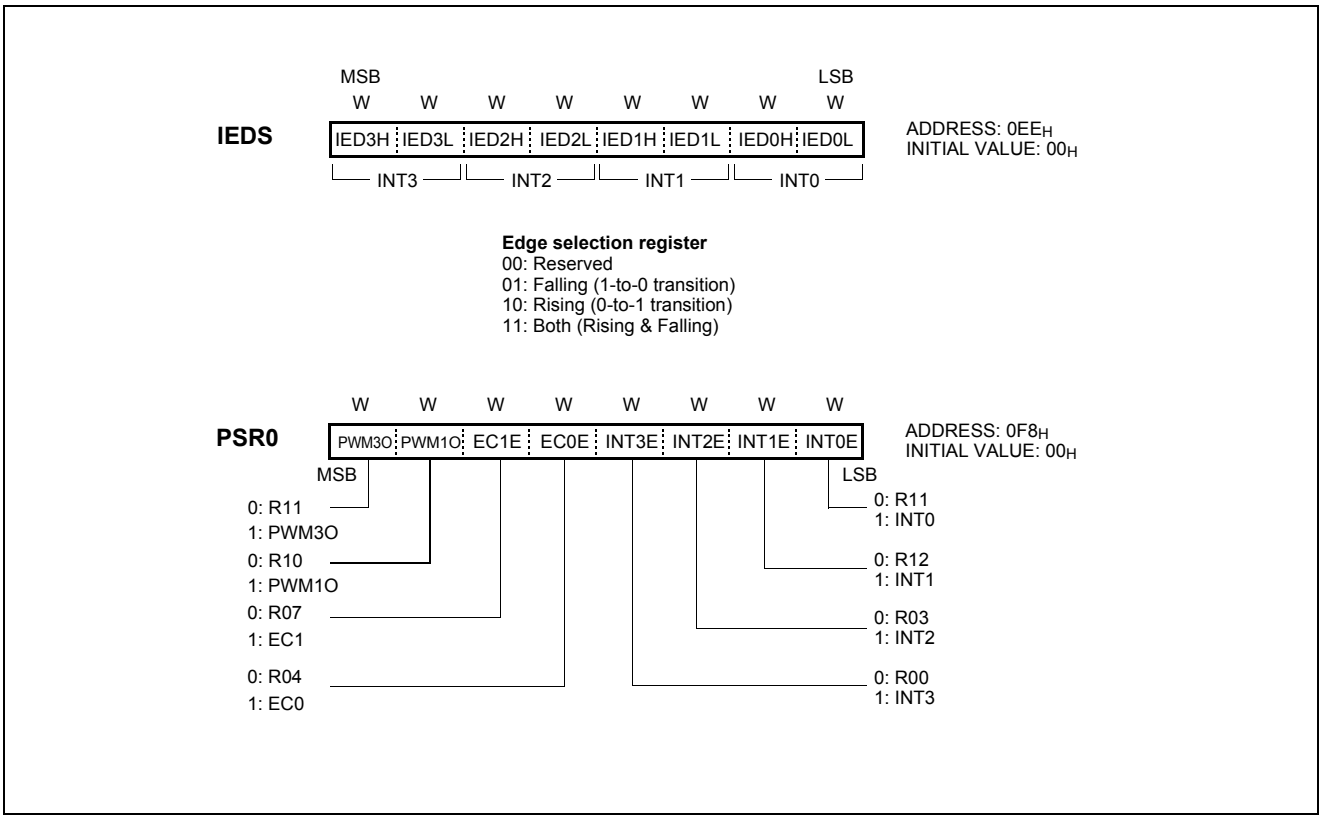


Figure 18-9 IEDS register and Port Selection Register PSR0

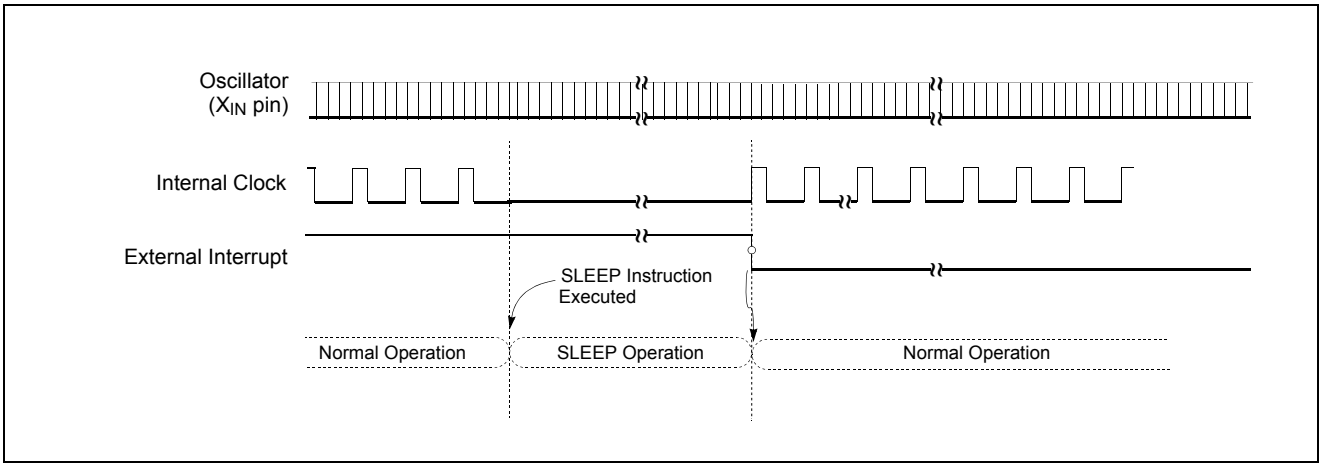


Figure 19-2 SLEEP Mode Release Timing by External Interrupt

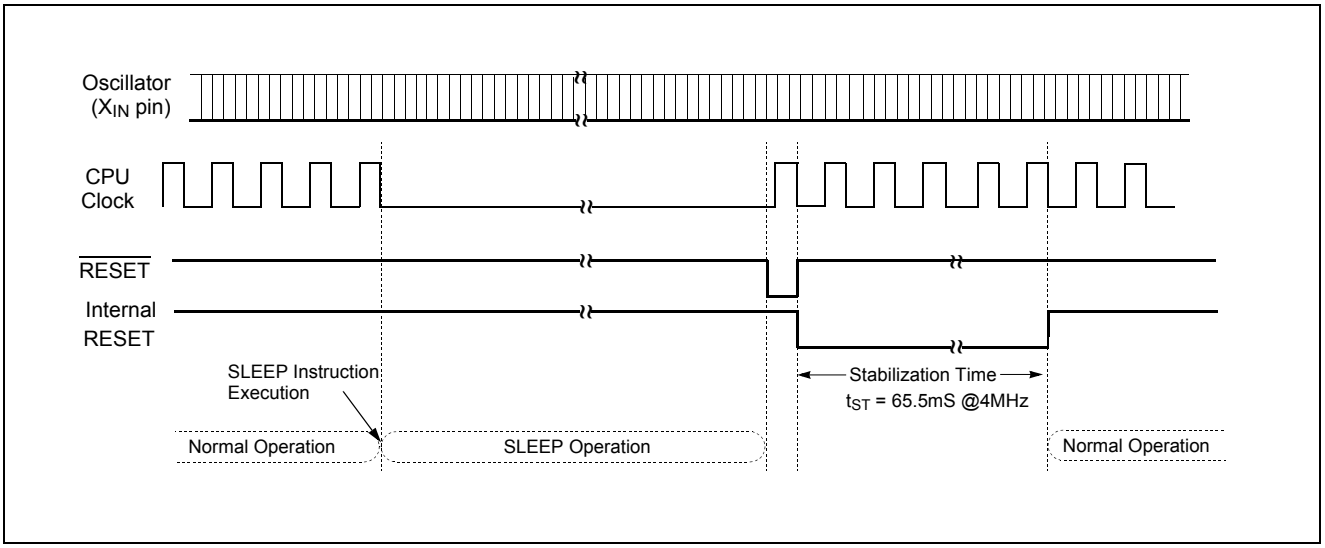


Figure 19-3 Timing of SLEEP Mode Release by Reset

19.2 Stop Mode

In the Stop mode, the main oscillator, system clock and peripheral clock is stopped, but RC-oscillated watchdog timer continue to operate. With the clock frozen, all functions are stopped, but the on-chip RAM and Control registers are held. The port pins out the values held by their respective port data register, port direction registers. Oscillator stops and the systems internal operations are all held up.

- The states of the RAM, registers, and latches valid immediately before the system is put in the STOP state are all held.
- The program counter stop the address of the instruction to be executed after the instruction "STOP" which starts the STOP operating mode.

Note: *The Stop mode is activated by execution of STOP instruction after setting the SSCR to "5A$_H$". (This register should be written by byte operation. If this register is set by bit manipulation instruction, for example "set1" or "clr1" instruction, it may be undesired operation)*

In the Stop mode of operation, V_{DD} can be reduced to minimize power consumption. Care must be taken, however, to ensure that V_{DD} is not reduced before the Stop mode is invoked, and that V_{DD} is restored to its normal operating level, before the Stop mode is terminated.

The reset should not be activated before V_{DD} is restored to its normal operating level, and must be held active long enough to allow the oscillator to restart and stabilize.

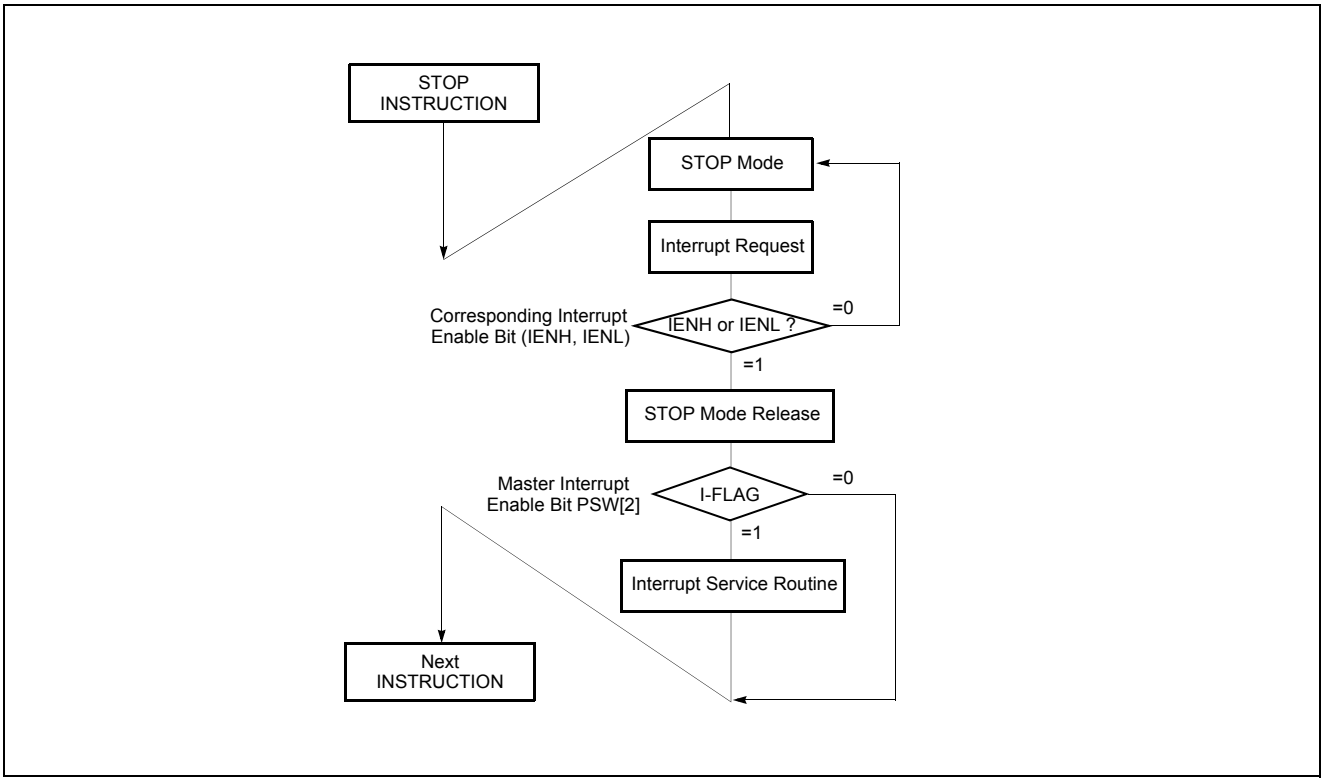


Figure 19-4 STOP Releasing Flow by Interrupts

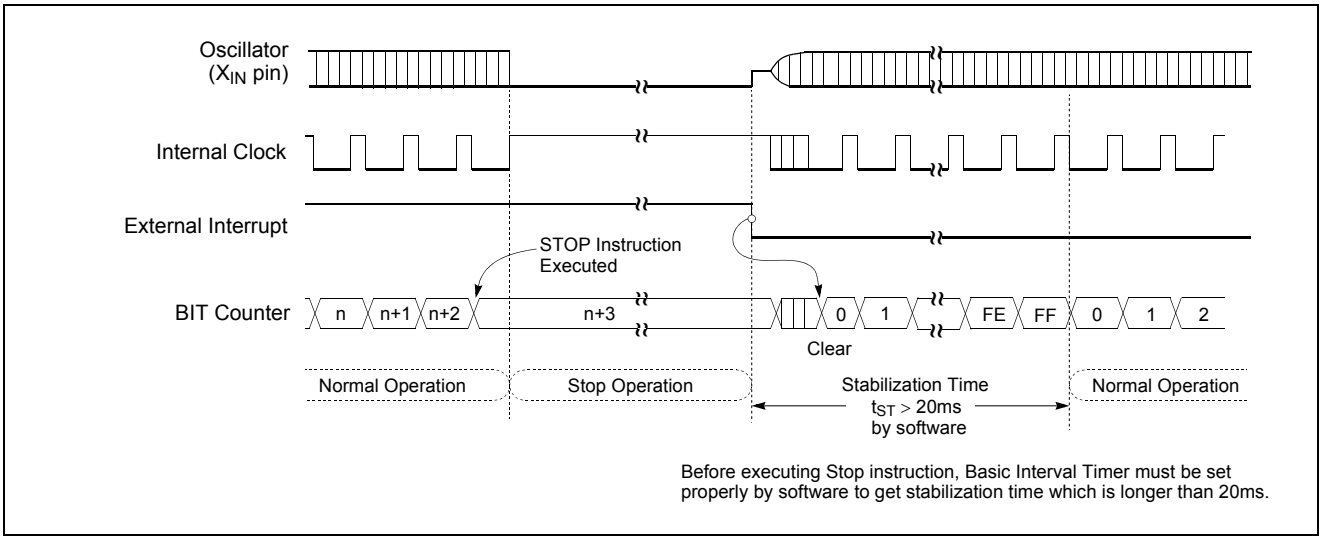


Figure 19-5 STOP Mode Release Timing by External Interrupt

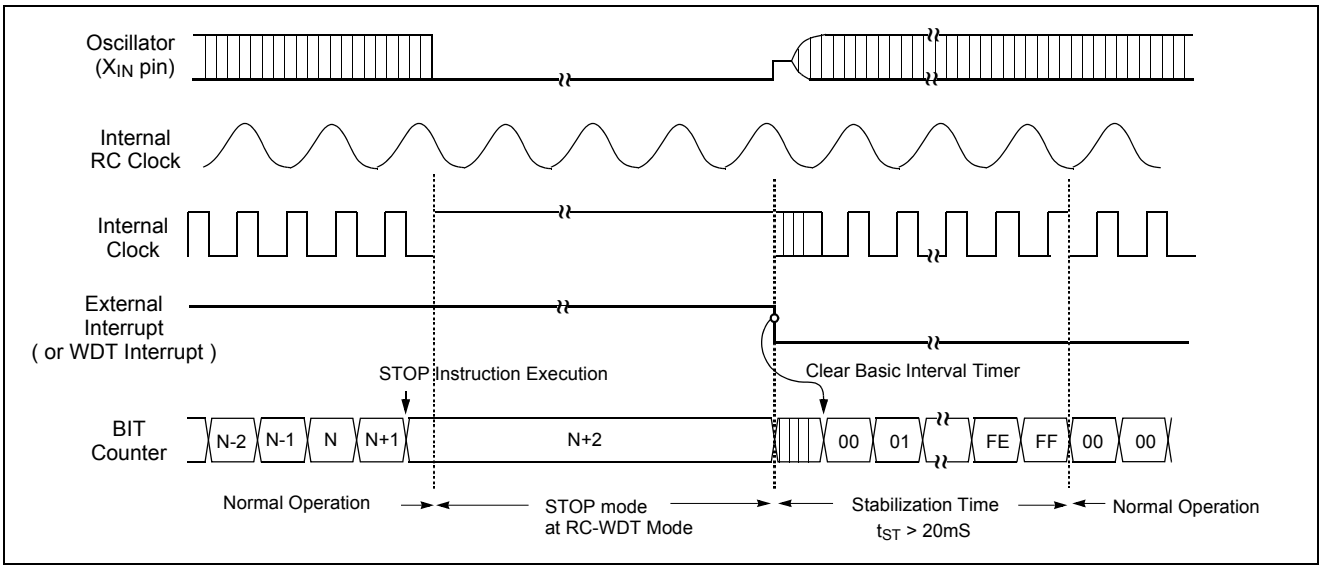


Figure 19-7 Stop Mode Release at Internal RC-WDT Mode by External Interrupt or WDT Interrupt

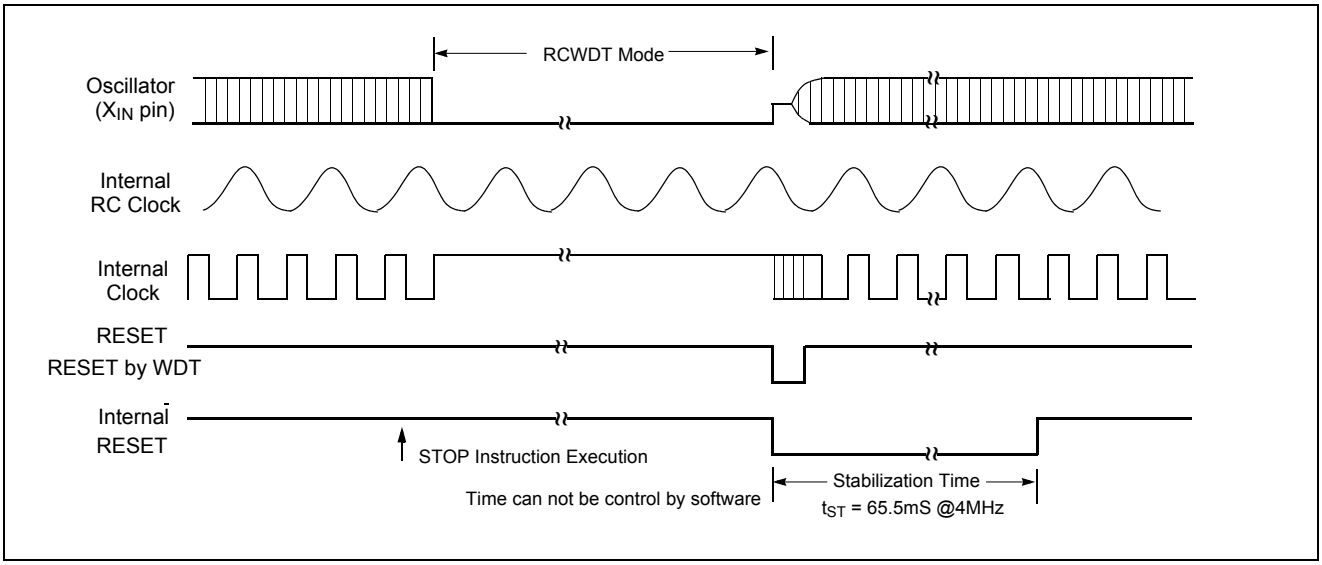


Figure 19-8 Internal RC-WDT Mode Releasing by Reset

19.4 Minimizing Current Consumption

The Stop mode is designed to reduce power consumption. To minimize current drawn during Stop mode, the user should turn-off output drivers that are sourcing or sinking current, if it is prac-

tical.

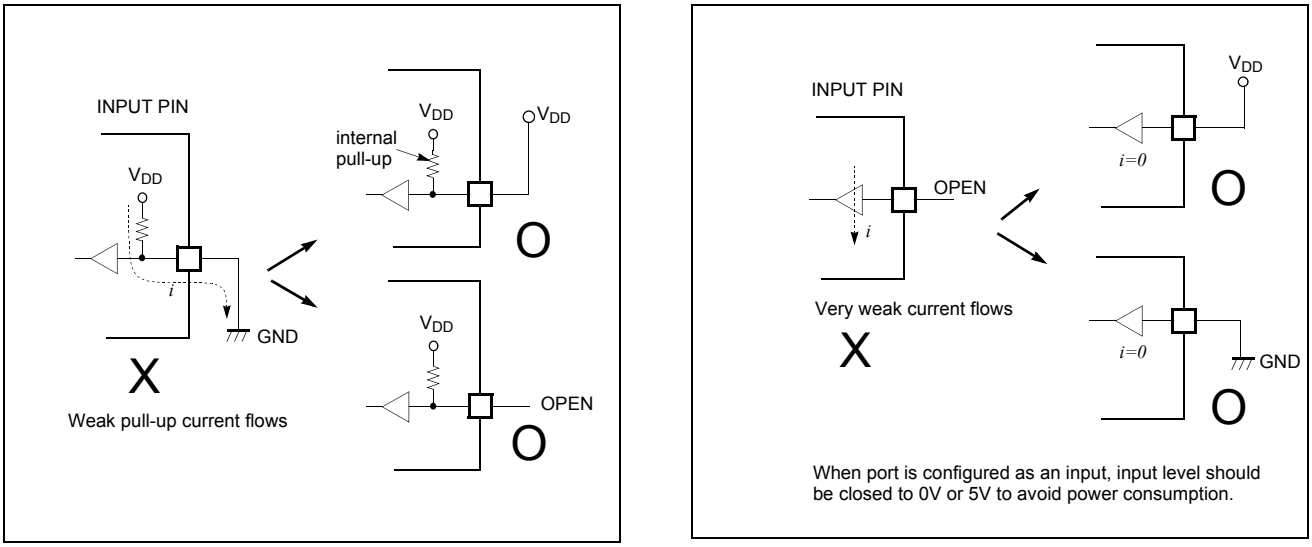


Figure 19-9 Application Example of Unused Input Port

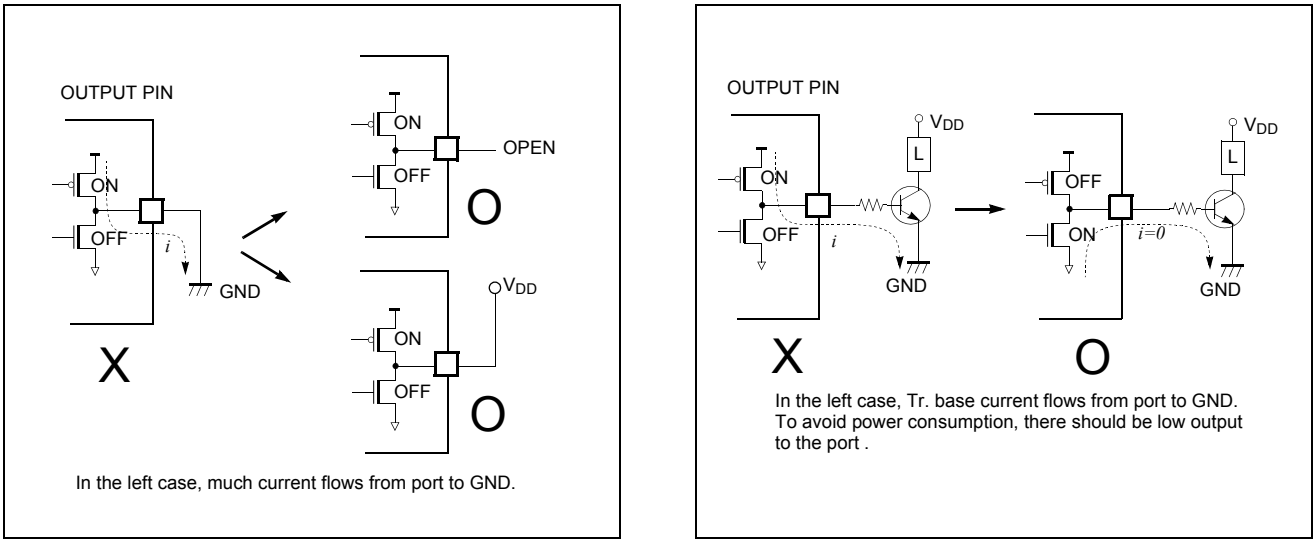


Figure 19-10 Application Example of Unused Output Port

Note: *In the STOP operation, the power dissipation associated with the oscillator and the internal hardware is lowered; however, the power dissipation associated with the pin interface (depending on the external circuitry and program) is not directly determined by the hardware operation of the STOP feature. This point should be little current flows when the input level is stable at the power voltage level (V_{DD}/V_{SS}); however, when the input level becomes higher than the power voltage level (by approximately 0.3V), a current begins to flow. Therefore, if cutting off the output transistor at an I/O port puts the pin signal into the high-impedance state, a current flow across the ports input transistor, requiring it to fix the level by pull-up or other means.*

It should be set properly in order that current flow through port doesn't exist.

First consider the port setting to input mode. Be sure that there is no current flow after considering its relationship with external circuit. In input mode, the pin impedance viewing from external MCU is very high that the current doesn't flow.

But input voltage level should be V_{SS} or V_{DD}. Be careful that if unspecified voltage, i.e. if uncertain voltage level (not V_{SS} or V_{DD}) is applied to input pin, there can be little current (max. 1mA at around 2V) flow.

If it is not appropriate to set as an input mode, then set to output mode considering there is no current flow. The port setting to

High or Low is decided by considering its relationship with external circuit. For example, if there is external pull-up resistor then it is set to output mode, i.e. to High, and if there is external pull-down register, it is set to low.

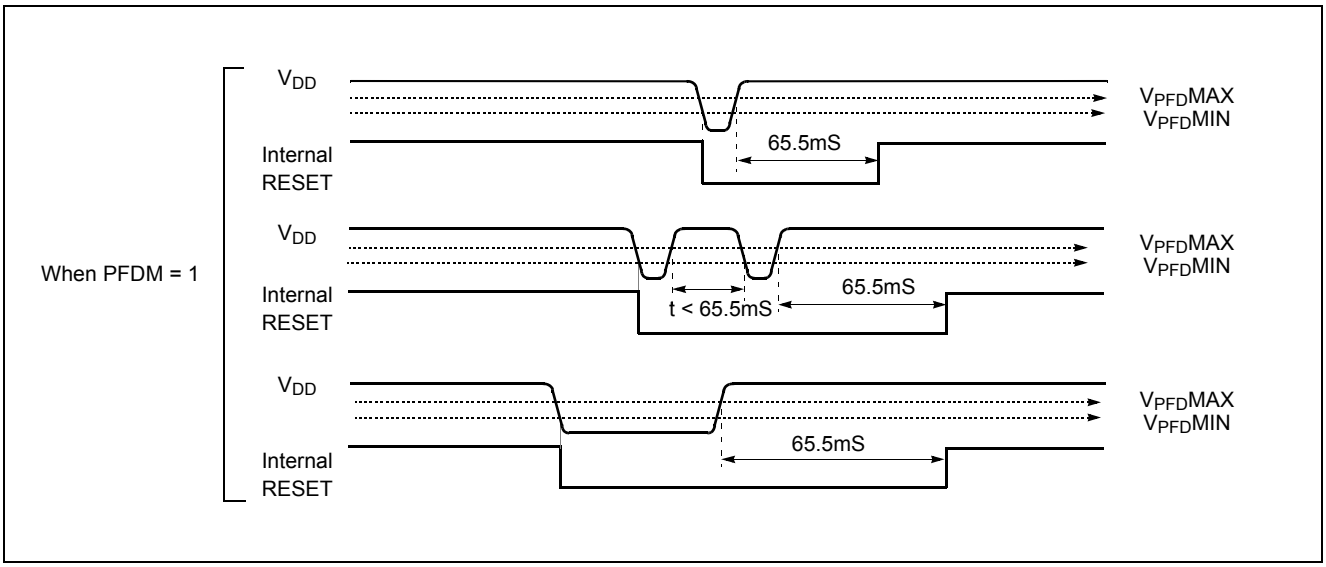


Figure 21-3 Power Fail Processor Situations (at 4MHz operation)

22. COUNTERMEASURE OF NOISE

22.1 Oscillation Noise Protector

The Oscillation Noise Protector (ONP) is used to supply stable internal system clock by excluding the noise which could be entered into oscillator and recovery the oscillation fail. This function could be enabled or disabled by the "ONP" bit of the Device configuration area ($20FF_H$) for the MC80F0304/0308/0316, "ONP" option bits MASK option.

The ONP function is like below.

- Recovery the oscillation wave crushed or loss caused by high frequency noise.
- Change system clock to the internal oscillation clock when the high frequency noise is continuing.
- Change system clock to the internal oscillation clock when the X_{IN}/X_{OUT} is shorted or opened, the main oscillation is stopped except by stop instruction and the low frequency noise is entered.

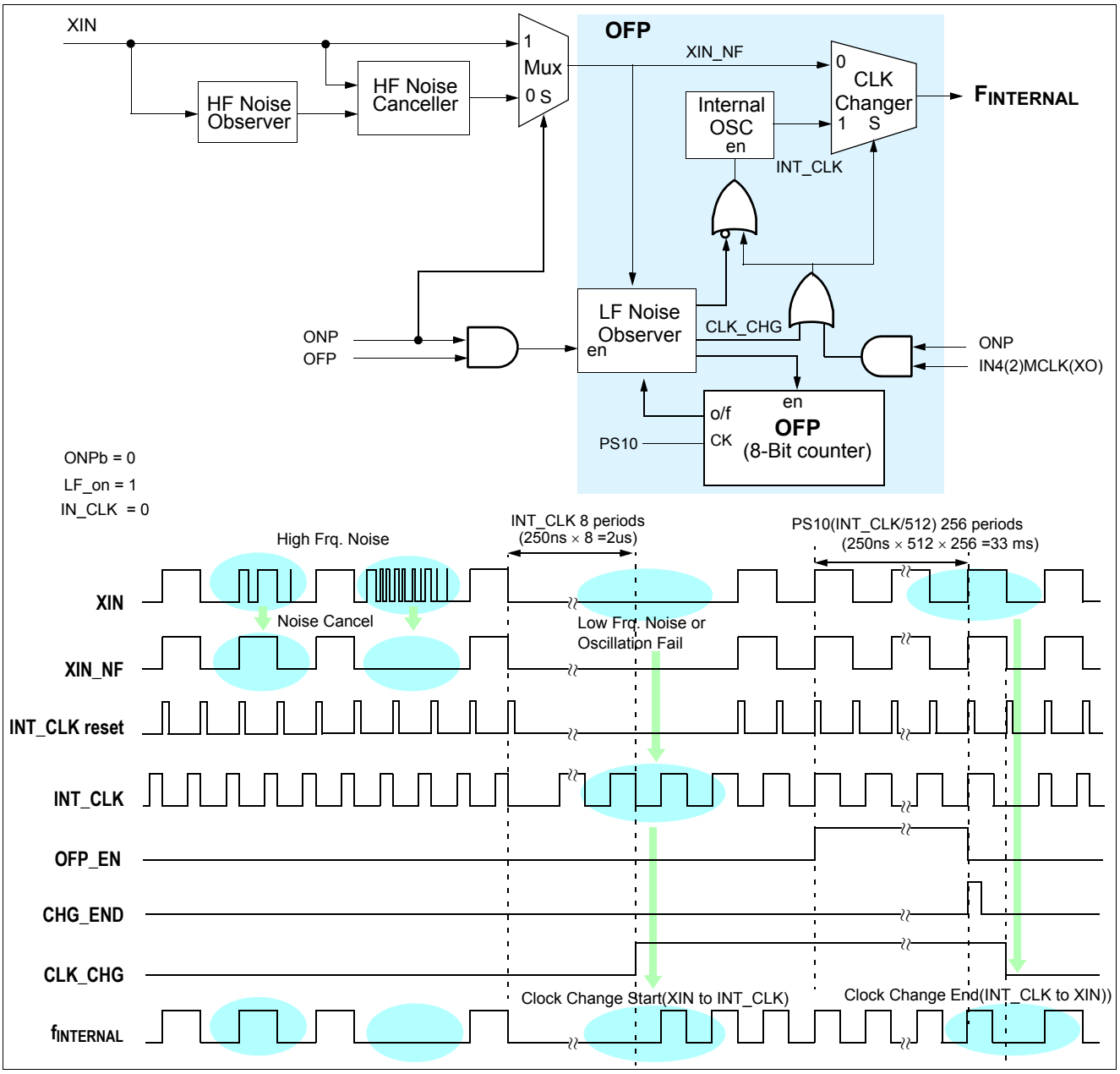


Figure 22-1 Block Diagram of ONP & OFP and Respective Wave Forms

22.2 Oscillation Fail Processor

The oscillation fail processor (OFP) can change the clock source from external to internal oscillator when the oscillation fail occured. This function could be enabled or disabled by the "OFP" bit of the Device Configuration Area (MASK option for MC80F0304/0308/0316).
And this function can recover the external clock source when the external clock is recovered to normal state.

IN4(2)MCLK/CLKXO(XO) Option

The "IN4MCLK(XO)", "IN2MCLK(XO)" bit of the Device Configuration Area (MASK option for MC80F0304/0308/0316) enables the function to operate the device by using the internal oscillator clock in ONP block as system clock. There is no need to connect the x-tal, resonator, RC and R externally. The user only to connect the X_{IN} pin to V_{DD}. After selecting the this option, the period of internal oscillator clock could be checked by X_{OUT} outputting clock divided the internal oscillator clock by 4.

23. DEVICE CONFIGURATION AREA

The Device Configuration Area can be programmed or left unprogrammed to select device configuration such as POR, ONP, CLK option and security bit. This area is not accessible during normal execution but is readable and writable during FLASH program / verify mode.

Note: *The Configuration Option may not be read exactly when VDD rising time is very slow. It is recommended to adjust the VDD rising time faster than 40ms/V (200ms from 0V to 5V).*

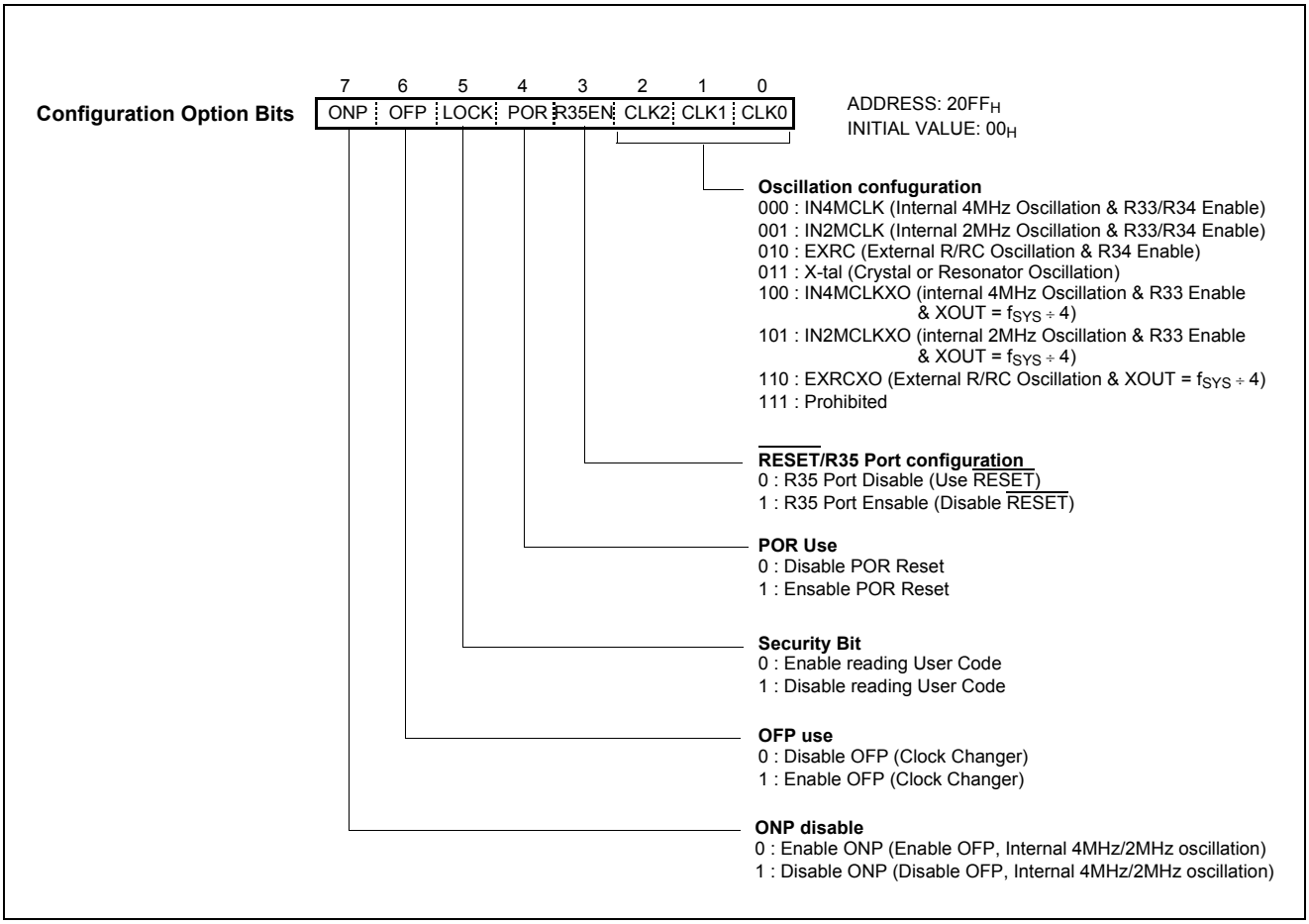


Figure 23-1 Device Configuration Area

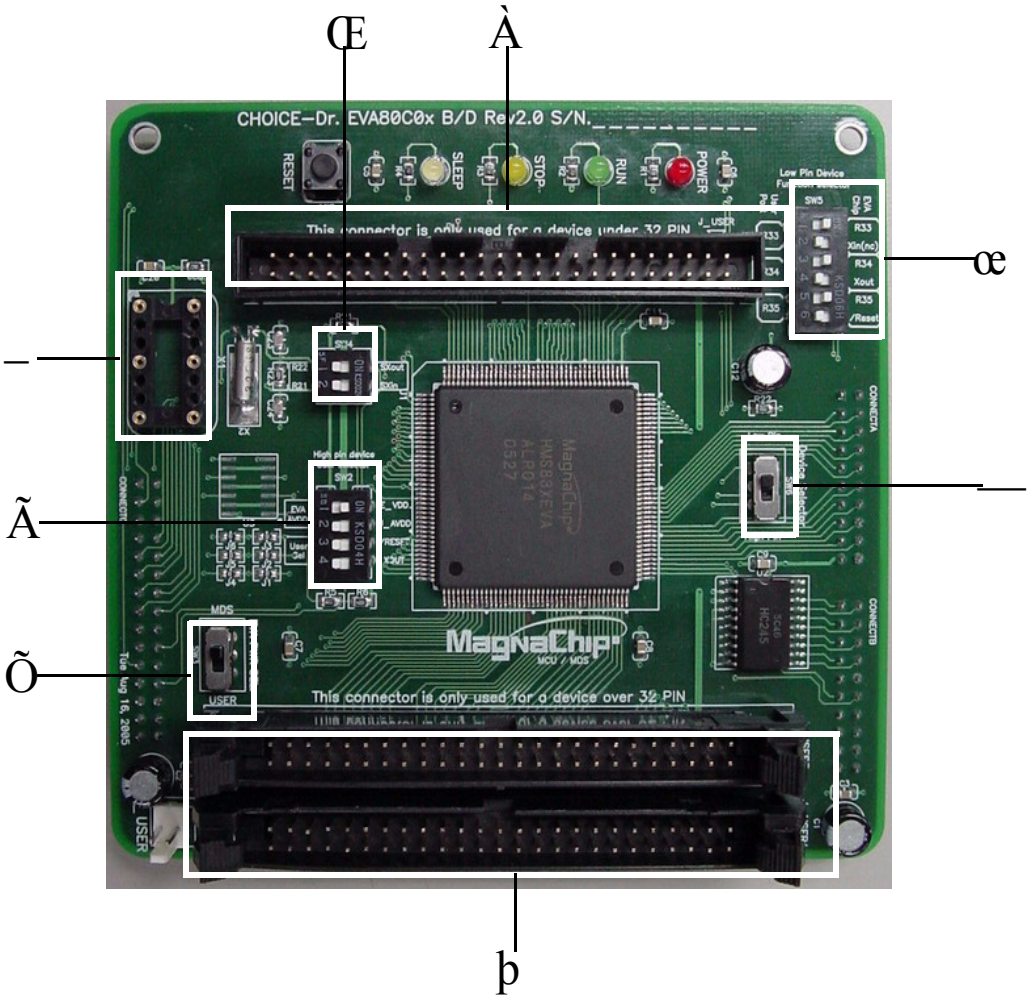
24. MASK OPTION (MC80C0304/08/16)

The MC80C0304/08/16 has several MASK option which configures the package type or use of some special features of the device. The MASK option of the MASK order sheet should be checked to select device configuration such as package type, Oscillation selection, oscillation noise protector, oscillation fail protector, internal 4MHz, amount of noise to be cancelled.

	Option	Check	Operation	Remark
MASK Option	Package	28 SKDIP	28 SKDIP type package select	
		32 PDIP	32 PDIP type package select	
	ONP	Yes	ONP Enable	OSC Noise Protector(ONP) Operation En/Disable Bit
		No	ONP Disable	
	OFP	Yes	Enables Oscillation Fail Processor (ONP clock changer)	Change the Inter clock when oscillation failed
		No	Disables Oscillation Fail Processor (ONP clock changer)	
	POR	Yes	Enables POR	To select Power-on Reset
		No	Disables POR	
	R35EN	Yes	R35 port Enable (Disable $\overline{RESET}$)	To use R35 port as nomarl input port
		No	R35 port Disable (Use $\overline{RESET}$)	
	CLK option	Crystal	Crystal Oscillation	To select Oscillation Type
		EXRC	External R/RC oscillation & R33 Enable	
		IN4MCLK	Internal 4MHz Oscillation & R33/R34 Enable	
		IN2MCLK	Internal 2MHz Oscillation & R33/R34 Enable	
		EXRCXO	External R/RC oscillation & R33 Enable X_{OUT} Pin : System clock ÷ 4	
		IN4MCLKXO	Internal 4MHz Oscillation & R33 Enable X_{OUT} Pin : System clock ÷ 4	
		IN2MCLKXO	Internal 2MHz Oscillation & R33 Enable X_{OUT} Pin : System clock ÷ 4	

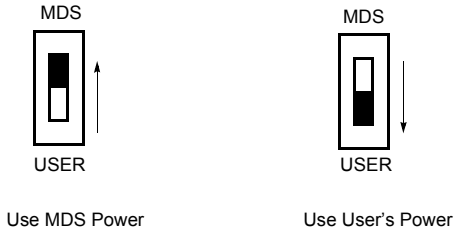
Table 24-1 MASK options

25. EMULATOR EVA. BOARD SETTING



25.1 DIP Switch and VR Setting

Before execute the user program, keep in your mind the below configuration

DIP S/W		Description	ON/OFF Setting
þ	-	This connector is only used for a device over 32 PIN.	For the MC80F0224/MC80F0448
A	-	This connector is only used for a device under 32 PIN.	For the MC80F0316.
Ã SW2	1 2	 AV_{DD} pin select switch	These switches select the AV_{DD} source. **ON & OFF** : Use Eva. V_{DD} **OFF & ON** : Use User AV_{DD}
	3	This switch select the /Reset source.	Normally **OFF**. EVA. chip can be reset by external user target board. **ON** : Reset is available by either user target system board or Emulator RESET switch. **OFF** : Reset the MCU by Emulator RESET switch. Does not work from user target board.
	4	This switch select the Xout signal on/off.	Normally **OFF**. MCU XOUT pin is disconnected internally in the Emulator. Some circumstance user may connect this circuit. **ON** : Output XOUT signal **OFF** : Disconnect circuit
Õ SW3	1	This switch select Eva. B/D Power supply source. 	Normally **MDS**. This switch select Eva. B/D Power supply source.
Œ SW4	1 2	This switch select the R22 or SX_{OUT}. This switch select the R21 or SX_{IN}.	These switchs select the Normal I/O port(off) or Sub-Clock (on). It is reserved for the MC80F0448. **ON** : SX_{OUT}, SX_{IN} **OFF** : R22, R21 Don't care (MC80F0224/MC80F0448).
œ SW5	1 2	These switches select the R33 or X_{IN}	This switch select the Normal I/O port(on&off) or special function select(off&on). It is reserved for the MC80F0316. **ON & OFF** : R33,R34,R35 Port selected. **OFF & ON** : X_{OUT}, X_{IN} , /Reset selected. Don't care (MC80F0224/MC80F0448).
	3 4	These switches select the R34 or X_{OUT}	
	5 6	These switches select the R35 or /Reset	
—	-	This is External oscillation socket(CAN Type. OSC)	This is for External Clock(CAN Type. OSC).

DIP S/W		Description	ON/OFF Setting
SW6	1	Eva. select switch	Must be **OFF** position. **ON** : For the MC80F0224/MC80F0448. **OFF** : For the MC80F0316.

26. IN-SYSTEM PROGRAMMING (ISP)

26.1 Getting Started / Installation

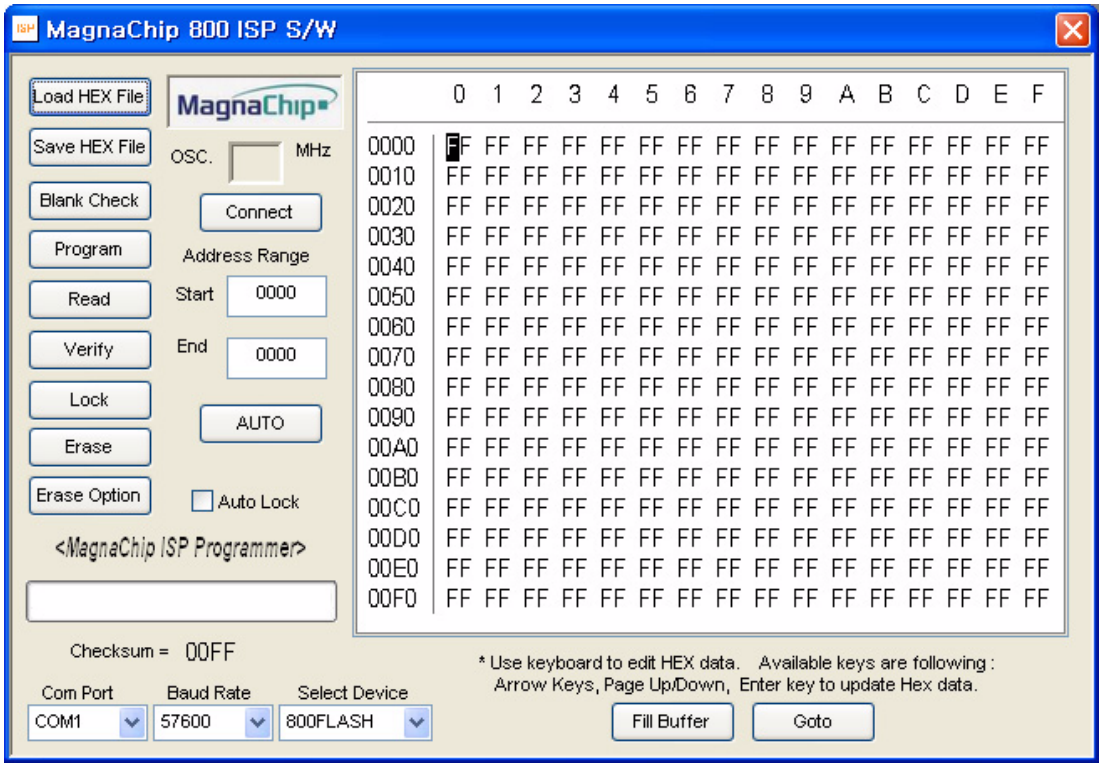
The following section details the procedure for accomplishing the installation procedure.

1. Connect the serial(RS-232C) cable between a target board and the COM1 serial port of your PC.
2. Configure the COM1 serial port of your PC as following.

Baudrate	115,200
Data bit	8
Parity	No
Stop bit	1
Flow control	No

3. Turn your target B/D power switch ON. Your target B/D must be configured to enter the ISP mode.
4. Run the MagnaChip ISP software.
5. Press the Reset Button in the ISP S/W. If the status windows shows a message as "Connected", all the conditions for ISP are provided.

26.2 Basic ISP S/W Information



Function	Description
Load HEX File	Load the data from the selected file storage into the memory buffer.
Save HEX File	Save the current data in your memory buffer to a disk storage by using the Intel Motorolla HEX format.
Erase	Erase the data in your target MCU before programming it.
Blank Check	Verify whether or not a device is in an erased or unprogrammed state.
Program	This button enables you to place new data from the memory buffer into the target device.
Read	Read the data in the target MCU into the buffer for examination. The checksum will be displayed on the checksum box.
Verify	Assures that data in the device matches data in the memory buffer. If your device is secured, a verification error is detected.
Lock	Secures devices so that their content can no longer be examined or modified.
Erase Option	-
AUTO	Erase & Program & Verify
Auto Lock	If selected with check mark, the security locking is performed after erasure.
Connect	Connect a MCU in your target Board with displaying as “Connected” in the status box. Users have to press this button at least one time to initialize a target MCU for entering the ISP mode. If failed to enter the ISP mode, all the buttons are unavailable. And, after entering successfully, the Connect button will be unavailable.
Edit Buffer	Modify the data in the selected address in your buffer memory
Fill Buffer	Fill the selected area with a data.
Goto	Display the selected page.
OSC. _____ MHz	Enter your target system’s oscillator value with discarding below point.
Start _____	Starting address
End _____	End address
Checksum	Display the checksum(Hexdecimal) after reading the target device.
Com Port	Select serial port.
Baud Rate	Select UART baud rate.
Select Device	Select target device.
Page Up Key	Display the previous page of your memory buffer.
Page Down Key	Display the higher page than the current location.

Table 1. ISP Function Description

26.3 Hardware Conditions to Enter the ISP Mode

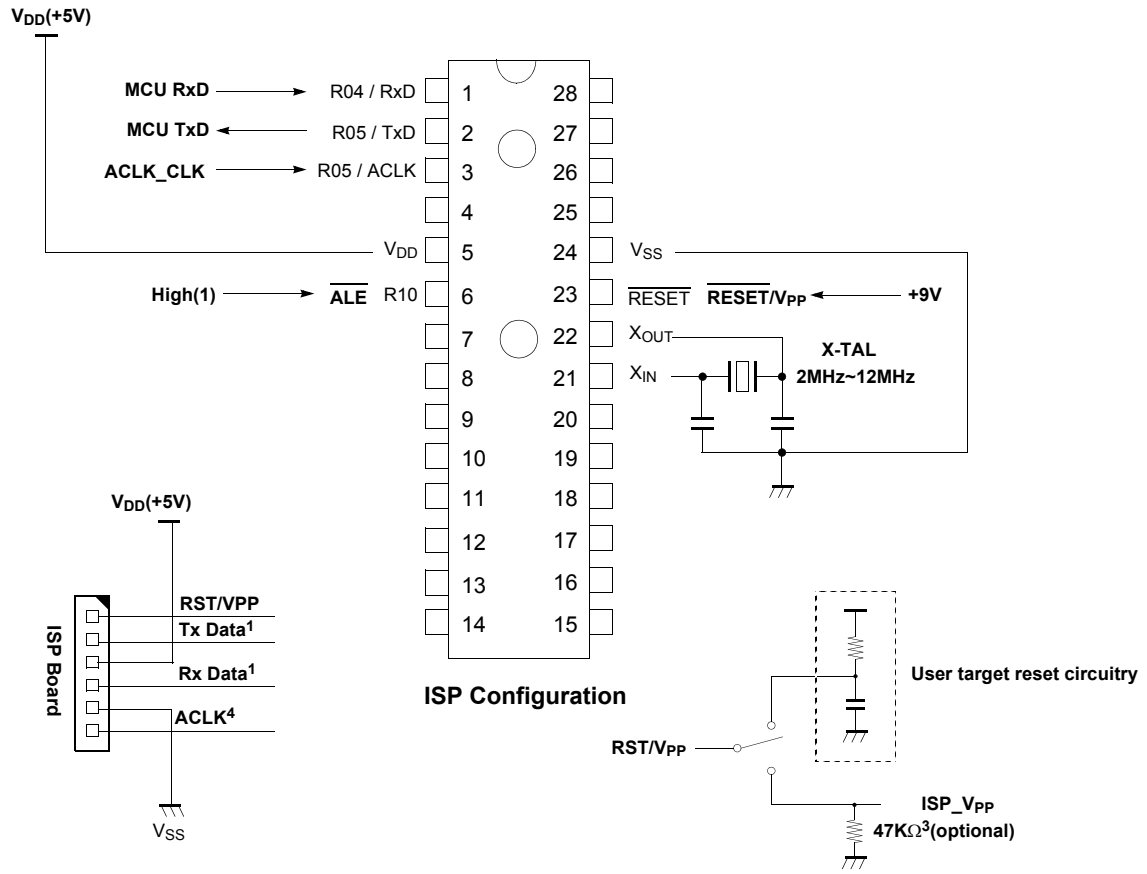
The boot loader can be executed by holding ALEB high, RST/V_{PP} as +9V, and ACLK(optional) with OSC. 1.8432MHz. The ISP function uses following pins: TxD, RxD, ALEB, ACLK and RST/V_{PP}.

Note: *If POR and R35 are enabled, Vdd and Vpp should be turned on simultaneously to enter ISP mode.*

Normal sequence above can not enter ISP mode when POR and R35 options are enabled.
Please follow below sequence instead of normal one.

1) Power off a target system.
2) Configure a target system as ISP mode.
3) Attach a ISP B/D into a target system.
4) Run the ISP S/W

5) Select target MCU - It makes condition to make Vpp to turn on when Vdd is turned on.
6) Power on a target system. : At this point, ISP mode is entered because the Vdd and Vpp are turned on simultaneously.



1. If other signals affect UART communiction in ISP mode, disconnect these pins by using a jumper or a switch.
2. The ALEB can be shared with other function. Toggle the port between ISP and user mode.
3. The pull down resister is optional. If user set to ISP Mode without connection ISP board, the Vpp/Reset Port is in floating state. The pull down resistor is for blocking this undefined state.
Do not power on a application B/D in ISP mode without connecting a ISP board.
4. Refer to the section 26.5 explaining the auto bua drate and ACK mode.

26.4 Sequence to enter ISP mode/user mode

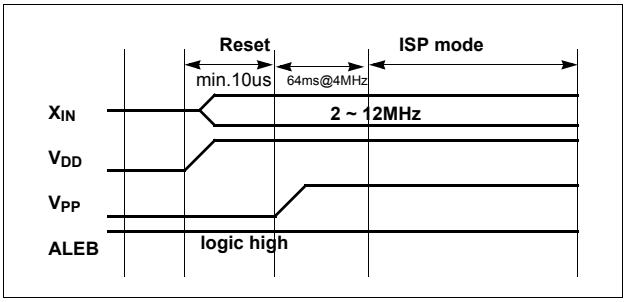


Figure 26-1 Timing diagram to enter the ISP mode

Sequence to enter ISP mode from user mode.
(If POR and R35 are enabled, the sequnence "Run the ISP S/W"should be followed by the sequence "Power on a target system" as shown in NOTE of chapter 26.3)

1. Power off a target system.
2. Configure a target system as ISP mode.
3. Attach a ISP B/D into a target system.
4. Power on a target system.
5. Run the ISP S/W.

S
Sequence to enter user mode from ISP mode.

1. Close the ISP S/W..
2. Power off a target system.
3. Configure a target system as user mode
4. Detach a ISP B/D from a target system.
5. Power on.

26.5 ACK mode

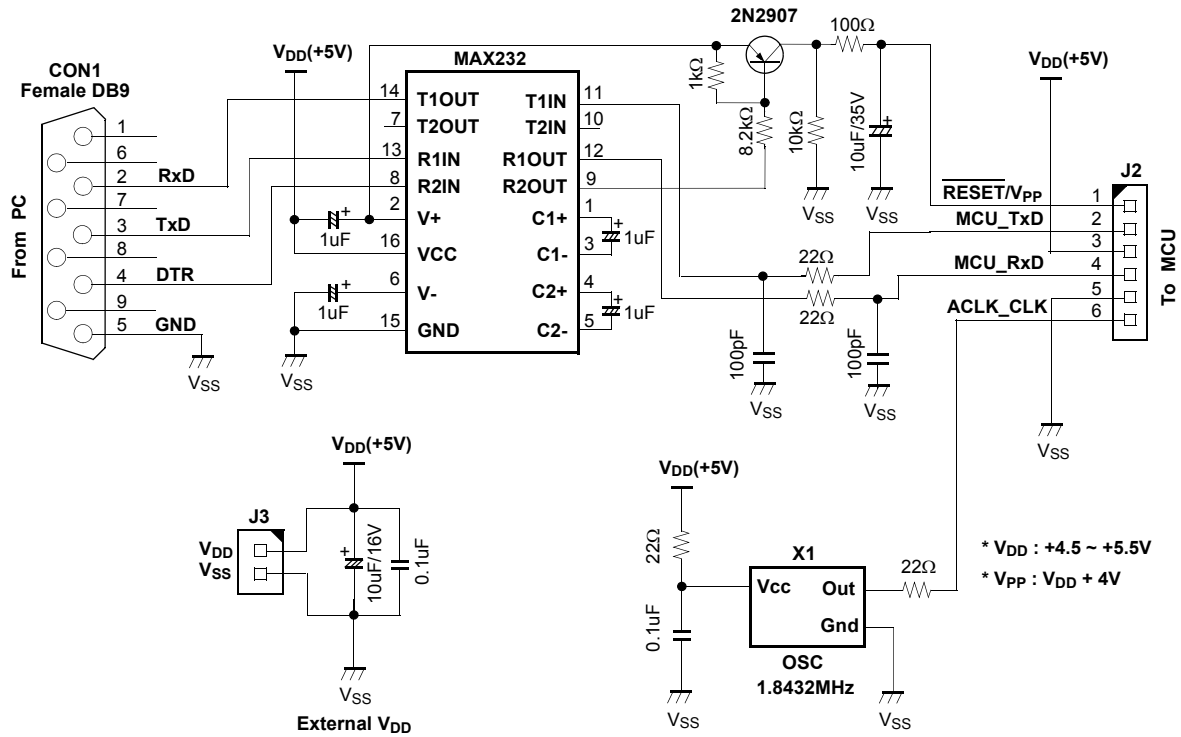
The ISP S/W can not detect user system clock. Users have to enter a user system clock. This mode is only used when failed to detect user system clock automatically.

Note: *Need to connect the ACK pin to ISP B/D.*

26.6 Reference ISP Circuit Diagram and ABOV Supplied ISP Board

The ISP software and hardware circuit diagram are provided at www.abov.co.kr . To get a ISP B/D, contact to sales department.

The following circuit diagram is for reference use.



The ragne of V_{DD} must be from 4.5 to 5.5V and ISP function is not supported under 2MHz system clock.
If the user supplied V_{DD} is out of range, the external power is needed instead of the target system V_{DD}.
For the ISP operation, power consumption required is minimum 30mA.

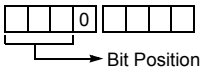
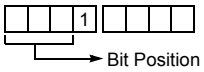
Figure 26-2 Reference ISP Circuit Diagram

Figure 26-3 ISP board supplied by ABOV

APPENDIX

A. INSTRUCTION

A.1 Terminology List

Terminology	Description
A	Accumulator
X	X - register
Y	Y - register
PSW	Program Status Word
#imm	8-bit Immediate data
dp	Direct Page Offset Address
!abs	Absolute Address
[ ]	Indirect expression
{ }	Register Indirect expression
{ }+	Register Indirect expression, after that, Register auto-increment
.bit	Bit Position
A.bit	Bit Position of Accumulator
dp.bit	Bit Position of Direct Page Memory
M.bit	Bit Position of Memory Data (000_H~$0FFF_H$)
rel	Relative Addressing Data
upage	U-page ($0FF00_H$~$0FFFF_H$) Offset Address
n	Table CALL Number (0~15)
+	Addition
x	 Upper Nibble Expression in Opcode
y	 Upper Nibble Expression in Opcode
–	Subtraction
×	Multiplication
/	Division
( )	Contents Expression
∧	AND
∨	OR
⊕	Exclusive OR
~	NOT
←	Assignment / Transfer / Shift Left
→	Shift Right
↔	Exchange
=	Equal
≠	Not Equal

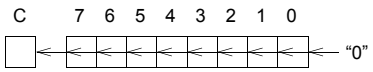
A.2 Instruction Map

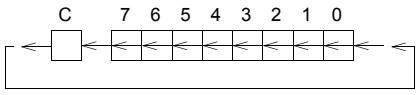
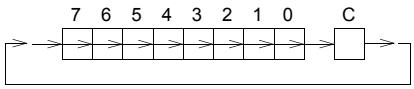
LOW HIGH	00000 00	00001 01	00010 02	00011 03	00100 04	00101 05	00110 06	00111 07	01000 08	01001 09	01010 0A	01011 0B	01100 0C	01101 0D	01110 0E	01111 0F
000	-	SET1 dp.bit	BBS A.bit,rel	BBS dp.bit,rel	ADC #imm	ADC dp	ADC dp+X	ADC !abs	ASL A	ASL dp	TCALL 0	SETA1 .bit	BIT dp	POP A	PUSH A	BRK
001	CLRC	“	“	“	SBC #imm	SBC dp	SBC dp+X	SBC !abs	ROL A	ROL dp	TCALL 2	CLRA1 .bit	COM dp	POP X	PUSH X	BRA rel
010	CLRG	“	“	“	CMP #imm	CMP dp	CMP dp+X	CMP !abs	LSR A	LSR dp	TCALL 4	NOT1 M.bit	TST dp	POP Y	PUSH Y	PCALL Upage
011	DI	“	“	“	OR #imm	OR dp	OR dp+X	OR !abs	ROR A	ROR dp	TCALL 6	OR1 OR1B	CMPX dp	POP PSW	PUSH PSW	RET
100	CLRV	“	“	“	AND #imm	AND dp	AND dp+X	AND !abs	INC A	INC dp	TCALL 8	AND1 AND1B	CMPY dp	CBNE dp+X	TXSP	INC X
101	SETC	“	“	“	EOR #imm	EOR dp	EOR dp+X	EOR !abs	DEC A	DEC dp	TCALL 10	EOR1 EOR1B	DBNE dp	XMA dp+X	TSPX	DEC X
110	SETG	“	“	“	LDA #imm	LDA dp	LDA dp+X	LDA !abs	TXA	LDY dp	TCALL 12	LDC LDCB	LDX dp	LDX dp+Y	XCN	DAS (N/A)
111	EI	“	“	“	LDM dp,#imm	STA dp	STA dp+X	STA !abs	TAX	STY dp	TCALL 14	STC M.bit	STX dp	STX dp+Y	XAX	STOP

LOW HIGH	10000 10	10001 11	10010 12	10011 13	10100 14	10101 15	10110 16	10111 17	11000 18	11001 19	11010 1A	11011 1B	11100 1C	11101 1D	11110 1E	11111 1F
000	BPL rel	CLR1 dp.bit	BBC A.bit,rel	BBC dp.bit,rel	ADC {X}	ADC !abs+Y	ADC [dp+X]	ADC [dp]+Y	ASL !abs	ASL dp+X	TCALL 1	JMP !abs	BIT !abs	ADDW dp	LDX #imm	JMP [!abs]
001	BVC rel	“	“	“	SBC {X}	SBC !abs+Y	SBC [dp+X]	SBC [dp]+Y	ROL !abs	ROL dp+X	TCALL 3	CALL !abs	TEST !abs	SUBW dp	LDY #imm	JMP [dp]
010	BCC rel	“	“	“	CMP {X}	CMP !abs+Y	CMP [dp+X]	CMP [dp]+Y	LSR !abs	LSR dp+X	TCALL 5	MUL	TCLR1 !abs	CMPW dp	CMPX #imm	CALL [dp]
011	BNE rel	“	“	“	OR {X}	OR !abs+Y	OR [dp+X]	OR [dp]+Y	ROR !abs	ROR dp+X	TCALL 7	DBNE Y	CMPX !abs	LDYA dp	CMPY #imm	RETI
100	BMI rel	“	“	“	AND {X}	AND !abs+Y	AND [dp+X]	AND [dp]+Y	INC !abs	INC dp+X	TCALL 9	DIV	CMPY !abs	INCW dp	INC Y	TAY
101	BVS rel	“	“	“	EOR {X}	EOR !abs+Y	EOR [dp+X]	EOR [dp]+Y	DEC !abs	DEC dp+X	TCALL 11	XMA {X}	XMA dp	DECW dp	DEC Y	TYA
110	BCS rel	“	“	“	LDA {X}	LDA !abs+Y	LDA [dp+X]	LDA [dp]+Y	LDY !abs	LDY dp+X	TCALL 13	LDA {X}+	LDX !abs	STYA dp	XAY	DAA (N/A)
111	BEQ rel	“	“	“	STA {X}	STA !abs+Y	STA [dp+X]	STA [dp]+Y	STY !abs	STY dp+X	TCALL 15	STA {X}+	STX !abs	CBNE dp	XYX	NOP

A.3 Instruction Set

Arithmetic / Logic Operation

NO.	MNEMONIC	OP CODE	BYTE NO	CYCLE NO	OPERATION	FLAG NVGBHIZC
1	ADC #imm	04	2	2	Add with carry. A ← (A) + (M) + C	NV--H-ZC
2	ADC dp	05	2	3		
3	ADC dp + X	06	2	4		
4	ADC !abs	07	3	4		
5	ADC !abs + Y	15	3	5		
6	ADC [dp + X]	16	2	6		
7	ADC [dp] + Y	17	2	6		
8	ADC { X }	14	1	3		
9	AND #imm	84	2	2	Logical AND A ← (A) ∧ (M)	N-----Z-
10	AND dp	85	2	3		
11	AND dp + X	86	2	4		
12	AND !abs	87	3	4		
13	AND !abs + Y	95	3	5		
14	AND [dp + X]	96	2	6		
15	AND [dp] + Y	97	2	6		
16	AND { X }	94	1	3		
17	ASL A	08	1	2	Arithmetic shift left 	N-----ZC
18	ASL dp	09	2	4		
19	ASL dp + X	19	2	5		
20	ASL !abs	18	3	5		
21	CMP #imm	44	2	2	Compare accumulator contents with memory contents (A) - (M)	N-----ZC
22	CMP dp	45	2	3		
23	CMP dp + X	46	2	4		
24	CMP !abs	47	3	4		
25	CMP !abs + Y	55	3	5		
26	CMP [dp + X]	56	2	6		
27	CMP [dp] + Y	57	2	6		
28	CMP { X }	54	1	3		
29	CMPX #imm	5E	2	2	Compare X contents with memory contents (X) - (M)	N-----ZC
30	CMPX dp	6C	2	3		
31	CMPX !abs	7C	3	4		
32	CMPY #imm	7E	2	2	Compare Y contents with memory contents (Y) - (M)	N-----ZC
33	CMPY dp	8C	2	3		
34	CMPY !abs	9C	3	4		
35	COM dp	2C	2	4	1'S Complement : (dp) ← ~(dp)	N-----Z-
36	DAA	-	-	-	Unsupported	-
37	DAS	-	-	-	Unsupported	-
38	DEC A	A8	1	2	Decrement M ← (M) - 1	N-----Z-
39	DEC dp	A9	2	4		
40	DEC dp + X	B9	2	5		
41	DEC !abs	B8	3	5		
42	DEC X	AF	1	2		
43	DEC Y	BE	1	2		
44	DIV	9B	1	12	Divide : YA / X Q: A, R: Y	NV--H-Z-

NO.	MNEMONIC	OP CODE	BYTE NO	CYCLE NO	OPERATION	FLAG NVGBHIZC
45	EOR #imm	A4	2	2	Exclusive OR A ← (A) ⊕ (M)	N-----Z-
46	EOR dp	A5	2	3		
47	EOR dp + X	A6	2	4		
48	EOR !abs	A7	3	4		
49	EOR !abs + Y	B5	3	5		
50	EOR [dp + X]	B6	2	6		
51	EOR [dp] + Y	B7	2	6		
52	EOR { X }	B4	1	3		
53	INC A	88	1	2	Increment M ← (M) + 1	N-----Z-
54	INC dp	89	2	4		
55	INC dp + X	99	2	5		
56	INC !abs	98	3	5		
57	INC X	8F	1	2		
58	INC Y	9E	1	2		
59	LSR A	48	1	2	Logical shift right 	N-----ZC
60	LSR dp	49	2	4		
61	LSR dp + X	59	2	5		
62	LSR !abs	58	3	5		
63	MUL	5B	1	9	Multiply : YA ← Y × A	N-----Z-
64	OR #imm	64	2	2	Logical OR A ← (A) ∨ (M)	N-----Z-
65	OR dp	65	2	3		
66	OR dp + X	66	2	4		
67	OR !abs	67	3	4		
68	OR !abs + Y	75	3	5		
69	OR [dp + X]	76	2	6		
70	OR [dp] + Y	77	2	6		
71	OR { X }	74	1	3		
72	ROL A	28	1	2	Rotate left through carry 	N-----ZC
73	ROL dp	29	2	4		
74	ROL dp + X	39	2	5		
75	ROL !abs	38	3	5		
76	ROR A	68	1	2	Rotate right through carry 	N-----ZC
77	ROR dp	69	2	4		
78	ROR dp + X	79	2	5		
79	ROR !abs	78	3	5		
80	SBC #imm	24	2	2	Subtract with carry A ← (A) - (M) - ~(C)	NV--HZC
81	SBC dp	25	2	3		
82	SBC dp + X	26	2	4		
83	SBC !abs	27	3	4		
84	SBC !abs + Y	35	3	5		
85	SBC [dp + X]	36	2	6		
86	SBC [dp] + Y	37	2	6		
87	SBC { X }	34	1	3		
88	TST dp	4C	2	3	Test memory contents for negative or zero (dp) - 00_H	N-----Z-
89	XCN	CE	1	5	Exchange nibbles within the accumulator A_7~A_4 ↔ A_3~A_0	N-----Z-

Register / Memory Operation

NO.	MNEMONIC	OP CODE	BYTE NO	CYCLE NO	OPERATION	FLAG NVGBHIZC
1	LDA #imm	C4	2	2	Load accumulator A ← (M)	N-----Z-
2	LDA dp	C5	2	3		
3	LDA dp + X	C6	2	4		
4	LDA !abs	C7	3	4		
5	LDA !abs + Y	D5	3	5		
6	LDA [dp + X]	D6	2	6		
7	LDA [dp] + Y	D7	2	6		
8	LDA { X }	D4	1	3		
9	LDA { X }+	DB	1	4	X- register auto-increment : A ← (M) , X ← X + 1	
10	LDM dp,#imm	E4	3	5	Load memory with immediate data : (M) ← imm	--------
11	LDX #imm	1E	2	2	Load X-register X ← (M)	N-----Z-
12	LDX dp	CC	2	3		
13	LDX dp + Y	CD	2	4		
14	LDX !abs	DC	3	4		
15	LDY #imm	3E	2	2	Load Y-register Y ← (M)	N-----Z-
16	LDY dp	C9	2	3		
17	LDY dp + X	D9	2	4		
18	LDY !abs	D8	3	4		
19	STA dp	E5	2	4	Store accumulator contents in memory (M) ← A	--------
20	STA dp + X	E6	2	5		
21	STA !abs	E7	3	5		
22	STA !abs + Y	F5	3	6		
23	STA [dp + X]	F6	2	7		
24	STA [dp] + Y	F7	2	7		
25	STA { X }	F4	1	4		
26	STA { X }+	FB	1	4	X- register auto-increment : (M) ← A, X ← X + 1	
27	STX dp	EC	2	4	Store X-register contents in memory (M) ← X	--------
28	STX dp + Y	ED	2	5		
29	STX !abs	FC	3	5		
30	STY dp	E9	2	4	Store Y-register contents in memory (M) ← Y	--------
31	STY dp + X	F9	2	5		
32	STY !abs	F8	3	5		
33	TAX	E8	1	2	Transfer accumulator contents to X-register : X ← A	N-----Z-
34	TAY	9F	1	2	Transfer accumulator contents to Y-register : Y ← A	N-----Z-
35	TSPX	AE	1	2	Transfer stack-pointer contents to X-register : X ← sp	N-----Z-
36	TXA	C8	1	2	Transfer X-register contents to accumulator: A ← X	N-----Z-
37	TXSP	8E	1	2	Transfer X-register contents to stack-pointer: sp ← X	N-----Z-
38	TYA	BF	1	2	Transfer Y-register contents to accumulator: A ← Y	N-----Z-
39	XAX	EE	1	4	Exchange X-register contents with accumulator :X ↔ A	--------
40	XAY	DE	1	4	Exchange Y-register contents with accumulator :Y ↔ A	--------
41	XMA dp	BC	2	5	Exchange memory contents with accumulator (M) ↔ A	N-----Z-
42	XMA dp+X	AD	2	6		
43	XMA {X}	BB	1	5		
44	XYX	FE	1	4	Exchange X-register contents with Y-register : X ↔ Y	--------

16-BIT Operation

NO.	MNEMONIC	OP CODE	BYTE NO	CYCLE NO	OPERATION	FLAG NVGBHIZC
1	ADDW dp	1D	2	5	16-Bits add without carry YA ← (YA) + (dp +1) (dp)	NV--H-ZC
2	CMPW dp	5D	2	4	Compare YA contents with memory pair contents : (YA) – (dp+1)(dp)	N-----ZC
3	DECW dp	BD	2	6	Decrement memory pair (dp+1)(dp) ← (dp+1) (dp) - 1	N-----Z-
4	INCW dp	9D	2	6	Increment memory pair (dp+1) (dp) ← (dp+1) (dp) + 1	N-----Z-
5	LDYA dp	7D	2	5	Load YA YA ← (dp +1) (dp)	N-----Z-
6	STYA dp	DD	2	5	Store YA (dp +1) (dp) ← YA	--------
7	SUBW dp	3D	2	5	16-Bits substact without carry YA ← (YA) - (dp +1) (dp)	NV--H-ZC

Bit Manipulation

NO.	MNEMONIC	OP CODE	BYTE NO	CYCLE NO	OPERATION	FLAG NVGBHIZC
1	AND1 M.bit	8B	3	4	Bit AND C-flag : C ← (C) ∧ (M .bit)	-------C
2	AND1B M.bit	8B	3	4	Bit AND C-flag and NOT : C ← (C) ∧ ~(M .bit)	-------C
3	BIT dp	0C	2	4	Bit test A with memory : Z ← (A) ∧ (M) , N ← (M_7) , V ← (M_6)	MM----Z-
4	BIT !abs	1C	3	5		
5	CLR1 dp.bit	y1	2	4	Clear bit : (M.bit) ← “0”	--------
6	CLRA1 A.bit	2B	2	2	Clear A bit : (A.bit)← “0”	--------
7	CLRC	20	1	2	Clear C-flag : C ← “0”	-------0
8	CLRG	40	1	2	Clear G-flag : G ← “0”	--0-----
9	CLRV	80	1	2	Clear V-flag : V ← “0”	-0--0---
10	EOR1 M.bit	AB	3	5	Bit exclusive-OR C-flag : C ← (C) ⊕ (M .bit)	-------C
11	EOR1B M.bit	AB	3	5	Bit exclusive-OR C-flag and NOT : C ← (C) ⊕ ~(M .bit)	-------C
12	LDC M.bit	CB	3	4	Load C-flag : C ← (M .bit)	-------C
13	LDCB M.bit	CB	3	4	Load C-flag with NOT : C ← ~(M .bit)	-------C
14	NOT1 M.bit	4B	3	5	Bit complement : (M .bit) ← ~(M .bit)	--------
15	OR1 M.bit	6B	3	5	Bit OR C-flag : C ← (C) ∨ (M .bit)	-------C
16	OR1B M.bit	6B	3	5	Bit OR C-flag and NOT : C ← (C) ∨ ~(M .bit)	-------C
17	SET1 dp.bit	x1	2	4	Set bit : (M.bit) ← “1”	--------
18	SETA1 A.bit	0B	2	2	Set A bit : (A.bit) ← “1”	--------
19	SETC	A0	1	2	Set C-flag : C ← “1”	-------1
20	SETG	C0	1	2	Set G-flag : G ← “1”	--1-----
21	STC M.bit	EB	3	6	Store C-flag : (M .bit) ← C	--------
22	TCLR1 !abs	5C	3	6	Test and clear bits with A : A - (M) , (M) ← (M) ∧ ~(A)	N-----Z-
23	TSET1 !abs	3C	3	6	Test and set bits with A : A - (M) , (M) ← (M) ∨ (A)	N-----Z-

Branch / Jump Operation

NO.	MNEMONIC	OP CODE	BYTE NO	CYCLE NO	OPERATION	FLAG NVGBHIZC
1	BBC A.bit,rel	y2	2	4/6	Branch if bit clear : if (bit) = 0 , then pc ← (pc) + rel	--------
2	BBC dp.bit,rel	y3	3	5/7		
3	BBS A.bit,rel	x2	2	4/6	Branch if bit set : if (bit) = 1 , then pc ← (pc) + rel	--------
4	BBS dp.bit,rel	x3	3	5/7		
5	BCC rel	50	2	2/4	Branch if carry bit clear if (C) = 0 , then pc ← (pc) + rel	--------
6	BCS rel	D0	2	2/4	Branch if carry bit set if (C) = 1 , then pc ← (pc) + rel	--------
7	BEQ rel	F0	2	2/4	Branch if equal if (Z) = 1 , then pc ← (pc) + rel	--------
8	BMI rel	90	2	2/4	Branch if minus if (N) = 1 , then pc ← (pc) + rel	--------
9	BNE rel	70	2	2/4	Branch if not equal if (Z) = 0 , then pc ← (pc) + rel	--------
10	BPL rel	10	2	2/4	Branch if minus if (N) = 0 , then pc ← (pc) + rel	--------
11	BRA rel	2F	2	4	Branch always pc ← (pc) + rel	--------
12	BVC rel	30	2	2/4	Branch if overflow bit clear if (V) = 0 , then pc ← (pc) + rel	--------
13	BVS rel	B0	2	2/4	Branch if overflow bit set if (V) = 1 , then pc ← (pc) + rel	--------
14	CALL !abs	3B	3	8	Subroutine call M(sp)←(pc_H), sp←sp - 1, M(sp)← (pc_L), sp ←sp - 1, if !abs, pc← abs ; if [dp], pc_L← (dp), pc_H← (dp+1) .	--------
15	CALL [dp]	5F	2	8		
16	CBNE dp,rel	FD	3	5/7	Compare and branch if not equal : if (A) ≠ (M) , then pc ← (pc) + rel.	--------
17	CBNE dp+X,rel	8D	3	6/8		
18	DBNE dp,rel	AC	3	5/7	Decrement and branch if not equal : if (M) ≠ 0 , then pc ← (pc) + rel.	--------
19	DBNE Y,rel	7B	2	4/6		
20	JMP !abs	1B	3	3	Unconditional jump pc ← jump address	--------
21	JMP [!abs]	1F	3	5		
22	JMP [dp]	3F	2	4		
23	PCALL upage	4F	2	6	U-page call M(sp) ←(pc_H), sp ←sp - 1, M(sp) ← (pc_L), sp ← sp - 1, pc_L ← (upage), pc_H ← "$0FF_H$" .	--------
24	TCALL n	nA	1	8	Table call : (sp) ←(pc_H), sp ← sp - 1, M(sp) ← (pc_L),sp ← sp - 1, pc_L ← (Table vector L), pc_H ← (Table vector H)	--------

Control Operation & Etc.

NO.	MNEMONIC	OP CODE	BYTE NO	CYCLE NO	OPERATION	FLAG NVGBHIZC
1	BRK	0F	1	8	Software interrupt : B ← ”1”, M(sp) ← (pc_H), sp ←sp-1, M(s) ← (pc_L), sp ← sp - 1, M(sp) ← (PSW), sp ← sp -1, pc_L ← ($0FFDE_H$) , pc_H ← ($0FFDF_H$) .	---1-0--
2	DI	60	1	3	Disable interrupts : I ← “0”	-----0--
3	EI	E0	1	3	Enable interrupts : I ← “1”	-----1--
4	NOP	FF	1	2	No operation	--------
5	POP A	0D	1	4	sp ← sp + 1, A ← M(sp)	--------
6	POP X	2D	1	4	sp ← sp + 1, X ← M(sp)	
7	POP Y	4D	1	4	sp ← sp + 1, Y ← M(sp)	
8	POP PSW	6D	1	4	sp ← sp + 1, PSW ← M(sp)	restored
9	PUSH A	0E	1	4	M(sp) ← A , sp ← sp - 1	--------
10	PUSH X	2E	1	4	M(sp) ← X , sp ← sp - 1	
11	PUSH Y	4E	1	4	M(sp) ← Y , sp ← sp - 1	
12	PUSH PSW	6E	1	4	M(sp) ← PSW , sp ← sp - 1	
13	RET	6F	1	5	Return from subroutine sp ← sp +1, pc_L ← M(sp), sp ← sp +1, pc_H ← M(sp)	--------
14	RETI	7F	1	6	Return from interrupt sp ← sp +1, PSW ← M(sp), sp ← sp + 1, pc_L ← M(sp), sp ← sp + 1, pc_H ← M(sp)	restored
15	STOP	EF	1	3	Stop mode (halt CPU, stop oscillator)	--------

B. MASK ORDER SHEET(MC80C0304)

MASK ORDER & VERIFICATION SHEET

P:Pb Free

MC80C0304-MC ☐☐☐ ☐☐

B, G, D or D32

Customer should write inside thick line box.

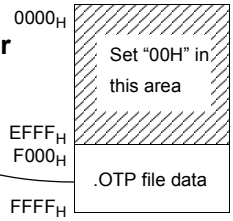
1. Customer Information

Company Name	
Application	
Order Date	YYYY MM DD • •
Tel: E-mail:	Fax:
Name & Signature:	

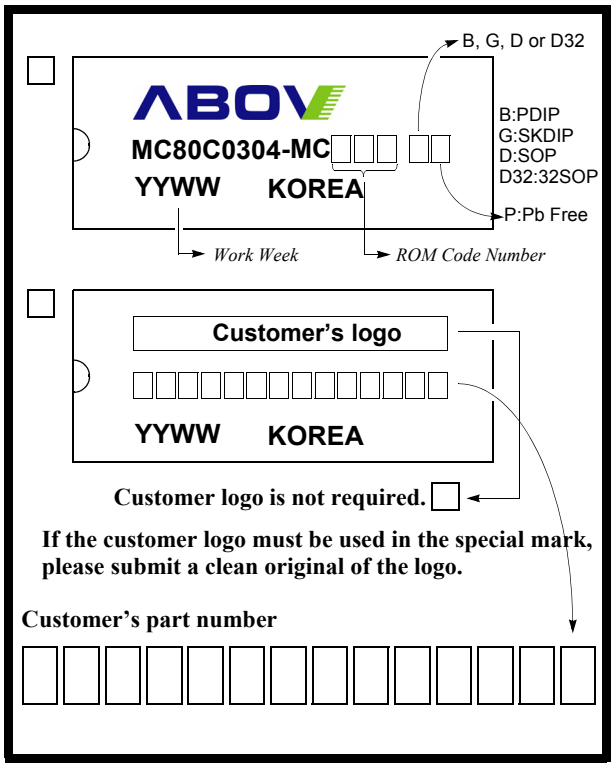
2. Device Information

Package	☐ 28SKDIP ☐ 32PDIP	☐ 28SOP ☐ 32SOP	
ROM Size	☐ 4K ☐ 8K	☐ 16K	
POR Use	☐ Yes	☐ No	
If POR is "Yes",	R35 Use	☐ Yes	☐ No
If POR is "No",	R35 Use		☐ No
ONP Use	☐ Yes	☐ No	
If ONP is "Yes",	OFP Use	☐ Yes	☐ No
	CLK Use	☐ Crystal ☐ IN4M ☐ IN4MXO ☐ IN2M ☐ IN2MXO ☐ EXRC ☐ EXRCXO	
If ONP is "No",	OFP Use		☐ No
	CLK Use	☐ Crystal ☐ EXRC ☐ EXRCXO	
Mask Data	File Name: (.OTP) Check Sum: ( )		

Notice : Unused user ROM area should be filled with "00H"



3. Marking Specification



(Please check mark into ☐)

4. Delivery Schedule

	Date	Quantity	ABOV Confirmation
Customer Sample	YYYY MM DD • •	pcs	
Risk Order	• •	pcs	

5. ROM Code Verification

Verification Date:	• •	Tel:	Fax:
Check Sum:		Name & Signature:	
E-mail:			

ABOV SEMICONDUCTOR

04-NOV-2011

C. MASK ORDER SHEET(MC80C0308)

MASK ORDER & VERIFICATION SHEET

MC80C0308-MC ☐☐☐ ☐ ☐

P:Pb Free

B, G, D or D32

Customer should write inside thick line box.

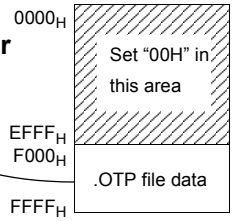
1. Customer Information

Company Name	
Application	
Order Date	YYYY MM DD • •
Tel: E-mail:	Fax:
Name & Signature:	

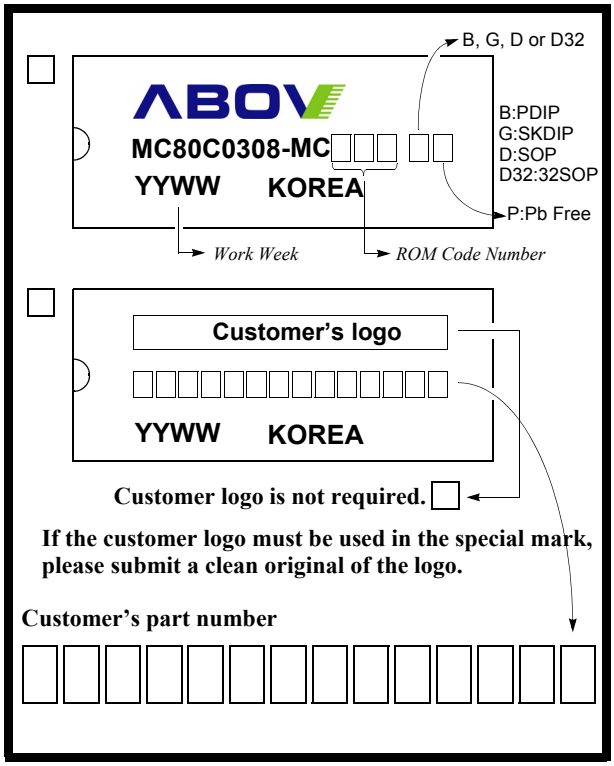
2. Device Information

Package	☐ 28SKDIP ☐ 32PDIP	☐ 28SOP ☐ 32SOP	
ROM Size	☐ 4K ☐ 8K	☐ 16K	
POR Use	☐ Yes	☐ No	
If POR is "Yes",	R35 Use	☐ Yes	☐ No
If POR is "No",	R35 Use		☐ No
ONP Use	☐ Yes	☐ No	
If ONP is "Yes",	OFP Use	☐ Yes	☐ No
	CLK Use	☐ Crystal ☐ IN4M ☐ IN4MXO ☐ IN2M ☐ IN2MXO ☐ EXRC ☐ EXRCXO	
If ONP is "No",	OFP Use		☐ No
	CLK Use	☐ Crystal ☐ EXRC ☐ EXRCXO	
Mask Data	File Name: (.OTP) Check Sum: ( )		

Notice : Unused user ROM area should be filled with "00H"



3. Marking Specification



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4. Delivery Schedule

	Date	Quantity	ABOV Confirmation
Customer Sample	YYYY MM DD • •	pcs	
Risk Order	• •	pcs	

5. ROM Code Verification

Verification Date:	• •	Tel:	Fax:
Check Sum:		Name & Signature:	
E-mail:			

ABOV SEMICONDUCTOR

04-NOV-2011

D. MASK ORDER SHEET(MC80C0316)

MASK ORDER & VERIFICATION SHEET

MC80C0316-MC ☐☐☐ ☐☐

P:Pb Free

B, G, D or D32

Customer should write inside thick line box.

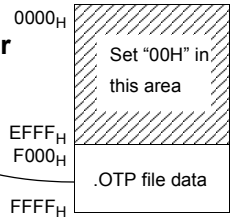
1. Customer Information

Company Name	
Application	
Order Date	YYYY MM DD • •
Tel: E-mail:	Fax:
Name & Signature:	

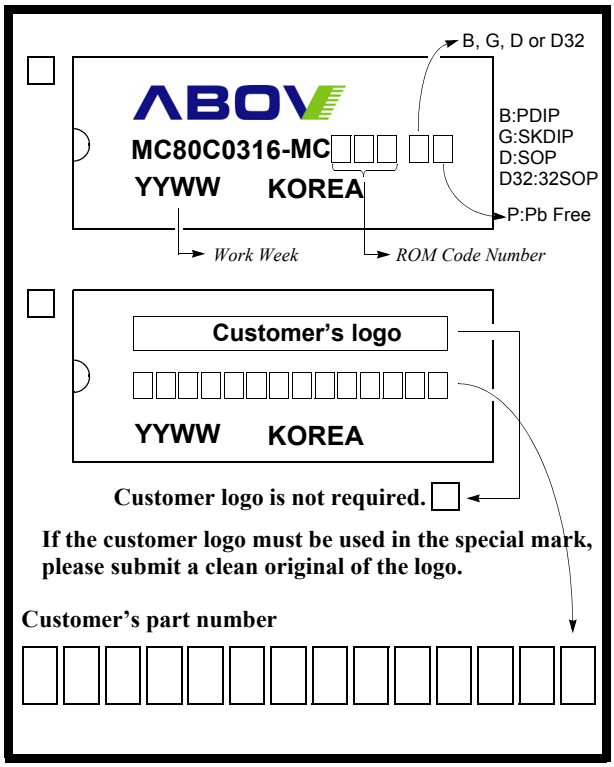
2. Device Information

Package	☐ 28SKDIP ☐ 32PDIP	☐ 28SOP ☐ 32SOP	
ROM Size	☐ 4K ☐ 8K	☐ 16K	
POR Use	☐ Yes	☐ No	
If POR is "Yes",	R35 Use	☐ Yes	☐ No
If POR is "No",	R35 Use		☐ No
ONP Use	☐ Yes	☐ No	
If ONP is "Yes",	OFP Use	☐ Yes	☐ No
	CLK Use	☐ Crystal ☐ IN4M ☐ IN4MXO ☐ IN2M ☐ IN2MXO ☐ EXRC ☐ EXRCXO	
If ONP is "No",	OFP Use		☐ No
	CLK Use	☐ Crystal ☐ EXRC ☐ EXRCXO	
Mask Data	File Name: (.OTP) Check Sum: ( )		

Notice : Unused user ROM area should be filled with "00H"



3. Marking Specification



(Please check mark into ☐)

4. Delivery Schedule

	Date	Quantity	ABOV Confirmation
Customer Sample	YYYY MM DD • •	pcs	
Risk Order	• •	pcs	

5. ROM Code Verification

Verification Date:	• •	Tel:	Fax:
Check Sum:		Name & Signature:	
E-mail:			

ABOV SEMICONDUCTOR

04-NOV-2011