



SPP9527W

P-Channel Enhancement Mode MOSFET

DESCRIPTION

The SPP9527W is the P-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology.

This high density process is especially tailored to minimize on-state resistance.

These devices are particularly suited for low voltage application , notebook computer power management and other battery powered circuits where high-side switching .

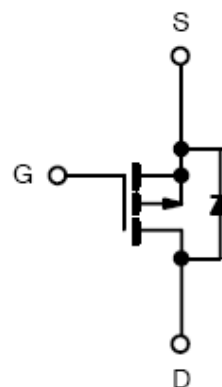
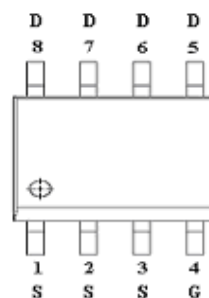
FEATURES

- ◆ $-40V/-10A, R_{DS(ON)} = 38m\Omega @ V_{GS} = -10V$
- ◆ $-40V/-8A, R_{DS(ON)} = 46m\Omega @ V_{GS} = -4.5V$
- ◆ Super high density cell design for extremely low $R_{DS(ON)}$
- ◆ Exceptional on-resistance and maximum DC current capability
- ◆ SOP – 8P package design

APPLICATIONS

- Power Management in Note book
- Portable Equipment
- Battery Powered System
- DC/DC Converter
- Load Switch
- DSC
- LCD Display inverter

PIN CONFIGURATION(SOP – 8P)



PART MARKING



A : Lot Code
B : Date Code



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PIN DESCRIPTION

Pin	Symbol	Description
1	S	Source
2	S	Source
3	S	Source
4	G	Gate
5	D	Drain
6	D	Drain
7	D	Drain
8	D	Drain

ORDERING INFORMATION

Part Number	Package	Part Marking
SPP9527WS8RGB	SOP- 8P	SPP9527W

※ SPP9527WS8RGB 13" Tape Reel ; Pb – Free ; Halogen – Free

ABSOLUTE MAXIMUM RATINGS

(TA=25°C Unless otherwise noted)

Parameter		Symbol	Typical	Unit
Drain-Source Voltage		V _{DSS}	-40	V
Gate –Source Voltage		V _{GSS}	±20	V
Continuous Drain Current(T _J =150°C)	T _A =25°C	I _D	-10	A
	T _A =70°C		-8	
Pulsed Drain Current		I _{DM}	-30	A
Continuous Source Current(Diode Conduction)		I _S	-2.3	A
Power Dissipation	T _A =25°C	P _D	2.8	W
	T _A =70°C		1.8	
Operating Junction Temperature		T _J	-55/150	°C
Storage Temperature Range		T _{STG}	-55/150	°C
Thermal Resistance-Junction to Ambient		R _{θJA}	70	°C/W



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ELECTRICAL CHARACTERISTICS

(T_A=25°C Unless otherwise noted)

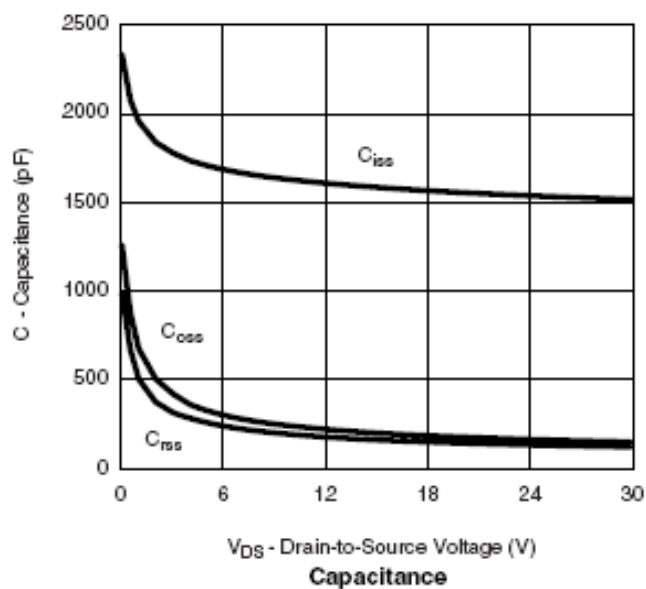
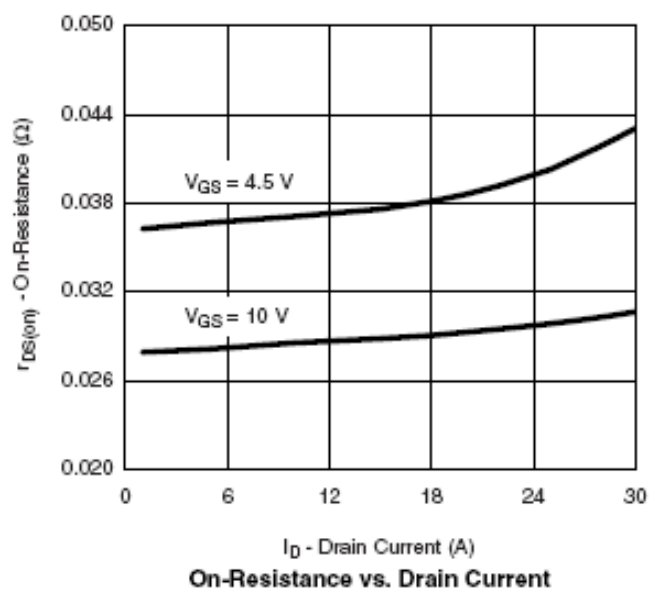
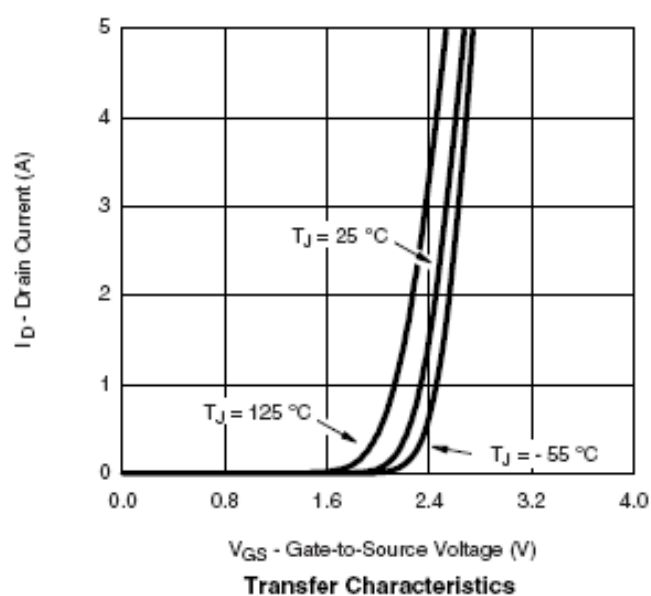
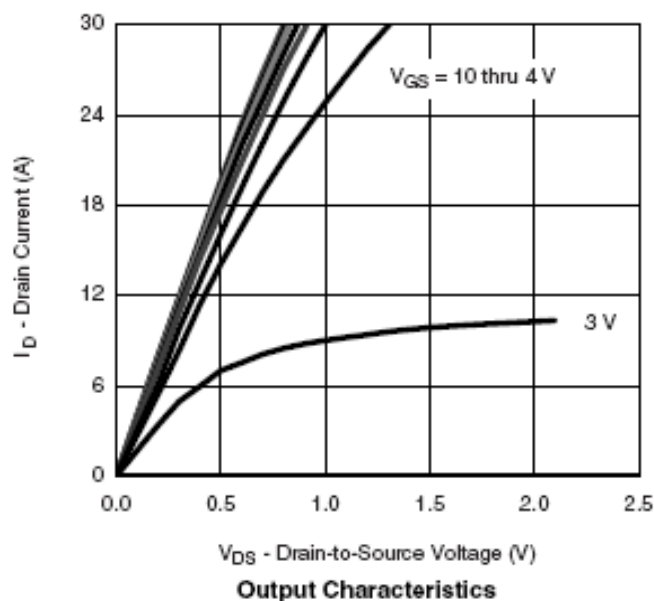
Parameter	Symbol	Conditions	Min.	Typ	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} =0V, I _D =-250uA	-40			V
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =-250uA	-0.8		-2.5	
Gate Leakage Current	I _{GSS}	V _{DS} =0V, V _{GS} =±20V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =-32V, V _{GS} =0V			-1	uA
		V _{DS} =-32V, V _{GS} =0V T _J =55°C			-10	
On-State Drain Current	I _{D(on)}	V _{DS} = -5V, V _{GS} = -4.5V	-10			A
Drain-Source On-Resistance	R _{DS(on)}	V _{GS} =-10V, I _D =-10A		0.032	0.038	Ω
		V _{GS} =-4.5V, I _D =- 8A		0.036	0.046	
Forward Transconductance	g _{fs}	V _{DS} =-15V, I _D =-5.7A		13		S
Diode Forward Voltage	V _{SD}	I _S =-2.3A, V _{GS} =0V		-0.8	-1.2	V
Dynamic						
Total Gate Charge	Q _g	V _{DS} =-20V, V _{GS} =-4.5V I _D = -5.0A		13	20	nC
Gate-Source Charge	Q _{gs}			4.5		
Gate-Drain Charge	Q _{gd}			6.5		
Input Capacitance	C _{iss}	V _{DS} =-20V, V _{GS} =0V f=1MHz		1100		pF
Output Capacitance	C _{oss}			145		
Reverse Transfer Capacitance	C _{rss}			115		
Turn-On Time	t _{d(on)}	V _{DD} =-20V, R _L =4Ω I _D =-5.0A, V _{GEN} =-4.5V R _G =1Ω		40	80	nS
	t _r			55	100	
Turn-Off Time	t _{d(off)}			30	60	
	t _f			12	20	



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TYPICAL CHARACTERISTICS

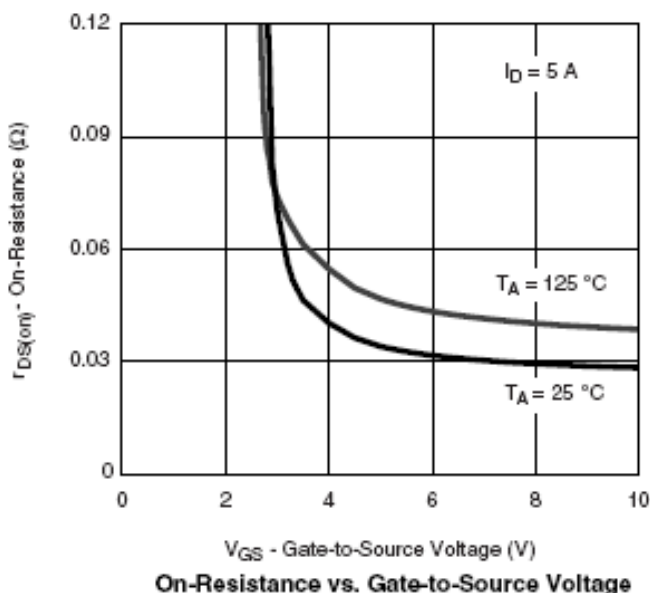
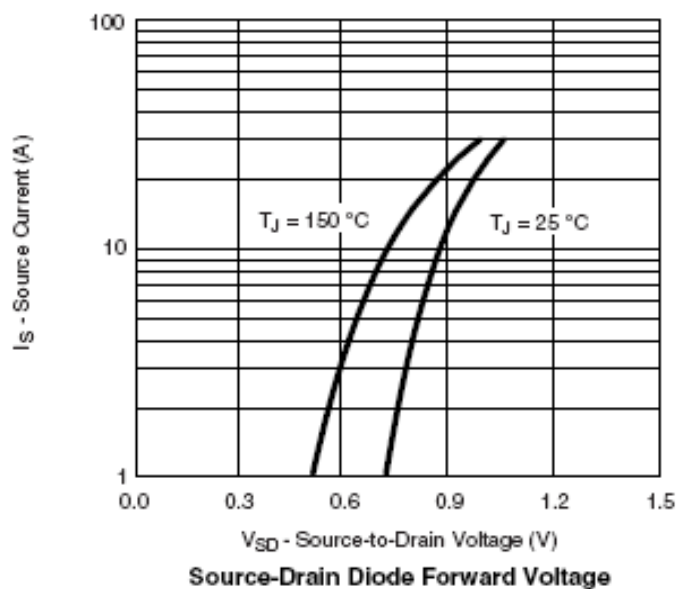
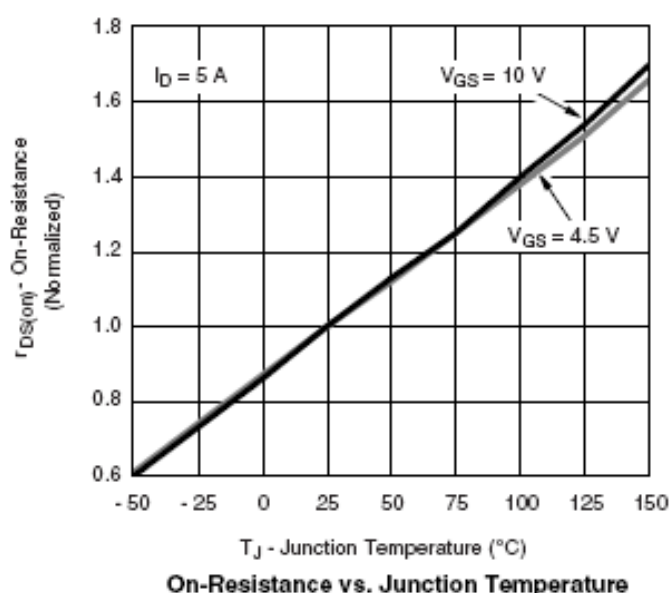
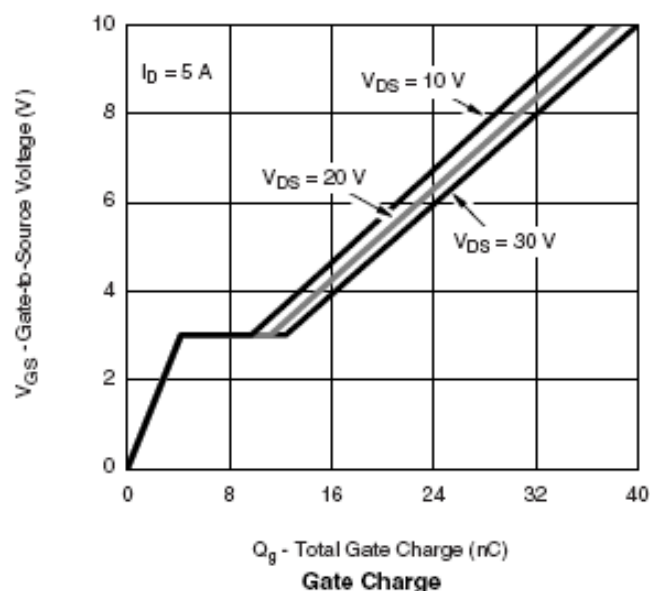




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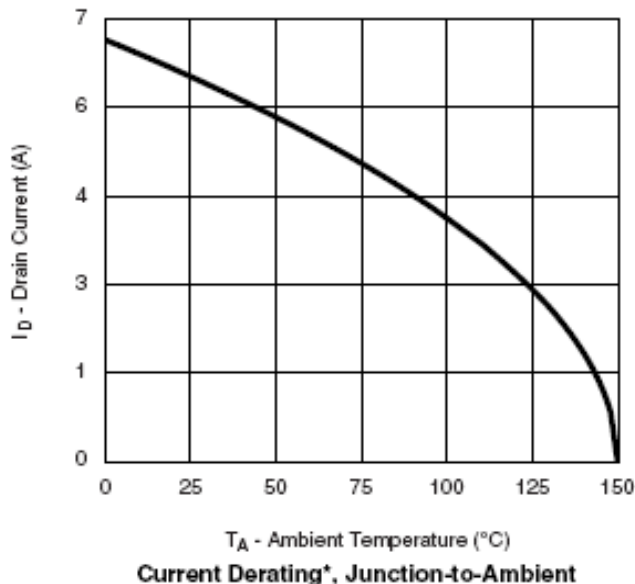
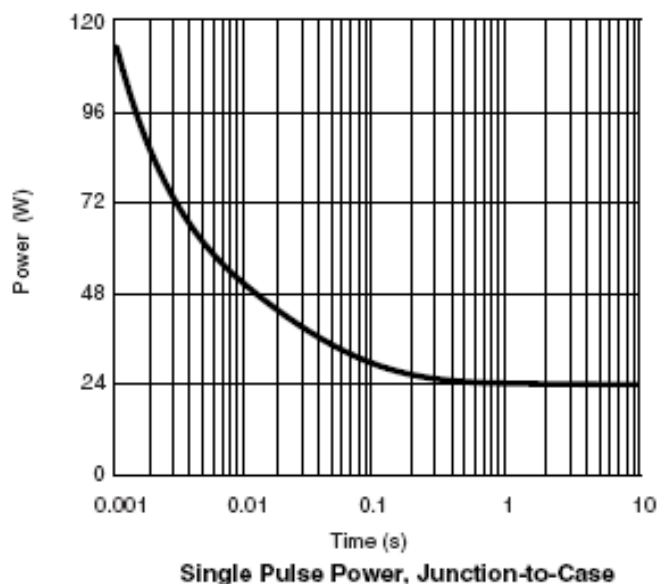
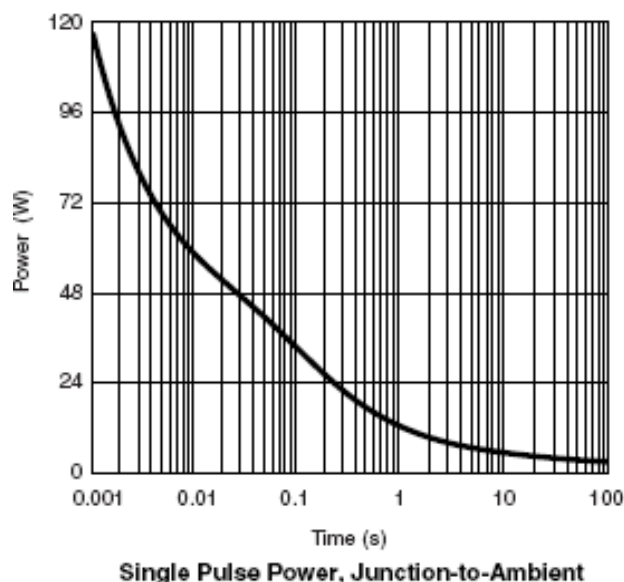
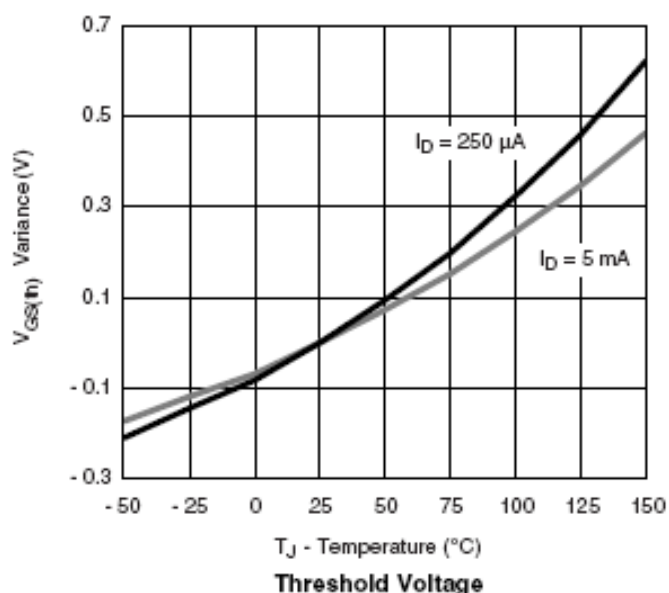




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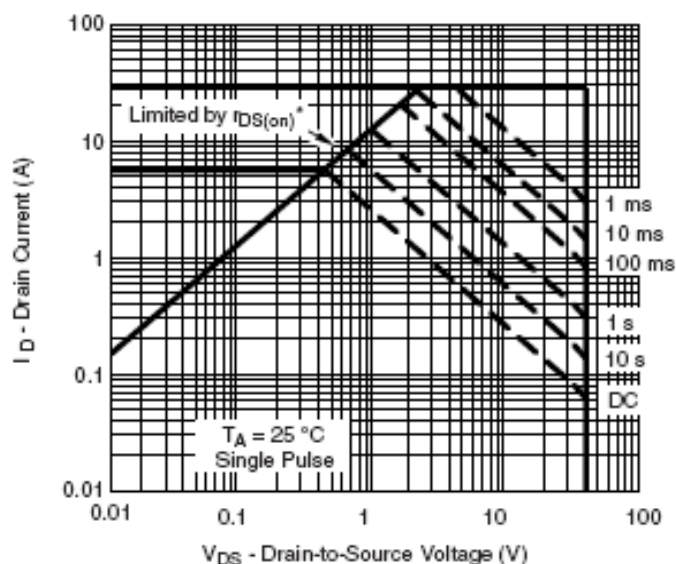




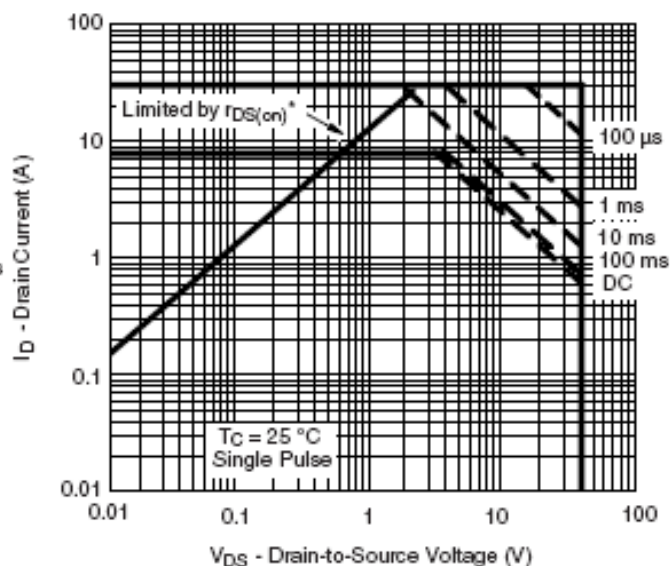
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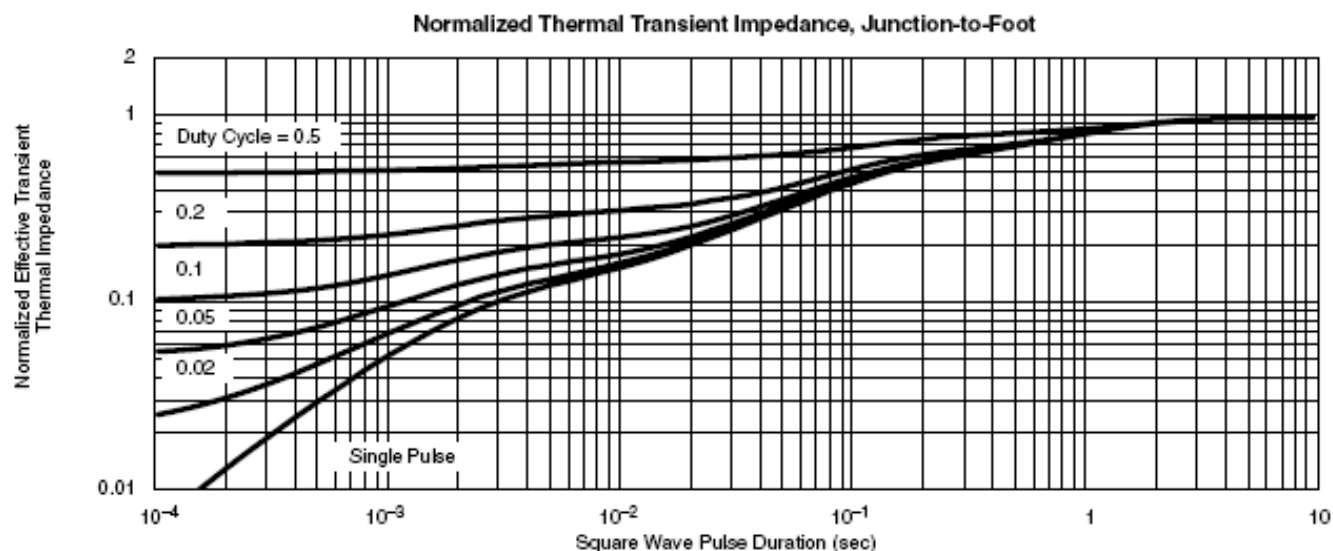
TYPICAL CHARACTERISTICS



* $V_{GS} >$ minimum V_{GS} at which $r_{DS(on)}$ is specified
Safe Operating Area, Junction-to-Ambient



* $V_{GS} >$ minimum V_{GS} at which $r_{DS(on)}$ is specified
Safe Operating Area, Junction-to-Case

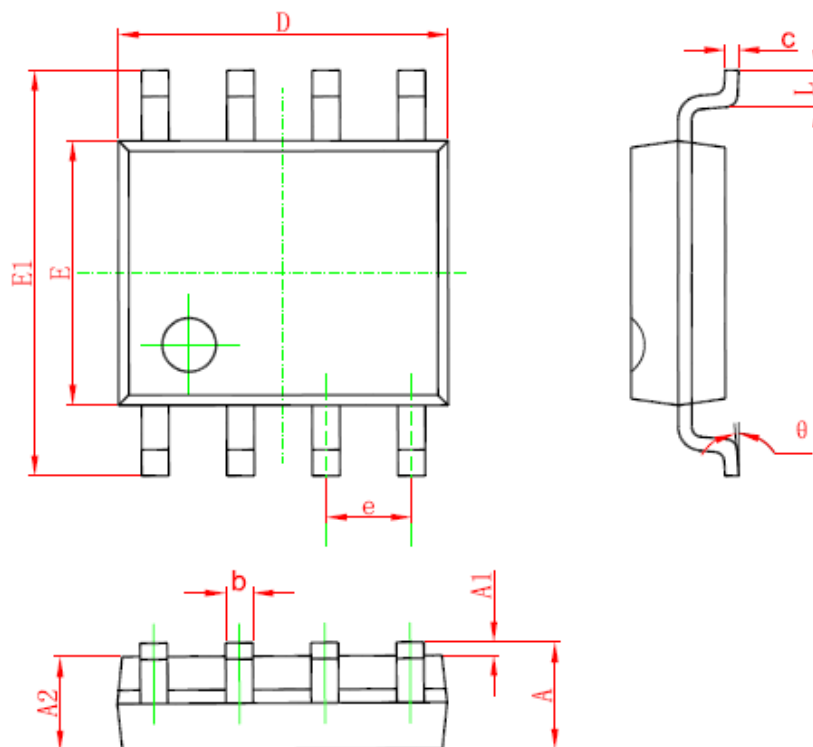




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SOP- 8 PACKAGE OUTLINE



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°



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