MICROCHIP

SST12CP21

2.4 GHz High-Gain, High-Efficiency Power Amplifier

Features

- High Gain:
  - Typically 39 dB gain across 2.4–2.5 GHz over temperature -20°C to +85°C
- High linear output power:
  - >30 dBm P1dB
    - Please refer to "Absolute Maximum Stress Ratings" on page 5
  - Meets 802.11g OFDM spectrum mask requirement up to 28 dBm
  - Typically 25 dBm with <3% EVM, 802.11g, 54 Mbps, 350 mA current
  - Typically 24 dBm with <2.5% EVM, 802.11n, MCS7-HT20, 50% duty cycle
  - Typically 23 dBm with <1.75% EVM, MCS9-HT40, 50% duty cycle, 320 mA current
  - Meets 802.11b ACPR requirement up to 28 dBm with 30% power-added efficiency
- High-speed power-up/down
  - Turn on/off time (10%-90%) <100 ns
- 10:1 VSWR survivability (unconditionally stable up to 28 dBm)
- On-chip power detection
  - >20 dB dynamic range
  - VSWR- and temperature-insensitive
- Simple input/output matching
- Packages available
  - 16-contact UQFN (3mm x 3mm)
- All non-Pb (lead-free) devices are RoHS compliant

Applications

- WLAN (IEEE 802.11b/g/n)
- WLAN 256 QAM
- AP router
- Home RF
- Cordless phones
- 2.4 GHz ISM wireless equipment

1.0 PRODUCT DESCRIPTION

SST12CP21 is a high-power and high-gain power amplifier (PA) based on the highly-reliable InGaP/GaAs HBT technology.

This PA can be easily configured for high-power applications with high power-added efficiency while operating over the 2.4-2.5 GHz frequency band. It typically provides 39 dB gain with 25% power-added efficiency @ P_{OUT} = 28 dBm for 802.11g.

SST12CP21 has excellent linearity, typically 25 dBm at 3% EVM with 54 Mbps 802.11g operation while meeting 802.11g spectrum mask at 28 dBm. SST12CP21 also has a single-ended power detector which lowers the users' cost for power control.

The power amplifier IC also features easy board-level usage along with high-speed power-up/-down control.

SST12CP21 is offered in 16-contact UQFN package. See Figure 3-1 for pin assignments and Table 4-1 for pin descriptions.

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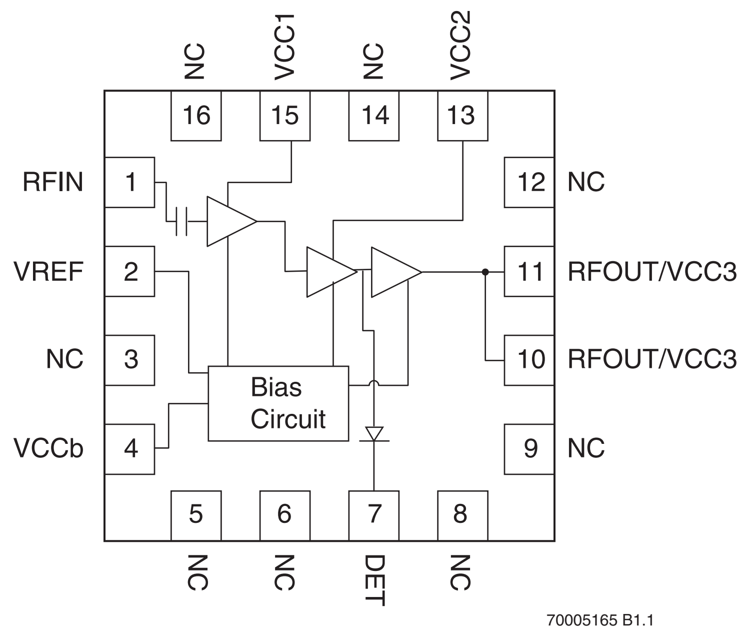
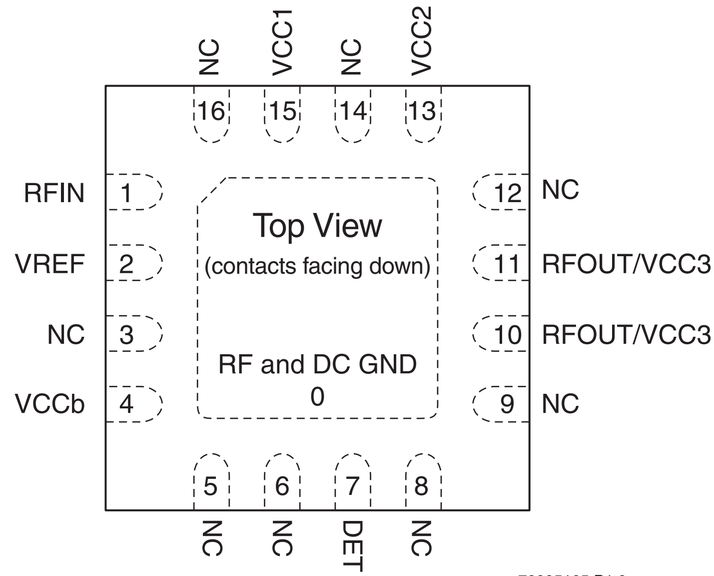
2.0 FUNCTIONAL BLOCKS

FIGURE 2-1: FUNCTIONAL BLOCK DIAGRAM



3.0 PIN ASSIGNMENTS

FIGURE 3-1: PIN ASSIGNMENTS FOR 16-CONTACT UQFN



4.0 PIN DESCRIPTIONS

TABLE 4-1: PIN DESCRIPTION

Symbol	Pin No.	Pin Name	Type[1]	Function
GND	0	Ground		The center pad should be connected to RF ground
RFIN	1	RF_{IN}	I	RF input, DC decoupled
VREF	2	V_{REF}	PWR	PA enable and idle-current control
NC	3	No Connection		No Internal Connection
VCCb	4	Power Supply	PWR	Supply voltage for bias circuit
NC	5	No Connection		No Internal Connection
NC	6	No Connection		No Internal Connection
VDET	7	V_{DET}	O	On-chip power detector
NC	8	No Connection		No Internal Connection
NC	9	No Connection		No Internal Connection
RFOUT	10	RF_{OUT}	O	RF output
RFOUT	11	RF_{OUT}	O	RF output
NC	12	No Connection		No Internal Connection
VCC2	13	V_{CC2}	PWR	PWR power supply, 2nd stage
NC	14	NC		No Internal Connection
VCC1	15	$V_{CC1'}$	PWR	PWR power supply, 1st stage
NC	16	No Connection		No Internal Connection

1. I=Input, O=Output

5.0 ELECTRICAL SPECIFICATIONS

The DC and RF specifications for the power amplifier are specified below. Refer to Table 5-2 for the DC voltage and current specifications.

Absolute Maximum Stress Ratings (Applied conditions greater than those listed under "Absolute Maximum Stress Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

Input power to pin 1 (P_{IN})[1] . . . . +12 dBm
Supply voltage at pins 4, 10, 11, 13 and 15 (V_{CC}) . . . . +6 V
Reference voltage to pin 2 (V_{REF1}) . . . . +3.2 V
DC supply current (I_{CC}) . . . . 600 mA
Operating Temperature (T_A) . . . . -40ºC to +85ºC
Storage Temperature (T_{STG}) . . . . -40ºC to +120ºC
Maximum Junction Temperature (T_J) . . . . +150ºC
Surface Mount Solder Reflow Temperature . . . . 260°C for 10 seconds

1. Maximum input power for V_{CC} = 5V with 50% duty cycle, 802.11g 54 Mbps, with maximum output VSWR = 10:1. At V_{CC} = 5V, a 10Ω resistor must be included on V_{CC1}, as shown in Figures 6-8 and 6-9.

TABLE 5-1: OPERATING RANGE

Range	Ambient Temp	V_{CC}
Industrial	-20°C to +85°C	5.0V

TABLE 5-2: DC ELECTRICAL CHARACTERISTICS AT 25ºC

Symbol	Parameter	Min.	Typ	Max.	Unit
V_{CC}	Supply Voltage	4.0	5.0	5.5	V
I_{CC}	DC Current				
	for 802.11g, 28 dBm		440		mA
	for 802.11b, 28 dBm		440		mA
I_{CQ}	Idle Current		275		mA
V_{REG}	Reference Voltage see Figure 6-8 on page 10	2.9	2.95	3.1	V
I_{REG}	Reference Current		8		mA

TABLE 5-3: AC ELECTRICAL CHARACTERISTICS FOR CONFIGURATION AT V_{CC} = 5V, V_{REF} = 2.95V, 25ºC, 50% DUTY CYCLE

Symbol	Parameter	Min.	Typ	Max.	Unit
F_{L-U}	Frequency range in 802.11b/g applications	2400		2500	MHz
P_{OUT}	Output power at 3% EVM with 802.11g OFDM at 54 Mbps		25		dBm
	Output power at 2.5% EVM with 802.11n MCS7 HT20		24		dBm
	Output power at 1.75% EVM with 256 QAM MCS9 HT40		23		dBm
	Output power meeting 802.11g spectral mask, 6 Mbps		28		dBm
	Output power meeting 802.11n HT20 spectral mask		26		dBm
	Output power meeting MCS9-HT40 spectral mask		26		dBm
	Output power meeting 802.11b spectral mask with 11 Mbps CCK		28		dBm
G	Power gain for 802.11b/g/n/256 QAM	37	39		dB
G_{VAR}	Gain variation over band			±0.5	dB
2f	Second Harmonic at 29 dBm, 802.11b mask compliance[1]		-50		dBm/MHz
3f	Third Harmonic at 29 dBm, 802.11b mask compliance[1]		-50		dBm/MHz

1. See Figure 6-9

6.0 TYPICAL PERFORMANCE CHARACTERISTICS

Test Conditions: V_{CC} = 5.0V, V_{REG} = 2.95V, T_A = 25°C, IEEE 802.11g, 54 Mbps, 50% duty cycle unless otherwise specified

FIGURE 6-1: S-PARAMETER

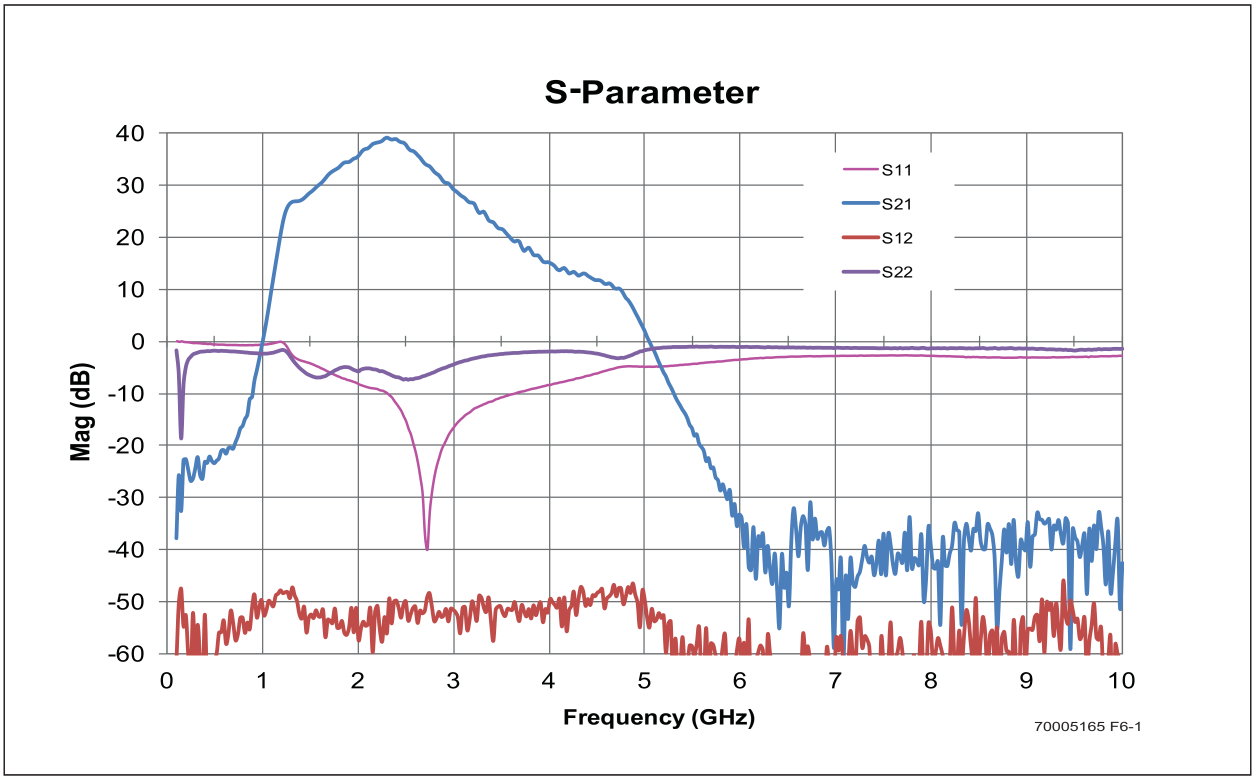


FIGURE 6-2: DYNAMIC EVM VERSUS OUTPUT POWER

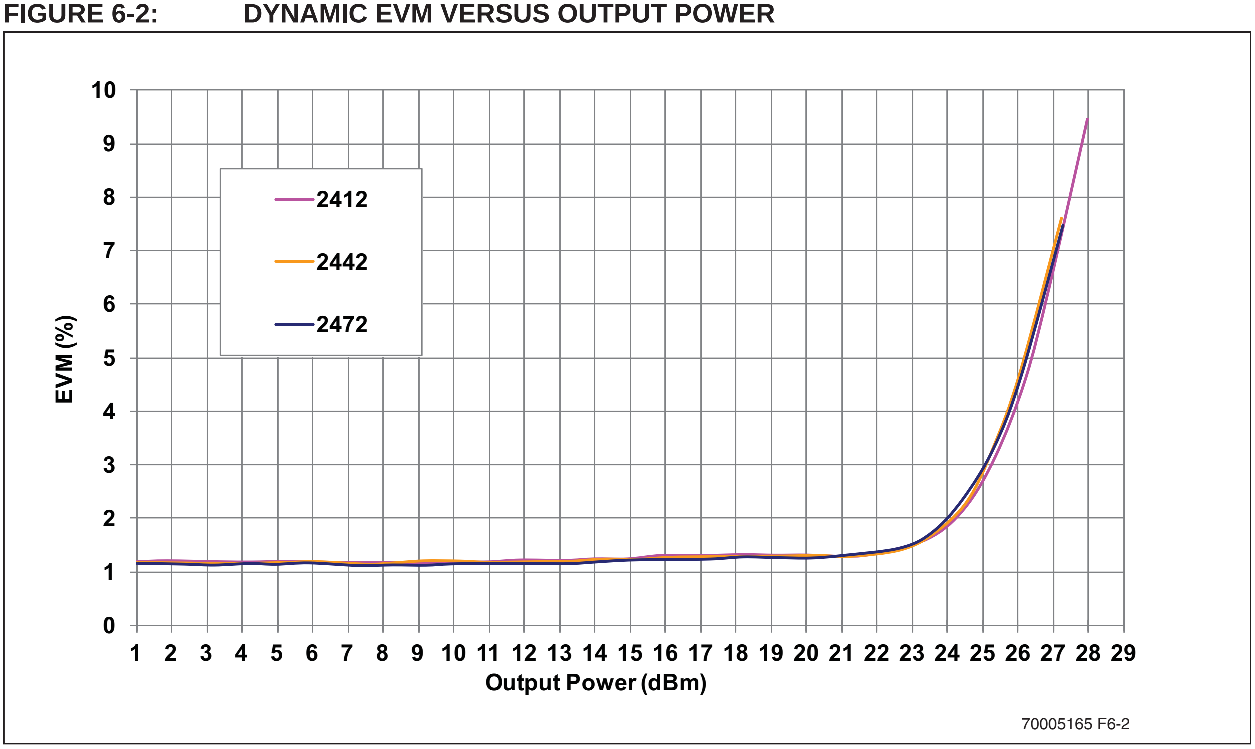


FIGURE 6-3: DYNAMIC EVM VERSUS OUTPUT POWER 802.11AC, MCS0-HT40, 50% DUTY CYCLE

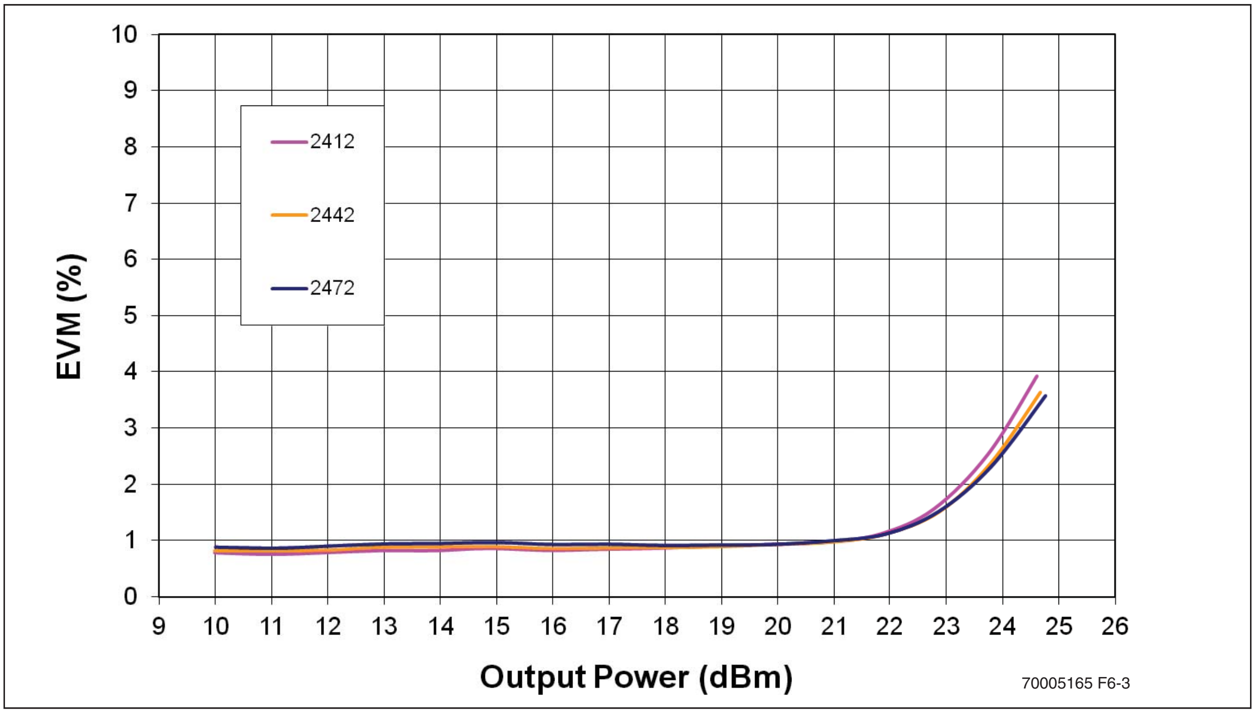


FIGURE 6-4: POWER GAIN VERSUS OUTPUT POWER

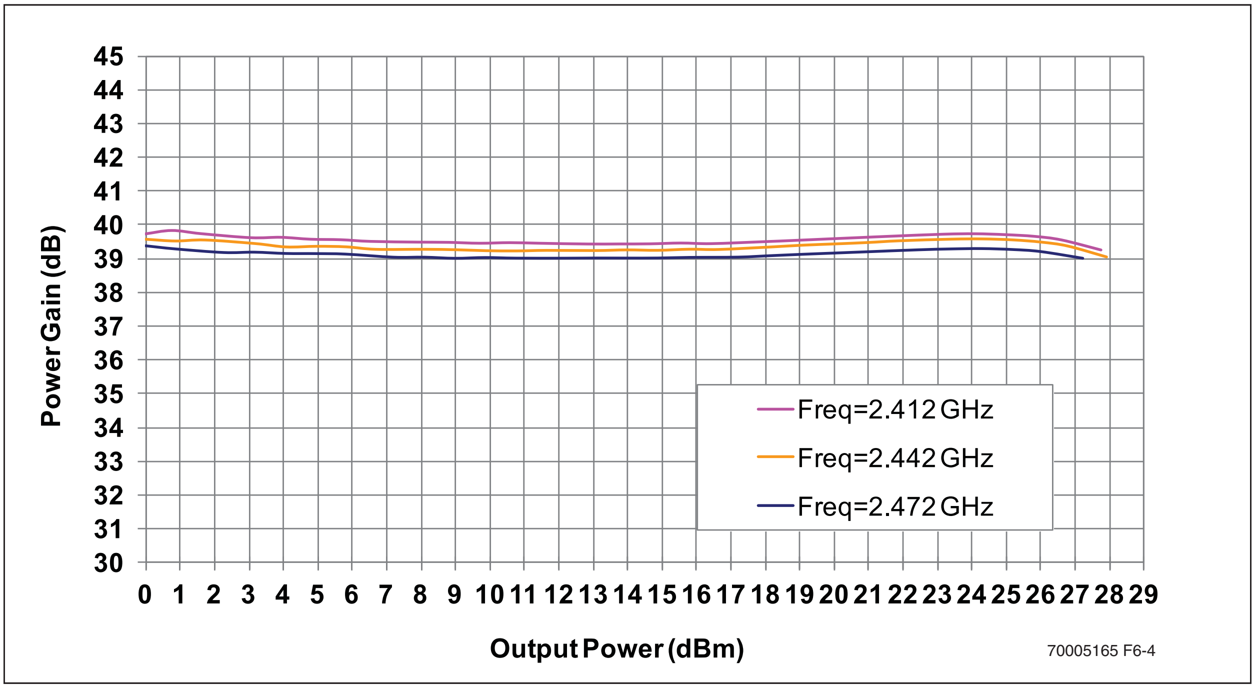


FIGURE 6-5: DC CURRENT VERSUS OUTPUT POWER

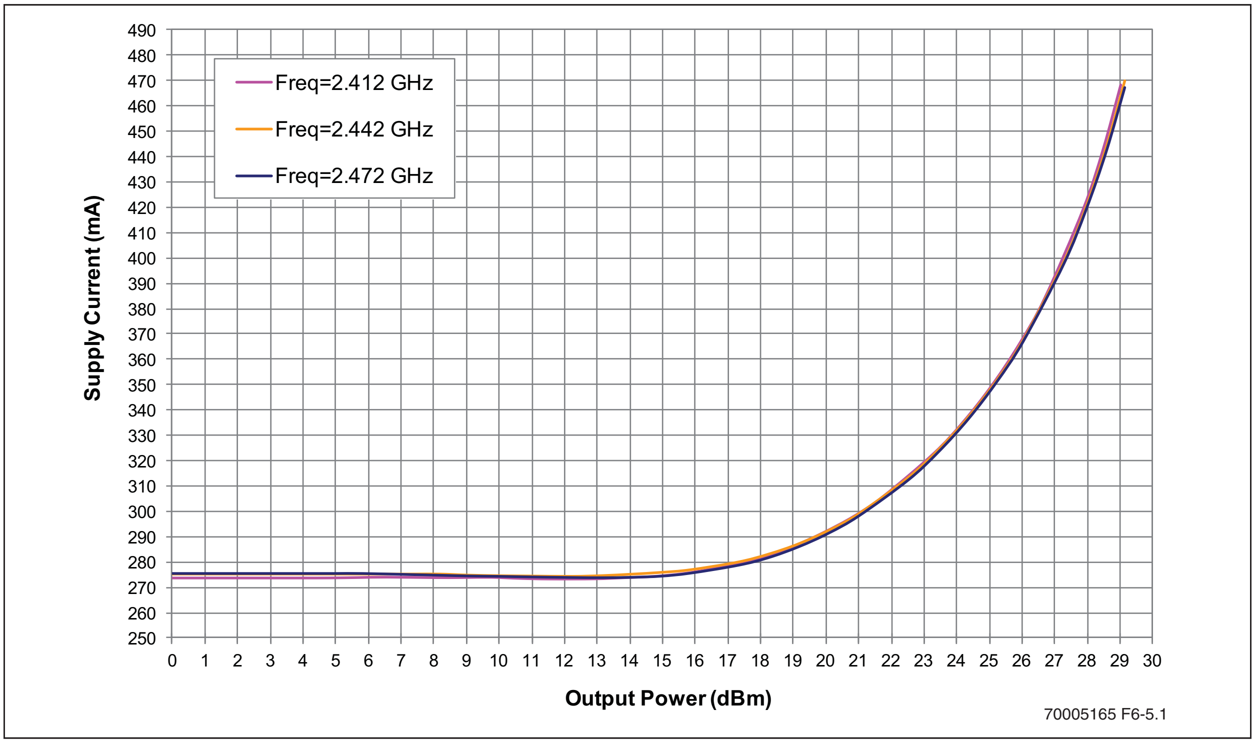


FIGURE 6-6: DETECTOR OUTPUT VOLTAGE VERSUS OUTPUT POWER

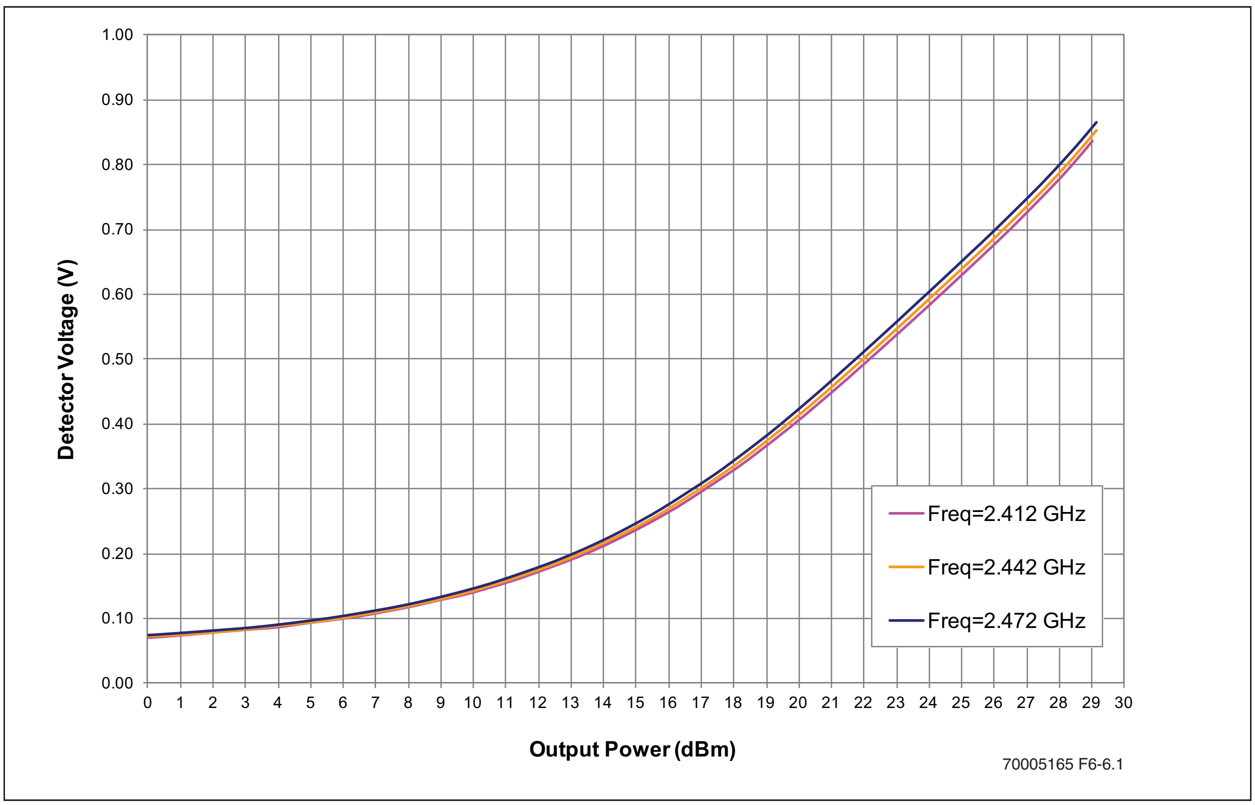


FIGURE 6-7: DYNAMIC EVM VERSUS OUTPUT POWER (WITH HARMONIC FILTER)

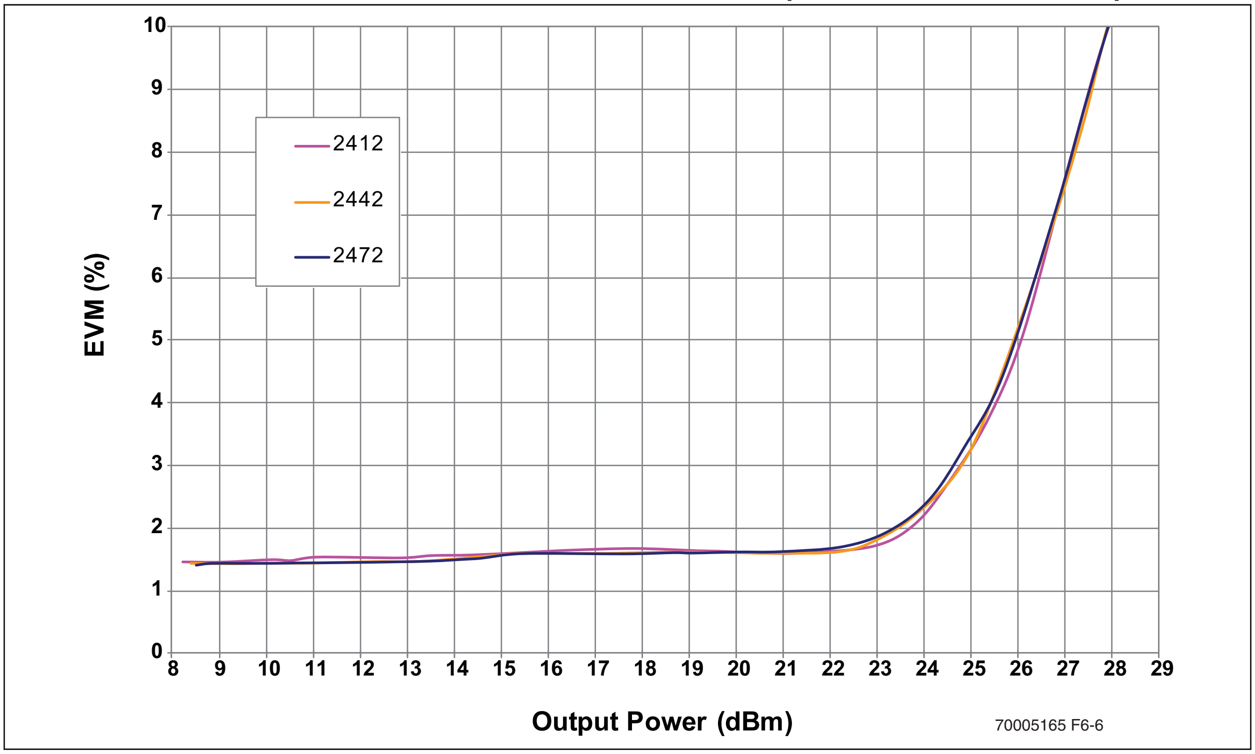


FIGURE 6-8: TYPICAL SCHEMATIC FOR 256 QAM APPLICATIONS

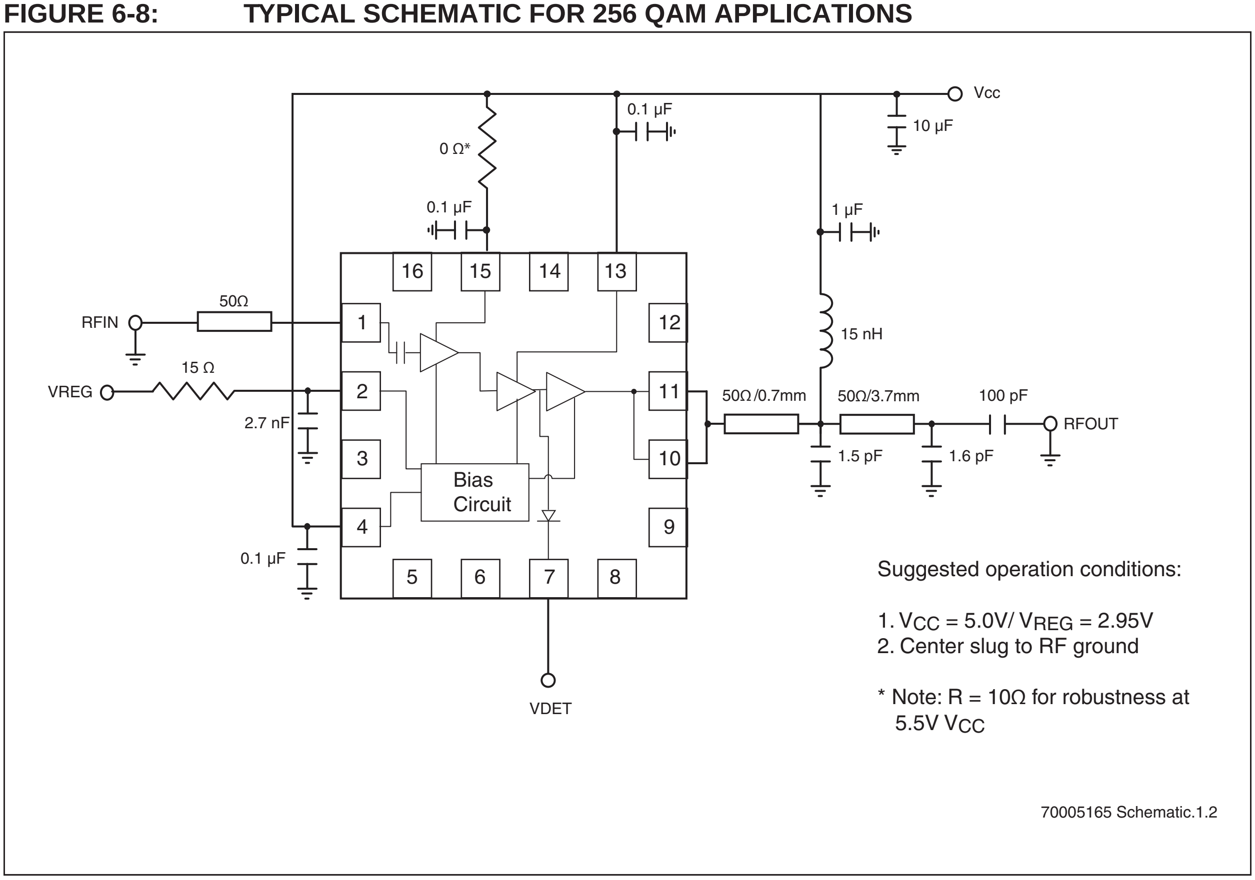
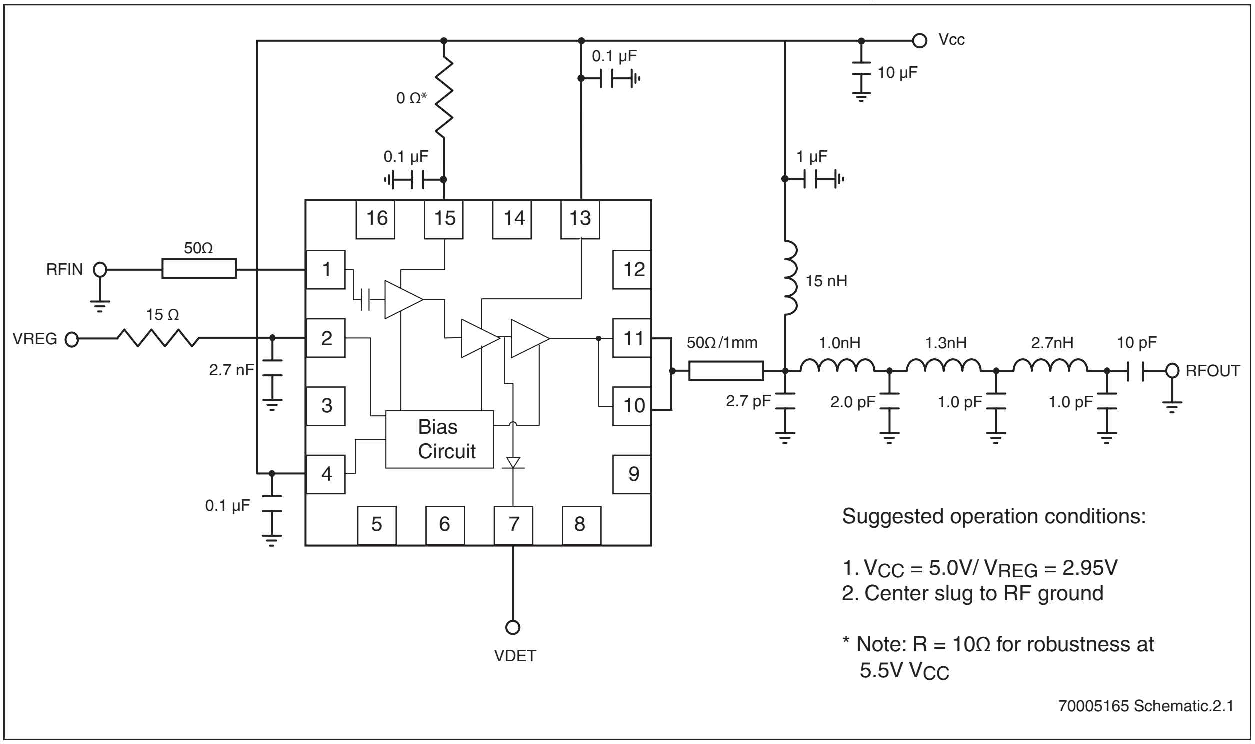


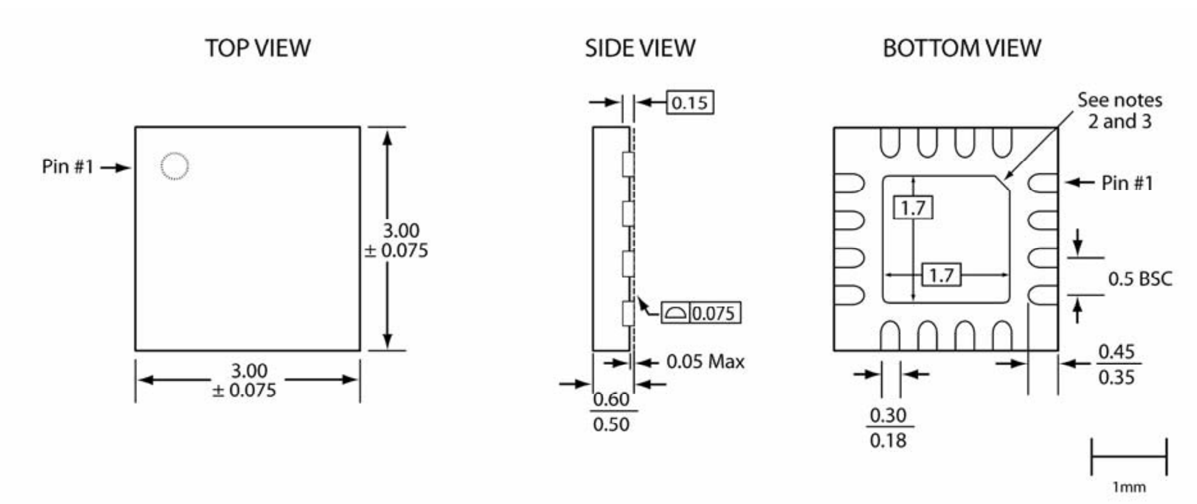
FIGURE 6-9: SCHEMATIC WITH HARMONIC FILTER FOR 256 QAM APPLICATIONS



7.0 PACKAGING DIAGRAMS

16-Lead Ultra Thin Quad Flatpack No-Leads (QUCE/F) - 3x3 mm Body [UQFN]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



16-uqfn-3x3-QUC-0.0

Note:

1. Complies with JEDEC JEP95 MO-248D, variant UEED-4 except external paddle nominal dimensions.
2. From the bottom view, the pin #1 indicator may be either a 45-degree chamfer or a half-circle notch.
3. The external paddle is electrically connected to the die back-side and possibly to certain VSS leads. This paddle can be soldered to the PC board; it is suggested to connect this paddle to the VSS of the unit. Connection of this paddle to any other voltage potential can result in shorts and/or electrical malfunction of the device
4. Untoleranced dimensions are nominal target dimensions.
5. All linear dimensions are in millimeters (max/min).

Microchip Technology Drawing C04-14014A Sheet 1 of 1

TABLE 7-1: REVISION HISTORY

Revision	Description	Date
A	• Initial release of data sheet	Aug 2014

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 Preliminary

8.0 PRODUCT IDENTIFICATION SYSTEM

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PART NO.	XXX
Device	Package

Device:	SST12CP21	= 2.4 GHz High-Gain, High-Efficiency Power Amplifier
Package:	QUCE	= UQFN (3mm x 3mm), 0.6 max thickness 16-contact
Evaluation Kit Flag	K	= Evaluation Kit

Valid Combinations:

SST12CP21-QUCE
SST12CP21-QUCE-K

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