

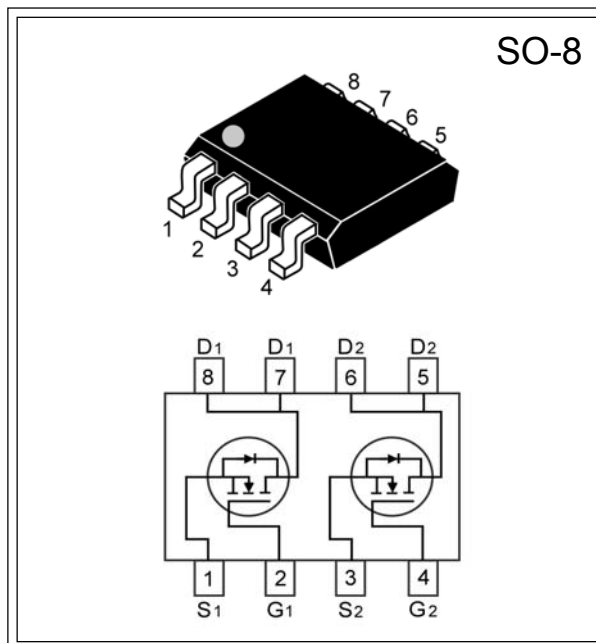
SSM9926

Dual N-Channel Enhancement Mode MOSFET

Product Summary		
V_{DS} (V)	I_D (A)	$R_{DS(ON)}$ (m Ω) Max
20V	5A	30 @ $V_{GS} = 4.0V$
		40 @ $V_{GS} = 2.5V$

FEATURES

- ◆ Super high dense cell design for low $R_{DS(ON)}$.
- ◆ Rugged and reliable.
- ◆ Surface Mount Package.



ABSOLUTE MAXIMUM RATINGS ($T_A=25^{\circ}C$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	20	V
Gate-Source Voltage	V_{GS}	± 10	V
Drain Current-Continuous @ $T_c=25^{\circ}C$ - Pulsed ^b	I_D	5	A
	I_{DM}	25	A
Drain-Source Diode Forward Current ^a	I_S	1.7	A
Maximum Power Dissipation ^a	P_D	2	W
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150	$^{\circ}C$

THERMAL CHARACTERISTICS

Thermal Resistance, Junction-to-Ambient ^a	$R_{\theta JA}$	62.5	$^{\circ}C/W$
--	-----------------	------	---------------

South Sea Semiconductor reserves the right to make changes to improve reliability or manufacturability without advance notice.

South Sea Semiconductor, July 2005 (Rev 1.0)



ELECTRICAL CHARACTERISTICS ($T_A=25^{\circ}\text{C}$ unless otherwise noted)						
Parameter	Symbol	Condition	Min	Typ ^c	Max	Unit
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	20			V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=-16V, V_{GS}=0V$			1	μA
Gate-Body Leakage	I_{GSS}	$V_{GS}=\pm 10V, V_{DS}=0V$			± 100	nA
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	0.6			V
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=4.0V, I_D=5A$		25	30	m Ω
		$V_{GS}=2.5V, I_D=5A$		35	40	
Forward Transconductance	g_{FS}	$V_{DS}=5V, I_D=6A$		12		S
Input Capacitance	C_{ISS}	$V_{DS}=8V,$		908		pF
Output Capacitance	C_{OSS}	$V_{GS}=0V,$		192		
Reverse Transfer Capacitance	C_{RSS}	$f=1.0\text{MHz}$		151		
Turn-On Delay Time	$t_{D(on)}$	$V_D=10V, I_D=1A,$ $V_{GEN}=4.5V,$ $R_{GEN}=10\Omega,$ $R_L=10\Omega$		35		ns
Rise Time	t_r			13		
Turn-Off Delay Time	$t_{D(off)}$			45		
Fall Time	t_f			25		
Total Gate Charge	Q_g	$V_{DS}=10V,$ $I_D=1A,$ $V_{GS}=4.5V$		15		nC
Gate-Source Charge	Q_{gs}			2.5		
Gate-Drain Charge	Q_{gd}			2.5		
Diode Forward Voltage	V_{SD}	$V_{GS}=0V, I_S=1.7A$		0.7	1.2	V

Notes :

- Surface Mounted on FR4 Board, $t \leq 10\text{sec}$.
- Pulse Test : Pulse Width $\leq 300\mu\text{s}$, Duty Cycle $\leq 2\%$.
- Guaranteed by design, not subject to production testing.

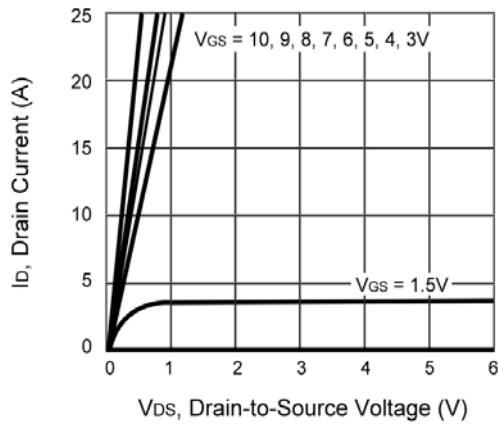


Figure 1. Output Characteristics

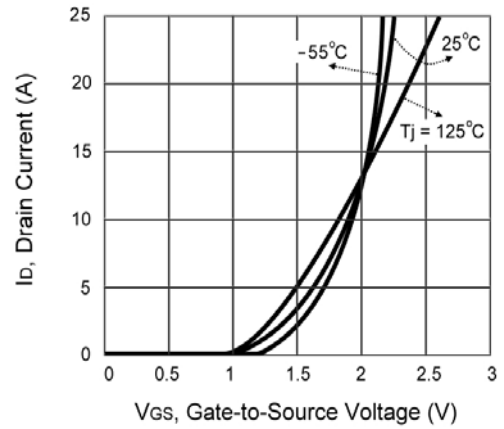


Figure 2. Transfer Characteristics

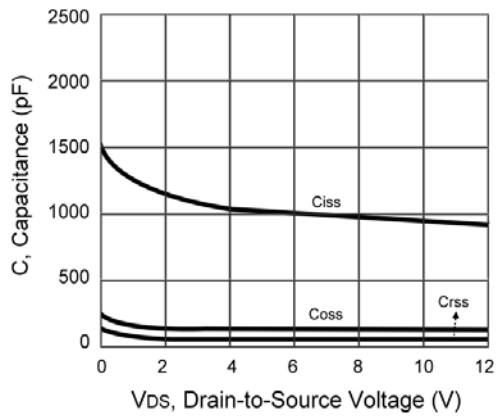


Figure 3. Capacitance

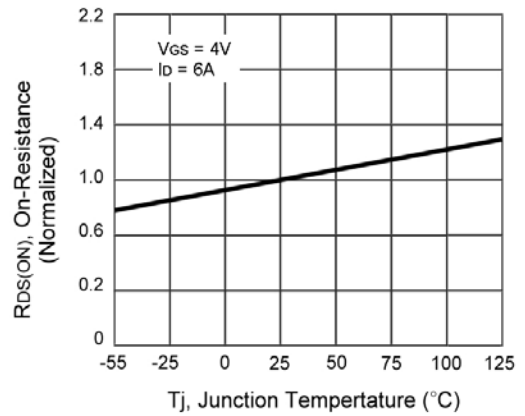


Figure 4. On-Resistance Variation with Temperature

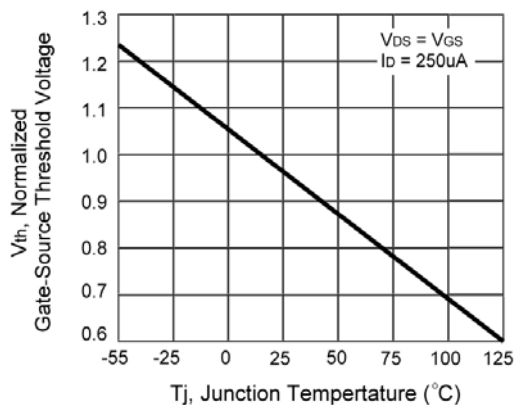


Figure 5. Gate Threshold Variation with Temperature

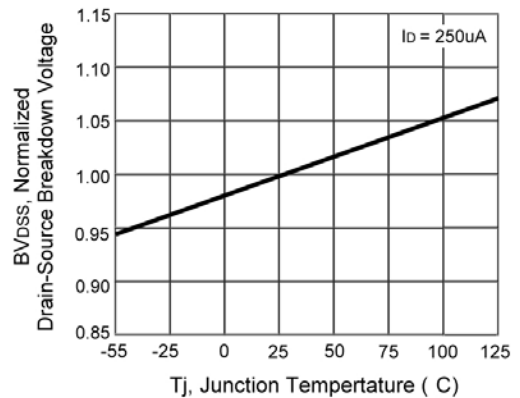


Figure 6. Breakdown Voltage Variation with Temperature

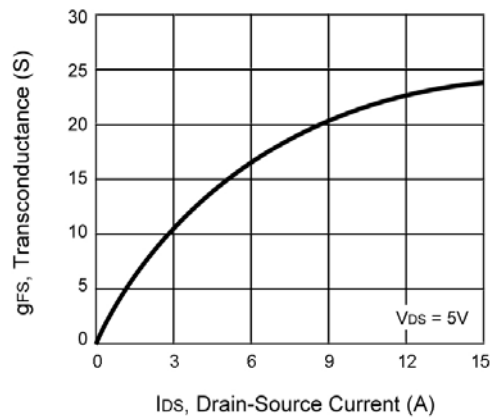


Figure 7. Transconductance Variation with Drain Current

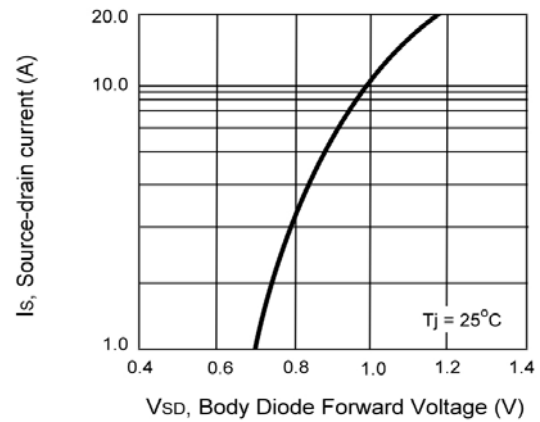


Figure 8. Body Diode Forward Voltage Variation with Source Current

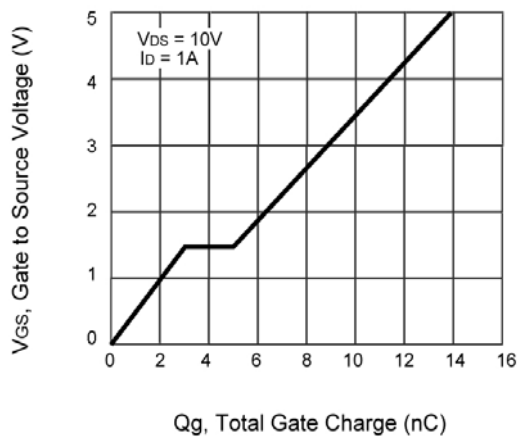


Figure 9. Gate Charge

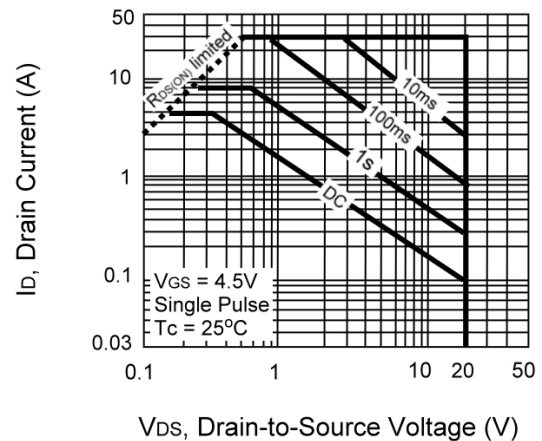


Figure 10. Maximum Safe Operating Area

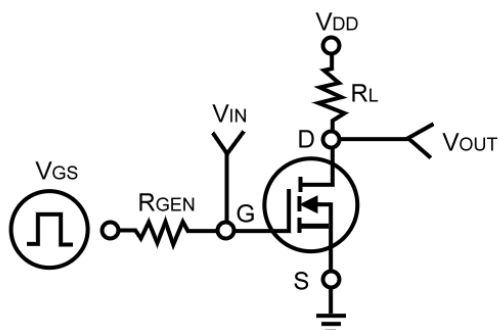


Figure 11. Switching Test Circuit

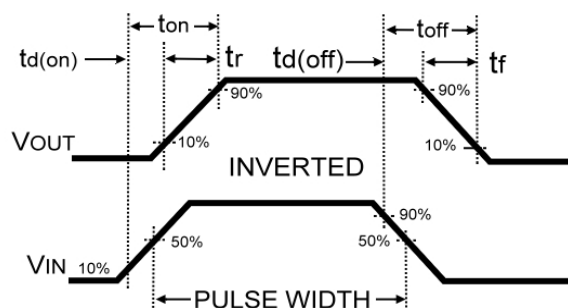


Figure 12. Switching Waveforms

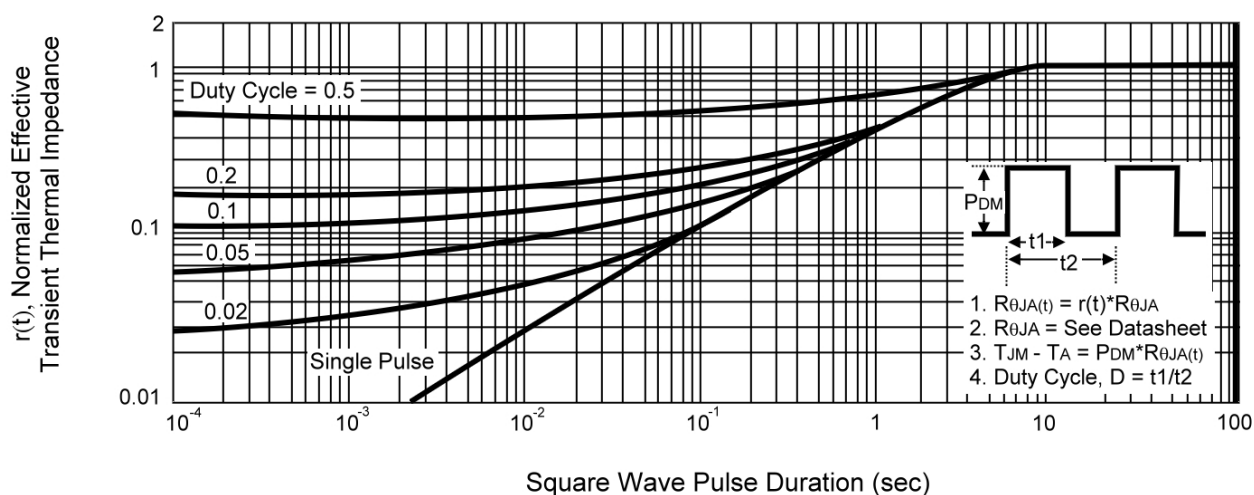
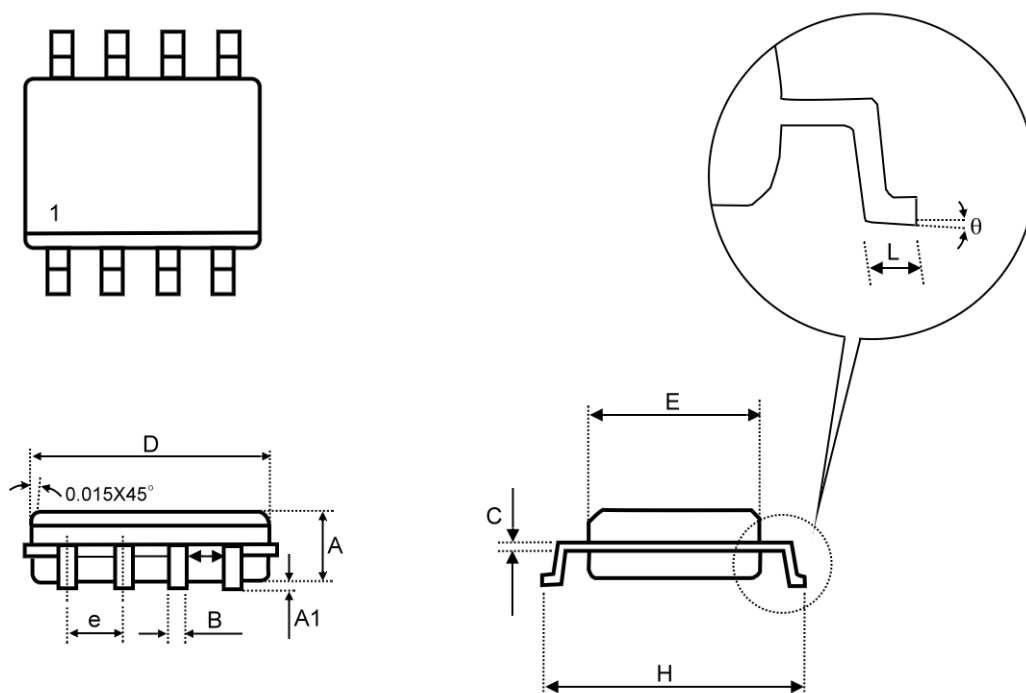


Figure 13. Normalized Thermal Transient Impedance Curve



Package Outline Dimensions

SO-8

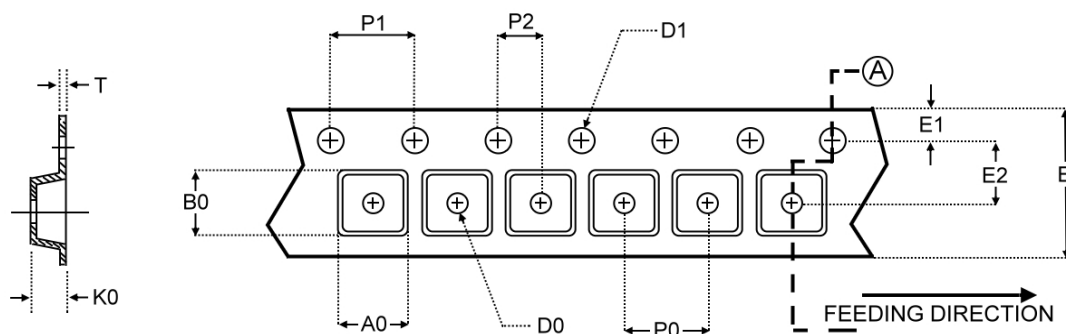


SYMBOLS	MILLIMETERS		INCHES	
	Min.	Max.	Min.	Max.
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
B	0.41 TYP.		0.016 TYP.	
C	0.20 TYP.		0.008 TYP.	
D	4.80	4.98	0.189	0.196
E	3.81	3.99	0.150	0.157
e	1.25 TYP.		0.05 TYP.	
H	5.79	6.20	0.228	0.244
L	0.41	1.27	0.016	0.050
θ	0°	8°	0°	8°



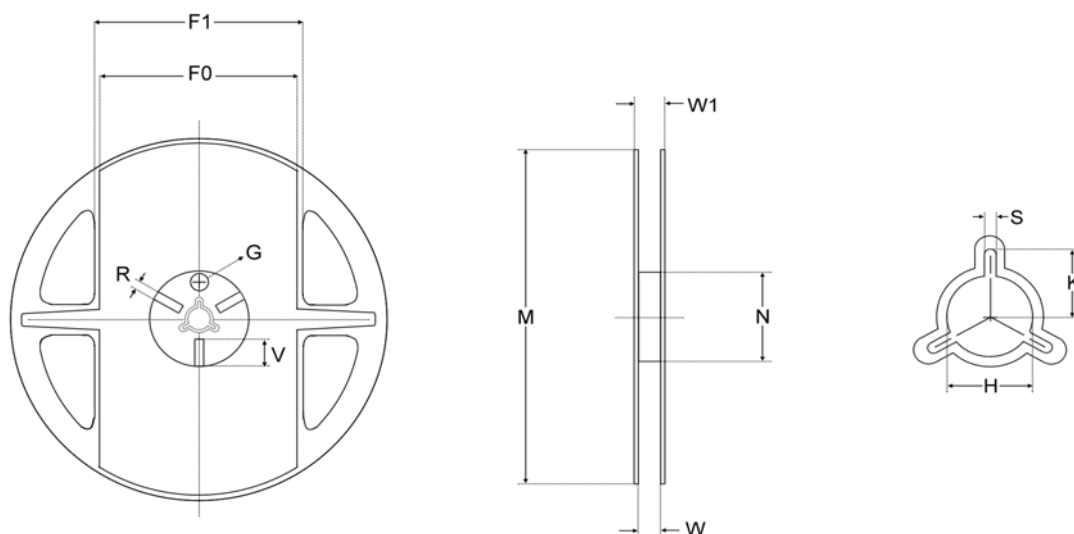
Carrier Tape & Reel Dimensions

SO-8



Package	A0	B0	K0	D0	D1	E	E1	E2	P0	P1	P2	T
SOP 8N 150mil	6.40	5.20	2.10	$\phi 1.50$ (Min.)	$\phi 1.50$ + 0.10 - 0.00	12.00 ± 0.30	1.75	5.50 ± 0.05	8.00	4.00	2.00 ± 0.05	0.30 ± 0.05

UNIT : mm



Tape Size	Reel Size	M	N	W	W1	H	K	S	G	R	V
12mm	$\phi 330$	330 ± 1	62 ± 1.5	12.4 + 0.2	16.8 - 0.4	$\phi 12.75$ 0.15	-	2.0 ± 0.15	-	-	-

UNIT : mm