

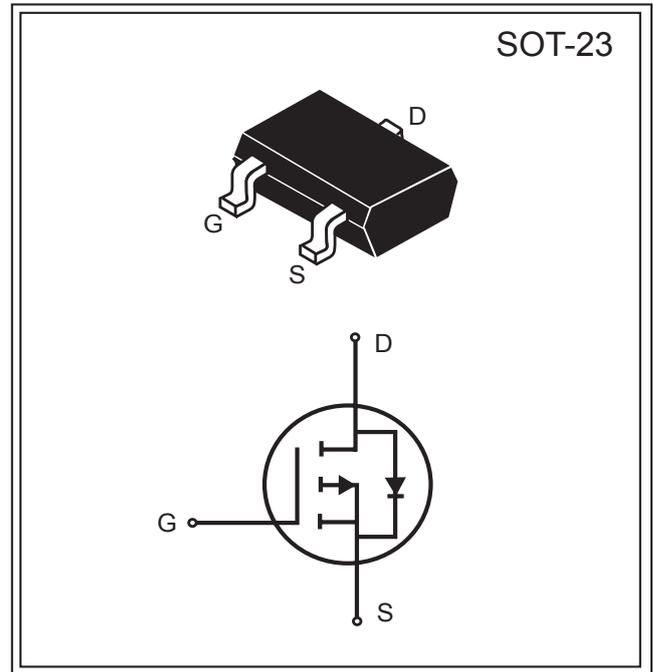


Product Summary

V_{DS} (V)	I_D (A)	$R_{DS(ON)}$ (m Ω) Max
-30V	-3A	75 @ $V_{GS} = -10V$
		100 @ $V_{GS} = -4.5V$

FEATURES

- ◆ Super high dense cell design for low $R_{DS(ON)}$.
- ◆ Rugged and reliable.
- ◆ SOT-23 package.

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	-30	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous @ $T_J = 25^\circ\text{C}$	I_D	-3	A
-Pulsed ^b	I_{DM}	-10	A
Drain-Source Diode Forward Current ^a	I_S	-1.25	A
Maximum Power Dissipation ^a	P_D	1.25	W
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Thermal Resistance, Junction-to-Ambient ^a	$R_{\theta JA}$	100	$^\circ\text{C/W}$
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P-Channel Electrical Characteristics (TA = 25°C unless otherwise noted)						
Parameter	Symbol	Condition	Min	Typ ^c	Max	Unit
Drain-Source Breakdown Voltage	BV _{DSS}	V _{GS} =0V, I _D =-250 μA	-30			V
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} =-24V, V _{GS} =0V			-1	μA
Gate-Body Leakage	I _{GSS}	V _{GS} =±20V, V _{DS} =0V			±100	nA
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} I _D =-250 μA	-1	-1.5	-2.5	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =-10V, I _D =-3A		65	75	mΩ
		V _{GS} =-4.5V, I _D =-2A		87	100	
On-State Drain Current	I _{D(ON)}	V _{DS} =-5V, V _{GS} =-10V	5			A
Forward Transconductance	g _{FS}	V _{DS} =-5V, I _D =-3A		5		S
Input Capacitance	C _{ISS}	V _{DS} =-15V V _{GS} =0V f=1.0MHz		530		pF
Output Capacitance	C _{OSS}			105		
Reverse Transfer Capacitance	C _{RSS}			80		
Turn-On Delay Time	t _{D(ON)}	V _{DD} =-15V, I _D =-1A, V _{GEN} =-10V, R _{GEN} =6Ω, R _L =15Ω		12		ns
Rise Time	t _r			6.5		
Turn-Off Delay Time	t _{D(OFF)}			60		
Fall Time	t _f			25		
Total Gate Charge	Q _g	V _{DS} =-15V, I _D =-3A, V _{GS} =-10V		11		nC
		V _{DS} =-15V, I _D =-3A, V _{GS} =-4.5V		6.5		
Gate-Source Charge	Q _{gs}	V _{DS} =-15V, I _D =-3A, V _{GS} =-10V		1.9		
Gate-Drain Charge	Q _{gd}			2.5		
Diode Forward Voltage	V _{SD}	V _{GS} =0V, I _D =-1.0A		-0.8	-1.2	V

Notes :

- a. Surface Mounted on FR4 Board, t ≤ 10 sec.
- b. Pulse Test : Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
- c. Guaranteed by design, not subject to production testing.

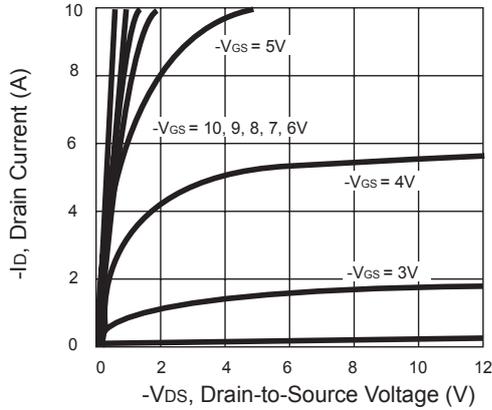


Figure 1. Output Characteristics

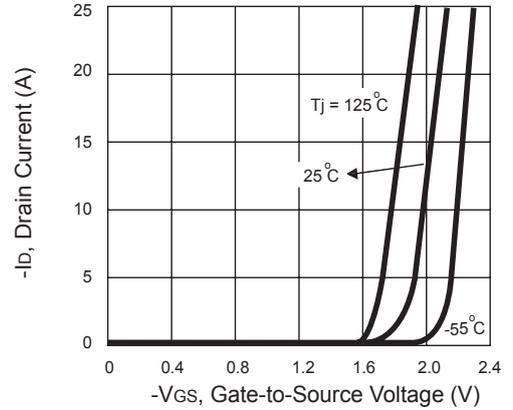


Figure 2. Transfer Characteristics

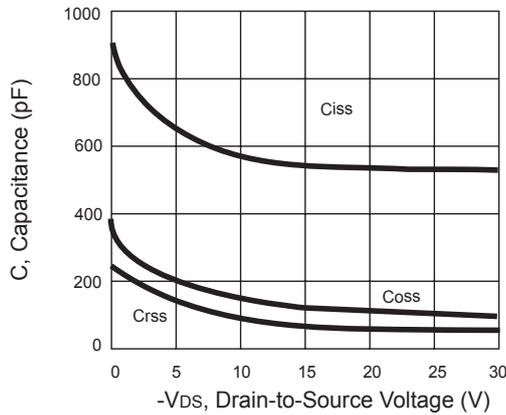


Figure 3. Capacitance

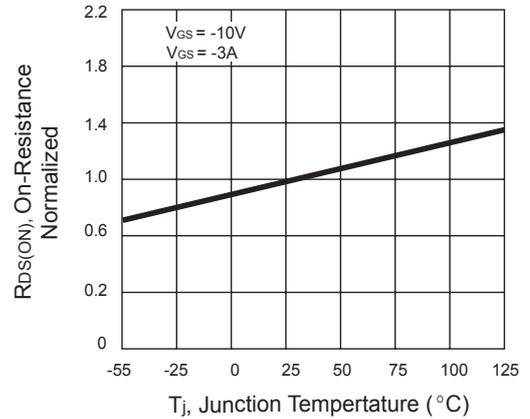


Figure 4. On-Resistance Variation with Temperature

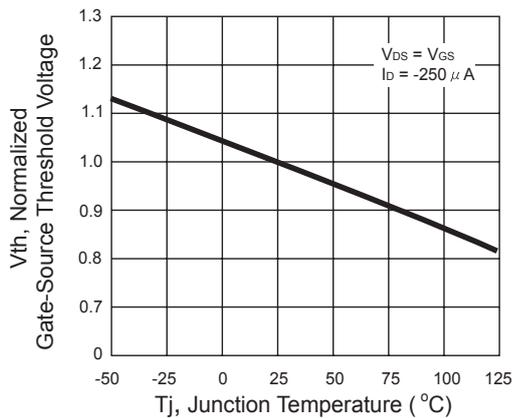


Figure 5. Gate Threshold Variation with Temperature

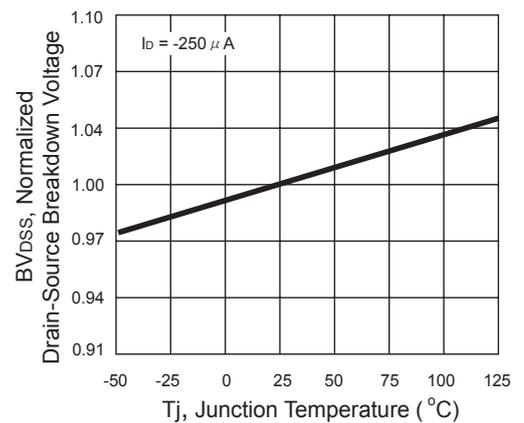


Figure 6. Breakdown Voltage Variation with Temperature

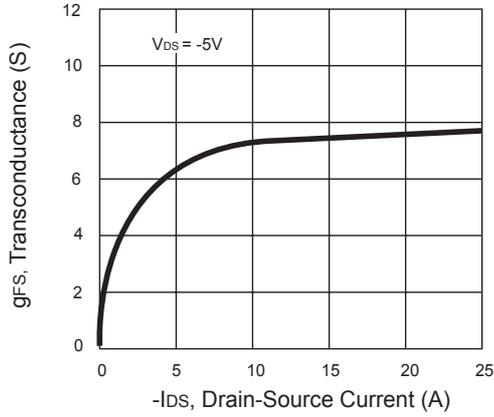


Figure 7. Transconductance Variation with Drain Current

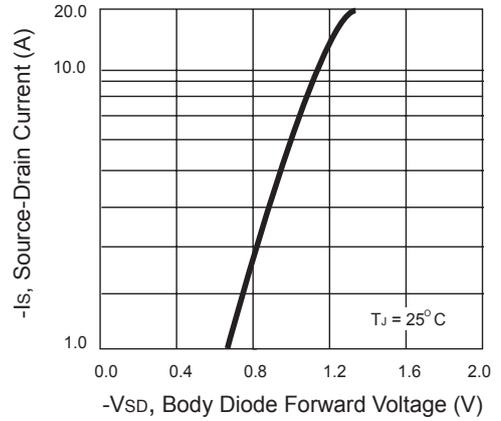


Figure 8. Body Diode Forward Voltage Variation with Source Current

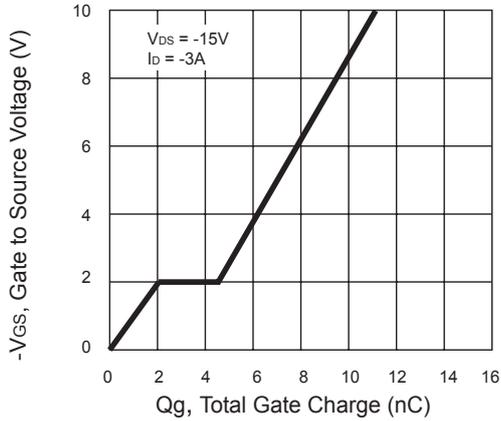


Figure 9. Gate Charge

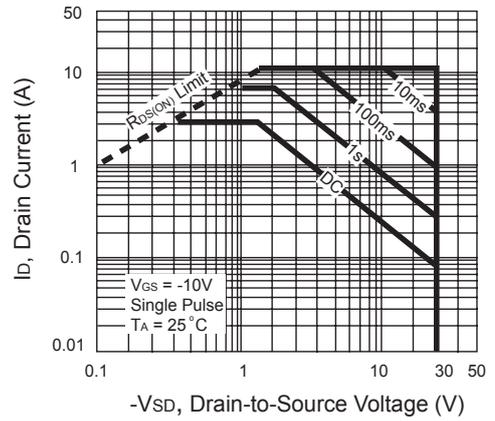


Figure 10. Maximum Safe Operating Area

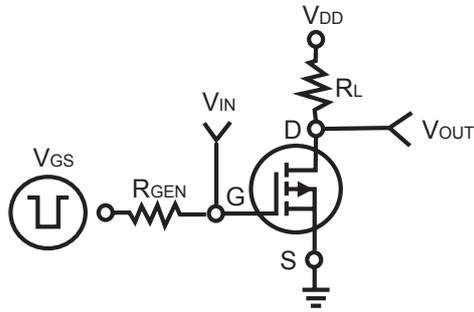


Figure 11. Switching Test Circuit

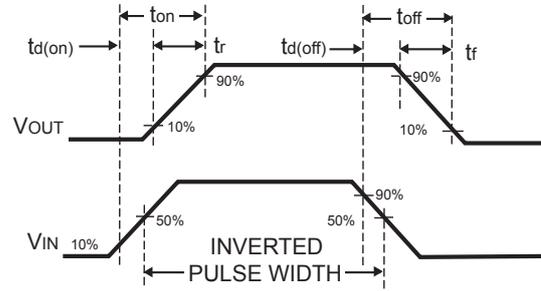


Figure 12. Switching Waveforms

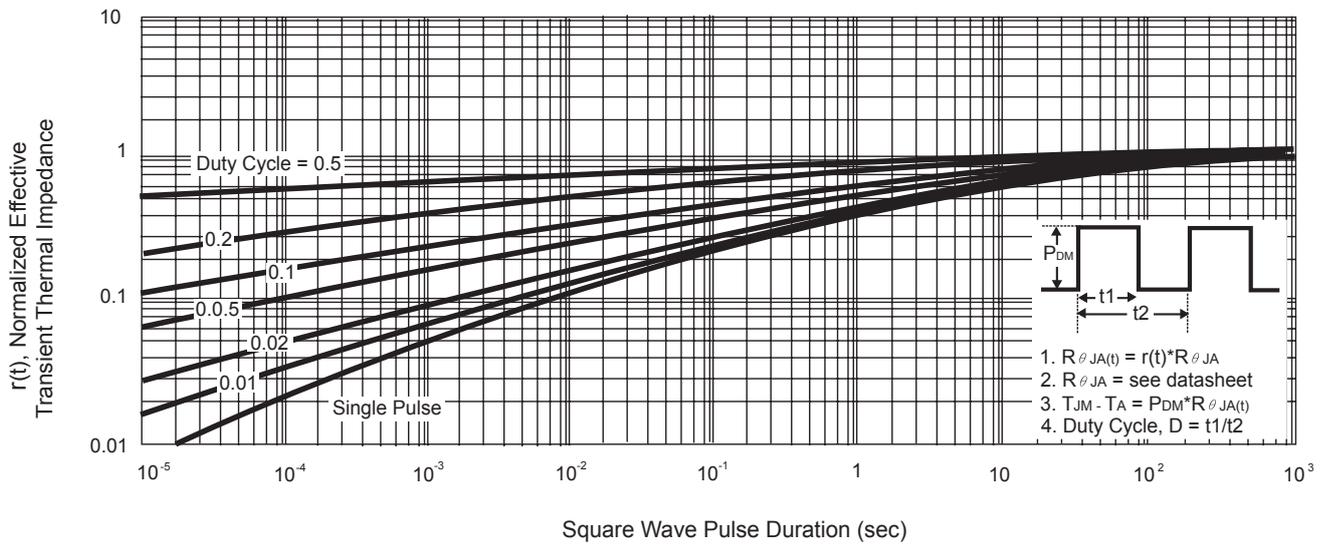


Figure 13. Normalized Thermal Transient Impedance Curve